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Choosing Data Acquisition Boards and Software

Data acquisition boards and software can be used in a variety of computers.

The Basics–Analog-to-Digital (A/D) Conversion, Digital-to-Analog (D/A) Conversion and Digital I/O

Data acquisition boards help you measure real-world information represented by analog signals. The analog signals come from sensors or transducers that convert temperature, pressure, sound, or light into voltage. The electronic sampling of analog signals is called A/D conversion or analog-to-digital conversion. A/D conversion changes real-world analog voltages into digital codes for computer processing and storage.

A complementary process, D/A conversion (digital-to-analog conversion) changes digital data into analog voltages. This permits a computer to drive chart recorders, audio amplifiers, process actuators, and other devices requiring an analog driving voltage.

Many data acquisition boards have both A/D and D/A converters. These permit computerized measurement and control of industrial processes and lab experiments, or recording and playback of audio signals.

To communicate with a device that itself is digital, many data acquisition boards provide digital I/O (digital input/output or DIO) lines. Digital I/O lines can be set for input or output operation in groups called ports, often composed of eight lines.



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Input Ranges

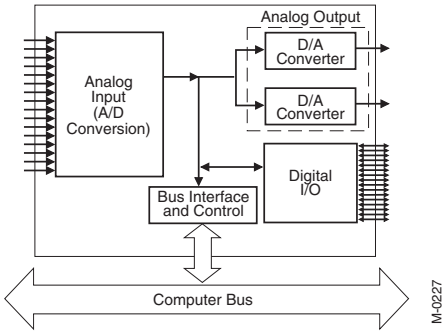
(Unipolar, Bipolar, PGH, PGL, Channel-Gain List)

One of the first things to consider in choosing a data acquisition system is the voltage range to measure. Begin by picking the type of sensor or sensors you will use—strain gauge, thermocouple, microphone, or pressure transducer, for example. Then determine the range of output voltages this sensor will provide (the sensor manufacturer can supply this information).

Input ranges for data acquisition boards are listed in each data sheet. Ranges can be unipolar (0-10 V, for example, for positive voltages only) or bipolar (±10 V, for example, for both positive and negative voltages). Pick a board that covers the range you wish to measure with as little overlap as possible. This will give you the greatest number of data points in the range you want to measure, and therefore the highest accuracy. For example, if the sensor output varies from 1 to 3 V, choose a board with a 0-5 V range. This will give you twice as many valid data points, or twice as much resolution, as an input range of ±5 V or 0-10 V, since the counts for ranges –5 V to 0 V and for +5 V to +10 V would not be used. A lower voltage range (0-2.5V, for example) would not let you measure the full output of the sensor.

Most data acquisition boards provide multiple input ranges by using software-programmable gain amplifiers. Data Translation offers high-level programmable gain (PGH) models, which provide gains of 1, 2, 4, and 8 and can measure inputs as low as 1.25 V with full resolution; and low-level programmable gain (PGL) models that provide gains of 1, 10, 100, and 500 and can measure signals as small as 20 mV with full resolution.

While programmable gain lets you change the input range in software, it has one disadvantage: changing the gain requires an extra software instruction, which can slow high speed data acquisition. The channel-gain list, a feature on



Multifunction data acquisition board with analog input, analog output, and digital I/O subsystems.

Programmable Gain and Input Ranges

	High-Level Gains (PGH)				Low-Level Gains (PGL)			
	1	2	4	8	1	10	100	500
Unipolar	0–10 V	0–5 V	0–2.5 V	0–1.25 V	0–10 V	0–1 V	0–.1 V	0–.02 V
Bipolar	±10 V	±5 V	±2.5 V	±1.25 V	±10 V	±1 V	±.1 V	±.02 V

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Channel-Gain List

Entry	Channel	Gain
0	1	1
1	7	2
2	4	1
3	10	4
4	1	2
5	12	1
6	9	8
7	11	1

M-0228

This channel-gain list samples channels in any sequence you specify at any available gain. You can even sample the same channel (channel one) at different gains.

many Data Translation high-performance boards, provides an elegant solution. The list, actually a small onboard memory buffer, is preloaded with up to 32,768 channel numbers and associated gains. During data acquisition, the channel-gain list automatically selects channel and gain values in hardware without compromising throughput.

Input Types

(Channels, SE/DI, Pseudo-Differential, CMRR, Simultaneous Sampling)

The number of input channels available determines the number of devices you can connect to an A/D board. The number of channels ranges from 4 to as many as 64. However, accessory products like the DT727 Channel Expansion Panel permit compatible A/D board to sample up to 256 inputs (data sheets indicate which products are compatible with the DT727).

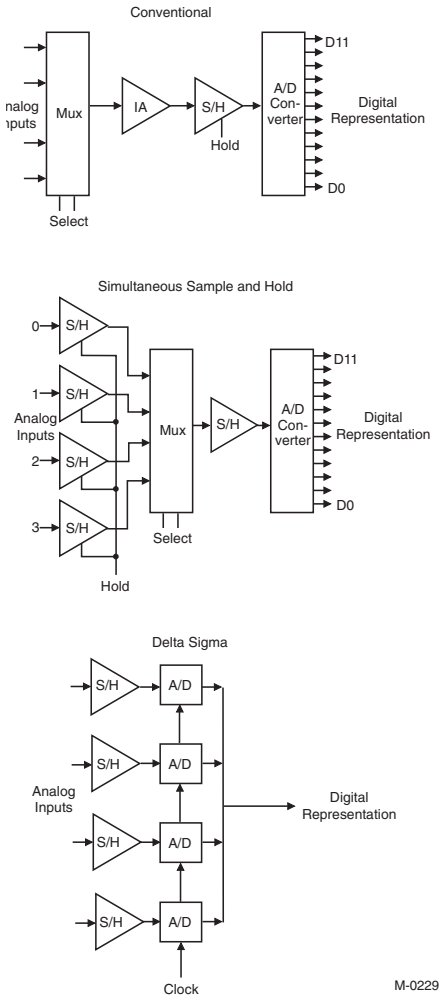
Input channels can be single-ended (SE) or differential (DI), a characteristic you can set on many data acquisition boards. Data sheets present this as "16SE/8DI," meaning you can set the board for 16 single-ended or 8 differential inputs.

Since you get half as many differential inputs as single-ended, why would you ever choose differential? Differential inputs offer a kind of noise immunity called common-mode rejection, abbreviated as CMRR (common mode rejection ratio), and given in decibels or dB. As the name suggests, differential inputs respond mainly to the differences in voltage levels between the two signal leads, and can improve accuracy where long cables, low-level input ranges (<1 V full-scale), or high-resolution converters (>16 bits) are used. Differential inputs are also recommended where input signals from different devices are at different ground potentials—differential inputs can float several volts with respect to one another, to analog ground, and to power ground.

A third type of input, known as pseudo-differential, gives enhanced common-mode rejection in designs where there is not enough space or power for true differential input circuitry. This design provides connections for both the low end and the high end of each input to achieve improved analog common-mode rejection. However, unlike true differential, only one of the signals is actually sampled by the A/D converter.

Some applications, such as destructive testing, involve the simultaneous sampling of several parameters. This requires a type of data acquisition system called Simultaneous Sample and Hold (SS&H). SS&H systems use a separate sample and hold circuit on each input. When sampling begins, all circuits simultaneously switch to hold, freezing each input signal until it can be sampled by the A/D converter. By contrast, conventional data acquisition systems use a single sample and hold circuit, and must sample inputs sequentially.

Simultaneous sampling is also a



Conventional data acquisition systems have a single sample and hold circuit, and sample inputs sequentially. Simultaneous Sample and Hold systems have one sample and hold input for each input, and can thus freeze values on all inputs simultaneously. Delta-sigma designs use a separate A/D converter per channel, and can both simultaneously sample and convert data values on all channels.

characteristic of delta-sigma A/D converters, such as those used on the DT9841 Fulcrum II Series. Since delta-sigma designs use a separate A/D converter per channel, it is possible to sample all inputs simultaneously.

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Using Low-Pass Filters to Eliminate Sampling Errors in A/D Conversion Systems

The Aliasing Phenomenon

Everyone who has gone to the movies has probably seen an example of aliasing. It's what makes the spokes of a wagon wheel or the rotor blades of a helicopter appear to be rotating slowly backwards.

In data acquisition systems, aliasing is a sampling phenomenon that can cause gross errors in results and reduce the accuracy of the data collected by an A/D board, which converts the analog output of a sensor into a digital number that can be read by the acquisition system's computer. It occurs whenever an input signal has frequency components at or higher than half the sampling rate. If the signal is not correctly band limited to eliminate these frequencies, aliases or spurious lower frequency errors recur which cannot be distinguished from valid sampled data. The alias signals are actually at a higher frequency, but are converted by the sampling process to a false frequency below half the sampling rate. For example, with a sampling rate of 1,000 Hz, a signal at 800 Hz aliased to 200 Hz (the false lower frequency). Thus, aliasing is a phenomenon that occurs when a high-frequency component effectively takes on the identity of a lower frequency.

One solution to the aliasing problem is to sample the signal at a very high rate and then filter out the high frequencies with digital techniques. But, such oversampling of data increases system costs by requiring faster A/D conversion for digital processing, more memory, and higher bandwidth buses. It also leads to higher analysis costs by creating more data to process and interpret.

Low-Pass Filtering

A more practical alternative is to limit the bandwidth of the signal below one-half the sample rate with an anti-alias filter, which can be implemented on each input channel in front of the A/D converter. Anti-alias filtering must be done before the signal is sampled or multiplexed, since there is no way to retrieve the original signal once it has been digitized and aliased signals have been created.

To avoid aliasing with a low-pass (or anti-aliasing) filter, two processes actually must occur:

- As dictated by the Nyquist theory, the input signal must be sampled at a rate of at least twice the highest frequency component of interest within the input signal.
- Any frequency components above half the sampling rate (also called the Nyquist frequency) must be eliminated by an anti-alias filter before sampling.

Under ideal conditions, a low-pass filter would exactly pass unchanged all slower signal components with frequencies from dc to the filter cutoff frequency. Faster components above that point would be totally eliminated, reducing the signal disturbance. But, real filters do not cut off sharply at an exact point. Instead, they gradually eliminate frequency components and exhibit a falloff or rolloff slope.

Filter Types

Among the types of filters more commonly used for anti-alias purposes are Cauer (Elliptic) filters, Bessel filters, and Butterworth filters. No filter is perfect, and different types of filters are imperfect in different ways. The optimum filter type for an application depends on which kinds of imperfections are most easily tolerated. Examples of imperfections include phase non-linearity, gain error, passband ripple and droop, and wideband noise.

An extremely sharp cutoff-frequency rolloff makes Cauer filters ideally suited for most anti-alias applications. Cauer filters also have good passband flatness and low wideband noise. But, their non-uniform group delay can cause some overshoot or ringing in time-domain plots if the input signal has sharp transitions. Bessel filters, on the other hand, have a uniform group delay with no ringing or overshoot. They are best suited for time-domain anti-alias applications requiring minimum distortion of rapid slope changes. Butterworth filters are useful when maximum passband flatness is critical. Both Bessel filters and Butterworth filters have a gentler cutoff slope as compared to the Cauer.

Summary

The aliasing phenomenon becomes a problem in A/D conversion systems when an input signal contains frequency components above half the A/D sampling rate. These higher frequencies can "fold over" into the lower frequency spectrum and appear as erroneous signals that cannot be distinguished from valid sampled data. The best approach to eliminating false lower frequencies is to use a low-pass filter, which inhibits aliasing by limiting the input signal bandwidth to below half the sampling rate.

Benefits of Using Low-Pass Filters

Applied to each input channel in front of the A/D board, a low-pass filter can eliminate high-frequency noise and interference introduced prior to sampling. It can reduce system cost, acquisition storage requirements, and analysis time by allowing for a lower sampling rate. A low-pass filter also can serve as an important element of any data acquisition system in which the accuracy of the acquired data is essential.

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Speed

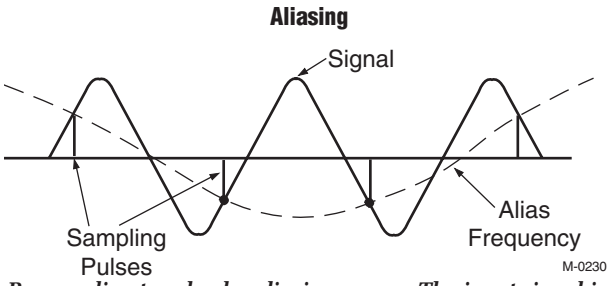
(Throughput, Aliasing, Acquisition Time, Conversion Time, Transfer Time, Overlap)

Speed is always a consideration in data acquisition. In audio, radar, destructive testing, and other high-speed applications, the rate at which data can be sampled—also called throughput—is often the most important factor in choosing a data acquisition board. Data Translation specifies throughput in mega and kilosamples per second (MS/s and kS/s): a board with 250 kS/s A/D throughput can sample inputs 250,000 times per second, and transfer the resulting data to system memory.

In cases where multiple A/D converters are used on a single board, such as the DT9841 Fulcrum II Series, the specified board throughput represents the aggregate, or sum total, of the individual converter throughputs.

According to sampling theory (the Nyquist Theorem), a data acquisition system should sample an input signal at least twice as fast as the input's highest frequency component. That is, to measure a 20 kHz sine wave, the A/D throughput should be at least 40 kS/s.

This avoids an error condition called aliasing, in which very high frequency input components appear in the digital code as erroneous lower frequencies.



By sampling too slowly, aliasing occurs: The input signal is represented by a lower frequency value. This erroneous alias frequency cannot be distinguished from valid data.

Where the input's frequency content is unknown, many users sample at the highest frequency they can, or remove very high frequencies by passing the input through a low-pass filter (such as the anti-aliasing filters built into some data acquisition boards). Boards using delta-sigma converters have very effective built-in anti-aliasing filters due to their high speed sampling and built-in DSP.

Since conventional analog input circuits share a common A/D converter, the number of input channels in use usually affects throughput. If you want to sample four channels at 40 kS/s each, you need a data acquisition system with a throughput of at least 160 kS/s (4 inputs times 40 kS/s/input equals 160 kS/s). Three elements determine A/D throughput: conversion time (the time needed to do the actual A/D conversion); acquisition time (the time needed by associated analog circuitry the multiplexer, amplifier, and sample and hold—to acquire a signal accurately) and transfer time (the time needed to transfer data from the board to system memory). (Issues affecting transfer time can be complex; these are discussed in a later section on data transfer.)

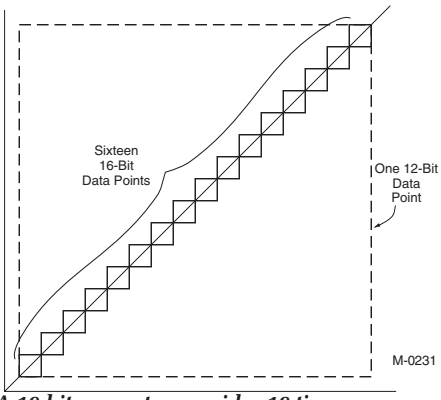
Normally, a board first acquires a signal and then converts it. Throughput is determined by the sum of the conversion time and the acquisition time. High-speed Data Translation boards (such as the DT3010 Series and DT300 Series) increase throughput by overlapping the acquisition time on one sample with the A/D conversion time of the previous sample. In effect, the A/D circuitry handles two signals at one time.

The high gains associated with .1 and .02 V input ranges necessarily reduce throughput. Like any amplifier, the onboard programmable gain amplifier's bandwidth (or speed) reduces as its gain increases. Because of this, many data acquisition boards uniformly extend the acquisition time for all gains and so reduce throughput from 50 kS/s, for example, to 2.5 kS/s.

Resolution, Ranges, and Bit Weights

				LSB Value			
Resolution (bits)	Number of Counts	dB	% of Range	±10 V Range	0-10 V ±5 V Range	0-2.5 V, ±.1.25 V Range	±.02 V Range
8	256	48.2	.39%	78 mV	39 mV	9.8 mV	.16 mV
10	1,024	60.2	.098%	20 mV	9.8 mV	2.4 mV	.04 mV
12	4,096	72.2	.024%	4.9 mV	2.4 mV	.61 mV	.01 mV
16	65,536	96.3	.0015%	.31 mV	.15 mV	.04 mV	.0006 mV
20	1,048,576	120.4	.000095%	—	—	—	—
24	16,777,216	144.5	.000006%	—	—	—	—

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A 16-bit converter provides 16 times as many points as a 12-bit converter operating over the same range: $\frac{2^{16}}{2^{12}} = \frac{65{,}536}{4{,}096} = 16$

Accuracy

(Resolution, LSBs, ENOB, THD)

Accuracy—how closely the binary code matches the incoming or outgoing analog signal—is also important. It can be a deciding factor when the analog signal contains much information (as an audio signal does), or when you must examine a small part of the range in great detail (as in chromatography applications). Data Translation products typically specify accuracy in terms of system error. The unit is percent of full-scale range. System error takes in all sources of error, including analog noise, system nonlinearities, and reference variation.

The major component of A/D or D/A accuracy, and its limiting factor, is resolution. Given in bits, resolution determines the number of counts or number of binary numbers used to represent the analog signal. Twelve-bit converters, for example, can assume 212 different states and so divide their ranges into 4,096 pieces. This translates into digital code that tracks the analog signal to within .024% of the range. More bits yield exponentially higher resolution.

Another measure of resolution is the least significant bit or LSB—the smallest change in the analog signal that the digital code can represent. LSBs are specified both as a percent of range and as the smallest voltage change that can be resolved on a particular range.

While these dc accuracy measurements are crucial, it is the ac characteristics of an A/D circuit that determine how accurately it digitizes complex waveforms. Errors introduced by nonlinearities, aperture uncertainty, noise, quantization, and other sources of signal distortion are involved in determining the Effective Number Of Bits (ENOB) an A/D circuit is capable of resolving in the frequency domain. Maximizing a board's ENOB, or making sure its ac performance is as good as its dc performance, involves meticulous system-level design, which considers the move from a data acquisition board an intricate analog component. Data Translation calculates ENOB according to the following formula:

$$\text{ENOB} = \frac{(S/(N + D)) - 1.76)}{6.02}$$

One of the most common effects of poor A/D circuit design is the introduction of harmonic distortion in the analog signal path. Total Harmonic Distortion (THD) is a ratio of the sum of the harmonics of the fundamental frequency of the input signal to the fundamental frequency itself.

A circuit with high THD likely has a design weakness that produces these distortion errors. To minimize THD, the circuit design at the analog input must be flawless, eliminating nonlinearities with respect to the ac characteristics of the input signal.

A/D Converter Types

(Successive Approximation, Flash, Integrating, V/F, Delta Sigma)

The heart of a data acquisition board is its A/D converter. No single converter type can meet the signal-acquisition needs of all applications equally well, and several different classes of converters exist. Each has its own particular advantages and disadvantages.

A typical A/D converter contains an analog multiplexer that chooses one from up to 16 analog input signals; an amplifier that buffers the analog signal and may also apply gain to boost its voltage level; a sample and hold circuit that holds the input signal constant during the actual conversion; and an A/D converter that changes the analog signal into a digital code.

Successive-approximation converters

Pacer Clock Characteristics

Target Frequency	400 kHz Oscillator (2.5µs)			5 MHz Oscillator (.2µs)		
	Best Fit	Next Higher	Next Lower	Best Fit	Next Higher	Next Lower
15 kHz	14.8 kHz	16 kHz	14.3 kHz	14.97 kHz	15.02 kHz	14.93 kHz
50 kHz	50 kHz	57 kHz	44 kHz	50.0 kHz	50.5 kHz	49.5 kHz
150 kHz	133 kHz	200 kHz	100 kHz	147 kHz	152 kHz	143 kHz
250 kHz	200 kHz	400 kHz	100 kHz	250 kHz	263 kHz	238 kHz

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Data Conversion Technologies

	Conventional	Delta Sigma
A/D Subsystem		
Overview	Excellent for measuring dc and very high speed signals; excellent dc characteristics; single-point acquisition and real-time response; high speed dynamic performance	Excellent for measuring ac signals; high-accuracy ac measurement with built-in anti-aliasingfi lter
Configurations	12 or 16 bits; 7.5 kHz to 1 MHz, aggregate throughput	16 bits at 52 kHz per channel 24-bits at 100 kHz per channel
Architecture	One A/D with multichannel multiplexer	One delta-sigma A/D per channel
Simultaneous Sampling	Requires special SS&H circuitry; available on some models	All models
Anti-Aliasing Filters	Available on some models; typically uses 4-pole analogfi lter; cutoff frequency = 5, 10, or 20 kHz; –24 dB at twice cutoff frequency rate)	All models; digital filter provides "Brick Wall'fi ltering (–110 dB at 1.2 times cutoff frequency) automatically tracks speed of A/D converter
DA Subsystem		
Overview	Typically two 12 or 16-bit DACs; excellent dc characteristics	Typically two 16-bit delta-sigma DACs; excellent ac characteristics
Output Filters	Not available on all models; when available, typically 2-pole analog; cutoff frequency = 20 kHz; –12 dB at twice cutoff frequency	All models; uses a combination of digital and analog filters to reduce glitches and other noise sources more than 80 dB

feed various binary codes into a D/A converter and then use an analog comparator to compare the resulting analog output with the sampled signal. Using what is essentially a binary search methodology, the binary code eventually settles on a number that most closely represents the value of the analog input signal. Successive-approximation A/Ds are relatively accurate and fast, although they can exhibit some nonlinearities and missing codes.

Parallel, or flash encoding is the fastest A/D conversion method. The input signal is fed to 2^{n-1}(where n equals the number of bits of resolution) analog comparators whose reference inputs are derived from equidistant taps off a linear resistor ladder. A priority encoder generates a digital output corresponding to the highest comparator activated by the input voltage. Unfortunately, flash encoders are prohibitively bulky and expensive for most applications, especially those requiring high resolution.

Several techniques, including dual-slope, use a capacitor to keep track of the ratio of an input signal to a voltage reference. These methods all average, or integrate, the input signal for a fixed time interval for each sampled measurement using a current source and a capacitor. Such integrating A/D converters have an important advantage: the output is proportional to the average input voltage over the integration time. By choosing a sampling interval that is a multiple of the power-line period, the converter becomes insensitive to 60 Hz "hum" (and its harmonics) on the input signal. The main disadvantage is that integrating A/Ds are relatively slow.

Voltage-to-frequency (V/F) methods convert an analog input voltage to an output pulse train whose frequency is proportional to the input level. V/F converters are relatively inexpensive and are useful when the converter output is to be used to digitally transmit a signal over a cable via carrier-signal modulation.

Delta-sigma A/Ds, such as those used in the DT9841Fulcrum II Series, use fundamentally different conversion techniques optimized for tracking ac signals over time. Delta-sigma A/Ds typically use a 1-bit converter that greatly oversamples the input signal. Using circuitry built into the A/D converter, the resulting bit stream is accumulated and decimated to provide the desired resolution and word-sampling rate. Since they are mostly made up of digital components, delta-sigma A/Ds exhibit exceptionally good ac performance, including noise, linearity, drift, monotonicity, accuracy, aliasing, and resolution characteristics.

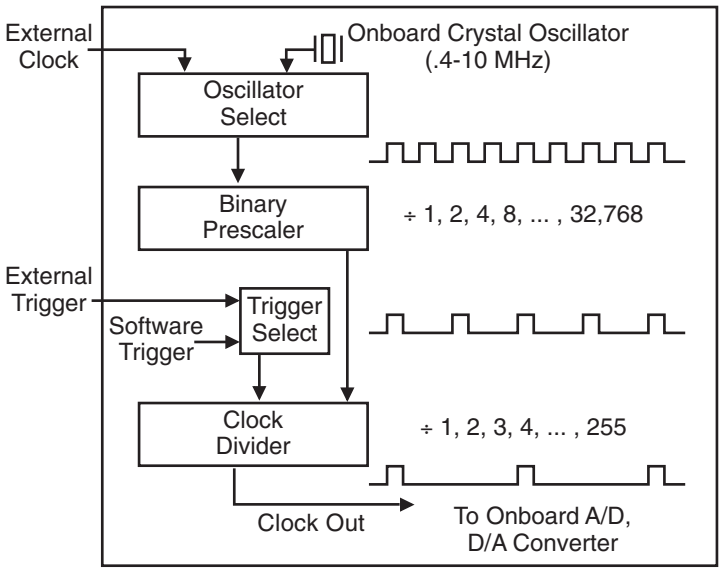
Another benefit of delta-sigma A/Ds is built-in digital filtering that effectively eliminates aliasing. Very rapid "brick wall" attenuation of input frequencies above the Nyquist frequency (half the sampling rate) is automatic.

The only disadvantage of delta-sigma converters is an inherent group delay. For example, each data point is effectively an average
of 18 conversion periods, an insignificant characteristic in most open-loop signal processing and analysis applications, but possibly of concern in real-time control situations.

Analog Outputs

(Independent DACs, Settling Time, Deglitched Outputs, Reconstruction

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A typical pacer clock circuit can accept an onboard external frequency source, and a hardware or software trigger, and divides the frequency source by both a prescaler and a divider.

Filters)

Most Data Translation analog output circuits have a separate D/A converter (DAC) and data buffer for each channel. This permits outputs to be updated one-at-a-time or simultaneously (to change both channels of an XY plotter, for example). When two DACs are updated at a time the total throughput can be twice the single-channel throughput.

The major component in DAC throughput is settling time. While a DAC's output begins to change as soon as it receives a new data value, the output is valid only after the analog circuitry has stabilized. Settling time is the period a DAC needs to reach rated accuracy after receiving an output change. Full-scale settling time is actually a worst-case value. Smaller than full-scale changes settle in less time. Settling time varies inversely with the size of the output change. Settling time is specified in microseconds (µs).

To provide a cleaner analog output signal, some Data Translation boards (DT9834 Series, for example) use a deglitching circuit. DACs produce glitches: rapid, high energy pulses caused by minute timing differences (skew) in the converter's data switches. The deglitching circuit holds the output constant for a brief period, then reconnects the DAC output after the glitch has passed.

Another way of reducing unwanted noise from an analog output is to pass the output through a low-pass reconstruction filter; this is a feature of the DT9841 Fulcrum II Series boards. The delta-sigma type DACs used in the DT9841 Fulcrum II Series construct an analog output signal by using an 8x interpolation filter followed by a 64x oversampling converter. This method automatically interpolates between data points to smooth the resulting analog output, giving the effect of much higher resolution. It also provides very steep "brick wall" filtering of unwanted output noise.

Clocks, Triggers, and Counter/ Timers

(Oscillator, Divider, Prescaler, Trigger)

To perform multiple conversions automatically at precisely-defined time intervals, many data acquisition boards are equipped with one or more pacer clock circuits. Where present, the pacer clock typically starts all conversions. Boards that permit simultaneous A/D and D/A operation.

Pacer clocks are made up of a frequency source (either an onboard free-running oscillator between 400 kHz and 10 MHz, or a user-supplied signal) and a divider network that steps the frequency source down to more usable values—from less than 1 Hz to the maximum throughput of the board. The frequency source is also called the clock's base frequency, and determines the granularity or distance between available settings. Higher base frequencies offer finer granularity, especially at high sampling frequencies. For example, values for a 400 khz oscillator are 2.5 µs apart; those for a 5 MHz oscillator are .2 µs apart. Dividers can typically be set for any value within an 8- or 16-bit range. Some designs also use a binary prescaler before the divider to extend the clock's range.

Pacer clocks are started by triggers: either by a program instruction (a software trigger), or on receipt of a digital pulse or analog voltage at the board's connector (an external trigger). External clock frequency sources and external triggers help you synchronize data conversions with off-board events. An external trigger can serve as a gate to enable conversion, while with each tick, the external frequency source starts a new conversion. External frequency sources can also be used to produce clock frequencies that cannot be achieved with the onboard oscillator.

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Converters on delta-sigma A/D and D/A converters, such as those used on Data Translation's DT3818 (Fulcrum Delta Sigma) Series, have an inherent "group delay" that introduces a latency period between the time a sampling window opens and the time valid data is actually available.

Delta-sigma A/D converters do not deliver the first valid data sample until 18 sample clocks after the start-to-acquire signal is given (the A/D group delay is 1/fs x 18 µs). This delay is analogous to the group phase delay introduced by analog front end antialiasing circuits. Delta-sigma DACs have a 33-clock group delay.

Many data acquisition boards also contain general purpose counter/timer circuits. These typically consist of several counters (digital circuits that count pulses) and frequency source that, when used with a counter, forms a precision timer. Counter/timers can be used in dozens of configurations. Counters can be used singly or in combination with other counters, external or internal frequency sources, and gates. While extremely flexible, counter/timers can be difficult to use without software that easily configures the circuitry for commonly-used functions.

Data Transfer Methods

For high speed data acquisition, the method of data transfer is just as important as the speed of the A/D or D/A converter. Data Translation manufactures boards for different I/O buses, and differing methods of data transfer (the means by which data values are transferred between the board and computer memory).

USB

The Universal Serial Bus (USB) is a new standard for connecting PCs to peripheral devices, such as printers, mice, and modems, and was developed to make more low-cost ports available for the increasing number of these devices. USB ports are standard on most PCs. Add an external hub, and you can run up to 127 peripherals off one USB port. With the backing of Intel, Microsoft, and hundreds of other computer and peripheral companies, USB is quickly becoming a new industry standard.

USB is a natural choice for data acquisition. USB modules, such as the DT9800 Series, reside outside the PC and install with a single cable so installation is easy. Modules can be "hot-swapped", or plugged and unplugged while the PC is on, making them useful for many data acquisition applications. And with a theoretical 480 Mbps bandwidth, USB can handle all but the highest data rates.

PCI Bus for High-Performance Data Transfers

Along with the cost-maturation of Pentium-class PCs has come a rise in the use of the PCI (Peripheral Component Interconnect) bus for high-speed data acquisition. PCI's 132 MB/s, 32-bit data pathways are more than an order of magnitude faster than the ISA Bus, making the bus ideal for high-performance data acquisition boards such as Data Translation's DT3010 Series.

In fact, the PCI Bus is fast enough so that all subsystems on the board—A/D, D/A, and digital I/O—can operate simultaneously, at full throughput, without interruption, up to the limits of available system memory! Not only does the PCI Bus simplify hardware installation through its plug-and-play facilities, its direct accesses to memory through the system's PCI controller allows a data acquisition board to directly access system memory at the full speed of the PCI Bus, using fast programmed I/O operations, without incurring the cost of special DMA hardware.

Onboard Memory

Another very high-speed method of data transfer is possible when the data acquisition board has extensive onboard memory. This transfer to onboard memory can occur at any rate you desire, limited only by the speed of memory and control logic on the board. To speed data transfer to the host bus, many boards provide built-in FIFO data buffers. This onboard memory permits the board to transfer large amounts of data to or from the host at one time, overcoming bus contention and latency problems.

Data Integrity

(Continuous Performance)

If you are scanning channels in a particular sequence, missing one data point can cause all subsequent values to be misinterpreted. Short-lived, very high-speed phenomena may show up in only a few samples; missing one point can cause you to mistake an important event for noise or statistical error.

To assure data integrity, Data Translation has developed boards and software, that support continuous performance, gap-free data transfers to and from memory or hard disk. Many additional methods have been developed over several years to accommodate different computer buses, board architectures, and throughput requirements. Continuous performance data acquisition is provided by the combination of software and hardware.

All continuous performance products share the ability to transfer data streams of arbitrary length to and from memory or

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hard disk at high speed—up to the maximum throughput of the board. Data acquisition using these products is typically limited in duration only by the amount of available memory or hard disk space. To assure that you have not missed a data value, most continuous performance boards contain error flagging circuitry that sets any time a new data value overwrites a previous value.

Software

Data Translation boards are supported by a variety of software products, aimed at a wide range of users. DT Measure Foundry is a powerful application builder software package that allows a user to easily program. The DataAcq SDK and DTx-EZ packages are for programmers wishing to create custom applications. Many popular third-party application software products such as, LabVIEW, MATLAB, and TestPoint also support Data Translation boards.

Our modular DT-Open Layers architecture isolates application software from hardware specific commands, automatically ensuring complete portability of DT-Open Layers compliant application code. This application-level hardware independence allows hardware upgrades without reprogramming—your software development investment is protected.

Our DTx-EZ ActiveX® Controls for Visual Basic and Visual C++ is a set of controls for data acquisition and display. DTx-EZ is also compliant with DT-Open Layers and provides controls



M-5890

The DT9800 Series of USB function modules offer a new option for data acquisition.

that greatly simplify setup of the data acquisition board and they acquire and display data values.

All Data Translation PCI and USB data acquisition boards ship with the Data Acquisition, Omni CD, a free software bundle. The Omni CD includes:

- Quick DataAcq™ – ready-to-run application
- DataAcq SDK™ – software development kit
- Scope instrument application
- Device drivers for PCI and USB boards
- DT Measure Foundry evaluation
- Documentation and example program code

High Performance Data Acquisition

(Simultaneous A/D and D/A, Real-Time DSP)

At the outer reaches of data acquisition stand a few advanced techniques developed by Data Translation to overcome specific computer limitations.

Simultaneous A/D and D/A transfers are possible on some high-speed multifunction boards, a feature very convenient for process control, audio recording and playback, and so on. The methods used vary from board to board, and may involve use of multiple DMA channels, an onboard chip that timeshares a single data bus, or onboard input and output data buses each connected to a separate DT–Connect or onboard processor port.

High-speed data transfer can present some daunting data storage and processing problems: at 1 MHz, every second you accumulate one million 16-bit data words! High-speed, real-time, application-specific DSP processors built into data acquisition boards can provide the solution.

For real-time applications that require absolutely deterministic, simultaneous data collection and analysis, Data Translation's Fulcrum II family tightly couples high-performance A/D and D/A front-end circuits with the industry's leading floating-point digital signal processor from Texas Instruments. The result is a deterministic acquisition/ analysis system that operates independent of the host computer, freeing up the PC for display and supervisory tasks.

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Board Features Supported by DT-Open Layers Software

	Continuous Transfer				Simultaneous A/D & D/A	
	1-Channel DMA	2-Channel DMA	Other	Max Throughput	High Speed Continuous	Single Conversion
DT01-EZ, DT16-EZ	✔	—	—	Board-Maximum	—	✔
DT21-EZ, DT23-EZ, DT24-EZ, DT24-EZ-PGL	✔	✔	—	Board-Maximum	—	✔
DT31-EZ, DT34-EZ	✔	✔	—	Board-Maximum	✔	—
DT300 Series	—	—	✔	Board-Maximum	—	✔
DT330 Series	—	—	—	System-Dependent	—	✔
DT335	—	—	—	System-Dependent	—	✔
DT340	—	—	—	System-Dependent	—	✔
DT2801 Series	✔	—	—	Board-Maximum	—	✔
DT2811-PGH, DT2811-PGL, DT2814, DT2815, DT2817, DT2819	—	—	—	<500 kS/s	—	DT2811 only
DT2812, DT2812-A	✔	—	—	Board-Maximum	—	✔
DT2821 Series	—	✔	—	Board-Maximum	—	✔
DT2831 Series	D/A only	✔	—	Board-Maximum	—	✔
DT2839	✔	✔	—	>950 kS/s	✔	—
DT3001, DT3002, DT3003, DT3004, DT3005	—	—	✔	Board-Maximum	✔	—
DT3010 Series	✔	—	—	1.25 MS/s	✔	✔
DT7101, DT7102	—	—	✔	Board-Maximum	—	✔
DT9800 Series	—	—	✔	Board-Maximum	✔	—
DT9834	—	—	✔	Board-Maximum	✔	—

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