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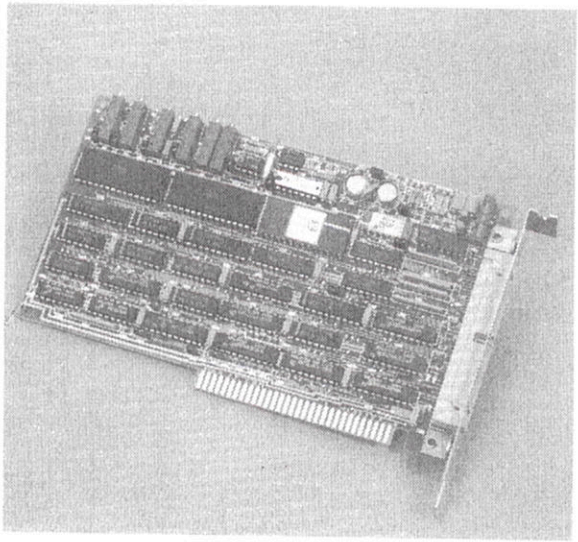
Find the *Measurement Computing / Data Translation DT2811-PGH* at our website: *Click HERE*

DATA TRANSLATION®

IBM Personal Computer
ANALOG AND DIGITAL I/O BOARD
DT2811 Series

FEATURES

- IBM® PC/XT/XT-compatible board featuring 20kHz A/D, two 50kHz D/As, 8 digital input lines, 8 digital output lines, and programmable pacer clock
- A/D features
  - 20kHz throughput
  - 12-bit resolution
  - Programmable gains of 1, 2, 4, 8 (DT2811-PGH)
  - Programmable gains of 1, 10, 100, 500 (DT2811-PGL)
  - 16SE/8DI channels
- D/A features
  - 50kHz throughput per DAC
  - 2 independent DACs
  - 12-bit resolution
  - Outputs are short-circuit protected
- Digital I/O
  - 8 lines of digital input
  - 8 lines of digital output
- Support for four-level bus interrupt
- I/O compatible with DT2801 Series boards to ensure pin-compatibility with wide range of screw terminal panels and signal conditioning products
- Optional subroutine library (LPCLAB™) and third party application software packages
- Shipped with comprehensive user manual which includes programming instructions



M-4575

Figure 1. The DT2811-PGH analog and digital I/O board for the IBM PC/XT/AT.

PC

TABLE 1. DT2811 FEATURES

MODEL	ANALOG INPUTS				ANALOG OUTPUTS		DIGITAL FUNCTIONS	
	Channels	Resolution (bits)	Input Ranges	Thruput (kHz)	Channels	Thruput (kHz)	I/O Lines	Pacer Clock
DT2811-PGH	16SE/8DI	12	0–.625,1.25,2.5,5V ±.31,.625,1.25,2.5,5V	20	2	50/chan	8 In 8 Out	√
DT2811-PGL	16SE/8DI	12	0–.01,.05,.5,5V ±.005,.01,.05,.5,5V	20	2	50/chan	8 In 8 Out	√

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DESCRIPTION

The DT2811 Series are low cost analog and digital I/O boards for the IBM PC/XT/AT featuring 20kHz D/A throughput at 12-bit resolution to fit a variety of laboratory, industrial, or control applications.

The DT2811 Series's analog-to-digital (A/D) subsystem has a throughput of 20,000 12-bit samples per second, and is jumper-selectable for sixteen single-ended or eight differential analog inputs. The DT2811-PGH has software-programmable gains of 1, 2, 4, and 8, while the DT2811-PGL has software programmable gains of 1, 10, 100, and 500 (throughput at gains of 100 and 500 is 2.5kHz). Full scale input ranges of 0 to +5V, ±5V, and ±2.5V are available.

The DT2811 Series's digital-to-analog (D/A) subsystem consists of two 12-bit D/A converters that can support analog data output at up to 50kHz per converter. DT2811 Series boards also contain eight lines of digital input and eight lines of digital output as well as a programmable clock which can be used to initiate A/D conversions.

Interrupts on completion of an A/D conversion or whenever an error occurs in A/D operation can be enabled or disabled under program control. The board can be assigned to interrupt level 2, 3, 5, or 7 on the host IBM PC.

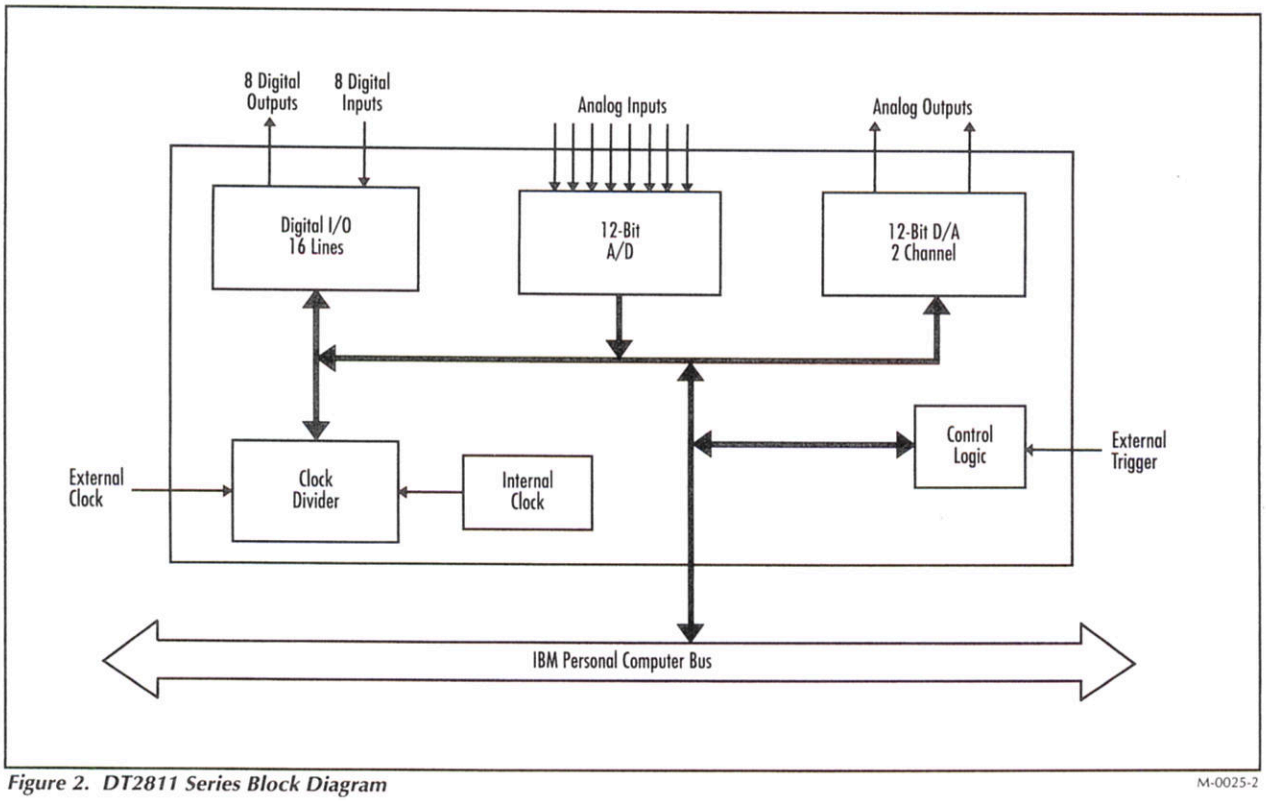


Figure 2. DT2811 Series Block Diagram

M-0025-2

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PRINCIPLES OF OPERATION

DIO SECTION

The digital I/O section of the DT2811 Series board is controlled by programmed I/O (PIO) reads and writes to the DIO register. Data transfer can occur at any time asynchronously. That is it is possible to output to or input from the DIO section at any time without having to check any status bits. Both input and output values are latched on the DT2811 Series board when the read or write command is issued.

D/A SECTION

The D/A section is controlled by programmed I/O writes to the four DAC registers. Data values are output to the DACs singly. The actual D/A conversion does not take place until the high byte of data is written to either D/A converter DAC0 or DAC1

A/D SECTION

The A/D section of the DT2811 Series board has different sources of signals that initiate A/D conversions. The naming convention used for the following discussion is as follows. The frequency source is the output of the Timer/Counter Register that divides either the onboard 600kHz clock or an external clock provided by the user. The frequency source becomes the A/D clock once enabled by an A/D trigger. An A/D trigger is the event that enables the A/D clock and can be either software or external. The A/D clock is the signal that initiates A/D conversions.

There are four modes of operation. Mode 0 is used for single A/D conversions. A/D conversions begin when the channel number and gain value are selected by a write to the A/D Gain/Channel Register. In mode 0, subsequent conversions take place on a newly selected gain and channel by issuing the channel/gain select once the previous A/D conversion has finished and the data has been read.

Mode 1 supports repetitive A/D conversions using the internal pacer clock. The mode is selected by writing to the A/D Control/Status Register and selecting mode 1. Next, the clock divisor is selected by writing to the programmable clock register. The A/D clocks are enabled by writing to the A/D Gain/Channel Register to select the input channel to be sampled. This selection causes a software trigger to be issued, initiating A/D conversions at a rate determined by the onboard clock and the selected clock divisor. When A/D Done sets (or when an interrupt is issued), the A/D data should be read.

Mode 2 is the same as mode 1 except the A/D conversion process (at a rate based on the internal frequency source) is started after an external trigger is received.

Mode 3 is the same as mode 2 except that an external clock supplied by the user is used to initiate conversions at a rate determined by the frequency of the external clock and the value of the clock divisor.

In all modes, a user program can determine when to read the converted A/D data by checking A/D Done (bit 7 of the A/D Control Status Register). Alternatively, the board can be set to interrupt on A/D Done, and data can be read using an interrupt handler routine.

In modes 1, 2, and 3, A/D conversions continue until an error occurs, or until the A/D conversion circuitry is disabled by writing to the A/D Control/Status Register and selecting mode 0.

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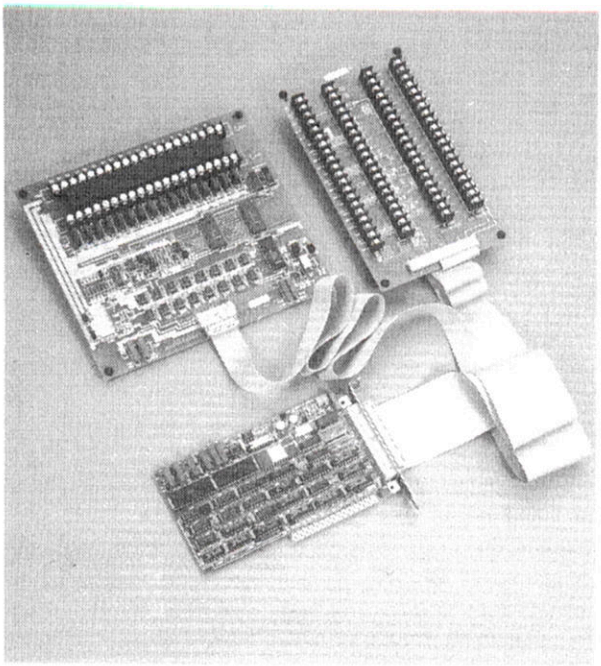


Figure 3. For thermocouple, RTD, or strain gauge inputs, the DT752 and DT756-Y combination provides 16 differential inputs, gains to 200, and thermocouple cold-junction compensation. M-4563

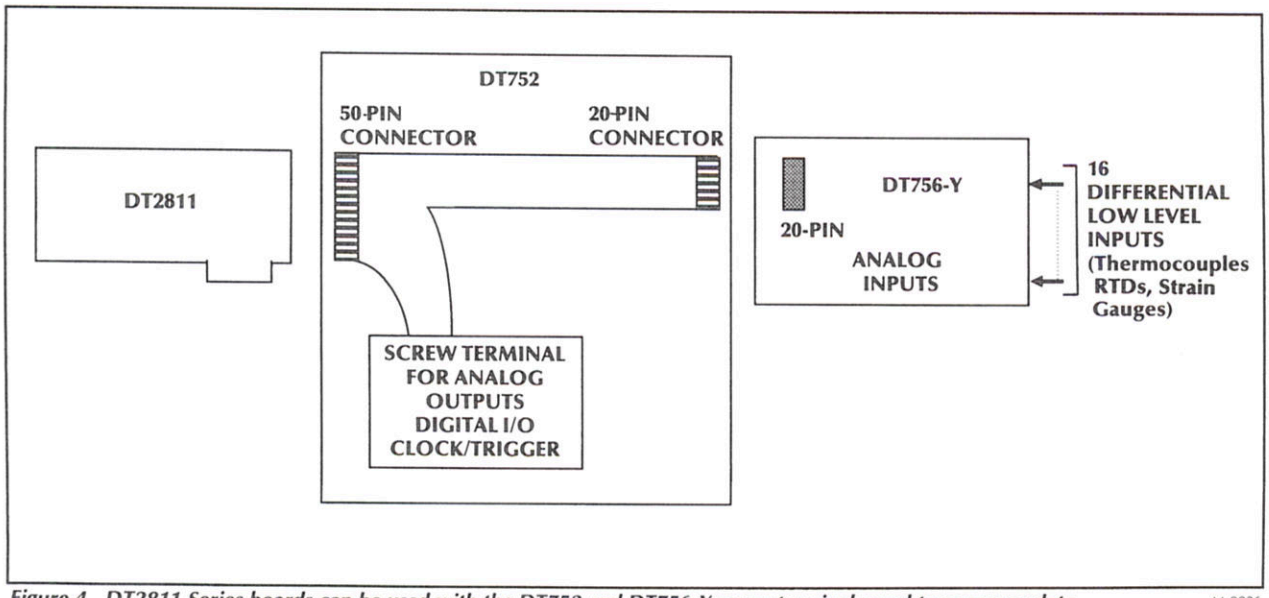


Figure 4. DT2811 Series boards can be used with the DT752 and DT756-Y screw terminal panel to accommodate inputs from thermocouples, RTDs, and strain gauges. M-0026

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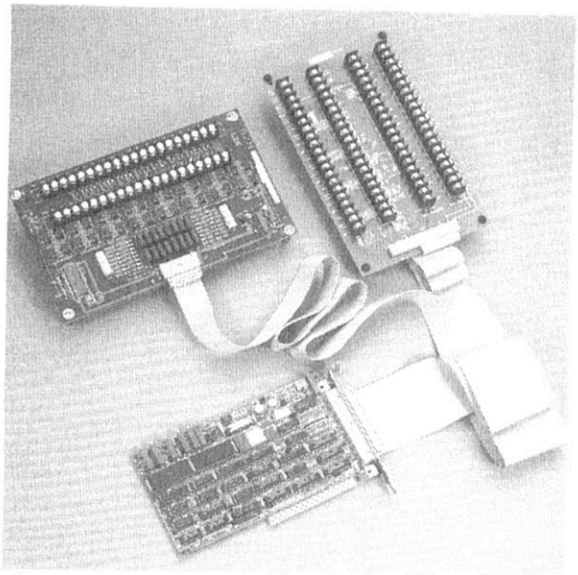


Figure 5. The DT752 and DT709-Y screw terminal panels permit up to 16 differential inputs to be connected to a DT2811 Series board. M-4564

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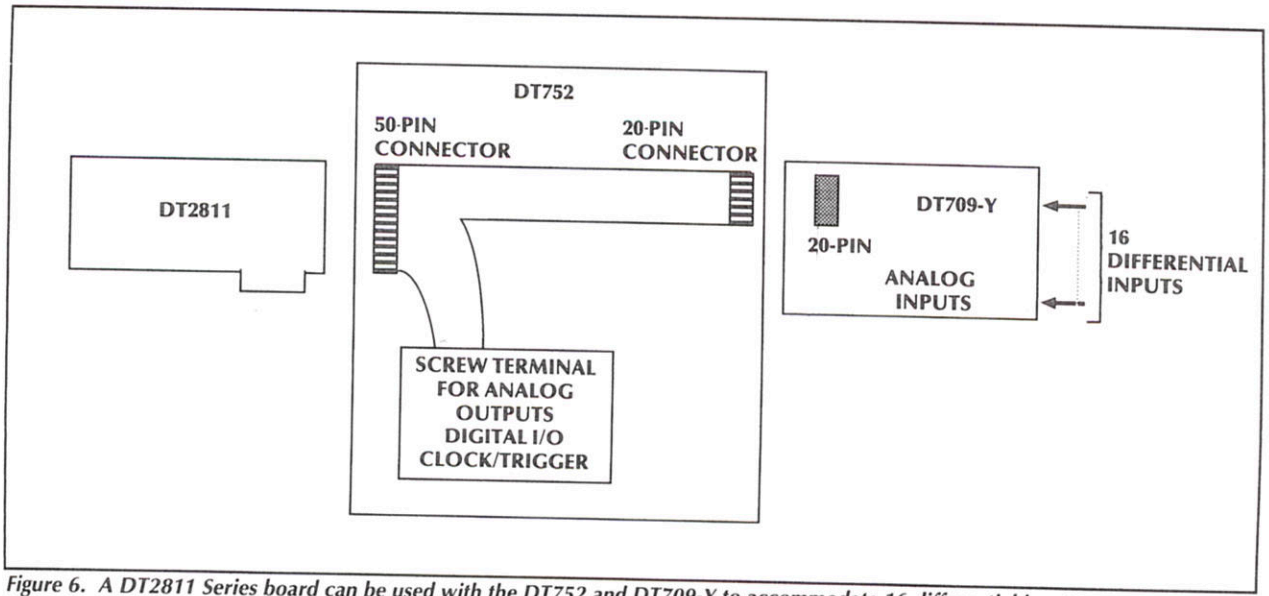


Figure 6. A DT2811 Series board can be used with the DT752 and DT709-Y to accommodate 16 differential inputs. M-0027

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EXAMPLE PROGRAMS

Also shipped with each DT2811 Series board is a group of example programs in BASIC. These programs show typical programming of the board. There is an example program for each of the four A/D modes of operation, for D/A operation, and for digital I/O operation. Programs can be used as is, or modified to meet the user's data acquisition needs.

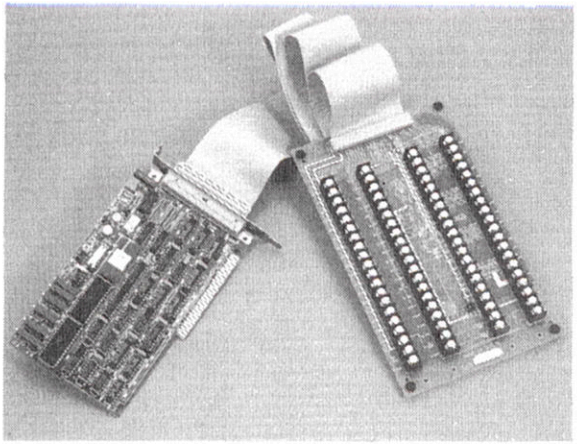
The example programs run under IBM interpreted BASIC or advanced BASIC, version 3.0 or higher.

SCREW TERMINAL PANEL ACCESSORIES

Three screw terminal panels are recommended for use with DT2811 Series boards: the DT707, the DT752, and the DT760.

The DT707 terminal panel accommodates all user connections to the DT2811 Series board on convenient screw terminal connections. Screw connections are labeled in silkscreen for analog input connections, analog output connections, DIO lines, external clock input, and external trigger input. In addition, blank circuit pads are provided for user-supplied current shunts to accommodate 0 to 20mA current inputs (current inputs should be used when differential inputs are selected). The DT707 is shipped with a one-meter (3.3 foot) flat ribbon cable which plugs directly into the DT2811 Series board's J1 connector. The DT707 is designed for table-top mounting, and comes equipped with rubber feet.

The DT752 is similar to the DT707, except analog input lines are directed to a separate 20-pin connector. This connector permits the DT2811 Series board to be used with any of a wide range of Data Translation signal conditioning accessories, including the DT709-Y or DT756-Y. When used with the DT709-Y or DT756-Y, a DT2811 Series board provides 16 differential inputs. The DT756-Y also provides selectable gains to accommodate low level signals, and offset and cold-junction compensation for thermocouple inputs.



M-4565

Figure 7. Most user requirements can be met by using the DT707 screw terminal panel for both high or low level voltage inputs or current inputs. The DT707-T has a thermocouple reference cold-junction compensation circuit which permits compensation for measurement errors caused by connection to the screw terminal panel.

The DT760 and DT500 Series of isolated signal conditioning products offer a variety of features, including differential inputs, gain, cold-junction compensation, RTD linearization, and bridge-completion circuitry. DT500 Series isolated signal conditioning modules offer a variety of features, including differential inputs, gain, cold-junction compensation, RTD linearization, or thermocouple linearization circuitry.

SPECIFIC
Typical at +
A/D SUBSYS
Number of Ir
Resolution
Programmabl
A/D Through
A/D Conversi
Channel Acq
System Accur
Input Ranges
Unipolar
Bipolar
Output Codin
(Jumper)
Common Mo
Common Mo
Maximum Inp
Power On
Power Off
Input Impedar
Off Channel
On Channel
Bias Current
Nonlinearity
Differential N
Inherent Quar
A/D Zero Drif
Gain Drift (pp
Differential Li
Amplifier Inpu
Channel Cross
Gain Error
Zero Error
Monotonicity
D/A SUBSYST
Number of DA
Resolution
Setting Time t
10V Step
100mV Step
Throughput
Slew Rate
Output Range

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M-4565

SPECIFICATIONS

Typical at +25°C and rated power, unless otherwise specified

A/D SUBSYSTEM	DT2811-PGH	DT2811-PGL
Number of Inputs	16SE/8DI (jumper)	16SE/8DI (jumper)
Resolution	12 bits	12 bits
Programmable Gains	1, 2, 4, 8	1, 10, 100, 500
A/D Throughput	20kHz	20kHz (gain of 1 or 10) 2.5kHz(gain of 100 or 500)
A/D Conversion Time	30µs	30µs
Channel Acquisition Time (±1/2 LSB)	20µs	20µs (gain of 1 or 10) 370µs (gain of 100 or 500)
System Accuracy (percent of FSR)	±.03% (G=1) ±.035% (G=2) ±.04% (G=4) ±.05% (G=8)	±.03% (G=1) ±.05% (G=10) ±.07% (G=100) ±.15% (G=500)
Input Ranges (Jumper)		
Unipolar	0 to +5V	0 to +5V
Bipolar	±5V, ±2.5V	±5V, ±2.5V
Output Coding (Jumper)	Binary Offset binary	Binary Offset binary
Common Mode Input Voltage, Maximum	±11V	±11V
Common Mode Rejection Ratio, (Gain=1, 60Hz)	70dB, 1kΩ	70dB, 1kΩ 100dB (gain of 500)
Maximum Input Voltage Without Damage		
Power On	±32V	±32V
Power Off	±20V	±20V
Input Impedance		
Off Channel	100MΩ, 10pF	100MΩ, 10pF
On Channel	100MΩ, 100pF	100MΩ, 100pF
Bias Current	±50nA	±50nA
Nonlinearity	±3/4 LSB	±3/4 LSB
Differential Nonlinearity	±1/2 LSB	±1/2 LSB
Inherent Quantizing Error	±1/2 LSB	±1/2 LSB
A/D Zero Drift (ppm of FSR/°C)	±10	±10
Gain Drift (ppm of FSR/°C)	±30	±30
Differential Linearity Drift (ppm of FSR/°C)	±3	±3
Amplifier Input Noise	2.0µV rms	2.0µV rms
Channel Crosstalk	–80dB @1kHz	–80dB @1kHz
Gain Error	Adjustable to zero	Adjustable to zero
Zero Error	Adjustable to zero	Adjustable to zero
Monotonicity	0 to +70°C	0 to +70°C

D/A SUBSYSTEM (ALL MODELS)	
Number of DACs	2
Resolution	12 bits
Setting Time to 0.01% of FSR	
10V Step	7µs
100mV Step	1µs
Throughput	50kHz max. (each DAC)
Slew Rate	10V/µs
Output Ranges (jumper)	0 to +5V, ±2.5V, ±5V

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SPECIFICATIONS (continued)

Input Data Coding (jumper)	
Unipolar	Straight Binary
Bipolar	Offset Binary
Output Current	±5mA
Output Impedance	0.1Ω
Capacitive Drive Capability	0.004µF
Protection Against	Short circuit to DAC Ground
Nonlinearity	.01% of FSR
Differential Nonlinearity	3/4 FSR
Inherent Quantizing Error	±1/2 FSR
Gain Error	Adjustable to zero
Zero Error	Adjustable to zero
Gain Drift (Bipolar)	±30ppm of FSR/°C
Zero Drift (Bipolar)	±10ppm of FSR/°C
Monotonicity	0 to +70°C

DIGITAL I/O SUBSYSTEM (ALL MODELS)

Number of Lines	8 in, 8 out
Logic Family	ALSTTL
Logic Sense	Positive true
Input Type	Level sensitive
Input Termination	None; unused input float
Input Logic Load	1 ALSTTL load
Logic High Input Voltage	2.0V minimum
Logic Low Input Voltage	0.8V maximum
Logic High Input Current	20µA maximum
Logic Low Input Current	–0.1mA maximum
Fanout	20 LSTTL loads
Logic High Output Voltage	2.4V minimum
Logic Low Output Voltage	0.4V maximum
Logic High Output Current	–15mA maximum
Logic Low Output Current	24mA maximum

ONBOARD CLOCK (ALL MODELS)

Base Frequency	600kHz ±0.01%
Divisor	1 to 120,000,000
Usable Frequencies	.005Hz to 20kHz

EXTERNAL TRIGGER (ALL MODELS)

Input Type	Asserted low
Logic Family	LSTTL
Logic Load	1 LSTTL load
Input Termination	22kΩ pullup to +5V
Logic High Input Voltage	2.0V minimum
Logic Low Input Voltage	0.8V maximum
Logic High Input Current	20µA maximum
Logic Low Input Current	–0.2mA maximum
Minimum Pulse Width	
Clock High	500ns
Clock Low	500ns

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SPECIFICATI

EXTERNAL CLOCI
Input Type
Logic Family
Logic Load
Input Termination
Logic High Input V
Logic Low Input Vc
Logic High Input C
Logic Low Input Cu
Minimum Pulse W
Clock High
Clock Low
Frequency

INTERFACE CHAR
Compatible Bus
Interface Type
Number of Locatio
Data Path
Base Address Rang
Factory-Assigned B
Interrupts
Interrupt Lines
Interrupt Sources
Mating Connector

POWER REQUIRE

PHYSICAL/ENVIRC
Dimensions

Weight
Operating Temperat
Storage Temperatur
Relative Humidity
Altitude

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SPECIFICATIONS (continued)

EXTERNAL CLOCKS (ALL MODELS)

Input Type	High-to-low transition
Logic Family	LSTTL
Logic Load	1 LSTTL load
Input Termination	22kΩ pullup to +5V
Logic High Input Voltage	2.0V minimum
Logic Low Input Voltage	0.8V maximum
Logic High Input Current	20µA maximum
Logic Low Input Current	–0.2mA maximum
Minimum Pulse Width	
Clock High	500ns
Clock Low	500ns
Frequency	DC to 1 MHz

INTERFACE CHARACTERISTICS (ALL MODELS)

Compatible Bus	IBM Personal Computer
Interface Type	I/O mapped with 10-bit addressing
Number of Locations Occupied	8 contiguous bytes
Data Path	8 bits
Base Address Range (jumper)	200 (hex) to 3F8 (hex) in increments of 8 (hex)
Factory-Assigned Base Address	218 (hex)
Interrupts	1 interrupt, jumper-configurable to any of four interrupt lines
Interrupt Lines	2, 3, 5, or 7
Interrupt Sources	A/D Error, A/D Done
Mating Connector	50-pin 3M type, user-supplied Ansley 609-5030 or equivalent Ansley 609-5031 or equivalent strain relief recommended

POWER REQUIREMENTS

+5V ±5% @290mA
+12V ±5% @50mA
–12V ±5% @100mA

PHYSICAL/ENVIRONMENTAL

Dimensions	4.5"H X 7.0"W X .75"D (11.4 X 17.8 X 1.9 cm)
Weight	6 ounces (168 g)
Operating Temperature Range	0 to +50°C (32 to 122°F)
Storage Temperature Range	–25 to +70°C (–13 to +158°F)
Relative Humidity	To 95% non-condensing
Altitude	To 7500 ft (2286 m)

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ORDERING GUIDE

All DT2811 Series boards are shipped with a comprehensive user manual that includes programming instructions, as well as example programs.

ANALOG AND DIGITAL I/O BOARD

DT2811-PGH

IBM PC/XT/AT-compatible analog and digital I/O board with A/D, D/A, digital I/O, and onboard programmable clock. The A/D subsystem features 16SE or 8DI analog inputs, 12-bit resolution, programmable gain (gains of 1, 2, 4, and 8), and 20kHz throughput. The D/A subsystem features two 12-bit D/A converters with 50kHz throughput. The digital I/O subsystem features 8 lines of input and 8 lines of output.

DT2811-PGL

Same as the DT2811-PGH except the programmable gain values supplied are 1, 10, 100, or 500, and A/D throughput is 2.5 kHz at gains of 100 and 500.

LPCLAB

IBM PC/XT/AT and PC-DOS compatible data acquisition subroutine library for use with the DT2811-PGH and DT2811-PGL. Software support provided for Microsoft® C, Pascal, FORTRAN, QuickC®, and QuickBASIC™, as well as Borland Turbo C® and Turbo Pascal®. LPCLAB is available in the following packages.

SP0159-CC

This initial license package is for new users. It consists of the initial license, a copy of the software, a user manual, and 90 days of free telephone support. It is supplied on 5.25" double-sided double-density diskette media.

SP0159-CK

This initial license package is for new users. It consists of the initial license, a copy of the software, a user manual, and 90 days of free telephone support. It is supplied on 3.5" 800 Kbyte diskette media.

ACCESSORIES

DT707

The DT707 is a screw terminal panel for all A/D, D/A, DIO, external trigger, and external clock connections. It includes a 1 meter (3.3 foot) flat ribbon cable. For use with thermocouples and no signal conditioning requirement, the DT707-T provides a reference cold-junction compensation circuit to determine the temperature of the screw terminal panel

DT752

Complete with cable and screw terminal panel for D/A, digital I/O, and trigger functions, the DT752 allows several signal conditioning products such as the DT709-Y (high level signals) and the DT756-Y (low level thermocouple signals) to be used with the A/D sections of the DT2811 Series boards. See individual signal conditioning product data sheets for complete details.

DT756-Y

The DT756-Y is used to interface low level signal such as thermocouples, RTDs, and strain gauges. The DT756-Y accepts 16 differential analog inputs, has gains of 100, 125, and 200 with selectable offsets, cold-junction compensation for J, T, K, E, S, R, or B thermocouples, and provides 16 single-ended analog inputs to the DT2811 Series data acquisition board.

DT709-Y

The DT709-Y is used to interface high levels to the DT2811 Series. The DT709-Y accepts 16 differential analog inputs, provides input protection to 100 volts, common mode rejection, and 16 single-ended analog inputs to the DT2811 Series data acquisition board.

DT760 and DT760-T

The DT760 and DT760-T support up to 16 input and two output modules from the DT500 Series isolated signal conditioning modules, and user connections for 16 lines of digital I/O. The DT760-T comes with 16 temperature sensors, required for thermocouple or RTD modules. Requires EP035 cable assembly for connection to DT2811 Series board.

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FEATURE

- Low-cost, PC/XT/AT
- Laptop co circuitry
- A/D featu
  - 16SE in
  - 25kHz
  - 12-bit
  - Input ra bipolar
- Programm repeated c
- Supports i is complet
- LPCLAB™ functions f Pascal, C, QuickBASI Pascal®
- Shipped wi example p for user ap
- Wide varie specialized capabilitie

TABLE 1. DT

MODEL
DT2814

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