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User Manual
for

DT2821 Series

DT2821, DT2825, DT2821-F-16SE, DT2821-F-8DI,
DT2821-G-16SE, DT2821-G-8DI,
DT2823, DT2824-PGH, DT2824-PGL, DT2827, AND DT2828

HIGH SPEED SINGLE-BOARD
ANALOG AND DIGITAL I/O SYSTEMS
for the IBM Personal Computer AT

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PREFACE

AUDIENCE

This manual is for the Data Translation DT2821 series board. The manual describes the configuration of the board, shows system interconnections, discusses the board's architecture, and provides you with enough information to program and operate the DT2821 series board. The manual assumes that you have a general knowledge of electronic circuitry, are familiar with the IBM Personal Computer AT, understand data conversion, and possess enough proficiency in software to write your own application programs.

ORGANIZATION

This manual is divided into seven chapters and six appendices as follows:

CHAPTER 1 INTRODUCTION
This chapter includes an overview discussion of the DT2821 series board's capabilities.

CHAPTER 2 SPECIFICATIONS
This chapter lists the electrical and mechanical specifications for the board.

CHAPTER 3 GETTING STARTED
This chapter discusses the configuration of the DT2821 series board.

CHAPTER 4 INSTALLATION AND USER CONNECTIONS
This chapter discusses the installation procedure and user connections.

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CHAPTER 5 INTERFACE REGISTERS
This chapter contains information on the eight registers on the DT2821 series board.

CHAPTER 6 PRINCIPLES OF OPERATION
This chapter provides an overview of how the DT2821 board operates. Included is a discussion of the A/D converter, RAM channel-gain list, D/A converter, Digital I/O, and pacer clock.

CHAPTER 7 PROGRAMMING
This chapter details the programming sequences for all operating modes and all subsystems of the DT2821 series boards.

APPENDIX A IBM AT P1 AND P2 SIGNALS
This appendix lists the signals on the P1 and P2 connectors for the IBM Personal Computer AT.

APPENDIX B CALIBRATION
This appendix presents a detailed discussion of how to calibrate the A/D and D/A subsystems.

APPENDIX C TROUBLESHOOTING AND FACTORY SERVICE
This appendix describes what to do if something goes wrong with the DT2821 series board.

APPENDIX D CODING TABLES
This appendix lists 12- and 16-bit binary coding tables for the A/D and D/A converters.

APPENDIX E DT707 AND DT752 SCREW TERMINAL PANELS
This appendix contains technical and applications information of the DT707 and DT752 accessory screw terminal panels, and their use with DT2821 series boards.

APPENDIX F ENGINEERING DRAWINGS
This appendix contains the assembly drawings for the DT2821 series, DT707, and DT752.

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CONVENTIONS

Throughout this manual, the term "DT2821 series" is used for all comments which apply equally to the DT2821, DT2821-F-16SE, DT2821-F-8DI, DT2821-G-16SE, DT2821-G-8DI, DT2823, DT2824, DT2825, DT2827, and DT2828. Comments which apply only to a particular board or boards, but not to the entire series, reference the specific board model number or numbers. For example:

"All DT2821 series boards have two 12-bit D/A converters."

"The DT2827 and DT2823 have 16-bit A/D converters with 100kHz throughput."

"The DT2823 has two 16-bit D/A converters with 100kHz throughput."

In the discussion on register bits, the following conventions are used:

'R/W' indicates read and write access.

'Read only' indicates read access only, writes are ignored.

'Read only with enabled clear' indicates read access, writing the bit to a one clears it.

'Write only' indicates reads are indeterminate, write access.

'Read as 0/W' indicates reads as a zero, write access.

'Read as 1/W' indicates reads as a one, write access.

'Read as 1/Write ignored' indicates reads as a one, writes are ignored (reserved bits).

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CHAPTER 1
INTRODUCTION

DESCRIPTION

ACCESSORIES

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1.1 DESCRIPTION

The DT2821 series boards are high-speed analog and digital I/O boards designed to be used with the IBM Personal Computer AT or compatible computer systems. The series consists of eleven models. Any board in the series can be plugged into one of the six fully bussed system expansion slots in the IBM Personal Computer AT backplane. The board can be programmed by the IBM Personal Computer AT to perform analog-to-digital (A/D) conversions; digital-to-analog (D/A) conversions (except the DT2824-PGH and DT2824-PGL); and digital input and output (DIO) transfers. The DT2821 series board can be configured to perform the analog I/O functions in programmed I/O (PIO) mode or Direct Memory Access (DMA) both with or without interrupt capability. Table 1-1 provides a comparative summary of the main features of the DT2821 series.

TABLE 1-1: DT2821 SERIES FEATURES COMPARISON

MODEL	RESOLUTION (BITS) A/D	D/A	THROUGHPUT (KHZ) A/D	D/A	MAX A/D GAIN	NUMBER OF A/D CHANNELS
DT2821	12	12	50	130	8	16SE/8DI[1]
DT2821-F-16SE	12	12	150	130	8	16SE
DT2821-F-8DI	12	12	150	130	8	8DI
DT2821-G-16SE	12	12	250	130	8	16SE
DT2821-G-8DI	12	12	250	130	8	8DI
DT2823	16	16	100	100	1	4DI
DT2824-PGH	12		50		8	16SE/8DI[1]
DT2824-PGL	12		50		500	16SE/8DI[1]
DT2825	12	12	45[2]	130	500	16SE/8DI[1]
DT2827	16	12	100	130	1	4DI
DT2828[3]	12	12	100	130	1	4SE

NOTES
1. Jumper selectable.
2. 2.5kHz at gains of 100 and 500.
3. Simultaneous sample and hold.

A/D selection on the DT2821 series is accomplished using a unique RAM channel-gain list. The RAM channel-gain list is a 16-location memory space which allows any of the channels at any gain to be sampled in any sequence at the full throughput rate. It also permits the same channel to be sampled at different gains.

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The DT2824-PGH and DT2824-PGL models do not include D/A subsections. The D/A subsections on all other models except the DT2823 include two 12-bit deglitched D/A converters. The DT2823 model only features two 16-bit deglitched D/A converters. These D/A converters can provide either single outputs (the analog outputs change at different times) or simultaneous outputs (the outputs of both D/A converters change at the same time). When used in DMA transfer mode, digital data can be converted to analog at up to 130kHz per channel from system memory (100kHz for DT2823).

In addition, the DT2821 series boards feature two 8-line digital I/O ports. Either port can be set for input or output.

The DT2821 series boards also contain an on-board programmable pacer clock, which can be used to provide clock pulses to control the rate of conversions for the board's A/D and D/A subsystems. The pacer clock operates under program control, and provides a usable range of 1.25 kHz microseconds (800kHz) to 2 seconds (0.5Hz). Alternatively, an external clock can be selected to start conversions, and an external trigger may be selected to gate A/D and D/A conversion events. The A/D and D/A converters can be operated simultaneously at the same clock speed; alternatively the D/A subsystem can be operated in single conversion mode while the A/D subsystem operates from the pacer clock or external clock.

The DMA interface is compatible with 16-bit data transfers and can be jumper-selected to use DMA channel 5, 6, or 7. DMA buffers may be located anywhere in the 16Mbyte memory space of the IBM Personal Computer AT and may be up to 65,536 words (128Kbytes) long. A unique configuration utilizing two DMA channels is also included to support Continuous Performance DMA. Continuous Performance is a data sampling method which provides gap-free transfers of large volumes of data from memory or disk (D/A conversions) or to memory or disk (A/D conversions) without any loss of samples.

The DT2821 series boards support interrupts. The interrupt level is jumper-selectable to level 3, 5, 7, 10, or 15.

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1.2 ACCESSORIES

Two screw terminals are recommended for use with the DT2821 series: the DT707 and the DT752.

- DT707
  The DT707 screw terminal panel accommodates all user connections to the DT2821 series board on convenient screw terminal connections. Screw connections are labeled in silkscreen for analog input connections, analog output connections, DIO lines, external clock input, and external trigger input. In addition, blank circuit pads are provided for user-supplied current shunts to accommodate 0 to 20mA current inputs (current inputs should only be used with differential input versions of the DT2821 series). The DT707 contains an integral one-meter (3.3 feet) flat ribbon cable which plugs directly into the DT2821 series board's J1 connector. The DT707 is designed for table top mounting and comes equipped with rubber feet.

- DT752
  The DT752 is similar to the DT707, except analog input lines are directed to a separate 20-pin connector. This connector permits the DT2821 series board to be used with any of a wide range of Data Translation signal conditioning accessories, including the non-isolated DT709-Y, DT756-Y, and the isolated DT760/DT500 series of signal conditioning modules. When used with the DT709-Y or DT756-Y, a DT2821 series board should be configured for single-ended inputs. The DT709-Y and DT756-Y convert 16 differential input signals into 16 single-ended signals for the DT2821 series board. The DT756-Y also provides a jumper-selectable gain to accommodate low level signals, as well as offset and cold-junction compensation for thermocouple inputs. The DT760/DT500 series isolated signal conditioning products offer a variety of features, including differential inputs, gain, cold-junction compensation, or RTD linearization.

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ATLAB is a real-time software package for Data Translation's IBM Personal Computer AT compatible DT2821 series of analog and digital I/O boards. The package contains libraries of routines designed to be CALLed from Microsoft's FORTRAN, C, and Pascal; and operated under MS or PC DOS. The ATLAB package allows you to control all the analog and digital I/O capabilities of the interface boards through operation-specific routines which greatly simplify the programming of the hardware interfaces. With ATLAB, direct access to the control registers is not required. An error processing system checks for argument errors and generates an error report if any are detected. Attempts to operate the interface in illegal modes of operation are reported and not executed. Routines are included for analog input, analog output, digital input, digital output, continuous sampling (memory and disk), pacer clock control, and configuration setup.

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CHAPTER 2
SPECIFICATIONS

DT2821 A/D SUBSYSTEM

DT2821-F-16SE AND DT2821-F-8DI A/D SUBSYSTEMS

DT2821-G-16SE AND DT2821-G-8DI A/D SUBSYSTEMS

DT2823 A/D SUBSYSTEM

DT2824-PGH A/D SUBSYSTEM

DT2824-PGL A/D SUBSYSTEM

DT2825 A/D SUBSYSTEM

DT2827 A/D SUBSYSTEM

DT2828 A/D SUBSYSTEM

D/A SUBSYSTEM

DIGITAL I/O SUBSYSTEM

EXTERNAL TRIGGER

CLOCK

INTERFACE CHARACTERISTICS

POWER REQUIREMENTS

PHYSICAL/ENVIRONMENTAL

CONNECTORS AND CABLES

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All specifications are typical at +25°C and rated voltage unless otherwise specified.

2.1 DT2821 A/D SUBSYSTEM

A/D MODULE	DT5712-PGH
ANALOG INPUTS	
Number of Analog Inputs	16SE, 8DI (user-selectable)
Input Ranges	0 to +10V (unipolar) ±10V (bipolar)
Output Data Codes	Straight binary (unipolar), offset binary, or two's complement (bipolar)
Gain Range	1, 2, 4, 8
Input Impedance	Off Channel: 100 megohms, 10pF On Channel: 100 megohms, 100pF
Bias Current	±20nA
Common Mode Input Voltage, Maximum	±11V
Common Mode Rejection Ratio (CMRR), Gain = 1	80dB at 60Hz, 1 kilohm unbalanced
Maximum Input Voltage without Damage, Power On	±35V
Maximum Input Voltage without Damage, Power Off	±20V
Amplifier Input Noise	0.1 LSB rms
NOTE: Where gain is greater than 1, input noise is multiplied by gain.	
Channel-to-channel Input Voltage Error	±5µV

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ACCURACY	
Resolution	12 bits
Nonlinearity	Less than ±½ LSB
Differential Nonlinearity	Less than ±½ LSB
Inherent Quantizing Error	±½ LSB
System Accuracy	To within ±0.03% FSR
Channel Crosstalk	-80dB at 1kHz
Gain Error	Adjustable to 0
Zero Error	Adjustable to 0
DYNAMIC PERFORMANCE	
Channel Acquisition Time to within ½ LSB	18µs
A/D Conversion Time	10µs
A/D Converter Throughput	50kHz
A/D Throughput to System Memory	50,000 samples per second
Sample & Hold Aperture Uncertainty	10ns
Sample & Hold Aperture Delay	50ns
Sample & Hold Droop Rate	0.1mV/ms
Sample & Hold Feedthrough Attenuation	80dB at 1kHz

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THERMAL CHARACTERISTICS

A/D Zero Drift	±10 ppm of FSR/°C
Amplifier Zero Drift	±20µV/°C
Gain Drift	±30 ppm of FSR/°C
Differential Linearity Drift	±3 ppm of FSR/°C
Monotonicity	0 to +70°C

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2.2 DT2821-F-16SE AND DT2821-F-8DI A/D SUBSYSTEMS

A/D MODULE	DT5725
ANALOG INPUTS	
Number of Analog Inputs	16SE, 8DI (factory configured)
Input Ranges	0 to +10V (unipolar) ±10V (bipolar)
Output Data Codes	Straight binary (unipolar), offset binary, or two's complement (bipolar)
Gain Range	1, 2, 4, 8
Input Impedance	Off Channel: 100 megohms, 10pF On Channel: 100 megohms, 50pF
Bias Current	±10nA
Common Mode Input Voltage, Maximum	±10.5V
Common Mode Rejection Ratio (CMRR), Gain = 1	80dB at 60Hz, 1 kilohm unbalanced
Maximum Input Voltage without Damage, Power On	±27V
Maximum Input Voltage without Damage, Power Off	±12V
Amplifier Input Noise	0.2 LSB rms
Channel-to-channel Input Voltage Error	±.1mV

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SPECIFICATIONS
DT2821-F-16SE AND DT2821-F-8DI A/D SUBSYSTEMS

ACCURACY

Resolution	12 bits
Nonlinearity	Less than ±½ LSB
Differential Nonlinearity	Less than ±½ LSB
Inherent Quantizing Error	±½ LSB
System Accuracy	
Gain = 1	To within ±0.03% FSR
Gain = 2	To within ±0.04% FSR
Gain = 4	To within ±0.05% FSR
Gain = 8	To within ±0.07% FSR
Channel Crosstalk	-100dB at 1kHz
Gain Error	Adjustable to 0
Zero Error	Adjustable to 0

DYNAMIC PERFORMANCE

Channel Acquisition Time to within ½ LSB	7.65µs
A/D Conversion Time	4µs
A/D Converter Throughput	150kHz
A/D Throughput to System Memory	150,000 samples per second
Sample & Hold Aperture Uncertainty	.5ns
Sample & Hold Aperture Delay	100ns
Sample & Hold Droop Rate	50mV/ms
Sample & Hold Feedthrough Attenuation	80dB at 1kHz

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THERMAL CHARACTERISTICS	
A/D Zero Drift	±10 ppm of FSR/°C
Amplifier Zero Drift	±25µV/°C
Gain Drift	±30 ppm of FSR/°C
Differential Linearity Drift	±3 ppm of FSR/°C
Monotonicity	0 to +70°C

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2.3 DT2821-G-16SE AND DT2821-G-8DI A/D SUBSYSTEMS

A/D MODULE	DT5727
ANALOG INPUTS	
Number of Analog Inputs	16SE, 8DI (specified when ordered)
Input Ranges	0 to +10V (unipolar) ±5V (bipolar) ±10V (bipolar)
Output Data Codes	Straight binary (unipolar), offset binary, or two's complement (bipolar)
Gain Range	1, 2, 4, 8
Input Impedance	Off Channel: 100 megohms, 50pF On Channel: 100 megohms, 100pF
Bias Current	±20nA
Common Mode Input Voltage, Maximum	±10.5V
Common Mode Rejection Ratio (CMRR), Gain = 1	80dB at 60Hz, 1 kilohm unbalanced
Maximum Input Voltage without Damage, Power On	±16V
Maximum Input Voltage without Damage, Power Off	±1V
Amplifier Input Noise	0.2 LSB rms
Channel-to-channel Input Voltage Error	±.1mV

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ACCURACY	
Resolution	12 bits
Nonlinearity	Less than ±½ LSB
Differential Nonlinearity	Less than ±½ LSB
Inherent Quantizing Error	±½ LSB
System Accuracy	
Gain = 1	To within ±0.03% FSR
Gain = 2	To within ±0.04% FSR
Gain = 4	To within ±0.05% FSR
Gain = 8	To within ±0.07% FSR
Channel Crosstalk	-100dB at 1kHz
Gain Error	Adjustable to 0
Zero Error	Adjustable to 0
DYNAMIC PERFORMANCE	
Channel Acquisition Time to within ½ LSB	2.5µs
A/D Conversion Time	2.5µs
A/D Converter Throughput	250kHz
A/D Throughput to System Memory	250,000 samples per second
Sample & Hold Aperture Uncertainty	.2ns
Sample & Hold Aperture Delay	50ns
Sample & Hold Droop Rate	50mV/ms
Sample & Hold Feedthrough Attenuation	80dB at 1kHz

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THERMAL CHARACTERISTICS

A/D Zero Drift	±10 ppm of FSR/°C
Amplifier Zero Drift	±25µV/°C
Gain Drift	±30 ppm of FSR/°C
Differential Linearity Drift	±3 ppm of FSR/°C
Monotonicity	0 to +70°C

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2.4 DT2823 A/D SUBSYSTEM

A/D MODULE	DT5726
ANALOG INPUTS	
Number of Analog Inputs	4DI
Input Range	±10V
Output Data Codes	Two's complement
Input Impedance	Off Channel: 100 megohms, 10pF On Channel: 100 megohms, 20pF
Bias Current	±250nA
Common Mode Input Voltage, Maximum	±10.5V
Common Mode Rejection Ratio (CMRR)	80dB at 60Hz, 1 kilohm unbalanced
Maximum Input Voltage without Damage, Power On	±27V
Maximum Input Voltage without Damage, Power Off	±12V
Amplifier Input Noise	0.5 LSB rms
Channel-to-channel Input Voltage Error	±5µV

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SPECIFICATIONS
DT2823 A/D SUBSYSTEM

ACCURACY	
Resolution	16 bits
Nonlinearity	Less than 1 LSB
Differential Nonlinearity	Less than 1 LSB
Inherent Quantizing Error	±½ LSB
System Accuracy	To within ±0.003% FSR
Channel Crosstalk	-100dB at 1kHz
Gain Error	Adjustable to 0
Zero Error	Adjustable to 0
DYNAMIC PERFORMANCE	
Channel Acquisition Time to within ½ LSB	8.5µs
A/D Conversion Time	6µs
A/D Converter Throughput	100kHz
A/D Throughput to System Memory	100,000 samples per second
Sample & Hold Aperture Uncertainty	.2ns
Sample & Hold Aperture Delay	100ns
Sample & Hold Feedthrough Attenuation	94dB at 100kHz
Sample & Hold Droop Rate	7.5mV/ms
THERMAL CHARACTERISTICS	
A/D Zero Drift	±10 ppm of FSR/°C
Amplifier Zero Drift	±25µV/°C
Gain Drift	±30 ppm of FSR/°C
Differential Linearity Drift	1.5 ppm of FSR/°C
Monotonicity	0 to +70°C

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All specifications are typical at +25°C and rated voltage unless otherwise specified.

2.5 DT2824-PGH A/D SUBSYSTEM

A/D MODULE	DT5712-PGH
ANALOG INPUTS	
Number of Analog Inputs	16SE, 8DI (user-selectable)
Input Ranges	0 to +10V (unipolar) ±10V (bipolar)
Output Data Codes	Straight binary (unipolar), offset binary, or two's complement (bipolar)
Gain Range	1, 2, 4, 8
Input Impedance	Off Channel: 100 megohms, 10pF On Channel: 100 megohms, 100pF
Bias Current	±20nA
Common Mode Input Voltage, Maximum	±11V
Common Mode Rejection Ratio (CMRR), Gain = 1	80dB at 60Hz, 1 kilohm unbalanced
Maximum Input Voltage without Damage, Power On	±35V
Maximum Input Voltage without Damage, Power Off	±20V
Amplifier Input Noise	0.1 LSB rms
NOTE: Where gain is greater than 1, input noise is multiplied by gain.	
Channel-to-channel Input Voltage Error	±5µV

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SPECIFICATIONS
DT2824-PGH A/D SUBSYSTEM

ACCURACY	
Resolution	12 bits
Nonlinearity	Less than ±½ LSB
Differential Nonlinearity	Less than ±½ LSB
Inherent Quantizing Error	±½ LSB
System Accuracy	To within ±0.03% FSR
Channel Crosstalk	-80dB at 1kHz
Gain Error	Adjustable to 0
Zero Error	Adjustable to 0
DYNAMIC PERFORMANCE	
Channel Acquisition Time to within ½ LSB	18µs
A/D Conversion Time	10µs
A/D Converter Throughput	50kHz
A/D Throughput to System Memory	50,000 samples per second
Sample & Hold Aperture Uncertainty	10ns
Sample & Hold Aperture Delay	50ns
Sample & Hold Droop Rate	0.1mV/ms
Sample & Hold Feedthrough Attenuation	80dB at 1kHz

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THERMAL CHARACTERISTICS	
A/D Zero Drift	±10 ppm of FSR/°C
Amplifier Zero Drift	±20µV/°C
Gain Drift	±30 ppm of FSR/°C
Differential Linearity Drift	±3 ppm of FSR/°C
Monotonicity	0 to +70°C

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2.6 DT2824-PGL A/D SUBSYSTEM

A/D MODULE	DT5712-PGL
ANALOG INPUTS	
Number of Analog Inputs	16SE, 8DI (user-selectable)
Input Ranges	0 to +10V (unipolar) ±10V (bipolar)
Output Data Codes	Straight binary (unipolar), offset binary, or two's complement (bipolar)
Gain Range	1, 10, 100, 500
Input Impedance	Off Channel: 100 megohms, 10pF On Channel: 100 megohms, 100pF
Bias Current	±20nA
Common Mode Input Voltage, Maximum	±11V
Common Mode Rejection Ratio (CMRR), Gain = 1	80dB at 60Hz, 1 kilohm unbalanced
Maximum Input Voltage without Damage, Power On	±35V
Maximum Input Voltage without Damage, Power Off	±20V
Amplifier Input Noise	0.1 LSB rms
NOTE: Where gain is greater than 1, input noise is multiplied by gain.	
Channel-to-channel Input Voltage Error	±5µV

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ACCURACY	
Resolution	12 bits
Nonlinearity	Less than ±½ LSB
Differential Nonlinearity	Less than ±½ LSB
Inherent Quantizing Error	±½ LSB
System Accuracy	To within ±0.03% FSR
Channel Crosstalk	-80dB at 1kHz
Gain Error	Adjustable to 0
Zero Error	Adjustable to 0
DYNAMIC PERFORMANCE	
Channel Acquisition Time to within ½ LSB	18µs
A/D Conversion Time	10µs
A/D Converter Throughput	50kHz
A/D Throughput to System Memory	50,000 samples per second
Sample & Hold Aperture Uncertainty	10ns
Sample & Hold Aperture Delay	50ns
Sample & Hold Droop Rate	0.1mV/ms
Sample & Hold Feedthrough Attenuation	80dB at 1kHz

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THERMAL CHARACTERISTICS

A/D Zero Drift	±10 ppm of FSR/°C
Amplifier Zero Drift	±20µV/°C
Gain Drift	±30 ppm of FSR/°C
Differential Linearity Drift	±3 ppm of FSR/°C
Monotonicity	0 to +70°C

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2.7 DT2825 A/D SUBSYSTEM

A/D MODULE	DT5713-PGL
ANALOG INPUTS	
Number of Analog Inputs	16SE, 8DI (user-selectable)
Input Ranges	0 to +10V (unipolar) ±10V (bipolar)
Output Data Codes	Straight binary (unipolar), offset binary, or two's complement (bipolar)
Gain Range	1, 10, 100, 500
Input Impedance	Off Channel: 100 megohms, 10pF On Channel: 100 megohms, 100pF
Bias Current	±20nA
Common Mode Input Voltage, Maximum	±11V
Common Mode Rejection Ratio (CMRR), Gain = 1	80dB at 60Hz, 1 kilohm unbalanced
Maximum Input Voltage without Damage, Power On	±35V
Maximum Input Voltage without Damage, Power Off	±20V
Amplifier Input Noise	0.1 LSB rms

NOTE: Where gain is greater than 1, input noise is multiplied by gain.

Channel-to-channel Input Voltage Error	±5μV

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SPECIFICATIONS
DT2825 A/D SUBSYSTEM

ACCURACY	
Resolution	12 bits
Nonlinearity	Less than ±½ LSB
Differential Nonlinearity	Less than ±½ LSB
Inherent Quantizing Error	±½ LSB
System Accuracy	To within ±0.03% FSR
Channel Crosstalk	-80dB at 1kHz
Gain Error	Adjustable to 0
Zero Error	Adjustable to 0
DYNAMIC PERFORMANCE	
Channel Acquisition Time to Within ½ LSB	
Gain = 1, 10	22µs
Gain = 100, 500	400µs
A/D Conversion Time	10µs
A/D Converter Throughput	
Gain = 1, 10	45kHz
Gain = 100, 500	2.5kHz
A/D Throughput to System Memory	45,000 samples per second
Sample & Hold Aperture Uncertainty	10ns
Sample & Hold Aperture Delay	50ns
Sample & Hold Droop Rate	0.1mV/ms
Sample & Hold Feedthrough Attenuation	80dB at 1kHz

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THERMAL CHARACTERISTICS	
A/D Zero Drift	±10 ppm of FSR/°C
Amplifier Zero Drift	±20µV/°C
Gain Drift	±30 ppm of FSR/°C
Differential Linearity Drift	±3 ppm of FSR/°C
Monotonicity	0 to +70°C

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2.8 DT2827 A/D SUBSYSTEM

A/D MODULE	DT5726
ANALOG INPUTS	
Number of Analog Inputs	4DI
Input Ranges	±10V (bipolar)
Output Data Codes	Two's complement
Input Impedance	Off Channel: 100 megohms, 10pF On Channel: 100 megohms, 20pF
Bias Current	±250nA
Common Mode Input Voltage, Maximum	±10.5V
Common Mode Rejection Ratio (CMRR)	80dB at 60Hz, 1 kilohm unbalanced
Maximum Input Voltage without Damage, Power On	±27V
Maximum Input Voltage without Damage, Power Off	±12V
Amplifier Input Noise	0.5 LSB rms
Channel-to-channel Input Voltage Error	±5µV

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ACCURACY	
Resolution	16 bits
Nonlinearity	Less than 1 LSB
Differential Nonlinearity	Less than 1 LSB
Inherent Quantizing Error	±½ LSB
System Accuracy	To within ±0.003% FSR
Channel Crosstalk	-100dB at 1kHz
Gain Error	Adjustable to 0
Zero Error	Adjustable to 0
DYNAMIC PERFORMANCE	
Channel Acquisition Time to within ½ LSB	8.5µs
A/D Conversion Time	6µs
A/D Throughput to System Memory	100,000 samples per second
Sample & Hold Aperture Uncertainty	.2ns
Sample & Hold Aperture Delay	100ns
Sample & Hold Droop Rate	7.5mV/ms
Sample & Hold Feedthrough Attenuation	94dB at 100kHz
THERMAL CHARACTERISTICS	
A/D Zero Drift	±10 ppm of FSR/°C
Amplifier Zero Drift	±25µV/°C
Gain Drift	±30 ppm of FSR/°C
Differential Linearity Drift	1.5 ppm of FSR/°C
Monotonicity	0 to +70°C

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2.9 DT2828 A/D SUBSYSTEM

A/D MODULE	DT5704
ANALOG INPUTS	
Number of Analog Inputs	4SE
Input Ranges	0 to +10V (unipolar) ±10V (bipolar)
Output Data Codes	Straight binary (unipolar), offset binary, or two's complement (bipolar)
Input Impedance	Off Channel: 10 megohms, 10pF On Channel: 100 megohms, 100pF
Bias Current	±200nA
Maximum Input Voltage without Damage, Power On	±31V
Maximum Input Voltage without Damage, Power Off	±16V
Channel-to-channel Input Voltage Error	10mV
ACCURACY	
Resolution	12 bits
Nonlinearity	less than ±½ LSB
Differential Nonlinearity	less than ±½ LSB
Inherent Quantizing Error	±½ LSB
System Accuracy	to within ±0.03% FSR
Channel Crosstalk	-80dB at 1kHz
Gain Error	Adjustable to 0
Zero Error	Adjustable to 0

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DYNAMIC PERFORMANCE	
Channel Acquisition Time to within ½ LSB	10µs
A/D Conversion Time	4µs
A/D Throughput to System Memory	100,000 samples per second
Sample & Hold Aperture Uncertainty	±5ns
Sample & Hold Aperture Delay	100ns
Sample & Hold Droop Rate	0.5mV/ms
Sample & Hold Feedthrough Attenuation	80dB at 1 kHz
THERMAL CHARACTERISTICS	
A/D Zero Drift	±20 ppm of FSR/°C
Amplifier Zero Drift	±25µV/°C
Gain Drift	±30 ppm of FSR/°C
Differential Linearity Drift	±3 ppm of FSR/°C
Monotonicity	0 to +70°C

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2.10 D/A SUBSYSTEM

NOTE

This section does not apply to the DT2824-PGH and DT2824-PGL models.

ANALOG OUTPUTS

Number of Channels	2, deglitched
Output Ranges (Jumper-selectable)	
All Except DT2823	0 to 5V (unipolar) 0 to 10V (unipolar) ±2.5V, ±5V, ±10V (bipolar)
DT2823	±10V
Output Data Coding (Jumper-selectable)	
All Except DT2823	Straight binary (unipolar) or offset binary (bipolar)
DT2823	Two's complement
Throughput	
All Except DT2823	130kHz max, single channel 260kHz max, aggregate
DT2823	100kHz max, single channel 200kHz max, aggregate
Current Output	±5mA max
Output Impedance	0.1 ohms max
Capacitive Drive Capability	0.004µF
Protection Against	Short circuit to analog common
Glitch Energy	
All Except DT2823	15mV-µs
DT2823	10mV-µs

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ACCURACY	
Resolution	
All Except DT2823	12 bits
DT2823	16 bits
Nonlinearity	
All Except DT2823	To within ±½ LSB
DT2823	To within 1.5 LSB
Differential Nonlinearity	
All Except DT2823	To within ±½ LSB
DT2823	To within 1 LSB
Gain Error	Adjustable to 0
Zero Error	Adjustable to 0
DYNAMIC PERFORMANCE	
Settling Time to 0.01% of FSR	
All Except DT2823	5µs, 20V step 1µs, 100mV step
DT2823	10µs, 20V step 3µs, 100mV step
Slew Rate	
All Except DT2823	10V/µs
DT2823	4V/µs
THERMAL CHARACTERISTICS	
D/A Zero Drift	±10 ppm of FSR/°C
Gain Drift	±30 ppm of FSR/°C
Monotonicity	0 to 70°C

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2.11 DIGITAL I/O SUBSYSTEM

Number of Lines	16
Number of Ports	2, 8-bit each
DIGITAL INPUTS	
Input Type	Level sensitive
Logic Family	LSTTL
Logic Sense	Positive true
Logic Load	1 LSTTL load
Logic High Input Voltage	2.0V minimum
Logic Low Input Voltage	0.8V maximum
Logic High Input Current	20µA maximum
Logic Low Input Current	-0.4mA maximum
Termination	None; unused inputs float
DIGITAL OUTPUTS	
Fanout	30 LSTTL loads
Logic Family	LSTTL
Logic High Output Voltage	2.5V minimum
Logic Low Output Voltage	0.4V maximum
Logic High Output Current	-15mA maximum
Logic Low Output Current	24mA maximum
Throughput	As fast as programmed I/O allows (200kHz benchmark)

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2.12 EXTERNAL TRIGGER

Input Type	Schmitt trigger, enables on TTL logic low
Logic Family	LSTTL
Logic Load	1 LSTTL load
Logic High Input Voltage	2.0V minimum
Logic Low Input Voltage	0.8V maximum
Logic High Input Current	-0.25mA maximum
Logic Low Input Current	25µA maximum
Minimum Pulse Width	
High	100ns
Low	100ns
Maximum Pulse Width	
Low	1µs
Termination	22kΩ pullup to +5V

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2.13 CLOCK

ON-BOARD CLOCK	
Base Frequency	4.00MHz ±0.01%
Prescaler Range	Powers of 2 from 0 to 15 (1 to 32,768)
Divisor Range	Integer values 1 to 256
Usable Frequency Range	4.0µs (250kHz) to 2s (0.5Hz)
EXTERNAL CLOCK	
Input Type	Schmitt trigger, edge sensitive, Clocks on falling edge
Logic Family	LSTTL
Logic Load	1 LSTTL load
Logic High Input Voltage	2.0V minimum
Logic Low Input Voltage	0.8V maximum
Logic High Input Current	-0.25mA maximum
Logic Low Input Current	25µA maximum
Minimum Pulse Width	
High	200ns
Low	200ns
Termination	22kΩ pullup to +5V

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2.14 INTERFACE CHARACTERISTICS

Compatible Bus	IBM Personal Computer AT
Interface Type	I/O mapped with 10-bit addressing
Number of Locations Occupied	8 words reserved
Factory-assigned Base Address	240 (hex), jumper-selectable from 200 (hex) to 3E0 (hex) in increments of 20 (hex)
Interrupts	1 interrupt, jumper-configurable to any of 5 interrupt lines
Interrupt Lines	3, 5, 7, 10, and 15
Factory-assigned Interrupt Level	15
Interrupt Sources	A/D Error, D/A Error, A/D Done, D/A Ready, Trigger Error, and DMA Done
Data Path	16 bits

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2.15 POWER REQUIREMENTS

+5 Volts

DT2821	±5%, @ 2.0A max (1.8A typ)
DT2821-F-16SE	±5%, @ 2.4A max (2.2A typ)
DT2821-F-8DI	±5%, @ 2.4A max (2.2A typ)
DT2821-G-16SE	±5%, @ 2.8A max (2.2A typ)
DT2821-G-8DI	±5%, @ 2.8A max (2.2A typ)
DT2823	±5%, @ 2.7A max (2.5A typ)
DT2824-PGH	±5%, @ 1.5A max (1.2A typ)
DT2824-PGL	±5%, @ 1.5A max (1.2A typ)
DT2825	±5%, @ 2.0A max (1.8A typ)
DT2827	±5%, @ 2.7A max (2.5A typ)
DT2828	±5%, @ 2.2A max (2.0A typ)

2.16 PHYSICAL/ENVIRONMENTAL

Dimensions	4.5"H X 13.25"W X 0.75"D (11.4 X 33.7 X 1.9 cm)
Weight	20 ounces (567g)
Storage Temperature Range	-13 to +185°F (-25 to +85°C)
Relative Humidity	To 95%, non-condensing

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2.17 CONNECTORS AND CABLES

Compatible Connectors J1	50-pin 3M, user-supplied (Ansley 609-5030 or equivalent; Ansley 609-5031, or equivalent strain relief recommended)
Compatible Cable Assemblies J1	EP035; plugs into J1; not required if DT707 or DT752 used
Compatible Screw Terminal Panels	DT707 and DT752; contain integral cable assembly and connector; plug into J1

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CHAPTER 3
GETTING STARTED

INTRODUCTION
JUMPERS
BASE ADDRESS
DMA CHANNEL
INTERRUPT LEVEL
A/D FUNCTIONS
D/A FUNCTIONS
JUMPER SUMMARY

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3.1 INTRODUCTION

Before installing the DT2821 series board into the IBM Personal Computer AT backplane, you should configure a number of parameters which are jumper-selectable on the DT2821 series boards. These parameters are selected by the addition or removal of jumpers. The parameters include single-ended or differential inputs (for the DT2821 only); analog output voltage ranges; unipolar or bipolar inputs; unipolar or bipolar outputs; DMA channel selection; interrupt level selection; and board base address selection.

3.2 JUMPERS

All jumpers are installed by adding a wire, or inserting a jumper plug, between wire wrap posts. Jumpers in this manual are designated by an upper case "W", followed by a number. In all cases, installing a jumper consists of connecting a pair of posts; and removing a jumper consists of removing the wire or jumper plug which connects the posts together. A single jumper number refers to a pair of posts. Installing W14, for example, consists of connecting together the pair of posts designated by the single number.

3.2.1 SHARED POST JUMPERS

Some of the jumpers on the DT2821 series boards share the same jumper posts. Only one connection should be made to any jumper post at any one time. Two jumpers which share any particular post are never installed at the same time. The shared post design makes it impossible to install two jumpers illegally when using jumper plugs. The connections of these shared post jumpers are detailed in Figure 3-1.

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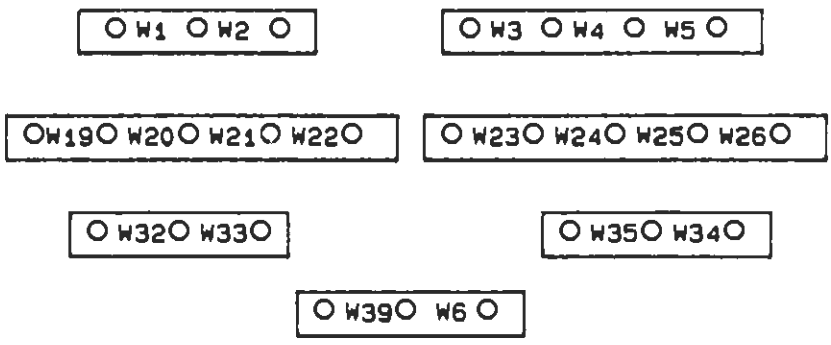


FIGURE 3-1: SHARED POST JUMPERS

Jumper locations are given in the configuration diagram (Figure 3-2). They are also indicated in silkscreen on the component side of the DT2821 series boards.

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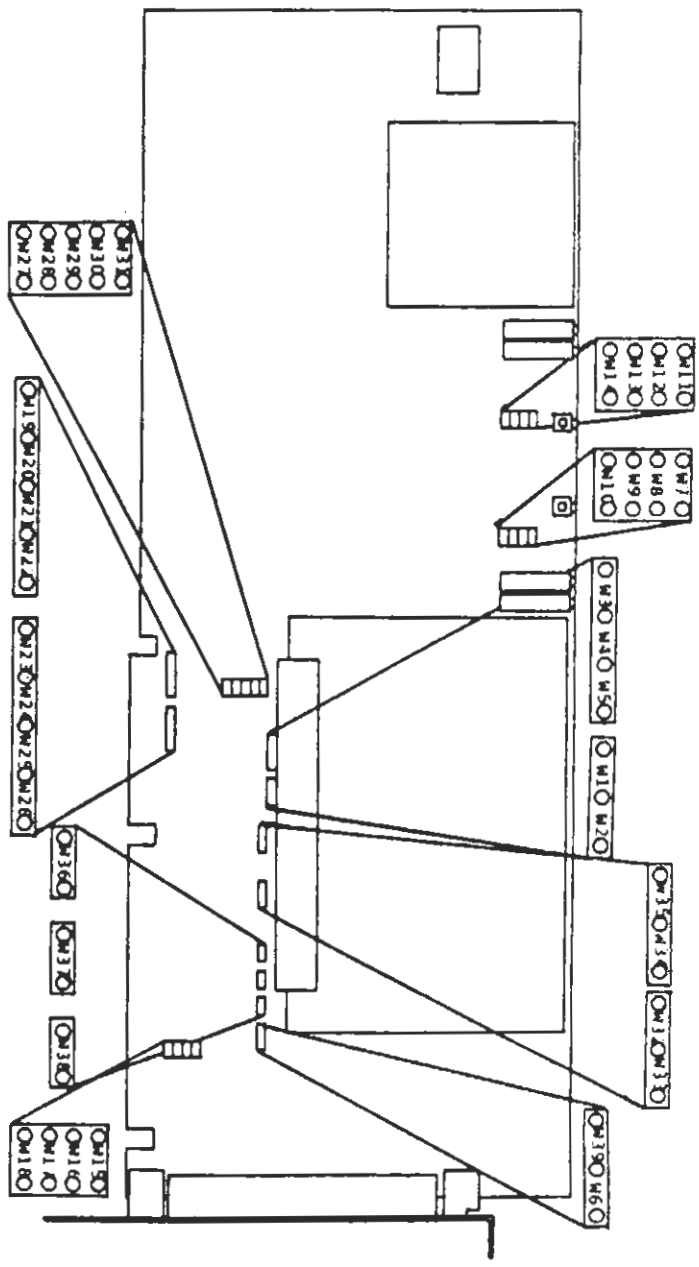


FIGURE 3-2: JUMPER LOCATIONS

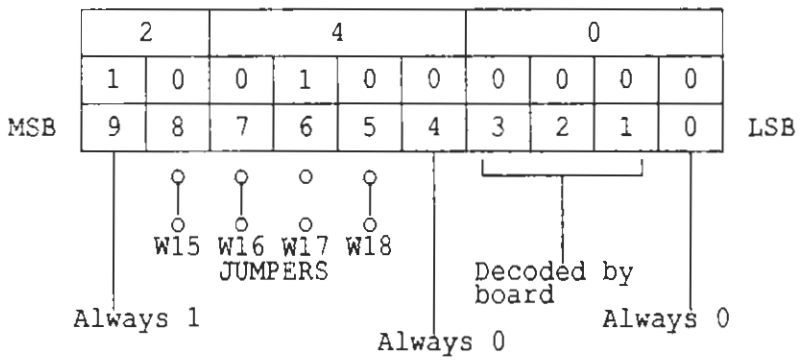
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3.3 BASE ADDRESS

The base address is the lowest I/O address location used by the DT2821 series board. Four jumpers (W15, W16, W17, and W18) allow you to set the base address anywhere between 200 (hex) and 3E0 (hex) in increments of 20 (hex). Figure 3-3 indicates how these jumpers can be used to select a base address. The figure shows the factory-shipped address of 240 (hex).

IMPORTANT

Each address location used by a DT2821 series board must be unused by any other device in the system, INCLUDING ANOTHER DT2821 SERIES BOARD. Multiple DT2821 series boards must be set to different base addresses, and must not occupy address locations used by other devices in the IBM Personal Computer AT system.



NOTES
- Bits 10 through 19 are not used.
- Installing a jumper selects the value of 0 for the bit it controls; removing the jumper sets the bit to a value of 1.
- Address bits 1, 2, and 3 are decoded on the DT2821 series board to select one of eight on-board registers.
- Address bit 0 is always 0 to provide word addresses.

FIGURE 3-3: JUMPER SETTING FOR BASE ADDRESS

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Recommended base addresses (in hex) are shown in Table 3-1.

TABLE 3-1: RECOMMENDED BASE ADDRESSES

BASE ADDRESS	JUMPERS W15	W16	W17	W18
200	In	In	In	In
220	In	In	In	Out
240 (FC)	In	In	Out	In
260	In	In	Out	Out
280	In	Out	In	In
2A0	In	Out	In	Out
2C0	In	Out	Out	In
2E0	In	Out	Out	Out
300	Out	In	In	In
320	Out	In	In	Out
340	Out	In	Out	In
380	Out	Out	In	In
3A0	Out	Out	In	Out
3E0	Out	Out	Out	Out

FC is Factory Configuration

3.4 DMA CHANNEL

The DT2821 series board allows you to select the IBM Personal Computer AT DMA channel or channels the board uses when performing DMA transfers. The DT2821 series board can be jumpered for two DMA channels, if two channels are available. The second DMA channel is only used when Dual-DMA mode is selected. The DT2821 series board can be jumpered to operate on DMA channel 5 (highest priority), 6, or 7 (lowest priority). Channel 5 or 6 can be selected as the first DMA channel using a jumper plug, but channel 7 must be selected with a wire wrap. Channel 6 or 7 can be selected as the second DMA channel using a jumper plug, but channel 5 must be selected with a wire wrap. The factory configuration selects channel 5 as the first DMA channel and channel 6 as the second DMA channel.

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IMPORTANT

Each DMA channel used by any board in the system must be unused by any other board in the IBM Personal Computer AT, INCLUDING ANOTHER DT2821 SERIES BOARD. Multiple DT2821 series boards must be set to different DMA channels, limiting the use of Dual-DMA to only one DT2821 series board. The other DT2821 series boards can only use single channel DMA as long as there is a channel available. The maximum configuration would be three boards doing single-channel DMA.

Jumpers W19, W20, W21, and W22 select the first and second DMA request channels. Jumpers W23, W24, W25, and W26 select the DMA acknowledge channels. Table 3-2 shows the jumper schemes for connecting to the first and second DMA channel.

TABLE 3-2: DMA CHANNEL SELECTION

	FIRST DMA CHANNEL				SECOND DMA CHANNEL			
CHANNEL	W19	W20	W23	W24	W21	W22	W25	W26
5[1]	In	Out	In	Out	Out	Out	Out	Out
6	Out	In	Out	In	In	Out	In	Out
7[2]	Out	Out	Out	Out	Out	In	Out	In
none	Out	Out	Out	Out	Out	Out	Out	Out

NOTES
1. To select channel 5 as the second DMA channel, you must use a wire wrap. See Figure 3-4 for details. Channel 5 is selected at the factory for the first DMA channel and Channel 6 is selected at the factory for the second DMA channel.
2. To select channel 7 as the first DMA channel, you must use a wire wrap. See Figure 3-4 for details.

The DMA request channel must be equal to the DMA acknowledge channel. Figure 3-4 shows the arrangement for the request and acknowledge configuration jumpers. If W19 is installed, W23 must be installed also to select channel 5 as the first DMA channel. If W20 is installed, W24 must be installed also to select channel 6 as the first DMA channel. If W21 is installed, W25 must be installed

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also to select channel 6 as the second DMA channel. If W22 is installed, W26 must be installed also to select channel 7 as the second DMA channel.

To select channel 5 as the second DMA channel, jumper the left post for W19 to the left post of W22 (which is also the right post for W21). Make sure you also jumper the left post of W23 to the left post of W26 (which is the right post of W25).

To select channel 7 as the first DMA channel, jumper the right post of W22 to the right post of W19 (which is also the left post of W20). Make sure you also jumper the right post of W26 to the right post of W23 (which is also the left post of W24).

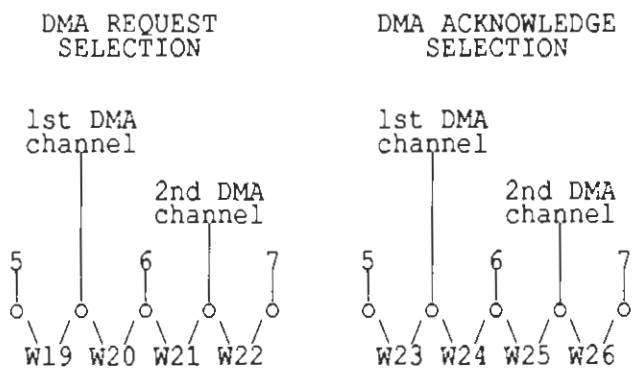


FIGURE 3-4: DMA CHANNEL SELECTION JUMPERS

3.5 INTERRUPT LEVEL

The DT2821 series board can interrupt the processor on any one of five different levels. The order of priority for these five levels is interrupt level 10 (highest), 15, 3, 5, and 7 (lowest). The factory configuration is interrupt level 15. The DT2821 series board generates one interrupt, no matter what the cause. It's up to the interrupt service routine to determine the cause of the interrupt by polling the ADCSR, DACSR, and SUPCSR. Once the cause of the interrupt is found, the interrupt service routine can take proper action.

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IMPORTANT

Each interrupt level used by a board in the IBM Personal Computer AT must be unused by any other device, INCLUDING ANOTHER DT2821 SERIES BOARD. Multiple DT2821 series boards must be set to different interrupt levels, if any are available. Any DT2821 series board that does not use interrupts should disable interrupts by removing W27, W28, W29, W30, and W31.

Table 3-3 shows the jumper settings for the interrupt levels.

TABLE 3-3: INTERRUPT LEVEL SELECTION

INTERRUPT LEVEL	JUMPERS W27	W28	W29	W30	W31
10	In	Out	Out	Out	Out
15 (FC)	Out	In	Out	Out	Out
3	Out	Out	In	Out	Out
5	Out	Out	Out	In	Out
7	Out	Out	Out	Out	In
none	Out	Out	Out	Out	Out

FC is factory configuration

3.6 A/D FUNCTIONS

The analog-to-digital section can be jumper-selected for unipolar or bipolar operation; binary, offset binary, or two's complement coding; and single-ended or differential input. The next sections describe the configuration of the A/D on different models of the DT2821 series boards.

3.6.1 INPUT RANGE

Some DT2821 series boards permit selection of unipolar or bipolar input ranges. If the board is configured for unipolar inputs, it should be used with positive voltages only. If configured for bipolar inputs, the board accepts both positive and negative voltages.

Table 3-4 indicates which DT2821 series boards have user-selectable input ranges, and which do not. The factory-shipped configuration is bipolar (+/-10V) for all models.

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TABLE 3-4: DT2821 SERIES INPUT RANGES

MODEL NUMBER	USER-SELECTABLE
DT2821	Yes
DT2821-F-16SE	Yes
DT2821-F-8DI	Yes
DT2821-G-16SE	Yes
DT2821-G-8DI	Yes
DT2823	No
DT2824-PGH	Yes
DT2824-PGL	Yes
DT2825	Yes
DT2827	No
DT2828	Yes

Table 3-5 indicates the jumper selection of the unipolar/bipolar input range.

TABLE 3-5: SELECTION OF INPUT RANGE

INPUT RANGE	JUMPERS W1	W2	W40
Bipolar			
DT2821-G-16SE, ±10V (FC)	Out	In	Out
DT2821-G-8DI, ±10V (FC)	Out	In	Out
DT2821-G-16SE, ±5V	Out	In	In
DT2821-G-8DI, ±5V	Out	In	In
All other models (FC)	Out	In	In
Unipolar			
DT2821-G-16SE	Out	Out	In
DT2821-G-8DI	Out	Out	In
All other models	In	Out	In

FC is factory configuration

NOTE

When changing the input range, you must recalibrate the A/D converter. See Appendix B for the calibration procedure.

The input range and the output coding (see next section) selected for the A/D converter should be compatible. Bipolar inputs require either offset binary or two's complement output coding. For unipolar inputs, straight binary output coding should be used.

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3.6.2 CODING

At the end of an A/D conversion, the incoming analog input signal has been changed into an equivalent digital output which permits analog input information to be understood and manipulated by the IBM Personal Computer AT processor. The output of the DT2821 series board is a binary data word, the coding of which depends on the converter module and board jumper configuration.

Unipolar input ranges should be used with straight binary output code. Bipolar input ranges can be represented using either offset binary or two's complement binary coding. Table 3-6 indicates which codes are available on each model. All models except the DT2823 and DT2827 are shipped in offset binary coding. The output coding on the DT2823 and DT2827 is not selectable. These two boards are shipped in two's complement binary coding.

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TABLE 3-6: DT2821 SERIES CODING

MODEL NUMBER	CODING AVAILABLE
DT2821 (FC)	Straight Binary Offset Binary Two's Complement
DT2821-F-16SE (FC)	Straight Binary Offset Binary Two's Complement
DT2821-F-8DI (FC)	Straight Binary Offset Binary Two's Complement
DT2821-G-16SE (FC)	Straight Binary Offset Binary Two's Complement
DT2821-G-8DI (FC)	Straight Binary Offset Binary Two's Complement
DT2823 (FC)	Two's Complement
DT2824-PGH (FC)	Straight Binary Offset Binary Two's Complement
DT2824-PGL (FC)	Straight Binary Offset Binary Two's Complement
DT2825 (FC)	Straight Binary Offset Binary Two's Complement
DT2827 (FC)	Two's Complement
DT2828 (FC)	Straight Binary Offset Binary Two's Complement

FC is factory configuration

Table 3-7 indicates the jumper configuration required to select straight binary, offset binary, or two's complement coding. The DT2823 and DT2827 are jumpered for two's complement binary, and cannot be reconfigured.

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TABLE 3-7: CODING SELECTION

OUTPUT CODE	JUMPERS W32	W33	W34	W35	W36	W37	W38	W39
Straight Binary	In	Out	Out	In	In	In	In	Out
Offset Binary(FC)	In	Out	Out	In	In	In	In	Out
Two's Complement Selectable Models	Out	In	In	Out	In	In	In	Out
Two's Complement DT2823	In	Out	In	Out	Out	Out	Out	In
Two's Complement DT2827	In	Out	In	Out	Out	Out	Out	In

FC is factory configuration

3.6.3 SE/DI

The DT2821 series boards can accept inputs in either single-ended input or differential input mode. In single-ended mode, DT2821, DT2821-F-16SE, DT2821-G-16SE DT2824-PGH, DT2824-PGL, and DT2825 make 16 channels available for 16 different signals with a common return path. In differential input mode, each signal has a separate return path, thus reducing the number of input signals to 8 on the DT2821, DT2821-F-8DI, DT2821-G-8DI, DT2824-PGH, DT2824-PGL and DT2825. The DT2823 and DT2827 each have 4 differential channels and the DT2828 has 4 single-ended channels. Table 3-8 specifies the input mode for each DT2821 series board.

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TABLE 3-8: DT2821 SERIES INPUT MODES

MODEL NUMBER	AVAILABLE MODES
DT2821 (FC)	Single-ended Differential
DT2821-F-16SE	Single-ended
DT2821-F-8DI	Differential
DT2821-G-16SE	Single-ended
DT2821-G-8DI	Differential
DT2823	Differential
DT2824-PGH (FC)	Single-ended Differential
DT2824-PGL	Single-ended
(FC)	Differential
DT2825	Single-ended
(FC)	Differential
DT2827	Differential
DT2828	Single-ended

FC is factory configuration

Table 3-9 indicates the jumper configuration required to select SE or DI input mode for the DT2821 series boards. Only the DT2821, DT2824-PGH, DT2824-PGL, and DT2825 have user-selectable input modes. The input mode configuration for the other boards is selected at the factory and should not be changed.

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TABLE 3-9: INPUT MODE SELECTION

MODEL NUMBER	JUMPERS W3	W4	W5	W6
DT2821				
Single-ended (FC)	In	Out	In	Out
Differential	Out	In	Out	In
DT2821-F-16SE	In	Out	In	Out
DT2821-F-8DI	Out	In	Out	In
DT2821-G-16SE	In	Out	In	Out
DT2821-G-8DI	Out	In	Out	In
DT2823	Out	In	Out	Out
DT2824-PGH				
Single-ended (FC)	In	Out	In	Out
Differential	Out	In	Out	In
DT2824-PGL				
Single-ended	In	Out	In	Out
Differential (FC)	Out	In	Out	In
DT2825				
Single-ended	In	Out	In	Out
Differential (FC)	Out	In	Out	In
DT2827	Out	In	Out	Out
DT2828	Out	Out	In	Out

FC is factory configuration

3.7 D/A FUNCTIONS

NOTE

This section does not apply to the DT2824-PGH and DT2824-PGL models.

The DT2821 series boards permit the selection of unipolar or bipolar output ranges separately for each of the two on-board DACs. If a DAC is configured for unipolar operation, it outputs positive voltages only. If configured for bipolar operation, a DAC can output either positive or negative voltages within its selected range (±10V, ±5V, or ±2.5V).

Tables 3-10 and 3-11 indicate jumper selections for the output range for each DAC and the factory configuration. When jumpered for unipolar operation, the DT2821 series board expects digital data in straight binary coding. When set for bipolar mode, the DT2821 series board expects

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digital data in offset binary coding only.

TABLE 3-10: DAC 0 OUTPUT RANGE SELECTION

DAC 0 OUTPUT RANGE	JUMPERS W7	W8	W9	W10
±10 Volts(FC)	Out	Out	In	In
±5 Volts	Out	In	In	Out
±2.5 Volts	In	In	In	Out
0 to 10 Volts	Out	In	Out	Out
0 to 5 Volts	In	In	Out	Out

FC is factory configuration

TABLE 3-11: DAC 1 OUTPUT RANGE SELECTION

DAC 1 OUTPUT RANGE	JUMPERS W11	W12	W13	W14
±10 Volts(FC)	Out	Out	In	In
±5 Volts	Out	In	In	Out
±2.5 Volts	In	In	In	Out
0 to 10 Volts	Out	In	Out	Out
0 to 5 Volts	In	In	Out	Out

FC is factory configuration

When changing the output range, you must recalibrate the D/A converter. See Appendix B for calibration procedures. Note that the DT2823 DACs operate at the input range of ±10V only and they accept data in two's complement binary coding.

3.8 JUMPER SUMMARY

Table 3-12 provides a summary of the jumpers used on the DT2821 series boards. The table lists the jumpers in numerical order, states whether the jumper is user-configurable ("X"), and lists the factory-configuration (In or Out).

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TABLE 3-12: JUMPER SUMMARY

JUMPER	DT2821/ DT2824- PGH	DT2824- PGL/ DT2825	DT2821- F-16SE/ DT2821- G-16SE	DT2821- F-8DI/ DT2821- G-8DI	DT2823 DT2827	DT2828
W1	X(Out)	X(Out)	X(Out)	X(Out)	Out	X(Out)
W2	X(In)	X(In)	X(In)	X(In)	In	X(In)
W3	X(In)	X(Out)	In	Out	Out	Out
W4	X(Out)	X(In)	Out	In	In	Out
W5	X(In)	X(Out)	In	Out	Out	In
W6	X(Out)	X(In)	Out	In	Out	Out
W7	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)
W8	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)
W9	X(In)	X(In)	X(In)	X(In)	X(In)	X(In)
W10	X(In)	X(In)	X(In)	X(In)	X(In)	X(In)
W11	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)
W12	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)
W13	X(In)	X(In)	X(In)	X(In)	X(In)	X(In)
W14	X(In)	X(In)	X(In)	X(In)	X(In)	X(In)
W15	X(In)	X(In)	X(In)	X(In)	X(In)	X(In)
W16	X(In)	X(In)	X(In)	X(In)	X(In)	X(In)
W17	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)
W18	X(In)	X(In)	X(In)	X(In)	X(In)	X(In)
W19	X(In)	X(In)	X(In)	X(In)	X(In)	X(In)
W20	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)
W21	X(In)	X(In)	X(In)	X(In)	X(In)	X(In)
W22	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)
W23	X(In)	X(In)	X(In)	X(In)	X(In)	X(In)
W24	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)
W25	X(In)	X(In)	X(In)	X(In)	X(In)	X(In)
W26	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)
W27	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)
W28	X(In)	X(In)	X(In)	X(In)	X(In)	X(In)
W29	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)
W30	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)
W31	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)	X(Out)
W32	X(In)	X(In)	X(In)	X(In)	In	X(In)
W33	X(Out)	X(Out)	X(Out)	X(Out)	Out	X(Out)
W34	X(Out)	X(Out)	X(Out)	X(Out)	In	X(Out)
W35	X(In)	X(In)	X(In)	X(In)	Out	X(In)
W36	X(In)	X(In)	X(In)	X(In)	Out	X(In)
W37	X(In)	X(In)	X(In)	X(In)	Out	X(In)
W38	X(In)	X(In)	X(In)	X(In)	Out	X(In)
W39	X(Out)	X(Out)	X(Out)	X(Out)	In	X(Out)
W40	In	In	In/X(Out)	In/X(Out)	In	In

NOTE

Jumpers W7 through W14 are not installed on the DT2824-PGH and DT2824-PGL models.

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CHAPTER 4
INSTALLATION AND USER CONNECTIONS

INSTALLING THE DT2821 SERIES BOARD

USER CONNECTIONS

SINGLE-ENDED AND DIFFERENTIAL INPUTS

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4.1 INSTALLING THE DT2821 SERIES BOARD

The DT2821 series board is installed into the IBM Personal Computer AT backplane the same way as any other board-level option, such as the IBM Monochrome Display or Parallel Printer Adapter. The literature supplied with the IBM Personal Computer AT describes the board installation procedure in detail.

The following discussion summarizes the installation procedure for the DT2821 series board.

PRELIMINARY STEPS

1. Turn off the IBM Personal Computer AT.
2. Turn off all accessories (printer, modem, monitor, and so on) connected to the IBM Personal Computer AT.
3. Make sure the Key Lock is unlocked (turn the key counterclockwise and remove the key).
4. Unplug the entire system, including all options, from wall outlets.
5. Unplug all cables from the rear of the computer.

BOARD INSTALLATION

1. Remove the back panel (if attached) from the rear of the IBM Personal Computer AT. This is attached with velcro fastener strips.
2. Unscrew the five cover mounting screws located on the four corners and the top middle of the computer's rear panel.
3. Gently remove the computer's cover, sliding it from the rear to the front of the computer until it goes no further; then tilt the front of the cover up diagonally and remove the cover from the system's base. Situated at the inside left rear on the IBM Personal Computer AT are six fully bussed expansion slots and two 8-bit bussed expansion slots. The DT2821 series board must be installed in a fully bussed slot.

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4. Remove the blank expansion slot cover, saving the screw which held it in place.

5. With the DT2821 series board's retaining bracket facing the expansion slot plate on the IBM Personal Computer AT's rear panel, and the board's P1 connector positioned by the computer's rear panel, firmly press the board into the chosen expansion slot.

6. Align the DT2821 series board's retaining bracket with the expansion slot plate on the IBM's rear panel and replace the screw, tightening it clockwise.

7. Replace the IBM Personal Computer AT's cover. Tilt the cover up and slide it onto the system's base, making sure the cover is under the rail on the frame. Install the five cover mounting screws. Reattach the back panel to the IBM Personal Computer AT by pressing the panel in place.

4.2 USER CONNECTIONS

The DT2821 series board has three connectors, labeled P1, P2, and J1. P1 and P2 connect the board to the IBM Personal Computer AT bus. All P1 and P2 connections are made automatically when the DT2821 series board is installed into the backplane of the IBM Personal Computer AT. All user connections to the DT2821 series board (including analog inputs, analog outputs, digital inputs and outputs, an external trigger, and an external clock) are made using connector J1 on the board. The pin assignments for P1 and P2 are given in Appendix A. The J1 pin assignments are given in Table 4-1 for the DT2821, DT2821-F-16SE, DT2821-F-8DI, DT2821-G-16SE, DT2821-G-8DI, DT2824-PGH, DT2824-PGL, and DT2825 boards. Table 4-2 shows the J1 pin assignments for the DT2823 and DT2827, and Table 4-3 shows the J1 pin assignments for the DT2828.

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TABLE 4-1: J1 PIN ASSIGNMENTS FOR THE DT2821, DT2821-F-16SE, DT2821-F-8DI, DT2821-G-16SE, DT2821-G-8DI, DT2824-PGH, DT2824-PGL, and DT2825

SIGNAL NAME	PIN #		SIGNAL NAME
Channel 0	1	2	Channel 8 (0 Ret)
Channel 1	3	4	Channel 9 (1 Ret)
Channel 2	5	6	Channel 10 (2 Ret)
Channel 3	7	8	Channel 11 (3 Ret)
Channel 4	9	10	Channel 12 (4 Ret)
Channel 5	11	12	Channel 13 (5 Ret)
Channel 6	13	14	Channel 14 (6 Ret)
Channel 7	15	16	Channel 15 (7 Ret)
AGND	17	18	Amp Low
+15V Out	19	20	-15V Out
PGND	21	22	DAC 0 Out
DAC 0 GND	23	24	DAC 1 Out
DAC 1 GND	25	26	DGND
DGND	27	28	DIO Port 0, Bit 0
DIO Port 0, Bit 1	29	30	DIO Port 0, Bit 2
DIO Port 0, Bit 3	31	32	DGND
DIO Port 0, Bit 4	33	34	DIO Port 0, Bit 5
DIO Port 0, Bit 6	35	36	DIO Port 0, Bit 7
DGND	37	38	DIO Port 1, Bit 0
DIO Port 1, Bit 1	39	40	DIO Port 1, Bit 2
DIO Port 1, Bit 3	41	42	DGND
DIO Port 1, Bit 4	43	44	DIO Port 1, Bit 5
DIO Port 1, Bit 6	45	46	DIO Port 1, Bit 7
DGND	47	48	DGND
External Trigger In	49	50	External Clock In

NOTE
- The ±15V on pins 19 and 20 is intended only to power active circuitry on Data Translation screw terminal panels. Very limited current is available. The ±15V should not be used to power external, user-supplied circuits.

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TABLE 4-2: J1 PIN ASSIGNMENTS FOR DT2823 AND DT2827

SIGNAL NAME	PIN #		SIGNAL NAME
Channel 0	1	2	Channel 0 Return
N/C	3	4	N/C
Channel 1	5	6	Channel 1 Return
N/C	7	8	N/C
Channel 2	9	10	Channel 2 Return
N/C	11	12	N/C
Channel 3	13	14	Channel 3 Return
N/C	15	16	N/C
AGND	17	18	N/C
+15V Out	19	20	-15V Out
PGND	21	22	DAC 0 Out
DAC 0 GND	23	24	DAC 1 Out
DAC 1 GND	25	26	DGND
DGND	27	28	DIO Port 0, Bit 0
DIO Port 0, Bit 1	29	30	DIO Port 0, Bit 2
DIO Port 0, Bit 3	31	32	DGND
DIO Port 0, Bit 4	33	34	DIO Port 0, Bit 5
DIO Port 0, Bit 6	35	36	DIO Port 0, Bit 7
DGND	37	38	DIO Port 1, Bit 0
DIO Port 1, Bit 1	39	40	DIO Port 1, Bit 2
DIO Port 1, Bit 3	41	42	DGND
DIO Port 1, Bit 4	43	44	DIO Port 1, Bit 5
DIO Port 1, Bit 6	45	46	DIO Port 1, Bit 7
DGND	47	48	DGND
External Trigger In	49	50	External Clock In

NOTE
- o The ±15V on pins 19 and 20 is intended only to power active circuitry on Data Translation screw terminal panels. Very limited current is available. The ±15V should not be used to power external, user-supplied circuits.
- o N/C means no connection.

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TABLE 4-3: J1 PIN ASSIGNMENTS FOR THE DT2828

SIGNAL NAME	PIN #		SIGNAL NAME
Channel 0	1	2	AGND
N/C	3	4	N/C
Channel 1	5	6	AGND
N/C	7	8	N/C
Channel 2	9	10	AGND
N/C	11	12	N/C
Channel 3	13	14	AGND
N/C	15	16	N/C
AGND	17	18	N/C
+15V Out[1]	19	20	-15V Out[1]
PGND	21	22	DAC 0 Out
DAC 0 GND	23	24	DAC 1 Out
DAC 1 GND	25	26	DGND
DGND	27	28	DIO Port 0, Bit 0
DIO Port 0, Bit 1	29	30	DIO Port 0, Bit 2
DIO Port 0, Bit 3	31	32	DGND
DIO Port 0, Bit 4	33	34	DIO Port 0, Bit 5
DIO Port 0, Bit 6	35	36	DIO Port 0, Bit 7
DGND	37	38	DIO Port 1, Bit 0
DIO Port 1, Bit 1	39	40	DIO Port 1, Bit 2
DIO Port 1, Bit 3	41	42	DGND
DIO Port 1, Bit 4	43	44	DIO Port 1, Bit 5
DIO Port 1, Bit 6	45	46	DIO Port 1, Bit 7
DGND	47	48	DGND
External Trigger In	49	50	External Clock In

NOTES
- o The ±15V on pins 19 and 20 is intended only to power active circuitry on Data Translation screw terminal panels. Very limited current is available. The ±15V should not be used to power external, user-supplied circuits.
- o N/C means no connection.

4.3 SINGLE-ENDED AND DIFFERENTIAL INPUTS

With single-ended A/D inputs, the return sides of all the analog channels are connected together to the low point of the board's analog input circuitry (amp low). The high side of each analog input is connected to its own input in the multiplexer circuit built into the board's A/D converter.

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In single-ended input mode, the voltage the board's A/D input amplifier sees equals:

INPUT VOLTAGE = V(CHAN HIGH) - V(AMP LOW)

For the DT2828, V(AMP LOW) is replaced with V(AGND).

Single-ended inputs have the advantage of providing maximum channel density. Because the DT2821 series boards (except the DT2827 and the DT2828) have 16 multiplexer switches, in single-ended operation the board can accommodate 16 A/D channels. The DT2828 has 4 multiplexer switches and can accomodate 4 A/D channels. The disadvantage to single-ended inputs, however, is that they are sensitive to noise picked up through the input cables. Single-ended connections should be restricted to applications with high level voltage inputs (full scale input range >1V) and short input lead lengths (<15 feet).

When a DT2821 series board with differential inputs is used, both the return side and the high side of each analog channel require a separate multiplexer switch. The board's input amplifier is operated in differential mode, where the voltage the amplifier sees on its input equals:

INPUT VOLTAGE = V(CHAN HIGH) - V(CHAN RET)

In differential operation, the amplifier sees only the "difference" in voltage between the high end of the input channel (CHAN HIGH) and the return side of the input channel (CHAN RET).

Differential connections have the advantage of reducing common mode noise (noise in the form of voltages common to both sides of the analog input). The amplifier built into the board's A/D converter has a Common Mode Rejection Ratio (CMRR) of 80dB[1] at a gain of one. This means that, in differential input mode, the board's analog inputs are 10,000 times less sensitive to voltages common to both sides of the input than they are to voltage

---

[1] A differential amplifier's Common Mode Rejection Ratio (CMRR) can be calculated by the following equation:

$$CMRR = 20 \log(10) \frac{DG}{CMG}$$

where DG is the differential gain and CMG is the amplifier's common mode gain.

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differences between the two sides of the input.

Differential inputs have the disadvantage of relatively low channel density. Because each analog channel uses two multiplexer switches, a DT2821 series board with differential inputs can accommodate only 8 analog input channels (except the DT2727 which can accommodate only 4 differential analog input channels).

Figure 4-1 through 4-3 illustrate some connection schemes used on the DT2821 series boards. Figure 4-1 shows the connection of sixteen single-ended channels; Figure 4-2 shows how a 4-channel single-ended connection is made; Figure 4-3 illustrates an 8-channel differential connection.

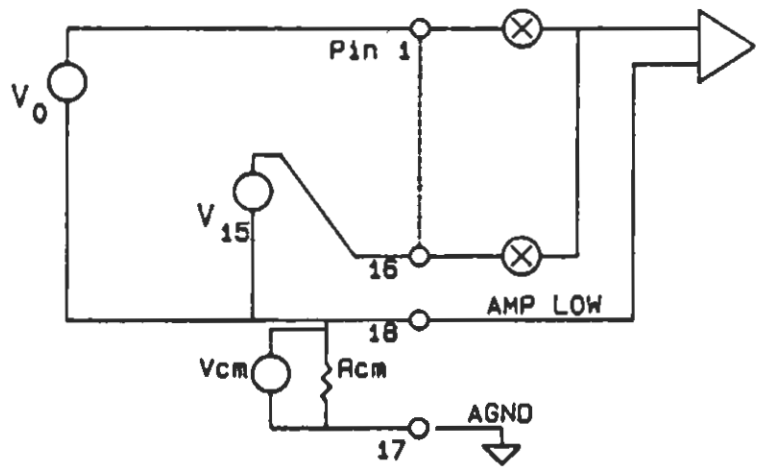


FIGURE 4-1: 16-CHANNEL SINGLE-ENDED CONNECTION

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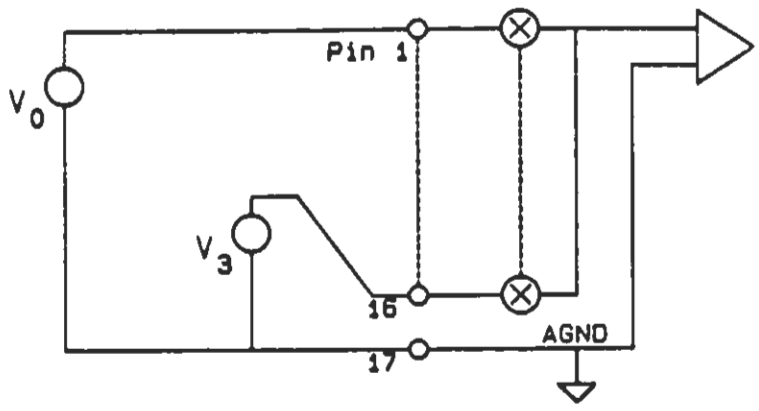


FIGURE 4-2: 4-CHANNEL SINGLE-ENDED CONNECTION

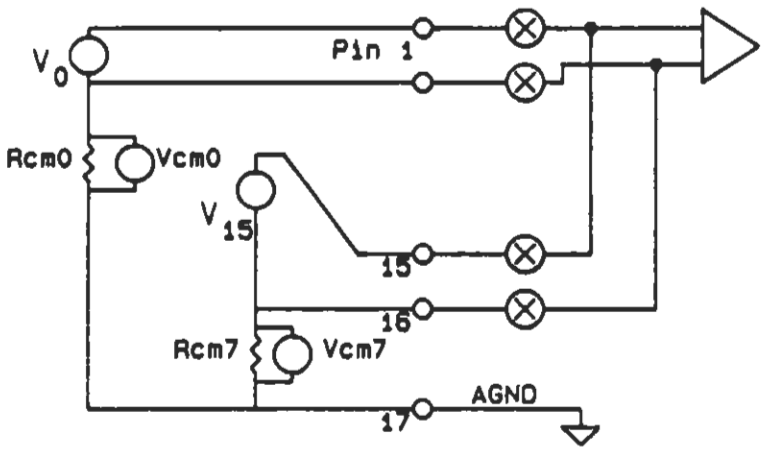


FIGURE 4-3: 8-CHANNEL DIFFERENTIAL CONNECTION

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CHAPTER 5
INTERFACE REGISTERS

INTRODUCTION
A/D CONTROL/STATUS REGISTER
CHANNEL-GAIN LIST CONTROL/STATUS REGISTER
A/D DATA REGISTER
D/A CONTROL/STATUS REGISTER
D/A DATA REGISTER
DIO DATA REGISTER
SUPERVISORY CONTROL/STATUS REGISTER
PACER CLOCK REGISTER

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5.1 INTRODUCTION

Eight interface registers are provided on the DT2821 series board for control, data transfer, and status functions. These registers are accessible in the I/O addressing area. The base register (ADCSR) address is jumper-selectable from 200 (hex) to 3E0 (hex) in increments of 20 (hex). All registers are 16-bits wide, and are word-accessible only.

All registers are fully described in this chapter, and are listed in Table 5-1. Register addresses are described as offsets from a user-selected base address.

TABLE 5-1: REGISTER ADDRESS ALLOCATIONS

ADDRESS BASE + (HEX)	REGISTER NAME	ACCESS
0	A/D Control/Status	R/W
2	Channel-Gain List Control/Status	R/W
4	A/D Data	Read
6	D/A Control/Status	R/W
8	D/A Data	Write
A	DIO Data	R/W
C	Supervisory Control/Status	R/W
E	Pacer Clock	R/W

The following sections contain explicit descriptions of each interface register and its program application. Conditions which set or clear each structure (bit or field) are shown.

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5.2 A/D CONTROL/STATUS REGISTER

The ADCSR is a read/write register that interfaces to and controls the A/D section of the board. This register:

- Enables the A/D Done Interrupt
- Reports an error condition
- Reports a done condition
- Reports a multiplexer busy condition
- Enables the pacer clock to start A/D conversions
- Is used to load the RAM channel-gain list.

Figure 5-1 gives the bit assignments of the ADCSR.

NAME: A/D Control/Status
MNEMONIC: ADCSR
ADDRESS: Base address + 0
ACCESS: R/W

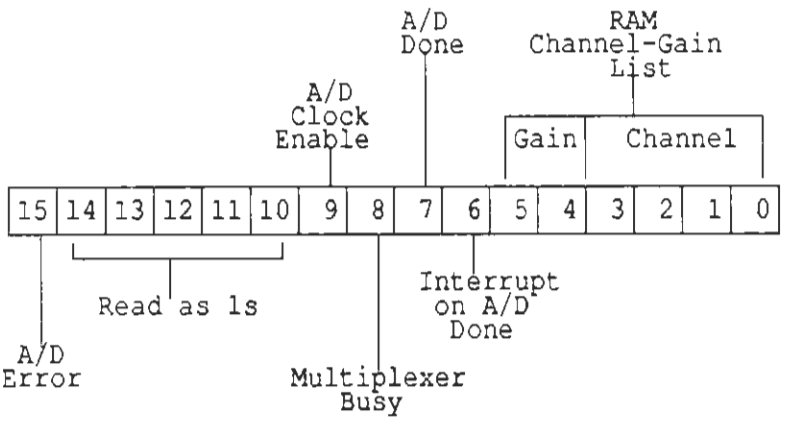


FIGURE 5-1: ADCSR BIT ASSIGNMENTS

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Bit 15 - A/D Error (A/DERR), Read only
This bit indicates an error has occurred from one of the following causes:

- Attempting any A/D conversion while the module is busy. The module is busy for a specified time that is dependent on each module used. Since the multiplexer settling time is overlapped with the A/D conversion, whenever the signal MUXBUSY (bit 8) is 1, an A/D clock (either internal or external) sets the error bit. This is a clock error.

- Attempting any A/D conversion while the DMA pipeline is full. The pipeline being full implies that both the module buffer and the on-board data buffer are currently occupied by valid data. This is a data overrun error.

- Attempting to trigger the DT2821 series board while SCDN (bit 8 of the SUPCSR) is clear (the DT2821 series board is currently in a triggered scan). Another trigger before the scan is finished causes an A/D error. Check to make sure SCDN is set before triggering the scan.

- Attempting to trigger the DT2821 series board while doing non-scan DMA (A/D or D/A). One trigger enables the pacer clock for the entire DMA transfer. In A/D clocked DMA or D/A clocked DMA mode, do not trigger the board when DMA Done (SUPCSR bit 15) is clear. This is a trigger overrun error.

This bit is cleared on bus reset, board initialization, or by setting ADCINIT (bit 6 in the SUPCSR).

Bits 14-10 - RESERVED, Read as 1/Write ignored
These bits are unassigned and read back as ones. All writes to these bits are ignored.

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Bit 9 - A/D Clock Enable (ADCLK), R/W
When set, this bit enables the overflow of the pacer clock to start the A/D conversion. When clear, this bit disables the pacer clock from causing conversions in the A/D section. This bit must be set in order to do A/D conversions.

This bit can be set and cleared under program control and is cleared at bus reset or board initialization.

Bit 8 - Multiplexer Busy (MUXBUSY), Read only
When set, this bit indicates that the multiplexer is still settling. A clock (either internal or external) pulse when MUXBUSY is set causes A/DERR (bit 15) to set. When clear, this bit indicates that the multiplexer in the module has settled and is ready to convert the analog value.

Bit 7 - A/D Done (A/DDONE), Read only
When set, this bit indicates that the A/D has completed a conversion and the data is now valid in the ADDAT Register. Reading the ADDAT Register automatically clears this bit. If another conversion completes before the A/D Data Register is read, two consecutive reads will be necessary to clear A/DDONE. In DMA mode, when this bit sets, a DMA transfer begins and the bit automatically clears once the data has been transferred.

This bit is cleared at bus reset, board initialization, by setting ADCINIT (bit 6 in the SUPCSR), or by reading the ADDAT Register.

Bit 6 - Interrupt on A/D Done (IA/DDONE), R/W
When this bit is set, the setting of A/DDONE (bit 7) generates an interrupt to the CPU upon completion of each conversion. When in the DMA mode, this bit allows DMAD (bit 15 of the SUPCSR) to cause an interrupt.

This bit can be set and cleared under program control and is cleared at bus reset or board initialization.

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Bits 5-4 - Gain Select (GS), R/W
These bits provide the programmable gain code for the RAM channel-gain list entry. Since the DT2827 and DT2828 do not have programmable gain, these bits are ignored on these boards. LLE (bit 15 of the CHANCSR) must be set in order to write to these bits. They can be read at anytime. When read, these bits reflect the gain of the channel settling not the gain of the channel being converted. See Chapter 6 for a discussion of the overlap mode.

The gain selected is determined as follows:

GAIN SELECTED	GS1 BIT 5	GS0 BIT 4
1	0	0
2 or 10	0	1
4 or 100	1	0
8 or 500	1	1

These bits can be set or cleared under program control when LLE=1, and are cleared at bus reset or board initialization.

Bits 3-0 - Channel Select (CHAN), R/W
These bits specify the next channel address to be written to the RAM channel-gain list. LLE (bit 15 of the CHANCSR) must be set in order to write to these bits. They can be read at any time. When read, these bits reflect the channel settling, not the channel being converted. See Chapter 6 for a discussion of the overlap mode.

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The channel selected is determined as follows:

CHANNEL SELECTED	CHANNEL SELECT BIT 3	2	1	0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4[1]	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTE
1. The DT2823, DT2827, and DT2828 have only four channels (numbered 0, 1, 2, and 3). Channel Select bits 2 and 3 are ignored for the DT2827 and DT2828. Addressing channels above channel 3 (channels 4 through 15) results in repetition. Channel 0 is addressed for channel 4, channel 1 is addressed for channel 5, and so on.

These bits can be set and cleared under program control when LLE=1, and are random at power up, and are unchanged at bus reset or board initialization.

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5.3 CHANNEL-GAIN LIST CONTROL/STATUS REGISTER

The CHANCSR is a read/write register that controls and monitors most of the activity associated with the RAM channel-gain list. Excess writes to the RAM channel-gain list result in overwriting of the RAM channel-gain list. For example, if the CHANCSR specifies 4 entries and you do 6 writes to the RAM channel-gain list, the first and the second entries are overwritten by the fifth and sixth entries, respectively.

Figure 5-2 gives the bit assignments of the CHANCSR. Section 6.1.4 details the channel-gain list RAM.

NAME: Channel List Control/Status
MNEMONIC: CHANCSR
ADDRESS: Base address + 2
ACCESS: R/W

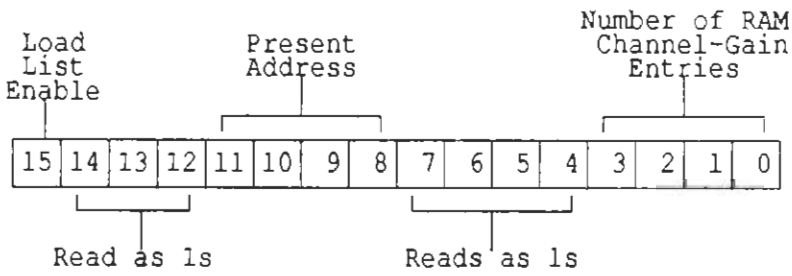


FIGURE 5-2: CHANCSR BIT ASSIGNMENTS

Bit 15 - Load List Enable (LLE), R/W
This bit must be set in order to load the RAM channel-gain list. When this bit is clear, writes to GS (bits 4 and 5 of the ADCSR) and CHAN (bits 0 to 3 of the ADCSR) are ignored.

This bit is cleared on bus reset or board initialization and can be set and cleared under program control.

Bits 14-12 - RESERVED, Read as 1/Write ignored
These bits are unassigned and read back as ones. All writes to these bits are ignored.

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Bits 11-8 - Present List Address (PRESLA), Read only
These bits specify the pointer into the RAM channel-gain list, not the contents of the list. When loading, these bits specify the address of the next entry.

These bits are cleared at bus reset or board initialization and when writing to the CHANCSR.

Bits 7-4 - RESERVED, Read as 1/Write ignored
These bits are unassigned and read back as ones. All writes to these bits are ignored.

Bits 3-0 - Number of RAM Entries (NUMB), R/W
These bits specify how many entries in the RAM channel-gain list are used for the scan. The RAM channel-gain list holds 16 entries, but you can specify from 1 to 16 channels for a scan.

The number of RAM channel-gain list entries is determined as follows:

NUMBER SELECTED	LAST RAM ADDRESS	NUMBER OF RAM ENTRIES BIT 3	BIT 2	BIT 1	BIT 0
1	0	0	0	0	0
2	1	0	0	0	1
3	2	0	0	1	0
4	3	0	0	1	1
5	4	0	1	0	0
6	5	0	1	0	1
7	6	0	1	1	0
8	7	0	1	1	1
9	8	1	0	0	0
10	9	1	0	0	1
11	10	1	0	1	0
12	11	1	0	1	1
13	12	1	1	0	0
14	13	1	1	0	1
15	14	1	1	1	0
16	15	1	1	1	1

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5.4 A/D DATA REGISTER

The ADDAT Register is a read-only register that contains the digital data from the A/D conversion. The bit assignment of the ADDAT Register is shown in Figure 5-3. The DT2823 and DT2827 use the full 16-bits in the register, while all other models (DT2821, DT2821-F-16SE, DT2821-F-8DI, DT2821-G-16SE, DT2821-G-8DI, DT2824-PGH, DT2824-PGL, DT2825 and DT2828) only use 12 bits in the register (bit 11 is the MSB). In binary (unipolar) and offset binary (bipolar) coding, bits 12 through 15 read back as zeros. In two's complement coding, bits 12 through 15 are tied to bit 11 to supply sign extension.

NAME: A/D Data
MNEMONIC: ADDAT
ADDRESS: Base address + 4
ACCESS: Read only

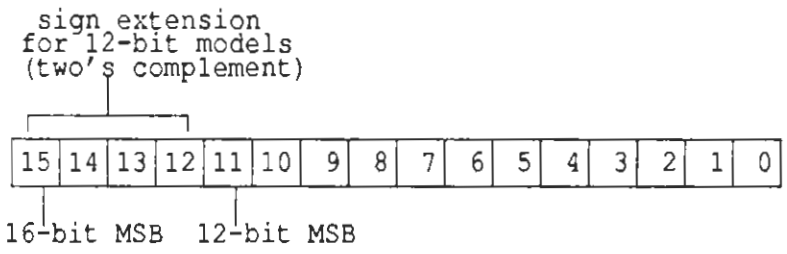


FIGURE 5-3: ADDAT REGISTER

Refer to the coding tables in Appendix D for examples of binary, offset binary, and two's complement data codes.

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5.5 D/A CONTROL/STATUS REGISTER

NOTE

This section does not apply to the DT2824-PGH and DT2824-PGL models.

The DACSR is a read/write register that interfaces to and controls the D/A and DIO sections of the DT2821 series board. The bit assignments are shown in Figure 5-4.

NAME: D/A Control/Status
MNEMONIC: DACSR
ADDRESS: Base address + 6
ACCESS: R/W

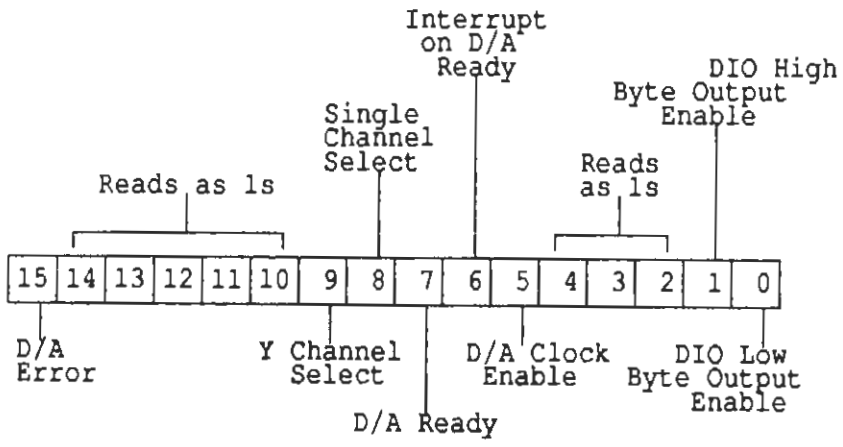


FIGURE 5-4: DACSR BIT ASSIGNMENTS

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Bit 15 - D/A Error (D/AERR), Read only
This bit indicates an error has occurred from one of the following causes:

- o Attempting any conversion while DACRDY (bit 7) is set. This is a clock error in programmed I/O mode.
- o Attempting any conversion before the DMA transfer is complete. This is a data late error in DMA mode.

This bit is cleared on bus reset or board initialization or by setting DACINIT (bit 5 in the SUPCSR).

Bits 14-10 - RESERVED, Read as 1/Write ignored
These bits are unassigned and read back as ones. All writes to these bits are ignored.

Bit 9 - Y Channel Select (YSEL), R/W
When SSEL (bit 8) is set, this bit chooses between the X channel (DAC 0), and the Y channel (DAC 1). When SSEL is clear, YSEL is ignored. By setting YSEL, the Y channel (DAC 1) receives the data. By clearing YSEL, the X channel (DAC 0) receives the data.

This bit can be set and cleared under program control and is cleared at bus reset or board initialization.

Bit 8 - Single Channel Select (SSEL), R/W
This bit determines whether the data alternates between both DACs or goes to one DAC. When cleared, this bit indicates dual-channel (X-Y) mode and YSEL (bit 9) is ignored. When set, SSEL indicates single-channel mode, and YSEL determines the DAC.

This bit can be set and cleared under program control and is cleared at bus reset or board initialization.

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Bit 7 - DAC Ready (DACRDY), Read only
When set, this bit indicates that the D/A has completed a conversion and new data can be entered into the DADAT Register. When clear, this bit indicates that the D/A can be clocked. The bit automatically clears when the DADAT Register is written to (once or twice depending upon the state of SSEL, bit 8), and the bit sets again following the D/A conversion caused by a clock (either internal or external). This bit operates similarly in DMA mode, in that when set, it causes a DMA request and is cleared as the DMA transfer of the word (or words) is completed.

This bit is set at bus reset, board initialization, or by setting DACINIT (bit 5 in the SUPSCR).

Bit 6 - Interrupt on D/A Ready (ID/ARDY), R/W
In non-DMA mode, when this bit is set, the setting of DACRDY (bit 7) generates an interrupt to the CPU. When in D/A clocked DMA mode, this bit enables the setting of DMAD (bit 15 of the SUPCSR) to generate an interrupt to the CPU. When in A/D clocked or A/D triggered scan DMA mode, DACRDY cannot interrupt the processor, and you must poll DACRDY (bit 7) to determine the state of the DAC.

This bit can be set and cleared under program control and is cleared at bus reset or board initialization.

Bit 5 - D/A Clock Enable (DACLK), R/W
When set, this bit enables the pacer clock to start a D/A conversion.

This bit can be set and cleared under program control and is cleared at bus reset or board initialization.

Bits 4-2 - RESERVED, Read as 1/Write ignored
These bits are unassigned and read back as ones. All writes to these bits are ignored.

Bit 1 - DIO High Byte Output Enable (HBOE), R/W
When set, this bit enables the high byte of the DIO port for digital output. When clear, the DIO high byte port lines are enabled for digital input--the external circuitry assumes control of them. The setting of this bit allows whatever is present in the DIODAT Register to be present on port 1.

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This bit can be set or cleared under program control and is cleared at bus reset or board initialization.

Bit 0 - DIO Low Byte Output Enable (LBOE), R/W
When set, this bit enables the low byte of the DIO port for digital output. When clear, the DIO low byte port lines are enabled for digital input--the external circuitry assumes control of them. The setting of this bit allows whatever is present in the DIODAT Register to be present on port 0.

This bit can be set or cleared under program control and is cleared at bus reset or board initialization.

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5.6 D/A DATA REGISTER

NOTE

This section does not apply to the DT2824-PGH and DT2824-PGL models.

The DADAT Register is a 12-bit, write-only register that receives the digital data that is to be converted by the D/A converter (or DAC). The bit assignments are shown in Figure 5-5.

NAME: D/A Data
MNEMONIC: DADAT
ADDRESS: Base address + 8
ACCESS: Write only

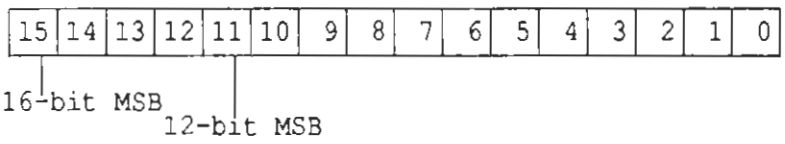


FIGURE 5-5: DADAT REGISTER

In dual-channel mode, the first data word goes to the X channel (DAC 0) and the second data word goes to the Y channel (DAC 1). Both are latched. Simultaneous conversions on DAC 0 and 1 occur on the first clock (either internal or external) after the second data word is written to the DADAT.

Refer to the coding tables in Appendix D for examples of binary or offset binary coding. The DACs on the DT2821 series do not recognize two's complement coding.

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5.7 DIO DATA REGISTER

The DIODAT Register is a read/write register that receives the digital data to be transferred to or from the DT2821 series board. The bit assignments are shown in Figure 5-6.

The state of LBOE and HBOE (DACSR bits 0 and 1) determines the direction of data flow in the DIO port. If the byte is set for digital inputs, writes to the corresponding byte in the DIODAT are ignored. Reads of the corresponding byte show the state of the port's input lines. Changes in the input line are reflected in the register immediately. If the byte is set for digital output, writes to the corresponding byte result in immediate changes to the digital outputs. Reads of the corresponding byte request the current state of the digital output lines.

When a port is enabled for output, the current contents of DIODAT is output to the corresponding port. It is recommended that you load the desired bit pattern into the DIODAT Register before enabling the port for output.

The contents of the DIODAT Register are random at power up and are unchanged at bus reset or board initialization.

NAME: DIO Data
MNEMONIC: DIODAT
ADDRESS: Base address + A
ACCESS: R/W

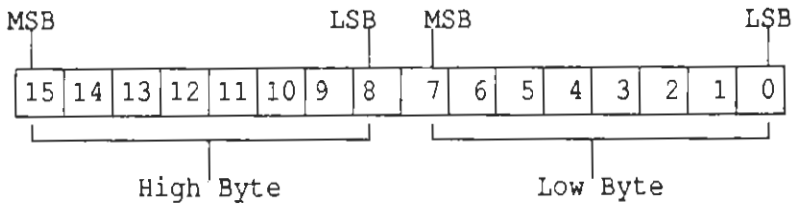


FIGURE 5-6: DIODAT REGISTER

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5.8 SUPERVISORY CONTROL/STATUS REGISTER

The SUPCSR is a read/write register that interfaces to and controls the supervisory sections of the board. These sections comprise the DMA Mode select, initialization bits, and clock source control. The bit assignments for the SUPCSR are shown in Figure 5-7.

NAME: Supervisory Control/Status
MNEMONIC: SUPCSR
ADDRESS: Base address + C
ACCESS: R/W

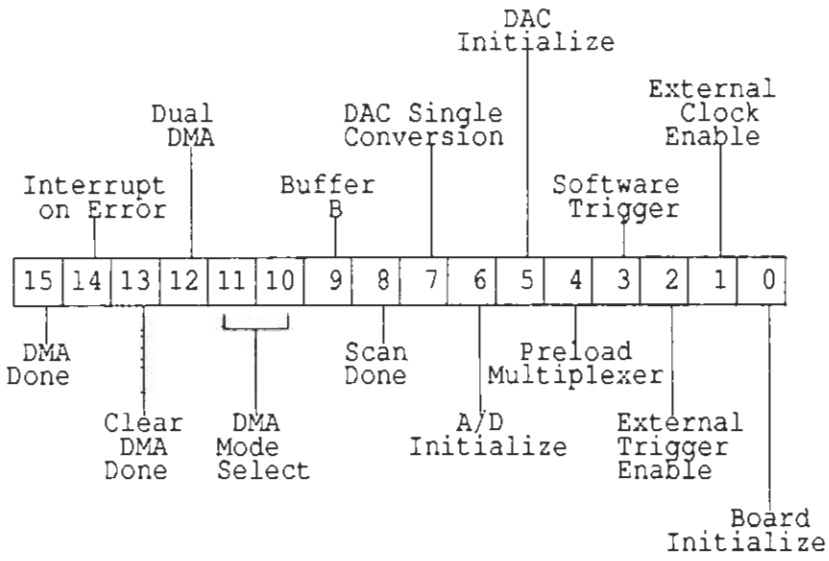


FIGURE 5-7: SUPCSR BIT ASSIGNMENTS

Bit 15 - DMA Done (DMAD), Read only
When set, this bit indicates that the DT2821 series board has completed the requested DMA transfer.

This bit can be cleared under program control (by setting CLRDMADNE--bit 13), and is cleared at bus reset or board initialization.

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Bit 14 - Interrupt on Error (ERRINTEN), R/W
When set, this bit enables the setting of either A/DERR (bit 15 of ADCSR) or D/AERR (bit 15 of DACSR) to generate an interrupt according to the following table. (See bits 10 and 11 for an explanation of the DMA modes.) When clear, no interrupt is generated on error.

DMA MODE	ERROR BIT ENABLED FOR INTERRUPT
0	A/DERR or D/AERR
1	A/DERR
2	D/AERR
3	A/DERR

This bit can be set and cleared under program control and is cleared at bus reset or board initialization.

Bit 13 - Clear DMA Done (CLRDMADNE), Read as 0/W
Writing a 1 to this bit clears DMAD (bit 15). Writing a 0 is ignored.

This bit can be set under program control and always reads as a 0.

Bit 12 - Dual DMA (DDMA), R/W
When set, this bit selects Continuous Performance DMA operation. In this mode, two DMA channels are used to transfer data continuously to (or from) memory. Setting this bit changes two distinct aspects of the DMA control used with the DT2821 series board. First, the DMA transfer does not terminate when DMA Terminal Count (T/C) is detected on bus finger B27. Second, the DMA alternates between two separate channels (switching occurs on T/C). The first DMA channel (jumper-selected) is always the one selected first in this alternating scheme. When this bit is clear, the first DMA channel (jumper-selected) is the default channel. This bit should only be set if you have jumper-selected two DMA channels.

This bit can be set and cleared under program control and is cleared at initialization.

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Bits 11-10 - DMA Select (DS), R/W
These bits define the DMA activity for the DT2821 series board as specified in the following chart. The different DMA modes are described in Chapter 6.

BIT 11 DS1	BIT 10 DS0	DMA MODE
0	0	No DMA (PIO)
0	1	A/D clocked DMA
1	0	D/A clocked DMA
1	1	A/D triggered scan DMA

These bits can be set and cleared under program control and are cleared at initialization.

Bit 9 - Buffer B (BUFFB), Read only with enabled clear
In Dual-DMA mode (bit 12 is set), this bit indicates which DMA buffer is being used. When set, this bit indicates that the present DMA buffer is buffer 2 (buffer B). When clear, this bit indicates that the present DMA buffer is buffer 1 (buffer A). Writing this bit to a 1 initializes DMA and clears this bit. Writing a 0 to this bit is ignored. If this bit is set, and you write a zero, this bit stays set. You must write BUFFB to a 1 (to clear it) before doing any DMA transfers. Single-buffer DMA must use buffer 1 (buffer A). Dual-DMA must start with buffer 1 (buffer A).

This bit is random at power up and is only cleared by its enabled clear (writing a 1 to this bit).

Bit 8 - Scan Done (SCDN), Read only
When set, this bit indicates that an A/D scan has completed and, if the DMA DONE bit is not set, that another scan can now be triggered. When clear after a trigger, this bit indicates that the A/D has not finished the scan. Before the first trigger, this bit can be ignored. Clock pulses are automatically disabled when this bit sets in DMA modes 0 and 3. In modes 1 and 2 this bit is not used. In DMA mode 3, another trigger starts another scan. A trigger when this bit is clear (after the first trigger) causes A/DERR (bit 15 of the ADCSR) to set.

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This bit is random on power up, and is unaffected by bus reset or board initialization.

Bit 7 - DAC Single Conversion (DACON), Read as 0/W
Writing a 1 to this bit causes a single D/A conversion. This bit can be used to cause D/A conversions in programmed I/O mode while the A/D is being used in DMA mode. This bit should only be set when DACRDY (bit 7 of DACSR) is clear. Writing a 0 to this bit is ignored.

This bit is cleared at initialization. This bit always reads as a 0.

Bit 6 - A/D Initialize (ADCINIT), Read as 0/W
Writing a 1 to this bit clears A/DERR (bit 15 of the ADCSR) and initializes the A/D data buffer circuitry. Writing a 0 to this bit is ignored. This bit should be set before A/D conversions are started.

This bit can be set under program control and always reads as a 0.

Bit 5 - D/A Initialize (DACINIT), Read as 0/W
Writing a 1 to this bit clears D/AERR (bit 15 of the DACSR) and initializes the DAC data buffers. Writing a 0 to this bit is ignored. This bit should be set before DAC conversions are started. Setting this bit does not change the output of the DACs.

This bit can be set under program control and always reads as a 0.

Bit 4 - Preload Multiplexer (PRLD), Read as 0/W
Writing a 1 to this bit preloads the first A/D channel (from the RAM channel-gain list) into the multiplexer. Writing a 0 to this bit is ignored. If the multiplexer is not preloaded, the first conversion is done on whatever channel is "left over" in the multiplexer. If you do not preload the multiplexer, the first conversion should be disregarded.

This bit is set under program control and always reads as a 0.

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Bit 3 - Software Trigger (STRIG), Read as 0/W
Writing a 1 to this bit starts the pacer clock circuit. Writing a 0 to this bit is ignored. STRIG is a program controlled trigger and can be used to enable the internal or external clock (depending on XCLK--bit 1).

DO NOT SET STRIG (BIT 3) AND XTRIG (BIT 2) AT THE SAME TIME.

This bit can be set under program control and always reads as a 0.

Bit 2 - External Trigger Enable (XTRIG), R/W
When set, this bit allows the external trigger signal on pin 49 of J1 to set up and enable the input to the pacer clock circuits. The external trigger does not start an A/D or D/A conversion. It signals the DT2821 series board that an event has happened and the board can begin conversions by either an external or internal clock (depending on XCLK).

DO NOT SET XTRIG (BIT 2) AND STRIG (BIT 3) AT THE SAME TIME.

This bit can be set and cleared under program control and is cleared at bus reset or board initialization.

Bit 1 - External Clock Enable (XCLK), R/W
When set, this bit enables the external clock signal on pin 50 of J1 as clock source for starting conversions. The external clock signal determines the clocking rate. When clear, the internal oscillator and pacer clock section determine the clocking rate.

This bit can be set or cleared under program control and is cleared at bus reset or board initialization.

Bit 0 - Board Initialization (BDINIT) Read as 0/W
Writing a 1 to this bit clears all the error flags, the control and status registers (ADCSR, DACSR, and SUPCSR), and the data buffers. Writing a 0 to this bit is ignored. BDINIT returns the DT2821 series board to the powered-up state. This bit does not effect the contents of DIODAT or DADAT.

This bit can be set under program control and always reads as a 0.

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5.9 PACER CLOCK REGISTER

The TMRCTR is a read/write register that contains the count that is loaded into the pacer clock circuit as well as the prescale count. When read, this register contains the current count and prescale of the divider. At overflow, the divider and prescale are reloaded with the original values. the bit assignments are shown in Figure 5-8.

Bits 11 through 8 form a 4-bit prescale that divides the 4MHz clock by a power of 2, from 0 to 15 (1 to 32,768). Bits 7 through 0 form the 8-bit count for the frequency set up by the prescaler bits. The frequency rate of A/D, D/A, or simultaneous A/D and D/A is a result of both the prescaler and counter bits. Chapter 6 has a detailed discussion of the pacer clock frequencies.

NAME: Pacer Clock
MNEMONIC: TMRCTR
ADDRESS: Base address + E
ACCESS: R/W

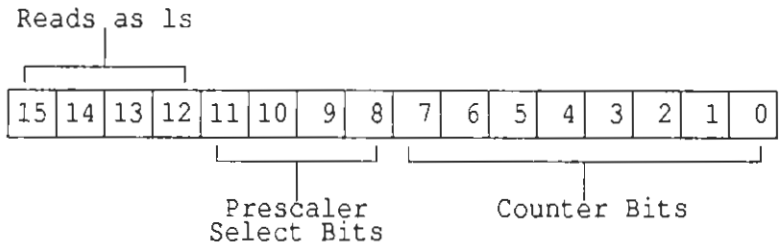


FIGURE 5-8: TMRCTR BIT ASSIGNMENTS

Bits 15-12 - RESERVED, Read as 1/Write ignored
These bits are not used and read back as ones.

Bits 11-8 - PRESCALER SELECT BITS (PRS3, PRS2, PRS1, PRS0), R/W
These bits select the value of the prescaler divider as shown in Table 5-2. The divided output of the prescaler clocks the pacer clock circuits.

These bits can be set and cleared under program control and are cleared at initialization.

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TABLE 5-2: TIMER COUNTER PRESCALE

PRESCALE BITS 11	10	9	8	PRESCALE DIVISION	RESULTING FREQUENCY (Hz)
0	0	0	0	1	4000000.
0	0	0	1	1	4000000.
0	0	1	0	4	1000000.
0	0	1	1	8	500000.
0	1	0	0	16	250000.
0	1	0	1	32	125000.
0	1	1	0	64	62500.
0	1	1	1	128	31250.
1	0	0	0	256	15625.
1	0	0	1	512	7812.5
1	0	1	0	1024	3906.25
1	0	1	1	2048	1953.125
1	1	0	0	4096	976.5625
1	1	0	1	8192	488.2813
1	1	1	0	16384	244.1406
1	1	1	1	32768	122.0703

The first two values of the prescale bits select the same frequency, as shown in the table.

The resulting frequency can be further divided by the counter bits (Bits 0 through 7).

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Bits 7-0 - COUNTER BITS, R/W
These bits are the divide by count loaded into the pacer clock. This value is the one's complement of the desired data value. When read, these bits provide the current count of the pacer clock.

These bits can be set and cleared under program control, are random at power up, and are unchanged at bus reset or board initialization.

TABLE 5-3: TMRCTR COUNTER BITS

DIVIDER (DECIMAL)	COUNTER BITS (ONE'S COMPLEMENT) HEX	DECIMAL
255	0	0
254	1	1
128	7F	127
127	80	128
126	81	129
1	FE	254
0	FF	255

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CHAPTER 6
PRINCIPLES OF OPERATION

A/D CONVERSION

D/A CONVERSION

DIGITAL I/O

TRIGGERS

CLOCKS

DMA MODES

PROGRAMMING THE DMA CONTROLLER

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6.1 A/D CONVERSION

An analog-to-digital (A/D) converter changes an analog voltage (like the output of a thermocouple, a pressure sensor, or an oscillator) into a digital code of 0's and 1's which is intelligible to a computer.

6.1.1 OVERLAP MODE A/D OPERATION

In the DT2821 series (except the DT2828--Simultaneous Sample and Hold) A/D system, A/D conversion happens as follows (refer to the block diagram of the A/D converter in Figure 6-1 and the timing diagram in Figure 6-2):

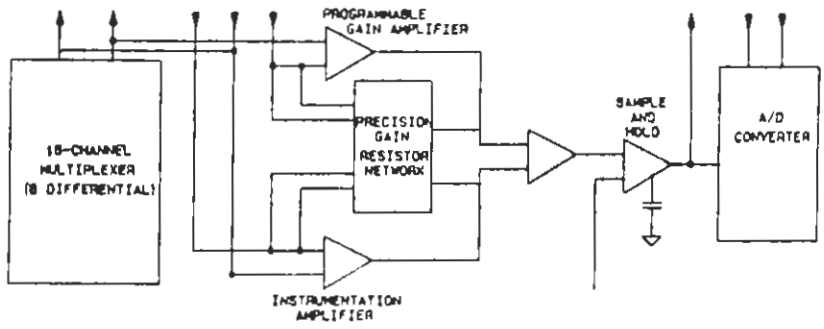


FIGURE 6-1: BLOCK DIAGRAM--A/D CONVERTER

1. The analog multiplexer chooses one input channel from those connected to the board. These channel addresses are preloaded into the RAM channel-gain list and the first channel is applied to the multiplexer's address lines when PRLD (bit 4 of the SUPCSR) is set. MUXBUSY (bit 8 of the ADCSR) automatically sets to signal that the multiplexer is settling.

2. The Programmable Gain Amplifier buffers the analog input, and may increase its voltage level based on the associated gain bits. Since the analog input signal from the transducer may be only +1.25V maximum on the DT2821, DT2821-F-16SE, DT2821-F-8DI,

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DT2821-G-16SE, or DT2821-G-8DI, an amplifier is used to boost the signal's voltage (by specifying a gain of 8) to the 0 to +10 volt (unipolar) or ±10 volt (bipolar) level required by the board's A/D converter. For the DT2827, the amplifier serves as a unity gain buffer. The voltage is not increased.

3. A sample and hold circuit samples the selected analog signal from the multiplexer. MUXBUSY (bit 8 of the ADCSR) clears to signal that the multiplexer has settled. A trigger (either internal or external) now marks the beginning of the scan.

4. On the first clock pulse (either internal or external) after the trigger, the sample and hold circuit switches to hold and the A/D converter translates the analog signal held by the sample and hold into a digital code. The next channel from the RAM channel-gain list is loaded into the multiplexer and MUXBUSY sets.

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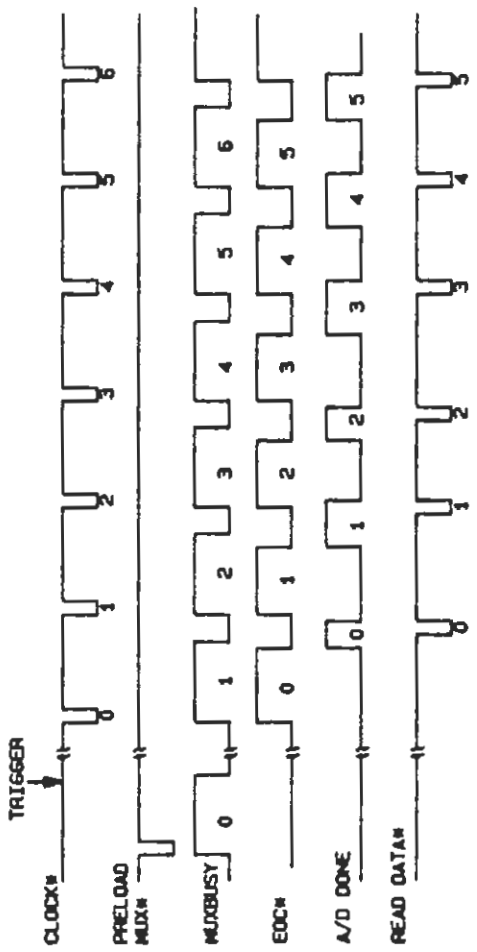


FIGURE 6-2: OVERLAP MODE TIMING DIAGRAM

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6.1.2 SIMULTANEOUS SAMPLE AND HOLD OPERATION

Simultaneous sample and hold converters are used in applications which require the analog input signals on multiple channels to be measured at the same time. The DT2828 accomplishes this by dedicating a separate sample and hold circuit to each input channel. These sample and hold circuits are simultaneously switched into hold mode by the first clock pulse after the trigger (either internal or external). The values captured by each channel's sample and hold circuit remain constant while the A/D channels are converted (one conversion per clock pulse). The DT2828 uses a single A/D converter to process the analog signals sequentially. The resulting digital codes represent the voltage present on the channels at the same instant.

Simultaneous sample and hold A/D conversion happens as described below. (Refer to the block diagram of the SS&H A/D converter in Figure 6-3 and the timing diagram in Figure 6-4.)

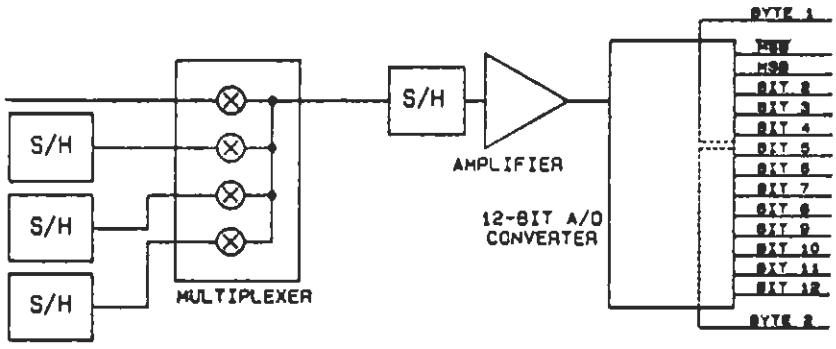


FIGURE 6-3: BLOCK DIAGRAM--SS&H A/D CONVERTER

1. PRLD (bit 4 of the SUPCSR) selects channel 0 on the multiplexer and puts all the sample and hold circuits in sample. Muxbusy (bit 8 of the ADCSR) automatically sets to signal that the multiplexer is setting on Channel 0.

2. The sample and hold circuits are now tracking the input analog signals. A clock pulse (either internal or external)

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triggers the circuitry into "hold" mode, and Channel 0 is converted while channel 1 is settling through the multiplexer.

3. The other three sample and hold circuits have acquired the analog signals, and are storing it on capacitors, awaiting subsequent clock pulses which convert the held values.

4. The Amplifier buffers the analog input. No gain is available on the DT2828.

5. Subsequent clock pulses cause remaining channels in the scan to be converted. When the final channel is converted and the input multiplexer returns to channel 0, all sample and hold circuits once again go into sample mode. This sequence repeats from step 2.

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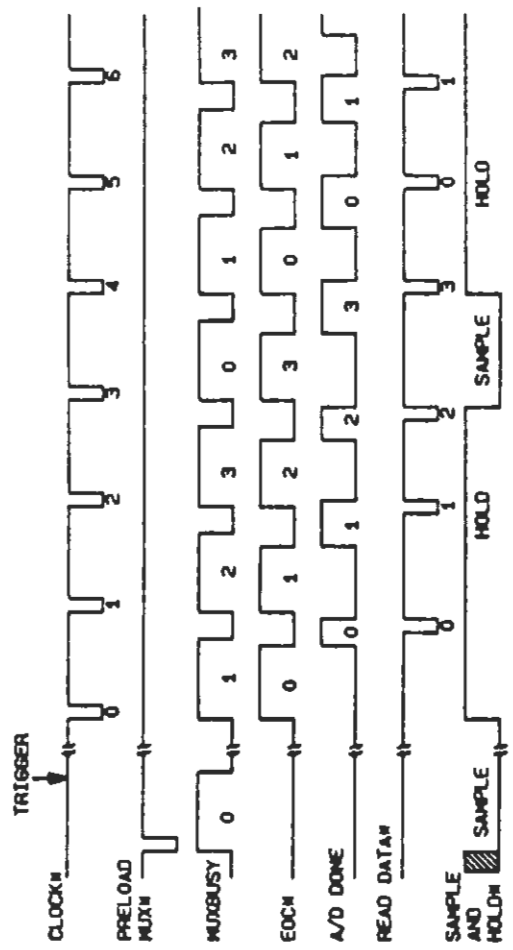


FIGURE 6-4: SS&H TIMING DIAGRAM

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6.1.3 RESOLUTION

The A/D system of the DT2821 series boards has 12 or 16 bits of resolution. Models DT2821, DT2821-F-16SE, DT2821-F-8DI, DT2821-G-16SE, DT2821-G-8DI, DT2824-PGH, DT2824-PGL, DT2825 and DT2828 use a 12-bit A/D converter; models DT2823 and DT2827 use a 16-bit converter.

In all DT2821 series boards, the incoming analog signal is converted into a binary number. With the DT2821, DT2821-F-16SE, DT2821-F-8DI, DT2821-G-16SE, DT2821-G-8DI, DT2824-PGH, DT2824-PGL, DT2825, or DT2828, the binary number is 12 bits long, and can assume 4096 different states (4096 equals 2 to the 12th). A 12-bit converter can therefore resolve differences on an analog input as small as 0.024% (0.024% equals 100 times 1/4096) of the selected analog input range. The 16-bit converters on the DT2823 and DT2827 models can assume 65,536 different states (65,536 is 2 to the 16th), and can resolve differences as small as 0.0015% (or 15.26 ppm) of the selected analog input range.

6.1.4 RAM CHANNEL-GAIN LIST

The DT2821 series boards have a 16-entry RAM channel-gain list that holds channel numbers and their associated gain in any order you want to sample them. Bits 0 through 5 of the ADCSR contain the channel (bits 0 to 3) and gain (bits 4 and 5) for the RAM channel-gain list entry. LLE (bit 15 of the CHANCSR) must be set before you can load the list.

Load NUMB (bits 0 to 3 of the CHANCSR) with the number of entries you want to load into the RAM channel-gain list (see Section 5.3). Then write to the ADCSR GS (bits 4 and 5) and CHAN (bits 0 to 3) for each entry. These writes are loading the list sequentially--the first write to the ADCSR (after LLE is set) loads the first channel and gain to be done, the second write to the ADCSR loads the second channel and gain. Section 7.2.3 (except for DT2828) or 7.2.7 (DT2828) has a step-by-step discussion of programming for an A/D triggered scan. The RAM channel-gain list overwrites any excess writes to the ADCSR. For example, if NUMB equals four and you write the ADCSR (when LLE=1) six times (with values 0, 1, 2, 3, 4, and 5) the RAM channel-gain list overwrites the first and second entries with the fifth and sixth writes (so the RAM channel-gain list

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ends up with 4, 5, 2, and 3 as the entries).

Once all the entries are loaded, clear LLE (bit 15 of the CHANCSR). Set PRLD (bit 4 of the SUPCSR). Wait for MUXBUSY to clear. While waiting, write to the ADCSR to enable interrupt on done or enable A/D clock (or both) if necessary. After MUXBUSY clears, send a trigger (either internal or external). SCDN (bit 8 of the SUPCSR) automatically clears on the first clock to indicate a scan is in progress. Conversions occur on each clock after the trigger. Do not retrigger until SCDN (bit 8 of the SUPCSR) sets again.

6.1.5 UNIPOLAR AND BIPOLAR RANGES

Unipolar input ranges recognize positive voltages only. On the DT2821, DT2821-F-16SE, DT2821-F-8DI, DT2821-G-16SE, DT2821-G-8DI, DT2824-PGH, DT2824-PGL, and DT2825, a unipolar range should be used only with input signals ranging from 0 to +1.25V to 0 to +10V, depending on the programmable gain selected. On the DT2828 a unipolar range should be used only with input signals ranging from 0 to +10V (no programmable gain). The DT2823 and DT2827 models are not configurable for a unipolar range.

Bipolar input ranges accept voltages which can be positive or negative. On the DT2821, DT2821-F-16SE, and DT2821-F-8DI they should be used with input signals from ±1.25V to ±10V full scale, depending on the programmable gain selected. On the DT2827 and DT2828 they should be used only with input signals ranging from ±10V full scale (no programmable gain).

On DT2821 series boards with 12-bit converters (all boards except the DT2827), you can select unipolar or bipolar input ranges by changing jumpers on the board. The DT2827 has a non-selectable bipolar input range. The jumper configurations are given in Chapter 3.

IMPORTANT

After changing the jumper configuration to select a different analog input range, the A/D conversion subsystem should be recalibrated. See Appendix B for the calibration procedure.

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6.1.6 OUTPUT DATA CODING

On unipolar input ranges, all DT282I series boards provide straight binary output coding. On bipolar ranges, the DT2821, DT2821-F-16SE, DT2821-F-8DI, DT2821-G-16SE, DT2821-G-8DI, DT2824-PGH, DT2824-PGL, DT2825, and DT2828 can provide either offset binary or two's complement coding. The DT2823 and DT2827 provide only two's complement coding for a bipolar input. Refer to Appendix D for 12-bit unipolar coding tables as well as 12-bit and 16-bit bipolar coding tables.

6.1.7 PROGRAMMABLE GAIN AMPLIFIER

Software selectable gains permit the analog inputs on the DT2821 series board to accommodate a wide range of voltage levels.

Table 6-1 details the full scale input ranges which result when the DT2821, DT2821-F-16SE, DT2821-F-8DI, DT2821-G-16SE, DT2821-G-8DI, or DT2824-PGH's amplifier gain is set for 1, 2, 4, or 8 in unipolar or bipolar modes. The DT2827 and DT2828 do not have programmable gains.

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TABLE 6-1: INPUT RANGES WITH PROGRAMMABLE GAIN

GAIN	INPUT RANGE	ACTUAL + FULL SCALE INPUT[1]
	Unipolar	
1	0 to +10 V	+9.9976 V
2	0 to +5 V	+4.9988 V
4	0 to +2.5 V	+2.4994 V
8	0 to +1.25 V	+1.2497 V
	Bipolar	
1	±10 V	+9.9951 V
2	±5 V	+4.9976 V
4	±2.5 V	+2.4988 V
8	±1.25 V	+1.2494 V

NOTE
1. The Actual + Full Scale Input is the lowest voltage required to produce an output code from the A/D converter of all 1's (or a zero followed by all 1's for two's complement). Increasing the input voltage beyond the Actual + Full Scale Input does not result in a change to the digital code output from the board's A/D converter. The Actual +Full Scale Input corresponds to the +Full Scale Voltage minus 1 LSB (Least Significant Bit).

6.2 D/A CONVERSION

NOTE

This section does not apply to DT2824-PGH and DT2824-PGL models.

A digital-to-analog (D/A) converter changes a digital code of 0's and 1's (as might come from a host computer) into a continuously-varying analog signal (as might be required to drive an audio amplifier, a chart recorder, or process actuators).

The DT2821 series board's D/A system contains

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two 12-bit D/A converters (DAC 0 and DAC 1) which may be operated in any of three modes, as determined by SSEL (bit 8 of the DACSR) and YSEL (bit 9 of the DACSR). SSEL specifies single- or dual-channel mode, and YSEL specifies the channel (when in single-channel mode). When SSEL is high, and YSEL is high, the Y Channel (DAC 1) receives the data. If SSEL is high, and YSEL is clear, the X channel (DAC 0) receives the data. If SSEL is clear, YSEL is ignored and the data alternates between the two DACs, with DAC 0 receiving the first data point, but conversion does not occur until the first clock pulse after the second data word (for DAC 1) is written.

The DACs on the DT2821 series boards provide constant output after the first data point is written to them. Subsequent writes to the DACs simply change the output voltage.

FOR EXAMPLE

> Data is written to DAC 0 which results in a +1V output. This +1V signal remains on the output of DAC 0 until new data is written to change it, or until the system is powered down.

The output of both DACs are random at power up and are unaffected by BINIT (bit 0 of the SUPCSR).

6.2.1 D/A RANGE SELECTION

The various output ranges for DAC 0 and DAC 1 are jumper-selected on the DT2821 series board. Since the output range for each DAC is selected separately, different output ranges can be selected at the same time on DAC 0 and DAC 1.

Unipolar output ranges provide positive voltages only. They should be selected where the output signal range is 0 to +5V or 0 to +10V.

Bipolar output ranges provide voltages which can be positive or negative. They should be selected where the output signal range is ±2.5V, ±5V, or ±10V.

When unipolar outputs are selected, the data written to the DT2821 series board should be in straight binary code. When bipolar outputs are selected, the data should be in offset binary code.

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Appendix D contains unipolar and bipolar coding D/A tables. The 16-bit DACs on the DT2823 accept digital code in two's complement only and provide bipolar outputs.

NOTE

Whenever the output range for either DAC is changed, that DAC should be recalibrated. Appendix B contains the D/A calibration procedure.

6.3 DIGITAL I/O

The Digital Input/Output (also called Digital I/O or DIO) subsystem of the DT2821 series board permits the IBM Personal Computer AT to be used with peripherals which accept or supply parallel digital data. Parallel data requires a separate electrical connection for each bit.

On the DT2821 series board, a total of 16 Digital I/O lines are provided. The 16 lines are divided into two ports of 8 lines each. Either port (or both ports together) can be used for writing data out of the DT2821 series board (digital output) or reading data into the DT2821 series board (digital input). All connections for the 16 Digital I/O lines are made on connector J1 or on the optional DT707 or DT752 Screw Terminal Panel.

Both ports are enabled for input after initialization or on power up. In order to output to one or both ports, you must set the enable bits (bits 0 and 1) of the DACSR. When set, the corresponding byte of the DIODAT Register is written to the Digital I/O lines. You should write the required bit pattern into the DIODAT Register before enabling the port for output. Whatever bit pattern is in the DIODAT Register when the port is enabled for output is sent to the DIO port.

FOR EXAMPLE

If LBOE (bit 0 of the DACSR) is high, and HBOE (bit 1 of the DACSR) is low, the data in the low byte of the DIODAT is output on the DIO lines (port 0). The high byte is masked out, and no data is written to port 1.

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6.4 TRIGGERS

A/D and D/A conversions are started by a trigger. There are two types of triggers: an external, user-supplied trigger; or an internal, software trigger (bit 3 of the SUPCSR).

Actual conversion of the analog data does not begin until the first clock after the trigger.

6.4.1 EXTERNAL TRIGGER

You may wish to synchronize the triggered scan with some outside event. You therefore must be able to specify the exact time at which to set up for conversions. To specify an external trigger, set ETRIG (bit 2 of the SUPCSR).

6.4.2 INTERNAL TRIGGER

With the software trigger the exact time at which an sequence begins (for example, the moment a triggered scan begins) is difficult to control. Since the trigger is created in software, anything which affects the IBM Personal Computer AT's bus activity affects the exact moment at which the software trigger is issued.

6.5 CLOCKS

On a DT2821 series board, a clock is an electronic frequency source which is used to initiate repetitive data conversions. You must enable the clock input to the A/D and D/A sections of the board separately. Either of two clock sources can be used on the DT2821 series board. Set XCLK (bit 1 of the SUPCSR) to enable the external clock signal (from pin 50 of J1). When XCLK is clear, the internal oscillator, TMRCTR, and pacer clock section determine the clocking rate. You need to enable the clock for the A/D (set ADCLK--bit 9 of the ADCSR) or the D/A (set DACLK--bit 5 of the DACSR) separately.

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6.5.1 EXTERNAL CLOCK

You may wish to synchronize the conversions with some outside event. You therefore must be able to specify the exact time at which to perform the conversions. To specify an external clock, set XCLK (bit 1 of the SUPCSR).

6.5.2 INTERNAL CLOCK

By writing to the TMRCTR, you can load the divider circuit as well as a prescale count for the pacer clock.

The total frequency range is from 4MHz to 0.476837Hz. This works out to a range of periods from 0.00000025 seconds (250 nanoseconds) to 2.097 seconds. The usable frequency range is from 129.032kHz to 0.476837Hz (7.75 microseconds to 2.097 seconds). Table 6-2 shows some frequencies available from the internal oscillator, TMRCTR, and pacer clock circuitry. These are not all the available frequencies, nor does the table show all the possible combinations to get a wanted frequency. For example, to get the pacer clock to output at 55.556kHz (last two entries on the next page), you can have a prescale of 0 and a counter of B8 (hex) or a prescale of 2 and a counter of A (hex).

Use the following formula to deduce the counter variable and use its neighboring prescaler. See Table 6-2 for the prescaler values.

The Equation for the DT2821 Pacer Clock

X = 255 - ((4,000,000 / 2^N) / F)

X = Counter Value (Bits 7-0 of Pacer Clock Register)
N = Prescale Divisor (Bits 11-8 of Pacer Clock Register)
F = Desired Sampling Frequency in Hertz

Example 1

If the "Desired Sampling Frequency" in Hertz is 50,000 or 50 kHz then:

Assumptions: Let N=0 for first iteration

X = 255 - ((4,000,000 / 2^0) / 50,000)

X = 255 - ((4,000,000 / 1) / 50,000)

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Solving inner parens

X = 255 - (4,000,000 / 50,000)

X = 255 - 80

X = 175

X = AF in hex

The value written to the Pacer Clock Register for a 50 kHz sampling rate is:

00AF hex

Example 2

If the "Desired Sampling Frequency" in Hertz is 1,500 or 1.5 kHz then:

Assumptions: Let N=0 for first iteration

X = 255 - ((4,000,000 / 2^0) / 1,500)

X = 255 - ((4,000,000 / 1) / 1,500)

Solving inner parens

X = 255 - (4,000,000 / 1,500)

X = 255 - 2666.7 Since 2666.7 is greater than 255 the prescale value must be increased. The next value that would change the prescaled frequency is to let N=2. This would also yield a value too great to be loaded into the counter part of the Pacer Clock Register. Let N=4.

X = 255 - ((4,000,000 / 2^4) / 1,500)

X = 255 - ((4,000,000 / 16) / 1,500)

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Solving inner parens

X = 255 - (250,000 / 1,500)

X = 255 - 166.7 Since 166.7 is not an integer it must be rounded to the nearest for the closest frequency available so I will round up to 167

X = 255 - 167

X = 88

X = 58 in hex

The value written to the Pacer Clock Register for a 1.5 kHz sampling rate is:

0458 hex

The sampling rate is:

F = ((4,000,000 / 2^N) / 255 - X)

F = ((4,000,000 / 2^4) / 255 - 88)

F = ((4,000,000 / 16) / 167)

F = (250,000 / 167)

F = 1,497.006 Hertz or 1.497 kHz

Hints

Remember the Prescaler is 2^0 = 1 and 2^1 = 1.
Remember the Pacer Clock Register is a 16 bit register.
Remember not ALL frequencies can be exactly obtained thus the round to nearest.

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TABLE 6-2: EXAMPLE PACER CLOCK FREQUENCIES

FREQUENCY (Hz)	TMRCTR PRESCALE	TMRCTR COUNTER
800.000k	0	FA
250.000k	0	EE
153.846k	0	E5
133.333k	0	E3
100.000k	0	D7
50.000k	2	AF
44.444k	0	A5
10.000k	4	E6
1.000k	4	05
.781k	8	EB

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6.6 DMA MODES

There are four DMA modes; Dual-DMA, A/D triggered scan, A/D clocked, and D/A clocked. Dual-DMA mode uses two DMA channels to provide Continuous Performance to (or from) memory. A/D triggered scan provides a means of starting a scan of channels on a software or external trigger. A/D clocked and D/A clocked DMA provide one conversion for each clock pulse received. The DMA mode is specified by DS (bits 10 and 11 of the SUPCSR).

TABLE 6-3: DMA MODES

DS1 BIT 11	DS0 BIT 10	DMA MODE
0	0	No DMA
0	1	A/D clocked DMA
1	0	D/A clocked DMA[1]
1	1	A/D triggered scan DMA

NOTE
1. This information does not apply to the DT2824-PGH and DT2824-PGL models.

6.6.1 DUAL-DMA MODE

By setting DDMA (bit 12 of the SUPCSR), you are selecting Dual-DMA mode for Continuous Performance to (or from) memory. The first DMA channel operates normally. The signal TERMINAL COUNT on bus finger B27 does not stop DMA transfers, but tries to start the other channel. In order to continue DMA transfers, you must have set up the other DMA channel with the required number of transfers, the DMA memory page, and the DMA base address. To stop DMA transfers, you should reset DDMA (bit 12 in the SUPCSR). The next TERMINAL COUNT stops DMA in the same manner as normal (single channel) DMA.

Both DMA controllers can be set up before starting the DMA transfers. The interrupt handling routine should reinitialize the DMA controller. Check BUFFB (bit 9 of the SUPCSR) to determine which buffer is currently being used. Refer to Chapter 7 for details on programming sequences. Dual-DMA is discussed where applicable.

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6.6.2 A/D TRIGGERED SCAN DMA

By setting bits 10 and 11 of the SUPCSR, you are selecting the A/D triggered scan DMA mode. The DT2821 series performs one A/D conversion on each clock pulse until the last element in the RAM channel-gain list is reached. The clock is automatically disabled, and the multiplexer is preloaded with the channel specified by the first entry in the RAM channel-gain list. The DT2821 series board does one conversion for each clock pulse, but does not restart the scan (as defined by the RAM channel-gain list) until either STRIG (bit 3 of the SUPCSR) sets or an external trigger occurs (if ETRIG--bit 2 of the SUPCSR is set). TERMINAL COUNT (T/C) on the IBM Personal Computer AT bus stops DMA transfers if not in Dual-DMA mode. Refer to Section 7.2.3 (except for the DT2828) or Section 7.2.7 (for the DT2828) for a detailed programming sequence for A/D triggered scan.

6.6.3 A/D CLOCKED DMA

By clearing bit 11 and setting bit 10 of the SUPCSR, you are selecting the A/D clocked DMA mode. Each clock, either internal or external, produces one conversion. TERMINAL COUNT (T/C) on the IBM Personal Computer AT bus stops DMA transfers if not in Dual-DMA mode. Refer to Section 7.2.4 (except for the DT2828) or Section 7.2.8 (for the DT2828) for a detailed programming sequence for A/D clocked DMA.

6.6.4 D/A CLOCKED DMA

NOTE

This section does not apply to the DT2824-PGH and DT2824-PGL models.

By setting bit 11 and clearing bit 10 of the SUPCSR, you are selecting the D/A clocked DMA mode. Each clock, either internal or external, produces one conversion (two conversions in X-Y mode). TERMINAL COUNT (T/C) on the IBM Personal Computer AT bus stops DMA transfers if not in Dual-DMA mode. Refer to Section 7.3.2 for a detailed programming sequence for D/A clocked DMA.

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6.7 PROGRAMMING THE DMA CONTROLLER

In order to program the IBM Personal Computer AT's DMA controller, you must supply the following information. If you are using Dual-DMA mode, you must supply this information twice. To continue in Dual-DMA mode, the DMA channel not being used must be reprogrammed while the other channel is in use.

1. DMA Memory Page

   The IBM Personal Computer AT's DMA controller handles a maximum of 16 address lines. These lines can be used to access up to 64K words of random access memory (RAM). A DMA page is a block of 64K words of RAM. By specifying a DMA page, you determine which 64K word block of RAM the DMA controller can access. Page 0 is the first 64K word block of RAM. Page 124 is the last 64K word block of a 16Mbyte RAM.

2. DMA Base Address

   The DMA Base Address is the lowest memory address on the designated 64K word memory page which is read from on a DMA Read Transfer or written to on a DMA Write Transfer.

   Note that after a transfer to or from the base address is accomplished, subsequent transfers in a DMA operation access higher addresses. That is, the DMA memory addresses always increments rather than decrements.

3. DMA Word Count

   The DMA Word Count represents the total number of DMA word transfers to or from memory which take place in any particular DMA operation. A DMA Word Count of zero specifies a single word. Therefore, the DMA Word Count is always one fewer than the number of word transfers required.

4. DMA Mode

   The DMA Mode specifies several DMA transfer characteristics:

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- DMA Channel

  DMA Channel selects whether DMA channel 5, DMA channel 6, or DMA channel 7 is used. The DMA channel specified in DMA Mode must be the same as selected in jumpers for the DT2821 series board. Before specifying a DMA channel, make sure the DMA channel is available. Check the technical information on the peripherals in the IBM Personal Computer AT to make sure that none of the peripherals are using the DMA channel (or channels) being used by the DT2821.

- Read Transfer/Write Transfer

  DMA Mode also determines whether the DMA transfer is from memory and into the DT2821 series board (a Read Transfer), or from the DT2821 series board into memory (a Write Transfer).

- Autoinitialize

  DMA Mode can also set the DMA controller to operate in Autoinitialize mode. In Autoinitialize mode, when the number of words specified by the DMA Word Count is reached, TERMINAL COUNT is not asserted as usual, and the DMA controller resets itself to the DMA Base Address, and the DMA operation repeats. This is not Dual-DMA mode, but rather allows the same DMA channel to be used continuously. Your program must make sure new data does not overwrite old data.

5. DMA Mask

   Before a DMA channel can accept a system DMA request, it must be enabled by the appropriate setting of the DMA mask. This permits the DMA channel to perform the requested data transfer.

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6.7.1 DMA REGISTERS

Information is written to the DMA controller by programming the DMA registers. Table 6-4 contains a list of the DMA registers which are used in running the DT2821 series board in DMA mode. All the DMA registers are eight bits wide.

TABLE 6-4: DMA REGISTERS

ADDRESS (HEX)	DESCRIPTION
8B	DMA Page Select, channel 5
89	DMA Page Select, channel 6
8A	DMA Page Select, channel 7
0C4	Base Address, channel 5
0C6	Word Count, channel 5
0C8	Base Address, channel 6
0CA	Word Count, channel 6
0CC	Base Address, channel 7
0CE	Word Count, channel 7
0D4	Mask Register
0D6	Mode Register
0D8	Byte Pointer Flip/Flop

6.7.1.1 DMA Page Select, Channel 5 (8B, WRITE)

The DMA Page Select Register for DMA channel 5 is a write-only register located at address 8B (hex). It selects which 64K word memory page is used for DMA transfers. A value of 0 selects the first page, and 124 selects the last page of a 16Mbyte system.

6.7.1.2 DMA Page Select, Channel 6 (89, WRITE)

The DMA Page Select Register for DMA channel 6 is a write-only register located at address 89 (hex). It selects which 64K word memory page is used for DMA transfers. A value of 0 selects the first page, and 124 selects the last page of a 16Mbyte system.

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6.7.1.3 DMA Page Select, Channel 7 (8A, WRITE)

The DMA Page Select Register for DMA channel 7 is a write-only register located at address 8A (hex). It selects which 64K word memory page is used for DMA transfers. A value of 0 selects the first page, and 124 selects the last page of a 16Mbyte system.

6.7.1.4 Base Address, Channel 5 (0C4, R/W)

The Base Address Register for DMA channel 5 is located at address 0C4 (hex). It should be written with a 16-bit Base Address value. The Base Address Register for channel 5 is a read/write register. When read, it indicates the current memory address where the DMA controller is reading or writing data.

6.7.1.5 Word Count, Channel 5 (0C6, R/W)

The Word Count Register for DMA channel 5 is located at address 0C6 (hex). The Word Count Register for DMA channel 5 is a read/write register. When read, it indicates the present word transfer taking place in the DMA controller.

6.7.1.6 Base Address, Channel 6 (0C8, R/W)

The Base Address Register for DMA channel 6 is located at address 0C8 (hex). It should be written with a 16-bit Base Address value. The Base Address Register for channel 6 is a read/write register. When read, it indicates the current memory address where the DMA controller is reading or writing data.

6.7.1.7 Word Count, Channel 6 (0CA, R/W)

The Word Count Register for DMA channel 6 is located at address 0CA (hex). The Word Count Register for DMA channel 6 is a read/write register. When read, it indicates the present word transfer taking place in the DMA controller.

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6.7.1.8 Base Address, Channel 7 (0CC, R/W)

The Base Address Register for DMA channel 7 is located at address 0CC (hex). It should be written with a 16-bit Base Address value. The Base Address Register for channel 7 is a read/write register. When read, it indicates the current memory address where the DMA controller is reading or writing data.

6.7.1.9 Word Count, Channel 7 (0CE, R/W)

The Word Count Register for DMA channel 7 is located at address 0CE (hex). The Word Count Register for DMA channel 7 is a read/write register. When read, it indicates the present word transfer taking place in the DMA controller.

6.7.1.10 Mask (0D4, WRITE)

The Mask Register is located at address 0D4 (hex). It is used to enable the channel which is used for DMA transfers. A byte value of 1 (hex) enables channel 5. A byte value of 2 (hex) enables channel 6. A byte value of 3 (hex) enables channel 7.

6.7.1.11 Mode (0D6, WRITE)

The Mode Register is located at location 0D6 (hex), and is used to select the DMA channel number, to determine whether the DMA operation is a write to memory or a read from memory, and whether to autoinitialize or not.

Any of twelve values can be written to the Mode Register. These values are listed in Table 6-5.

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TABLE 6-5: MODE REGISTER VALUES

VALUE (HEX)	MEMORY FUNCTION	DMA CHANNEL	AUTOIN-ITIALIZE?
45	Write	5	No
49	Read	5	No
55	Write	5	Yes
59	Read	5	Yes
46	Write	6	No
4A	Read	6	No
56	Write	6	Yes
5A	Read	6	Yes
47	Write	7	No
4B	Read	7	No
57	Write	7	Yes
5B	Read	7	Yes

6.7.1.12 Byte Pointer Flip/Flop (0D8, WRITE)

Writing any data value to the Byte Pointer Flip/Flop Register (address 0D8, hex) causes the DMA controller's byte flip/flop to be reset, and indicates the next write to any 16-bit register is the first (low) byte of data. This register should be written before any programming of the DMA register commences. This register should be written to even if all the data to program the DMA controller is 16-bit transfers.

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CHAPTER 7
PROGRAMMING

INTRODUCTION

A/D SUBSYSTEM

D/A SUBSYSTEM

DIGITAL I/O SUBSYSTEM

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7.1 INTRODUCTION

This chapter discusses the steps that should be followed in programming the DT2821 series boards. All operating modes of the A/D subsystems, as well as the operations of the D/A and digital I/O subsystems are covered.

Throughout the discussions on programming, only register bits directly involved with the particular operating mode are listed. The remaining bits are either read-only, user-selectable, reserved, or irrelevant. Also, it is assumed that the DMA controller is properly programmed (see Section 6.7) before initiating any operation whenever DMA is used for data transfers.

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7.2 A/D SUBSYSTEM

Programming the A/D subsystem of the DT2821 series board consists of executing sequentially five major segments of instructions:

1. Initialization
2. Selection of the operating parameters
3. Selection of the input channels
4. Conversion of the analog input signals
5. Processing of converted digital data

A/D conversion operations are executed differently for models using conventional converters (all models except DT2828), and the DT2828, which features a simultaneous sample and hold circuit. Programming sequences for the DT2828 are discussed separately. The following topics are covered:

- Single-channel non-DMA (Except DT2828)
- Single-channel DMA (Except DT2828)
- A/D Triggered Scan DMA (Except DT2828)
- A/D Clocked DMA (Except DT2828)
- Single-channel non-DMA (DT2828, Ch 0)
- Single-channel Clocked DMA (DT2828, Ch 0)
- A/D Triggered Scan DMA (DT2828)
- A/D Clocked DMA (DT2828)

Dual-DMA mode is discussed as a sideline under the DMA sequences.

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7.2.1 SINGLE-CHANNEL NON-DMA (EXCEPT DT2828)

The single-channel non-DMA conversion operation performs one conversion on a selected channel and stops. Data transfers are done by programmed I/O, from the A/D Data Register to the system memory.

To convert an input signal in the single-channel non-DMA mode, proceed as follows:

1. Set the pacer clock to a rate no faster than the maximum speed of A/D subsystem. This is done by loading the TMRCTR with selected values for the Prescaler (bits 11-8) and Counter (bits 7-0). These bits determine the frequency of the pacer clock outputs (conversion triggers) based on an initial frequency of the internal oscillator.

2. Load the SUPCSR with the following bit pattern:

   - o Bit 13 = 1 - Clear DMA Done
   - o Bit 9 = 1 - Buffer B
   - o Bit 6 = 1 - A/D Initialize

   You have now:

   A. Cleared the DMA Done.
   B. Selected Buffer 1 (A) for DMA transfers.
   C. Initialized the A/D data buffer circuitry.

3. Load the CHANCSR with the following bit pattern:

   - o Bit 15 = 1 - Load List Enable
   - o Bits 3-0 = 0000 - Number of RAM Entries

   You have now:

   A. Enabled writes to the RAM channel-gain list.
   B. Specified a single-channel conversion.

   The channel number and the gain are written to the ADCSR but are placed into the RAM channel-gain list.

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4. Load the ADCSR with the following bit pattern:

   - o Bit 9 = 1 - A/D Clock Enable
   - o Bit 6 = 1 - Interrupt on A/D Done (optional)
   - o Bits 5-4 = 00 to 11 - Gain Select
   - o Bits 3-0 = 0000 to 1111 - Channel Select (the channel number)

   You have now:

   A. Enabled the pacer clock to issue trigger pulses to the A/D subsystem.
   B. Selected the input channel and the gain to be applied to the input signal.
   C. Set the board to issue an interrupt to the processor at the end of the A/D conversion (optional).

5. Write 0 to bit 15 (LLE) of the CHANCSR to preclude further writes to the RAM channel-gain list and to enable succeeding events.

6. Load the SUPCSR with the following bit pattern:

   - o Bit 14 = 1 - Interrupt on Error (optional)
   - o Bits 11-10 = 00 - DMA Select (PIO)
   - o Bit 9 = 0 - Buffer B
   - o Bit 6 = 0 - A/D Initialize
   - o Bit 4 = 1 - Preload Multiplexer
   - o Bit 3 = 0 - Software Trigger
   - o Bit 2 = 0 - External Trigger Enable
   - o Bit 1 = 0 - External Clock Enable
   - o Bit 0 = 0 - Board Initialization

   You have now:

   A. Selected the internal clock source for pacer clock outputs (bit 1 should be set for an external clock source).
   B. Selected programmed I/O (non-DMA) transfers.
   C. Set the board to issue an interrupt to the processor if an error occurs during the conversion.
   D. Preloaded the selected channel into the multiplexer channel latch.

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As soon as the SUPCSR is loaded, the A/D module sets MUXBUSY (ADCSR bit 8), indicating that the multiplexer is settling on the input from the selected channel.

7. Monitor MUXBUSY until clear, indicating that the multiplexer has settled on the selected channel, then load the SUPCSR with the following bit pattern:

    - o Bit 14 = 1 - Interrupt on Error (optional)
    - o Bits 11-10 = 00 DMA Select (PIO)
    - o Bit 9 = 0 - Buffer B
    - o Bit 6 = 0 - A/D Initialize
    - o Bit 4 = 0 - Preload Multiplexer
    - o Bit 3 = 1 - Software Trigger
    - o Bit 2 = 0 - External Trigger Enable
    - o Bit 1 = 0 - External Clock Enable
    - o Bit 0 = 0 - Board Initialization

    You have now:

    A. Software-actuated the pacer clock circuit on the board (if you select bit 3 to be clear and bit 2 to be set, trigger the pacer clock circuit externally).
    B. Selected the internal clock source to control the pacer clock pulse rates (bit 1 should be set for external clock source).

    The first clock pulse after the SUPCSR is loaded triggers the A/D conversion.

8. At the end of the A/D conversion, the module places the data in the A/D Data Register and sets A/DDONE (ADCSR bit 7). If Interrupt on A/D Done (ADCSR bit 6) is set, as in the current option, the board issues an interrupt to the processor. Otherwise the program must continually poll A/DDONE to set, to ascertain that the module has completed the conversion. When A/DDONE sets, it disables the pacer clock pulses. The board must be set up again for a new A/D conversion.

9. The processor, under program control, reads the converted data from the A/D Data Register. This clears the A/D Done bit in the ADCSR. The single-channel non-DMA conversion is complete.

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10. To start another single-channel non-DMA conversion on a different channel, proceed from step 2 above. To do repetitive overlap conversions on the same channel, proceed from step 6, after a trigger is issued on the current signal (when step 7 has been executed).

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7.2.2 SINGLE-CHANNEL DMA (EXCEPT DT2828)

The single-channel DMA performs up to 64K conversions on a selected channel with one trigger if a single DMA buffer is used. If you select Dual-DMA, you can define as many buffers as needed, each buffer containing up to 64K words. Conversions can be performed continuously until all user-defined buffers are full. Data transfers are done automatically by the DMA circuit from the A/D Data Register to the DMA buffer.

To convert input signals in the single-channel DMA mode, proceed as follows:

1. Load the TMRCTR with selected values for the Prescaler (bits 11-8) and Counter (bits 7-0). These bits determine the frequency of the pacer clock output (conversion pulses) based on an initial frequency of the internal oscillator.

2. Load the SUPCSR with the following bit pattern:

   - o Bit 13 = 1 - Clear DMA Done
   - o Bit 9 = 1 - Buffer B
   - o Bit 6 = 1 - A/D Initialize

   You have now:

   A. Cleared DMA Done.
   B. Selected DMA Buffer 1 (A) for DMA data transfers.
   C. Initialized the A/D data and DMA buffer circuit.

3. Load the CHANCSR with the following bit pattern:

   - o Bit 15 = 1 - Load List Enable
   - o Bits 3-0 = 0000 - Number of RAM entries

   You have now:

   A. Enabled writes to the RAM channel-gain list.
   B. Specified a list size of one channel.

   The channel number and the gain are written to the ADCSR but are placed into the RAM

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channel-gain list.

4. Load the ADCSR with the following bit pattern:

   - o Bit 9 = 1 - A/D Clock Enable
   - o Bit 6 = 1 - Interrupt on A/D Done
   - o Bits 5-4 = 00 to 11 - Gain Select
   - o Bits 3-0 = 0000 to 1111 - Channel Select (the channel number)

   You have now:

   A. Enabled the pacer clock to issue trigger pulses to the A/D subsystem.
   B. Selected the input channel and the gain to be applied to the input signal.
   C. Set the board to issue an interrupt to the processor at the end of the DMA buffer.

5. Write a 0 to bit 15 (LLE) of the CHANCSR to preclude further writes to the RAM channel-gain list and enable succeeding events.

6. Load the SUPCSR with the following bit pattern:

   - o Bit 14 = 1 - Interrupt on Error
   - o Bit 13 = 0 - Clear DMA Done
   - o Bit 12 = 0 - Dual-DMA
   - o Bits 11-10 = 01 - DMA Select
   - o Bit 9 = 0 - Buffer B
   - o Bit 6 = 0 - A/D Initialize
   - o Bit 4 = 1 - Preload Multiplexer
   - o Bit 3 = 0 - Software Trigger
   - o Bit 2 = 0 - External Trigger Enable
   - o Bit 1 = 0 - External Clock Enable
   - o Bit 0 = 0 - Board Initialization

   You have now:

   A. Selected the internal clock source for pacer clock outputs (bit 1 should be set for external clock source).
   B. Set the board to issue an interrupt to the processor if an error occurs during the conversion.
   C. Preloaded the selected channel into the multiplexer channel latch.

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As soon as the SUPCSR is loaded, the A/D module sets MUXBUSY (ADCSR bit 8), indicating that the multiplexer is settling on the input from the selected channel.

7. Monitor MUXBUSY (ADCSR bit 8) until clear, indicating that the multiplexer has settled on the selected channel, then load the SUPCSR with the following bit pattern:

   - Bit 14 = 1 - Interrupt on Error
   - Bit 13 = 0 - Clear DMA Done
   - Bit 12 = 0 - Dual-DMA
   - Bits 11-10 = 01 - DMA Select
   - Bit 9 = 0 - Buffer B
   - Bit 6 = 0 - A/D Initialize
   - Bit 4 = 0 - Preload Multiplexer
   - Bit 3 = 1 - Software Trigger
   - Bit 2 = 0 - External Trigger Enable
   - Bit 1 = 0 - External Clock Enable
   - Bit 0 = 0 - Board Initialization

   You have now:

   A. Software-actuated the pacer clock circuit on the board (if you select bit 3 to be clear and bit 2 to be set, trigger the pacer clock circuit externally).
   B. Selected the internal clock source for pacer clock outputs (bit 1 should be set for external clock source).

   The first pacer clock pulse after the SUPCSR is loaded starts A/D conversions.

8. At the end of the A/D conversion, the module places the data in the A/D Data Register and sets A/DDONE (ADCSR bit 7). The DMA circuit transfers the converted data from the A/D Data Register to the DMA buffer. This clears A/DDONE. A/D conversion of the signal on the selected channel is complete.

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9. For repetitive overlap conversions on the same channel, resume the procedure from step 6, after a trigger is issued on the current signal (when step 7 has been executed). To perform a single-channel DMA conversion on another channel, proceed from step 2. The single-channel DMA conversions complete when the user-defined DMA buffer is filled. At that point:

   A. DMA Done (SUPCSR bit 15) sets.
   B. DMA Done issues an interrupt to the processor.
   C. Triggers are disabled.

When the board is operated in the Dual-DMA mode, two DMA channels are used. In this mode, conversions do not halt at DMA Done, but data transfers switch from one DMA channel to the other. The memory segments used by each channel for DMA buffers are assigned by the DMA controller. To avoid buffer overwrites and consequent data loss, each time there is a switch of channels, a different segment of memory defined by the contents of the DMA page and offset registers for that channel is used for data transfers. However, if data is transferred from memory to disk concurrent with data acquisition, no loss of data occurs. The Dual-DMA scheme allows a continuous stream of operations until the programmed number of conversions are performed. The DMA circuit issues interrupts to the processor at each DMA Done. When the last buffer is filled, the DMA circuit sets DMA Done, issues an interrupt to the processor, and disables further triggers.

CAUTION

The speed of operations in the continuous performance mode is limited by the memory to disk transfer rate of the converted data because seek times on the disk are much longer than the A/D conversion times.

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The interrupt service routine should perform the following tasks in the Dual-DMA mode:

A. Clear DMA Done by setting Clear DMA Done (SUPCSR bit 13). This is done by writing the following bit pattern to the SUPCSR:

- o Bit 14 = 1 - Interrupt on Error
- o Bit 13 = 1 - Clear DMA Done
- o Bit 12 = 1 - Dual-DMA
- o Bits 11-10 = 01 - DMA Select
- o Bit 9 = 0 - Buffer B
- o Bit 6 = 0 - A/D Initialize
- o Bit 4 = 0 - Preload Multiplexer
- o Bit 3 = 0 - Software Trigger
- o Bit 2 = 0 - External Trigger Enable
- o Bit 1 = 0 - External Clock Enable
- o Bit 0 = 0 - Board Initialization

CAUTION

Inadvertently writing 1 to bit 9 immediately switches the operating DMA channel to Buffer A.

If the next buffer is the last one in the Dual-DMA transfers, the interrupt routine must perform a second write to the SUPCSR to clear the Dual-DMA bit as follows:

- o Bit 14 = 1 - Interrupt on Error
- o Bit 13 = 0 - Clear DMA Done
- o Bit 12 = 0 - Dual-DMA
- o Bits 11-10 = 01 - DMA Select
- o Bit 9 = 0 - Buffer B
- o Bit 6 = 0 - A/D Initialize
- o Bit 4 = 0 - Preload Multiplexer
- o Bit 3 = 0 - Software Trigger
- o Bit 2 = 0 - External Trigger Enable
- o Bit 1 = 0 - External Clock Enable
- o Bit 0 = 0 - Board Initialization

The next setting of DMA Done stops further conversions.

B. Check the A/D Error bit in the ADCSR.
C. Reprogram the DMA controller.
D. Exit the interrupt subroutine.

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7.2.3 A/D TRIGGERED SCAN DMA (EXCEPT DT2828)

Channel scan conversions can be performed when the board is used in the A/D triggered scan DMA mode. As discussed earlier in Chapter 5, the board performs conversions on a list of channels (up to 16) loaded in the RAM channel-gain list. Data transfers are done automatically by the DMA circuit, from the A/D Data Register to the DMA buffer. External triggers are normally used with this mode of operation.

To convert input signals in this mode, proceed as follows:

1. Load the TMRCTR with selected values for the Prescaler (bits 11-8) and Counter (bits 7-0). These bits determine the frequency of the pacer clock output (conversion pulses) based on an initial frequency of the internal oscillator.

2. Load the SUPCSR with the following bit pattern:

   - o Bit 13 = 1 - Clear DMA Done
   - o Bit 9 = 1 - Buffer B
   - o Bit 6 = 1 - A/D Initialize

   You have now:

   A. Cleared the DMA Done bit.
   B. Selected DMA Buffer 1 (A) for DMA data transfers.
   C. Initialized the A/D data and DMA buffer circuit.

3. Load the CHANCSR with the following bit pattern:

   - o Bit 15 = 1 - Load List Enable
   - o Bits 3-0 = 0000 to 1111 - No. of RAM entries

   You have now:

   A. Enabled writes to the RAM channel-gain list.
   B. Delimited the number of channels in the scan (1 channel for the value of 0, 16 channels for the value of 15).

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The channel numbers and gains are written to the ADCSR but they are placed into the RAM channel-gain list. Channel numbers and gains can be loaded in any order, consecutive or random, and multiple entries can be done on any channel. The A/D module accesses the channels in the order you enter them in the RAM channel-gain list.

4. Load channels and associated gain bits into the RAM channel-gain list by writing to bits 3 to 0 (channel number) and bits 5 and 4 (gain) of the ADCSR. Write as many channels as the number of RAM entries specified in step 3.

5. Write 0 to LLE (CHANCSR bit 15) to preclude further writes to the RAM channel-gain list and enable succeeding events.

6. Load the ADCSR with the following bit pattern:

   - Bit 9 = 1 - A/D Clock Enable
   - Bit 6 = 1 - Interrupt on A/D Done

   You have now:

   A. Enabled the pacer clock circuit to issue conversion triggers.
   B. Set the board to issue an interrupt to the processor when the DMA buffer is filled.

7. Load the SUPCSR with the following bit pattern:

   - Bit 14 = 1 - Interrupt on Error
   - Bit 13 = 0 - Clear DMA Done
   - Bit 12 = 0 - Dual-DMA (optional)
   - Bits 11-10 = 11 - DMA Select
   - Bit 9 = 0 - Buffer B
   - Bit 6 = 0 - A/D Initialize
   - Bit 4 = 1 - Preload Multiplexer
   - Bit 3 = 0 - Software Trigger
   - Bit 2 = 0 - External Trigger
   - Bit 1 = 0 - Internal Clock Source
   - Bit 0 = 0 - Board Initialization

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You have now:

A. Selected the internal clock source for pacer clock outputs (bit 1 should be set for external clock source).
B. Set the board to issue an interrupt if an error occurs during the scan conversions.
C. Preloaded the first channel in the scan into the multiplexer channel latch.

8. The module sets MUXBUSY (ADCSR bit 8) as soon as the multiplexer is preloaded with the number of the first channel in the scan, indicating that it has started acquisition of the signal on the selected channel.

9. Monitor MUXBUSY to clear, indicating that the multiplexer has settled on the selected channel, then load the SUPCSR with the following bit pattern:

- o Bit 14 = 1 - Interrupt on Error
- o Bits 11-10 = 11 - DMA Select
- o Bit 9 = 0 - Buffer B
- o Bit 6 = 0 - A/D Initialize
- o Bit 4 = 0 - Preload Multiplexer
- o Bit 3 = 0 - Software Trigger
- o Bit 2 = 1 - External Trigger Enable
- o Bit 1 = 0 - External Clock Enable
- o Bit 0 = 0 - Board Initialization

You have now:

A. Enabled the external trigger to actuate the pacer clock circuit on the board.
B. Selected the internal frequency source to determine the output rate of the pacer clock (bit 1 should be set for an external clock source).

The first pacer clock pulse after the SUPCSR is loaded starts A/D conversions.

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10. At the end of the A/D conversion, the module places the data in the A/D Data Register and sets A/DDONE (ADCSR bit 7). The DMA circuit transfers the converted data from the A/D Data Register to the DMA buffer. This clears A/DDONE.

11. The multiplexer automatically selects the next channel in the RAM channel-gain list and starts data acquisition concurrent with the conversion of the signal on the previous channel. This process continues until the last channel in the scan is converted. At that point:

    A. Scan Done (SUPCSR bit 8) sets, indicating the end of the current scan.
    B. Triggers are disabled.

12. Successive scans continue with each external trigger until the number of data transfers programmed into the DMA controller is complete. At that point:

    A. DMA Done (SUPCSR bit 15) sets.
    B. The DMA circuit issues an interrupt to the processor.
    C. Triggers are disabled.

A/D triggered scan DMA conversions terminate.

When the board is operated in the Dual-DMA mode, two DMA channels are used. In this mode, conversions do not halt at DMA Done, but data transfers switch from one DMA channel to the other. The memory segments used by each channel for DMA buffers are assigned by the DMA controller. To avoid buffer overwrites and consequent data loss, each time there is a switch of channels, a different segment of memory defined by the contents of the DMA page and offset registers for that channel is used for data transfers. However, if data is transferred from memory to disk concurrent with data acquisition, no loss of data occurs. The Dual-DMA scheme allows a continuous stream of operations until the programmed number of conversions are performed. The DMA circuit issues interrupts to the processor at each DMA Done. When the last buffer is filled, the DMA circuit sets DMA Done, issues an interrupt to the processor, and disables further triggers.

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CAUTION

The speed of operations in the continuous performance mode is limited by the memory to disk transfer rate of the converted data because seek times on the disk are much longer than the A/D conversion times.

The interrupt service routine should perform the following tasks in the Dual-DMA mode:

A. Clear DMA Done by setting Clear DMA Done (SUPCSR bit 13). This is done by writing the following bit pattern to the SUPCSR:

- o Bit 14 = 1 - Interrupt on Error
- o Bit 13 = 1 - Clear DMA Done
- o Bit 12 = 1 - Dual-DMA
- o Bits 11-10 = 11 - DMA Select
- o Bit 9 = 0 - Buffer B
- o Bit 6 = 0 - A/D Initialize
- o Bit 4 = 0 - Preload Multiplexer
- o Bit 3 = 0 - Software Trigger
- o Bit 2 = 0 - External Trigger Enable
- o Bit 1 = 0 - External Clock Enable
- o Bit 0 = 0 - Board Initialization

CAUTION

Inadvertently writing 1 to bit 9 immediately switches the operating DMA channel to Buffer A.

If the next buffer is the last one in the Dual-DMA transfers, the interrupt routine must perform a second write to the SUPCSR to clear the Dual-DMA bit as follows:

- o Bit 14 = 1 - Interrupt on Error
- o Bit 13 = 0 - Clear DMA Done
- o Bit 12 = 0 - Dual-DMA
- o Bits 11-10 = 01 - DMA Select
- o Bit 9 = 0 - Buffer B
- o Bit 6 = 0 - A/D Initialize
- o Bit 4 = 0 - Preload Multiplexer
- o Bit 3 = 0 - Software Trigger
- o Bit 2 = 0 - External Trigger Enable
- o Bit 1 = 0 - External Clock Enable
- o Bit 0 = 0 - Board Initialization

The next setting of DMA Done stops further conversions.

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B. Check the A/D Error bit in the ADCSR.
C. Reprogram the DMA controller.
D. Exit the interrupt subroutine.

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7.2.4 A/D CLOCKED DMA (EXCEPT DT2828)

This mode of A/D conversions is similar to scan conversions discussed in the previous section. However, in this mode, continuous conversions can occur on up to 64K inputs if a single DMA buffer is used. If Dual-DMA is selected, conversions continue until all buffers programmed in the DMA controller are filled. Data transfers are done automatically by the DMA circuit from the A/D Data Register to the DMA buffer.

To convert input signals in this mode, proceed as follows:

1. Load the TMRCTR with selected values for the Prescaler (bits 11-8) and Counter (bits 7-0). These bits determine the frequency of the pacer clock output (conversion pulses) based on an initial frequency of the internal oscillator.

2. Load the SUPCSR with the following bit pattern:

   - o Bit 13 = 1 - Clear DMA Done
   - o Bit 9 = 1 - Buffer B
   - o Bit 6 = 1 - A/D Initialize

   You have now:

   A. Cleared the DMA Done bit.
   B. Selected DMA Buffer 1 (A) for DMA data transfers.
   C. Initialized the A/D data and DMA buffer circuit.

3. Load the CHANCSR with the following bit pattern:

   A. Bit 15 = 1 - Load List Enable
   B. Bits 3-0 = 0000 to 1111 - Number of RAM entries

   You have now:

   A. Enabled writes to the RAM channel-gain list.
   B. Delimited the number of channels in the scan (1 channel for the value of 0, 16 channels for the value of 15).

   The channel numbers and gains are written

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to the ADCSR but they are placed into the RAM channel-gain list. Channel numbers and gains can be loaded in any order, consecutive or random, and multiple entries can be done on any channel. The A/D module accesses the channels in the order they are loaded into the channel-gain list.

4. Load the numbers of channels and the associated gain bits into the RAM channel-gain list by writing to bits 3 to 0 (channel number) and bits 5 and 4 (gain) of the ADCSR.

5. Write 0 to LLE (CHANCSR bit 15) to preclude further writes to the RAM channel-gain list and enable succeeding events.

6. Load the ADCSR with the following bit pattern:

   - o Bit 9 = 1 - A/D Clock Enable
   - o Bit 6 = 1 - Interrupt on A/D Done

   You have now:

   A. Enabled the pacer clock circuit to issue conversion triggers.
   B. Set the board to issue an interrupt to the processor at DMA Done.

7. Load the SUPCSR with the following bit pattern:

   - o Bit 14 = 1 - Interrupt on Error
   - o Bit 13 = 0 - Clear DMA Done
   - o Bit 12 = 0 - Dual-DMA (optional)
   - o Bits 11-10 = 01 - DMA Select
   - o Bit 9 = 0 - Buffer B
   - o Bit 6 = 0 - A/D Initialize
   - o Bit 4 = 1 - Preload Multiplexer
   - o Bit 3 = 0 - Software Trigger
   - o Bit 2 = 0 - External Trigger
   - o Bit 1 = 0 - Internal Clock Source
   - o Bit 0 = 0 - Board Initialization

   You have now:

   A. Selected the internal clock source for pacer clock outputs (bit 1 should be set for external clock source).
   B. Set the board to issue an interrupt

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if an error occurs during the process of A/D conversions.

C. Preloaded the first RAM entry into the multiplexer channel latch.

8. The module sets MUXBUSY (ADCSR bit 8) as soon as the multiplexer is preloaded with the number of the first channel in the scan, indicating that it has started acquisition of the signal on the selected channel.

9. Monitor MUXBUSY until clear, indicating that the multiplexer has settled on the selected channel, then load the SUPCSR with the following bit pattern:

- o Bit 14 = 1 - Interrupt on Error
- o Bits 11-10 = 01 - DMA Select
- o Bit 6 = 0 - A/D Initialize
- o Bit 4 = 0 - Preload Multiplexer
- o Bit 3 = 1 - Software Trigger
- o Bit 2 = 0 - External Trigger Enable
- o Bit 1 = 0 - External Clock Enable
- o Bit 0 = 0 - Board Initialization

You have now:

A. Software-actuated the pacer clock circuit on the board (if you select bit 3 to be clear and bit 2 to be set, trigger the pacer clock circuit externally).

B. Selected the internal frequency source to determine the output rate of the pacer clock (bit 1 should be set for external clock source).

The first pacer clock pulse after the SUPCSR is loaded triggers the A/D conversion.

10. At the end of the A/D conversion, the module places the data in the A/D Data Register and sets the A/DDONE (ADCSR bit 7). The board DMA circuit transfers the data from the A/D Data Register to the first location in the DMA buffer. This clears A/DDONE.

11. The multiplexer automatically selects the next channel in the RAM channel-gain list and starts data acquisition concurrent with

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the conversion of the signal on the previous channel. This process continues until the last channel in the scan is converted. At that point the multiplexer wraps around to the first channel in the scan and conversions resume until DMA Done sets. Successive scans continue with the initial trigger until the number of data transfers programmed into the DMA controller is complete. At that point:

A. DMA Done (SUPCSR bit 15) sets.
B. Triggers are disabled.

A/D clocked DMA conversions terminate.

When the board is operated in the Dual-DMA mode, two DMA channels are used. In this mode, conversions do not halt at DMA Done, but data transfers switch from one DMA channel to the other. The memory segments used by each channel for DMA buffers are assigned by the DMA controller. To avoid buffer overwrites and consequent data loss, each time there is a switch of channels, a different segment of memory defined by the contents of the DMA page and offset registers for that channel is used for data transfers. However, if data is transferred from memory to disk concurrent with data acquisition, no loss of data occurs. The Dual-DMA scheme allows a continuous stream of operations until the programmed number of conversions are performed. The DMA circuit issues interrupts to the processor at each DMA Done. When the last buffer is filled, the DMA circuit sets DMA Done, issues an interrupt to the processor, and disables further triggers.

CAUTION

The speed of operations in the continuous performance mode is limited by the memory to disk transfer rate of the converted data because seek times on the disk are much longer than the A/D conversion times.

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The interrupt service routine should perform the following tasks in the Dual-DMA mode:

A. Clear DMA Done by setting Clear DMA Done (SUPCSR bit 13). This is done by writing the following bit pattern to the SUPCSR:

- o Bit 14 = 1 - Interrupt on Error
- o Bit 13 = 1 - Clear DMA Done
- o Bit 12 = 1 - Dual-DMA
- o Bits 11-10 = 01 - DMA Select
- o Bit 9 = 0 - Buffer B
- o Bit 6 = 0 - A/D Initialize
- o Bit 4 = 0 - Preload Multiplexer
- o Bit 3 = 0 - Software Trigger
- o Bit 2 = 0 - External Trigger Enable
- o Bit 1 = 0 - External Clock Enable
- o Bit 0 = 0 - Board Initialization

CAUTION

Inadvertently writing 1 to bit 9 immediately switches the operating DMA channel to Buffer A.

If the next buffer is the last one in the Dual-DMA transfers, the interrupt routine must perform a second write to the SUPCSR to clear the Dual-DMA bit as follows:

- o Bit 14 = 1 - Interrupt on Error
- o Bit 13 = 0 - Clear DMA Done
- o Bit 12 = 0 - Dual-DMA
- o Bits 11-10 = 01 - DMA Select
- o Bit 9 = 0 - Buffer B
- o Bit 6 = 0 - A/D Initialize
- o Bit 4 = 0 - Preload Multiplexer
- o Bit 3 = 0 - Software Trigger
- o Bit 2 = 0 - External Trigger Enable
- o Bit 1 = 0 - External Clock Enable
- o Bit 0 = 0 - Board Initialization

The next setting of DMA Done stops further conversions.

B. Check the A/D Error bit in the ADCSR.
C. Reprogram the DMA controller.
D. Exit the interrupt subroutine.

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7.2.5 SINGLE-CHANNEL NON-DMA (DT2828, CH 0)

The single-channel non-DMA conversion on the DT2828 is performed most effectively on Channel 0. For conversions on channels other than zero, single non-zero channel or scan, use either the A/D triggered scan DMA or A/D clocked DMA. As with the conventional modules, data acquisition starts as soon as the channel number is preloaded into the multiplexer. A/D conversion starts with a pulse from the pacer clock controlled either by software or external trigger. Data transfers are done by programmed I/O, from the A/D Data Register to the system memory.

To convert an input signal from Channel 0 in the single-channel non-DMA mode, proceed as follows:

1. Set the rate of the pacer clock pulses. This is done by loading the TMRCTR with selected values for the Prescaler (bits 11-8) and Counter (bits 7-0). These bits determine the frequency of the pacer clock outputs (conversion pulses) based on an initial frequency of either the internal oscillator or an external source.

2. Load the SUPCSR with the following bit pattern:

   - o Bit 13 = 1 - Clear DMA Done
   - o Bit 9 = 1 - Buffer B
   - o Bit 6 = 1 - A/D Initialize

   You have now:

   A. Cleared the DMA Done bit.
   B. Selected DMA Buffer 1 (A) for DMA data transfers.
   C. Initialized the A/D data and DMA buffer circuit.

3. Load the CHANCSR with the following bit pattern:

   - o Bit 15 = 1 - Load List Enable
   - o Bits 3-0 = 0000 - Single channel (Number of RAM entries)

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You have now:

A. Enabled writes to the RAM channel-gain list.
B. Specified a single-channel access.

The channel numbers and the gains are written to the ADCSR but they are placed into the RAM channel-gain list.

4. Load the ADCSR with the following bit pattern:

   - Bit 9 = 1 - A/D Clock Enable
   - Bit 6 = 1 - Interrupt on A/D Done (optional)
   - Bits 3-0 = 0000 - Channel Select

   You have now:

   A. Enabled the pacer clock to issue trigger pulses.
   B. Selected Channel 0 for con=ver=sion.
   C. Set the board to issue an interrupt to the processor at the completion of the A/D conversion.

   NOTE

   The DT2828 operates at a gain of one only. The gain bits in the ADCSR are ignored.

5. Write 0 to bit 15 (LLE) of the CHANCSR to preclude further writes to the RAM channel-gain list and to enable succeeding events.

6. Load the SUPCSR with the following bit pattern:

   - Bit 14 = 1 - Interrupt on Error
   - Bits 11-10 = 00 - DMA Select
   - Bit 9 = 0 - Buffer B
   - Bit 6 = 0 - A/D Initialize
   - Bit 4 = 1 - Preload Multiplexer
   - Bit 3 = 0 - Software Trigger
   - Bit 2 = 0 - External Trigger Enable
   - Bit 1 = 0 - External Clock Enable
   - Bit 0 = 0 - Board Initialization

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You have now:

A. Initialized the A/D data buffer circuit.
B. Selected the internal clock source for pacer clock outputs (bit 1 should be set for external clock source).
C. Selected programmed I/O for the conversion operation (non-DMA).
D. Preloaded Channel 0 into the multiplexer channel latch.
E. Set the board to issue an interrupt to the processor if an error occurs during the A/D conversion.

As soon as the SUPCSR is loaded, MUXBUSY (bit 8 of the ADCSR) sets, indicating that the multiplexers on the DT2828 have entered the sample mode.

7. Monitor MUXBUSY until clear, indicating that the multiplexers on all channels have completed data acquisition. An A/D conversion can now be triggered on Channel 0.

8. Load the SUPCSR with the following bit pattern:

- Bit 14 = 1 - Interrupt on Error
- Bits 11-10 = 00 - DMA Select
- Bit 6 = 0 - A/D Initialize
- Bit 4 = 0 - Preload Multiplexer
- Bit 3 = 1 - Software Trigger
- Bit 2 = 0 - External Trigger Enable
- Bit 1 = 0 - External Clock Enable
- Bit 0 = 0 - Board Initialization

You have now:

A. Software-actuated the pacer clock circuit on the board (if you select bit 3 to be clear and bit 2 to be set, trigger the pacer clock circuit externally).
B. Selected the internal clock source to control the pacer clock pulse rates (bit 1 should be set for external clock source).

The first clock pulse after the SUPCSR is loaded triggers an A/D conversion on Channel 0.

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9. At the end of the A/D conversion, the module places the data in the A/D Data Register and sets A/DDONE (ADCSR bit 7). If the Interrupt on A/D Done (ADCSR bit 6) is set, as in the current option, the board issues an interrupt to the processor. Otherwise the program must continually poll A/DDONE to clear, to ascertain that the module has completed the conversion.

10. The processor, under program control, reads the converted data from the A/D Data Register. This clears the A/D Done bit in the ADCSR. The single-channel non-DMA conversion on Channel 0 has completed.

11. To start another single-channel non-DMA conversion on Channel 0, proceed from step 6.

As stated above, it is recommended that Channel 0 be used for all single-channel conversions. However, it is possible to perform single-channel conversions on a different channel using the following procedure:

1. Do steps 2 to 10 on the selected channel and disregard the data.

2. Do steps 2 to 7 on Channel 0 (to put the converter back in the sample mode).

3. Do steps 2 to 10 on the selected channel.

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7.2.6 SINGLE-CHANNEL DMA (DT2828, CH 0)

The single-channel DMA performs up to 64K conversions on a selected channel with one trigger if a single DMA buffer is used. If you select Dual-DMA, you can define as many buffers as needed, each buffer containing up to 64K words. Conversions can be performed continuously on the selected channel until all user-defined buffers are full. Data transfers are done automatically by the DMA circuit from the A/D Data Register to the DMA buffer. As with the conventional modules, data acquisition starts when the channel is preloaded into the multiplexer. A/D conversion starts with a pulse from the pacer clock controlled either by software or external trigger.

The single-channel DMA conversions are most effectively performed on Channel 0 because only one conversion separates two successive sample phases. If any other channel is selected, two conversions will have to be performed, one on Channel 0 and another on the selected channel, before entering the next sample phase. For conversions on channels other than zero, single non-zero channel or scan, use either the A/D triggered scan DMA or A/D clocked DMA mode of operation.

To convert an input signal from Channel 0 in the A/D clocked DMA mode, proceed as follows:

1. Set the rate of the pacer clock pulses. This is done by loading the TMRCTR with selected values for the Prescaler (bits 11-8) and Counter (bits 7-0). These bits determine the frequency of the pacer clock outputs (conversion pulses) based on an initial frequency of the internal oscillator.

2. Load the SUPCSR with the following bit pattern:

    - Bit 13 = 1 - Clear DMA Done
    - Bit 9 = 1 - Buffer B
    - Bit 6 = 1 - A/D Initialize

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You have now:

A. Cleared the DMA Done bit.
B. Selected DMA Buffer 1 (A) for DMA data transfers.
C. Initialized the A/D data and DMA buffer circuit.

3. Load the CHANCSR with the following bit pattern:
   - o Bit 15 = 1 - Load List Enable
   - o Bits 3-0 = 0000 - Number of RAM entries

You have now:

A. Enabled writes to the RAM channel-gain list.
B. Specified a single-channel access.

The channel number is written to the ADCSR but it is placed into the RAM channel-gain list.

4. Load the ADCSR with the following bit pattern:

   - o Bit 9 = 1 - A/D Clock Enable
   - o Bit 6 = 1 - Interrupt on A/D Done
   - o Bits 3-0 = 0000 - Channel Select

You have now:

A. Enabled the pacer clock to issue trigger pulses.
B. Selected Channel 0 for conversions.
C. Set the board to issue an interrupt to the processor when the DMA buffer is filled.

5. Write 0 to bit 15 (LLE) of the CHANCSR to preclude further writes to the RAM channel-gain list and to enable succeeding events.

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6. Load the SUPCSR with the following bit pattern:

   - o Bit 14 = 1 - Interrupt on Error
   - o Bits 11-10 = 01 - DMA Select
   - o Bit 9 = 0 - Buffer B
   - o Bit 6 = 0 - A/D Initialize
   - o Bit 4 = 1 - Preload Multiplexer
   - o Bit 3 = 0 - Software Trigger
   - o Bit 2 = 0 - External Trigger Enable
   - o Bit 1 = 0 - External Clock Enable
   - o Bit 0 = 0 - Board Initialization

   You have now:

   A. Selected the internal clock source for pacer clock outputs (bit 1 should be set for external clock source).
   B. Selected DMA for transfers of converted data.
   C. Set the board to issue an interrupt if an error occurs during the the process of A/D conversions.
   D. Started data acquisition on all four channels.

   As soon as the SUPCSR is loaded, MUXBUSY (bit 8 of the ADCSR) sets.

7. Monitor MUXBUSY until clear, indicating that the multiplexers on all channels have completed data acquisition and that all channels are placed in the hold mode. An A/D conversion can now be triggered on Channel 0.

8. Load the SUPCSR with the following bit pattern:

   - o Bit 14 = 1 - Interrupt on Error
   - o Bits 11-10 = 01 - DMA Select
   - o Bit 6 = 0 - A/D Initialize
   - o Bit 4 = 0 - Preload Multiplexer
   - o Bit 3 = 1 - Software Trigger
   - o Bit 2 = 0 - External Trigger Enable
   - o Bit 1 = 0 - External Clock Enable
   - o Bit 0 = 0 - Board Initialization

   You have now:

   A. Software-actuated the pacer clock circuit on the board (if you select bit 3 to be clear and bit 2 to be

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set, you trigger the pacer clock circuit externally).

B. Selected the internal clock source to control the pacer clock pulse rates (bit 1 should be set for external clock source).

The first clock pulse after the SUPCSR is loaded triggers A/D conversion on Channel 0.

9. At the end of the A/D conversion, the module places the data in the A/D Data Register and sets A/DDONE (ADCSR bit 7). The DMA circuit transfers the converted data from the A/D Data Register to the DMA buffer. This clears A/DDONE. The single-channel DMA conversion completes when the user-defined DMA buffer is filled. At that point:

   A. DMA Done (SUPCSR bit 15) sets
   B. DMA Done issues an interrupt to the processor
   C. Triggers are disabled.

   The single-channel DMA conversion has completed.

To perform a single-channel DMA conversion on another channel, proceed from step 2 above.

When the board is operated in the Dual-DMA mode, two DMA channels are used. In this mode, conversions do not halt at DMA Done, but data transfers switch from one DMA channel to the other. The memory segments used by each channel for DMA buffers are assigned by the DMA controller. To avoid buffer overwrites and consequent data loss, each time there is a switch of channels, a different segment of memory defined by the contents of the DMA page and offset registers for that channel is used for data transfers. However, if data is transferred from memory to disk concurrent with data acquisition, no loss of data occurs. The Dual-DMA scheme allows a continuous stream of operations until the programmed number of conversions are performed. The DMA circuit issues interrupts to the processor at each DMA Done. When the last buffer is filled, the DMA circuit sets DMA Done, issues an interrupt to the processor, and disables further triggers.

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CAUTION

The speed of operations in the continuous performance mode is limited by the memory to disk transfer rate of the converted data because seek times on the disk are much longer than the A/D conversion times.

The interrupt service routine should perform the following tasks in the Dual-DMA mode:

A. Clear DMA Done by setting CLRDMADNE (SUPCSR bit 13). This is done by writing the following bit pattern to the SUPCSR:

- o Bit 14 = 1 - Interrupt on Error
- o Bit 13 = 1 - Clear DMA Done
- o Bit 12 = 1 - Dual-DMA
- o Bits 11-10 = 01 - DMA Select
- o Bit 9 = 0 - Buffer B
- o Bit 6 = 0 - A/D Initialize
- o Bit 4 = 0 - Preload Multiplexer
- o Bit 3 = 0 - Software Trigger
- o Bit 2 = 0 - External Trigger Enable
- o Bit 1 = 0 - External Clock Enable
- o Bit 0 = 0 - Board Initialization

CAUTION

Inadvertently writing 1 to bit 9 immediately switches the operating DMA channel to Buffer A.

If the next buffer is the last one in the Dual-DMA transfers, the interrupt routine must perform a second write to the SUPCSR to clear the Dual-DMA bit as follows:

- o Bit 14 = 1 - Interrupt on Error
- o Bit 13 = 0 - Clear DMA Done
- o Bit 12 = 0 - Dual-DMA
- o Bits 11-10 = 01 - DMA Select
- o Bit 9 = 0 - Buffer B
- o Bit 6 = 0 - A/D Initialize
- o Bit 4 = 0 - Preload Multiplexer
- o Bit 3 = 0 - Software Trigger
- o Bit 2 = 0 - External Trigger Enable
- o Bit 1 = 0 - External Clock Enable
- o Bit 0 = 0 - Board Initialization

The next setting of DMA Done stops further conversions.

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B. Check the A/D Error bit in the ADCSR.
C. Reprogram the DMA controller.
D. Exit the interrupt subroutine.

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7.2.7 A/D TRIGGERED SCAN DMA (DT2828)

Channel scan conversions can be performed when the board is used in the A/D triggered scan DMA mode. The simultaneous sample and hold module performs conversions on a list of channels (up to 16) loaded in the RAM channel-gain list. Data transfers are done automatically by the DMA circuit, from the A/D Data Register to the DMA buffer. This operating mode is recommended to be used with external triggers. The multiplexer scans the channels in the RAM channel-gain list once with each trigger.

NOTE

The module enters the hold mode on all channels when the first conversion clock is received and exits the hold mode (enters the sample mode) each time Channel 0 is loaded into the multiplexer from the RAM channel-gain list. Due to the sample and hold circuit droop rate and requirements of conversion accuracy to within 1 LSB, the hold mode of the DT2828 is limited by hardware to a maximum of 50ms. At the end of that period, the module automatically reverts to the sample mode. It is necessary, therefore, that your software process all channels within the scan and access the next Channel 0 (if applicable) before the permitted hold period expires.

To convert input signals in this mode, proceed as follows:

1. Load the TMRCTR with selected values for the Prescaler (bits 11-8) and Counter (bits 7-0). These bits determine the frequency of the pacer clock output (conversion pulses) based on an initial frequency of either the internal oscillator or an external source.

2. Load the SUPCSR with the following bit pattern:

   - o Bit 13 = 1 - Clear DMA Done
   - o Bit 9 = 1 - Buffer B
   - o Bit 6 = 1 - A/D Initialize

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You have now:

A. Cleared the DMA Done bit.
B. Selected DMA Buffer 1 (A) for DMA data transfers.
C. Initialized the A/D data and DMA buffer circuit.

3. Load the CHANCSR with the following bit pattern:
   - o Bit 15 = 1 - Load List Enable
   - o Bits 3-0 = 0000 to 1111 - Number of RAM entries

   You have now:

   A. Enabled writes to the RAM channel-gain list.
   B. Delimited the number of channels in the scan (0 for one channel; 15 for 16 channels).

   The channel numbers are written to the ADCSR but they are placed into the RAM channel-gain list.

4. Load the channel numbers into the RAM channel-gain list by writing to bits 3 to 0 (channel number) of the ADCSR in the order to be accessed. The channel numbers can be loaded in any order, consecutive or random. The A/D module accesses the channels in the order loaded into the RAM channel-gain list, and each time the multiplexer selects Channel 0, the module reverts to the sample mode. If a channel is accessed more than once within the same hold period, it yields the same digital value as the first conversion on the channel, provided the maximum hold period (50ms) has not expired. At the expiration of the maximum hold period, the module automatically reverts to the sample mode. You can perform a complete scan (Channels 0 to 3) up to four times, or convert inputs from a channel other than Channel 0 up to eight times with a single trigger.

5. Write 0 to LLE (bit 15 of the CHANCSR) to preclude further writes to the RAM channel-gain list and enable succeeding events.

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6. Load the ADCSR with the following bit pattern:

   - o Bit 9 = 1 - A/D Clock Enable
   - o Bit 6 = 1 - Interrupt on A/D Done

   You have now:

   A. Enabled the pacer clock circuit to issue conversion triggers.
   B. Set the board to issue an interrupt to the processor when the DMA buffer is filled.

7. Load the SUPCSR with the following bit pattern:

   - o Bit 14 = 1 - Interrupt on Error
   - o Bit 13 = 0 - Clear DMA Done
   - o Bit 12 = 0 - Dual-DMA (optional)
   - o Bits 11-10 = 11 - DMA Select
   - o Bit 9 = 0 - Buffer B
   - o Bit 6 = 0 - A/D Initialize
   - o Bit 4 = 1 - Preload Multiplexer
   - o Bit 3 = 0 - Software Trigger
   - o Bit 2 = 0 - External Trigger
   - o Bit 1 = 0 - Internal Clock Source
   - o Bit 0 = 0 - Board Initialization

   You have now:

   A. Initialized the A/D data and DMA buffer circuit.
   B. Selected the internal clock source to control the pacer clock pulse rates (bit 1 should be set for external clock source).
   C. Preloaded the multiplexer with the address of the first channel in the scan (Channel 0).
   D. Set the board to issue an interrupt if an error occurs during the scan.

   As soon as the SUPCSR is loaded, MUXBUSY (bit 8 of the ADCSR) sets, indicating that the A/D module has started data acquisition on signals present at the input channels. The A/D module is now in the sample mode.

8. Monitor MUXBUSY until clear, indicating that the channel is ready to be converted. An A/D conversion can now be triggered on Channel 0.

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9. Load the SUPCSR with the following bit pattern:

   - o Bit 14 = 1 - Interrupt on Error
   - o Bits 11-10 = 11 - DMA Select
   - o Bit 9 = 0 - Buffer B
   - o Bit 6 = 0 - A/D Initialize
   - o Bit 4 = 0 - Preload Multiplexer
   - o Bit 3 = 1 - Software Trigger
   - o Bit 2 = 0 - External Trigger Enable
   - o Bit 1 = 0 - External Clock Enable
   - o Bit 0 = 0 - Board Initialization

   You have now:

   A. Software-actuated the pacer clock circuit on the board (if you select bit 3 to be clear and bit 2 to be set, you trigger the pacer clock circuit externally).
   B. Selected the internal clock source to control the pacer clock pulse rates (bit 1 should be set for external clock source).

   The first clock pulse after the SUPCSR is loaded puts all the channels in the hold mode and triggers A/D conversion on Channel 0.

10. At the end of the A/D conversion, the module places the data in the A/D Data Register and sets A/DDONE. The DMA circuit transfers the converted data from the A/D Data Register to the DMA buffer. This clears A/DDONE.

11. The module starts to convert the next channel in the scan. Conversions continue until the multiplexer selects Channel 0 again. At that point all channels are placed back in the sample mode. This process continues until all channels in the RAM channel-gain list are converted. At that point:

    A. Scan Done (SUPCSR bit 8) sets, indicating the end of the current scan.
    B. Triggers are disabled.

12. For another scan on the same channel list, proceed from step 7 above. If a scan is to

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be performed on a different list of channels, proceed from step 2.

13. Successive scan operations can be performed on the same channels with each external trigger until the number of data transfers programmed into the DMA controller is complete. At that point:

    A. DMA Done (SUPCSR bit 15) sets
    B. The DMA circuit issues an interrupt to the processor
    C. Triggers are disabled.

    A/D triggered scan DMA conversions terminate.

When the board is operated in the Dual-DMA mode, two DMA channels are used. In this mode, conversions do not halt at DMA Done, but data transfers switch from one DMA channel to the other. The memory segments used by each channel for DMA buffers are assigned by the DMA controller. To avoid buffer overwrites and consequent data loss, each time there is a switch of channels, a different segment of memory defined by the contents of the DMA page and offset registers for that channel is used for data transfers. However, if data is transferred from memory to disk concurrent with data acquisition, no loss of data occurs. The Dual-DMA scheme allows a continuous stream of operations until the programmed number of conversions are performed. The DMA circuit issues interrupts to the processor at each DMA Done. When the last buffer is filled, the DMA circuit sets DMA Done, issues an interrupt to the processor, and disables further triggers.

CAUTION

The speed of operations in the continuous performance mode is limited by the memory to disk transfer rate of the converted data because seek times on the disk are much longer than the A/D conversion times.

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The interrupt service routine should perform the following tasks in the Dual-DMA mode:

A. Clear DMA Done by setting Clear DMA Done (SUPCSR bit 13). This is done by writing the following bit pattern to the SUPCSR:

- o Bit 14 = 1 - Interrupt on Error
- o Bit 13 = 1 - Clear DMA Done
- o Bit 12 = 1 - Dual-DMA
- o Bits 11-10 = 11 - DMA Select
- o Bit 9 = 0 - Buffer B
- o Bit 6 = 0 - A/D Initialize
- o Bit 4 = 0 - Preload Multiplexer
- o Bit 3 = 0 - Software Trigger
- o Bit 2 = 0 - External Trigger Enable
- o Bit 1 = 0 - External Clock Enable
- o Bit 0 = 0 - Board Initialization

CAUTION

Inadvertently writing 1 to bit 9 immediately switches the operating DMA channel to Buffer A.

If the next buffer is the last one in the Dual-DMA transfers, the interrupt routine must perform a second write to the SUPCSR to clear the Dual-DMA bit as follows:

- o Bit 14 = 1 - Interrupt on Error
- o Bit 13 = 0 - Clear DMA Done
- o Bit 12 = 0 - Dual-DMA
- o Bits 11-10 = 01 - DMA Select
- o Bit 9 = 0 - Buffer B
- o Bit 6 = 0 - A/D Initialize
- o Bit 4 = 0 - Preload Multiplexer
- o Bit 3 = 0 - Software Trigger
- o Bit 2 = 0 - External Trigger Enable
- o Bit 1 = 0 - External Clock Enable
- o Bit 0 = 0 - Board Initialization

The next setting of DMA Done stops further conversions.

B. Check the A/D Error bit in the ADCSR.
C. Reprogram the DMA controller.
D. Exit the interrupt subroutine.

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7.2.8 A/D CLOCKED DMA (DT2828)

This mode of A/D conversions is similar to scan conversions discussed in the previous section. However, in this mode, continuous conversions can occur with one trigger on up to 64K inputs if a single DMA buffer is used. If Dual-DMA is selected, conversions continue until all buffers programmed in the DMA controller are filled. Data transfers are done automatically by the DMA circuit from the A/D Data Register to the DMA buffer. This operating mode should be selected for a single conversion on a channel as well as for conversions on a scan of channels. Also, this operating mode allows continuous conversions on Channel 0 with maximum throughput.

NOTE

The module enters the hold mode on all channels when the conversion clock is received and exits the hold mode (enters the sample mode) each time Channel 0 is loaded into the multiplexer from the RAM channel-gain list. Due to the sample and hold circuit droop rate and requirements of conversion accuracy to within 1 LSB, the hold mode of the DT2828 is limited by hardware to a maximum of 50ms. At the end of that period, the module automatically reverts to the sample mode. It is necessary, therefore, that your software process all channels within the scan and access the next Channel 0 (if applicable) before the permitted hold period expires.

To convert input signals in this mode, proceed as follows:

1. Load the TMRCTR with selected values for the Prescaler (bits 11-8) and Counter (bits 7-0). These bits determine the frequency of the pacer clock output (conversion pulses) based on an initial frequency of either the internal oscillator or an external source.

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2. Load the SUPCSR with the following bit pattern:

   - o Bit 13 = 1 - Clear DMA Done
   - o Bit 9 = 1 - Buffer B
   - o Bit 6 = 1 - A/D Initialize

   You have now:

   A. Cleared the DMA Done bit.
   B. Selected DMA Buffer 1 (A) for DMA data transfers.
   C. Initialized the A/D data and DMA buffer circuit.

3. Load the CHANCSR with the following bit pattern:

   A. Bit 15 = 1 - Load List Enable
   B. Bits 3-0 = 0000 to 1111 - Number of RAM entries

   You have now:

   A. Enabled writes to the RAM channel-gain list.
   B. Delimited the number of channels in the scan (0 for one channel; 15 for 16 channels).

   The channel numbers are written to the ADCSR but they are placed into the RAM channel-gain list.

4. Load the channel numbers into the RAM channel-gain list by writing to bits 3 to 0 (channel number) of the ADCSR in the order to be accessed. The channel numbers can be loaded in any order, consecutive or random. The A/D module accesses the channels in the order loaded into the RAM channel-gain list, and each time the multiplexer selects Channel 0, the module reverts to the sample mode. If a channel is accessed more than once within the same hold period, it will yield the same digital value as the first conversion on the channel, provided the maximum hold period (50ms) has not expired. At the expiration of the maximum hold period, the module automatically reverts to the sample mode. If you select continuous conversions on Channel 0, just load number 0 in the first location of the RAM

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channel-gain list (specify one entry in the CHANCSR). For continuous conversions on a single channel other than Channel 0, load Channel 0 in the first location of the RAM channel-gain list, and the number of the selected channel in the second location (specify two entries in the CHANCSR).

5. Write 0 to LLE (bit 15 of the CHANCSR) to preclude further writes to the RAM channel-gain list and enable succeeding events.

6. Load the ADCSR with the following bit pattern:

   - Bit 9 = 1 - A/D Clock Enable
   - Bit 6 = 1 - Interrupt on A/D Done

   You have now:

   A. Enabled the pacer clock circuit to issue conversion triggers.
   B. Set the board to issue an interrupt to the processor when the DMA buffer is full.

7. Load the SUPCSR with the following bit pattern:

   1. Bit 14 = 1 - Interrupt on Error
   2. Bit 13 = 1 - Clear DMA Done
   3. Bit 12 = 0 - Dual-DMA (optional)
   4. Bits 11-10 = 01 - DMA Select
   5. Bit 9 = 0 - Buffer B
   6. Bit 6 = 0 - A/D Initialize
   7. Bit 4 = 1 - Preload Multiplexer
   8. Bit 3 = 0 - Software Trigger
   9. Bit 2 = 0 - External Trigger
   10. Bit 1 = 0 - Internal Clock Source
   11. Bit 0 = 0 - Board Initialization

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You have now:

A. Selected the internal clock source to control the pacer clock pulse rates (bit 1 should be set for external clock source).
B. Set the board to issue an interrupt if an error occurs during the process of A/D conversions.
C. Started data acquisition on all four channels.

As soon as the SUPCSR is loaded, MUXBUSY (bit 8 of the ADCSR) sets, indicating that the A/D module has started data acquisition on signals present at the input channels. The A/D module is now in the sample mode.

8. Monitor MUXBUSY until clear, indicating that the multiplexers on all channels have settled and the inputs are ready to be converted. An A/D conversion can now be triggered on Channel 0.

9. Load the SUPCSR with the following bit pattern:

- Bit 14 = 1 - Interrupt on Error
- Bits 11-10 = 01 - DMA Select
- Bit 9 = 0 - Buffer B
- Bit 6 = 0 - A/D Initialize
- Bit 4 = 0 - Preload Multiplexer
- Bit 3 = 1 - Software Trigger
- Bit 2 = 0 - External Trigger Enable
- Bit 1 = 0 - External Clock Enable
- Bit 0 = 0 - Board Initialization

You have now:

A. Software-actuated the pacer clock circuit on the board (if you select bit 3 to be clear and bit 2 to be set, trigger the pacer clock circuit externally).
B. Selected the internal clock source to control the pacer clock pulse rates (bit 1 should be set for external clock source).

The first clock pulse after the SUPCSR is loaded triggers A/D conversion on Channel 0.

10. At the end of the A/D conversion, the

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module places the data in the A/D Data Register and sets the A/DDONE (ADCSR bit 7). The board DMA circuit transfers the data from the A/D Data Register to the first location in the DMA buffer. This clears A/DDONE. The first conversion (Channel 0) is complete.

There are three possible conversion sequences after completion of the first conversion on Channel 0, depending on the entries in the RAM channel-gain list:

A. A single entry of Channel 0. The A/D module reverts to the sample mode and resumes data acquisition.

B. Two entries, Channel 0 and any other channel. The A/D module starts conversion on the other channel as soon as converted data from Channel 0 is placed in the A/D Data Register, then reverts to the sample mode.

C. More than two entries (up to 16). The A/D module completes conversion on all succeeding channels (maximum of 3 channels), then selects Channel 0 and reverts to the sample mode.

11. A/D conversions continue uninterrupted until the DMA buffer(s) is full. At that point:

A. DMA Done (SUPCSR bit 15) sets.
B. The DMA circuit issues an interrupt to the processor.
C. Triggers are disabled.

A/D clocked DMA conversions terminate.

When the board is operated in the Dual-DMA mode, two DMA channels are used. In this mode, conversions do not halt at DMA Done, but data transfers switch from one DMA channel to the other. The memory segments used by each channel for DMA buffers are assigned by the DMA controller. To avoid buffer overwrites and consequent data loss, each time there is a switch of channels, a different segment of memory defined by the contents of the DMA page and offset registers for that channel is used for data transfers. However, if data is transferred from memory to disk

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concurrent with data acquisition, no loss of data occurs. The Dual-DMA scheme allows a continuous stream of operations until the programmed number of conversions are performed. The DMA circuit issues interrupts to the processor at each DMA Done. When the last buffer is filled, the DMA circuit sets DMA Done, issues an interrupt to the processor, and disables further triggers.

CAUTION

The speed of operations in the continuous performance mode is limited by the memory to disk transfer rate of the converted data because seek times on the disk are much longer than the A/D conversion times.

The interrupt service routine should perform the following tasks in the Dual-DMA mode:

A. Clear DMA Done by setting Clear DMA Done (SUPCSR bit 13). This is done by writing the following bit pattern to the SUPCSR:

- Bit 14 = 1 - Interrupt on Error
- Bit 13 = 1 - Clear DMA Done
- Bit 12 = 1 - Dual-DMA
- Bits 11-10 = 01 - DMA Select
- Bit 9 = 0 - Buffer B
- Bit 6 = 0 - A/D Initialize
- Bit 4 = 0 - Preload Multiplexer
- Bit 3 = 0 - Software Trigger
- Bit 2 = 0 - External Trigger Enable
- Bit 1 = 0 - External Clock Enable
- Bit 0 = 0 - Board Initialization

CAUTION

Inadvertently writing 1 to bit 9 immediately switches the operating DMA channel to Buffer A.

If the next buffer is the last one in the Dual-DMA transfers, the interrupt routine must perform a second write to the SUPCSR to clear the Dual-DMA bit as follows:

- Bit 14 = 1 - Interrupt on Error
- Bit 13 = 0 - Clear DMA Done
- Bit 12 = 0 - Dual-DMA
- Bits 11-10 = 01 - DMA Select
- Bit 9 = 0 - Buffer B
- Bit 6 = 0 - A/D Initialize

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- o Bit 4 = 0 - Preload Multiplexer
- o Bit 3 = 0 - Software Trigger
- o Bit 2 = 0 - External Trigger Enable
- o Bit 1 = 0 - External Clock Enable
- o Bit 0 = 0 - Board Initialization

The next setting of DMA Done stops further conversions.

B. Check the A/D Error bit in the ADCSR.
C. Reprogram the DMA controller.
D. Exit the interrupt subroutine.

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7.3 D/A SUBSYSTEM

NOTE

This section does not apply to the DT2824-PGH and DT2824-PGL models.

The D/A conversion on the DT2821 series board is performed in three stages:

1. Selection of the conversion parameters. This is done by writing to the SUPCSR and DACSR.
2. Loading the digital code into the DADAT.
3. Converting the digital input code into an analog output voltage level.

The D/A subsystem permits two methods of digital code transfer to the DAC(s): Single conversion in programmed I/O, or multiple conversions using DMA. In single conversion programmed I/O, the program loads successive digital codes to be converted into the D/A Data Register. In multiple conversions with DMA, the program loads the DMA buffer with the list of digital codes to be converted. The DMA circuit then feeds the digital codes from the DMA buffer to the DAC(s) in consecutive order, considerably reducing the software overhead.

NOTE

The DMA circuit can be used by only one subsystem when more than one subsystem is operating on the board. When the A/D subsystem is using the DMA, for example, the D/A subsystem must operate in programmed I/O.

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7.3.1 SINGLE D/A CONVERSION

To obtain a voltage output from the DAC(s), proceed as follows:

1. Write 1 to bit 5 of the SUPCSR. This clears the D/A Error (DACSR bit 15) and initializes the DAC data buffers.

2. Load the D/A Control/Status Register with the following bit pattern:

   - o Bit 9 = 0 - Y Channel Select (DAC 0, bit 8 = 1)
     = 1 - Y Channel Select (DAC 1, bit 8 = 1)
   - o Bit 8 = 0 - Single Channel Select (DACs 0 and 1)
     = 1 - Single Channel Select (DAC 0 or 1)
   - o Bit 6 = 1 - Int. on D/A Ready (optional)
   - o Bit 5 = 0 - D/A Clock Enable

   You have now:

   A. Allowed single D/A conversions.
   B. Selected DAC 0, DAC 1, or both DACs, depending on the states of bits 9 and 8 (see Section 5.5).
   C. Set the DAC(s) to interrupt the processor when the D/A conversion is complete (optional).

3. Load the D/A Data Register with the digital code to be converted.

4. Load the SUPCSR with the following bit pattern:

   - o Bit 14 = 1 - Interrupt on Error
   - o Bits 11-10 = 00 - DMA Select
   - o Bit 7 = 1 - DAC Single Conversion
   - o Bit 5 = 0 - D/A Initialize
   - o Bit 0 = 0 - Board Initialization

   You have now:

   A. Selected the programmed I/O mode of operation.
   B. Caused the D/A subsystem to execute a single conversion.
   C. Set the D/A subsystem to interrupt the processor on error.

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5. At the next pulse of the pacer clock, the selected DAC starts conversion of the digital code into the corresponding output voltage level.

6. When the D/A conversion completes, DACRDY (DACSR bit 7) sets, indicating that the DAC has completed the current conversion. If the D/A subsystem is operating in programmed I/O mode (as in this sequence) the setting of bit 7 generates an interrupt to the processor.

NOTE

When the board is operating in the A/D triggered scan mode or the A/D clocked DMA mode, setting bit 6 does not enable DACRDY (bit 7) to interrupt. When operating the A/D subsystem in either one of these two modes, you must monitor bit 7 to ascertain the state of the DAC.

7. Load the D/A Data Register with the next digital code to be converted. The D/A conversion triggers with the next pulse of the pacer clock. Loading the D/A Data Register and subsequent conversions continue at each clock pulse in the selected mode until the program ceases to load the D/A Data Register or the pacer clock is disabled by clearing the D/A Clock Enable.

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7.3.2 D/A CLOCKED DMA

To convert digital input codes into corresponding voltage levels in the D/A clocked DMA mode, proceed as follows:

1. Write 1 to bit 5 of the SUPCSR. This clears the D/A Error (DACSR bit 15) and initializes the DAC data buffers.

2. Load the D/A Control/Status Register with the following bit pattern:

   - Bit 9 = 0 - Y Channel Select (DAC 0, bit 8 = 1)
     = 1 - Y Channel Select (DAC 1, bit 8 = 1)
   - Bit 8 = 0 - Single Channel Select (DACs 0 and 1)
     = 1 - Single Channel Select (DAC 0 or 1)
   - Bit 6 = 1 - Int. on D/A Ready
   - Bit 5 = 1 - D/A Clock Enable

   You have now:

   A. Enabled the pacer clock to trigger D/A conversions.
   B. Selected DAC 0, DAC 1, or both DACs, depending on the states of bits 9 and 8 (see Section 5.5).
   C. Set the DAC(s) to interrupt the processor when the D/A conversion is complete.

3. Load the SUPCSR with the following pattern:

   - Bit 14 = 1 - Interrupt on Error
   - Bit 13 = 1 - Clear DMA Done
   - Bit 12 = 0 - Dual-DMA
   - Bits 11-10 = 10 - DMA Select
   - Bit 9 = 1 - Buffer B
   - Bit 5 = 1 - D/A Initialize
   - Bit 0 = 0 - Board Initialization

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You have now:

A. Set the D/A subsystem for D/A clocked DMA conversions.
B. Cleared the DMA Done bit.
C. Cleared A/DERR and initialized the DAC data buffers.
D. Selected DMA buffer 1 (A) for input codes.
E. Set the D/A subsystem to interrupt the processor on error.

4. Load the DMA buffer with digital codes to be converted. You can use the full buffer (64K words for single buffer) or only the buffer segment defined by the DMA controller.

5. Load the D/A Data Register with any digital code to initiate D/A conversions.

6. At the next pulse of the pacer clock, the selected DAC starts conversion of the digital input data into the corresponding output voltage level.

7. When the first D/A conversion completes, DACRDY (DACSR bit 7) sets, indicating that the DAC has completed the current conversion. If bit 14 of the SUPCSR is set (as in this discussion), the D/A subsystem generates an interrupt to the processor. Otherwise, the program must poll bit 7 to ascertain the completion of a D/A conversion. The interrupt service routine should perform the following tasks:

   A. Check DMA Done.
   B. If DMA Done is not set, check D/A Error in the DACSR. If the error bit is set, handle error. If the error bit is not set, reprogram the DMA controller, then exit the subroutine.
   C. If DMA Done is set, check D/A Error in the DACSR. If the error bit is set, handle error. If the error bit is not set, exit the subroutine.

8. The DMA circuit transfers the first digital code from the DMA buffer into the D/A Data Register. Conversion starts on the new

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digital data at the first clock pulse after the D/A Data Register is loaded.

9. At the end of the conversion, the DAC outputs the analog voltage to be used as required by the application.

10. The DMA circuit transfers the next digital code from the DMA buffer to the A/D Data Register and the conversion operation resumes as described above. Digital codes are transferred to the D/A Data Register in the order they are loaded into the DMA buffer. D/A conversions are triggered at each pulse of the pacer clock (two conversions per clock pulse if bit 8 of DACSR is clear) after the DMA circuit loads the digital code into the D/A Data Register.

11. When all the digital codes in the DMA buffer are converted, the DMA circuit sets DMAD (SUPCSR bit 15), indicating the completion of DMA transfers.

When the D/A subsystem is operated in the Dual-DMA mode, two DMA channels are used. In this mode, conversions do not halt at DMA Done, but data transfers switch from one DMA channel to the other. The memory segments used by each channel for DMA buffers are assigned by the DMA controller. DMA channels alternate, and each time there is a switch of channels, a different segment of memory is used for data transfers. This scheme allows a continuous stream of conversions until the programmed number of conversions are performed.

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The interrupt service routine should perform the following tasks in the Dual-DMA mode:

A. Clear DMA Done by setting Clear DMA Done (SUPCSR bit 13). This is done by writing the following bit pattern to the SUPCSR:

   - o Bit 14 = 1 - Interrupt on Error
   - o Bit 13 = 1 - Clear DMA Done
   - o Bit 12 = 1 - Dual-DMA
   - o Bits 11-10 = 10 - DMA Select
   - o Bit 9 = 0 - Buffer B
   - o Bit 6 = 0 - A/D Initialize
   - o Bit 4 = 0 - Preload Multiplexer
   - o Bit 3 = 0 - Software Trigger
   - o Bit 2 = 0 - External Trigger Enable
   - o Bit 1 = 0 - External Clock Enable
   - o Bit 0 = 0 - Board Initialization

   If the next buffer is the last one in the Dual-DMA transfers, the interrupt routine must perform a second write to the SUPCSR to clear the Dual-DMA bit as follows:

   - o Bit 14 = 1 - Interrupt on Error
   - o Bit 13 = 0 - Clear DMA Done
   - o Bit 12 = 0 - Dual-DMA
   - o Bits 11-10 = 01 - DMA Select
   - o Bit 9 = 0 - Buffer B
   - o Bit 6 = 0 - A/D Initialize
   - o Bit 4 = 0 - Preload Multiplexer
   - o Bit 3 = 0 - Software Trigger
   - o Bit 2 = 0 - External Trigger Enable
   - o Bit 1 = 0 - External Clock Enable
   - o Bit 0 = 0 - Board Initialization

   The next setting of DMA Done stops further conversions.

B. Check D/A Error in the DACSR.
C. Reprogram the DMA controller.
D. Exit the interrupt subroutine.

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7.4 DIGITAL I/O SUBSYSTEM

The DIO Data Register serves to transfer data under program control between the computer system (IBM Personal Computer AT) and an I/O device attached to the J1 connector of the DT2821 series. The direction of data transfer through the DIO Data Register is controlled by bits 1 and 0 of the D/A Control/Status Register as discussed in Section 5.5.

To operate the digital I/O subsystem, proceed as follows:

1. For an output operation, load the DIO Data Register with the word or byte to be transferred to the I/O device.

2. Load the D/A Control/Status Register with the bit pattern appropriate to the data transfer as shown in Table 7-1. This outputs the data stored in the DIO Data Register to the user interface.

TABLE 7-1: DIO DATA TRANSFERS

DATA TRANSFER DIRECTION	D/A CONTROL/STATUS REGISTER BIT 1	BIT 0
Output Low Byte	0	1
Output High Byte	1	0
Output Word	1	1

When a port is set for input (corresponding transfer control bit clear), the DT2821 series board can read the data sent to the port by an I/O device.

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APPENDIX A

IBM AT P1 AND P2 SIGNALS

TABLE A-1: P1 PIN ASSIGNMENTS

PIN	MNEMONIC	SIGNAL DESCRIPTION
A01	-I/O CH CK	No Connection
A02	SD7	Data bit 7
A03	SD6	Data bit 6
A04	SD5	Data bit 5
A05	SD4	Data bit 4
A06	SD3	Data bit 3
A07	SD2	Data bit 2
A08	SD1	Data bit 1
A09	SD0	Data bit 0 (LSB)
A10	-I/O CH RDY	No Connection
A11	AEN	Address enable
A12	SA19	No Connection
A13	SA18	No Connection
A14	SA17	No Connection
A15	SA16	No Connection
A16	SA15	No Connection
A17	SA14	No Connection
A18	SA13	No Connection
A19	SA12	No Connection
A20	SA11	No Connection
A21	SA10	No Connection
A22	SA9	Address bit 9
A23	SA8	Address bit 8
A24	SA7	Address bit 7
A25	SA6	Address bit 6
A26	SA5	Address bit 5
A27	SA4	Address bit 4
A28	SA3	Address bit 3
A29	SA2	Address bit 2
A30	SA1	Address bit 1
A31	SA0	Address bit 0 (LSB)

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TABLE A-1: P1 PIN ASSIGNMENTS (continued)

PIN	MNEMONIC	SIGNAL DESCRIPTION
B01	DGND	Digital ground
B02	RESET DRV	Reset drive
B03	+5VDC	+5 volt power
B04	IRQ2	No Connection
B05	-5VDC	No Connection
B06	DRQ2	No Connection
B07	-12VDC	No Connection
B08	0WS	No Connection
B09	+12VDC	No Connection
B10	DGND	Digital ground
B11	-SMEMW	No Connection
B12	-SMEMR	No Connection
B13	-IOW	I/O write command
B14	-IOR	I/O read command
B15	-DACK3	No Connection
B16	DRQ3	No Connection
B17	-DACK1	No Connection
B18	DRQ1	No Connection
B19	-REFRESH	No Connection
B20	CLOCK	No Connection
B21	IRQ7	Interrupt request 7
B22	IRQ6	No Connection
B23	IRQ5	Interrupt request 5
B24	IRQ4	No Connection
B25	IRQ3	Interrupt request 3
B26	-DACK2	No Connection
B27	T/C	Terminal count
B28	BALE	No Connection
B29	+5VDC	+5 volt power
B30	OSC	No Connection
B31	DGND	Digital ground

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TABLE A-2: P2 PIN ASSIGNMENTS

PIN	MNEMONIC	SIGNAL DESCRIPTION
C01	-SBHE	System bus high enable
C02	LA23	No connection
C03	LA22	No connection
C04	LA21	No connection
C05	LA20	No connection
C06	LA19	No connection
C07	LA18	No connection
C08	LA17	No connection
C09	-MEMR	No connection
C10	-MEMW	No connection
C11	SD08	Data bit 8
C12	SD09	Data bit 9
C13	SD10	Data bit 10
C14	SD11	Data bit 11
C15	SD12	Data bit 12
C16	SD13	Data bit 13
C17	SD14	Data bit 14
C18	SD15	Data bit 15
D01	-MEMCS16	No connection
D02	-I/O CS16	I/O 16-bit chip select
D03	IRQ10	Interrupt request 10
D04	IRQ11	No connection
D05	IRQ12	No connection
D06	IRQ15	Interrupt request 15
D07	IRQ14	No connection
D08	-DACK0	No connection
D09	DRQ0	No connection
D10	-DACK5	DMA acknowledge 5
D11	DRQ5	DMA request 5
D12	-DACK6	DMA acknowledge 6
D13	DRQ6	DMA request 6
D14	-DACK7	DMA acknowledge 7
D15	DRQ7	DMA request 7
D16	+5VDC	+5 volt power
D17	-MASTER	No connection
D18	DGND	Digital ground

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APPENDIX B

CALIBRATION

B.1 INTRODUCTION

This appendix contains calibration procedures for the A/D and D/A sections of the DT2821 series board.

B.2 A/D CALIBRATION

Before performing an A/D calibration on the DT2821 series board, the computer's top cover must be removed.

B.2.1 ASSUMPTIONS

1. Calibration is done on channel 0 with all other channels returned to analog ground.
2. The input cable is less than 3 meters (10 feet) long.
3. Software is available to provide continuous readings of Channel 0 and display them on the IBM Personal Computer AT's monitor.

B.2.2 EQUIPMENT REQUIRED

1. Precision voltage source, Electronic Development Corporation model 501J, or equivalent
2. Miscellaneous cables and connectors
3. Flat bladed screwdriver

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IMPORTANT

Always switch the computer power off before removing or installing a DT2821 series board. Damage to the DT2821 series board can result if the power is not turned off.

B.2.3 SINGLE-ENDED CONNECTIONS (SE)

For single-ended operation, calibration is done on Channel 0 with all other channels connected to analog ground. Figures B-1 and B-2 show the calibration setup. In SE operation, all analog inputs are referenced to a single ground potential.

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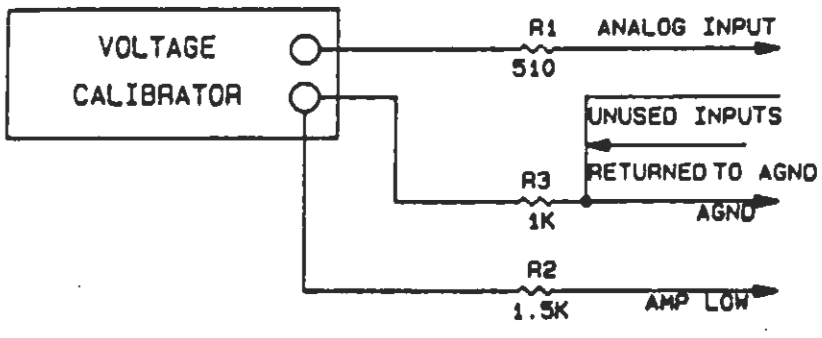


FIGURE B-1: SE CONNECTIONS (EXCEPT DT2828)

- R1 is used for additional input protection.
- R2 is used to balance the amplifier input and represents 1 kilohm for the multiplexer plus 510 ohms for the input protection resistor R1.
- R3 isolates the calibrator lo signal (CH 0 RET) from analog ground.

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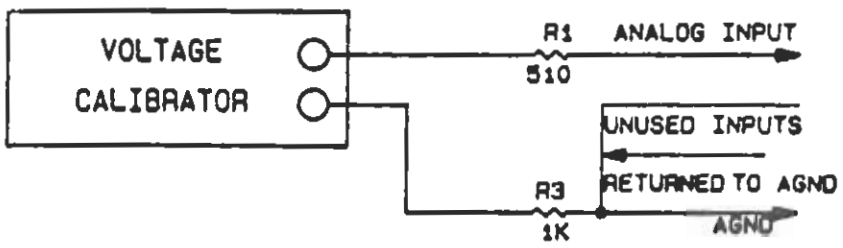


FIGURE B-2: DT2828 SE CONNECTIONS

- R1 is used for additional input protection.
- R2 is used to balance the amplifier input and represents 1 kilohm for the multiplexer plus 510 ohms for the input protection resistor R1.

B.2.4 DIFFERENTIAL INPUT CONNECTIONS (DI)

In differential input operation, each input has a high (CH 0) and a low (CH 0 RETURN) connection. The measurement taken is the difference between these two potentials, thereby rejecting any noise common to both signals.

With non-isolated systems, analog ground of the board must be connected to the low (return) side of the input device. If the system is isolated, then a return path for bias current must be provided to analog ground of the DT2821 series board (J1 pin

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17). Isolation of the grounds is accomplished by using a 1 kilohm to 100 kilohm resistor to connect the return path to analog ground. Direct connection is discouraged due to the possibility of creating large ground currents that could harm the system. Stray capacitance and non-isolated grounds can cause large ground currents to flow making the accuracy of the board and the system reliability not meet specifications. Figure B-3 shows the calibration setup.

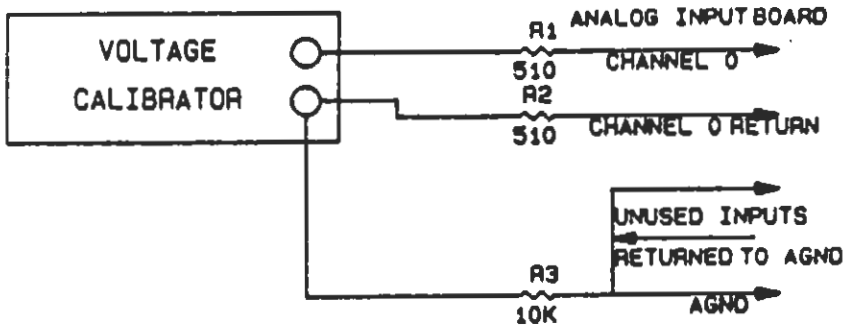


FIGURE B-3: DI CONNECTIONS

1. R1 and R2 are used for additional input protection
2. R3 is used to reference the inputs to analog common.

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B.2.5 CALIBRATION

1. Allow one hour for the entire system to warm up and stabilize before calibration.
2. The calibration must be done at a gain of one first.
3. When adjusting the potentiometers (pots), center the code on the proper value by noting where the adjacent codes are. That is, mechanically center the pot between the position that yields the desired value plus 1 LSB and the desired value minus 1 LSB.
4. A second calibration must be done to eliminate interaction between the Zero and Full Scale (Offset) adjustments.
5. On a ±10 volt input, the range is 20 volts (Range equals the upper input voltage minus the lower input voltage. For ±10V, that is +10V - (-10V) = 20V range).
6. Refer to the following sections for the calibration procedure for your specific board.

B.2.5.1 DT2821, DT2824-PGH, DT2824-PGL, AND DT2825

The DT2821, DT2824-PGH, DT2824-PGL, and DT2825 can be configured for single-ended or differential input, as well as unipolar or bipolar. Use the appropriate input connections. Figures B-1 and B-3 show the connections for SE and DI signals. The DT2821 is calibrated by inputting -full scale + 1 LSB, then +full scale - 2 LSBs, and then zero (at a gain of 8 for DT2821 and 500 for DT2825).

TABLE B-1: CALIBRATION TABLE--DT2821, DT2824-PGH, DT2824-PGL, and DT2825

INPUT RANGE	-FULL SCALE + 1 LSB	+FULL SCALE - 2 LSB
±10V	-9.9951V	+9.9902V
0 to 10V	-0.00244V	+9.9951V

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TABLE B-2: CODING TABLE--DT2821, DT2824-PGH DT2824-PGL, AND DT2825

CODING	-FULL SCALE + 1 LSB				+FULL SCALE - 2 LSB			
Binary	0000	0000	0000	0001	0000	1111	1111	1110
(hex)	0	0	0	1	0	F	F	E
Offset Binary	0000	0000	0000	0001	0000	1111	1111	1110
(hex)	0	0	0	1	0	F	F	E
Two's Complement	0000	1000	0000	0001	0000	0111	1111	1110
(hex)	0	8	0	1	0	7	F	E
Two's Complement[1]	1111	1000	0000	0001	1111	0111	1111	1110
(hex)	F	8	0	1	F	7	F	E

1. Sign extension. Bits 12, 13, 14, and 15 of the ADDAT Register track the MSB (bit 11). See Table 3-7 for the sign extension jumper configuration.

B.2.5.1.1 -Full Scale + 1 LSB

Apply the appropriate voltage input (see Table B-1) to channel 0 and read the ADDAT Register repetitively. Adjust the ZERO pot (on the top of the module) until the proper code (see Table B-2) is read from the ADDAT Register.

B.2.5.1.2 +Full Scale - 2 LSBs

Apply the appropriate voltage input (see Table B-1) to channel 0 and read the ADDAT Register repetitively. Adjust the FULL SCALE pot (on the top of the module) until the proper code (see Table B-2) is read from the ADDAT Register.

B.2.5.1.3 Zero

Apply zero volts to channel 0, with a gain of 8 for DT2821 and 500 for DT2825 (bits 12 and 13 of the ADCSR both set) and read the ADDAT Register repetitively. Adjust the PG ZERO pot (on the top of the module) until the proper code (all zeros) is read from the ADDAT Register. In unipolar mode, the ADDAT Register does not reflect a negative reading, but continues to display all zeros. To be certain

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that the A/D converter is calibrated properly in unipolar mode, apply +0.00244V, which at a gain of 8 should produce a reading of 0000 0000 1000 (008 hex). Repeat the last three steps if +0.00244V does not produce 008 (hex).

B.2.5.2 DT2821-F-16SE, DT2821-F-8DI, DT2821-G-16SE, AND DT2821-G-8DI

The DT2821-F-16SE, DT2821-F-8DI, DT2821-F-16SE, and DT2821-F-8DI can be configured as either unipolar or bipolar. Use the appropriate input hook-up. Figure B-1 shows the connection for SE signals and Figure B-3 shows the connection for DI signals. These boards are calibrated by inputting -full scale + 1 LSB, then +full scale - 2 LSBs, and then zero (at a gain of 8).

TABLE B-3: CALIBRATION TABLE--
DT2821-F-16SE, DT2821-F-8DI,
DT2821-G-16SE, DT2821-G-8DI

INPUT RANGE	-FULL SCALE + 1 LSB	+FULL SCALE - 2 LSB
±10V	-9.9951V	+9.9902V
0 to 10V	-0.00244V	+9.9951V

TABLE B-4: CODING TABLE--
DT2821-F-16SE, DT2821-F-8DI,
DT2821-G-16SE, AND DT2821-G-8DI

CODING	-FULL SCALE + 1 LSB				+FULL SCALE - 2 LSB			
Binary	0000	0000	0000	0001	0000	1111	1111	1110
(hex)	0	0	0	1	0	F	F	E
Offset Binary	0000	0000	0000	0001	0000	1111	1111	1110
(hex)	0	0	0	1	0	F	F	E
Two's Complement	0000	1000	0000	0001	0000	0111	1111	1110
(hex)	0	8	0	1	0	7	F	E
Two's[1] Complement	1111	1000	0000	0001	1111	0111	1111	1110
(hex)	F	8	0	1	F	7	F	E

1. Sign extension. Bits 12, 13, 14, and 15 of the ADDAT Register track the MSB (bit 11).

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B.2.5.2.1 -Full Scale + 1 LSB

Apply the appropriate voltage input (see Table B-3) to channel 0 and read the ADDAT Register repetitively. Adjust the ZERO pot (on the top of the module) until the proper code (see Table B-4) is read from the ADDAT Register.

B.2.5.2.2 +Full Scale - 2 LSBs

Apply the appropriate voltage input (see Table B-3) to channel 0 and read the ADDAT Register repetitively. Adjust the FULL SCALE pot (on the top of the module) until the proper code (see Table B-4) is read from the ADDAT Register.

B.2.5.2.3 Zero (At A Gain Of 8)

Apply zero volts to channel 0, with a gain of 8 (bits 12 and 13 of the ADCSR both set) and read the ADDAT Register repetitively. Adjust the PG ZERO pot (on the top of the module) until the proper code (all zeros) is read from the ADDAT Register. In unipolar mode, the ADDAT Register does not reflect a negative reading, but continues to display all zeros. To be certain that the A/D converter is calibrated properly when in unipolar mode, apply +0.00244V, which at a gain of 8 should produce a reading of 0000 0000 1000 (008 hex). Repeat the last three steps if +0.00244V does not produce 008 (hex).

B.2.5.3 DT2823 AND DT2827

The DT2823 and DT2827 can only be configured as bipolar (two's complement coding), differential input. Use the appropriate input hook-up as shown in Figure B-3. The DT2823 and DT2827 are calibrated by inputting -full scale + 1 LSB, then +full scale - 2 LSBs.

TABLE B-5: CALIBRATION TABLE--DT2823 AND DT2827

INPUT RANGE	-FULL SCALE + 1 LSB	+FULL SCALE - 2 LSB
±10V	-9.99969V	+9.99939V

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TABLE B-6: CODING TABLE--DT2823 AND DT2827

CODING	-FULL SCALE + 1 LSB	+FULL SCALE - 2 LSB
Two's Complement (hex)	1000 0000 0000 0001 8 0 0 1	0111 1111 1111 1110 7 F F E

B.2.5.3.1 -Full Scale + 1 LSB

Apply the appropriate voltage input (see Table B-5) to channel 0 and read the ADDAT Register repetitively. Adjust the ZERO pot (on the top of the module) until the proper code (see Table B-6) is read from the ADDAT Register.

B.2.5.3.2 +Full Scale - 2 LSBs

Apply the appropriate voltage input (see Table B-5) to channel 0 and read the ADDAT Register repetitively. Adjust the FULL SCALE pot (on the top of the module) until the proper code (see Table B-6) is read from the ADDAT Register.

B.2.5.4 DT2828

The DT2828 can be configured as bipolar or unipolar. Use the appropriate input connection for SE signals as shown in Figure B-2. The DT2828 is calibrated by inputting -full scale + 1 LSB, then +full scale - 2 LSBs.

TABLE B-7: CALIBRATION TABLE--DT2828

INPUT RANGE	-FULL SCALE + 1 LSB	+FULL SCALE - 2 LSB
±10V	-9.9951V	+9.9902V
0 to 10V	-0.00244V	+9.9951V

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TABLE B-8: CODING TABLE--DT2828

CODING	-FULL SCALE + 1 LSB				+FULL SCALE - 2 LSB			
Binary	0000	0000	0000	0001	0000	1111	1111	1110
(hex)	0	0	0	1	0	F	F	E
Offset Binary	0000	0000	0000	0001	0000	1111	1111	1110
(hex)	0	0	0	1	0	F	F	E
Two's Complement	0000	1000	0000	0001	0000	0111	1111	1110
(hex)	0	8	0	1	0	7	F	E
Two's[1] Complement	1111	1000	0000	0001	1111	0111	1111	1110
(hex)	F	8	0	1	F	7	F	E

1. Sign extension. Bits 12, 13, 14, and 15 of the ADDAT Register track the MSB (bit 11). See Table 3-7 for the sign extension jumper configuration.

B.2.5.4.1 -Full Scale + 1 LSB

Apply the appropriate voltage input (see Table B-7) to channel 0 and read the ADDAT Register repetitively. Adjust the ZERO pot (on the top of the module) until the proper code (see Table B-8) is read from the ADDAT Register.

B.2.5.4.2 +Full Scale - 2 LSBs

Apply the appropriate voltage input (see Table B-7) to channel 0 and read the ADDAT Register repetitively. Adjust the FULL SCALE pot (on the top of the module) until the proper code (see Table B-8) is read from the ADDAT Register.

B.3 D/A CALIBRATION

NOTE

This section does not apply to the DT2824-PGH and DT2824-PGL models.

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Before performing a D/A calibration on the DT2821 series board, the computer's top cover must be removed, if it's not already off.

B.3.1 ASSUMPTIONS

1. The output cable is less than 3 meters long (10 feet).
2. The output load impedance is not less than 5 kilohms.
3. Software is available which can program the D/A converter with the appropriate output codes (analog data values).

B.3.2 EQUIPMENT REQUIRED

1. Precision voltage meter, accurate to 4½ digits
2. Oscilloscope (for the optional pedestal calibration)
3. Miscellaneous cables and connectors
4. Flat-bladed screwdriver

IMPORTANT

Always switch the computer power off before removing or installing a DT2821 series board. Damage to the DT2821 series board can result if the power is not turned off.

B.3.3 CALIBRATION

1. Allow one hour for the entire system to warm up and stabilize before calibration.
2. Select the 10V scale on the voltmeter and do not change it during the calibration procedure.
3. Connect the selected DAC output (both DACs

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must be calibrated, one at a time) to the positive input of the voltmeter and connect the DAC GND output to the negative input of the voltmeter (see Figure B-4).

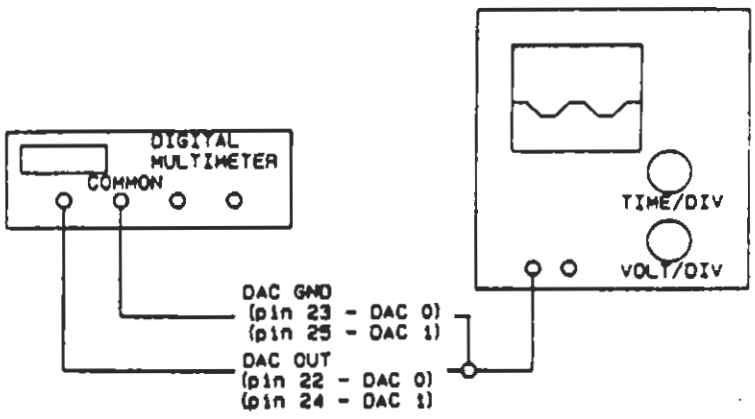


FIGURE B-4: DAC CONNECTION

B.3.3.1 12-bit DACs

This calibration applies to all models except the DT2823.

B.3.3.1.1 Offset Adjustment

Write the proper OFFSET code (see Table B-9) to the D/A and adjust R7 (DAC 0) or R3 (DAC 1) until the voltmeter produces the correct value.

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TABLE B-9: 12-BIT DAC OFFSET CODES

RANGE	ANALOG DATA VALUE	VOLTAGE
±10V	0000 0000 0000 0000	-10.000V
(hex)	0 0 0 0	
±5V	0000 0000 0000 0000	-5.0000V
(hex)	0 0 0 0	
±2.5V	0000 0000 0000 0000	-2.5000V
(hex)	0 0 0 0	
0 to +10V	0000 0000 0000 0000	0.0000V
(hex)	0 0 0 0	
0 to +5V	0000 0000 0000 0000	0.0000V
(hex)	0 0 0 0	

B.3.3.1.2 Full Scale Adjustment

Write the proper FULL SCALE code (see Table B-10) to the D/A and adjust R10 (DAC 0) or R2 (DAC 1) until the voltmeter produces the correct value.

TABLE B-10: 12-BIT DAC FULL SCALE CODES

RANGE	ANALOG DATA VALUE	VOLTAGE
±10V	0000 1111 1111 1111	9.9951V
(hex)	0 F F F	
±5V	0000 1111 1111 1111	4.9976V
(hex)	0 F F F	
±2.5V	0000 1111 1111 1111	2.4988V
(hex)	0 F F F	
0 to +10V	0000 1111 1111 1111	9.9976V
(hex)	0 F F F	
0 to +5V	0000 1111 1111 1111	4.9988V
(hex)	0 F F F	

B.3.3.2 16-bit DACs

This calibration applies to model DT2823 only.

B.3.3.2.1 Offset Adjustment

Write the proper OFFSET code (see Table B-11) to the D/A and adjust R6 (DAC 0) or R2 (DAC 1) so that the output voltage is 0.0000 ±0.0003 volts.

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TABLE B-11: 16-BIT DAC OFFSET CODE

ANALOG DATA VALUE	VOLTAGE
1000 0000 0000 0000	-10.000V

B.3.3.2.2 Full Scale Adjustment

Write the FULL SCALE code (FFFF) to the D/A and adjust R7 (DAC 0) or R2 (DAC 1) so that the output voltage is +9.0007 ±0.0003 volts.

TABLE B-12: 16-BIT DAC FULL SCALE CODE

ANALOG DATA VALUE	VOLTAGE
0111 1111 1111 1111	9.99969V

B.3.3.3 Pedestal Adjustment

Both DAC outputs are updated simultaneously by a clock (external, internal, or single convert). The output of the DACs are deglitched through a sample and hold output stage that switches into hold mode for 700 nanoseconds, allowing the glitch created by the DAC current sources to die out while the output is holding the last value output. While the sample and hold is in hold mode, it can exhibit a dc offset introduced to the output of the sample and hold (pedestal). This offset is caused by charge imbalances in the output stage and must be trimmed out by adjusting the variable capacitors on the DT2821 series board.

Refer to Figure B-5 for a diagram of the pedestal offset as seen on an oscilloscope.

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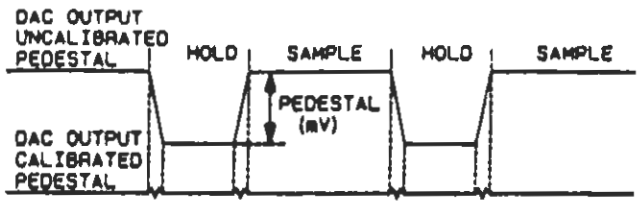


FIGURE B-5: PEDESTAL ADJUSTMENT

NOTE

The pedestal adjustment is done at the factory and should not need to be readjusted. The following instructions are for reference only, or in case the variable capacitors changed setting in transit.

1. Set the DACs in programmed I/O dual channel mode.

2. Set the oscilloscope on bandwidth limited, 10mV per division.

3. Repeatedly write data value 0000 (hex) for unipolar ranges, or 0800 (hex) for bipolar ranges (8000 for 16-bit DACs). You must continuously write and convert to get the DACs to switch from sample to hold modes.

4. Look at the DAC output on an oscilloscope and trim C6 (for the X DAC) and C3 (for the Y DAC) for a maximum flat output. The DACs are trimmed independently of each other.

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APPENDIX C

TROUBLESHOOTING AND FACTORY SERVICE

C.1 INTRODUCTION

If there is difficulty with the DT2821 series board or the screw terminal panel, consult the following checklist before calling Data Translation.

CHECK THESE FIRST:

1. Check that the DT2821 series board is firmly seated in the IBM Personal Computer AT connectors. The DT2821 series board is powered from the IBM Personal Computer AT, and transfers all data and instructions over the IBM Personal Computer AT bus.

2. Check that all ICs are firmly seated in their sockets.

3. Check the +5V power supply. It should be between +4.75V and +5.25V.

4. Check the voltage in and out of the dc/dc converter on the DT2821. There should be +5V in and ±15V out.

5. Check that the screw terminal cable assembly, or whatever user-supplied cable assembly is used, is connected securely to J1.

6. Check the DT2821 series board jumper configuration. The jumper functions are described in Chapter 3.

7. Check to make sure no components are making contact to an adjacent board.

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C.2 SYMPTOMS AND SOLUTIONS

The following sections list specific problems and solutions. If, after trying these solutions, the DT2821 series board is still not functioning properly, call the Customer Service department and get a Return Material Authorization (RMA) number.

Check all the items listed under the Introduction first.

C.2.1 NO BOARD RESPONSE

- Check the board's base address jumpers.
- Clean the board connector fingers with a soft pencil eraser.

C.2.2 DIGITAL OUTPUT CODE ALL ONES (OR ALL ZEROS)

- Check for floating inputs (see the section on Floating Inputs).
- Make sure that the input is not greater than the range that the A/D is on.
- Make sure that none of the other inputs is above the power supply voltage (±15V).
- In unipolar mode, check for a negative voltage input.

C.2.3 FIRST READING ON A CHANNEL IS INCORRECT

Input settling time is budgeted from one linear region to another. If the sample and hold is saturated due to overvoltage on an open channel, the first reading on a valid channel could be in error.

- Check for floating inputs (see the section on Floating Inputs).
- Check to make sure the input cable is not over 3 meters (10 feet) in length.
- Check to make sure the source impedance is not over 1 kilohm.

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C.2.4 ZERO WILL NOT CALIBRATE

The total adjustment range of the ZERO pot on the module is approximately 30 counts (see the Data Coding Tables in Appendix D). If there are offsets in the system, such as bridge imbalances, they usually cannot be removed with the ZERO pot on the module.

C.2.5 FULL SCALE WILL NOT CALIBRATE

The total adjustment range of the FULL SCALE pot on the module is approximately 30 counts (see the Data Coding Tables in Appendix D). If there are other gain errors in the system, they usually cannot be adjusted out with the FULL SCALE pot on the module.

C.2.6 THE READINGS ARE NOISY

- All cables must be routed away from switching power supplies and digital signals.
- In a high noise environment, the inputs should be differential with shielded twisted pair cable. The shield should only be connected at one end.
- RC filters can be added at the inputs to remove high frequency noise pickup.
- Digital averaging of the data can be done simply by adding 16 12-bit A/D conversions and then shifting right 4 times (divide by 16). This is especially useful to minimize the rms noise in high gain applications.

C.2.7 FLOATING INPUTS

Floating inputs are those signals that do not have a reference to analog ground of the DT2821 series board.

With single-ended inputs, it is recommended that the inputs be isolated from earth ground. All the signal commons then would be connected separately to analog common of the board (for example, SGND on the DT707).

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With differential inputs, it is necessary to reference the signal's return path to analog ground of the system. If the signal is not referenced back to analog common, leakage currents on the input drives the signal out of the common mode voltage range (±11V) thereby saturating the amplifier. This reference should not be a direct connection, but should be some impedance from 1 kilohm to 100 kilohms. Refer to the calibration procedure, and specifically the section on the differential connections for more information.

IMPORTANT

Unused differential inputs must be returned to analog common.

C.3 RMA NUMBER

If you determine that factory service is necessary, call the Customer Service department at Data Translation [(508) 481-3700] for a Return Material Authorization (RMA) number. All return shipments to Data Translation must be marked with RMA numbers.

Wrap the DT2821 series board in the original shipping materials, if available and in good condition. Be careful to wrap the board in an electrically conductive plastic, and to handle it with ground protection. A static electric discharge can destroy components on the DT2821 series board. Ship the board to the following address:

Customer Service
Data Translation, Inc.
100 Locke Drive
Marlboro, MA, USA 01752-1192

The Data Translation Customer Service can be reached by:

Telephone: (508)481-3700
Telex: 951646 (DATATRANS MARO)
Easylink 62825999

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APPENDIX D

CODING TABLES

D.1 INTRODUCTION

The DT2821 series board's analog-to-digital (A/D) converter can convert the analog voltage at any one of its input channels into a binary code at its output. The digital-to-analog converters (DACs), conversely, convert binary codes into analog voltages.

In this manual, the binary code representation of an analog voltage is called an Analog Data Value (ADV). Analog Data Values are encoded in straight binary if they represent voltages in a unipolar range (0 to +10V is a unipolar range). On 12-bit boards, they are encoded in either two's complement or offset binary if they represent voltages in a bipolar range (±10V is a bipolar range). On 16-bit boards, Analog Data Values are encoded in two's complement coding and they represent voltages in a bipolar range.

To convert an Analog Data Value into a voltage value, you need to know the number of codes (NOC) used by the A/D or D/A converter, as well as the high (PFS) and the low (MFS) voltage values of the analog range. NOC is determined by raising the number 2 to the power n, where n is the number of bits of resolution in the analog converter. Thus, for a 12-bit converter NOC equals 4096 and for a 16-bit converter, 65536. PFS is plus full scale, which is the highest voltage of a given range (for example, +10V on a ±10V range); MFS is minus full scale, which is the lowest voltage of a given bipolar (for example, -10V on the ±10V range). Zero is the lowest value for unipolar ranges.

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NOTE

The highest possible value is actually one LSB less that PFS. However, PFS is the correct number to use in the equations that follow.

To calculate the input voltage detected by an A/D converter which uses binary or offset binary coding, use the equation in Figure D-1. To calculate the input voltage to an A/D converter which uses two's complement coding use the equation in Figure D-2.

To determine the Analog Data Value that produces a desired output voltage from a D/A converter which uses binary or offset binary coding (all the DACs on the DT2821 series boards), use the equation in Figure D-3. Two's complement coding is not available on the DACs.

$$\text{Analog Voltage} = \left[\text{ADV} \times \frac{(\text{PFS} - \text{MFS})}{\text{NOC}} \right] + (\text{MFS})$$

FIGURE D-1: CALCULATING THE INPUT VOLTAGE TO AN A/D CONVERTER USING BINARY OR OFFSET BINARY CODING

$$\text{Analog Voltage} = \text{ADV} \times \frac{(\text{PFS} - \text{MFS})}{\text{NOC}}$$

FIGURE D-2: CALCULATING THE INPUT VOLTAGE TO AN A/D CONVERTER USING TWO'S COMPLEMENT CODING

$$\text{ADV} = (\text{Analog Voltage} - \text{MFS}) \times \frac{\text{NOC}}{(\text{PFS} - \text{MFS})}$$

FIGURE D-3: CALCULATING THE ANALOG DATA VALUE TO A D/A CONVERTER USING BINARY OR OFFSET BINARY CODING

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The balance of this appendix consists of a series of tables indicating Analog Data Values for key points in the ranges of the A/D and D/A sections of DT2821 series boards. The tables list analog voltages in one column and the corresponding binary code in another. For convenience the binary codes are represented as hexadecimal numbers.

Tables D-1, D-2, D-3, and D-4 are unipolar and bipolar coding tables for the A/D ranges found on the DT2821 series boards. Tables D-1 and D-2 cover the 12-bit bipolar coding schemes (offset binary and two's complement). Table D-3 covers the 12-bit unipolar coding table, and Table D-4 covers the 16-bit bipolar coding table.

Tables D-5 and D-6 are the unipolar and bipolar coding tables for the D/A ranges on the DT2821 series boards. Table D-5 covers 12-bit bipolar coding and Table D-6 covers 12-bit unipolar coding.

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TABLE D-1: 12-BIT A/D BIPOLAR CODING--OFFSET BINARY

% OF FULL SCALE	DIGITAL CODING	ANALOG VOLTAGES GAIN OF 1	GAIN OF 2	GAIN OF 4	GAIN OF 8
+FS - 1 LSB	0FFF	+9.9951V	+4.9976V	+2.4988V	+1.2494V
+FS - 2 LSBS	0FFE	+9.9902V	+4.9951V	+2.4976V	+1.2488V
+½ FS	0C00	+5.0000V	+2.5000V	+1.2500V	+0.6250V
+1 LSB	0801	+4.8828mV	+2.4414mV	+1.2207mV	+610.35µV
0	0800	0.0000V	0.0000V	0.0000V	0.0000V
-1 LSB	07FF	-4.8828mV	-2.4414mV	-1.2207mV	-610.35µV
-½ FS	0400	-5.0000V	-2.5000V	-1.2500V	-0.6250V
-FS + 1 LSB	0001	-9.9951V	-4.9976V	-2.4988V	-1.2494V
-FS	0000	-10.0000V	-5.0000V	-2.5000V	-1.2500V

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12-BIT A/D BIPOLAR CODING--TWO'S COMPLEMENT

TABLE D-2: 12-BIT A/D BIPOLAR CODING--TWO'S COMPLEMENT

% OF FULL SCALE	DIGITAL CODING	ANALOG VOLTAGES GAIN OF 1	GAIN OF 2	GAIN OF 4	GAIN OF 8
+FS - 1 LSB	07FF	+9.9951V	+4.9976V	+2.4988V	+1.2494V
+FS - 2 LSBS	07FE	+9.9902V	+4.9951V	+2.4976V	+1.2488V
+¼ FS	0400	+5.0000V	+2.5000V	+1.2500V	+0.6250V
+1 LSB	0001	+4.8828mV	+2.4414mV	+1.2207mV	+610.35μV
0	0000	0.0000V	0.0000V	0.0000V	0.0000V
-1 LSB	0FFF	-4.8828mV	-2.4414mV	-1.2207mV	-610.35μV
-¼ FS	0D00	-5.0000V	-2.5000V	-1.2500V	-0.6250V
-FS + 1 LSB	0801	-9.9951V	-4.9976V	-2.4988V	-1.2494V
-FS	0800	-10.0000V	-5.0000V	-2.5000V	-1.2500V

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TABLE D-3: 12-BIT A/D UNIPOLAR CODING--BINARY

% OF FULL SCALE	DIGITAL CODING	ANALOG VOLTAGES GAIN OF 1	GAIN OF 2	GAIN OF 4	GAIN OF 8
+FS - 1 LSB	0FFF	+9.9976V	+4.9988V	+2.4994V	+1.2497V
+FS - 2 LSBS	0FFE	+9.9951V	+4.9976V	+2.4988V	+1.2494V
+3/4 FS	0C00	+7.5000V	+3.7500V	+1.8750V	+0.9375V
+½ FS	0800	+5.0000V	+2.5000V	+1.2500V	+0.6250V
+¼ FS	0400	+2.5000V	+1.2500V	+.62500V	+0.3125V
0 + 1 LSB	0001	+2.4414mV	+1.2207mV	+610.36μV	+305.17μV
0	0000	0.0000V	0.0000V	0.0000V	0.0000V

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TABLE D-4: 16-BIT A/D BIPOLAR CODING
--TWO'S COMPLEMENT

% OF FULL SCALE	DIGITAL CODING	ANALOG VOLTAGES GAIN OF 1
+FS - 1 LSB	7FFF	+9.999695V
+FS - 2 LSBS	7FFE	+9.999390V
+½ FS	4000	+5.000000V
+1 LSB	0001	+305.1758μV
0	0000	0.000000V
-1 LSB	FFFF	-305.1758μV
-½ FS	C000	-5.000000V
-FS + 1 LSB	8001	-9.999695V
-FS	8000	-10.00000V

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TABLE D-5: 12-BIT D/A BIPOLAR CODING--OFFSET BINARY

% OF FULL SCALE	DIGITAL CODING	D/A RANGE +/-10V	D/A RANGE +/-5V	+/-2.5V
+FS - 1 LSB	0FFF	+9.9951V	+4.9976V	+2.4988V
+FS - 2 LSBS	0FFE	+9.9902V	+4.9951V	+2.4976V
+¼ FS	0C00	+5.0000V	+2.5000V	+1.2500V
+1 LSB	0801	+4.8828mV	+2.4414mV	+1.2207mV
0	0800	0.0000V	0.0000V	0.0000V
-1 LSB	07FF	-4.8828mV	-2.4414mV	-1.2207mV
-¼ FS	0400	-5.0000V	-2.5000V	-1.2500V
-FS + 1 LSB	0001	-9.9951V	-4.9976V	-2.4988V
-FS	0000	-10.0000V	-5.0000V	-2.5000V

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TABLE D-6: 12-BIT D/A UNIPOLAR CODING--BINARY

% OF FULL SCALE	DIGITAL CODING	D/A RANGE	
		0 TO +10V	0 TO +5V
+FS - 1 LSB	0FFF	+9.9976V	+4.9988V
+FS - 2 LSBS	0FFE	+9.9951V	+4.9976V
+3/4 FS	0C00	+7.5000V	+3.7500V
+½ FS	0800	+5.0000V	+2.5000V
+¼ FS	0400	+2.5000V	+1.2500V
0 + 1 LSB	0001	+2.4414mV	+1.2207mV
0	0000	0.0000V	0.0000V

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TABLE D-7: 16-BIT D/A BIPOLAR CODING--OFFSET BINARY

% OF FULL SCALE	DIGITAL CODING	±10V	D/A RANGE ±5V	±2.5V
+FS - 1 LSB	FFFF	+9.999695V	+4.999848V	+2.499924V
+FS - 2 LSB'S	FFFE	+9.999390V	+4.999695V	+2.499848V
+1/2 FS	C000	+5.000000V	+2.500000V	+1.250000V
+1 LSB	8001	+305.17578uV	+152.58789uV	+76.293945uV
0	8000	0.000000V	0.000000V	0.000000V
-1 LSB	7FFF	-305.17578uV	-152.58789uV	-76.293945uV
-1/2 FS	4000	-5.000000V	-2.500000V	-1.250000V
-FS + 1 LSB	0001	+9.999695V	+4.999848V	+2.499924V
-FS	0000	-10.000000V	-5.000000V	-2.500000V

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TABLE D-8: 16-BIT D/A BIPOLAR CODING--TWO'S COMPLEMENT

% OF FULL SCALE	DIGITAL CODING	±10V	D/A RANGE ±5V	±2.5V
+FS - 1 LSB	7FFF	+9.999695V	+4.999848V	+2.499724V
+FS - 2 LSB'S	7FFE	+9.999390V	+4.999695V	+2.499848V
+1/2 FS	4000	+5.000000V	+2.500000V	+1.250000V
+1 LSB	0001	+305.17578uV	+152.58789uV	+76.293945uV
0	0000	0.000000V	0.000000V	0.000000V
-1 LSB	FFFF	-305.17578uV	-152.58789uV	-76.293945uV
-1/2 FS	C000	-5.000000V	-2.500000V	-1.250000V
-FS + 1 LSB	8001	+9.999695V	+4.999848V	+2.499924V
-FS	8000	-10.000000V	-5.000000V	-2.500000V

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TABLE D-9: 16-BIT D/A UNIPOLAR CODING--BINARY

% OF FULL SCALE	DIGITAL CODING	D/A RANGE 0 TO +10V	0 TO +5V
+FS - 1 LSB	FFFF	+9.999847V	+4.999924V
+FS - 2 LSB'S	FFFE	+9.996894V	+4.998447V
+3/4 FS	C000	+7.500000V	+3.750000V
+1/2 FS	8000	+5.000000V	+2.500000V
+1/4 FS	4000	+2.500000V	+1.250000V
0 + 1 LSB	0001	+152.58789uV	+76.293945uV
0	0000	0.000000V	0.000000V

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APPENDIX E

DT707 AND DT752 SCREW TERMINAL PANELS

E.1 INTRODUCTION

The DT707 screw terminal panel is an accessory product which permits all user connections (A/D, D/A, digital I/O, external trigger, and external clock) to the DT2821 series board to be made on screw terminals. The DT752 is identical to the DT707 except that the analog input connections are not made on the screw terminal panel. The DT752 accommodates D/A, digital I/O, external trigger, and external clock connections, but directs the DT2821 series board's analog input connections to a separate 20-pin connector. This 20-pin connector is intended to accommodate signal conditioning products, such as the Data Translation DT709-S or DT709-Y signal conditioning board, or the Data Translation DT6700 series of signal conditioning components.

Both the DT707 and the DT752 provide screw terminals for most of the DT2821 series board's input and output signals. Screw terminal connections are easier to make and to change than are solder connections. The DT707 or DT752 plugs into connector J1 on the DT2821 series board through an integral one meter ribbon cable. Each screw terminal panel has rubber feet for horizontal table-top mounting.

The DT707 can accommodate the shunting resistors required to operate the DT2821 series board with current loop inputs (0 to 20mA).

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E.2 SPECIFICATIONS

These specifications are typical at +25°C and standard voltages, unless otherwise noted.

GENERAL SPECIFICATIONS, DT707 AND DT752

Outline Dimensions:
5.20"H X 8.75"W X 0.875"D
(13.21 X 22.23 X 2.22 cm)

Weight:
12.5 ounces
(355 grams)

Screw Terminal:
The screw terminal panel consists of 80 barrier strip connections in four sections of 20 connections each

Barrier Strip Screw Size:
6-32 Screws

Barrier Strip Screw Material:
Magnum

Barrier Strip Material:
Polyester, UL grade, 94V-0 polypropylene

Acceptable Wire Size:
18 to 11 AWG

CURRENT LOOP OPERATION, DT707 ONLY

Resistor: Supplied by user

Resistor Value:
250 ohms (0 to 20 mA range)

Resistor Tolerance:
±0.02% or better

Resistor Power Dissipation:
¼watt

Resistor Temperature Coefficient:
±15 ppm/°C or better

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E.3 USING THE DT707

The function of each screw terminal on the DT707 is indicated directly on the board's silkscreen. The silkscreen for the DT707 is reproduced in the board's assembly drawing, located in Appendix F.

Connections for the D/A, Digital I/O, and External Clock subsystems, and those for the External Trigger, are simply the DT2821 series board's J1 pins brought out to screw terminal connectors. The various signals on these connectors are described in Chapter 4.

The DT707 provides facilities for accommodating several types of A/D inputs. Jumpers and blank circuit pads are provided to facilitate the use of the DT2821 series board's A/D subsystem with:

- Differential inputs
- Single-ended inputs
- 0 to 20mA current-loop inputs

The following sections describe the use of the DT707 with these types of inputs.

E.3.1 DT707 WITH DIFFERENTIAL INPUTS

Whenever differential inputs are used, some external return path must be made between channel X RET (the low or return side of any differential analog input channel) and Analog Ground. This is accomplished easily on the DT707 by installing 10 kilohm, 0.25 watt resistors at resistor location R2, R3, R6, R7, R10, R11, R14, and R15. These resistors are user-supplied.

E.3.2 DT707 WITH SINGLE-ENDED INPUTS

Single-ended signals have a common return path at Analog Ground voltage potential. The DT707 connects Signal Ground to Analog Ground. Connecting single-ended input signals consists of hooking the channel up, and making the return path connection.

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E.3.3 DT707 WITH CURRENT LOOP INPUTS

To use the DT707 with a 0 to 20mA current loop input, first make sure the DT2821 series board is jumpered for unipolar differential inputs and that a gain of two is used.

Next, install 250 ohm[1] current shunt resistors at DT707 resistor locations R1, R4, R5, R8, R9, R12, R13, and R16. The current shunts cause the A/D converter to see a 0V signal for a 0mA input, and a +5V signal for a 20mA input.

Many devices set up for current loop operation provide 4 to 20mA ranges. When the DT2821 series is used with such devices, the lower part of the converter's input range (0 to +1V) is not used. This results in some loss of resolution, and may require that the software compensate for the fact that the low end of the input range (4mA) does not produce an output code of 0000 0000 0000 0000 (binary) from the A/D converter.

E.3.4 DT707 WITH THE DT2823, DT2827, AND DT2828

The DT2823, DT2827, and DT2828 do not use all the analog input connection points on the DT707 screw terminal panel. Table E-1 shows the screws to use on the DT707 to assure that these three boards are connected properly.

---

[1] To ensure the accuracy of which the DT2821 or DT2821-DI-F's A/D converter is capable, the current shunt resistors should be precision (±0.02% or better tolerance), high stability (tempco of 12 ppm/°C, or better) resistors of at least ¼watt power dissipation.

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TABLE E-1: DT707 WITH DT2823, DT2827, AND DT2828

DT707 SCREW	CONNECTIONS DT2823	DT2827	DT2828
CH0	CH0	CH0	CH0
CH0 RET	CH0 RET	CH0 RET	AGND
CH2	CH1	CH1	CH1
CH2 RET	CH1 RET	CH1 RET	AGND
CH4	CH2	CH2	CH2
CH4 RET	CH2 RET	CH2 RET	AGND
CH6	CH3	CH3	CH3
CH6 RET	CH3 RET	CH3 RET	AGND

E.3.5 REFERENCE JUMPERS ON THE DT707

On the DT707, jumpers W3 and W4 are installed at the factory, and should be left installed for all applications discussed in this manual.

When installed, W3 connects all the screw terminal marked SGND (Signal Ground) on the DT707 to AGND (Analog Ground) on the DT2821 series board through a zero-ohm resistor. When a DT2821 series board is jumpered for single-ended inputs, W4 connects amp low (the low side of the DT2821 series board's A/D instrumentation amplifier) to AGND on the DT2821 series board. When the DT2821 series board is jumpered for differential inputs W4 has no effect.

If AGND is connected directly to an external ground, ground loops may be formed resulting in electrical noise and inaccurate data conversions. Should this be a problem, replace R17 on the DT707 with a 1 kilohm resistor. For the DT2828, R17 must be a zero ohm resistor or a jumper.

E.4 USING THE DT752

The DT752 screw terminal panel accommodates user connections for the DT2821 series board's:

- o D/A subsystem
- o Digital I/O subsystem
- o External clock
- o External trigger

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The DT752 directs analog input connections to a separate 20-pin connector. Like the DT707, the function of each screw terminal on the DT752 is indicated directly on the board's silkscreen. The silkscreen for the DT752 is the same as that for the DT707, and is reproduced in Appendix F.

Connections for the D/A subsystem, Digital I/O subsystem, external clock, and external trigger are simply the DT2821 series board's J1 pins brought out to screw terminal connectors. The various signals on these connectors are described in Chapter 4.

E.4.1 DT752 ANALOG INPUT CONNECTIONS

Even though the DT752's screw terminal panel has screws marked for analog input, there is no connection between these screw terminals and the DT2821 series board. When a DT752 is used, ALL ANALOG INPUT CONNECTIONS MUST BE MADE USING THE 20-PIN 3M CONNECTOR ATTACHED TO THE DT752. Typically, connections can be made using a Data Translation signal conditioning board, like the DT709-S, DT709-I, or the DT6700 series of boards. Connections are then made to the signal conditioning board.

Table E-2 contains the pin assignments for the DT752's 20-pin analog input connector. Note that DT752 cannot be used with differential inputs. Also, the DT2828 should not be used with the DT752 because the signal conditioning circuitry interferes with the simultaneousness of the signals and results in non-simultaneous signals at the sample and hold circuitry. Figure E-1 shows the typical connection of a DT752 to a DT2821 series board.

TABLE E-2: DT752 20-PIN CONNECTOR PIN ASSIGNMENTS

SIGNAL	PIN		SIGNAL
Channel 0	1	2	Channel 8
Channel 1	3	4	Channel 9
Channel 2	5	6	Channel 10
Channel 3	7	8	Channel 11
Channel 4	9	10	Channel 12
Channel 5	11	12	Channel 13
Channel 6	13	14	Channel 14
Channel 7	15	16	Channel 15
AGND	17	18	Amp low
+15V out	19	20	-15V out

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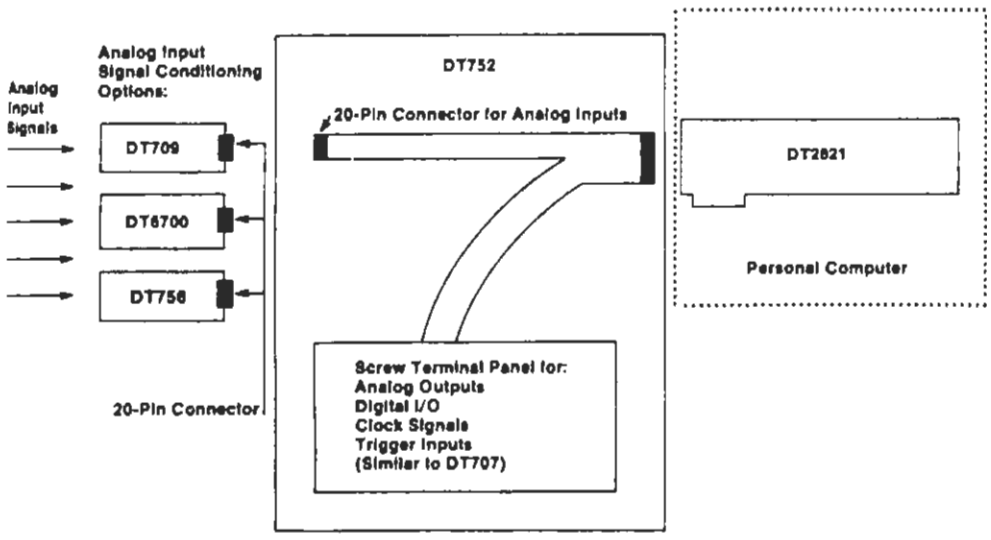


FIGURE E-1: DT752 INTERCONNECTIONS

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b. A 72-hour service plan is available. Contact factory for details.

c. If a product should fail during the warranty period, it will be repaired free of charge. For out of warranty repairs, the customer will be invoiced for repair charges.

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   2. Carefully package the product in anti-static package and ship prepaid to Data Translation. The RMA number should show on the outside of the package. Include a description of the malfunction along with the return address and telephone number of a technical contact.

b. Upon completion of the services required, an invoice is issued stating charges, when applicable, and work completed. A packing slip is enclosed in the return shipment. Data Translation will prepay return shipment via UPS for all continental USA returns. For returns requested via air freight, material will be sent "Air Collect".

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