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# *READ THIS FIRST*

Before Using the DT2919

RTF-09111-A

# Notes for the DT2919

## Introduction

This document contains replacement pages for the *DT2919 User Manual* (UM-08888-A).

## Where to Get Help

If you have any problems installing or using the DT2919, contact Data Translation's **Technical Support Department** at **(508) 481-3700.**

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## Corrections to User Manual

Tables 1, 3, 14, and 15 in the *DT2919 User Manual* incorrectly list the pin assignments for pins 28 and 29 of the J1 connector and DT758-C screw terminal panel.

The pin assignment for Pin 28 should be "Port 0 Latched/" and the pin assignment for Pin 29 should be "Digital Ground."

Replacement pages containing corrected Tables 1, 3, 14, and 15 are enclosed with this document. Please substitute these pages for the corresponding pages in your user manual.

---

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DATA TRANSLATION®

UM-08888-A

# DT2919

## User Manual

**Counter/Timer Board**
**for the IBM® Personal System/2®**

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**First Edition**
September, 1989

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# Table of Contents

**How to Use This Manual** ..... ix
Related Documents ..... x
Where to Get Help ..... xi

## Installing and Using

**Chapter 1: Getting Started** ..... 1
About the DT2919 ..... 3
DT758-C Screw Terminal Panel ..... 4
PACER Subroutine Library ..... 4
Unpacking ..... 5
Installing the DT2919 ..... 6
What You Will Need ..... 7
Step 1: Copy the Adapter Description File to the Reference Diskette ..... 8
Step 2: Install the Board ..... 10
Step 3: POS-Configure the Board ..... 11
Step 4: Connect the Screw Terminal Panel ..... 13
Step 5: Connect the Counter/Timer Devices ..... 14
Connecting Counter/Timer Sources ..... 17
Connecting Counter/Timer Gates ..... 17
Connecting Counter/Timer Outputs ..... 17
Connecting the Interrupt Signal ..... 18
Connecting the Frequency Output Signal ..... 18
Step 6: Connect the Digital I/O Devices ..... 19



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Connecting the Digital I/O Lines . . . . . 21
Connecting the "Port 0 Strobe/" Line . . . . . 21
Connecting the "Port 0 Latched/" Line . . . . . 21
Step 7: Power Up the System . . . . . 22

**Chapter 2: Using the DT2919 . . . . . 23**
Overview . . . . . 25
Counter/Timer Subsystem . . . . . 27
8-bit Bus Interface . . . . . 28
Frequency Scaler . . . . . 28
Counter/Timers . . . . . 30
Binary and BCD Counting . . . . . 30
Count Source . . . . . 32
Gating Control . . . . . 32
Output Control . . . . . 32
Alarm Comparators . . . . . 33
Time-of-Day Option . . . . . 33
Digital I/O Subsystem . . . . . 35
Interrupt Operation . . . . . 36
The DT2919 Registers . . . . . 37
Am9513A Control Register . . . . . 39
Command Register . . . . . 39
Status Register . . . . . 47
Am9513A Data Register . . . . . 48
Master Mode Register . . . . . 49
Counter "x" Mode Register . . . . . 52
Counter "x" Load Register . . . . . 55



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Counter "x" Hold Register . . . . . 55
Alarm "x" Register . . . . . 55
Control/Status Register . . . . . 56
Port 0 Data Register . . . . . 60
Port 1 Data Register . . . . . 61
Clear Interrupt Register . . . . . 62
Basic Operational Sequences . . . . . 63
Initializing the DT2919 . . . . . 64
Programming a Counter/Timer . . . . . 66
To Calculate the Load Register Value for Generating a Frequency Output . . . . . 68
Performing Digital I/O Operations . . . . . 69
To Input Digital Data From an External Device (Port 0: Latch Disabled) . . . . . 69
To Input Digital Data From an External Device (Port 0: Latch Enabled) . . . . . 70
To Send Digital Data to an External Device . . . . . 71
Generating and Clearing Interrupts . . . . . 72
To Generate an Interrupt . . . . . 72
To Clear an Interrupt . . . . . 73

## Reference

**Reference 1: Troubleshooting . . . . . 75**
General Checklist . . . . . 77
Specific Problems . . . . . 78
Service and Support . . . . . 79
If Your DT2919 Needs Factory Service . . . . . 80



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**Reference 2: Configuration** . . . . . 81
Programmable Option Select . . . . . 83
The POS Registers . . . . . 84
I/O Base Address Selection . . . . . 85
Interrupt Priority Level Selection . . . . . 86

**Reference 3: Connectors and Accessories** . . . . . 87
DT2919 Connectors . . . . . 89
P1: IBM Personal System/2 Bus Connector . . . . . 90
J1: External Device Connector . . . . . 95
DT758-C Screw Terminal Panel . . . . . 97
Pin Functions . . . . . 97
Specifications . . . . . 99

**Reference 4: Specifications** . . . . . 101

## Appendixes

**Appendix A: Am9513A Data Sheet** . . . . . 109

**Glossary** . . . . . 145

**Index**

**Warranty**

**Reader's Comment Form**



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# Figures


Figure 1: Connecting the Screw Terminal Panel ..... 13
Figure 2: DT2919 Block Diagram ..... 26
Figure 3: Time-of-Day Format ..... 33
Figure 4: Element and Group Values ..... 42
Figure 5: Status Register Bit Functions ..... 47
Figure 6: Master Mode Register Bit Functions ..... 49
Figure 7: Counter "x" Mode Register Bit Functions .... 52
Figure 8: Control/Status Register Bit Functions ..... 56
Figure 9: I/O Base Address ..... 85
Figure 10: DT2919 Board Connectors ..... 89




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# Tables


Table 1: DT758-C Screw Terminal Assignments ..... 15
Table 2: J1 Pin Assignments – Counter/Timers ..... 16
Table 3: J1 Pin Assignments – Digital Inputs/Outputs . 20
Table 4: Am9513A Subfrequencies (Binary Scaling) .. 28
Table 5: Am9513A Subfrequencies (BCD Scaling) ... 29
Table 6: Binary to Hexadecimal Equivalents ..... 31
Table 6: BCD to Decimal Equivalents ..... 31
Table 7: Time-of-Day Counting Supported Frequencies ..... 34
Table 9: DT2919 I/O Registers ..... 37
Table 10: Command Register Codes ..... 40
Table 11: Load Data Pointer Commands ..... 43
Table 12: POS Registers ..... 84
Table 13: P1 Pin Assignments ..... 91
Table 14: J1 Pin Assignments ..... 96
Table 15: DT758-C Screw Terminal Assignments ..... 98
Table 16: DC Specifications of Digital Lines ..... 105




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# How to Use This Manual

This manual introduces you to Data Translation's DT2919 counter/timer board for IBM Personal System/2 Micro Channel models.

It is assumed that you have a general understanding of digital I/O and counter/timer operations, and that you possess enough proficiency in software to write your own application and diagnostic programs. It is also assumed that you have some familiarity with the IBM Personal System/2 Micro Channel architecture.

Listed below is an overview of the information presented in this manual.

## Installing and Using

Chapter 1, "**Getting Started,**" acquaints you with the major features of the DT2919 and shows you how to install the board in your IBM Personal System/2, POS-configure the board, and connect external devices.

Chapter 2, "**Using the DT2919,**" describes the DT2919 board functions, the board I/O registers, and the Am9513A internal registers. This chapter also instructs you in the basic operation of the DT2919.

## Reference

Reference 1, "**Troubleshooting,**" explains what to do if you encounter difficulty using the DT2919.

Reference 2, "**Configuration,**" describes the POS feature and the POS-configurable options on the DT2919.

Reference 3, "**Connectors and Accessories,**" describes the connectors on the DT2919 board and lists their pinouts, and also discusses the DT758-C Screw Terminal Panel.

Reference 4, "**Specifications,**" lists the electrical and mechanical specifications for the DT2919 board.



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## Appendixes

Appendix A, **"Am9513A Data Sheet,"** contains the data sheet for the Am9513A System Timing Controller from Advanced Micro Devices, Inc.

The **Glossary** defines terms used in this manual.

## Related Documents

The documents listed below may provide additional information for the DT2919 user:

- *PACER User Manual*, UM-08932, Data Translation, Inc.
- *IBM Personal System/2 Technical Reference*, International Business Machines Corporation.
- *IBM Personal System/2 Quick Reference Manual*, International Business Machines Corporation.
- *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*, International Business Machines Corporation.
- *Am9513A/Am9513 System Timing Controller Technical Manual*, Order Number 03402D, Advanced Micro Devices, Inc.
- *Am9513A/AmZ8073A System Timing Controller Data Sheet*, Order Number 01731D, Advanced Micro Devices, Inc.
- *Am9513 Electrical Specification*, Advanced Micro Devices, Inc.



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# Chapter 1

# Getting Started



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*Chapter 1, "**Getting Started**," acquaints you with the major features of the DT2919 and shows you how to install the board in an IBM Personal System/2, POS-configure the board, and connect external devices.*

*This chapter is organized as follows:*

- *About the DT2919*
- *Unpacking*
- *Installing the DT2919*



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# About the DT2919

The DT2919 is a multi-function counter/timer board for the IBM Personal System/2 Micro Channel models (except Model 35). It provides counting, sequencing, and timing functions for a wide variety of applications as well as digital data transfers between the host system and a peripheral device.

The DT2919 plugs into a single I/O expansion slot in the IBM Personal System/2's backplane and operates from the +5V power line on the Micro Channel bus.

The DT2919 adapter description file is located on the PACER distribution diskette, shipped with the DT2919 board.

The **counter/timer subsystem** consists of an Am9513A System Timing Controller and a software-selectable 5MHz or 1MHz base frequency. The Am9513A contains five general purpose counters that use scaled frequencies off the onboard 5MHz or 1MHz clock or from external sources connected to the DT2919. These counters are software-configurable for active-high or active-low polarity and for counting up or down in BCD or binary, and can be cascaded to form an effective counter length of up to 80 bits. The host processor may read an accumulated count at any time without disturbing the counting process.

The **digital input/output subsystem** has two 8-bit digital I/O ports that provide for the transfer of digital data between the Personal System/2 and a peripheral device.

The DT2919 provides a single **interrupt** that is POS-configurable to level 7, 5, 4, 12, 11, 10, or 9. An interrupt is generated on a high-to-low transition (falling edge) signal from an external source connected to the board.

Eight 8-bit I/O mapped **registers** interface the DT2919 with the Personal System/2. These registers are accessed using 8-bit I/O instructions. Two of these registers provide all communication with the Am9513A. Four registers perform all board functions external to the counter/timers. Two registers are reserved for future use. The base I/O address is POS-configurable.



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## DT758-C Screw Terminal Panel

The DT758-C screw terminal panel, available from Data Translation, facilitates external device connections to the DT2919 board. The DT758-C is shipped with an integral 3.3 foot (1 meter) 50-conductor cable assembly that plugs into the DT2919's J1 connector.

## PACER Subroutine Library

The PACER subroutine library package, shipped with the DT2919, supports the board's counter/timer operations and provides subroutines for programming the Am9513A chip directly. The PACER subroutines are callable from Microsoft C, FORTRAN, Pascal, and QuickBASIC.



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# Unpacking

Before you begin installing your DT2919 board, make sure you have received the following items:

- DT2919 Counter/Timer board
- *DT2919 User Manual*
- PACER diskette
- *PACER User Manual*
- *PACER Quick Reference Card*

If an item is missing or damaged, call Data Translation's **Customer Service Department** at **(508) 481-3700**. They will guide you through the appropriate steps for replacing missing or damaged items.

***Note*** *Save the original packing material in the unlikely event any item is damaged and requires factory service.*

Keep the DT2919 board in its protective anti-static bag until you are ready to install it. When you remove the board from the bag, hold the board by the edges and do not touch the components.



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# Installing the DT2919

The DT2919 board is shipped ready for installation for most applications. Follow the steps below to install the adapter description file and DT2919 board and connect external devices to the board. These steps are described in detail on the following pages.

Step 1: Copy the adapter description file to the Reference diskette

Step 2: Install the board

Step 3: POS-configure the board

Step 4: Connect the screw terminal panel

Step 5: Connect the counter/timer devices

Step 6: Connect the digital I/O devices

Step 7: Power up the system

***Caution*** *Be sure to read the directions in each step carefully before attempting it. Follow these steps in the exact order given.*



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## What You Will Need

To install the DT2919 board, you will need the following equipment:

- IBM Personal System/2 Micro Channel computer system (except Model 35)
- Working copy of the Personal System/2 Reference diskette
- Data Translation screw terminal panel or similar product (for connecting external devices)
- Flatblade screwdriver (for connecting devices to the screw terminal panel)
- Small coin (for loosening the cover screws on the Personal System/2 unit cover)



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## Step 1: Copy the Adapter Description File to the Reference Diskette

Before you install the DT2919, copy the adapter description file (@5F6F.ADF, located on the PACER distribution diskette) to a working copy of the Reference diskette shipped with your Personal System/2.

1. Make sure your Personal System/2 is functioning properly.
   - Power up the Personal System/2.

     If the Personal System/2 powers up without errors and the system prompt appears, continue as described below.

     If the Personal System/2 powers up and reports errors, correct the errors before continuing.
   - Power down the system.
2. Power up the Personal System/2 using your working copy of the Reference diskette.
3. When the IBM logo appears, press ENTER to display the Main menu.
4. Select COPY AN OPTION DISKETTE from the menu.
5. When prompted, remove the Reference diskette from drive A and insert the PACER distribution diskette; press ENTER.
6. When prompted, remove the PACER diskette from drive A and insert the Reference diskette.

   *The Reference diskette is updated with the adapter description file.*
7. Exit from the menu.



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8. Remove the Reference diskette from drive A.

9. Store the PACER diskette in a safe place.

10. Power down the system.



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## Step 2: Install the Board

Install the DT2919 board in any available expansion slot in the IBM Personal System/2.

1. Power down the Personal System/2.

2. Power down all accessories (printer, modem, monitor, etc.) connected to the computer.

3. Unplug the system and all accessories from their wall outlets.

4. Disconnect all cables from the rear of the computer.

5. Remove the cover from the Personal System/2 following the instructions for "System Unit Cover Removal" in the *IBM Personal System/2 Quick Reference.*

6. Remove the DT2919 board from its anti-static bag.

7. Install the DT2919 board in any available expansion slot in the Personal System/2 following the instructions for "Adapter Installation" in the *IBM Personal System/2 Quick Reference.*

8. Replace the cover following the instructions for "System Unit Cover Installation" in the *IBM Personal System/2 Quick Reference.*

9. Connect all cables to the rear of the computer.



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## Step 3: POS-Configure the Board

The SET CONFIGURATION utility on the Reference diskette is used to view or change your POS-configured settings for board base I/O address and interrupt priority level, or to run the automatic configuration program.

During automatic configuration, the Personal System/2 makes a list of the boards it finds installed and their particular operation settings. The Personal System/2 then stores the configuration information in battery backed-up memory.

**Note** *You must run the SET CONFIGURATION utility on the Reference diskette whenever you remove, install, or change a board.*

1. Insert your working copy of the Reference diskette, which now contains the adapter description file, into drive A.

2. Power up the Personal System/2.

   *The system reports an error (error code 165).*

3. When the IBM logo displays, press ENTER.

   *The ADAPTER CONFIGURATION ERROR screen appears.*

4. Enter "Y" at the prompt to allow automatic configuration of the system.

5. When done, press ENTER.

   *The system reboots using the Reference diskette in drive A. No error codes should appear at this time. The logo displays.*

6. Press ENTER.

   *The Main menu appears.*

7. Select SET CONFIGURATION.

   *The CONFIGURATION menu appears.*



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8. Select VIEW from the Set Configuration menu.

9. Make note of the board settings for each parameter.

10. If these settings are OK, press the ESC key twice to return to the Main menu. Continue with step 16.

    If any setting needs to be changed, press ESC once to return to the Set Configuration menu. Continue with steps 11 through 17 below.

11. Select CHANGE CONFIGURATION from the Set Configuration menu.

12. Highlight the setting to be changed.

13. Use the F5 and F6 keys to select the new value.

    *If your selection conflicts with settings for another board installed in your system, that selection is highlighted with an asterisk (*).*

    ***Caution*** *Make sure you correct the conflict. If you do not select an alternative setting, the DT2919 board is disabled for use in your system when you try to save the configuration settings.*

14. When done, SAVE (or QUIT).

15. Press ESC to return to the Main menu.

16. Remove the Reference diskette from drive A.

17. Power down the system.



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## Step 4: Connect the Screw Terminal Panel

If you are using a Data Translation screw terminal panel, follow the instructions below for connecting the panel to the DT2919 board.

If you are interfacing peripheral devices to your DT2919 board via another type of device or panel, continue with step 5, "Connect the Counter/Timer Devices," for device connection instructions.

1. Power down the Personal System/2.

2. Position the Personal System/2 so that the rear panel connectors are easily accessed.

3. Plug the 50-pin connector on the DT758-C into the mating connector (J1) on the rear of the DT2919, as shown in Figure 1.

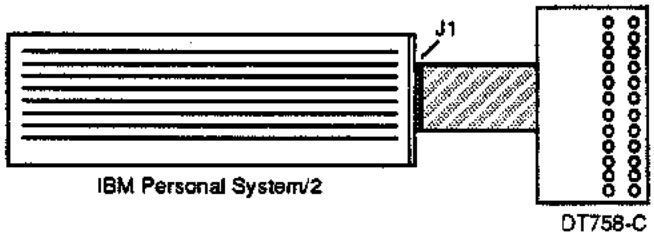



**Figure 1: Connecting the Screw Terminal Panel**



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## Step 5: Connect the Counter/Timer Devices

Each counter/timer has three external connections associated with it: the **source**, **gate**, and **output**.

The **source** is an input to the DT2919. Up to 5 external sources may be connected to the DT2919. The counter/timer uses the source input for counting. The source signal may be a frequency or an event and is user-programmable.

The **gate** is an input to the DT2919. Up to 5 external gates may be connected to the DT2919. A gate can be used as a source to the counters or used to gate the counting of a counter. The gate's function is user-programmable.

The counter/timer **outputs** are the terminal count output of the specific counter/timers. Up to 5 outputs may be connected to the DT2919.



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Table 1 lists the screw terminal assignments for the DT758-C.

**Table 1: DT758-C Screw Terminal Assignments**

| Description | Terminal | | Description |
|---|---|---|---|
| Frequency Out (FOUT) | 1 | 2 | Digital Ground [2] |
| Counter/Timer 1 Output | 3 | 4 | Digital Ground [2] |
| Counter/Timer 2 Output | 5 | 6 | Digital Ground [2] |
| Counter/Timer 3 Output | 7 | 8 | Digital Ground [2] |
| Counter/Timer 4 Output | 9 | 10 | Digital Ground [2] |
| Counter/Timer 5 Output | 11 | 12 | Digital Ground [2] |
| Source 1 | 13 | 14 | Gate 1 |
| Digital Ground [2] | 15 | 16 | Source 2 |
| Gate 2 | 17 | 18 | Digital Ground [2] |
| Source 3 | 19 | 20 | Gate 3 |
| Digital Ground [2] | 21 | 22 | Source 4 |
| Gate 4 | 23 | 24 | Digital Ground [2] |
| Source 5 | 25 | 26 | Gate 5 |
| Digital Ground [2] | 27 | 28 | Port 0 Latched/ |
| Digital Ground [2] | 29 | 30 | Port 0 Strobe/ |
| Port 0 Bit 0 | 31 | 32 | Port 1 Bit 0 |
| Port 0 Bit 1 | 33 | 34 | Port 1 Bit 1 |
| Port 0 Bit 2 | 35 | 36 | Port 1 Bit 2 |
| Port 0 Bit 3 | 37 | 38 | Port 1 Bit 3 |
| Port 0 Bit 4 | 39 | 40 | Port 1 Bit 4 |
| Port 0 Bit 5 | 41 | 42 | Port 1 Bit 5 |
| Port 0 Bit 6 | 43 | 44 | Port 1 Bit 6 |
| Port 0 Bit 7 | 45 | 46 | Port 1 Bit 7 |
| Fuse +5V (1A max) [1] | 47 | 48 | Interrupt Enable |
| Fuse +5V (1A max) [1] | 49 | 50 | Interrupt/ |

*1 External devices requiring power for operation may use the Fuse +5V power sources. Care should be taken, however, not to draw more than 1A or the power supply etch, F1, will blow.*

*2 On the screw terminal panel, all digital grounds should be tied together to reduce crosstalk on the ribbon cable.*



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Table 2 lists the J1 connector pin assignments for the counter/timer connections. Refer to this table if you are connecting devices directly to the J1 connector without the use of a screw terminal panel.

**Table 2: J1 Pin Assignments – Counter/Timers**

| Description | Pin | Pin | Description |
|---|---|---|---|
| Frequency Output | 1 | 2 | Digital Ground |
| Counter/Timer 1 Output | 3 | 4 | Digital Ground |
| Counter/Timer 2 Output | 5 | 6 | Digital Ground |
| Counter/Timer 3 Output | 7 | 8 | Digital Ground |
| Counter/Timer 4 Output | 9 | 10 | Digital Ground |
| Counter/Timer 5 Output | 11 | 12 | Digital Ground |
| Source 1 | 13 | 14 | Gate 1 |
| Digital Ground | 15 | 16 | Source 2 |
| Gate 2 | 17 | 18 | Digital Ground |
| Source 3 | 19 | 20 | Gate 3 |
| Digital Ground | 21 | 22 | Source 4 |
| Gate 4 | 23 | 24 | Digital Ground |
| Source 5 | 25 | 26 | Gate 5 |
| | | | |
| Fuse +5V (1A max)[1] | 47 | 48 | Interrupt Enable |
| Fuse +5V (1A max)[1] | 49 | 50 | Interrupt/ |

1 *External devices requiring power for operation may use the Fuse +5V power sources. Care should be taken, however, not to draw more than 1A or the power supply etch, F1, will blow.*



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**Note** *In the following connection procedures, "terminal" refers to a screw terminal pin on the DT758-C and "pin" refers to a pin on the DT2919's J1 connector.*

## Connecting Counter/Timer Sources

1. Connect the high side of the source to a Source terminal or pin.

2. Connect the low side of the source to any Digital Ground terminal or pin.

3. If you are using the Frequency Output (FOUT) signal as a source for the counter/timers, connect the Frequency Out (FOUT) terminal or pin to a Source terminal or pin.

4. If you are using a counter/timer output signal as a source for the counter/timers, connect the Counter/Timer Output terminal or pin to the Source pin of a different counter/timer.

## Connecting Counter/Timer Gates

1. Connect the high side of the gate to a Gate terminal or pin.

2. Connect the low side of the gate to any Digital Ground terminal or pin.

## Connecting Counter/Timer Outputs

1. Connect one of the five Counter/Timer Output terminals or pins to the high side of the device receiving the output signal.

2. Connect the low side of the device receiving the output signal to any Digital Ground terminal or pin.



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## Connecting the Interrupt Signal

1. Connect the high side of the interrupt signal to the Interrupt/ terminal or pin.

2. Connect the low side of the interrupt signal to any Digital Ground terminal or pin.

**If you wish to hardware enable the interrupt:**

1. Connect the high side of the enabling device to the Interrupt Enable terminal or pin.

2. Connect the low side of the signal to any Digital Ground terminal or pin.

3. If you are using the counter/timer output as an interrupt signal, connect the Counter/Timer Output terminal or pin to the Interrupt/ terminal or pin.

***Note*** *Refer to the Chapter 2 section entitled "Interrupt Operation" for more information on using interrupts.*

## Connecting the Frequency Output Signal

1. Connect the high side of the device receiving the signal to the Frequency Output (FOUT) terminal or pin.

2. Connect the low side of the device receiving the signal to any Digital Ground terminal or pin.



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## Step 6: Connect the Digital I/O Devices

The DT2919 contains 16 digital I/O lines organized as two 8-bit line ports. Each port can be software-programmed for digital input or digital output operations. Digital inputs can monitor alarms or sensors that have TTL outputs; digital outputs can drive TTL inputs on control and measurement equipment.

There are two optional signals for inputting data to Port 0. A high-to-low transition on the Port 0 Strobe/ line latches the data into the Port 0 Data register. When the data has been latched in, the "Port 0 Latched/" flag clears. (The Latched bit in the Control/Status register also indicates when data has been latched in.) A read of the data sets the Port 0 Latched/ line, indicating new data may be latched in. If you do not enable the Latch function, a read of the data returns the actual value on these lines at the time of the read.

The Port 0 Strobe/ line is an input and the Port 0 Latched/ line is an output.



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If you are using the DT758-C screw terminal panel, refer to Table 1 for the digital I/O terminal assignments when making your digital I/O connections.

If you are connecting directly to the DT2919's J1 connector, refer to Table 3 below for the J1 connector pin assignments for digital I/O connections.

**Table 3: J1 Pin Assignments – Digital Inputs/Outputs**

| Description | Pin | Pin | Description |
|---|---|---|---|
| Digital Ground | 27 | 28 | Port 0 Latched/ |
| Digital Ground | 29 | 30 | Port 0 Strobe/ |
| Port 0 bit 0 | 31 | 32 | Port 1 bit 0 |
| Port 0 bit 1 | 33 | 34 | Port 1 bit 1 |
| Port 0 bit 2 | 35 | 36 | Port 1 bit 2 |
| Port 0 bit 3 | 37 | 38 | Port 1 bit 3 |
| Port 0 bit 4 | 39 | 40 | Port 1 bit 4 |
| Port 0 bit 5 | 41 | 42 | Port 1 bit 5 |
| Port 0 bit 6 | 43 | 44 | Port 1 bit 6 |
| Port 0 bit 7 | 45 | 46 | Port 1 bit 7 |



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**Note** *In the following connection procedures, "terminal" refers to a screw terminal pin on the DT758-C and "pin" refers to a pin on the DT2919's J1 connector.*

## Connecting the Digital I/O Lines

1. For each digital I/O line being used, connect the high side to the appropriate Port and bit terminal or pin.

2. Connect the low side of the digital I/O line to any Digital Ground terminal or pin.

## Connecting the "Port 0 Strobe/" Line

1. Connect the high side of the device providing the latch signal to the Port 0 Strobe/ terminal or pin.

2. Connect the low side of the signal to any Digital Ground terminal or pin.

## Connecting the "Port 0 Latched/" Line

1. Connect the Port 0 Latched/ line to the high side of the device receiving the signal.

2. Connect any Digital Ground terminal or pin to the low side of the device receiving the signal.



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## Step 7: Power Up the System

Once you are satisfied that connections are made properly and are secure, arrange the components so you can work with them comfortably.

1. Power up all accessories.

2. Power up the system (without the Reference diskette).



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# Chapter 2

# Using the DT2919



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*Chapter 2, "**Using the DT2919**," describes the DT2919 board functions, the board I/O registers, and the Am9513A internal registers. This chapter also instructs you in the basic operation of the DT2919.*

*This chapter is organized as follows:*

- *Overview*
- *Counter/Timer Subsystem*
- *Digital I/O Subsystem*
- *Interrupt Operation*
- *The DT2919 Registers*
- *Basic Operational Sequences*



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# Overview

The DT2919 features two main subsystems for performing counter/timer functions and digital I/O operations. Figure 2 on the following page provides a functional block diagram of the DT2919 board.

Six 8-bit I/O registers, located in the Personal System/2 I/O space, control the DT2919 board operations. Two of these registers perform all data transfer operations with the Am9513A System Timing Controller chip. The other four registers perform general functions not contained in the Am9513A, as well as digital data transfers at the two digital I/O ports.

**Note** *Refer to "The DT2919 Registers" later in this chapter for important information on working with the Am9513A System Timing Controller chip. Additional information can be found in Appendix A, "Am9513A Data Sheet."*

The following sections describe the operation of the DT2919's counter/timer and digital I/O subsystems.

**Note** *The PACER subroutines handle most of the low-level board functions discussed in this chapter; if you are using PACER, you may wish to refer to this material for reference only. If you are not using PACER, you will need to read this chapter to understand the functionality of your board.*



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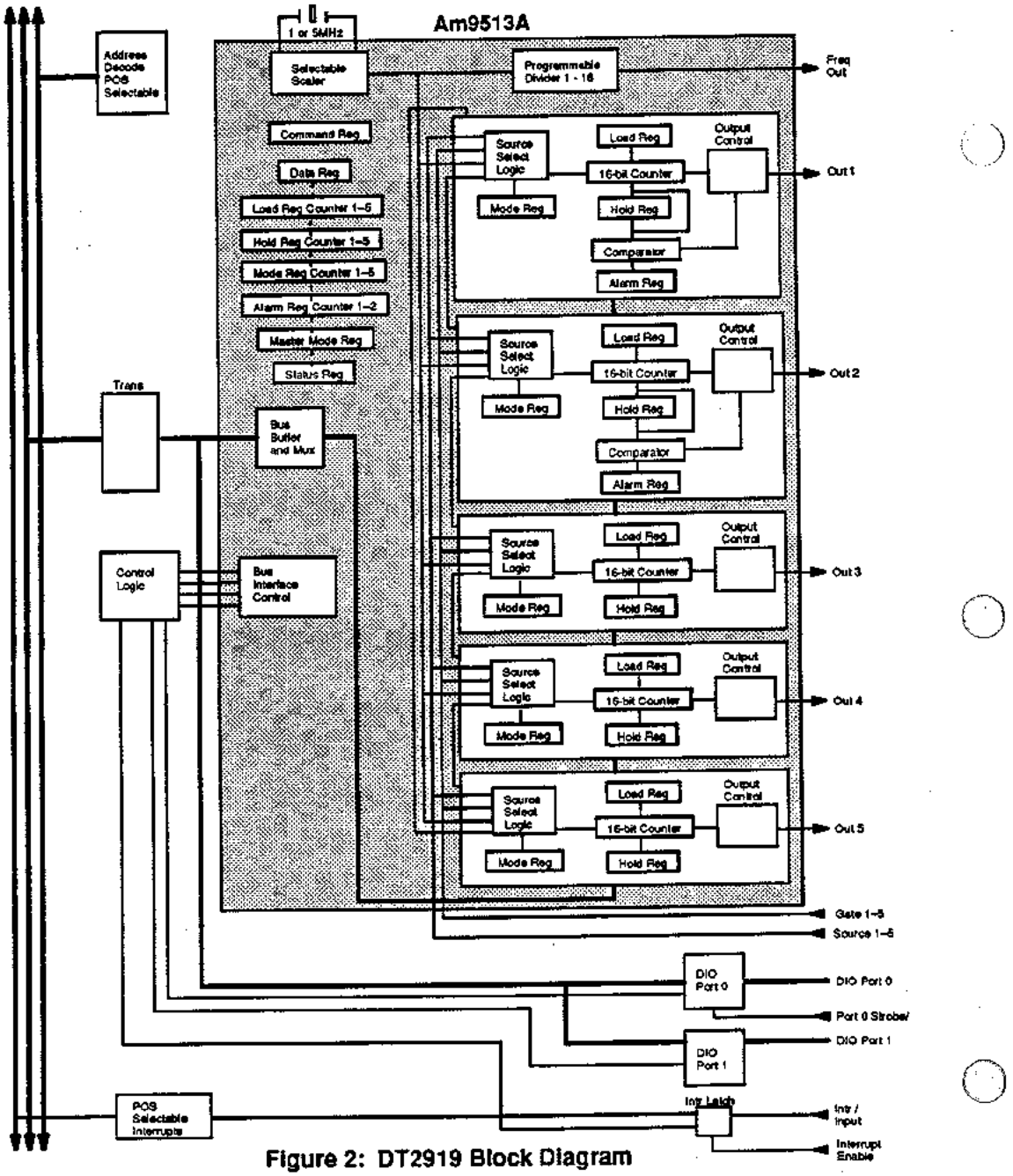



**Figure 2: DT2919 Block Diagram**



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# Counter/Timer Subsystem

The DT2919 counter/timer subsystem consists of an Am9513A System Timing Controller and a software-selectable 1MHz or 5MHz clock. The Am9513A provides the following features:

- Five independent 16-bit counter/timers
- Up/down and binary/BCD counting
- Selectable frequency scaler
- Programmable frequency output
- 8-bit bus interface
- Time-of-day option
- Alarm comparators on counter/timers 1 and 2
- Complex duty cycle outputs
- One-shot or continuous outputs
- Programmable count/gate source selection
- Programmable gating functions
- Retriggering capability

This section provides an overview of the counter/timer subsystem on the DT2919 board. Additional information on the counter/timers can be found later in this chapter and in Appendix A, "Am9513A Data Sheet."



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## 8-bit Bus Interface

The block diagram in Figure 2 illustrates the basic flow of information in the five counter/timers. The Am9513A's internal data bus for the counter/timers is 16 bits wide. The DT2919 interface to these internal registers is 8 bits wide. Data transfers to and from the Am9513A are accomplished in two steps. These data transfers occur at two of the six I/O registers on the DT2919. The Am9513A's internal registers are subaddressed by specific commands written to the two Am9513A I/O registers on the DT2919.

## Frequency Scaler

A software-selectable 1MHz or 5MHz clock on the DT2919 is the base frequency source to the Am9513A. The Am9513A divides the base frequency by the Selectable Scaler to provide several subfrequencies that may be used as frequency sources for the counter/timers. This frequency division is software-selectable for binary or BCD scaling. In the binary scaling mode, each resulting subfrequency is 1/16 of the preceding frequency. In the BCD scaling mode, each resulting subfrequency is 1/10 of the preceding frequency. The Selectable Scaler offers five different subfrequencies, referred to as F1, F2, F3, F4, and F5. Tables 4 and 5 list resulting subfrequencies from the Selectable Scaler using binary and BCD scaling, respectively.

**Table 4: Am9513A Subfrequencies (Binary Scaling)**

| Subfrequency | 5MHz | 1MHz |
|---|---|---|
| F1 | Oscillator = 5MHz | Oscillator = 1MHz |
| F2 | F1/16 = 312.5kHz | F1/16 = 62.5kHz |
| F3 | F1/256 = 19.5kHz | F1/256 = 3.9kHz |
| F4 | F1/4096 = 1.2kHz | F1/4096 = 244Hz |
| F5 | F1/65,536 = 76.3Hz | F1/65,536 = 15.3Hz |



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**Table 5: Am9513A Subfrequencies (BCD Scaling)**

| Subfrequency | 5MHz | 1MHz |
|---|---|---|
| F1 | Oscillator = 5MHz | Oscillator = 1MHz |
| F2 | F1/10 = 500kHz | F1/10 = 100kHz |
| F3 | F1/100 = 50kHz | F1/100 = 10kHz |
| F4 | F1/1000 = 5kHz | F1/1000 = 1kHz |
| F5 | F1/10,000 = 500Hz | F1/10,000 = 100Hz |

The subfrequency (F1 through F5) may also be used as an input to the Am9513A's Programmable Divider and as an output at the Frequency Output (FOUT) pin on the DT2919's J1 connector. The Programmable Divider has 16 software-selectable divider ratios ranging from a value of 1 to 16. Other sources to the Programmable Divider include the five source signals and the five external gate inputs on the J1 connector. The Frequency Output (FOUT) at the J1 connector is software-enabled.

The Frequency Output (FOUT) may be used as an external source (Source 1 through Source 5) for any of the five counter/timers or an external device.

16 x

$10^5 \times 1/8$

100 C



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## Counter/Timers

The Am9513A has five 16-bit counter/timers. Each counter/timer has a count source, a gate input, and an output. The remainder of this section discusses the counter/timer controls and options.

### Binary and BCD Counting

Each counter/timer is programmable for up or down counting in binary or binary coded decimal (BCD). Count values range from 0000 to FFFF (hex) for binary counting and 0000 to 9999 for BCD counting. The hex values represent decimal values from 0 to 65,535.

The count is a 16-bit value represented as a series of binary digits having values of 0s and 1s. In binary counting, each binary digit represents a power of two. The first (least significant) digit is $2^0$. The next is $2^1$, then $2^2$, and so on. To determine the decimal equivalent of a binary number, determine the value of each digit having a value of 1 and then add these numbers together. For example, an 8-bit binary value of 00010101 equals $2^0 + 2^2 + 2^4$, or $1 + 4 + 16 = 21$ (decimal).

Binary numbers are frequently expressed as their hexadecimal ($base_{16}$) equivalents. To determine the hexadecimal equivalent of a binary number, divide the binary number into groups of 4 digits and then determine the hex equivalent of each 4-digit group. Table 6 on the following page lists the hex equivalents of the 4-digit binary values.



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**Table 6: Binary to Hexadecimal Equivalents**

| Binary | Hex | | Binary |
|---|---|---|---|
| 0000 | 0 | 8 | 1000 |
| 0001 | 1 | 9 | 1001 |
| 0010 | 2 | A | 1010 |
| 0011 | 3 | B | 1011 |
| 0100 | 4 | C | 1100 |
| 0101 | 5 | D | 1101 |
| 0110 | 6 | E | 1110 |
| 0111 | 7 | F | 1111 |

For example, 01001100 (binary) equals 4C (hex).

BCD counting, used with the DT2919's time-of-day option, uses four binary digits to represent one decimal digit. To calculate the decimal equivalent of a binary number, divide the binary number into groups of 4 digits and then determine the BCD equivalent of each 4-digit group. Table 7 lists the BCD to decimal equivalents.

**Table 7: BCD to Decimal Equivalents**

| BCD | Decimal |
|---|---|
| 0000 | 0 |
| 0001 | 1 |
| 0010 | 2 |
| 0011 | 3 |
| 0100 | 4 |
| 0101 | 5 |
| 0110 | 6 |
| 0111 | 7 |
| 1000 | 8 |
| 1001 | 9 |

For example, 00010101 (binary) equals 0001 0101 (BCD), or 15 (decimal).



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## Count Source

Each counter can be clocked from one of 16 sources and can be clocked on the rising or falling edge of the source. These sources include any of the five external source signals, any of the five external gate signals, the terminal count of the previous counter (TCN–1), and any of the five scaled frequencies (F1 through F5). More than one counter/timer can use the same clock source.

## Gating Control

Each counter/timer is enabled or disabled for counting by a gate input. This gate input can come from a number of sources. It can be the counter/timer's own gate input (GATE N), the terminal count of the previous counter (TCN–1), or the gate input of adjacent counters (GATE N+1, GATE N–1). An external gate can be a level input (active high or low) or an edge (rising or falling). More than one counter/timer can be gated off the same signal.

## Output Control

Each counter/timer can be programmed to count once or repetitively with its output a pulse or toggle at terminal count. The output pulse can be high or low for one clock cycle of the source. When toggled, the output alternates between high or low on each terminal count.

Terminal count occurs when the counter reaches the equivalent of 0. This is 0000 for down counting, 9999 (BCD) for BCD up counting, and FFFF (hex) for binary up counting.

In the non-toggle mode, the counter/timer output sets at terminal count. In the toggle mode, the output changes states on the next count after terminal count. The timing diagrams for each mode are located in Appendix A, "Am9513A Data Sheet." These diagrams illustrate the relationship of the various counter/timer signals during counter/timer operations.



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## Alarm Comparators

Counter/timers 1 and 2 contain a 16-bit alarm register and comparator. When the counter value reaches the value in the alarm register, the counter output will go true if the comparator enable bit is set. When the comparator enable bit is set, the alarm output is substituted for the normal counter output.

Each comparator can be used individually, or both comparators can be used together for a full 32-bit compare. If the time-of-day operation is enabled and both comparators are enabled, a true 32-bit compare will generate a true signal on the output from counter 2. The output from counter 1 will continue to reflect the 16-bit comparison between alarm 1 and the counter value in counter/timer 1.

## Time-of-Day Option

Counter/timers 1 and 2 can be operated in an optional time-of-day mode. That is, counter/timers 1 and 2 roll over at the counts required for time-of-day accumulation. Figure 3 illustrates the format of the 24-hour clock.

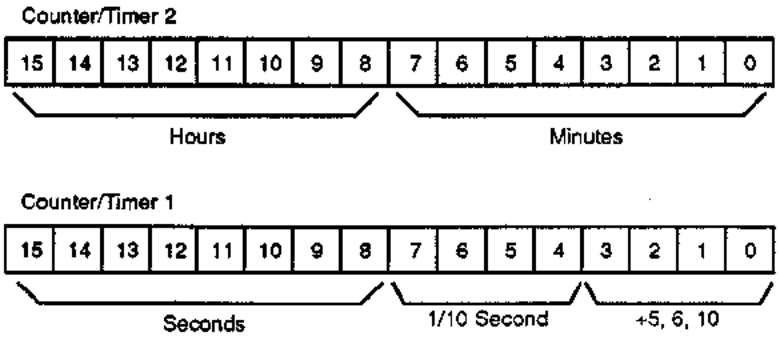



**Figure 3: Time-of-Day Format**

Time-of-day mode is selected using bits 0 and 1 in the Master Mode register. These bit values also represent the input frequency to counter/timer 1. Table 8 lists the frequencies supported by the Time-of-Day function.



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**Table 8: Time-of-Day Counting Supported Frequencies**

| Frequency | Bit 1 | Bit 0 |
|---|---|---|
| Time-of-Day disabled | 0 | 0 |
| 50Hz input | 0 | 1 |
| 60Hz input | 1 | 0 |
| 100Hz input | 1 | 1 |

The DT2919's 1MHz frequency, provided for time-of-day functions, can be divided down to 100Hz using the BCD scaling mode. This 100Hz signal appears on F5.

It is recommended that counter/timer 1 be set as follows:

- select desired source input
- no gating
- disable special gate
- reload from Load register
- count up
- BCD counting
- count repetitively

Counter/timer 2 should be set in the same manner as counter/timer 1 except the source input is specified as TCN–1.

***Note*** *Refer to Chapter 4, "Time-of-Day Counting," in the* Am9513A/Am9513 System Timing Controller Technical Manual *for detailed information on programming time-of-day operations.*



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# Digital I/O Subsystem

The DT2919's digital I/O subsystem transfers 8-bit digital data under program control between user memory and a user-supplied peripheral I/O device connected to the board. The digital I/O subsystem is independent of the counter/timer subsystem and can function concurrently with counting and timing operations.

The DT2919 provides two 8-line digital I/O ports. Both ports input and output data separately. Both ports are always readable and are configured for read-only operations after DT2919 initialization or power-up.

The input to Port 0 consists of a latch with a strobe line. This latch is optional and must be separately enabled. When latch-enabled, a high-to-low transition on the Port 0 Strobe/ line causes data to be latched into Port 0. The Port 0 Latched/ line and the Latched bit in the Control/Status register indicate when data has been latched and is available for reading. Reading Port 0 sets the Port 0 Latched/ line and indicates that another value may be latched in. When the latch is not enabled, a read of Port 0 returns the actual value on the DIO lines for Port 0 at the time of the read.

The input to Port 1 is not latched. A read of Port 1 returns the actual value on the DIO lines for Port 1 at the time of the read.

Each port is output-enabled separately. When output-enabled, the value written to the port's register is output immediately to the external device connected to that port. A read of an output-enabled port returns the value last written to the port.



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# Interrupt Operation

The DT2919 provides a connection for an external interrupt signal. This signal, when driven high-to-low, generates an interrupt on the system interrupt line determined by the POS configuration of your board. (Refer to Reference 2, "Configuration," for information on interrupt level selection.)

The DT2919 recognizes the external interrupt when the following conditions are met:

- the interrupt signal is connected to the Interrupt/ line at the J1 connector
- the Software Interrupt Enable bit in the Control/Status register is set
- the external Interrupt Enable line is high

The interrupt is generated on a high-to-low transition of the Interrupt/ line. The external Interrupt Enable line can be driven high by a device connected to that line for hardware control of the interrupts. If no device is connected, the DT2919 pulls this line high internally, allowing software control of the interrupts.

There are three ways to clear the interrupt:

1. Write any value to the Clear Interrupt register.

   This software method clears the interrupt and leaves it enabled.

2. Clear the Software Interrupt Enable bit in the Control/Status register.

   This software method clears the interrupt and disables generation of additional interrupts.

3. Disable the external Interrupt Enable line by bringing it low.

   This hardware method clears the interrupt and disables generation of additional interrupts.



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# The DT2919 Registers

The DT2919 board uses six 8-bit I/O registers for control and status purposes. These six registers are located in the Personal System/2's I/O space and are accessed using 8-bit I/O operations.

The DT2919 I/O registers and their functions are listed in Table 9 and are described in detail in the following sections. Note that both the table and the register descriptions are presented in functional order (not in order by register memory address).

**Table 9: DT2919 I/O Registers**

| Register | Function | Address |
|---|---|---|
| Am9513A Control | Accesses the Am9513A internal Command register via writes; accesses the Am9513A internal Status register via reads | I/O Base + 1 |
| Am9513A Data | Communicates with the Am9513A data port | I/O Base + 0 |
| Control/Status | Performs general DT2919 functions not performed by the Am9513A | I/O Base + 4 |
| Port 0 Data | Controls Port 0 digital I/O operations | I/O Base + 2 |
| Port 1 Data | Controls Port 1 digital I/O operations | I/O Base + 3 |
| Clear Interrupt | Clears an interrupt | I/O Base + 5 |
| Reserved | | I/O Base + 6 |
| Reserved | | I/O Base + 7 |



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All data transfers with the Am9513A System Timing Controller chip occur through two of the DT2919 board's registers: the Am9513A Control register and the Am9513A Data register.

The Am9513A is programmed via the following registers, which are internal to the chip itself:

- Command register
- Status register
- Master Mode register
- Counter "x" Mode register
- Counter "x" Load register
- Counter "x" Hold register
- Counter "x" Alarm register

The DT2919's Am9513A Control register (I/O base + 1) communicates with the chip's Command and Status registers. A write to the Am9513A Control register accesses the chip's Command register; while a read of the AM9513A Control register accesses the chip's Status register.

The DT2919's Am9513A Data register (I/O base + 0) communicates with all other internal registers in the Am9513A. Data transfers between the Am9513A's Master Mode register and the Counter Mode, Load, Hold, and Alarm registers for each counter/timer and the DT2919 occur at this register.

***Note*** *Appendix A, "Am9513A Data Sheet," describes these registers and Am9513A operation in detail. Additional information is contained in the* Am9513A/Am9513 System Timing Controller Technical Manual *available from Advanced Micro Devices, Inc.*



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## Am9513A Control Register

***Address: I/O Base + 1*** ***Access: Read/Write***

The DT2919's Am9513A Control Register is a read/write register that directly accesses the internal Am9513A Command and Status registers. A write to this register loads a command code into the Command register. A read of this register returns the contents of the Status register.

The following sections discuss the Am9513A's internal Command and Status registers. Refer to Appendix A, "Am9513A Data Sheet," for detailed information on these registers.

### Command Register

The Command register, accessed by writes to the DT2919's Am9513A Control register, provides command codes that select the internal register to be programmed. The selected register can then be programmed via the DT2919's Am9513A Data register. Additional command codes perform specific counter/timer operations, or clear or set bits in the Master Mode register.

Table 10 on the following page summarizes these command codes. A brief description of each command code follows Table 10.



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## Table 10: Command Register Codes

| Command Code | | | | | | | | Function |
|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | E2 | E1 | G4 | G2 | G1 | Load Data Pointer register with E & G |
| | | | | | | | | |
| 0 | 0 | 1 | S5 | S4 | S3 | S2 | S1 | Arm counting for all selected counters |
| 0 | 1 | 0 | S5 | S4 | S3 | S2 | S1 | Load contents of selected counters |
| 0 | 1 | 1 | S5 | S4 | S3 | S2 | S1 | Load and arm all selected counters |
| 1 | 0 | 0 | S5 | S4 | S3 | S2 | S1 | Disarm and save all selected counters |
| 1 | 0 | 1 | S5 | S4 | S3 | S2 | S1 | Save all selected counters in Hold register |
| 1 | 1 | 0 | S5 | S4 | S3 | S2 | S1 | Disarm all selected counters |
| | | | | | | | | |
| 1 | 1 | 1 | 0 | 1 | N4 | N2 | N1 | Set output counter N (001 <= N <= 101) |
| 1 | 1 | 1 | 0 | 0 | N4 | N2 | N1 | Clear output counter N (001 <= N <= 101) |
| 1 | 1 | 1 | 1 | 0 | N4 | N2 | N1 | Step counter N (001 <= N <= 101) |
| | | | | | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | Disable pointer sequencing (set MM14) |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Gate Frequency Out Off (set MM12) |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | Enter 16-bit bus mode (set MM13) [1] |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Enable Pointer sequencing (clear MM14) |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | Gate Frequency Out On (clear MM12) |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | Enter 8-bit bus mode (clear MM13) |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | Enable prefetch |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | Disable prefetch |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Master reset |

[1] *This command must never be executed on the DT2919. The DT2919 uses the 8-bit bus mode only.*



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Bits 7, 6, and 5 of the command codes perform the following functions, depending on their state.

- All codes beginning with 000 select a particular register according to the E and G fields.
- All codes beginning with 001 to 110 directly control the counting process in the five counter/timers. These command codes contain a 5-bit S field. Each bit in the S field corresponds to one of the five counter/timers. When an S bit is 1, the specified operation is performed on the corresponding counter/timer. When an S bit is 0, no operation is performed on the counter/timer.
- All codes beginning with 111 and ending with N4, N2, N1 use a 3-bit binary code (N4, N2, N1) to identify a specific counter/timer. These command codes allow you to program only one counter at a time with a specific function.
- All codes beginning with 111 and ending with 000, 110, or 111 clear and set bits in the Master Mode register. (Writing to the Master Mode register also performs these functions.)



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**Load Data Pointer Register (0 0 0 E2 E1 G4 G2 G1)**

Selects the counter/timer register for subsequent loading or reading. The particular register is determined by the E2 and E1 values. The counter/timer is determined by the G4, G2, and G1 values. Refer to Figure 4 for the possible E and G values.

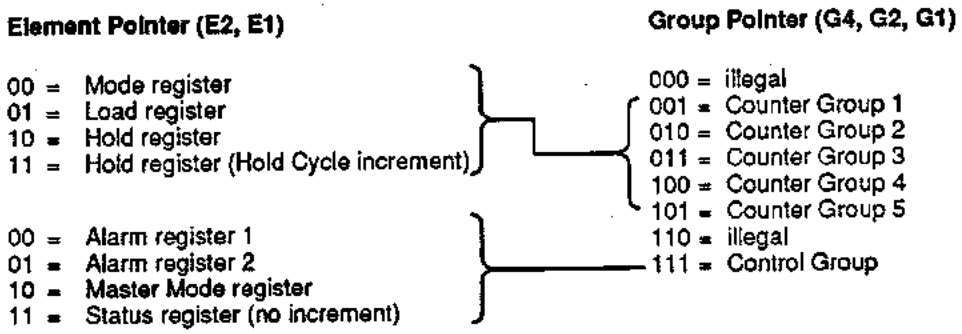



**Figure 4: Element and Group Values**



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Table 11 summarizes the Load Data Pointer register values for each of the counter/timers.

**Table 11: Load Data Pointer Commands**

| | Element Cycle | | | Hold Cycle |
|---|---|---|---|---|
| | Mode | Load | Hold | Hold |
| Counter/Timer 1 | 01 | 09 | 11 | 19 |
| Counter/Timer 2 | 02 | 0A | 12 | 1A |
| Counter/Timer 3 | 03 | 0B | 13 | 1B |
| Counter/Timer 4 | 04 | 0C | 14 | 1C |
| Counter/Timer 5 | 05 | 0D | 15 | 1D |
| Master Mode register = 17 | | | | |
| Alarm 1 register = 07 | | | | |
| Alarm 2 register = 0F | | | | |
| Status register = 1F | | | | |

*All codes are in hex.*

Automatic incrementing of the various Data Pointer elements is normally invoked, but can be turned off through bit 14 (Auto Incrementing) in the Master Mode register. Refer to Appendix A, "Am9513A Data Sheet," for further information on this feature.

When E1 = 0 or E2 = 0 and a Counter group is selected, the Data Pointer automatically sequences through the Counter Mode, Load, and Hold registers for that counter/timer and then increments to the next counter/timer, sequencing through its registers.

When E1 and E2 are 11 and a Counter group is selected, then the Data Pointer sequences only through the Hold registers. The Counter Mode and Load registers are not accessed.

When E1 = 0 or E2 = 0 and the Group pointer is 111, the Data Pointer cycles through Alarm 1, Alarm 2, and Master Mode registers only.

When E1 and E2 are 11 and the Group pointer is 111, no incrementing takes place and only the Status register is available through the DT2919's Data register.



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**Arm Counters (0 0 1 S5 S4 S3 S2 S1)**

Enables those counter/timers specified (via the S field) for counting.

**Load Counters (0 1 0 S5 S4 S3 S2 S1)**

Loads those counter/timers specified (via the S field) with the contents of the Load or Hold register (as determined by the counter/timer's Counter Mode register).

**Load-and-Arm Counters ( 0 1 1 S5 S4 S3 S2 S1)**

Performs a Load Counter command followed by an Arm Counter command on all counter/timers specified (via the S field).

**Disarm-and-Save Counters (1 0 0 S5 S4 S3 S2 S1)**

Performs a Disarm Counter command followed by a Save Counter command on all counter/timers specified (via the S field).

**Save Counters (1 0 1 S5 S4 S3 S2 S1)**

Transfers the count of all counter/timers specified (via the S field) into their respective Hold registers. This transfer does not interface with the counting operation.

**Disarm Counters (1 1 0 S5 S4 S3 S2 S1)**

Disables counting for all counter/timers specified (via the S field).

**Set Toggle Out (1 1 1 0 1 N4 N2 N1)**

When in the Toggle mode (determined by the Counter Mode register), sets the initial output level high for the specified counter/timer. (The counter/timer is specified by the N4, N2, and N1 values.)



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**Clear Toggle Out (1 1 1 0 0 N4 N2 N1)**

When in the Toggle mode (determined by the Counter Mode register), sets the initial output level low for the specified counter/timer. (The counter/timer is specified by the N4, N2, and N1 values.)

**Step Counter (1 1 1 1 0 N4 N2 N1)**

Increments or decrements the count value of the specified counter/timer by 1. The direction of the step is determined by the count direction set in the Counter Mode register for that counter/timer. (The counter/timer is specified by the N4, N2, and N1 values.)

**Disable Data Pointer Sequencing (1 1 1 0 1 0 0 0)**

Sets bit 14 (Auto Incrementing) in the Master Mode register, disabling the auto-incrementing mode of the Data Pointer.

**Gate Off FOUT (1 1 1 0 1 1 1 0)**

Sets bit 12 (FOUT Gate) in the Master Mode register, disabling the Frequency Output signal at the J1 connector.

**16-bit Bus Mode (1 1 1 0 1 1 1 1)**

*This command must never be executed on the DT2919. The DT2919 uses the 8-bit bus mode only.*

**Enable Data Pointer Sequencing (1 1 1 0 0 0 0 0)**

Clears bit 14 (Auto Incrementing) in the Master Mode register, enabling the auto-incrementing mode of the Data Pointer.

**Gate On FOUT (1 1 1 0 0 1 1 0)**

Clears bit 12 (FOUT Gate) in the Master Mode register, enabling the Frequency Output signal at the J1 connector.



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**8-bit Bus Mode (1 1 1 0 0 1 1 1)**

Clears bit 13 (Data Bus Width) in the Master Mode register, setting the Am9513A for 8-bit transfers with the DT2919.

**Enable Prefetch (1 1 1 1 1 0 0 0)**

Enables the prefetch circuitry for Write operations after it has been disabled.

**Disable Prefetch (1 1 1 1 1 0 0 1)**

Disables the prefetch circuitry for Write operations, reducing the write recovery time.

**Master Reset (1 1 1 1 1 1 1 1)**

Performs a reset of the Am9513A. It disarms all counter/timers, and loads 0000 into the Master Mode, Load, and Hold registers, and 0B00 into the Counter Mode registers.



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## Status Register

The Status register, accessed by reads of the Am9513A Control register, indicates the state of the output signal for each of the five counter/timers and the state of the byte pointer for the Data register. Figure 5 illustrates the Status register bit functions.

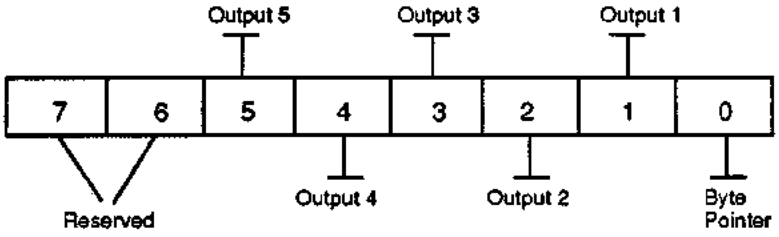



**Figure 5: Status Register Bit Functions**

### Bits 7 and 6: Reserved

These bits are not used and will return a value of 0 or 1.

### Bits 5 through 1: Output "x"

Reflects the exact state of the counter/timer "x" output. This state can be an active-high or active-low terminal count output, or a toggled output as determined by the Output Control bits in the Counter "x" Mode register. Output 1 and Output 2 will reflect the comparator output if the comparators are enabled.

### Bit 0: Byte Pointer

Indicates whether the data high byte or the data low byte is to be transferred on the next access through the Data register. This bit state toggles following each 8-bit data transfer. When this bit is clear, the data high byte is expected. When this bit is set, the data low byte will transfer. The Byte Pointer sets whenever the data pointer (command codes starting with 000) is loaded.



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## Am9513A Data Register

***Address: I/O Base + 0*** ***Access: Read/Write***

The DT2919's Am9513A Data register communicates with the data port of the Am9513A chip. Data transfers between the chips's Master Mode, Counter Mode, Counter Load, Counter Hold, and Alarm registers for each counter/timer and the DT2919 occur at this register. A command code written to the Command register (through the DT2919's Am9513A Control register ) selects the register for addressing.

The Master Mode, Counter Mode, Counter Load, Counter Hold, and Alarm registers are 16-bit registers. Therefore, two writes to the Am9513A Data register are required to load a register with a value and two reads of this register are necessary to obtain a counter/timer register's value.

The following sections describe the Am9513A's internal Master Mode, Counter Mode, Counter Load, Counter Hold and Alarm registers. Refer to Appendix A, "Am9513A Data Sheet," for detailed information on these registers.



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## Master Mode Register

The Master Mode register controls those counter/timer functions not controlled by the Counter "x" Mode registers. These functions include the time-of-day option, comparator enables, data bus width, data pointer sequencing, Programmable Divider value, and Frequency Output enable. Figure 6 illustrates the Master Mode register bit functions.

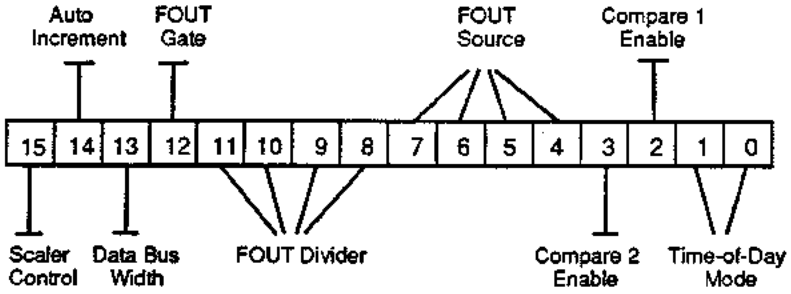



**Figure 6: Master Mode Register Bit Functions**

### Bit 15: Scaler Control

Determines whether the scaled frequencies available to the counter/timers are divided in binary or BCD steps. The scaled frequencies are selected for binary division at reset. This bit can assume the following values:

0 = binary division
1 = BCD division

### Bit 14: Auto Incrementing

Determines whether the Data Pointer will automatically increment through the counter/timer registers. The auto-incrementing mode is selected at reset. This bit can assume the following values:

0 = auto-incrementing enabled
1 = auto-incrementing disabled



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### Bit 13: Data Bus Width

Select the 8-bit bus width for communicating with the DT2919 board. This bit must always be clear.

### Bit 12: FOUT Gate

Enables/disables the Frequency Output signal at the J1 connector. The Frequency Output signal is enabled at reset. This bit can assume the following values:

0 = FOUT signal enabled
1 = FOUT signal disabled

### Bits 11 through 8: FOUT Divider

Determines which of the 16 possible divider values is used to generate the Frequency Output signal. The divider value is set to 16 at reset. These bits can assume the following values:

0000 = divide by 16
0001 = divide by 1
0010 = divide by 2
0011 = divide by 3
0100 = divide by 4
0101 = divide by 5
0110 = divide by 6
0111 = divide by 7
1000 = divide by 8
1001 = divide by 9
1010 = divide by 10
1011 = divide by 11
1100 = divide by 12
1101 = divide by 13
1110 = divide by 14
1111 = divide by 15



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**Bits 7 through 4: FOUT Source**

Determines which of the 16 possible sources is to be used as the source input to the Programmable Divider. The source is set to the 5MHz internal oscillator (F1) at reset. These bits can assume the following values:

0000 = F1
0001 = Source 1
0010 = Source 2
0011 = Source 3
0100 = Source 4
0101 = Source 5
0110 = Gate 1
0111 = Gate 2
1000 = Gate 3
1001 = Gate 4
1010 = Gate 5
1011 = F1
1100 = F2
1101 = F3
1110 = F4
1111 = F5

**Bits 3 and 2: Compare 1 and 2 Enable**

Determines whether the comparator output is substituted for the normal counter/timer output on counter/timers 1 and 2 respectively. The comparators are disabled at reset. These bits can assume the following values:

0 = comparator disabled
1 = comparator enabled

**Bits 1 and 0: Time-of-Day Mode**

Enables/disables the Time-of-Day option. The Time-of-Day option is disabled at reset. These bits can assume the following values:

00 = Time-of-Day disabled
01 = Time-of-Day enabled; ÷ 5 input
10 = Time-of-Day enabled; ÷ 6 input
11 = Time-of-Day enabled: ÷ 10 input



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## Counter "x" Mode Register

The Counter "x" Mode register is a 16-bit register that controls the operating mode of each counter/timer by selecting the gating, type of counting, output, and input source to each counter/timer. Figure 7 illustrates the Counter "x" Mode register bit functions.

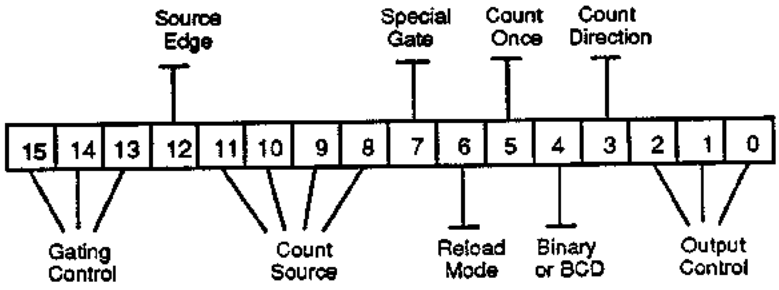



**Figure 7: Counter "x" Mode Register Bit Functions**

### Bits 15 through 13: Gating Control

Determines which of the 8 possible gate options is to be used for the counter/timer. The counter/timer is set to "no gating" at reset. These bits can assume the following values:

000 = no gating
001 = active high TCN–1
010 = active high level Gate N+1
011 = active high level Gate N–1
100 = active high level Gate N
101 = active low level Gate N
110 = active high edge Gate N
111 = active low edge Gate N



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**Bit 12: Source Edge**

Determines whether the counter/timer counts on the rising or falling edge of the source. The counter/timer is set to count on the rising edge at reset. This bit can assume the following values:

0 = count on rising edge
1 = count on falling edge

**Bits 11 through 8: Count Source**

Determines which of the 16 possible sources is to be used as the input to the counter/timer. The counter/timer is set to use the internal 5MHz oscillator as its source at reset. These bits can assume the following values:

0000 = TCN–1
0001 = Source 1
0010 = Source 2
0011 = Source 3
0100 = Source 4
0101 = Source 5
0110 = Gate 1
0111 = Gate 2
1000 = Gate 3
1001 = Gate 4
1010 = Gate 5
1011 = F1
1100 = F2
1101 = F3
1110 = F4
1111 = F5

**Bit 7: Special Gate**

Controls hardware retriggering. The counter/timer is set for no hardware retriggering at reset. This bit can assume the following values:

0 = disable hardware triggering
1 = enable hardware triggering



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**Bit 6: Reload Mode**

Determines whether the counter/timer reloads from the Load or Hold registers at terminal count. The counter/timer is set to reload from the Load register at terminal count at reset. This bit can assume the following values:

0 = reload from Load register
1 = reload from Load or Hold register

**Bit 5: Count Once**

Determines whether the counter/timer counts to terminal count once or repetitively. The counter/timer is set to count once to terminal count at reset. This bit can assume the following values:

0 = count once
1 = count repetitively

**Bit 4: Binary or BCD**

Determines whether the count occurs in binary or BCD. The count is set to binary at reset. This bit can assume the following values:

0 = binary count
1 = BCD count

**Bit 3: Count Direction**

Determines whether the counter/timer will count up or down. It is set to count down at reset. This bit can assume the following values:

0 = count down
1 = count up



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**Bits 2 through 0: Output Control**

Determines whether the counter/timer output at terminal count is inactive, a pulse, or a toggled level. If it is a pulse, the pulse can be selected to be high or low. The pulse width is one cycle of the clock source to the counter/timer. The counter/timer output is inactive at reset. These bits can assume the following values:

000 = inactive, output low
001 = active high pulse
010 = toggled output
011 = illegal
100 = inactive, output high – impedance
101 = active low pulse
110 = illegal
111 = illegal

## Counter "x" Load Register

The Counter "x" Load register is a 16-bit register that controls the effective length of the counter/timer. Any 16-bit value is legal. This value can be transferred to the counter each time Terminal Count (TC) occurs or on a Load command.

## Counter "x" Hold Register

The Counter "x" Hold register is a 16-bit register that can function in two ways: (1) it can be used in the same way as the Counter "x" Load register, alternately loading its contents into the counter at TC with the Load register; or (2) it can store accumulated counter values for later transfer to the host processor.

## Alarm "x" Register

The Alarm "x" register is a 16-bit register associated with counter/timers 1 and 2. It controls the comparator output when the comparator is enabled. Any 16-bit value can be written to this register. When the value in the counter reaches the value in the Alarm register, the comparator output goes true and appears on the Output pin for that counter/timer. The output remains true as long as the comparison is true.



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## Control/Status Register

***Address: I/O Base + 4*** ***Access: Read/Write***

The Control/Status register controls DT2919 functions not performed by the Am9513A. This register performs the following **control** functions:

- Selects a 5MHz or 1MHz frequency input to the Am9513A
- Enables or disables the software interrupt enable for the DT2919 external interrupt input
- Enables or disables the output-enable for Port 0 and Port 1
- Enables or disables the latch-enable for data input on Port 0

This register also reports the following **statuses:**

- Am9513A recovery
- Receipt of interrupt signal
- Latching of data into Port 0

Figure 8 illustrates the bit functions for the Control/Status register.

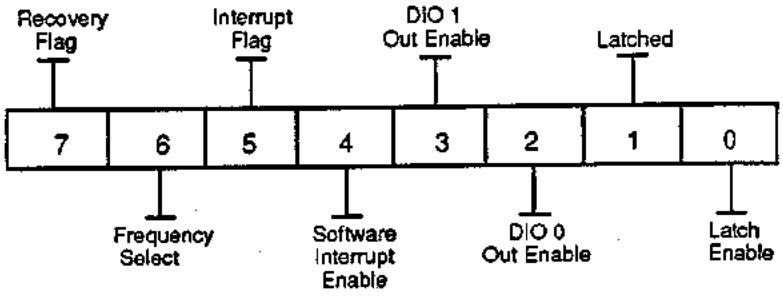



**Figure 8: Control/Status Register Bit Functions**



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## Bit 7: Recovery Flag

Determines when the Am9513A is ready for another read or write. The Am9513A needs a 1.5µs recovery time between each read and write. This bit sets to 1 for 1.5µs after each read or write to the Am9513A. This bit is clear when the Am9513A registers can be read or written to. This bit must be monitored between reads or writes to the Am9513A in order to determine when it is in the ready state.

**READ:** 0 = Am9513A available for reading or writing
1 = Am9513A recovery in progress

**WRITE:** ignored

## Bit 6: Frequency Select

Selects a 5MHz or 1MHz frequency input to the Am9513A. The 5MHz frequency input is selected when this bit is clear. The 1MHz frequency input is selected when this bit is set. This bit is cleared at power-up.

**READ:** currently selected frequency input to the Am9513A

**WRITE:** 0 = 5MHz frequency input
1 = 1MHz frequency input

## Bit 5: Interrupt Flag

Indicates whether a high-to-low transition has occurred on the Interrupt/ line at the J1 connector. This bit sets when a transition occurs while interrupts are enabled. This bit clears when the interrupt is serviced. This bit is cleared at power-up.

**READ:** 0 = external interrupt signal has not occurred
1 = external interrupt signal has been received

**WRITE:** ignored



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## Bit 4: Software Interrupt Enable

Enables/disables software control of recognition of the external interrupt signal to the DT2919. When this bit is set and the Interrupt Enable line is high, the DT2919 will generate an interrupt when a high-to-low transition occurs on the Interrupt/ line. When this bit is clear, the DT2919 does not recognize a signal on the Interrupt/ line. Clearing this bit also clears the interrupt. This bit is cleared at power-up.

**READ:** current Software Interrupt Enable status

**WRITE:** 0 = interrupt cleared and disabled
1 = interrupts enabled (if the Interrupt Enable line is also high)

## Bit 3: DIO 1 Out Enable

Controls the direction of data flow on Port 1. When set, Port 1 is output-enabled. When clear, Port 1 is input-enabled. This bit is cleared at power-up.

**READ:** current output-enable status of Port 1

**WRITE:** 0 = read-only
1 = output-enabled

## Bit 2: DIO 0 Out Enable

Controls the direction of data flow on Port 0. When set, Port 0 is output-enabled. When clear, Port 0 is input-enabled. This bit is cleared at power-up.

**READ:** current output-enable status of Port 0

**WRITE:** 0 = read-only
1 = output-enabled



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## Bit 1: Latched

Indicates when data has been latched in on Port 0 and is ready for reading when Port 0 has been latch-enabled. This bit sets when the Port 0 Latched/ line sets on a high-to-low transition on the Port 0 Strobe/ line. This bit resets to 0 when Port 0 is read.

***Note*** *This bit will only set if bit 0 (Latch Enable) is also set.*

**READ:** 0 = Port 0 is ready for more data
1 = data is available for reading on Port 0

**WRITE:** ignored

## Bit 0: Latch Enable

Enables/disables the latching in of data on Port 0. When this bit is set, Port 0 is latch-enabled and data latches in on a high-to-low transition on the Port 0 Latched/ line.. A read of Port 0 returns the value latched in. When this bit is clear, Port 0 is not latch-enabled and a read of Port 0 returns the value on the DIO lines for Port 0 at the time of the read. This bit is cleared at power-up.

**READ:** current latch-enable status of Port 0

**WRITE:** 0 = Port 0 not latch-enabled
1 = Port 0 latch-enabled



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## Port 0 Data Register

***Address: I/O Base + 2*** ***Access: Read/Write***

The Port 0 Data Register receives 8-bit digital data to be transferred from an external device to user memory (or from user memory to an external device). These eight bits are associated with Port 0 on the DT2919. This port is always readable and is output-disabled at reset. This port is output-enabled via a control bit (bit 2) in the Control/Status register.

In the input-enabled mode, a read of the DIO lines for Port 0 results in a read of any external device connected to those DIO pins on J1. If no device is connected, a read returns all floating outputs for these bits.

The Port 0 DIO lines also have an input latch with a strobe line. If the latch is enabled, data is latched in when a high-to-low transition occurs on the Port 0 Strobe/ line. A signal called Port 0 Latched/ is brought out to J1 and to the Control/Status register to indicate when data has been latched. When the data is read, the Port 0 Latched/ line sets to indicate another data value can be latched.

When a port is output-enabled, a write to that port outputs that value immediately to an external device connected to the Port 0 DIO lines at the J1 connector. A read of an output-enabled port reads back the data previously written to that port.



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## Port 1 Data Register

***Address: I/O Base + 3*** ***Access: Read/Write***

The Port 1 Data Register receives 8-bit digital data to be transferred from an external device to user memory (or from user memory to an external device). These eight bits are associated with Port 1 on the DT2919. This port is output-disabled at reset. This port is output-enabled using a control bit (bit 3) in the Control/Status register.

Reads of this register in the input-enabled mode return the actual value at the DIO lines for Port 1 at the J1 connector. There is no input latch for this port.

When this port is output-enabled, a write to this port outputs that value to a connected external device immediately. A read of this port when output-enabled returns the data last written to this port.



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## Clear Interrupt Register

***Address: I/O Base + 5*** ***Access: Write Only***

The Clear Interrupt register allows you to clear an interrupt without disabling it. The DT2919 recognizes a high-to-low transition on the Interrupt/ line as an interrupt signal when it is software-enabled for interrupts and the Interrupt Enable line is high. Writing any value to this register clears the interrupt and leaves the DT2919 in an interrupt-enabled state.

***Note*** *For alternative methods of clearing interrupts and for more detailed information on the interrupt feature, refer to the section entitled "Interrupt Operation" earlier in this chapter.*



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# Basic Operational Sequences

This section summarizes the steps for programming your DT2919 board to perform the following operations:

- Initializing the DT2919
- Programming a Counter/Timer
- Performing Digital I/O Operations
- Generating and Clearing Interrupts

**Note** *Refer to the section entitled "The DT2919 Registers" earlier in this chapter for a detailed description of each of the registers mentioned in these programming sequences.*



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## Initializing the DT2919

The following procedure describes how to place the DT2919 board in a known state:

1. Write 00 (hex) to the Control/Status register (I/O base + 4).

   This value sets Ports 0 and 1 for input and disables latching for Port 0. This value also clears the Software Interrupt Enable bit.

2. Clear the Am9513A by writing FF (hex) to the Command register (I/O base + 1).

   This value resets the Am9513A, disabling all five counter/timers. (The counter values are not reset.) In addition, this value causes the Am9513A to load 0B00 into each Counter Mode register, and 0000 into the Master Mode and the Load and Hold registers for each counter/timer.

   The Master Mode register is initialized to the following:

   - Time-of-Day option disabled
   - Comparator Enables for Counters 1 and 2 disabled
   - Frequency Out (FOUT) source set to F1 (5MHz internal oscillator)
   - Binary division for programmable scaler
   - Data Pointer incrementing
   - 8-bit bus width
   - Frequency Out (FOUT) on

   The Counter Mode registers are initialized to the following:

   - Output low, inactive
   - Count down
   - Binary counting
   - Count once
   - Reload counter from Load register
   - Special gating disabled
   - Counter source set to F1 (5MHz oscillator)
   - Count on rising edge
   - No gating



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3. Monitor bit 7 (Recovery Flag) in the Control/Status register (I/O base + 4) until it clears.

4. Reset the counters to 0000 by writing 5F (hex) to the Command register (I/O base + 1).

   This value loads the contents of the Load register (0000, from step 2 above) into all five counters to ensure that any counter at terminal count is cleared.

5. Monitor bit 7 in the Control/Status register until it clears.



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## Programming a Counter/Timer

The following procedure describes how to load a value into the Load register of a counter/timer and start the counter.

1. Initialize the DT2919 board as described in the preceding section, "Initializing the DT2919".

2. Monitor bit 7 (Recovery Flag) in the Control/Status register (I/O base + 4) until it clears.

3. Select the Counter Mode register for the counter/timer to be programmed using the Load Data Pointer function of the Command register (I/O base + 1).

   For example, to select counter/timer 1's Counter Mode register, write 01 (hex) to the Command register.

4. Monitor bit 7 in the Control/Status register until it clears.

5. Specify the counter/timer's operation by writing the appropriate 16-bit value to the Data register (I/O base + 0). (Two writes are required to load this value.)

   a. Write the value for the low byte.

      For example, to enable repetitive counting, counting down, and toggled output, write 22 (hex) to the Data register.

   b. Monitor bit 7 in the Control/Status register until it clears.

   c. Write the value for the high byte.

      For example, to select the internal 5MHz oscillator as the counter source and count on the rising edge, write 0B (hex) to the Data register.

6. Monitor bit 7 in the Control/Status register until it clears.



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7. Select the Load register for the counter/timer to be programmed using the Load Data Pointer function of the Command register (I/O base + 1).

   For example, to select counter/timer 1's Load register, write 09 (hex) to the Command register.

8. Monitor bit 7 in the Control/Status register until it clears.

9. Write the Load register's value to the Data register (I/O base + 0). (Two writes are required to load this value.)

   a. Write the value for the low byte.

      For example, to produce a 50kHz output pulse, write 32 (hex) for this value.

   b. Monitor bit 7 in the Control/Status register until it clears.

   c. Write the value for the high byte.

      For example, write 00 (hex) for this value. A value of 0032 produces a 50kHz square wave output in the toggle mode.

10. Monitor bit 7 in the Control/Status register until it is clear.

11. Load and arm the counter/timer via the Command register (I/O base + 1).

    The load-and-arm command loads the counter with the value in the Load register and gates the counter operation on. The counter/timer counts down until terminal count is reached. Depending on how the counter/timer is programmed, the counter outputs a pulse or toggles the output and the counter is reloaded with the Load or Hold register value. If repetitive counting is enabled, another count cycle occurs.

    In this example, write 61 (hex) to the Command register to load and arm counter/timer 1. Counter/timer 1 immediately begins counting and produces a 50kHz toggled output.



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## To Calculate the Load Register Value for Generating a Frequency Output

These values are calculated for binary counting. The counter is set for counting down.

**Non-toggle Mode:**

**X = (Source / (Frequency at Output "x")**

X = Load register value
X cannot equal 1; if X = 0, divider value = 65536
If X = (2,3,4...65535), divider value = (2,3,4...65535)

Example: Frequency at Output "x" = 100kHz
Source = 5MHz

X = 5000000/100000
X = 50 (decimal)

Convert the Load register value to hex before writing it to the register. In this example, the Load register value becomes 0032.

**Toggle Mode:**

**X = (Source / (Frequency at Output "x" * 2))**

X = Load register value
X can equal 1, but the base frequency is divided by 2
If X = 0, divider value = 65536, the frequency is twice the divider value

Example: Frequency at Output "x" = 100kHz
Source = 5MHz

X = (5000000 / (100000 * 2))
X = (5000000 / 200000)
X = 25 (decimal)

Convert the Load register value to hex before writing it to the register. In this example, the Load register value becomes 0016.

***Note*** *When* TCN–1 *is used as the source, and counter* N–1 *is in toggle mode, each toggle is a terminal count.*



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## Performing Digital I/O Operations

Digital data can be transferred between a device connected to the digital I/O lines at the J1 connector for Ports 0 and 1 and user memory. Data input to Port 0 can be read at any time or latched in. Data input to Port 1 can be read at any time. Each port is separately output-enabled.

### To Input Digital Data From an External Device (Port 0: Latch Disabled)

1. Set the port for input:
   - Set Port 0 for input by clearing bit 2 (DIO 0 Out Enable) and bit 0 (Latch Enable) in the Control/Status register (I/O base + 4).
   - Set Port 1 for input by clearing bit 3 (DIO 1 Out Enable) in the Control/Status register (I/O base + 4).
2. Read the Port 0 Data register (I/O base + 2) or Port 1 Data register (I/O base + 3) to transfer the value from the external device to user memory.
3. Repeat step 2 as desired.



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## To Input Digital Data From an External Device (Port 0: Latch Enabled)

1. Set Port 0 for input and enable latching by setting the appropriate bits in the Control/Status register (I/O base + 4).

   - Set Port 0 for input by clearing bit 2 (DIO 0 Out Enable).
   - Enable latching by setting bit 0 (Latch Enable).

2. Connect an external strobe to the Port 0 Strobe/ and Port 0 Latched/ lines at the DT2919's J1 connector (J1, pins 21 and 22, respectively).

   Data latches into Port 0 when a high-to-low transition occurs on the Port 0 Strobe/ line.

3. Monitor bit 1 (Latched) in the Control/Status register (I/O base + 4) until it sets.

   When this bit sets, data has been latched into Port 0.

4. Read the Port 0 Data register (I/O base + 2).

   This read clears bit 1 (Latched) in the Control/Status register and signals the external device (via the Port 0 Latched/ line) that the data has been transferred to user memory and that new data may be latched in.

5. Repeat steps 3 and 4 as desired.



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## To Send Digital Data to an External Device

1. Set the selected port for output by setting the appropriate bits in the Control/Status register (I/O base + 4).
   - Set Port 0 for output by setting bit 2 (DIO 0 Out Enable).
   - Set Port 1 for output by setting bit 3 (DIO 1 Out Enable).
2. Write the value to be output to the Port 0 Data register (I/O base + 2) or Port 1 Data register (I/O base + 3) .

   This value is output immediately to the external device connected to that port's DIO lines.
3. Repeat step 2 as desired.

Data output to the external device from Port 1 can be read back at any time. Data output from Port 0 can be read back at any time when the latch is disabled.



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# Generating and Clearing Interrupts

The interrupt signal to the DT2919 may come from any device connected to the Interrupt/ line on the J1 connector (J1, pin 1). The interrupt priority level is POS-configurable.

## To Generate an Interrupt

1. Connect the signal for the interrupt to the Interrupt/ line on the J1 connector.

2. Enable the interrupt (it must be both software- and hardware-enabled).

   *To software-enable the interrupt:*

   - Set bit 4 (Software Interrupt Enable) to 1 in the Control/Status register (I/O base + 4).

   *To hardware-enable the interrupt:*

   - If you wish to have a signal from an external device determine when the interrupt should be enabled, connect a device which drives the line high to the external Interrupt Enable line at the J1 connector.

     ***Note*** *The Interrupt Enable line must be driven high in order to enable the interrupt.*

   - OR, if you do not connect a device to this line, the DT2919 pulls this line high so the interrupt is hardware-enabled.

3. An interrupt occurs when the external device generates a high-to-low transition signal on the Interrupt/ line.

   The edge generates the interrupt.



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## To Clear an Interrupt

- To clear the interrupt and leave it enabled, write any value to the Clear Interrupt register (I/O base + 5).

- To clear the interrupt and disable interrupt generation:

  *To software-disable interrupt generation:*

  - Clear bit 4 (Software Interrupt Enable) in the Control/Status register (I/O base + 4).

  *To hardware-disable interrupt generation:*

  - To hardware-disable interrupt generation, drive the external Interrupt Enable line low. This disables and clears interrupts.



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