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ANDOR DESIGN CORP



CIC101-4
MIL-STD-1553 A, B, McAir MULTI PROTOCOLS Simulator/Analyzer/Tester

1/2 Size ISA Bus Interface Card

FEATURES

*** SUPPORTS VALIDATION/PRODUCTION TEST PLANS.**
*** 1/2 SIZE PC CARD.**
*** SIMULTANEOUS BC, MULTIPLE RTS, MONITOR.**
*** 1553A. B, McAir AND USER DEFINED PROTOCOLS.**
*** FULL ERROR DETECTION AND GENERATION.**
*** ON BOARD MAJOR/MINOR FRAME TIMING.**
*** PROGRAMMABLE MESSAGE PARAMETERS.**
*** PROGRAMMABLE OUTPUT AMPLITUDE.**
*** SOFTWARE WITH SOURCE CODE INCLUDED.**
*** 256 KBYTE DUAL PORT, FAST, STATIC RAM.**

DESCRIPTION

The CIC101 is a full-featured, high performance, Dual Redundant MIL-STD-1553A/B serial bus Simulator Analyzer Tester designed as a plug in card for ISA or compatible backplane. The CIC101 includes full error injection and can operate in independent or simultaneous mode as a Bus Controller, multiple simulated Remote Terminals and full/selective Monitor. Its data structure can be changed on the fly without interrupting the processor for real time operation. The active monitor stores bus traffic in a monitor Buffer. Stored messages are time tagged and annotated with the bus message type and any detected errors. Stored words are annotated with a break down of the word error.

DATA FILTERING

The CIC101 data filter looks at the complete command rather than just addresses and sub addresses. The user designate individual Messages to be ignored, monitored, replied to or monitored and replied to.

APPLICATIONS

The CIC101 can be used for Validation Testing, Production Testing, full bus simulation and monitoring, as a general purpose 1553 interface or a stand alone bus Analyzer. It provides precise message scheduling and measurements. Major and minor frame times are independent of message sequences or retransmissions on errors. The start of all command messages may be set to be independent of message length, response time or length of response. The CIC101 features a calibrated Message timing and low jitter RT responses.

GENERAL SPECIFICATIONS	
Parameter	Value
1553 SRAM	128K x 16
Major Frame Count	1 to 32768, Continuous
Major Frame Size	1 to 1024 Minor Frames
Minor Frame Time	0 to 419/4190 msec
Minor Frame Size	0 to 32766 Commands
BC Messages	0 to 2048
Message intervals	2 to 6400 usec. in .1 usec. steps
Response timeout	2 to 33 usec. in .5 usec. steps
Response Time jitter	2 to 33 usec. in .5 usec. steps 50ns Max
Retry on Error	Same or alternate bus
Internal time tag	16 bits, 6.4 or 64 usec. steps 32 bits, 1.0 usec steps

WORD ERROR INJECTION/DETECTION
- Low bit count (1, 2)
- High bit count (1, 2, 3)
- Parity error
- Manchester low
- Manchester high
- Inverted Sync
- Zero crossing deviation (+/- 150 nsec, External)

MESSAGE ERROR INJECTION/DETECTION
- Format
- No response/Late response
- Sync
- Non contiguous data (2 microsec.)
- Word count error
- Data on two channels
- Status word
- Invalid Word

MAXIMUM RATINGS	
Parameter	Value
Temperature Range	
Operating	0 to +70 Deg. C
Storage	-65 to +150 Deg. C
Power supplies	
+5 Volts +/- 5%	0.5 Amps Max
Physical characteristics	
1/2 Size ISA card	4.5 x 6.5 x 0.44 inches

SOFTWARE
The CIC101 comes with software drivers for DOS and windows 98/NT/2000/XP. A set of well-documented API's with source code written in "C" and "C# "is included.

STAND ALONE OPERATION
A menu driven user interface is included for stand-alone operation. With this program the user can set up 1553 traffic, simulate RT'S responses, monitor all or selected traffic in real time and capture data using trigger and search arguments.

SWITCH PROGRAMMABLE
- Time Tag resolution
- I/O channel address
- Interrupt level

CIC101 OPERATION
The CIC101 processes 1553 messages with a minimum attention from the CPU. The user need only write a set of command Blocks, a message list and number of messages to define a minor frame. He writes a minor frame time, the number of minor frames per major frame and a minor frame list to define a major frame. The bus controller sends the major frame a number of times as programmed in the major frame count, without any further attention from the CPU.

In the Remote Terminal mode, the user writes a set of command Blocks, a look-up table for the CIC101 to respond autonomously to incoming messages. In both modes an active monitor analyzes, annotates and stores bus traffic in a monitor Buffer.

1553 OUTPUT
- Direct coupling
- Transformer stub coupling

TIMING
The CIC101 will normally return an I/O channel ready to the CPU in 50 to 100 nanoseconds. This time is extendible to 900 nanoseconds if the CIC101 is processing a MIL-STD-1553 message.

COMPUTER INTERFACE
The CIC101 operates as a 16-bit I/O channel slave device. It generates interrupt flags to show completion of a frame in the BC mode, receipt of a specified message, receipt of a specified Data word, receipt of a specified Status word, detected message errors or triggers.

A Dual ported, I/O Mapped, static RAM serves as the intermediate for data exchange with the 1553 bus. An auto incrementing address register serves to hold the initial RAM Address and increments after each data transfer. Two additional registers control the mode of operation. Both the registers and the RAM can be loaded with new data while a message is being transmitted over the 1553 channel for real time applications. Essentially, programming the CIC101 consists of transferring data to or from the RAM.

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Data Sheet, Mar 1, 2007

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