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IP-COMM360

Intelligent IndustryPack® with MC68360 QUICC CPU

Features

- MC68360 Quad Integrated Communication Controller (QUICC) @ 25 MHz
- Four serial communication controllers
- 14 dedicated DMA channels, two general purpose DMA channels
- 2 Mbytes (1 Mbyte optional) of 32-bit wide dual-port dynamic RAM @ one wait state
- 256 Kbyte volatile 16-bit wide SRAM @ one wait state for boot and application code
- 256 Kbyte 16-bit wide Flash memory @ two wait states for boot and application code
- Dual mailbox interrupts for host<—>68360 communication
- Asynch, SDLC/HDLC, Bisync, DCMP, V.14, X.21, Ethernet/IEEE 802.3, ISDN (2B+D channels).
- Physical layer implemented with transition modules
- Single-high IndustryPack, type II (components on back)

IP-COMM360 places the powerful 25 MHz Motorola MC68360 communication processor onto a single-wide IndustryPack®. The 68360 provides four sophisticated communication channels, including DMA to the local dual-port DRAM and SRAM. IP-COMM360 occupies 8 Mbytes of host address space.

A variety of physical layer standards, such as RS-232-D, RS-422, ISDN, Ethernet/IEEE 802.3, X.21, and V.14 are supported by the use of transition modules. The architecture makes it easy for customers to implement special physical interface requirements by substituting their own transition module.

Internal microcode in the 68360 supports a variety of protocols: Asynch, SDLC/HDLC, Bisync, DCMP, V.14, X.21, ISDN (2B+D channels). Some protocols require additional software available from Motorola.

The 68360 contains a 32-bit CPU32+ core processor, a microcoded RISC communications processor, 14 dedicated DMA channels, two general purpose DMA channels, four timers including a tick timer (for a local kernel) and watchdog timer, an interrupt controller, four high performance serial channels, internal memory, and a conventional parallel 68000 bus interface as well as an expandable serial interface.

The IndustryPack implements 256 Kbyte dual-port SRAM (0 KB SRAM optional) and 256 Kbyte dual-port Flash memory for boot and application code. The Flash memory may be used in lieu or in addition to the SRAM. The boot code is installed into the Flash or SRAM by the host before reset is removed from the 68360. The IndustryPack also implements 2 Mbytes (one optional) of high speed dynamic RAM as dual-port memory for both 68360 code and communications data.

A pair of mailbox supports interrupts in both directions: host to 68360 and 68360 to host. The dual-port memory may be easily partitioned to support arbitrarily complex inter-processor communication.

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Specifications

Form Factor	Single-wide Type II IndustryPack
IndustryPack Interface	Complies with ANSI/VITA-4
Number of Serial Ports	4
Signals Supported	RXD, TXD, RXC, TXC, CD, CTS, RTS, BRG??
CPU	MC68360 (QUICC) at 25 MHz
Memory	256 Kbytes SRAM (none on –25-1) 256 Kbytes Flash 1 Mbyte (-25-1) or 2 Mbyte (others) DRAM All memory is dual-ported between CPU and host system
BDM Port	Fitted on –25-2D variant only
Crystal	32768 Hz feeds CPU PLL for clock and baud rate generation
Baud Rates	Up to 2 Mb/s sync, depending on protocol and interface Up to 10 Mb/s for Ethernet
DMA	14 channels dedicated, 2 general purpose
Timers	Four, 16 bit
ESD Protection	33 Ohm resistors on all I/O
Interrupts	Maskable, vectored. Host can interrupt CPU. CPU can interrupt host.
Dimensions	1.8 inches x 3.9 inches
Power Requirements (no load)	+5 VDC, 350 mA typ; +12 VDC, 0 mA typ; -12 VDC, 0 mA typ
Environmental	Operating temperature: 0° to +70°C. Storage temperature: –40° to +85°C Humidity: 5% to 95% non-condensing

Order Information

IP-COMM360-25-2	Serial communication IndustryPack with MC68360 QUICC @ 25 MHz, with 256 K SRAM, 256 K Flash, 2 Mbyte DRAM
XM-360-4	4 channel EIA-422 transition module for IP-Comm360 with 6U front panel, HD26
XM-360-16	16 channel EIA-422 transition module for 4 IP-Comm360s with 6U front panel, RJ45
C-HD50M-HD50M	6-foot HD50 male to HD50 male cable
C-HD50M-CM50M	6- foot Champ50 male to HD50 male cable
IP-TERM	50-screw terminal block with ribbon connector
IP-TERM-HD50	50 screw terminal block with HD50 female connector

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