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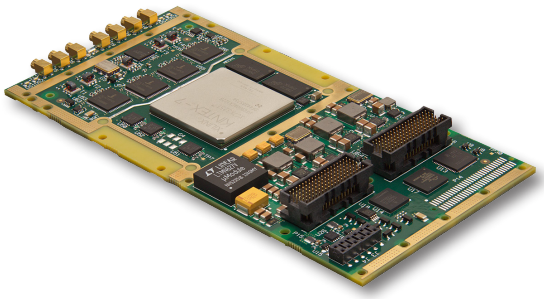
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XF07-516

4x 250 MSPS 16-bit Analog I/O XMC Xilinx® Kintex™ XC7K325T FPGA

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Key Features

- Quad channel 250 MSPS 16-bit analog inputs
- Xilinx user programmable Kintex-7 XC7K325T FPGA
- 2 x banks of 16b x 128M DDR3 SDRAM (total 512 Mbytes)
- XMC format
- Embedded DDC IP option
- VxWorks® and Linux® host support
- Air- and Conduction-cooled variants

Applications

- Radar
- SIGINT/ELINT
- Electronic Warfare (EW)

Overview

The XF07-516 is a high-speed quad channel 250 MSPS analog input XMC format mezzanine card, with a user programmable FPGA for combining data acquisition and user algorithms. The combination of direct high-speed analog I/O and next generation FPGA processing makes the XF07-516 ideal for demanding applications including radar, imaging and test equipment within commercial and defense market spaces.

The XF07-516 is a member of Curtiss-Wright's XF07 XMC family of products based on the Xilinx® Kintex®-7 XC7K325T FPGA. The XF07 family includes fiber-optic and analog I/O variants based on a common FPGA processing and interface building block.

Analog Input

The XF07-516 provides four synchronously sampled analog input channels connected through front panel (or bulkhead for conduction-cooled) connectors. Each analog input is AC coupled to an Intersil™ ISLA216P25 ADC and is able to sample at up to 250 MSPS with an analog input bandwidth of up to 340 MHz.

An onboard user programmable sample clock generator is provided for a complete integrated acquisition solution. Alternatively, the sample clock can be derived from either a 10 MHz or direct RF external clock source. The Kintex-7 FPGA controls the choice of clock source.

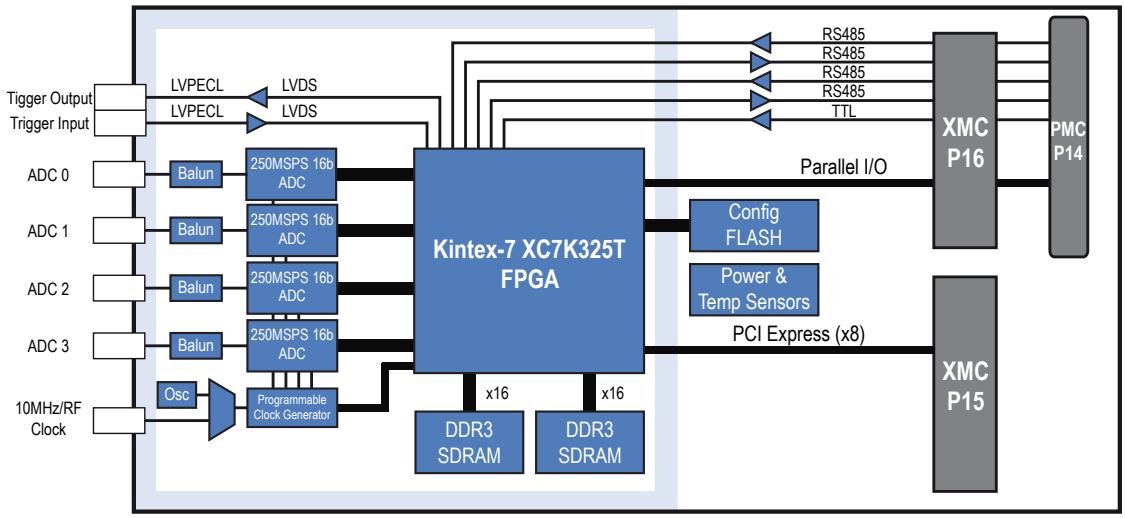


Figure 1: XF07-516 block diagram

Specifications

FPGA

- Device: Xilinx Kintex-7 K325T (speed grade 2)
- Configuration: Over PCI Express® (PCIe) interface
  - 1 Gbit Flash (FPGA boot/configuration including recovery image)
  - JTAG/ChipScope™ Pro port

Analog input

- Number of channels: 4, single-ended
- Sampling frequency: Up to 250 MSPS
- Full scale input: 12 dBm @ 40 MHz
- ADC devices: Intersil ISLA216P25
- Analog bandwidth: 340 MHz
- SFDR: 73 dBc
- SNR: 66 dBFS
- ENOB: 10.3 bits
- Input Impedance: 50 Ohm, AC coupled
- Input connector: Front panel MMCX

Clock and trigger inputs

- Clock input connector: Front panel MMCX
- Clock input: 50 Ohm, AC coupled LVPECL
- Clock input frequency: 10 MHz (reference) or 80-250 MHz (RF)
- Internal clock: Programmable (derived from 10 MHz external source or internal): Si571 VCXO
- Trigger input/output: Single-ended, 50 Ohm, LVPECL buffered to host FPGA

Rear I/O (build option)

- PMC/XMC digital I/O
  - 20 x differential pairs + 38x single-ended (XMC)
  - 32 x differential pairs (PMC)
  - Note:
    - PMC and XMC digital I/O are mutually exclusive build options
    - 1 x signal is input TTL and 4 x RS-485 buffered (2 x input pairs and 2 x output pairs)
- Connector: XMC P16 or PMC P14 (build options)

Memory

- Type: DDR3 SDRAM
- Capacity:
  - Total: 512 MB
  - Arranged as two banks, each 128M x 16-bit
- Bandwidth: >2 Gbytes/sec

XMC interface

- Compliance: VITA 42.0
- XMC P15:
  - 8 x GTX or
  - x4/x8 PCIe

Software/HDL

- Support/Utilities
  - FusionXF development kit
  - FPGA/flash programming, diagnostics
- Host drivers
  - VxWorks 6.x (contact factory for availability),
  - Linux (Fedora) 15
- HDL examples: Memory interfaces, PCIe, data DMA
- Acquisition: Digital receiver ADC application mode

Miscellaneous

- Weight:
  - Air-cooled: 218 g
  - Conduction-cooled: 170 g
- Minimum airflow rates
  - Air-cooled Level 0 variants: 15 CFM 0 to 50°C air-inlet temperature
  - Air-cooled Level 100 variants: 20 CFM -40 to +71°C air-inlet temperature
  - See Curtiss-Wright ruggedization levels for more details

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TABLE 1	FPGA resources
Slices	50,950
Logic cells	326,080
CLP flip-flops	407,600
Total Block RAM (Kbits)	16,020
DSP48E1 slices	840

Note: Kintex-7 devices are a member of Xilinx's 28nm 7-Series family which also includes Artix-7 and Virtex-7 members.

Triggers, Synchronization and Digital I/O

'Trigger In' and 'Trigger Out' signals are routed to the front panel. The functionality of these signals is dependent on the HDL code and therefore may be retargetted. Both 'Trigger In' and 'Trigger Out' are single-ended LVPECL buffered signals connected to the host FPGA. It is possible to synchronize the ADCs on multiple XF07-516s using the 'Trigger In' & 'Trigger Out' signals with appropriate HDL code; effectively the function of these signals is changed to a sync mode when this is required.

Up to 64 digital I/O signals are provided through the PMC P14 connector and directly controlled by the Kintex-7 FPGA for general purpose I/O. The majority of signals are 3.3V differential signals, but RS-485 and TTL compliant I/O is also provided. These are available for the user application and can be used for user defined functions as secondary triggers, PPS inputs or any other function. As an alternative build option to PMC P14 I/O, up to 78 digital I/O signals are provided to an XMC P16 connector. I/O to PMC P14 and XMC P16 is mutually exclusive.

Xilinx Kintex-7 FPGA

The XF07-516 features a user programmable Xilinx Kintex-7 XC7K325T FPGA resource (speed grade 2, industrial temperature range). Although a Kintex-7 FPGA is a mid-range Xilinx 7-Series FPGA, it is a powerful resource compared to Virtex®-5 or even Virtex-6 previous generation devices.

The FPGA configuration images can be stored in the flash memory that can be updated and controlled by the host CPU using the PCIe interface. The FPGA can be reconfigured from images indexed in the flash including a write protected recovery configuration. FPGA configuration from flash can also take advantage of AES encryption.

Multiple Memory Banks

The XF07-516 supports two banks of 128Mx16-bit DDR3 SDRAM, each directly connected to the FPGA. As each memory bank is independently connected to the FPGA, there is great flexibility in how they may be used. Each memory bank supports read or write bandwidths of >2 Gbytes/sec.

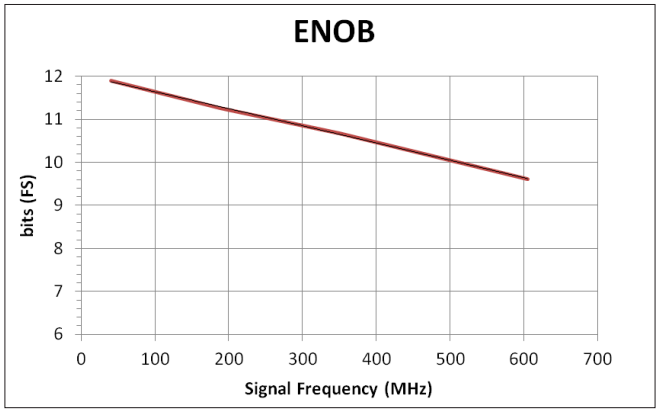


Figure 2: Typical ENOB

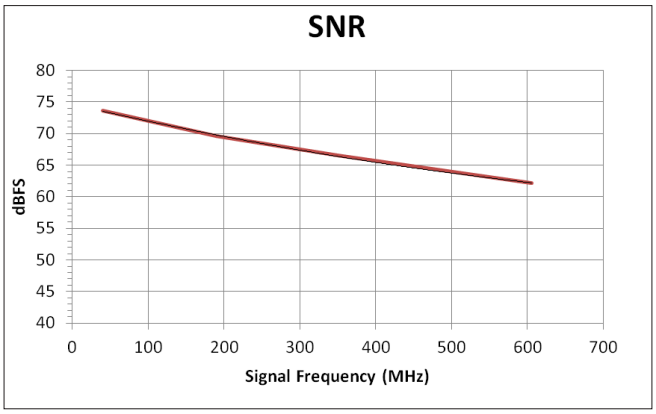


Figure 3: Typical SNR

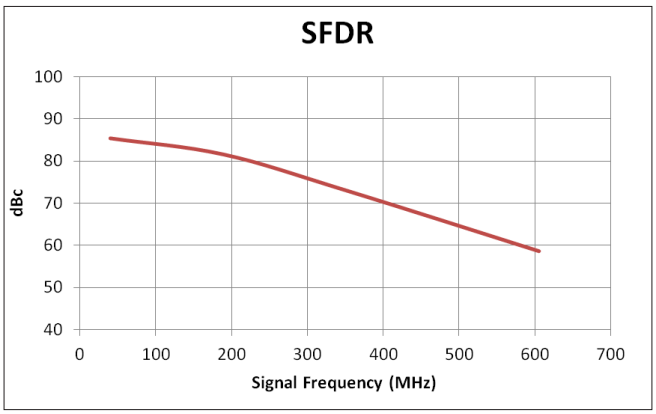


Figure 4: Typical SFDR

PCIe and Multi-GB/s I/O

The XF07-516 supports a x4/x8 PCIe channel through the primary XMC P15 connector using the FPGA's built-in PCIe end-point block. Alternatively, the XMC P15 can be used to provide user defined protocol support over the data links, such as Aurora™ for higher bandwidth and lower latency operation. However, this mode would require customer HDL development for new modes.

FusionXF™ Software/HDL Support

Curtiss-Wright's FusionXF Development Kit includes software, HDL and utilities complete with examples for using the XF07-516. FusionXF includes a C programming language API, driver framework and sophisticated DMA support. One of the core elements to the FusionXF development kit is a framework for adding in new IP functionality or capabilities to the FPGA easily and effectively. FusionXF allows user applications to be associated with standard drivers, thereby speeding up application development.

Software utilities are provided for configuring the FPGA. These include flash programming and configuring the FPGA from one of multiple indexed images in stored in flash.

FusionXF supports VxWorks® and Fedora™ Linux® operating systems. Contact factory for support of alternative operating systems.

Rugged Build Options

A range of environmental requirements are addressed by the XF07-516 including commercial, air-cooled rugged and conduction-cooled.

XF07-516 Digital Down Converter

Features

- 16-bit input
- NCO with 32-bit tuning word, 120 dB SFDR
- 18-bit coefficients
- Four independent programmable coefficient sets
- Up to 2560 filter taps
- Complex or real outputs
- Decimation of 2, 4, 8, 16, 32 or 64 (complex)
- Decimation of 1, 2, 4, 8, 16 or 32 (real)
- Output formatting to 16-bits or 24-bits
- Output spectrum can be inverted or shifted by Fo/2

Overview

The DDC option for the XF07-516 is a wideband Digital Down Converter (DDC) providing similar functionality to the GC1012B from Texas Instruments. XF07-516 are available with or without embedded DDC IP examples in configuration FLASH memory. For these variants of the XF07-516, customers can use the card without needing to develop FPGA IP. For users that wish to integrate this IP into their application, a separate DRK (DDC Resource Kit) is available. Contact Curtiss-Wright for ordering information.

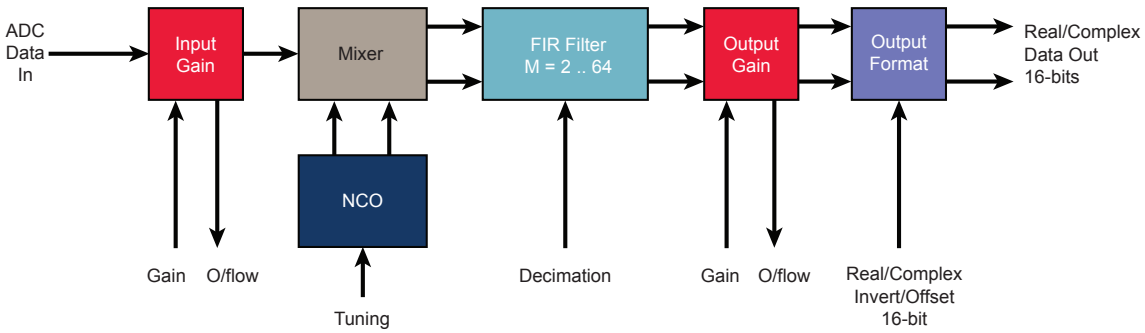


Figure 5: DDC001 block diagram

Input Gain

Permits scaling of the input signal by up to 72 dB with a granularity of 0.03 dB, the gain is specified by a 20-bit input with an 8-bit fractional part. The Input Gain Block has an overflow output, in the event of an overflow the output from this block saturates to the maximum positive or negative value as appropriate.

NCO

The NCO has a 32-bit accumulator and 21-bit outputs to the mixer and provides a 120 dB SFDR using phase dithering and Taylor series correction. The NCO also supports an 11-bit phase offset.

Mixer

The Mixer takes a real input from the Input Gain Block and multiplies it with the Cos and –Sin inputs from the NCO to produce a complex output which is passed to the Decimating FIR filter.

Decimating FIR Filter

Decimates and filters the output of the Mixer, supports decimation rates of 2, 4, 8, 16, 32 and 64. All four sets of filter coefficients are programmable; two sets are pre-programmed with coefficients supporting passbands of 80% and 90% of the output bandwidth.

TABLE 2 Characteristics of the supplied filters

FILTER PASSBAND* (of Fo/2)	PASSBAND RIPPLE	STOPBAND
80%	< 0.08 dB	> 93 dB
90%	< 0.05 dB	> 74 dB

*Note: Passband is defined as the point at which the filter attenuation exceeds the specified ripple.

TABLE 3 Number of taps for each of the decimation rates

DECIMATION RATE	FILTER TAPS
2	80
4	160
8	320
16	640
32	1280
64	2560

Output Gain

The amplitude of the output from the filter can be modified by 90 dB with a granularity of 0.03 dB. The Output Gain Block saturates in the event of overflow and indicates that an overflow has occurred on a status output.

Output Formatter

The output from the DDC can be real or complex, rounded to 24 or 16-bits, with the output spectrum inverted or offset by Fo/2.

TABLE 4 Resource usage

RESOURCE TYPE	RESOURCE USED	% OF KINTEX-7 K325T
DSP48E1	64	7
Slices	6200	2
BlockRAM	13	2

Note: The resource utilization is approximate and provided for guidance as it may change slightly as improvements are made to the design.

Ordering Information

TABLE 5 Board ordering information

PRODUCT NUMBER	ANALOG INPUTS	DIGITAL I/O	RUGGEDIZATION	COMMENT
XF07-516-A004040	4 x 250 MSPS x16b	PMC P14: 32 x DIFF	Air-cooled, Level 0	
XF07-516-A004060	4 x 250 MSPS x16b	XMC P16: 30 x DIFF + 38 x SE	Air-cooled, Level 0	
XF07-516-A104040	4 x 250 MSPS x16b	PMC P14: 32 x DIFF	Air-cooled, Level 100	
XF07-516-A104060	4 x 250 MSPS x16b	XMC P16: 30 x DIFF + 38 x SE	Air-cooled, Level 100	
XF07-516-C204040	4 x 250 MSPS x16b	PMC P14: 32 x DIFF	Conduction-cooled, Level 200	May require host front panel cut-out
XF07-516-C204060	4 x 250 MSPS x16b	XMC P16: 30 x DIFF + 38 x SE	Conduction-cooled, Level 200	May require host front panel cut-out

TABLE 6 Software, HDL and Support

PRODUCT NUMBER	COMMENT
XF07-516-XFV	› FusionXF for VxWorks › Note: common software also for use on XF07-518
XF07-516-XFL	› FusionXF for Linux (Intel CPU host – contact factory for non-Intel host support) › Note: common software also for use on XF07-518
XF07-516-DRK	DDC Resource Kit (DRK). HDL library for allowing DDC IP to be integrated in user programmable HDL environment (contact factory for availability)
JTAG-ZF5	JTAG adaptor module for use with Xilinx JTAG pod

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