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DVME-614

for DATEL's
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DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-9984
(508) 339-3000

April, 1991

UM-DVME-614

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Pressure			
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Flow			
Other			

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CAUTION

DO NOT APPLY POWER TO THIS BOARD UNTIL YOU HAVE READ THIS MANUAL

UNPACKING

This product should include a DVME board in a static-protective bag, an MS-DOS 5.25-inch, 360K program disk and a User Manual. Upon receipt, carefully remove the board from the anti-static bag and visually inspect the board for physical damage which may have occurred in shipment. In the event of damage, save all packing materials for inspection by your carrier to validate shipping damage claims. Should the board need repair at a later date, it may be safely returned in its original packing materials. If you do not intend to use the board immediately, store it in the anti-static bag until use.

CAUTION - ALWAYS STORE THE BOARD IN THE ANTI-STATIC BAG

This board contains components that can be damaged by static discharge and should be handled with caution. Make sure your body is grounded before handling the board, especially in dry, low humidity conditions. Avoid board contact with clothing having a high synthetic content. Avoid contact after walking across carpeting. Before you first touch the board, continuously hold the VME chassis that it will be installed into. In severe static discharge environments, consider grounding wrist straps or use other protective measures.

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INTRODUCTION

1.0 General Introduction

This manual contains a complete set of hardware and programming information for the DVME-614 data acquisition board, including installation, configuration, I/O connections and programming. It is designed to be a detailed guide to using the board and not as a repair manual. All specifications, pinouts and Engineering drawings are for purely information purposes and are only intended to aid in implementing individual user applications. In the event of DVME-614 failure or malfunction, DATEL recommends shipping the faulty board back to its facility in Mansfield, Massachusetts, for service and repair. Overseas customers may return boards to their nearest DATEL representatives. For users with critical downtime applications, DATEL recommends that they stock some spare boards and test them periodically.

Section 1 of this manual contains a functional description of the DVME-614 as well as a detailed list of functional specifications. Section 2 outlines the installation, setting up and calibration of the board. Section 3 deals with the programming aspect of the DVME-614, containing details of on-board registers. Section 4 explains the operation of the 82C54 Pogrammable Interval Timer and lists some example source code for configuring it. Section 5 deals with some application examples and strategies. Hardware theory and operation is covered in Section 6 and, finally, Appendix A contains a complete set of details on the operation modes of the 82C54 Timer while Appendix B contains schematics, assembly drawings and a DVME-614 product data sheet.

1.1 Implementation Procedure

The general procedure for application development is outlined below and will be expanded throughout the rest of this manual.

1. Study your host computer and its documentation to decide how the DVME-614 will be integrated in your system. You must determine the correct board slot, memory addressing, interrupt usage, software interface, etc.

2. Configure the on-board hardware (jumpers for A/D converter, PGA for DVME-614A, internal timers, interrupt procedures, memory addressing, etc.)

3. Install the board, apply power and confirm that your host computer operates normally. Do preliminary testing and initial programming. Connect analog input signals and confirm proper data.

4. Develop and debug the final software. Document the application so that it can be maintained and made readily available for applications support in the future.

1.2 General Description

Designed for parallel channel, seamless non-stop data acquisition applications, the DVME-614 is a high speed analog input board for VMEbus computers. The DVME-614 accepts analog data on up to 16 single ended input channels, with sampling rates up to 4 MHz possible. Model DVME-614A uses a Simultaneous Sample/Hold (SSH) section, thus allowing it to acquire signals on parallel channels simultaneously and then the A/D converter rapidly digitizes each held signal sequentially. Raw A/D data passes to on-board First In First Out (FIFO) data memory. The DVME-614 can continuously collect analog data with non-stop ADC triggering while data is simultaneously being read from the FIFO. The FIFO decouples the precise timing of the A/D section to conform with the block oriented data transfers to the host system bus.

Data may be transferred to mass storage devices such as magnetic tapes or disks across the host interface under host software control. Also, the raw A/D data output from the FIFO can be routed to the parallel digital output port. This enhances fast I/O throughput by making the data available to other external

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devices and processors. This parallel outport uses a universal ready/acknowledge handshake procedure which is adaptable to any remote parallel port.

There are three possible input voltage ranges; 0 to +10V, ±5V, and ±10V. To provide for very low level inputs, the DVME-614A board has Programmable Gain Amplifiers on two input channels which enable input ranges of 0 to 1V and ±1V. Gains x1 to x100 are resistor programmable on the DVME-614E. Great care must be taken that the maximum input voltage of ±10V is not exceeded. If for any reason this value is exceeded, then the A/D goes into overvoltage recovery (which typically lasts a few microseconds) yielding incorrect A/D data. If the overvoltage protection maximum of ±15V is exceeded then permanent hardware damage may occur.

A/D triggering may use several sources under software control. The primary source is the programmable interval timer which specifies the number of conversions per scan, the conversion period and the internal trigger frequency. This programmable sample counter allows sample blocks independent of FIFO length. An external trigger clock may also be used to synchronize sampling with external events. This external trigger may be digital or analog - the latter using a level-triggered comparator, the reference level of which is set by the on-board DAC. These external triggers can initiate a single sample, a single multichannel scan or a specified number of scans, separated by programmable delays.

Five A/D converter module options are available, including single channel, 12 bit, 4 MHz; 4 channel, 12 bit, 1.5 MHz and 16 channel, 12 bit, 250 KHz cards. Also available is a quad channel, 14 bit, 500 KHz option. Output coding on all modules is selectable as straight unipolar binary or as 2's complement bipolar binary. All data is right-justified, with sign extension through bit 15 for bipolar ranges.

The DVME-614 is supplied with a set of low level device driver programs in assembly language and in "C", which are adaptable to most host Operating Systems. These are available on 5.25" floppy diskette (IBM format) and include program examples that configure the DVME-614 to do single/multi-channel scans, and data transfers from the FIFO to host memory buffers or disk file. There is also a production test code listing included. Also this user manual has register and timing information to assist users in writing their own application specific routines, as well as setup and configuration examples for the 82C54 programmable interval timer.

1.3 Simultaneous Sample/Hold

The front end A/D section on the DVME-614A board differs from that on the other versions, (B, C, D, and E), in that its analog multiplexer is preceeded by four Sample/Hold amplifiers - one on each input channel. The Sample/Hold control logic is such that all four channels are strobed simultaneously. Instead of the multiplexer switching through the analog input channels directly it now switches between the sample/hold moduli. Once the signals are acquired simultaneously, they are digitized sequentially at rates up to 1 MHz. In multi-channel mode, the data throughput to the FIFO decreases to 1 megasample per second. Therefore, if sampling all four channels simultaneously, the maximum conversion rate is 1 MHz - imposing a 250 KHz maximum limit on the sample/hold trigger rate.

This Simultaneous Sample and Hold (SSH) option is ideal where up to four signals must be sampled at the same instant in time. When correlating phase related signals, SSH removes skew delay errors from conventional MUX scanning techniques. SSH is selected by setting bit 6 in the Channel Address Register and Counter Register #0 must be loaded with the number of channels to be sampled simultaneously (3 or 4).

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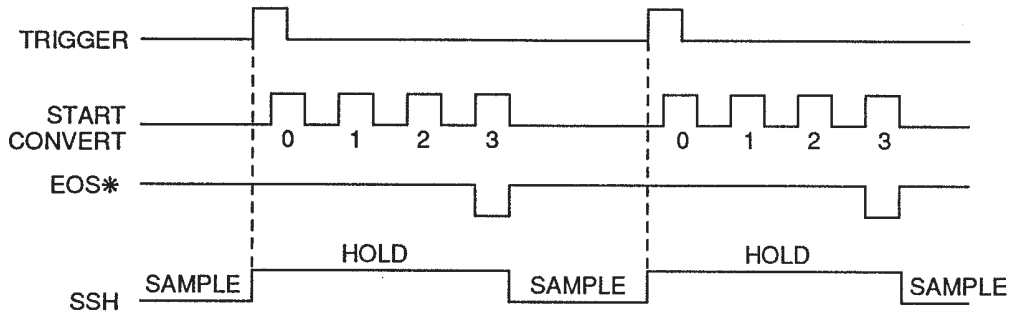


Figure 1.0 Simultaneous Sample/Hold Timings

1.4 Functional Specifications

(Specifications are for the total system and are typical at +25 °C, with a PGA gain of 1)

Analog Inputs

Number of Channels	4 single-ended, (614A,B,C). 1 single-ended, (614D). 16 single-ended/8 differential-ended, (614E)	
Full Scale Input Ranges gain=1	Unipolar 0 to 10V (A,B,C,E)	Bipolar ±10V (A,B,C,E) ±5V (B,C) ±1.25V (D)
gain = 10 (note: programmable gain on 2 channels only)	0 to 1V (A)	±1V (A)
Input Bias Current	±1 nanoamp.	
Input Impedance (power on)	10 Megohms (minimum) (See Tech. Note 1)	
Input Impedance (power off)	1.5 Kilohms.	
Input Amplifier	Jumper selectable for gains of x1 or x10 on 2 channels on the DVME-614A only. Resistor programmable gains from x1 to x100 available on the DVME-614E.	
Input Capacitance	10 pF per channel	
Input Overvoltage Protection	±15V max. (without damage)	
Input Overvoltage Recovery	2 microseconds max.	
Addressing Modes	Single Channel Sequential with autosequenced addressing Random addressing by host software All channels simultaneously (614A)	

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A/D Converter

A/D Output Resolution	12 binary bits (DVME-614A,C,D,E) 14 binary bits (DVME-614B)
A/D Output Coding	Selectable as unipolar straight binary, or bipolar 2's complement binary with sign extension through bit 15. All data is right justified.
A/D Conversion Period	500 nanoseconds (DVME-614A) 1 microsecond (DVME-614B,C,E) 200 nanoseconds (DVME-614D)
A/D Converter Start Sources	Local Programmable Timer. External TTL sample clock. Analog threshold comparator, (not available on the DVME-614D). Write to Channel Address Register.
A/D Memory	First-In, First-Out with 1024 A/D samples standard. Up to 4096 optional.
FIFO Access Time	100 nanoseconds max., 80 nanoseconds typical.

System DC Characteristics
[See Tech. note 2]

Differential Nonlinearity	± 0.75 LSB of FSR max.(614A,C) ±1.0 LSB of FSR max.(614B,D,E)
Integral Nonlinearity	±1 LSB of FSR max.(614A,C,D,E) ±1.5 LSB of FSR max. (614B)
Full Scale Temp. Coefficient	±0.1 LSB per °C (614A,C,D,E) ±0.3 LSB per °C (614B)
Zero or Offset Temp. Coefficient	±0.1 LSB per °C (614A,C,D,E) ±0.3 LSB per °C (614B)
Power Supply Rejection	±0.004% of bus +5V.

Sample/Hold Performance

Acquisition Time (FSR step, to 0.01% of FSR)	750 nanoseconds max. (DVME-614A,B,E) 200 nanoseconds max. (DVME-614C) 50 nanoseconds max. (DVME-614D)
Aperture Delay	6 nanoseconds (DVME-614A) 10 nanoseconds (DVME-614D) 30 nanoseconds (DVME-614B,C,E)
Aperture Delay Uncertainty	±1 nanosecond (DVME-614A) ±5 nanoseconds (DVME-614B,C,E) ±10 picoseconds (DVME-614D)
Droop Rate	1 microVolt/microSecond
SSH Channel-Channel Linearity Tracking	±0.03% (DVME-614A only)

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System Dynamic Performance

System Bandwidth (single channel, half scale input to rated specifications)	1 MHz for DVME-614A,C 200 KHz for DVME-614B,E 2.5 MHz for DVME-614D
Total Throughput to FIFO (single channel, gain=1, includes all acquisition and MUX settling times)	700 nanoseconds (DVME-614A) 2 microseconds (DVME-614B,E) 1 microsecond (DVME-614C) 250 nanoseconds (DVME-614D)
Total Throughput to FIFO (sequential channels, gain=1) (See Tech. note [3])	1 microsecond (DVME-614A) 3 microseconds (DVME-614B) 2 microseconds (DVME-614C) 4 microseconds (DVME-614E) 10 microseconds(DVME-614A, gain=10)
Total Harmonic Distortion (±10V FS input) (See Tech. note [4])	-72dB (614A,C,E), -75dB (614B) -68dB (614D)

VMEbus Interface

Standards Compliance	IEEE P1014/D1.0
Architecture	A24:D16 slave consisting of 16 contiguous word registers.
Data Bus Width	16 bits using P1 connector.
Address Bus	23 address lines(A23-A01) plus 6 Address Modifier (AM) lines.
Address Modifier Codes	39 or 3D hex, selectable.
Address Mapping	Decodes address lines A23-A08
VMEbus Interrupt	1 line, selectable IRQ*1-7. Asserts maskable, programmable 8-bit vector ID code.
Interrupt Source	Scan Acquire Flag (sample count reached), FIFO Full or Half Full flags.
Data Transfer	Uses 16 MHz VMEbus SYSCLK to generate DTACK*, with selectable delays. Data transfer rates vary. (See Tech. note 5)

Trigger Control

Timer/Counter	82C54 programmable interval timer,
Counter Functions	a. End Of Scan, sample count reached b. A/D start rate (16 bit divisor) c. Scan or frame rate(16 bit divisor)
Pacer Sample Counter	3 to 65,536 samples. Drives ACQ flag/interrupt.
Clock Sources (User Selectable)	Internal 8 MHz (VME bus derived) or external TTL A/D start rate clock. Choice of 500, 250 or 125 KHz internal trigger clocks.
Analog Trigger I/P Range (See Tech. note 6)	±10 Volts. Note that there is no provision on the DVME-614D for an analog trigger.

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Analog Output
See Tech. note [7]

Number of Channels	1
Functions (user selectable)	General purpose analog output. Set threshold comparator for external analog trigger.
Resolution	12 Bits
Output Voltage Range	0-10V, ±5V, ±10V at ±5 milliamps max.
Linearity	±0.05% of FSR
Settling Time	5 microSeconds to 0.05% (10V step)
Input Coding	Straight binary

Connectors

VMEbus Connector, P1	96-pin, male DIN connector. P2 connector is not used.
Local Analog Input	Four BNC bayonet coaxial, mounted on the front panel (614A,B,C,D), 614E uses a 25-pin, DB-25S female which also contains the analog output and trigger input lines.
Multipurpose Connector (614A,B,and C only)	BNC, user-selectable as pacer trigger input,analog comparator threshold input or D/A channel output. They are available through the DB-25S on 614E.

Parallel Port

Parallel Port Connector	Front panel, 25-pin DB-25S female.
Outport Type	16 data lines, TTL levels from FIFO. Includes Ready out, Acknowledge In and Transfer enable handshakes and it does not provide addressing. Output steering is software enabled.
Function	Asynchronous slave to remote master. Data transfer from FIFO to external device or peripheral and provides for external clocking. It is not a DVME-614 low-level programming interface. It also contains the analog output channel for 614A,B,C,E.
Port Loading	TTL compatible (24mA out,1.6mA in)
Port Data Rate	4 MHz max. to external processor

Miscellaneous

Power Required	+5V dc ±5% at 3.0 Amps max. from VME bus.
Operating Temperature Range	0 to +60 °C
Storage Temperature Range	-25 to +80 °C

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Relative Humidity	10% to 90%, non-condensing. Forced cooling is recommended.
Altitude	0 to 10,000 feet.
Outline Dimensions	Double height VME, 6U outline. 9.19"W x 6.3"D x 0.6"H (233.5 x 160 x 15.24 mm)
Analog section modularity	The MUX-S/H-A/D module is socketed for function interchange.
Analog adjustments	Offset and gain per channel for SSH on DVME-614A. A single offset and gain trimmer is provided on all of 614B,C,D and E. Recommended recalibration period is 90 days in stable operating conditions.

Technical Notes

1. This high input impdance minimizes signal attenuation errors associated with the input source resistance. For varying analog input signals an inline 50 ohm shunt resistor, inserted adjacent to the front-end connectors, is recommended for reducing line reflections and standing wave errors. The input impedance on the DVME-614D is 150 Kohms, with an option on the module for inserting a termination resistor between the analog input signal line and ground.

2. Allow 20 minutes warm-up time to rated specifications for the DVME-614B card.

3. The rates shown are the maximum A/D converter start rates and include MUX sequencing and settling delays. To calculate the per-channel throughput, multiply the quoted rate by the number of channels being scanned, eg. if 4 channels of the DVME-614C are being used, the maximum sample rate on any one channel is 2 x 4 = 8 microseconds (125 KHz).

4. THD test conditions are:

   a. Input Frequency:
   500 KHz (DVME-614A)
   200 KHz (DVME-614B, E)
   300 KHz (DVME-614C)
   1 MHz (DVME-614D)

   b. Generator/filter THd is -90 dB minimum.

   c. THD computed by FFT to fifth harmonic.

$$THD = \frac{20*\log10\left((V2^2 + V3^2 + V4^2 + V5^2)^{0.5}\right)}{V_{IN}}$$

   d. Inputs are half full scale, no channel advance.

   e. A/D trigger rate:
   1.5 MHz (DVME-614A)
   500 KHz (DVME-614B, C, E)
   4 MHz (DVME-614D)

5. Maximum data transfer rates over the VMEbus must be determined by testing. The VMEbus has an inherent 125 to 250 nanosecond cycle time for each data transfer. This places a theoretical 4 to 8 megawords per second on 16-bit bus transfers - even when using DMA.

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6. To obtain fastest response when using the external trigger input, keep the reference voltage near the trip input voltage. To avoid overload recovery delays, do not let the trip voltage exceed ±10V. In fact, this latter input voltage range restraint should be maintained on all input signals. Note that there is no external analog trigger input capability on the DVME-614D.

7. There is no D/A converter on the DVME-614D. Thus, there is no analog output channel on this board.

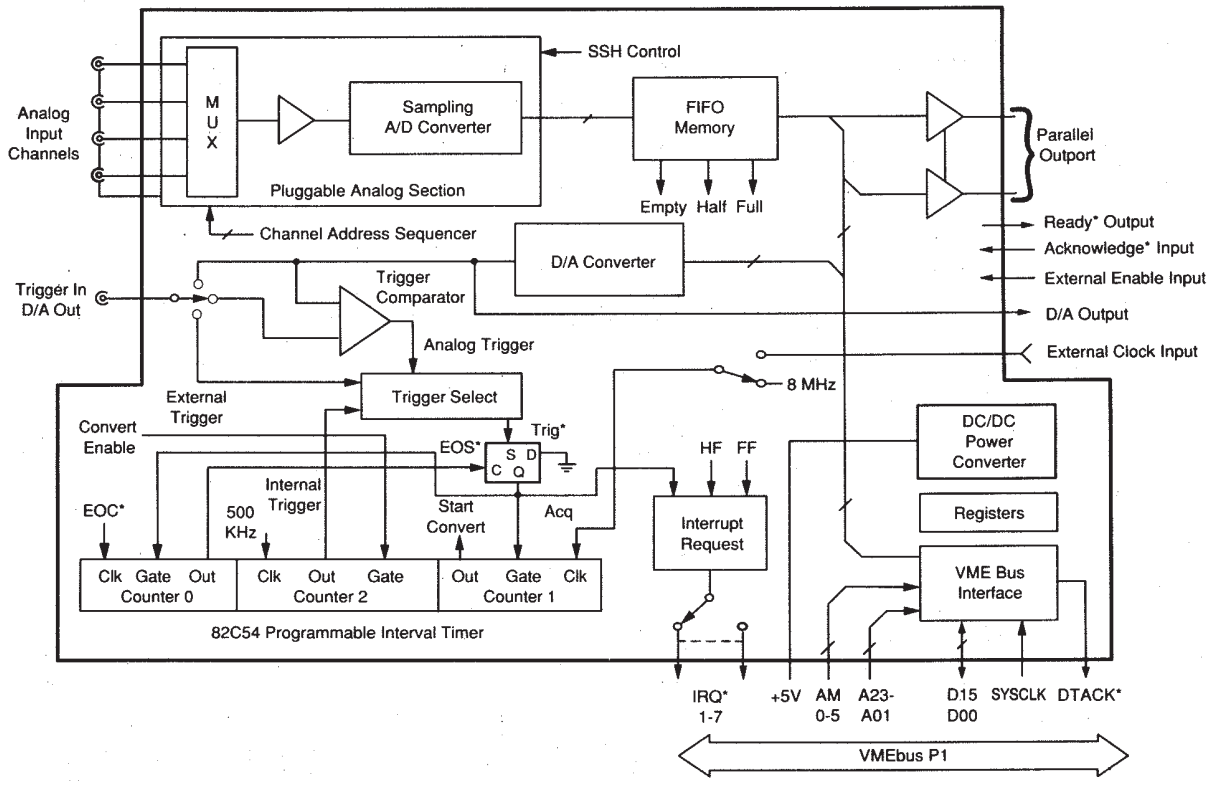


Figure 1.1 Block Diagram

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CONFIGURATION AND INSTALLATION

2.0 Determining Your Host Environment

Important: In the sections below describing jumper installation, use only the jumpers shown. Omit other jumpers that are not listed. Remember to save the jumper plugs for later use.

USE ANTI-STATIC PROTECTION !! Although the DVME-614 inputs are protected, many components on the board can be damaged by static discharge. Use grounding protection when handling the board.

Before installing the board in your host computer, study your host documentation. Installation must not disrupt the normal operation of your host and must be compatible with its resources. If your development environment differs from the target application, be aware of the differences.

Host compatibility involves both hardware and software. Hardware compatibility covers bus slot selection, memory mapping and interrupts.

2.1 Bus Slot Selection

Choose the slot but do not install yet.

The DVME-614 will operate in any VME bus slot with a full set of bus signals on its J1 backplane connector. The 16 MHz VMEbus SYSCLK signal on pin A10 MUST be present and is provided by all standard CPU boards. Generally, CPU boards and bus controllers are installed in the left end of the card cage (slot 1). If possible, position the DVME-614 away from other boards, especially those with high speed/high current digital logic. This will offer slightly improved noise performance.

The DVME-614 daisy-chains the VMEbus Bus Request, Bus Grant and Interrupt signals. Therefore, boards further away from the CPU than the DVME-614 (lower priority) will have their access preserved when the DVME-614 is installed. If you have empty slots between the CPU and the DVME-614, and you want DVME-614 interrupts, make sure the backplane jumpers are installed to carry these signals across empty slots. Rearrange the sequence of boards to vary the hardware priority of DVME-614 interrupts. Higher priority, at the same interrupt request level, is allotted to the nearer board to the CPU board.

2.2 Host Memory Map Compatibility

The DVME-614 registers appear to the host as 12 contiguous words (24 bytes) mapped in the host's memory within a 256-byte memory reservation. The starting location, called the BASE address, is selected by on-board DIP switches, discussed in a later section. The BASE address may be located anywhere in 24-bit (16 megabyte) address space on 256-byte boundaries. This contiguous memory block must not conflict with other system memory. This block cannot overlay or respond to the same address codes as other memory or peripherals in the system. Usually the DVME-614 is located in high memory, beyond any Random Access Memory. Note that the highest BASE address allowed is $FFFF00 (hexadecimal).

2.3 Host Interrupt Compatibility

If you have several concurrent tasks present in your application, A/D data ready interrupts from the DVME-614 are an effective way to maintain total system bandwidth and avoid lost A/D data. This is especially true for random, asynchronous, unpredictable tasks. Interrupts require the following decisions:

1. The Interrupt Request line to VMEbus (IRQ1 through IRQ7) must be selected on the DVME-614. This request level determines software priority of the interrupt. Board slot position determines hardware priority for interrupts at the same request level.

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2. A vector ID code must be loaded by your host program into the DVME-614's Interrupt ID register after power-up. This ID code corresponds to the address of the interrupt service routine (ISR) which handles interrupts from the DVME-614. The ID code is used by the CPU (after 2 left shifts) to develop the ISR address. This ISR address is either an absolute address or an offset from the CPU's Vector Base Register (VBR) for 680X0 CPU's. The VBR also must be loaded by host programs before interrupt usage.

3. The ISR is written by the user and must be resident in memory before DVME-614 interrupts are sent. The programs on the floppy diskette accompanying the DVME-614 may be used as examples when writing an ISR. Interrupts must be enabled in the DVME-614 Command Register before usage.

Interrupts are handled in software in one of two ways:

A. If you are NOT using a Real Time Operating System (RTOS), the interrupt controller in your host must be initialized with low level code as described above.

B. If you ARE using a RTOS interrupts are handled more symbolically and you probably will not have to do low level controller programming. You must still supply code to send DVME-614 commands, retrieve A/D data and to arbitrate with the RTOS. You will need to decide a priority for the DVME-614, how it communicates with other system tasks and how its status is managed.

All RTOS's operate in a similar manner. However exact details of RTOS programming vary greatly between different suppliers. Consult your RTOS documentation.

2.4 Base Address Selection

In the following sections refer to Figures 2.8a - f, 2.12a, b, and c and to the assembly diagram in Appendix B to help pinpoint switch, jumper and solder gap locations on the DVME-614. Position the board with the VMEbus connector, P1 at the lower right. You should carefully check ALL factory jumpering before inserting the board. Setting up the board configuration should only be done by a person skilled at miniature electronic assembly. Improper procedures may damage the board.

The BASE address, described in Section 2.2, is selected by DIP (Dual Inline Package) switches SW2 and SW3. These DIP switches are located directly above the left half of P1. Each individual switch is numbered and the "OFF" direction is marked clearly. Switches are set using a small tool such as a miniature screwdriver. The switches may be either small slide switches or rockers. When a switch is ON, it decodes a logic "0". The OFF position decodes logic "1". Switches SW2 and SW3 decode the top sixteen bits (address bits A23 through A08). Bits A07 through A05 are not decoded ("don't care") and board control will repeat every 16 bytes in the 256-byte address reservation for the board. A4 through A1 are PAL decoded for some control signal generation and individual register access.

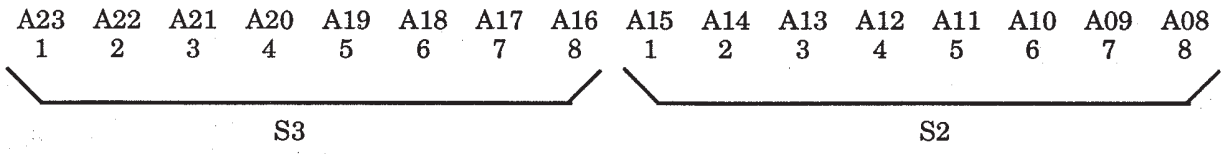


Figure 2.0 BASE Address Switch Assignments

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The factory BASE address is $FA00xx (hexadecimal), set as follows:

A23															A8
OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON
"F"				"A"				"0"				"0"			

(Note: OFF = '1', ON = '0')

Figure 2.1 Factory BASE address setting

2.5 Address Modifier Selection

The DVME-614 may be accessed in either privileged (supervisory) or non-privileged (user) modes. These modes have Address Modifier codes which are described in the VMEbus specifications. If you use a device driver, remember that the CPU will be in supervisor mode during an interrupt service routine triggered by the DVME-614. In addition, the DVME-614 may use 16-bit short I/O addressing if required. The SW1 DIP switch is to the left of center of the board. Normally, you may leave the AM jumpers in the factory configuration.

Important: Select ONLY the switches shown below:

Switch SW1:					Responds to	
1	**2**	**3**	**4**	**5**	**AM Code**	**Access Description**
1	1	1	0	0	$39	Standard non-privileged data access
					$3D	Standard supervisory data access (this is the factory shipping standard)
1	1	0	1	0	$3D	Standard supervisory data access
1	0	1	1	1	$29	Short non-privileged access
					$2D	Short supervisory access
0	1	1	1	1	$2D	Short supervisory access only

"0"=ON, "1"=OFF

Figure 2.2 Address Modifier Selection

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2.6 DTACK* Delay Setting

The DTACK* delay jumper normally should not be altered. DTACK* requires the 16 MHz SYSCLK, VMEbus signal. Delays may need to be introduced for slower host processors as follows:

DTACK* Delay	Jumper	
Do not use	E28-E31	
125-250 nS	E28-E32	(factory standard)
250-375 nS	E28-E33	
375-500 nS	E28-E34	
500-625 nS	E28-E35	
625-750 nS	E28-E25	
750-875 nS	E28-E26	
875-1000 nS	E28-E27	

Figure 2.3 DTACK* Delay Jumpers

2.7 Interrupt Level Selection

Interrupts may be generated on levels 1 through 7. DIP switch SW4 is used to select the actual hardware line, and DIP switch SW1 (switches 6,7,8) is used to set the level. (This is the same DIP package as used for Address Modifier decoding.) Figure 2.4 shows the switch settings for different configurations.

Interrupt Level	SW1 Switch Settings 6	7	8	SW4 Switch Settings
IRQ 1	ON	ON	OFF	Switch 7 ON only
IRQ 2	ON	OFF	ON	Switch 6 ON only
IRQ 3 (std.)	ON	OFF	OFF	Switch 5 ON only
IRQ 4	OFF	ON	ON	Switch 4 ON only
IRQ 5	OFF	ON	OFF	Switch 3 ON only
IRQ 6	OFF	OFF	ON	Switch 2 ON only
IRQ 7	OFF	OFF	OFF	Switch 1 ON only

Note: OFF = '1', ON = '0'

Figure 2.4 Interrupt Level Selection

2.8 Interrupt Source

VMEbus interrupts may be derived from the Data Acquisition Flag (ACQ) which is reset by counter 0 output (EOS*). Interrupt Requests may also be generated by the FIFO Half-Full (HF) and FIFO Full (FF) flags. The required source may be specified by the Command Register - see Section 3.3.

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2.9 Clock Selections

Selection	Frequency	Jumper
A/D Sample Clock for Counter #1 (Counter 1 specifies the A/D conversion rate)	8 MHz	E41 - E40 (standard)
	External Clk	E41 - E42
Internal Trigger Clock for Counter #2 (Counter 2 specifies the internal A/D trigger frequency)	500 KHz	E100 - E101
	250 KHz	E100 - E102
	125 KHz	E100 - E103

Figure 2.5 Clock Jumper Selections

2.10 A/D Converter Connections

All DVME-614 A/D converter hardware selections are made using jumpers and solder gaps on the analog module, M1. Jumpers are removable "Berg" plugs that fit over square pins that are mounted on the analog daughter card. They may be replaced by wire wrap connections if desired. Also connect only those jumpers shown, leave all others disconnected. The solder gaps are gaps or open-circuit traces on the module that are either filled with solder to make the connection or desoldered to break the connection. Note that only the gaps listed in this section for a particular option must be soldered - all others must be desoldered. This task should be done by experienced personnel since any damage inflicted may void the product warranty.

A/D Resolution

The A/D converter type and resolution is configured at the factory and should normally never need to be changed. They are as follows:

A/D Converter Type	Resolution	Jumper	Channel Advance at
DVME-614A	12 bits	Y16-Y17	End of Conversion
DVME-614B	14 bits	Y15-Y16	Start of Conversion
DVME-614C,D,E	12 bits	Y15-Y16	Start of Conversion

Figure 2.6 A/D Type and Resolution

External Trigger Inputs

Function	Jumper
Digital Trigger Input	E4 - E7
Analog Trigger Input	E4 - E6

Figure 2.7 A/D Trigger Selection

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Input Voltage Range Selection

The jumpers and solder gaps for input range selection are on the M1 modules as illustrated in Figures 2.8a - e. Carefully remove this daughter card from the motherboard and, depending on which A/D converter type is on the board, set the jumpers or Solder Gaps (SG) as follows (note: solder only the gaps listed, desolder all others).

Input Range	DVME-614A	DVME-614B	DVME-614C	DVME-614D	DVME-614E
± 10 Volts	SG3	E4-E5	Y1-Y3, Y4-Y5	N/A	SG8, 10, 6
± 5 Volts	N/A	E1-E2, E4-E5	Y1-Y2, Y4-Y5	N/A	SG9, 11, 6
0 to +10V	SG4	E1-E2, E3-E4	Y1-Y2, Y5-Y6	N/A	SG9, 11, 7

(Note: ±10V setting is the factory shipping standard.
DVME-614D input range is fixed at ±1.25V.)

Table 2.1 Input Voltage Range jumper Settings

On the DVME-614E, the input configuration is selectable as 16 single ended (SE) or 8 differential ended (DE) as follows:

Single Ended (SE): Solder SG1, SG3 and SG5
Differential Ended (DE): Solder SG2 and SG4

A/D Output Binary Coding

Options of straight binary and 2's complement offset binary are jumper selectable as illustrated in the following table.

Output Coding	DVME-614A	DVME-614B	DVME-614C	DVME-614D	DVME-614E
Unipolar or Offset Binary	SG5, SG8	E6-7, E10-11	Y7-8, Y10-11	SG1, SG4	SG12
2's Complement	SG6, SG7	E7-8, E9-11	Y8-9, Y11-12	SG2, SG3	SG12 open

(Note: the factory shipping standard is for 2's complement coding)

Table 2.2 Output binary Coding Jumper Setting

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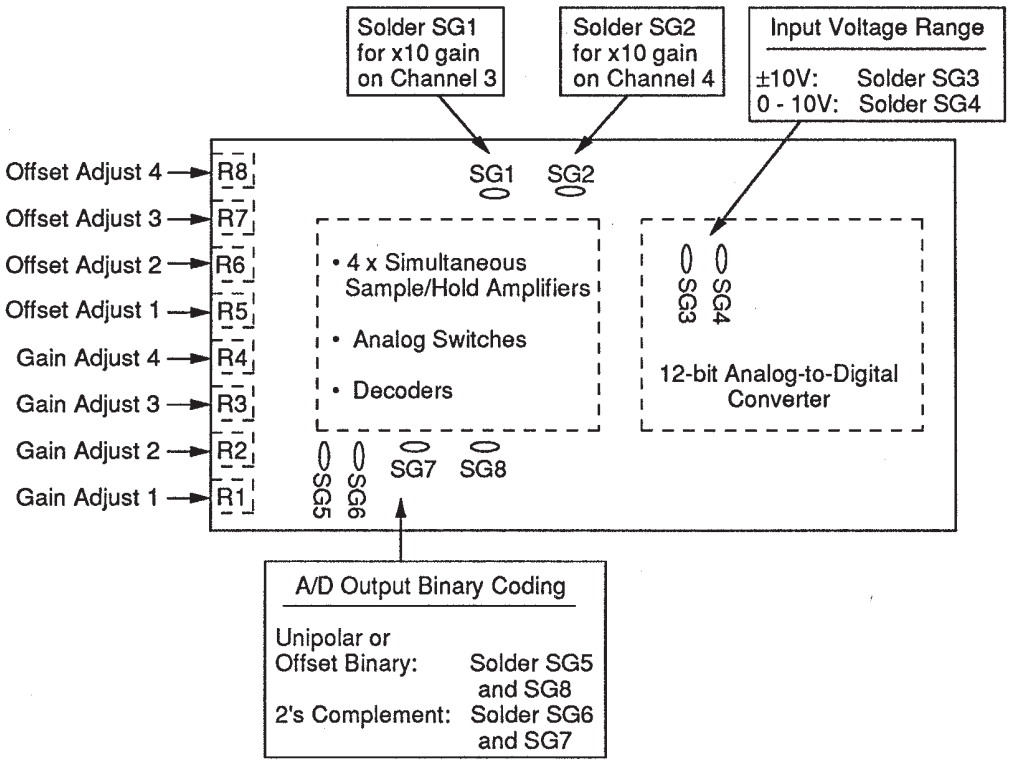


Figure 2.8a M1 Module for DVME-614A (Solder Side)

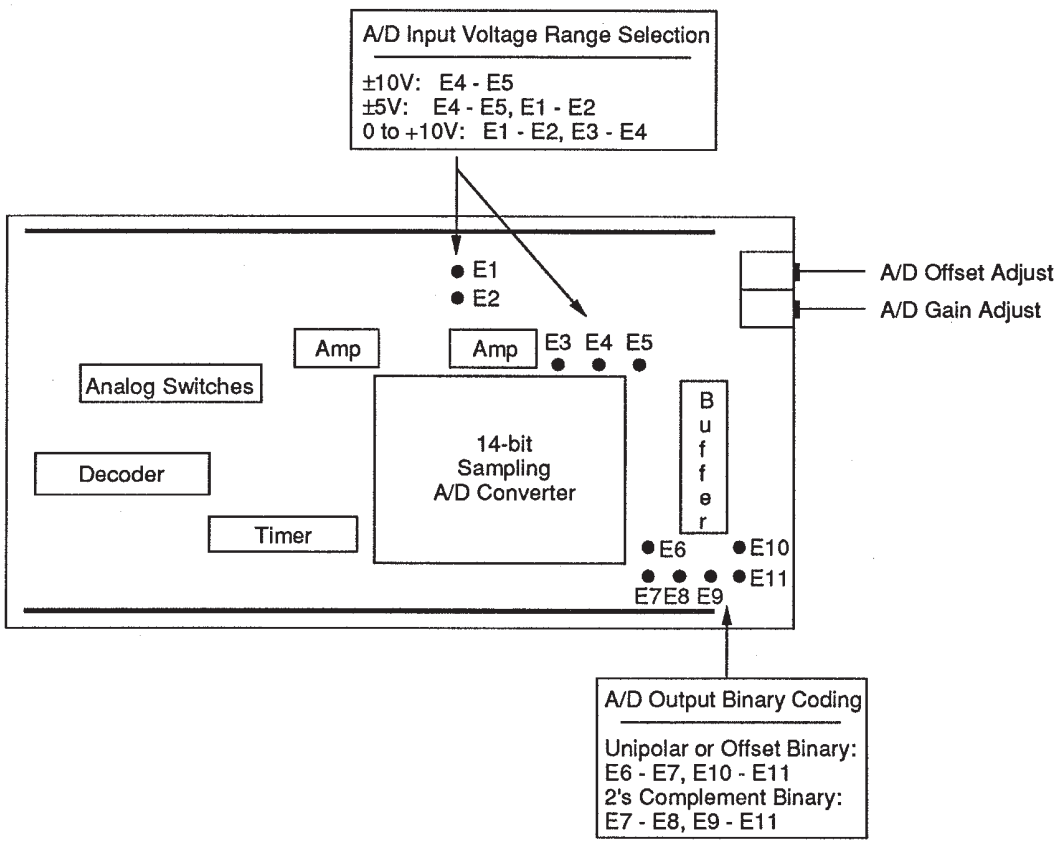


Figure 2.8b M1 Module for DVME-614B (Component Side)

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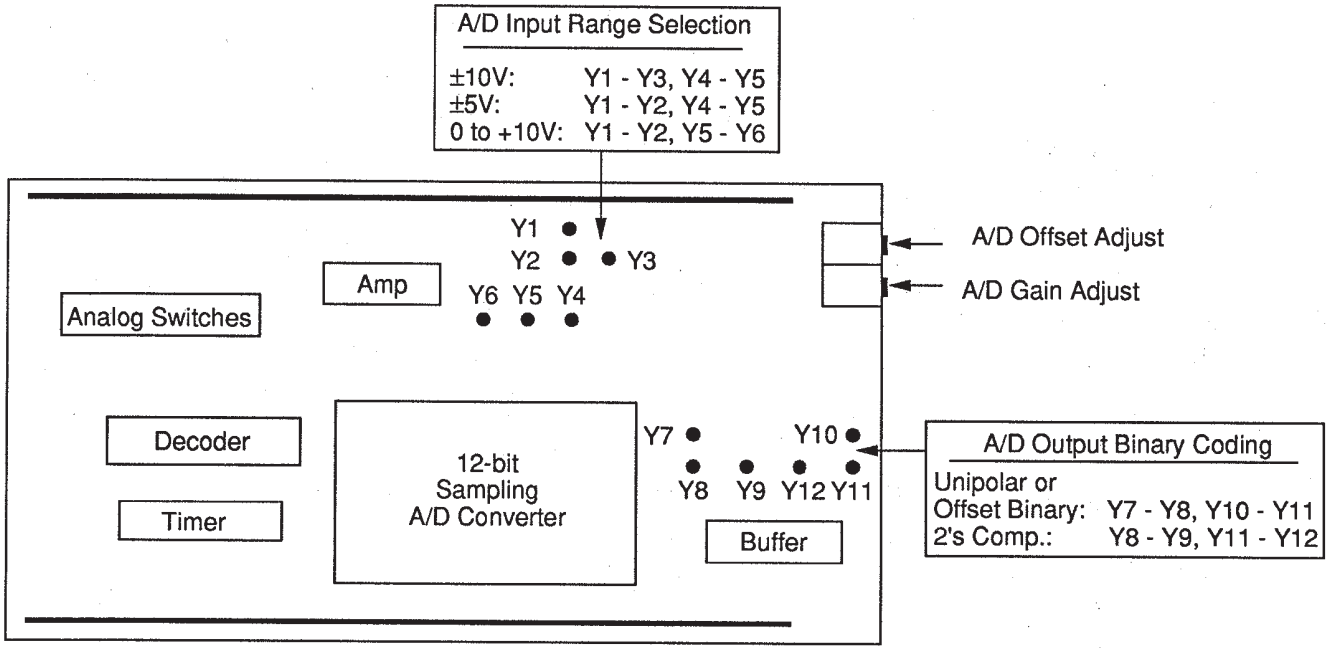


Figure 2.8c M1 Module for DVME-614C (Component Side)

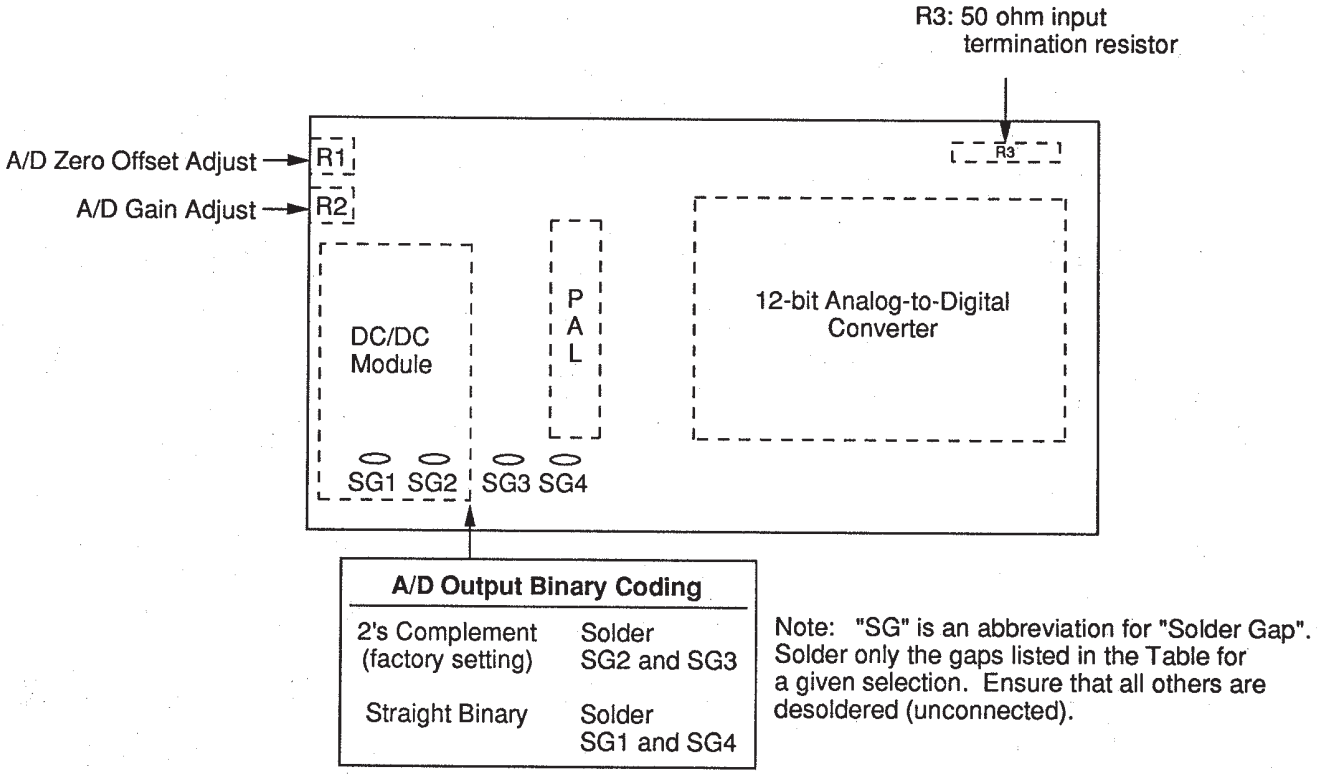
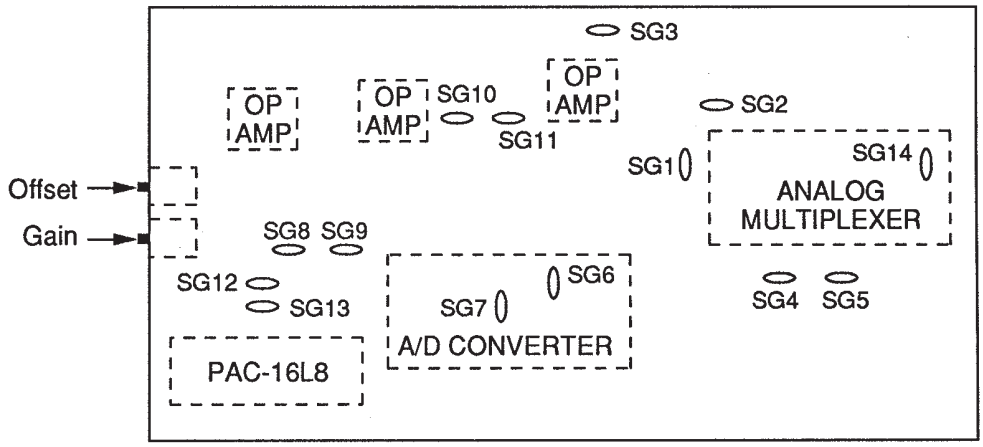


Figure 2.8d M1 Module for DVME-614D (Solder Side)

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Single-ended input	SG1, 3 & 5	0 to +10V Range	SG7, 9, & 11
Differential input	SG2, 4	Straight Binary	SG12 closed
±10V Range	SG6 , 8, & 10	2's Complement	SG12 open
±5V Range	SG6, 9, & 11		

Figure 2.8e M1 Module for DVME-614E (Solder Side)

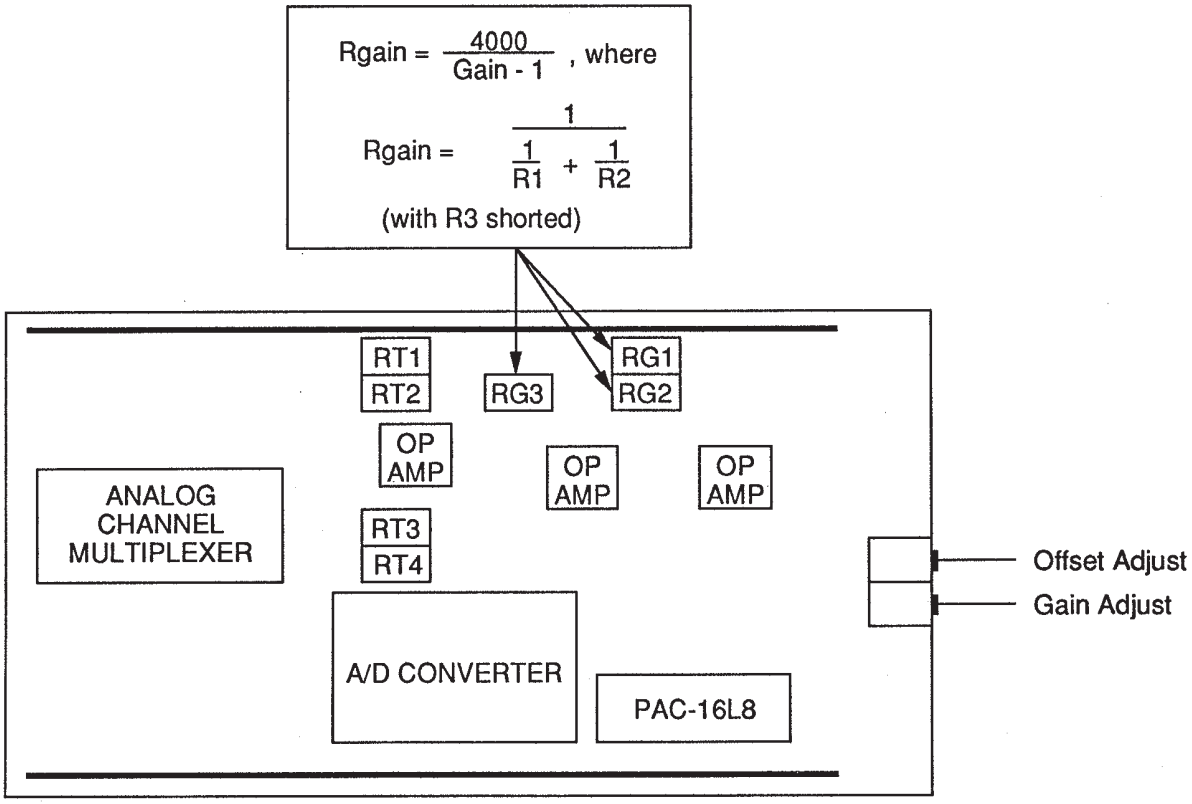


Figure 2.8f M1 Module for DVME-614E (Component Side)

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2.11 Input Amplifier Gain Selections

Input amplifier gains are selectable on both the DVME-614A and E modules to accomodate low level, analog input signals.

DVME-614A: The gain on input channels J3 and J4 is selectable as times 1 or times 10 by soldering selected gaps on the analog module (see Figure 2.8a). This task should be done by experienced personnel and extreme caution should be exercised to avoid damaging the module. Note that any damage inflicted in this respect may void the warranty.

The following are the selections:

Channel 2 (J3) gain = x10 Solder SG1
Channel 3 (J4) gain = x10 Solder SG2
(Note: the default setting is for x1, with no gaps soldered.)

DVME-614E: The input instrumentation amplifier gain is resistor programmable for gains from x1 to x100. The gain resistor designations are RG1, RG2, and RG3 - refer to Figure 2.8f. These are configured with RG1 in parallel with RG2 and RG3 in series with the combination. The total gain resistance may be calculated from the following equation:

$$R_{GAIN}\text{ (total)} = 4000/(\text{Gain} - 1)\text{ Ohms,}$$
$$\text{where } R_{GAIN}\text{ (total)} = [1/(1/RG1 + 1/RG2)] + RG3$$

The recommended procedure is to short out RG3 by connecting a wire across its pads. This forces RG3 = 0 in the above equation. RG1 should be a low drift, high precision resistor (0.1% tolerance) and RG2 is used to fine tune the gain.

2.12 Analog Output Selection

Note that there is no analog output channel on the DVME-614D.

To use the DAC channel as a general purpose analog output channel then simply connect jumper E4 to E5.

Jumpers E9 through E13 select the analog output voltage range as follows:

Range	Jumper	
±10V	E9-E10, E12-E13	(standard)
0 to +10V	E8-E9, E11-E12	
±5V	E9-E10, E11-E12	

Figure 2.9 DAC Output Voltage Selection

2.13 Board Installation

Remember anti-static protection.

If you have followed all the steps above, all jumpers should now be properly positioned. Confirm that your host computer and its Operating System (OS) function normally. Shut off host power.

Using the board slot you have chosen, carefully slide the DVME-614 into the VME card guides. Make sure your hands are grounded before handling the board. Do not force the board. If it does not seat properly, observe the P1 connector to see that it is receiving the board.

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Now reapply power with the DVME-614 installed. Confirm that your OS boots up normally. Verify the memory size message if it is normally present. If the OS fails to boot up normally, immediately turn power off and determine the cause. Remove the DVME-614 and check for overheated components remembering that the DC/DC converter normally runs quite warm.

2.14 VMEbus Connections

The interface to the VMEbus host is made through the P1 connector, shown in Figure 2.10. This interface uses the IEEE-P1014/D1.0 specification. Note that the Interrupt Acknowledge connections are fully implemented and that internal DVME-614 logic uses the 16 MHz SYSCLK.

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

Figure 2.10 VMEbus Connector - P1

(Note that the P2 connector is also provided on the DVME-614 board, but is NOT connected to any on board signals. It is available as an optional port e.g. parallel port, by hardwiring the required signals over from the P1 connector. P2 also provides stronger and more distributed physical support and anchorage for the DVME-614 board when in a VMEbus card-cage)

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2.15 Front Panel Connectors

For ease of access, the DVME-614 board has all its analog and digital connectors, (apart from the VMEbus connector), mounted on the front panel as illustrated in Figure 2.10. The DVME-614A, B, C, and D include 5 BNC, bayonet connectors and 1 parallel port connector - DB-25S female. Four of the BNC connectors are analog input channels (DVME-614D uses Channel 0 (J1) only), while the fifth, J5, is user selectable as a trigger input or as an analog output. There is no analog output channel on the DVME-614D. The parallel outport accesses the raw A/D data in the FIFO Data Register, thus providing a medium through which external devices and peripherals may read the data without transferring it over the VMEbus. This connector contains the external clock input and the D/A analog output signals. The DVME-614E also has this parallel output port but its analog inputs are now provided on a second DB-25S connector - J1. This connector includes the trigger inputs and the analog output signal lines.

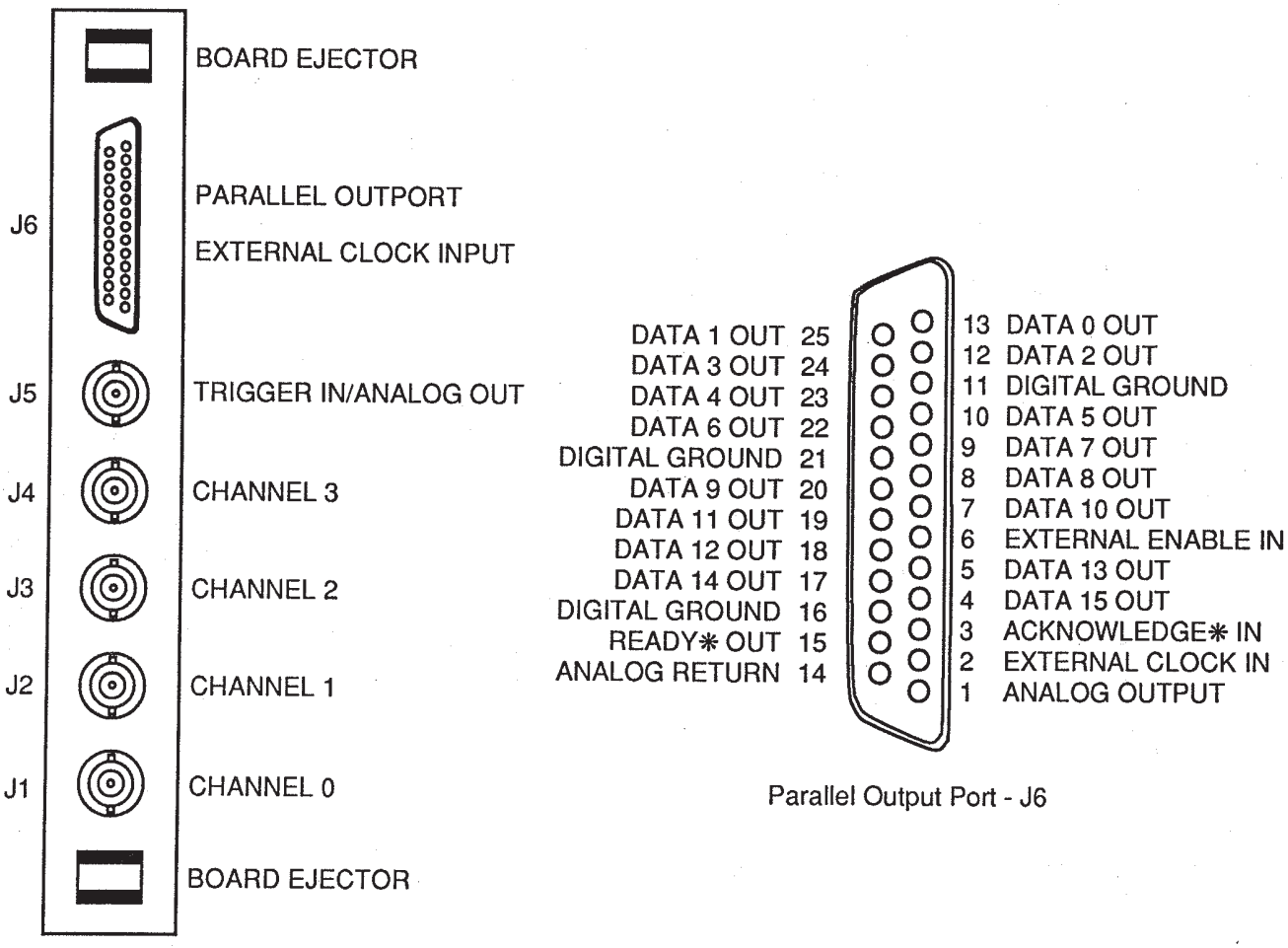


Figure 2.11a DVME-614A,B,C,D Front Panel Connectors

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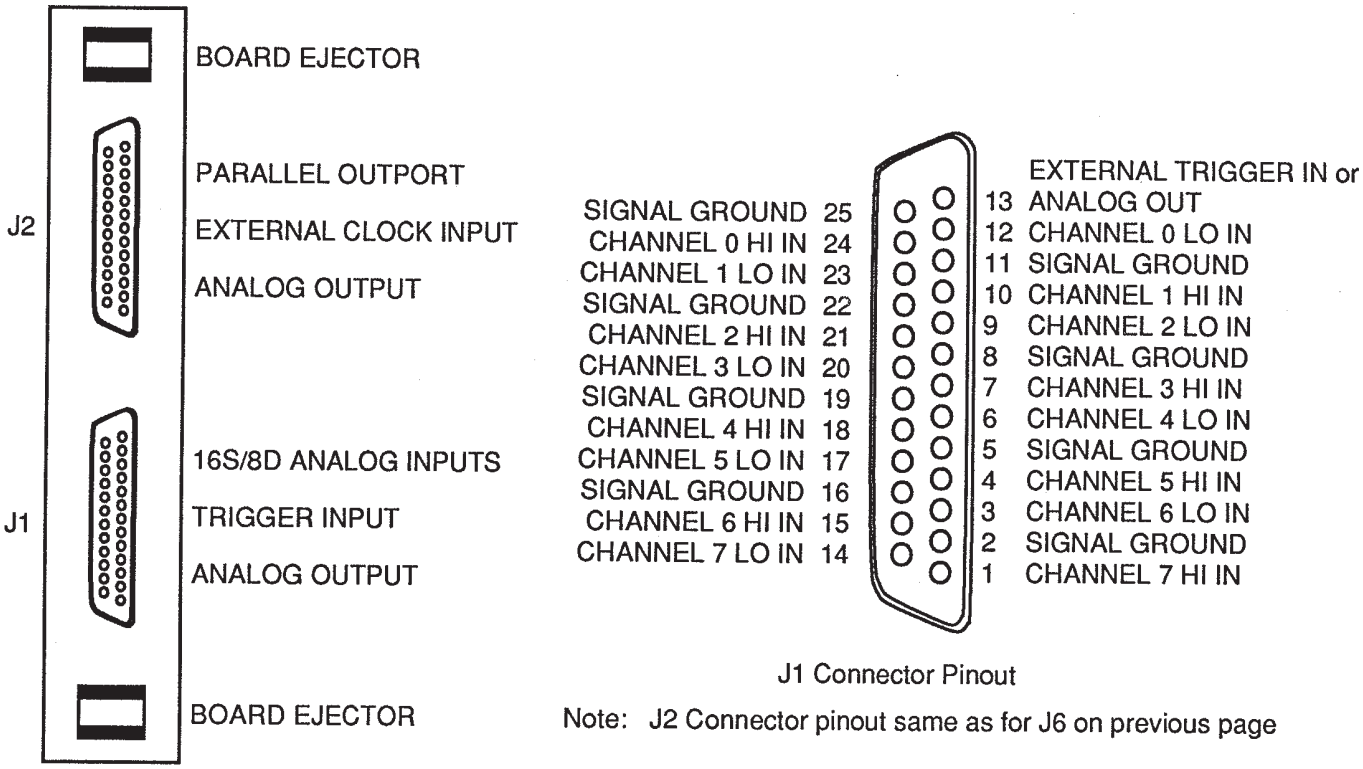


Figure 2.11b DVME-614E Front Panel Connectors

2.16 DVME-614D Analog Input Signal Connection

There is a 50 ohm termination resistor installed on the analog module's front end. The function of this shunt resistor is to match the input impedance of the DVME-614D with both the cable and source impedances in an effort to eliminate transmission line phenomena such as reflections and standing wave errors. The user must determine if the resistor should be left installed or should be removed/replaced to best suit his application. He should determine the output impedance of the source and the characteristic impedance of the cable, (typically 50, 75 or 93 ohm for co-axial cable), and then decide if a 50 ohm termination is appropriate. If not, remove R3 from the analog module and install an in-line shunt termination resistor, (of the correct value to match the system), on the PC-414D input - as close to the analog module as possible. This should be done by an experienced person since any damage incurred during soldering/desoldering the resistor may void the warranty on the product. Because the system will still not be completely matched keep the input cable length as short as possible - 1 to 2 feet maximum.

2.17 A/D Calibration

The DVME-614 is supplied by DATEL fully calibrated and tested. However, depending on the operating environment, it should be recalibrated every 90 days. To avoid damage, users performing calibration procedures should be thoroughly familiar with electronic test equipment, the host computer and microelectronic assemblies. Handle the board very carefully using anti-static protection.

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DVME-614 calibration should be performed according to the following procedure:

1. Equipment Required

Precision voltage calibrator such as DATEL's DVC-8500.
Precision digital voltmeter such as a FLUKE 8800.
VME Extender board.
Miniature jewellers screwdriver and clipleads.
Assemblies and schematics to verify jumpers and trimmers.

2. Consult the assembly drawings and schematics in Appedix B of this manual and examine the DVME-614 board. Locate the gain and offset adjust potentiometers on the A/D plug-in module - they are blue trimmer pots, with the screw terminals facing over the edge of the board as illustrated in Figures 2.12a,b,c. They are labelled clearly, as "GAIN" or "OFFSET" as appropriate, on the Printed Circuit Board (PCB).

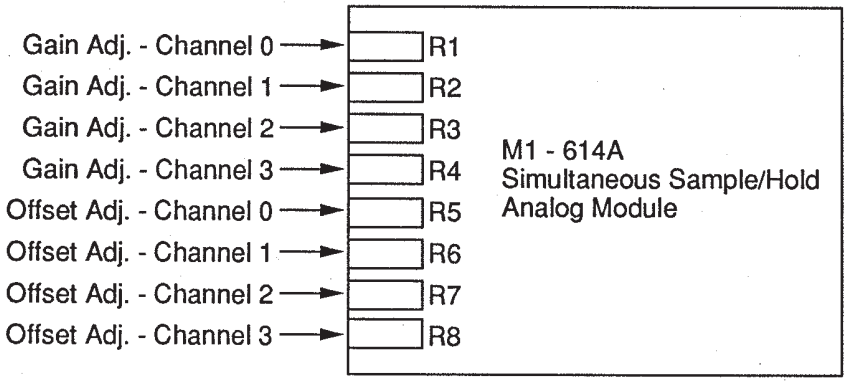


Figure 2.12a S/H Gain and Offset Trimmer Locations on "A" Module

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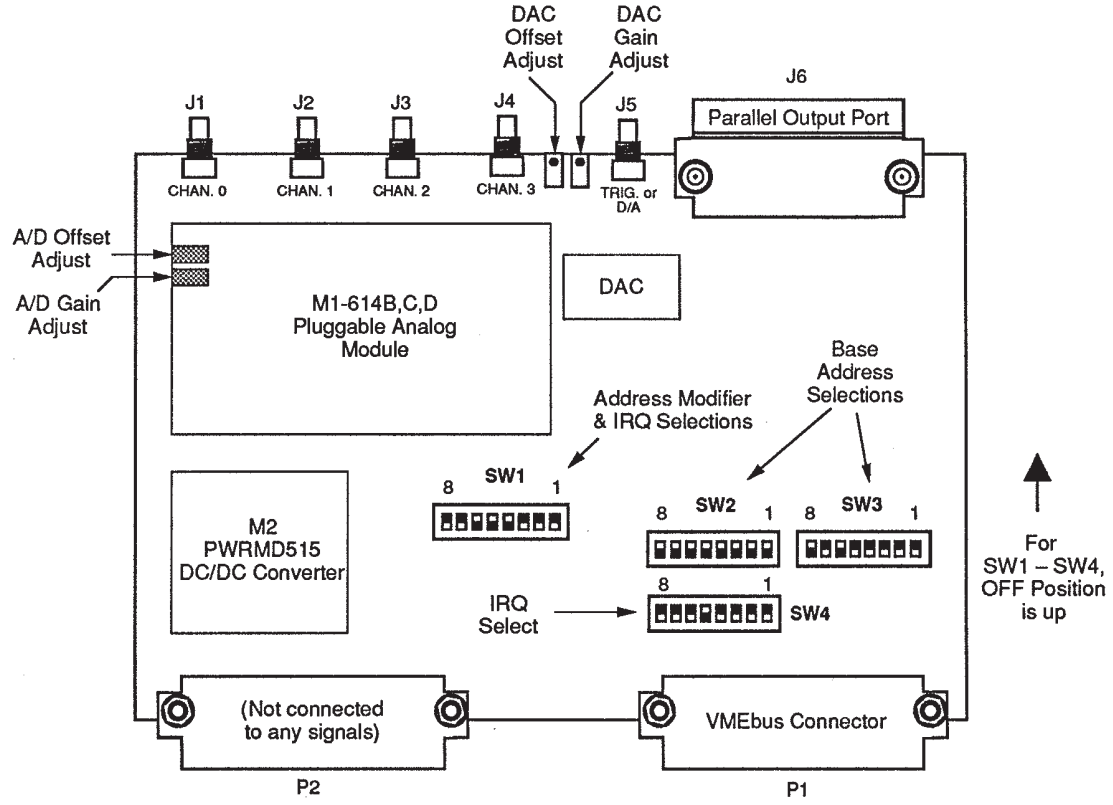


Figure 2.12b A/D Gain and Offset Trimmer Locations for B, C, and D Modules

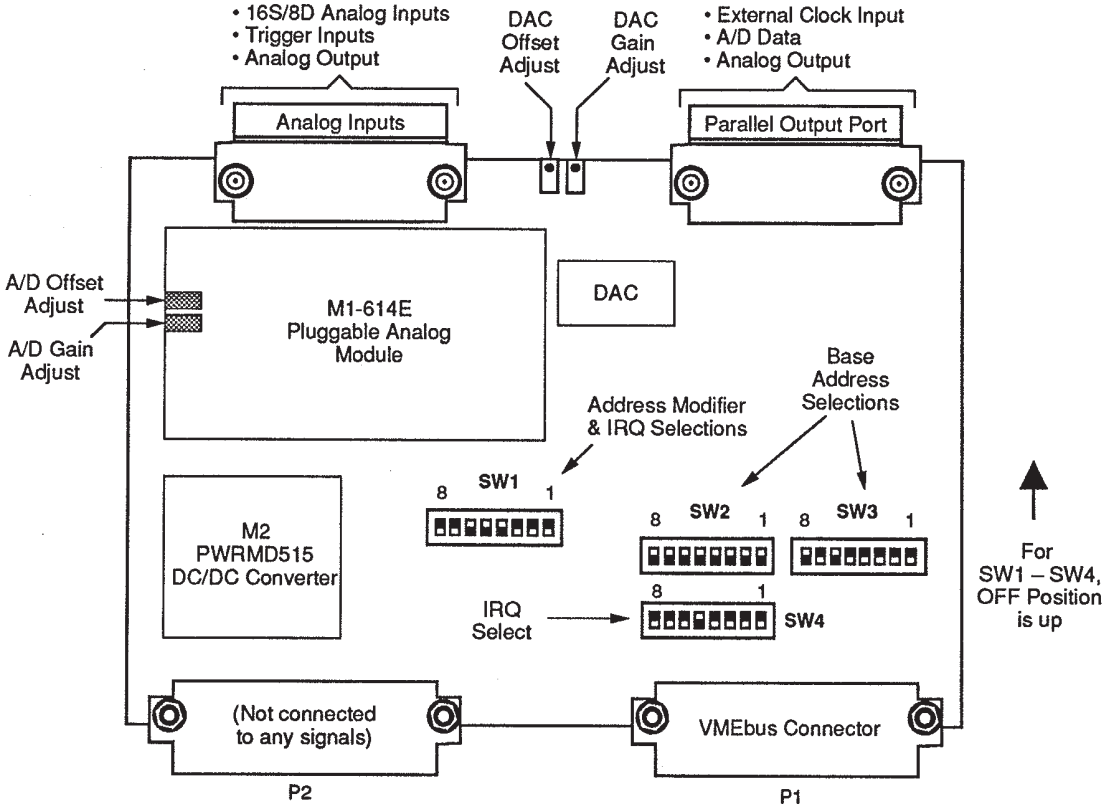


Figure 2.12c A/D Gain and Offset Trimmer Locations for E Module

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Note that on the DVME-614A, gain and offset adjustment potentiometers are provided for each of the Sample/Hold moduli, rather than for the ADC itself. The PCB designations of each of the potentiometers are as follows:

Model	Designation
614 A	R1.....R8
614 B	RN1 - Gain
	RN2 - Offset
614 C	R10 - Gain
	R7 - Offset
614 D	R2 - Gain
	R1 - Offset
614 E	R5 - Gain
	R6 - Offset

Figure 2.13 A/D Offset and Gain Pot Designations

3. Next install the DVME-614 board into the desired slot in the VMEbus cardcage - not forgetting to backplane jumper the daisy-chain signals, BR0*..BR3*, BG0..3IN*, BG0..3OUT*, IACKIN* and IACKOUT*, if there are any empty slots between the DVME-614 and the CPU board. Power up the host system, making sure that it is operating normally.

4. The calibration environment should be electrically quiet. Avoid large industrial switching noise or RF fields during calibration. Connect the voltage calibrator to the J1, channel 0, input terminal on the board, using a short signal lead which is not routed near electrically noisy sources - especially the switching power supply.

5. Set the analog input voltage range jumpers to ±1.25V (614D), ±5V, ±10V or 0 to +10V as required by your application - see Section 2.10 for jumper selections.

6. There is a calibration routine, written in 'C', supplied on the 5.25" diskette that comes with the DVME-614. This may be used for performing A/D conversions, as well as reading and displaying the A/D data on the screen. Run the executable code on your host system.

7. Enter a base address of $FA0000, since this is the factory shipping standard. If you wish to change this address, refer to Section 2.4. Select Channel 0 as the input channel, since the input signal lead is connected to the J1 connector. Enter a Conversion Rate Frequency of 100000 Hz.

8. Now, referring to Table 2.3, set the voltage calibrator input to the DVME-614 to the NEGATIVE Full Scale value. Observe the hexadecimal data readings displayed on the terminal and adjust the Offset potentiometer, (see Figure 2.12a,b,c), on the A/D module until the data reading corresponds to the Offset Trim Output reading in Table 2.3. When adjusted, check the accuracy of the output by applying other input voltages, as per Table 2.3, and observing the corresponding Hex. outputs. Note that the Offset Trim Output coding is given in 2's complement form.

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Model	Calibrator Input Voltages for A/D ranges of:			Offset Trim Output in hexadecimal	
	±10V	±5V	0-10V		
614 A,C, D,E	-10.0000V	-5.0000V	+0.0024V	F800	O
	-5.0000V	-2.5000V	+2.5000V	FC00	
	0.0000V	0.0000V	+5.0000V	0000	
	+5.0000V	+2.5000V	+7.5000V	0400	
	+9.9902V	+4.9951V	+9.9951V	07FE	G
614 B	-10.0000V	-5.0000V	+0.0000V	E000	O
	-5.0000V	-2.5000V	+2.5000V	F000	
	0.0000V	0.0000V	+5.0000V	0000	
	+5.0000V	+2.5000V	+7.5000V	1000	
	+9.9976V	+4.9988V	+9.9997V	1FFE	G

'O' - initial setting for Zero Offset adjustment
'G' - initial setting for Gain adjustment

Table 2.3 A/D Offset Calibration Table

Note: the factory jumpering standard is for an input range of ±10V, with an A/D output coding of 2's complement binary. To change the jumper selections refer to Section 2.10.

9. To calibrate the A/D gain, follow the same procedure as in 7 above, only this time set the initial input from the calibrator to NEAR the POSITIVE Full Scale value. Adjust the Gain trimmer until the output corresponds to that in Table 2.3. Again, verify the output accuracy by applying other voltages from the Table and observing the outputs.

Once the gain adjustment is completed, repeat the Offset test again. Since these two adjustments interact, repeat them alternately until no further improvement can be obtained.

This completes the A/D calibration procedure.

2.18 DAC Calibration

Note: This procedure applies to the DVME-614A, B, C, and E boards only. The DVME-614D card does not have a D/A channel.

1. Locate the offset and gain trimmer potentiometers on the DVME-614 board - these are on the motherboard, as opposed to being on the A/D module as in the previous section, see Figure 2.12a,b,c. Thus, they are the same for all DVME-614 models - A,B,C,E. They are located between the J4 and J5 SMA channel connectors on the board. Their Printed Circuit Board designations are:

R5 - Offset adjust
R6 - Gain adjust

2. Configure the J5 channel as an output channel, as described in Section 2.12. Connect a precision digital voltmeter to the J5 connector - Fluke 8800 or equivalent.

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3. Set the analog output range jumpers to 0 to +10V, ±10V or ±5V as your application requires - see jumper configurations in Section 2.12.

4. Write the hexadecimal values, as shown in Table 2.4, to the D/A Register (at BASE + 4-see Section 3.6). Start with the MINUS Full Scale setting for trimming the Offset, (line marked with 'O'), and set to NEAR POSITIVE Full Scale initially for adjusting the Gain (line marked with 'G'). The other DAC Register data settings in Table 2.4 may be used to verify the output accuracy.

A software routine similar to the following will allow you to write to the DAC Register.

```
# include (stdio.h)
#define FOREVER for(;;)
#define BASE 0x300
main( )
{

unsigned short *dac_register;
long count, data;
dac_register = BASE + 0x04;

   FOREVER
   {
   printf("Input the Hex DAC data value" );
   printf("\nEnter 'D' to terminate) ");
   scanf("%x", &data);                          /*read input*/
   if(data==0x0D)  exit(0);
   *dac_register = data;                        /* write data to DAC Register */
   }
}
```

DAC Data (Hex)	Analog Output Voltage for each D/A Full Scale Input Range			
	±10V	±5V	0 - 10V	
0000	-10.000V	-5.000V	0.000V	O
0200	- 7.500V	-3.750V	+1.250V	
0400	- 5.000V	-2.500V	+2.500V	
0800	0.000V	0.000V	+5.000V	
0C00	+ 5.000V	+2.500V	+7.500V	
0E00	+ 7.500V	+3.750V	+8.750V	
0FFE	+ 9.990V	+4.995V	+9.995V	G

'O'- initial Offset adjustment setting
'G'- initial Gain adjustment setting

Note: Straight binary coding.

Table 2.4 D/A Calibration Table

As with the A/D calibration, repeat these two procedures alternately until no further improvement can be obtained.

This completes the D/A calibration procedure.

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PROGRAMMING

3.0 General Programming Information

The DVME-614 appears to the host computer as a contiguous block of 16-bit word registers, mapped within the host's address space on 256-byte boundaries. To program the DVME-614, read/write memory operations may be used in any language from any Operating System. In "C", short pointers will access these registers. In 680X0 assembly language, indirect word move (move.w) operations do the job. In a few high level languages, you may need to link in a pair of small assembly language subroutines (read memory word and write memory word). In BASIC for example, the standard PEEK and POKE memory accesses only operate on bytes. Newer versions may include memory word pointer operations. Whatever language is utilized for writing application software, please be fully aware of the signal settling times of the DVME-614 hardware - particularly where channel addresses are being sequenced or changed. (Refer to Section 3.5 for further details).

The programs supplied with the board are examples of how to control the board. Because of the many ways the board can be used, you will probably need to make small modifications to the programs. Refer to the programming guidelines below. If you are an experienced programmer, skip to the register description.

3.1 Initial Monitor/Debugger Tests (Optional)

This section is optional. It allows you to quickly test the board before you have written your program.

If you have a low level Monitor or Debugger program on your host, you can verify the bus interface of the DVME-614 using memory read/write commands which directly access the 614's registers. No program is needed.

The DVME-614 registers are not exactly like RAM memory. Word access is needed for most but some registers can be accessed as bytes. Some registers are read or write only. Other registers (the Command/Status) do not use all the 16 bits. A readback will have some undefined bits which do not agree with the write value but will not cause a bus error. The memory modify (write) commands on some Debuggers do a blind readback of the written values to confirm proper loading. If the write and read values do not agree, the Debugger reports an error (but not a bus error). However, the memory write operation usually succeeds. Do a memory read to confirm - looking at only the "live" bits. You should understand hexadecimal notation thoroughly.

Several types of errors are possible when doing these low level tests. The Debugger readback error was described above. Bus errors are more severe. They will often abort the Debugger and may have messages such as "bus timeout", meaning that the host did not receive the DTACK* VMEbus signal from the DVME-614. Bus errors often cause a dump of the CPU registers. Severe bus errors lock up the whole system, requiring a hardware reset. If you consistently get bus errors, either the BASE address or address modifier switches are incorrect or do not match the address values sent by your CPU. You may also be using a memory address which conflicts with other host hardware. If only the Super User or supervisor (privileged) mode works, the address modifier may not be correct.

The Debugger must be able to send the absolute physical address to the DVME-614. If you can control the data size, (8-bit byte or 16-bit word), some registers are easier to access.

ID Register Test

First, make sure interrupts are off by writing $0000 into BASE + 0 and/or turn all the IRQ switches OFF. Byte location BASE + 0Dh is the interrupt ID register and this register acts like read/write memory. Write and read back several values into the byte address BASE + 0Dh. If you get Debugger memory modify

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errors (but not bus errors), use a second memory display command after the write. Only the low order bits are active (the byte at the higher address, BASE + 0Dh). Byte address BASE + 0Ch is not defined since the higher address contains the lower data byte. If these tests succeed, you are ready to program.

3.2 Register Memory Mapping

BASE address switches must be selected for even address boundaries. All registers must be accessed on 16-bit word (.W) memory operations (note that there is no connection to the P2 connector, hence, no 32-bit longword accesses allowed). Table 3.0 below illustrates the memory map of the registers.

Address (hex)	Direction	Description
Base + 0	Write	Command Register
Base + 0	Read	Status Register
Base + 2	Write	Channel Address Register
Base + 4	Write	D/A Data Register
Base + 6	Write	FIFO Reset Register
Base + 8	Not used	
Base + 0Ah	Not used	
Base + 0Ch	Read/Write	Interrupt Vector ID
Base + 0Eh	Read	FIFO Data Register
Base + 10h	Read/Write	Counter #0 (82C54)
Base + 12h	Read/Write	Counter #1 (82C54)
Base + 14h	Read/Write	Counter #2 (82C54)
Base + 16h	Read/Write	Control Register (82C54)

Table 3.0 DVME-614 Register Set

The base address may be selected anywhere up to $FFFF00h on 256-byte boundaries. (Note that the factory shipping standard is $FA0000h.)

At power-up or VMEbus reset, all registers contain zeroes except the FIFO HF and FF bits. The registers may be programmed in any sequence as long as the Command Register is last.

3.3 Command Register (Write BASE + 0)

The Command Register is a byte-wide, write only register that controls the operation of the board including interrupt source select, trigger specification, scan selection and FIFO data transfer. The register's bit field is configured as follows:

15....8	7 6 5	4	3	2	1 0
x.....x	Interrupt Source FF HF ACQ	Para/ Bus*	Trig Pol	Cnvrt Enbl	Trigger Source

("x" bits are not used or don't care)

Figure 3.1 Command Register Bit Field

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Trigger Source [Bits 1,0]	00 =Scan by a write to the channel address register (normally not used). 01 =Scan by internal trigger. 10 =Scan by external TTL trigger. 11 =Scan by external analog threshold trigger.
Convert Enable [Bit 2]	0 = Disable A/D conversion (default) 1 = Enable A/D conversion
Trigger Polarity [Bit 3]	0 = Trigger on falling edge (default) 1 = Trigger on rising edge
Select FIFO Output Data Steering [Bit 4]	0 = Select VMEbus data register (Inhibit parallel port) 1 = Enable FIFO transfers to parallel port (Inhibit VMEbus data access)
Interrupt Source [Bits 7,6,5] These bits are OR'd.	Bit 5 = 1: Enable interrupt on Acquisition done flag. Bit 6 = 1: Enable interrupt on FIFO half full flag. Note that HF occurs when half the FIFO size plus 1 samples are converted. Bit 7 = 1: Enable interrupt on FIFO full flag.
Note:	Bit 5,6,7 = 0: Disable interrupts (default)

3.4 Status Register (Read BASE + 0)

The Status Register resides at the same address location in the host processor's memory map as the Command Register but it exhibits a different bit representation. It is a byte-wide, read-only register that enables host monitoring of the DVME-614 data acquisition process.

15-8	7	6	5	4	3	2	1	0
x-x	FIFO Status			Ovr Smp Err	Xfr in Pro	Ana Trg Lvl	EOC Sts	ACQ Sts
	FF	HF	EF					

Figure 3.2 Status Register Bit Field

Acquisition Status [Bit 0]	0 = A/D scan not in progress or scan done (Counter 0 sample count was reached). 1 = A/D scan in progress (Counter 0 sample count not reached).
End of A/D Conversion Status (EOC) [Bit 1]	0 = A/D conversion in progress, data invalid 1 = A/D conversion done, data valid
Analog Trigger Comparator Output [Bit 2]	0 = Analog trigger input is below reference 1 = Analog trigger input is above reference

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Transfer in Progress [Bit 3]	0 = Remote device not ready for transfer 1 = Remote device is ready for transfer

Bit 3 displays parallel port pin 6 (external Transfer Enable In) AND'ed with Command bit 4.

Oversample Error [Bit 4]	0 = No error 1 = A/D triggered before EOC is done.

Bit 4 is cleared by disabling A/D conversions (Command Register bit 2)

FIFO Status Flags [Bits 7,6,5]	Bit 5: 0=FIFO is empty, 1= FIFO not empty Bit 6: 0=FIFO is half full, 1=less than half full Bit 7: 0=FIFO is full, 1=FIFO is not full

Note the negative true coding on these bits.

3.5 Channel Address Register (Write BASE + 2)

This 8-Bit, write-only register specifies the required analog input channel as well as the number of conversions per scan. The register is organized as follows:

15-8	7	6	5 4	3 2 1 0
x-x	Auto Incr	SSH Ctrl	Not Used	Channel Addr 3 2 1 0

Figure 3.3 Channel Address Register Bit Field

Channel Address Bits [3-0]	This 4-Bit address field provides for 16 different channel specifications. Therefore only bits 1 and 0 need to be used for the 4-channel analog modules (A,B,C) on this board. All 4 bits are used for DVME-614E. Only channel 0 available on 614D.

Simultaneous Sample/Hold Control [Bit 6]	0 = Sequential or single channel mode 1 = Simultaneous Sample/Hold mode (see Section 1.3)

In SSH mode, counter 0 must be programmed with the number of SSH channels (max = 4). One trigger is required per A/D scan.

Channel Address Autoincrement [Bit 7]	0 = Single channel (no increment) 1 = Sequence channel address at A/D conversion

Note: Input analog channel settling time is a major factor as regards speed, when programming the DVME-614. In sequential channel mode (bit 7 = 1), or if the channel address bits are being rewritten after each sample, then the time for a static analog signal to be present at the A/D converter input is longer than in single channel scan mode (bit 7 = 0 and no address bit alterations). This obviously decreases the sample rates on each individual channel. For typical single channel and sequential channel settling times, refer to the Functional Specifications in Section 1.4

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3.6 D/A Data Register (Write BASE + 4)

Note: There is no D/A channel on the DVME-614D.

This 16-Bit register latches host VMEbus data into the DAC to provide a general purpose analog output or to set the trigger level threshold on the level-triggered comparator. Since the on-board DAC has 12-Bit resolution, only twelve bits of this register are used. The data is right justified and the 'x's, in Figure 3.4, for most significant nybble data indicate "don't care" bits. (In DAC terminology, Bit 1 is the MSB.)

15 12	11	10	2	1	0
x - x	DA1 MSB	DA2 ------	DA10	DA11	DA12 LSB

Figure 3.4 D/A Data Register Bit Field

3.7 FIFO Reset Register (Write BASE + 6)

Writing to this 16-bit register will reset the FIFO's

D15				D0
x	x	x ------ x	x	x

'x' indicates don't care

Figure 3.5 FIFO Reset Register Bit Field

Any write to this register will clear the FIFO and set the empty flag true (low) in the Status Register. If A/D conversion is still running, the FIFO will be not empty when the next A/D conversion (EOC*) completes.

3.8 Interrupt Vector Register (Read/Write BASE + 0Ch)

This register contains the interrupt vector for the DVME-614 board. If the IACK* level from the VMEbus matches the DVME-614 IRQ level, when an interrupt occurs, then the contents of this register are placed on the VMEbus data lines. From this the host calculates the start address of the interrupt service routine.

15 8	7	6	5	4	3	2	1	0
x - x	V7	V6	V5	V4	V3	V2	V1	V0

'x' indicates don't care

Figure 3.6 Interrupt Vector Register Bit Field

This register may also be used to verify proper board addressing before interrupts are enabled. Write and read back a range of values into the bits 7 - 0.

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3.9 FIFO Data Register (Read BASE + 0Eh)

Raw A/D data is temporarily latched by this register for host read operations.

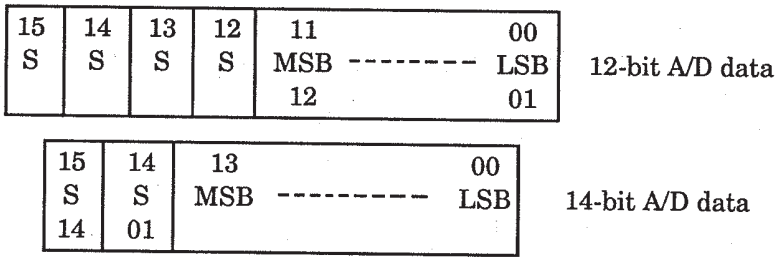


Figure 3.7 FIFO Data Register Bit Field

"S" bits are sign-extended from either bit 11 (12 bit A/D's) or bit 13 (14-bit A/D's) in bipolar input ranges. For unipolar ranges, S = 0.

3.10 Internal Programmable Timer

[Refer to Section 4 and Appendix A for operational details]

The 82C54 programmable timer contains three counters, each individually programmable for different speeds. Each counter on the DVME-614 board functions as:

Counter #0: This specifies the number of conversions per scan - up to a maximum of 65,536. If more samples than this maximum are required, this counter should be disabled , leaving operation under software control (refer to Section 5.13). THE NUMBER LOADED INTO COUNTER #0 SHOULD BE 1 LESS THAN THE NUMBER OF CONVERSIONS REQUIRED PER SCAN. The End Of Conversion pulse (EOC*) from the ADC provides the clock, the gate is controlled by the Acquire flag and its output is the End Of Scan signal (EOS*).

Counter #1: This specifies the conversion rate , its output being the A/D's start conversion pulse, negated. As with counter #0, the gate is controlled by the Acquire flag and it is clocked by the 8MHz divided VMEbus clock or by an external clock input (the choice being jumper selectable, see Section 2.9).

Counter #2: This specifies the internal trigger frequency for starting A/D scans. It is clocked by 125 KHz, 250 KHz or 500 KHz clocks, (jumper selectable), and the gate is controlled by bit 2 from the Command Register.

Counter Registers

To specify the counter speeds there are three individual Counter Registers at the following address locations in the VMEbus host processor's address space.

Counter Register: (Read/Write BASE + 10h - Counter #0)
(Read/Write BASE + 12h - Counter #1)
(Read/Write BASE + 14h - Counter #2)

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The user loads the Counter Registers with 16 bit data, written in two separate bytes. When initialized, (after setting up the Control Word Register), the 82C54 counts down from this value to 0 or 1 (depending on the mode of operation) and then strobes a pulse. The Control Word Register specifies if this count is in straight binary or in BCD. Therefore the data in this register determines the pulse periods of each of the three counter outputs.

Note: Counter values and status can be read back at any time during the counting process using the Readback and Latch commands as described in Section 4.1.

15 8	7	6	5	4	3	2	1	0
x - x	C07	C06	C05	C04	C03	C02	C01	C00

'x' indicates don't care

Figure 3.8 Counter Register Bit Field Control Word Register (Write BASE + 16h)

The Control Word register is a byte-wide register that specifies which counter is being accessed, the Read/Load operation to be performed and the type of counting procedure to be implemented i.e. straight binary or BCD.

15 8	7	6	5	4	3	2	1	0
x - x	SC1	SC0	RL1	RL0	M2	M1	M0	BCD

'x' indicates don't care

Figure 3.9 Control Word Register Bit Field

Select Counter [Bits 7, 6]	SC1	SC0	
	0	0	Select counter #0
	0	1	Select counter #1
	1	0	Select counter #2
	1	1	Read back command

Read/Load [Bits 5, 4]	RL1	RL0	
	0	0	Counter latch operation
	0	1	Read/Load LSB only to the Counter Register
	1	0	Read/Load MSB only to the Counter Register
	1	1	Read/Load LSB then MSB to the Counter Register

Mode [Bits 3, 2, 1]	M2	M1	M0	
	0	0	0	Mode 0 Operation
	0	0	1	Mode 1 "
	X	1	0	Mode 2 "
	X	1	1	Mode 3 "
	1	0	0	Mode 4 "
	1	0	1	Mode 5 "

BCD [Bit 0]	BCD	
	0	16-bit binary count
	1	4-decade binary coded decimal count

Note: See Section 4 and Appendix A for detailed operational and functional descriptions of the 82C54 programmable timer, as well as some example configuration outlines and code listings.

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3.11 Memory Access and Addressing

On some Operating Systems, you will not be able to make memory access to the DVME-614 board until you allocate some memory space to it. This is not the family of 'alloc()' functions in the "C" language, because the 'alloc' call does not tie a specific physical address to an allocated block. Check your Operating System documentation for the proper function. Some systems may even need a device driver for this allocation function because the Operating System needs to know about it at boot up time.

All the DVME-614 registers require the absolute physical memory address. In some Operating Systems, (notably UNIX), you must convert the physical address into a logical address using a conversion function supplied with it. These function types vary between Operating Systems and have names such as phy(addr), map(addr), mmap(), valloc(), etc.

3.12 Transferring Software

DATEL's standard software distribution media are 5.25-inch, 360K IBM-PC (MS-DOS) floppy disks. The software is provided in plain-text, commented ASCII source format. This avoids problems with binary files for specific computers. The software can be printed out, copied, modified, or included in the user's application as long as it is used with DATEL's boards. The code is highly portable and contains very few system-specific functions. Most programs are in the "C" language. For other languages, follow the comments in the "C" code to understand the program sequence.

To transfer the software, connect the PC-compatible computer to the VME computer using the RS-232-C serial ports and a null-modem cable. A straight-through cable may be used if one end is pinned out as a DCE device and the other is a DTE. Otherwise a crossover cable will be needed. The baud rates, parity and stop bits must agree on both computers. Compatible file transfer programs will be required on both computers. The public domain Kermit and XMODEM protocols work well and are error-correcting. On some computers, you may only have a buffer capture file transfer facility. Some transfer errors may result. If all else fails, type in the software using your text editor.

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82C54 PROGRAMMABLE TIMER

4.0 General Description

The 82C54 is a CMOS programmable interval timer containing three individual 16 bit counters that can count at speeds up to 10 MHz. The timer features six different counter modes and all timer modes and functions are fully programmable by the host VME data bus. 82C54 functions are pre-selected by a Control Word register and initial counter data is written to the Counter Registers - one for each counter.

4.1 Functional Description

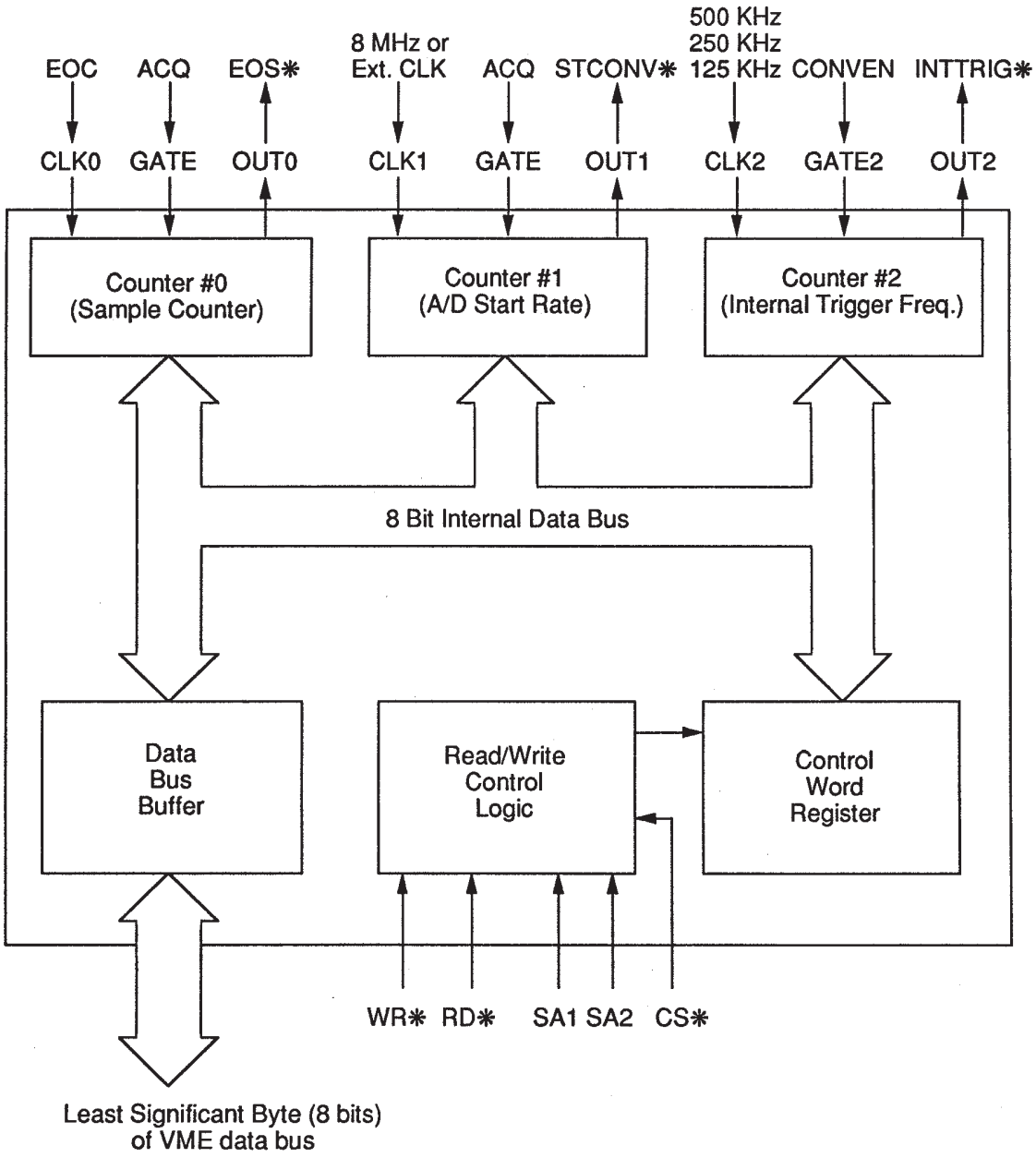


Figure 4.0 82C54 Programmable Timer

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Figure 4.0 is a functional block diagram of the 82C54 timer chip. The Control Word Register controls the operation of the timer. Functions are selected using 8-bit control words written to the Control Word Register by the host computer. This register in turn configures the operation of all three counters. Each counter data register is then loaded with a 16-bit initial value by the host. On the next input clock signal this initial data is loaded into the counters and counting commences. The output pulse duty cycle and frequency depends on a particular counter's mode of operation - refer to Section 4.2 for details.

NOTE: Control words must always be written before counter data!

Control Word Register

Each counter's operating mode is configured by control word programming. The format of the control word is shown in Figure 4.1.

15 - 8	7	6	5	4	3	2	1	0
x....x	SC1	SC0	RL1	RL0	M2	M1	M0	BCD

'x' indicates "don't care" bits

Figure 4.1 Control Word Register

Select Counter	SC1	SC0	
[Bits 7, 6]	0	0	Select counter #0
	0	1	Select counter #1
	1	0	Select counter #2
	1	1	Read Back command

The Read Back Command may be used to monitor the counter status at any time during operation - see later for details.

Read/Load	RL1	RL0	
[Bits 5,4]	0	0	Counter latch operation - stores a given counter's output value for host reading. This value is held until read by the host.
	0	1	Read/Load a counter with its 8-bit LSB initial data value.
	1	0	Read/Load a counter with its 8-bit MSB initial data value.
	1	1	Read/Load a counter with its 8-bit LSB followed by its 8-bit MSB initial data value.

Note: A bit setting of '1 1' means loading the initial count value in two data bytes - one 8-bit write followed by another 8-bit write. It does NOT mean the host can write a 16-bit data word to the 82C54 - simply because the Counter data Registers are physically only 8 bits wide.

Mode Select	M2	M1	M0	
[Bts 3..1]	0	0	0	Mode 0, event counter.
	0	0	1	Mode 1, programmable one-shot.
	X	1	0	Mode 2, rate generator.
	X	1	1	Mode 3, square wave generator
	1	0	0	Mode 4, software triggered strobe.
	1	0	1	Mode 5, hardware triggered strobe

These bits select the mode of operation of each counter on the 82C54 timer. Each mode is dealt with in detail in Section 4.3 and Appendix A.

BCD		
[Bit 0]	0	Straight binary count
	1	BCD count

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Read Back Command

The Read Back Command enables the user to check the count value, program mode, output pin state and null count flag of each counter.When this command is written the format is as shown in Figure 4.2.

D7	D6	D5	D4	D3	D2	D1	D0
1	1	CNT	STS	CNT2	CNT1	CNT0	0

Figure 4.2 Read Back Command Bit Field

D5: 0 = Select counter latch operation -setting this bit to '0' stores the specified counter's value at a given instant during counting for reading by the host computer.
D4: 0 = Select counter status latch operation - setting this bit to '0' will latch the status information of each counter.
D3: 1 = Counter #2 selection
D2: 1 = Counter #1 selection
D1: 1 = Counter #0 selection

Read-Back Status

The read back status format is as follows:

D7	D6	D5	D4	D3	D2	D1	D0
O/P	NCNT	RL1	RL0	M2	M1	M0	BCD

Figure 4.3 Counter Status Read Back Format

D7: This bit indicates the status of the output pin.
0 = The output is low
1 = The output is high

D6: Null Count pin indicates that the count value written in the Counter Register, (i.e input data register), has been loaded into the counter. Counting can now begin on the next clock pulse - depending on the mode of operation and on the gate signal level.
1 = Control Word and/or Counter Register data already written but data not yet loaded into the counter to enable operation.
0 = Initial count value now loaded into the counter and counting is enabled.

D5..D0 Same as the corresponding bits in the Control Word Register.

Counter Register

After writing the Control Word Register load the Counter Register with the initial counter data. The Counter Register bit format is a follows:

15....8	7	6	5	4	3	2	1	0
Not Used	C7	C6	C5	C4	C3	C2	C1	C0

Figure 4.4 Counter Register

C7..C0 [Bits 7...0] Initial counter value data bits. Note that this is only an 8-bit register. 16-bit data is written as two bytes - controlled by bits 5 and 4 in the Control Word Register. Setting both of these to '1' and writing two bytes to the Counter Register will load the Register with the Least Significant Byte first, then the Most Significant Byte.

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4.2 82C54 Modes of Operation

There are six different modes of operation for each of the three counters in the 82C54. These are specified by bits D3, D2 and D1 in the Control Word Register - as illustrated in Section 4.1. On the DVME-614, Mode 2 is used for continuous internal A/D triggering, Mode 4 is may be used to disable the sample counter and Mode 5 is used for generating single internal A/D triggers. These three modes are now outlined in detail. All modes are detailed in Appendix A.

In the following descriptions of the 82C54 timer modes the term 'Counter Element (CE)' is constantly used. This refers to the counter itself, as opposed to the Counter Register which is just a data register/latch for the data. Data is first latched into this register and then loaded into the counter later. Obviously, no counting can occur until the initial value is loaded into the counter proper. This usually happens on the next falling clock edge after writing the data to the Counter Register (or after a gate trigger, depending on the mode of operation). This 'loading', clock edge does not decrement the initial count value.

Mode 2 - Rate Generator

Control Word setting asserts the output high. When the count decrements to 1 the output goes low for the duration of one clock period and then returns high again. The initial count value is then reloaded into the counter and the sequence restarts. If the initial count value is N, then the sequence repeats at intervals of N clock pulses.

A high level on the gate validates counting while a low invalidates counting. On the falling edge of the gate signal the output goes high and counting terminates. The rising edge of the gate retriggers the counter i.e. the old initial value is reloaded, or, if a new value has been written by the host, the new initial count value is loaded on the next falling clock edge. If a new value is written to the Counter Register during a count sequence it is loaded into the Counter Element either after gate retriggering or when the present count sequence terminates.

NOTE: In mode 2, a count value of 1 is prohibited

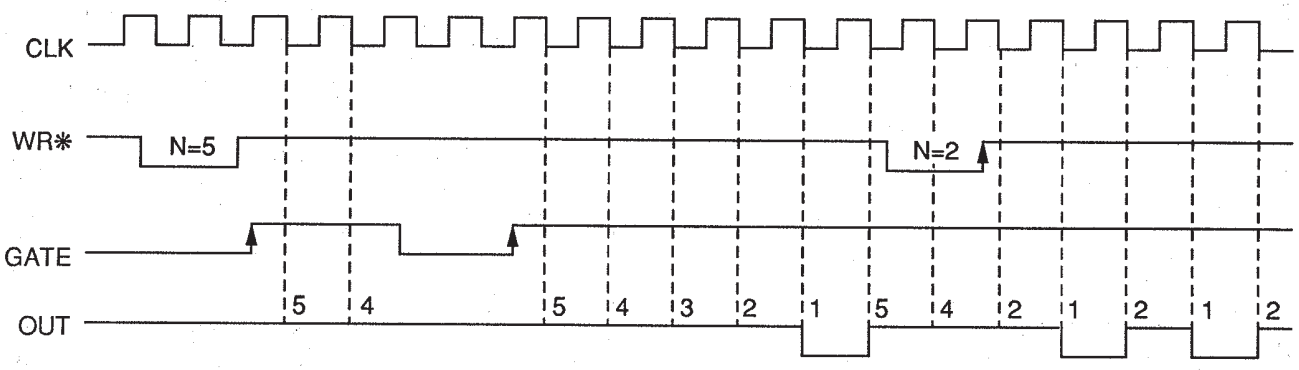


Figure 4.5 Mode 2 Timing Diagram

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Mode 4 - Software Triggered Strobe

Mode 4 may be used to disable the sample counter if an application requires digitizing more than 65,536 sample points. This is accomplished by writing the Control Word Register to configure Counter 0 for Mode 4 operation and writing no initial counter data to the Counter Register.

After Counter Register writing and Counter Element loading with an initial data value the output goes high. When the counter value decrements to '0' the output goes low for one clock period and then returns high.The count sequence restarts only when a new initial count value is written to the Counter Register by the host.

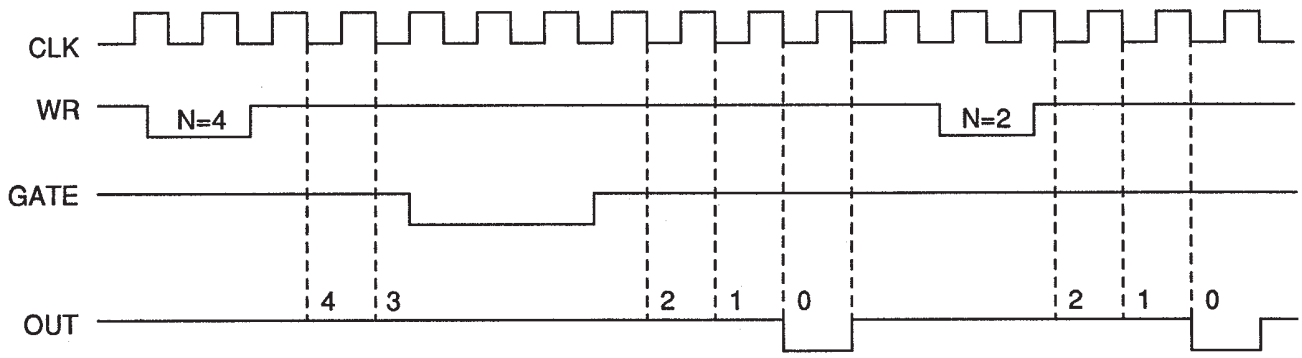


Figure 4.6 Mode 4 Timing Diagram

Mode 5 - Hardware Triggered Strobe

On the DVME-614 Mode 5 is used for generating single internal triggers and operation is based on triggering by the rising edge of the gate signal. The gate is hardwired to bit 2 in the Command Register, i.e. the A/D Convert Enable bit. Therefore, a single write to the Command Register to enable A/D conversions triggers the counter and generates one internal trigger.

When the Counter Element is loaded with the initial data, (on the falling clock edge after the gate trigger), the output is set high and counting commences. The loading clock pulse does not decrement the initial count value. When the count reaches '0' the output goes low for one clock period and then returns high. New data or old data reloading occurs only after another gate trigger.

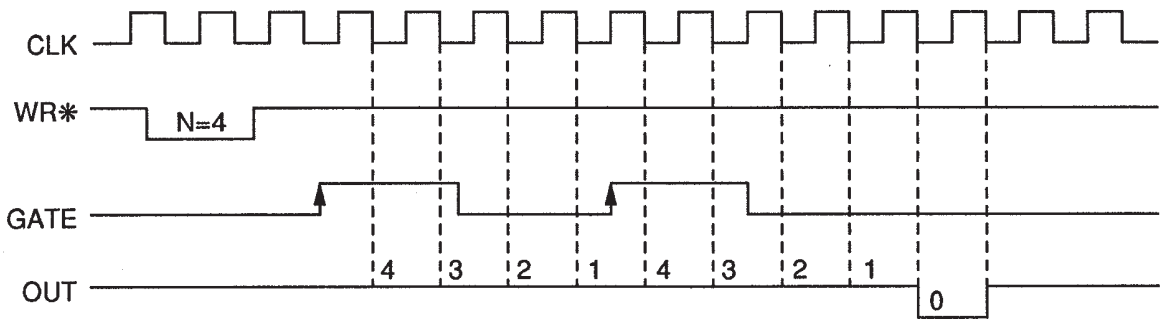


Figure 4.7 Mode 5 Timing Diagram

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4.3 82C54 Programming Guide for the DVME-614

Note 1: The timer value registers are eight bits wide. The counter value must be divided into an eight bit LSB and an eight bit MSB. The timer counter registers expect the LSB to be loaded first, followed by the MSB.

Note 2: The actual number loaded into timer # 0 must be 1 less than the desired number of conversions per trigger. For any of the three counters operating in Mode 2, the minimum initial count value that can be loaded into the Counter Register is 2 - *a count value of 1 is prohibited in Mode 2.* Thus, due to the counter timings, the minimum possible number of conversions per trigger on the DVME-614 is three. (Refer to timing diagram in Section 5.4)

In the following examples: CLOCK1 = 8 MHZ
CLOCK2 = 500 KHZ

Single Internal Trigger:

Counter #2 specifies the trigger rate. If only one trigger is required then this counter must be configured for operation in Mode 5. In this mode, a single write to the Command Register to enable A/D conversions, (bit 2 = 1), generates this single trigger.

Load the following hexadecimal numbers into the Control Word Register:

Load $3C at Base+16h	Timer#0, R/L LSB then MSB,Mode 2, Binary Count
Load $7C at Base+16h	Timer#1, R/L LSB then MSB, Mode 2, Binary Count
Load $6A at Base+16h	Timer#2, R/L LSB then MSB, Mode 5, Binary Count

Load xxxx at Base + 10h	Timer #0 counter
Load yyyy at Base + 12h	Timer #1 counter
Load zzzz at Base + 14h	Timer #2 counter

xxxx = The number of conversions per Trigger - 1
yyyy = CLOCK1/(Conversion rate in HZ)
zzzz = CLOCK2/(Trigger rate in HZ)

(See Example #1 in Section 4.4)

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Continuous Internal Trigger

In this mode, Counter #2 (the trigger rate specifier) is set up for operation in Mode 2. When the counter decrements from the initial count value to 1 the output goes low for one clock. The Counter Element reloads the initial value and the sequences restarts. Internal triggering continues until Counter 2 is disabled by resetting bit 2 in the Command Register to 0. A/D conversions are disabled when Counter 0 generates an End of Scan (EOS*).

Load $3C at Base+16h	Timer#0, R/L LSB then MSB, Mode 2, Binary Count
Load $7C at Base+16h	Timer#1, R/L LSB then MSB, Mode 2, Binary Count
Load $BC at Base+16h	Timer#2, R/L LSB then MSB, Mode 2, Binary Count

Load xxxx at Base + 10h	Counter Register #0
Load yyyy at Base + 12h	Counter Register #1
Load zzzz at Base + 14h	Counter Register #2

xxxx = The number of conversions per Trigger - 1
yyyy = CLOCK1/(Conversion rate in HZ)
zzzz = CLOCK2/(Trigger rate in HZ)

(See Example #1 in Section 4.4).

External Trigger

An external trigger event starts the A/D conversion process. Bits 0 and 1 in the Command Register specify this DVME-614 external trigger mode and the Control and Counter Registers for each counter can be configured to generate a single internal trigger, or continuous internal triggers - on receiving the external strobe. Hence, the 82C54 configurations are identical to those outlined above.

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4.4 82C54 Timer Configuration Example

Example #1

To program the 82C54 timer for the Internal Trigger mode:
The Internal Trigger will have a frequency of 10Hz.
The conversion rate will be 200KHz.
The number of conversions per Trigger will be 512.

```
#include (stdio.h)
#define Base 0xFA0000

unsigned short *Control_word;
unsigned short *counter0, *counter1, *counter2 ;
unsigned short count_value;
unsigned long CLOCK2, CLOCK1, trig_freq,conv_freq, number_convs;

main()
{

  CLOCK1 = 8000000L;                          /*  counter #1 clock input freq. = 8MHz   */
  CLOCK2 = 500000L;                           /*  counter #2 Clock input freq. = 500KHz */
  Control_word = (unsigned char *)(Base + 0x16);  /*  Control Word Register address */
  counter0 = (unsigned short *)(Base + 0x10);     /* address of timer # 0 Counter Register */
  counter1 = (unsigned short *)(Base + 0x12);     /* address of timer # 1 Counter Register */
  counter2 = (unsigned short *)(Base + 0x14);     /* address of timer # 2 Counter Register */

                /* * * * * * * * * * * * * * * * * * * * * */
                /*          Programming Timer counter # 2          */
                /*          Internal Trigger Frequency             */
                /* * * * * * * * * * * * * * * * * * * * * */

  trig_freq = 10L;                            /*  internal trigger freq = 10Hz   */

  count_value = (unsigned short)(CLOCK2/trig_freq);
  *Control_word = 0xBC;                       /* Counter 2, Load LSB then MSB, Mode 2,
                                                 Binary Count */

  *counter2 = count_value % 256 ;             /*  load LSB */
  *counter2 = count_value / 256 ;             /*  load MSB */
```


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```
                    /* * * * * * * * * * * * * * * * * * * * */
                    /*          Programming Timer counter # 1        */
                    /*          Conversion Rate Frequency            */
                    /* * * * * * * * * * * * * * * * * * * * */

    conv_freq = 200000L;            /* conversion rate of 200KHz  */

    count_value = (unsigned short)(CLOCK1/conv_freq);
    *Control_word = 0x7C;           /* Counter 1, Load LSB then MSB, Mode 2, Binary count */

    *counter1 = count_value % 256;  /* load LSB */
    *counter1 = count_value / 256;  /* load MSB */


                    /* * * * * * * * * * * * * * * * * * * * */
                    /*          Programming Timer counter # 0        */
                    /*          Number of conversions per trigger    */
                    /* * * * * * * * * * * * * * * * * * * * */

    number_convs = 512 - 1;         /* must load one less than required  */

    count_value = number_convs;
    *Control_word = 0x3C;           /* Counter 0, Load LSB then MSB, Mode 2, Binary count */

    *counter0 = count_value % 256;  /* load the LSB */
    *counter0 = count_value / 256;  /* load the MSB */

}
```

In a practical application, after configuring the individual timers as shown above, the next step is to write input channel sequencing information to the Channel Address Register. Then, reset the FIFO's by writing to the FIFO Reset Register. Finally, specify the trigger and interrupt sources, enable interrupts and start A/D conversions - all done by writing to the Command register. Either by configuring the FIFO Half Full Flag (HF) as an interrupt or by polling the Status Register, (bit 6), block transfer the raw A/D binary data to host memory buffers - when the HF occurs. The A/D conversion process terminates when the pre-specified number of conversions are complete, or it can be stopped by the host by resetting bit 2 in the Command Register at any time.

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DVME-614 APPLICATIONS

5.0 Sampling Rate Theory

The DVME-614 forms part of a switched-channel, sampled data acquisition system. In order to fully recover a continuous band-stopped signal on any channel, that channel must be sampled at more than twice the frequency of the input signal's highest frequency spectra. If it is not sampled fast enough, periodic magnitude errors may occur from alias frequency folding. This requirement is also variously referred to as the Nyquist criteria.

As a practical matter, this sampling theory does not merely say to sample at more than twice the frequency of interest. It says to be sure there are NO input frequency components present at more than half the sample rate. For a moderate bandwidth input with unpredictable spectral content, users must employ an external hardware filter on each channel to sharply attenuate signals well below the upper frequency limit.

5.1 Averaging High Gain Data

With long signal leads, somewhat increased noise may be apparent in the data. The high speed sampling A/D converter will pick off random portions of the combined signal and noise and will then faithfully convert that signal. A suggested technique is to convert a number of samples, then average the data. If you collect a power-of-2 number of samples, a root-2 shift right will do a quick average. (Example: sum 8 samples, then right shift 3 bits). This avoids floating point operations in assembly language. Using this method while locked on one channel, starting with the second sample, you can avoid the 1 to 2 microsecond settling delay normally needed after switching the channel address.

5.2 Unused Input Channels

The input multiplexer uses an extremely high impedance design. Avoid switching through any disconnected input channels at high speed. If the channel is not connected to any input signal, tiny bias currents from the MUX and PGA will force that channel into full scale saturation. This will not damage the inputs but may cause overload recovery time problems if you quickly switch and convert on an active channel. If you must sequence through disconnected channels, terminate them using high value, input resistors, (say 1 Megohm), to signal ground. This will prevent input saturation. Otherwise, wait a longer settling period before starting the next A/D conversion.

5.3 VMEbus Interrupt Operation

Before you try VMEbus interrupts, always get your application to run flawlessly in status polled mode, without VMEbus interrupts.

The following is a quick checklist for DVME-614 to VMEbus interrupts:

1. Are the desired VMEbus IRQ line and the IRQ code switches properly selected? Do other boards share the same IRQ lines? Are they closer to the CPU board and therefore have they higher hardware priority?

2. Is bit 5, 6 or 7 of the Command Register (BASE+0) set to 1 to enable the required interrupt? Is the Command Register A/D enable bit (Bit 2) set to 1?

3. Is the CPU board, which will handle the 614 interrupt, also the current bus master? Interrupts sent to the wrong CPU board master will have undefined results. Remember that the IRQ lines are read by all CPU's.

4. Is the vector ID loaded in the Interrupt Vector Register at BASE+0C on the 614 ? This should be the ISR longword address (or VBR longword offset) divided by 4 (2 right shifts with zero MSB fill). Note that the Motorola vector ID's are given in decimal. For ID 64, load $40 hex meaning ISR address offset $100 hex.

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5. Is the 614 really sending VMEbus interrupts? Confirm with an oscilloscope on the interrupt lines. If you get spurious interrupts, the hardware is probably working but the ID or ISR or Real Time OS (RTOS) setup and allocation is probably faulty. Get your DVME-614 host program to work properly without interrupts first, under polled status mode.

6. Is the the host CPU Vector Base Register loaded properly? Is the user-written host interrupt service routine loaded in memory at the the absolute address pointed to by the host CPU VBR plus the vector ID code times 4? If necessary, compare your ISR list file with the disassembly from your host debugger. In the case of a Real Time Operating System, verify priorities, task initialization, memory allocation, etc., etc.

7. What exactly does your ISR code do? At the very least, it should signal the OS (perhaps with a message structure, flag or mailbox) that the 614 interrupt has occurred and what the resulting action is going to be e.g. abort the program if the FIFO Full flag is set. Does your ISR disable other interrupts, then re-enable them? Does your ISR finish with 'RTE'? Are registers properly LINKed and UNLKed? Is the interrupt priority mask properly managed and restored during the ISR? What are the consequences of another interrupt received while processing a DVME-614 transfer? Is your ISR fully re-entrant, with registers properly saved and restored? Within the ISR, will the address modifier switches allow DVME-614 access under priviledged supervisor mode?

8. The DVME-614 asserts an 8-bit vector ID code only on data lines D0-D7. Some recent implementations of the VMEbus interrupt may look for 16 or 32 bit interrupt codes. Most CPU boards should be able to accomodate the 8-bit ID code.

9. Are the IACK*, IACKIN* and IACKOUT* lines daisy-chained on board slots between the DVME-614 and the CPU board? For empty slots, make sure these lines are jumpered on the backplane.

5.4 DVME-614 Timing Considerations

Before incorporating the DVME-614 data acquisition board into an application, it is very important that the user fully understands the board level, A/D control signal inter-relationships/timings. 82C54 programmable interval timer operation, which is the focus center of the more important DVME-614 timing signals, is dealt with in detail in Section 4 and in Appendix A.

When internal triggering is used on the DVME-614, all the control signals generated by the 82C54 timer are phase synchronous with both the clocks and the trigger strobes. Therefore, 82C54 inputs and outputs are analogous to those illustrated in Section 4 of this manual - with Counter 0 and 1 operating in Mode 2, and Counter 2 operating in Mode 2 or Mode 5.

However, when external triggering is used, then the trigger signal becomes asynchronous with the on-board timer clocks. This introduces skew delays between the trigger signal and the start of conversion pulse, as illustrated in Figure 5.0a & 5.0b. The sample clock (CLK1) is the 8 MHz divided VMEbus SYSCLK, ACQ is the gate signal for both Counters 0 and 1 and EOC* clocks Counter 0 - the output of which is EOS* (see DVME-614 schematics in Appendix B). The occurrence of the trigger in relation to the sample clock is arbitrary. Assume that a Counter value of 3 has been written to Counter Register 0, (i.e. 4 samples per trigger), just before the trigger event. Because of the way the timer operates, this value will be loaded into the Counter Element on the falling edge of the first EOC* pulse after the trigger. Similarly, on the sample clock falling edge, after the ACQ trigger, the initial sample period value is loaded into Counter 1. When this decrements to 1, (driven by the 8 MHz or an external clock), the output goes low. This generates a start convert pulse for the A/D converter. The output returns high after one clock period and the initial count value reloads. This process continues until the sample count is reached - Counter 0 generates an End of Scan (EOS*).

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From this example, obviously the maximum skew delay between the trigger and loading of the sample period value into Counter 1 is one sample clock period. The minimum length of time from loading this value until the output goes low is the value minus 1 times the sample clock period. That is, the maximum delay from the external trigger to the first start convert pulse is the initial value in Counter 1 multiplied by the sample clock period.

Note: To maintain phase synchronizm in external trigger mode and to minimize skew delays, the solution is to also use an external A/D sample clock - which is in phase with the trigger signal. While this eliminates the skew delays, there still remains the clock times for loading counter data and counting to occur. However, this delay from the synchronous trigger event to the first start convert pulse can be calculated, (and thus compensated for) - since it is solely based on fixed clock periods.

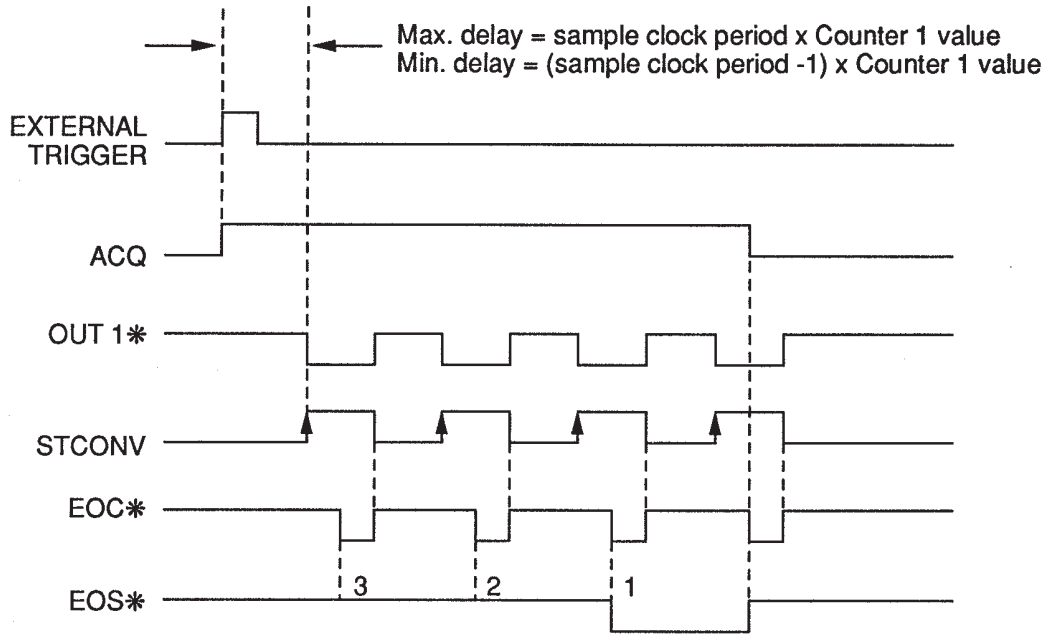
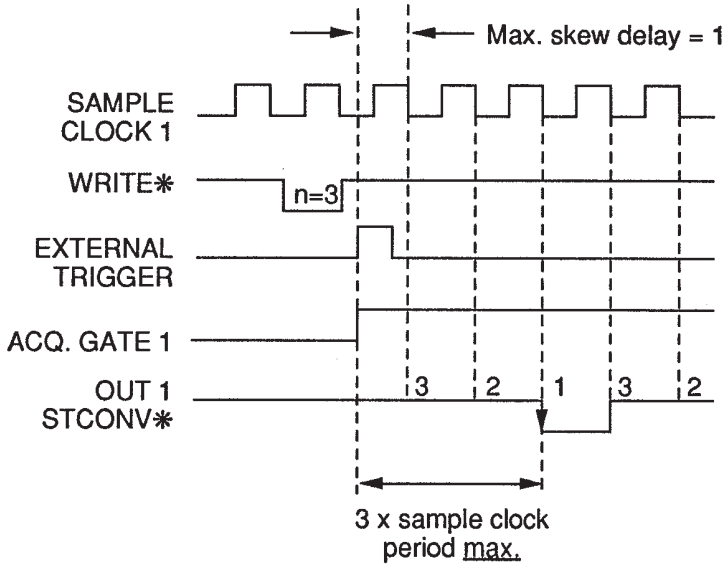


Figure 5.0a External Trigger Timing Diagram



Note: An initial value of 3 yields an A/D conversion rate of 2.66 MHz and is only possible on the DVME-614D. Higher initial values must be written for DVME-614A,B,C, and E.

Figure 5.0b External Trigger Skew Delay

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5.5 FIFO Transfer Strategies for Seamless Data

The following discussion covers applications where the number of contiguous A/D samples is larger than the FIFO size or the A/D triggering runs non-stop ("forever"). The A/D trigger rate is assumed to be constant. This discussion is very important because of the speed limits of the VMEbus.

There are several ways to read data from the FIFO. These methods trade off speed versus availability of the host system for other tasks. The highest possible speed occurs by polling the FIFO Half Full flag (HF) in assembly language and then doing the block transfer without using a HF interrupt. Here is the most standard method.

1. Set up the Timer, Channel address and Command registers. Program the interrupt and DMA systems if used.

2. Start A/D conversions.

3. Poll the FIFO Half Full flag (HF) or wait until a HF interrupt. Note the negative true coding of all the FIFO flags.

4. This step is optional. When HF is true, test the FIFO full flag (FF). In the event that transfers have not kept up with FIFO data, the full flag may have been set sometime after the HF flag was set. Poll the full flag at this time and report a lost data error if FF is true. Note that it is possible for FF to go true just AFTER it is polled, thereby missing the overflow error. The most efficient and failsafe way to catch the FF error is to configure it as a hardware interrupt - this ensures it is caught and eliminates the overhead of polling the FF flag.

5. With HF true, block transfer half the FIFO to a host buffer array. For a 4096-sample FIFO, the HF flag guarantees at least 2048 samples available in the FIFO. The FIFO will collect spill A/D samples while you are doing the block transfer.

The block transfer should be done at the highest possible system speed to achieve maximum system offloading. Use a DMA controller if available. Otherwise use a tight assembly language loop with register pointers to the source data register and incrementing destination memory array. Use a decrementing CPU register as a block size counter. See the following software example.

```
        movea.l   #FIFO,A0          ;load FIFO data register address
        movea.l   #BUFBASE,A1       ;load base address of memory buffer
        move.l    #count-1,D0       ;load number of samples to transfer
LOOP:   move.w    (A0),(A1)+        ;transfer data and bump address pointer
        dbf       D0,LOOP           ;repeat if count is not reached
        rts                         ;dbf exits at  D0 < 0
```

The block move-dbf loop takes 30 clocks on a 680x0 CPU. At 33 MHz, this is about 1 microsecond. Additional time may be needed for VMEbus arbitration. Use DMA, a RISC CPU or the parallel port for higher speed.

6. If more samples are needed, reprogram the CPU or DMA controller then go to step 3. Remember to advance the buffer pointer if you are filling a large buffer.

7. Exit when done.

Notice that the empty flag is never polled.

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5.6 Data Transfer Speed Enhancement - Method 1

Once half the FIFO is block transferred, the FIFO will not be empty since it collected A/D spill samples during the block transfer. Immediately after the block transfer, while still in the Service Routine (SR), poll the empty flag (EF). Start reading FIFO samples as long as the FIFO is not empty. When empty, exit the routine and resume polling the HF bit.

Polling EF and transferring single samples is significantly slower than the block transfer. However, this double method may offer slightly greater overall system throughput. The reason is that the system is already executing the service routine, registers have been saved and the time required to do an Operating System context switch may favor collecting the spill samples left in the FIFO.

On the other hand, if A/D triggering is faster than the poll-EF loop, this loop may never exit. It will eventually allow the FIFO to overflow. By configuring the FIFO FF flag as an interrupt source, the program will abort on overflow - displaying the appropriate error message on the host terminal.

5.7 Data Transfer Speed Enhancement - Method 2

Another alternative is to block transfer a larger number of samples than half the FIFO when HF occurs. Using a block size too large will collect empty FIFO data. You will need to do some testing to determine whether you are over-reading the FIFO. A suggested method is to use a very precise triangle wave analog input signal. The output data should show an almost constant number of counts difference between successive samples. At the triangle peaks, the sample-to-sample difference changes polarity and the absolute value difference may be less than for other samples. Any discontinuities (large sample-to-sample differences) in the reconstructed signal indicate lost samples due to insufficient speed in transferring from the FIFO.
An experimental way to test for how large the HF block size should be is the following:

Assuming non-stop A/D triggering, start a block transfer of "N" samples at the HF, where "N" is larger than half the FIFO. Immediately test the EF after the block transfer. Since the A/D is busy filling the FIFO, your system may not be fast enough to detect the EF. Use another CPU register as a pointer to the Status Register to retain speed when testing the EF. Set up this pointer before the block transfer. The other alternative method is to use the EF as an interrupt, thus making sure that the flag assertion is not missed by the host processor.

If EF was not empty, increment the value "N" and try another block at the next HF. If A/D triggering is not too fast, eventually EF will be true. This will mean that the FIFO was over-read. Report the value of "N" to the screen so you will know how filled the FIFO is before the block size failed.

Now reduce the value "N" by several samples until you have a safe amount that will not over-read. For very fast triggering, you may find that "N" is most of the size of the FIFO, meaning that your system is just slightly faster than the A/D.

Make sure you understand the frequency of all system interrupts during these FIFO block transfers (or turn off all possible interrupts). If several interrupts occur while servicing the HF interrupt, you may lose data. Also, for disk writes, be aware of the fragmentation of the disk. Excessive seek variation for scattered sectors will risk data loss.

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5.8 External Parallel Port Transfers

Data transfers using the external parallel port must be initiated and controlled using the DVME-614 interrupts or registers. The parallel port itself has no command function to start and stop each block. The port only has handshake lines to synchronize each word transfer. The parallel port uses a very simple, universal interface which may be adapted to many devices. A typical interface would use a high speed parallel port on a CPU/RAM board which can be dedicated full time to the A/D FIFO port.

The asynchronous port handshakes can be enabled or disabled using Command Register bit 4. With bit 4=0, the ready output will not be asserted and acknowledge input will not cause a read of the FIFO to get the next sample word.

The port should not be operated with the external receiver doing uncontrolled polling of the ready line, since there is no hardware mechanism to avoid reading an empty FIFO. The preferred approach is to have host software initiate a fixed-length block transfer when the Half Full FIFO flag occurs. This means that the host must be able to set the block length counter on the parallel receiver and to start transfers.

The parallel port transfer should be treated similarly to the VMEbus transfer. That is, a fixed number of samples, (half the FIFO size or more), should be read using a counter on the parallel receiver.

At the HF flag, start the parallel receiver polling the ready output. When ready, start the actual transfer by reading the first data word into the receiver's buffer. Advance the buffer pointer, decrement the buffer counter and assert the acknowledge input from the parallel receiver. This will reset the ready output and cause the next read of the FIFO. Then test for the end of the block counter. When the next FIFO data word is available, ready will be set true again.

When writing DVME-614 Command Register bits, remember to leave all other bits in the Command Register set as they were before. If the A/D converter is accidentally disabled (Command bit 2=0), A/D sampling will stop. In your program, use a shadow register variable for the Command Register code. Modify the shadow variable then write the entire shadow to the Command Register.

5.9 External Transfer Enable Input

The external transfer enable input is provided so that the parallel receiver can control the ready flag and indicate to the VME host that the receiver is active. This input is optional. If pin 6 is not connected, the internal pullup resistor will force a TRUE state and the interface will only use the Ready/Acknowledge handshakes.

If pin 6 is not controlled by the external receiver, the ready output will be inhibited when pin 6 is low (FALSE). This will prevent reads of the FIFO and the transfer of data samples over the interface. This state can be detected by polling Status bit 3 for a low level. The host program can poll Status bit 3 and use it to start the parallel block transfer when Status bit 3 is high (TRUE).

It is important to note that the parallel interface can still attempt to read samples if the FIFO is empty. The FIFO flags have no effect on the hardware Ready/Acknowledge handshakes. These handshakes merely step the FIFO reads along asynchronously in time to the external parallel receiver. The maximum A/D data transfer rate over the parallel port is 4 MHz.

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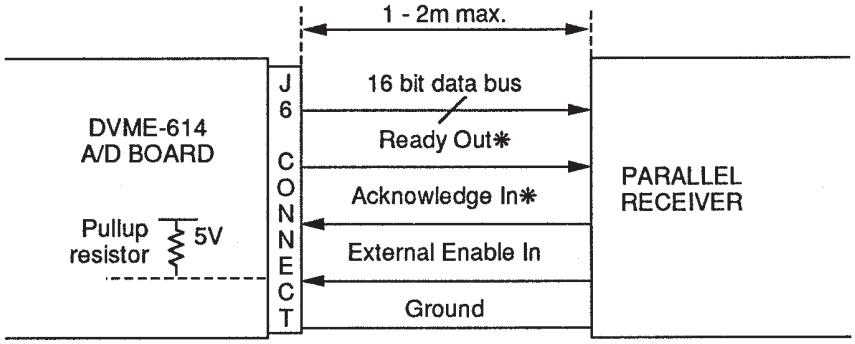
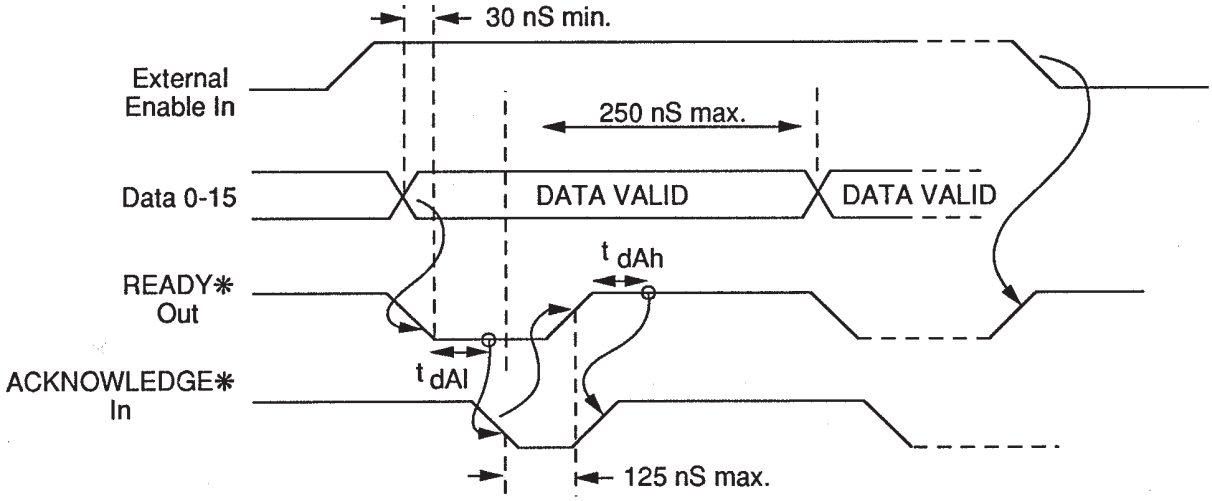


Figure 5.1 Parallel Port Connections



tdAl - time delay between READY going low and ACK. going low
tdAh - time delay between READY going high and ACK. going high

Figure 5.2 Parallel Outport Timing

5.10 Event Triggering

Many applications use a single external event to start high speed analog sampling. Sometimes the sampling activity cannot be precisely timed relative to the event. Three possibilities exist:

A. Analog sampling may be started shortly after the event but the exact delay is not critical.

B. Sampling must start after a fixed delay. This is called "post triggering".

C. Sampling must have started before the event and data must have been saved for some fixed interval or number of samples before the event. This is termed "pretriggering".

The DVME-614, combined with software, will accomodate all three modes.

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In all cases, the event is either an external digital or analog signal. The DVME-614 includes an on-board comparator to start A/D sampling after an analog reference signal crosses a given threshold. The reference threshold signal may be generated by the internal D/A converter or by an external analog reference input. The analog comparator input will also accept digital signals by setting the D/A reference level at the appropriate logic voltage levels.

5.11 Pretriggering

A pretriggered data acquisition system is one which is continuously performing A/D conversions before a particular external event occurs. This pre-sampled data is stored temporarily in a circular buffer in the host system and is constantly overwritten until the external event actually occurs. At this point, the raw A/D data is permanently stored, i.e. store in a linear buffer, and a specified number of pre-trigger samples are concatenated with them until the allocated buffer is full. When this happens the A/D conversion process may be halted ,or, if more samples are required, data may be written to mass storage devices e.g. magnetic disk. Typical applications of this procedure would be in situations where the exact trigger event time is not known and where some pretrigger samples are required to be stored for later processing purposes, e.g. recording seismic activity, astronomical and astrophysical experiments, etc.

The DVME-614 is ideal for implementing pretriggered applications. Configuration and control of the process is totally software dependent, as is the efficiency and transfer speed. Code may be written in any high or low level language and under almost any Operating System. The following setup and control procedure may be followed when developing user code for a specific pretriggering application.

1. Initially, the DVME-614 input trigger channel must be configured and host memory must be allocated for the circular buffer. Before the external trigger event happens, A/D conversions must continually be performed. Therefore the board must be configured for Continuous Internal Triggering (refer to Section4.3). However, the external event trigger source must be monitored and detected. One possible way to accomplish this is to connect the external trigger line to the External Analog Trigger input channel and poll bit 2 of the Status Register for a low to high transition. Because the trigger is connected to the analog input trigger channel. The comparator's threshold voltage level must be first set using the on-board DAC.

If the trigger is digital, set the threshold for 2.5V as follows:

```
BASE = 0XFA0000                          /*DVM-614 default address*/
unsigned short *dac_reg;

dac_reg = (unsigned short *)(BASE + 0x04);   /* DAC register address */
*dac_reg = 0xC00;                            /* 3/4 of full scale, assuming ±5V range */
```

Now, we need to allocate a specified portion of host memory to be used as a circular buffer for temporarily storing A/D data from the DVME-614 FIFO registers. This buffer will be continuously filled and over-written until the event trigger occurs, at which point overwriting will cease. All further data samples will be now stored in a linear buffer. The following code allocates memory for the circular buffer - a similar routine may be used for the linear buffer allocation.

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```
#include (stdio.h)
unsigned long *start, *head, *buf_strt_addrs, *finish;
unsigned long blocks, mem_size;
char *malloc();

main ()
{

printf(" Enter the circular buffer size as a number of 1024 byte blocks - 64 maximum" );

scanf("%l", &blocks);
mem_size = blocks*1024;

                              /* Next, allocate memory - a multiple of the FIFO size  */

start=(unsigned long *) (malloc(sizeof(unsigned short)*mem_size));
if(start==0)
     {     printf(" Not enough memory ");
           exit (0);                        /*abort*/
     }

head=buf_strt_addrs=start;                /* point at start address of buffer */
tail = (start) + (mem_size)-1;            /* point at end of buffer */
```

2. Next, the DVME-614 board must be configured for the correct mode of operation - continuous internal triggering until the required number of samples have been acquired. Because we pretrigger, we do not know the exact time when the trigger will occur and therefore the total number of samples per scan cannot be specified. Therefore the software must disable the End of Scan pulse being generated. This may be done by configuring Counter #0 for Mode 4 operation (Software trigger, see Section 4 on the 82C54 timer) and writing no Count Register data as follows:

```
unsigned short *control_word_reg, *counter0;
control_word_reg = (unsigned short *) (BASE + 0x16);

*control_word_reg = 0x38;                 /* Counter #0, Read/Load LSB then MSB, Mode 4, Binary
                                             counting */
```

Counter #1 specifies the conversion frequency and is configured for Mode 2 operation. Counter #2 specifies the internal trigger frequency and also operates in Mode 2:

```
*control_word_reg = 0x74;                 /* Counter #1, Read/Load LSB then MSB, Mode 2, Binary
                                             counting */

*control_word_reg = 0x64;                 /* Counter #2, Read/Load LSB then MSB, Mode 2, Binary
                                             counting */
```


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The Counter Register values may be input from the keyboard and written to the respective counters accordingly - LSB first, see Section 4.4.

3. Now, set up the Command Register for internal trigger on the falling trigger edge, select VMEbus Data Register (as opposed to the parallel outport), specify FIFO Full Flag as an interrupt, enable interrupts and start A/D conversions. The FIFO Full flag is specified as the interrupt source because if the FIFO fills it means that there will be a lot of data lost since the host processor cannot transfer the data from the FIFO fast enough. On the occurrence of the interrupt, simply display the error message and abort the program. The following code configures the Command Register and starts A/D conversions.

```
unsigned long *command_reg;
command_reg = (unsigned long *) (BASE + 0x00);      /* Point to the Command Register */

*command_reg = 0x45;                    /* Configure Command Register for continuous internal trigger, select
                                           VMEbus Data Register, enable FIFO Half Full interrupt and start
                                           A/D conversions */
```

While A/D conversions are continually being performed, bit 2 of the Status Register must be polled, for a low to high transition, to detect the external trigger event. Up to this point data is written to the allocated buffer on a circular basis (i.e. when the circular buffer fills, reset the 'head' to the start address and continue filling from there, thus overwriting the previously stored data). When the trigger occurs, all the succeeding samples must be stored in a linear buffer in the host. If enough host memory cannot be allocated to hold all the sample data from the FIFO, then block transfer the data to mass storage devices when the linear buffer fills. When the A/D conversion process terminates, concatenate the required number of pretrigger data samples from the circular buffer to the linear buffer, (or to disk file), to complete the procedure.

Note: For example code listings, in 'C' and assembler, including FIFO to host data transfers and data transfer to disk, please refer to the programs on the 5.25" floppy diskette accompanying this manual.

5.12 Post-triggering

In a post-triggered data acquisition application, sampled data is not required for a specified length of time AFTER the trigger event occurs. Here, the "length of time " parameter cannot be defined in terms of host processor cycles - especially not in multi-tasking systems. Therefore the post-trigger time delay must be specified in terms of a number of samples since the sample clock period is fixed and known on the DVME-614. The initial setup and configuration is similar to that used for pretriggering and the complete procedure is as follows:

1. Set the analog trigger comparator trigger threshold level by writing to the DAC register, selecting a 2.5V level for the digital trigger input as in Section 5.11.

2. Allocate host storage memory, using malloc( ) function, and set the buffer pointer to the base address.

3. Disable EOS* by configuring Counter #0 for Mode 4 operation and not writing any Counter Register data. Set up Counter #1 in Mode 2 and it specifies the conversion frequency. Counter #2 specifies the internal trigger frequency (refer to Section 5.11).

4. Specify the post-trigger time delay in terms of a number of samples as follows:

   number of samples = (desired time delay/sample clock period)

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5. As in pretriggering, poll bit 2 of the Status Register to detect the trigger event. When the trigger occurs, write the Command Register to enable A/D conversions in internal trigger mode, leaving interrupts disabled for the moment.

6. Start the sample counter. Poll bit 1 of the Status Register to detect EOC* pulses and bump the sample count. (Note: For higher speed applications poll the Half Full Bit (6), having set the time delay to be a of half the FIFO size). When the required number of samples is reached, (as specified in [4] above), reset the FIFO and enable HF interrupts by writing the Command Register. Note that a shadow register should be used for this so that none of the other Command Register bits are altered - except bit 6 set to 1.

7. When a FIFO Half Full interrupt occurs, use an assembly language routine to transfer a data block of half the FIFO size to a host memory buffer or to a diskfile - see Section 5.5 for code/speed optimization.

8. The conversion process may be terminated any time by resetting bit 2 in the Command Register.

5.13 Greater than 64K Samples per Trigger

The number of samples per A/D scan on the DVME-614 is determined by Counter #0 in the 82C54 programmable interval timer. The End Of Scan (EOS*) pulse is generated when the counter counts down from the initial value to 1, assuming the counter is configured for Mode 2 operation. The clock for this counter is the End of Conversion pulse from the A/D converter which means that the counting operation, in effect, counts the number of conversions and therefore the number of samples per scan. However, there is a finite limit to the number that can be specified and this is determined by the number of data bit combinations possible. An 8 bit LSB is written first, followed by an 8 bit MSB - as defined by bits 4 and 5 in the Control Word Register. The combined total of a 16 bit word yields a maximum value possible of 65,536, or FFFF in Hexadecimal.

But what happens if the application requires more samples than this maximum limit? The answer relies on the software control coding, and the fundamental strategy is similar to that developed in the pretriggering and post-triggering discussions in the previous two sections. Basically, EOS* must be disabled so that it doesn't inhibit the internal triggering mechanisms. When the required number of samples have been acquired, the A/D conversion process may be terminated, (reset bit 2 in the Command Register), or simply just stop reading the FIFO.

The following flow chart outlines the general process for collecting greater than 65,536 samples on the DVME-614 board.

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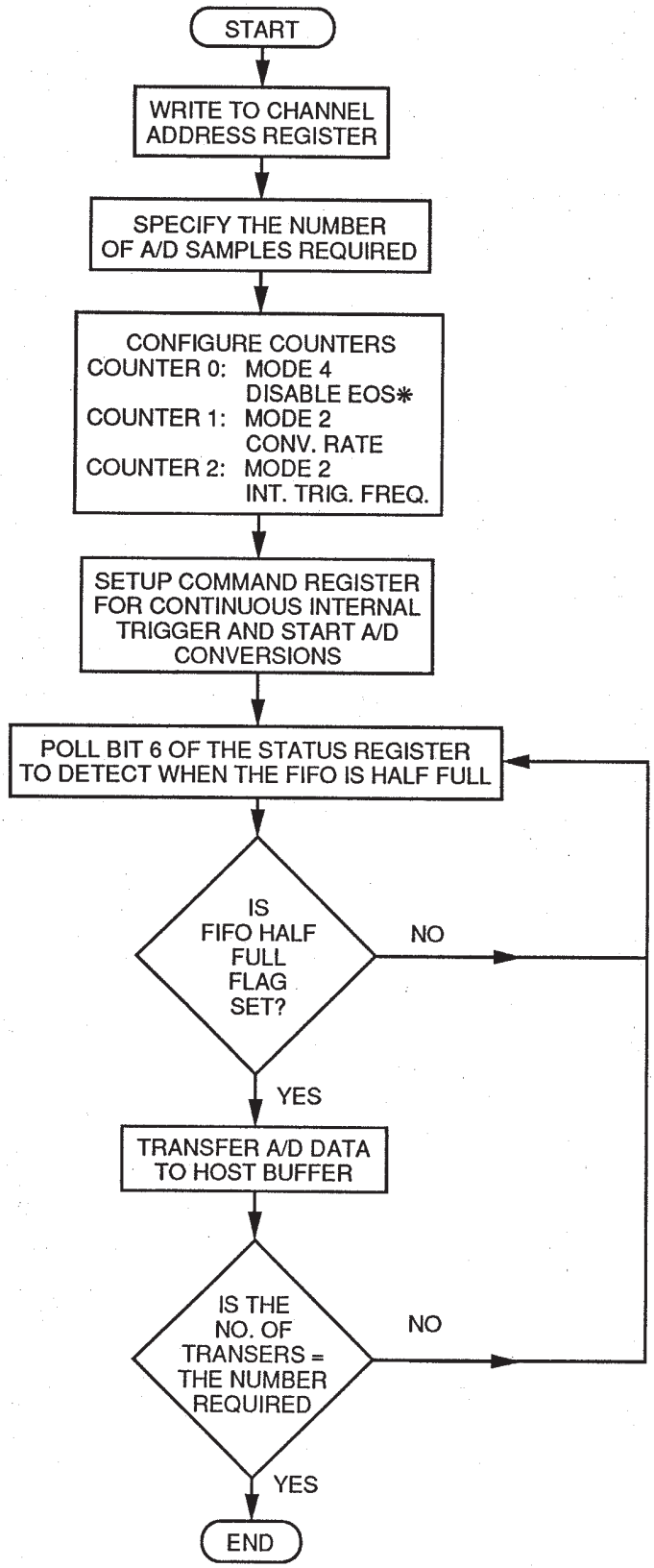


Figure 5.3 Method for Obtaining More Than 65,536 Samples

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5.14 High Speed Multi-Channel Scanning

The DVME-614 is designed for high speed data acquisition applications. Versions 614A, B, and C are quad channel cards, with single channel FIFO throughputs up to 1.5 megasamples per second. However, on sequential channel operation, analog multiplexer sequencing and settling time decrease the data throughput rates - see technical specifications in Section 1.4.

Channel scanning is configured by the Channel Address Register. For DVME-614B, and C cards bits 0 and 1 select the start channel address (0, 1, 2, or 3) and the autoincrement bit is set to 1. The input channel address is automatically sequenced after each A/D conversion is complete. Scanning will continue to cycle through all four input channels until an End of Scan (EOS*) is generated by Counter 0 or until data acquisition is terminated by resetting bit 2 in the Command Register to 0. Each channel scanned adds extra MUX settling time, thus decreasing per-channel throughput. Therefore, if an application requires scanning two of the four input channels the unwanted delay overhead of scanning the two unconnected channels is unacceptable - and unnecessary! Connect one of the two analog input signals to Channel 0 and Channel 2 simultaneously and tie the other input signal to Channel 1 and Channel 3, (as shown in Figure 5.4). When the DVME-614 now scans the four channels it is in effect simulating a dual channel scan - effectively doubling A/D data throughput to the FIFO.

Note: Optimal throughput rates may be also obtained on the DVME-614E, (when scanning 2, 4, or 8 of the 16 input channels), by implementing a similar input configuration.

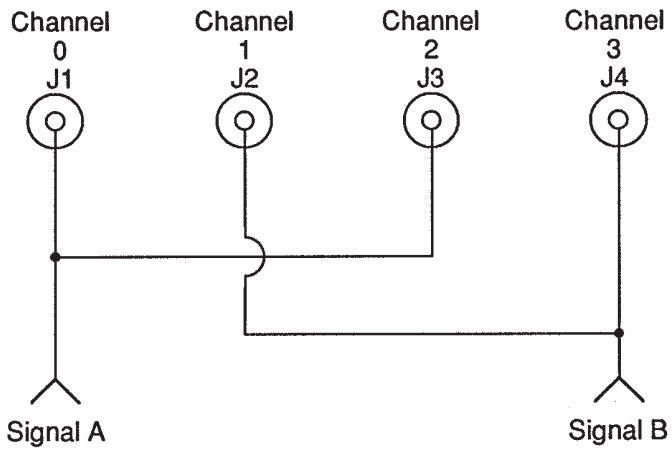


Figure 5.4 High-Speed Scanning

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DVME-614 HARDWARE THEORY

6.0 Introduction

The information presented here is not intended to be a repair and troubleshooting guide. It is included to give you, the user, a better functional understanding of the DVME-614 board. The board is easily damaged by personnel that are not specifically trained in its repair. Damage caused by unauthorized user repair may void the warranty. Except for field recalibration, DATEL strongly recommends that the user return the DVME-614 board to home office for service. Doing this will also provide the user with the latest analysis according to the most recent Engineering release versions.

DATEL attempts to stock a small quantity of boards at the home office but cannot guarantee their availability at short notice. Therefore users with critical downtime applications should stock their own spare boards and retest them periodically.

Board Power

All the power to the DVME-614 board is obtained from the host's +5V supply. On-board DC/DC converter converts this to +15V and -15V to provide for the boards analog circuit supply requirements.

6.1 VMEbus Interface Logic - Schematic 1

VMEbus data lines D15...D0 are buffered by octal bus transceivers U34 and U39 (74ALS645-1). The base address lines A23...A08 are decoded by octal comparators U32 and U38 (74ALS518), which compare these address bits with the DIP switch settings of SW2 and SW3. The remaining low order address bits are latched onto the board by U40 (74ALS274) for individual register access. VMEbus Address Modifier lines, AM0...AM5, are decoded by the 256 X 4 bipolar PROM IC U33 (TBP14S10), which determines the address modifier codes that the board responds to. Also, U33 decodes the VMEbus LWORD* and IACK* signals to prevent board response to longword operations and during and interrupt acknowledge sequence. SYSCLK, the VMEbus 16MHz clock signal is divided by D-type FF U35 (74ALS74-11) to produce an 8 MHz square wave for clocking Shift Register U20 (74LS164). This Shift Register is used in the generation of the VMEbus Data Transfer Acknowledge signal, DTACK*, to provide eight jumperable delays to accomodate slower host processors. The VMEbus AS*, DS0*, DS1* and WRITE* are buffered by U36 (74ALS244) and are decoded by U30 (PAL16L8) to generate several on-board control and timing signals. These include clocking for the Board Select FF, U35 (74ALS74-3), data bus buffer direction controls, BASE address decode comparator enables and a strobe for latching the low order VMEbus address bits A7...A1 onto the board.

6.2 VMEbus Interrupt Logic- Schematic 1

The VMEbus Interrupt section is primarily based on the Interrupt PAL, U25 (PAL20R4), which forms a 4-Bit state machine. This PAL generates the VMEbus interrupts on one of the Interrupt Request lines IRQ*7...IRQ*1, selectable by the DIP switch setting of SW4. In response to an interrupt, the VMEbus Interrupt Handler places a 3-Bit Interrupt Acknowledge level on address lines A1...A3 and generates the daisy chain IACKIN* and IACK signals.

The IACK level is decoded in U25 (PAL20R4). If this level matches the DVME-614 Interrupt Request level, U26 (PAL20L10) places the interrupt vector contained in register U29 (74LS374) on the low order VMEbus data bus lines. The Interrupt Vector register, U29, may be written by the host computer data bus. If the interrupt level on A1...A3 doesn't match the request generated by the DVME-614 then Interrupt PAL U25 (PAL20R4), asserts the daisy chain IACKOUT* signal on to the VMEbus.

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6.3 A/D Control and FIFO's - Schematic 2

Channel address select and control information is written by the host to Address Register U14 (74ALS174). U9 (74LS273) forms the 8-Bit Command Register with U8 (PAL20L8) further decoding the Command information and generating other on-board control and timing signals. These include Interrupt Register FF clock signal (U17-74ALS74), trigger (TRIG) for data acquisition and Simultaneous Sample/Hold Select (SS&HSEL). Status Register U11 (74ALS244) is a read-only, 8-bit register for board status monitoring by the host processor.

FIFO registers U7 and U12 are socketed IC's to provide for various buffer capacities (note that the factory shipping standard sized FIFO is 1KB, with 4KB optional). U5 and U6 (74ALS541) make up the FIFO Data Register and they provide a channel for the host CPU for reading raw A/D data from the board for processing and storage. Outport Data Register, U2 and U3 (74LS373's) , latch the ADC data to the parallel output port - J6, for access by external devices and processors.

Synchronous binary counter U16 (74LS393) divides down the 8 MHz square wave to produce, jumper selectable interval timer clocking speeds of 500 KHz, 250KHz and 125 KHz. Internal triggering is achieved by U23 (82C54), a CMOS programmable interval timer. It accepts on-board control signals -ACQ (Acquire), derived from the TRIG* signal from U8 (PAL20L8) by Setting U17(74ALS74) latch output and CONVEN, (Convert Enable) from the Command Register and End of Conversion (EOC*) from the A/D converter, as well as programming data from the host data lines D7...D0. The timer generates A/D trigger and control signals that determine the number of conversions per scan (EOS*), the internal trigger frequency (INTTRIG*) and the conversion frequency (STCONV). The parallel output port, J6, uses a universal Ready/Acknowledge transfer handshake adaptable to any parallel port and so U22 (74ALS74) and U18 (74ALS112) as well as buffer U10 (74ALS240) and NAND gate U21 (74ALS00) generate and accept these external port handshakes - ACK*, RDY* and EXTXEN. Delay line DLY00A provides five jumperable delays for the End of Conversion signal, (EOC*), to cater for various FIFO register speeds by controlling the FIFO Write, (W*), signal from U8 (PAL20L8).

6.4 A/D and D/A Section - Schematic 3

The DVME-614 data acquisition board provides up to 16 selectable input channels with four optional Simultaneous Sample and Holds. M1 is a monolithic consisting of an input analog multiplexer, an amplifier section, a sample/hold and 12/14-Bit ADC. The Channel Count Register, U13 (74ALS193), a 4-Bit programmable Up/Down binary counter, specifies the current analog input channel. The other A/D control signals, CHWR*, CONVOUT and AUTOINC are generated in Schematic 2. RST* is the buffered, inverted VMEbus RSTDRV system reset signal. A/D data is temporarily stored in the FIFO registers for transferring to the host for processing and storage and the EOC* pulse from the A/D converter indicates when each conversion is complete and valid A/D data is available. Also provided on the DVME-614 (except 614D) is a 12-Bit DAC module U4 (DAC1201). Data may be written to it directly from the host CPU's data bus (LD0..LD11) and the analog output is available, as ANAOUT, on the J5 and J6 connectors. (Available on J2 on the DVME-614E.)

Analog sampling may also be level triggered using the on-board comparator, U1 (LM393). The trigger reference level may be set by the on-board DAC. Note there is no DAC on the DVME-614D.

M2 (PWRMD515) is a DC/DC converter and generates +15V and -15V for powering the analog circuits from the VMEbus +5V supply line.

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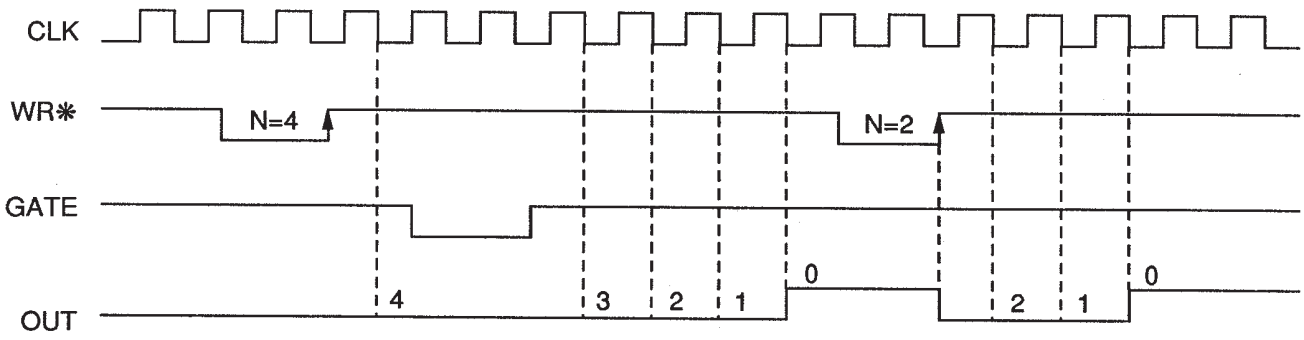
APPENDIX A

82C54 Programmable Timer - Modes of Operation

Mode 0 - Interrupt on Terminal Count

This mode may be used as an event counter. The output is set to "L" level by the Control Word setting, and is kept low until the count reaches 0. At this instant the output is set to "H" level. A "H" level gate pulse validates the count operation, otherwise it is invalidated. However, the gate level does not affect the output.

After writing the initial Control Word and Count data, the count value is written into the Counter Element (CE, actual counter as opposed to the input register) on the next falling edge of the clock signal. The first clock pulse does not cause the value to be decremented and so, if the initial count value is N, the output goes to "H" level after (N+1) clock pulses. If a new count value is written during counting it is loaded into the CE on the next falling clock edge (after writing the second byte), and counting continues from this new value. The output is automatically set to "L" level when the first byte is written - without a clock pulse.



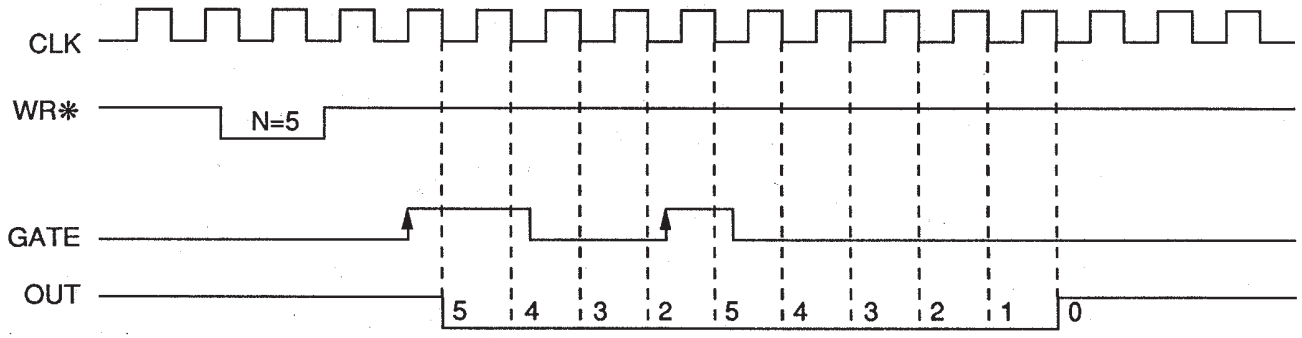
Mode 0 Timing Diagram

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Mode 1 - Programmable One-shot

In this mode of operation the counter is retriggerable using the gate. Control Word writing sets the output to "H" level. It is set to "L" level on the falling edge of the clock after the active high gate trigger, and kept low until the counter reaches 0. The output then goes to "H" level and stays high until the the clock pulse after the next gate trigger signal.

Count value writing does not affect the one-shot pulse being counted until retriggering occurs. At this instant the Counter Register value is reloaded into the Counter Element and counting continues from this new value. If the initial count value is N then the one-shot pulse interval equals N clock pulses. The one-shot is not repetitive.



Mode 1 Timing Diagram

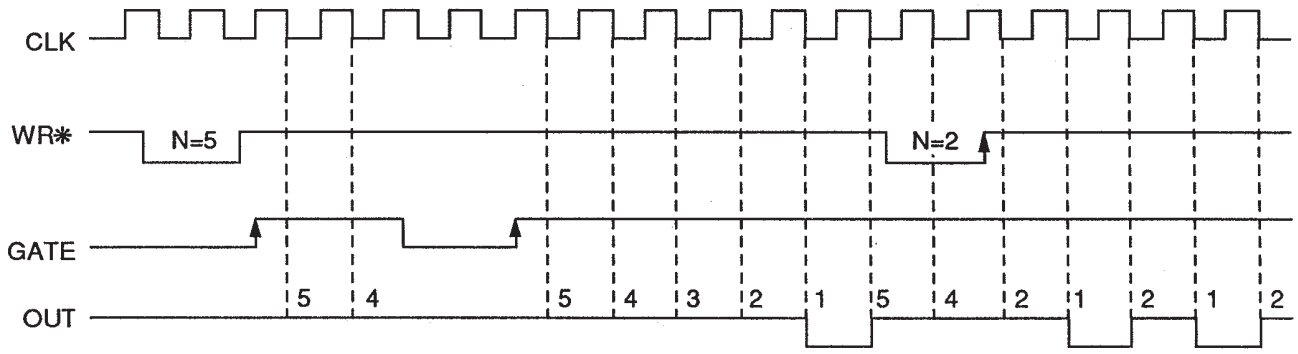
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Mode 2 - Rate Generator

This mode is useful where continuous triggering is required without the existence of trigger strobes. Control Word setting sets the output to "H" level. When the count decrements to 1 the output level goes to "L" level for the duration of one clock pulse and then returns to "H" level again. The initial count value is then reloaded into the Counter Element and the above sequence restarts. If the initial count value is N, then the sequence repeats at intervals of N clock pulses.

The gate signal still acts like a trigger signal. A "H" level validates counting and a "L" level invalidates it. On the falling edge of the gate signal the output is immediately set to "H" level. At the falling edge of the next clock pulse the count value is reloaded and counting starts. The gate input can be used for counter synchronization in this way. If a new count value is loaded into the Count Register during a counting sequence, counting from the new value starts either at the end of the current counting operation or on the falling clock edge succeeding the next gate trigger.

Note: In Mode 2 a count value of 1 is prohibited.



Mode 2 Timing Diagram

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Mode 3 - Square Wave Generator

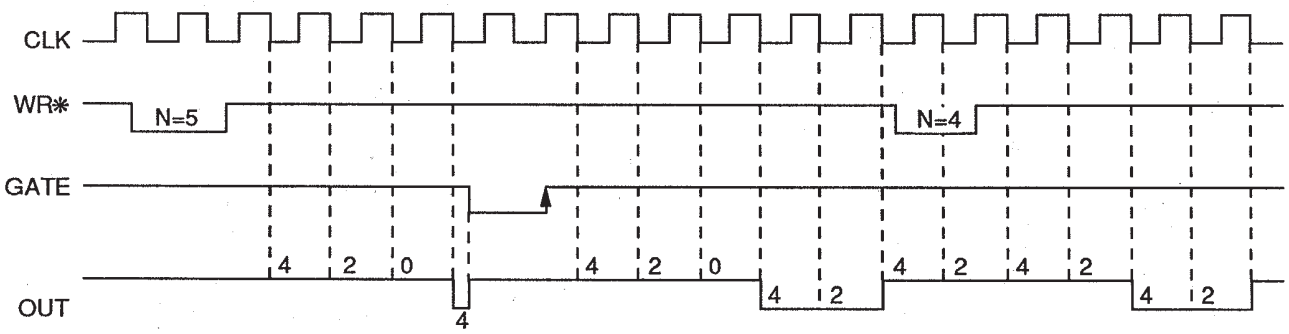
Operation in Mode 3 is similar to that in Mode 2 except that the output duty cycle is different. The output is set "H" by Control Word setting. When the count becomes half the initial value the output goes "L" and remains low for the remainder of the count. Mode 3 repeats the above sequence periodically, generating a square wave with period N (where N is initial count value).

Gate operation is the same as for Mode 2. If a new count value is written to the Counter Register during a count half cycle, counting starts from this new value either at the end of the half cycle or at the falling edge of the next clock after a gate trigger (active low).

Odd and Even number operations are treated differently by the 82C54.

For an even number, initially the output is high after CE loading. The counter decrements by 2 on every clock pulse until it reaches a value of 2. Then the output goes low for one clock pulse, the count initial value is reloaded and counting restarts.

For odd number Control Word Register programming, the initial value minus 1 is loaded into the CE. The counter decrements by 2 until it reaches a value of 0, the output goes low for one clock pulse, the initial count value is reloaded and counting restarts.



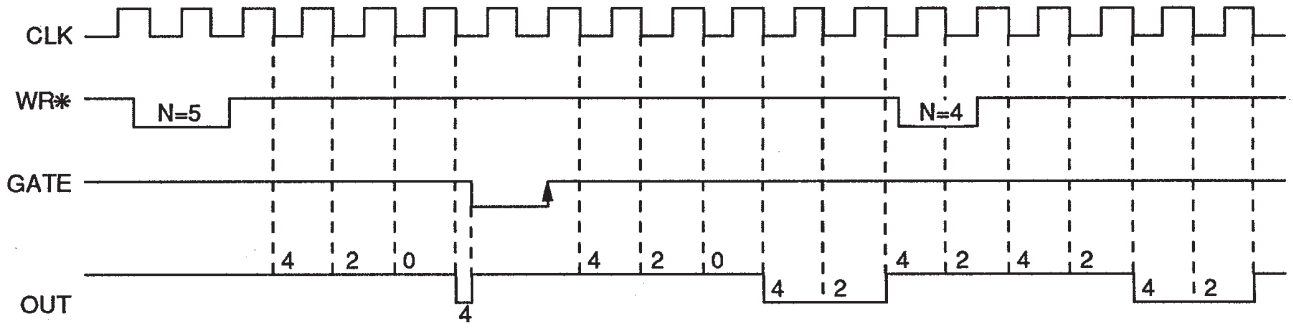
Mode 3 Timing Diagram

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Mode 4 - Software Triggered Strobe

Mode 4 is ideal for software triggering applications. After initial CE loading the output is "H" level. When the counter value becomes 0 the output goes "L" level for one clock pulse and then returns high. The count sequence restarts when the initial count value is written by the host.

The gate signal does not affect the output and a gate "H" level validates counting. When the Control Word and initial count value are written, the Counter Element is loaded on the falling edge of the next clock pulse. The clock pulse does not decrement the count value and so if the initial count is N, the output strobe is not generated until N+1 clocks are applied after writing by the host. If the new count value is written during counting, the Counter Element is written on the next falling clock edge and counting starts from the new value. This evidently means that the counting operation is retriggered by software.

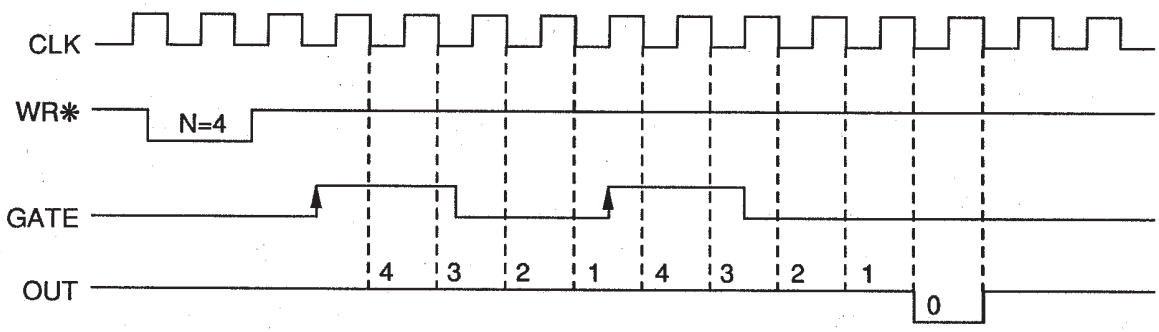


Mode 4 Timing Diagram

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Mode 5 - Hardware Retrigger

Operation in this mode is based on triggering by the rising edge of a gate pulse. The output is initially set to "H" level. When the counter value reaches 0, the output goes "L" level for one clock pulse and then restores to "H" level. Even after Control Word and initial counter value data is written, loading to the Counter Element does not occur until the input of the clock pulse succeeding the trigger. This first CE loading clock pulse does not decrement the count value. Therefore if the initial count value is N, the output is not set to "L" until N+1 clock pulses after triggering. If the gate trigger is asserted after a new count value is written, before current counting completes, the new count value is loaded to the CE at the falling edge of the next clock pulse, and counting continues using this new count value.



Mode 5 Timing Diagram

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APPENDIX B

DVME-614 Circuit Schematics	D17743 rev. A 3 pages
DVME-614 Hardware Assembly Drawings	D17742 rev. B 1 page
DVME-614 Data Sheet	

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DATEL®

DATE ISSUED: October, 1992

ADDENDUM

TO THE

DVME-614 User's Manual

DOCUMENT NUMBER: UM-DVME-614

This addendum provides updated information for the document listed above.

Place this addendum at the front of your document to ensure that you have the most current information about this product.

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Section 1.3, page 1-2

The DVME-614F offers 2 simultaneous sample/hold channels, 12-bit at up to 2MHz per channel. SS&H mode is selected simply by writing '2' to the Channel Address Register.

Section 1.4, page 1-3

Replace complete set of functional specifications with following updated list:

1.4 Functional Specifications
(Typical at +25 °C, dynamic conditions, gain = 1, unless noted)

Analog Inputs

Number of Channels

4 channels (models DVME-614A,B,C)
1 channel (model DVME-614D)
16S/8D channels (DVME-614E)
2 channels (DVME-614F)

Input Configuration

Single-ended, non-isolated (models DVME-614A,B,C,F). Single-ended or differential non-isolated (models DVME-614D,E).

Full Scale Input Ranges (user-selectable)

	0 to +10V ±10V	±5V	±1V
DVME-614A	yes	no	2 chans. gain = 10
DVME-614B	yes	yes	no
DVME-614C	yes	yes	no
DVME-614D	no	yes	no
DVME-614E	yes	yes	Note 1
DVME-614F	0 to +10V	yes	no

Programmable Gain

See Note 1.

Input Impedance (Note 2)

10 Megohms, min. power on. (DVME-614A,B,C,E)
1.5 kilohms power off.
2 kilohms, DVME-614D
1 kilohm, DVME-614F

Input Bias Current

± 1 nA

Input Capacitance

10 pF per channel

Input Overvoltage

± 15V (no damage)

Overvoltage Recovery Time

2 microseconds max.

Addressing Modes

1. Single channel
2. Simultaneous Sample/Hold (DVME-614A only)
3. Sequential with autosequenced addressing
4. Random addressing by host software
5. Dual-channel simultaneous (DVME-614F)

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Sample/Hold

Acquisition Time (FSR step) to 0.01% of FSR	900 ns max. (DVME-614A) 750 ns max. (DVME-614B,E) 200 ns max. (DVME-614C) 50 ns max. (DVME-614D) 165 ns max. (DVME-614F)
Aperture Delay	15 ns (DVME-614A) ±20 ns (DVME-614B) 20 ns (DVME-614C,E,F) 10 ns (DVME-614D)
Aperture Delay Uncertainty	±8 ps (DVME-614A) ±100 ps (DVME-614B) ±40 ps (DVME-614C,E,F) ±7 ps (DVME-614D)
Droop Rate	1.5 µV/µs (DVME-614A) 1 µV/µs (DVME-614B,C,D,E,F)
SSH Channel-to-channel Linearity Tracking (DVME-614A only)	± 0.03%

A/D Converter

Resolution	12 bits (DVME-614A,C,D,E,F) 14 bits (DVME-614B)
Conversion Period	500 nanoseconds (DVME-614A) 1.6 microseconds (DVME-614B) 500 nanoseconds (DVME-614C,E) 200 nanoseconds (DVME-614D) 400 nanoseconds (DVME-614F)
Output Coding	Positive-true right-justified straight binary (unipolar) or right-justified two's complement (bipolar) with sign extension through bit 15.
Start Clock Sources (Jumper selectable)	1. Local Pacer sample clock 2. External TTL sample clock

Total System DC Characteristics

Gain = 1 (Note 3)

Integral Non-linearity at +25 °C	±1 LSB of FSR (DVME-614A,C,E,F) ±1.5 LSB of FSR (DVME-614B,D)
Differential Non-linearity at +25 °C	± 0.75 LSB of FSR max. (DVME-614A,C,E) ± 1 LSB of FSR (DVME-614B,D,F)
Full Scale Temperature Coefficient	±0.1 LSB per °C max. (DVME-614A,C,E,F) ±0.3 LSB per °C max. (DVME-614B,D)

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Zero or Offset Temperature Coefficient	±0.1 LSB per °C max. (DVME-614A,C,E,F) ±0.3 LSB per °C max. (DVME-614B,D)
Power Supply Rejection	±0.004% per % of bus +5V
Total System Dynamic Performance	
System Bandwidth (single channel, FS input)	1 MHz (DVME-614A) 1 MHz (DVME-614C) 200 kHz (DVME-614B,E) 2.5 MHz (DVME-614D) 1 MHz (DVME-614F)
Total Throughput to FIFO (single channel, gain = 1)	700 nanoseconds (DVME-614A) 2 microseconds (DVME-614B,E) 625 nanoseconds (DVME-614C) 200 nanoseconds (DVME-614D) 500 nanoseconds (DVME-614F)
Throughput to FIFO per A/D sample (multi-channel, gain = 1) [Note 4]	1 microsecond (DVME-614A) 3 microseconds (DVME-614B) 2 microseconds (DVME-614C) 4 microseconds (DVME-614E) 500 nanoseconds (DVME-614F)
Total Harmonic Distortion FS input (Note 5)	-72 dB (DVME-614A,C) -75 dB (DVME-614B) -65 dB (DVME-614D) -70 dB (DVME-614F)
A/D Memory	
Architecture	First-In, First-Out (FIFO)
Memory Capacity	1024 samples DVME-614_1 4096 samples DVME-614_2 16384 samples DVME-614_3 2k samples, 8k samples and 32k samples FIFO's also compatible.
VMEbus Interface	
Standards Compliance	IEEE P1014/D1.0
Architecture	A24:D16 slave consisting of 16 contiguous word registers.
Data Bus Width	16 bits using P1 connector.
Address Bus	23 address lines(A23-A01) plus 6 Address Modifier (AM) lines.

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Address Modifier Codes	39 or 3D hex, selectable.
Address Mapping	Decodes address lines A23-A08
VMEbus Interrupt	1 line, selectable IRQ*1-7. Asserts maskable, programmable 8-bit vector ID code.
Interrupt Source	Scan Acquire Flag (sample count reached), FIFO Full or Half Full flags.
Data Transfer	Uses 16 MHz VMEbus SYSCLK to generate DTACK*, with selectable delays. Data transfer rates vary.
Trigger Control	
Timer/Counter	82C54 programmable interval timer,
Counter Functions	a. End Of Scan, sample count reached b. A/D start rate (16 bit divisor) c. Scan or frame rate(16 bit divisor)
Pacer Sample Counter	3 to 65,536 samples. Drives ACQ flag/interrupt. (Greater 65k non-stop samples are programmable)
Clock Sources (User Selectable)	Internal 8 MHz crystal or external TTL A/D start rate clock. Choice of 500, 250 or 125 kHz internal trigger clocks.
Analog Trigger Input Range (See Tech. Note 6)	±10 Volts. Note that there is no provision on the DVME-614D for an analog trigger.
Analog Output (See Tech. Note 7)	
Number of Channels	1
Functions (user selectable)	General purpose analog output. Set threshold for external analog trigger.
Resolution	12 Bits
Output Voltage Range	0-10V, ±5V, ±10V at ±5 milliamps max.
Linearity	±0.05% of FSR
Settling Time	5 microseconds to 0.05% (10V step)
Input Coding	Straight binary, right justified
Connectors	
VMEbus Connector, P1	96-pin, male DIN connector. P2 connector is not used.
Local Analog Input	Four BNC bayonet coaxial, mounted on the front panel (614A,B,C,D,F), 614E uses a 25-pin, DB-25S female which also contains the analog output and trigger input lines.

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Multipurpose Connector (614A,B,C,D, and F)	BNC, user-selectable as TT; trigger input, analog comparator threshold input or D/A channel output. This is available through the DB-25S on 614E.
Parallel Port	
Parallel Port Connector	Front panel, 25-pin DB-25S female.
Outport Type	16 data lines, TTL levels from FIFO. Includes Ready out, Acknowledge In and Transfer enable handshakes and it does not provide addressing. Output steering is software enabled.
Function	Asynchronous slave to remote master. Can be hardwired as synchronous master. Data transfer from FIFO to external device or peripheral and provides for external clocking. It is not a DVME-614 low-level programming interface. It also contains the analog output channel.
Port Loading	TTL compatible (24mA out,1.6mA in)
Port Data Rate	4 MHz max. to external processor in asynchronous mode. Can hardwire for external clocking to provide higher synchronous rates.
Miscellaneous	
Power Required	+5V dc ±5% at 3.0 Amps max. from VME bus.
Operating Temperature Range	0 to +60 °C
Storage Temperature Range	-25 to +80 °C
Relative Humidity	10% to 90%, non-condensing. Forced cooling is recommended.
Altitude	0 to 10,000 feet.
Outline Dimensions	Double height VME, 6U outline. 9.19"W x 6.3"D x 0.6"H (233.5 x 160 x 15.24 mm)
Analog section modularity	The MUX-S/H-A/D module is socketed for function interchange.
Analog adjustments	Offset and gain per channel for SSH on DVME-614A. A single offset and gain trimmer is provided on all of 614B,C,D and E. Recommended recalibration period is 90 days in stable operating conditions.

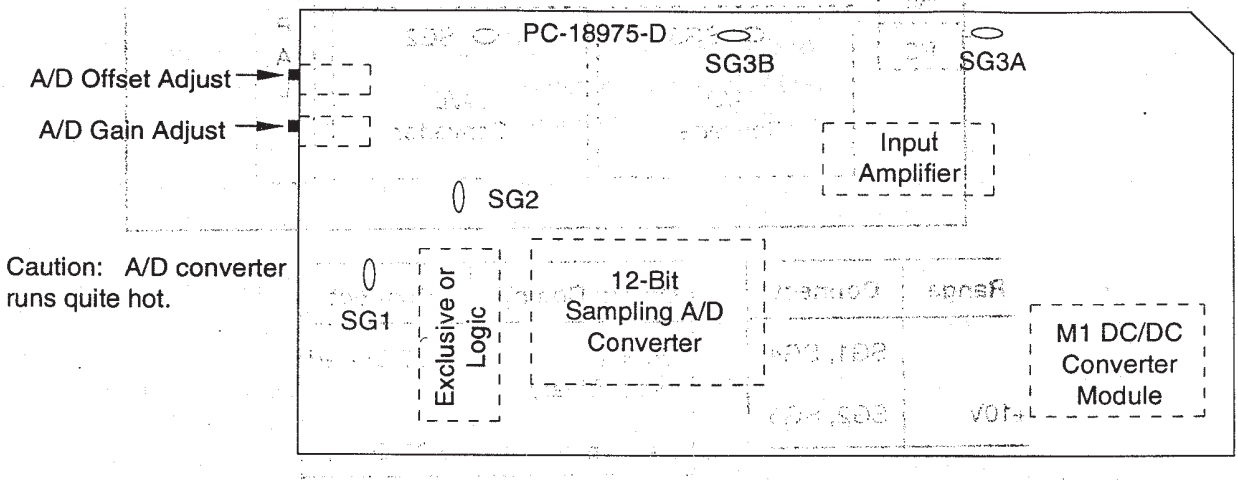
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Section 2.10, page 2-8

A minor jumper modification has occurred with the DVME-614C A/D module in Figure 2.8c (M1 revision B and later):

For ease of connection jumper Y1 has been divided in 2, jumpers A and B. This allows jumper plugs to interconnect Y1(A)-Y2 and Y1(B)-Y3 without wire wrapping.

The DVME-614D A/D module has been re-designed as follows (Revision C):



A/D Binary Coding	Solder Gap
2's Complement	Open SG1 & SG2 (std.)
Offset Binary	Close SG1 & SG2

The input voltage range is fixed at ±5V.

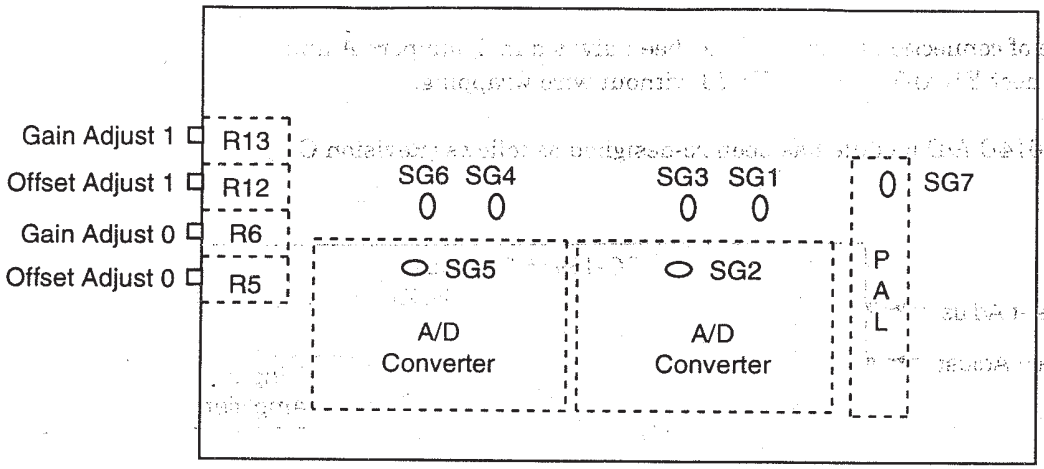
Leave SG3 closed

Figure 2.8d M1 Analog Module for the DVME-614D (solder side)

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Section 2.10, page 2-9

Add the following diagram:



Input Range	Connect
±5V	SG1, SG4
0 to +10V	SG2, SG5

Output Coding	Connect
Unipolar or Offset Binary	SG7 Closed
2's Complement	SG7 Open

Note: Leave SG3 and SG6 closed.

Figure 2.8g M1 Module (Revision B) for DVME-614F (solder side)

Section 2.15, page 2-12

On the DVME-614D and DVME-614F unused 'J' inputs are not connected on the A/D module.

Section 2.16, page 2-13

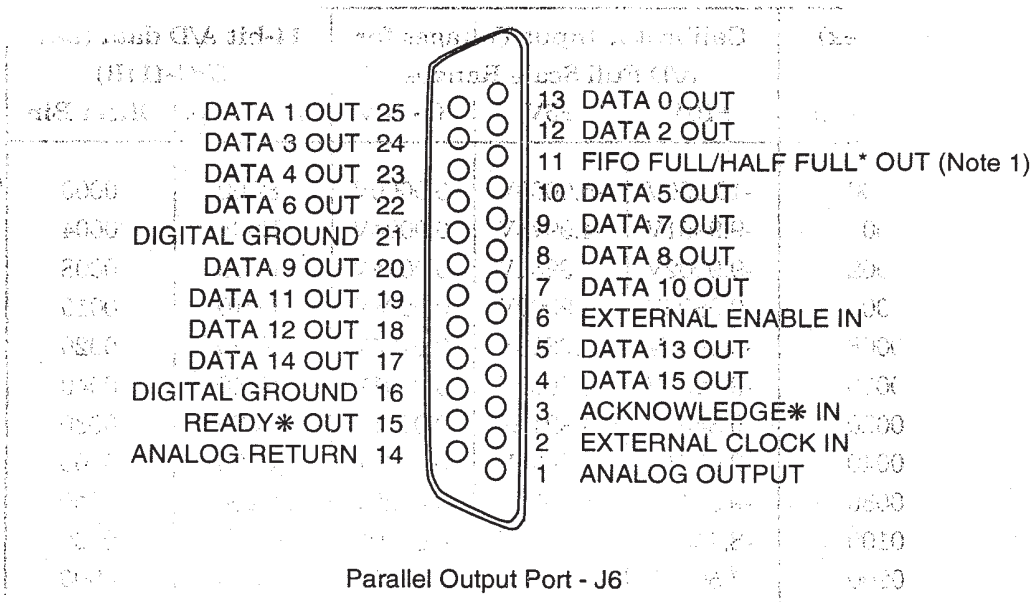
Replace existing Section 2.16 with the following:

The DVME-614D A/D module has been redesigned (revision C). The input impedance of the DVME-614D is 2 kilohms. An external termination resistor can be installed (on the input connector) if necessary. The A/D can now be triggered at 5 MHz - must use external 82C54 clock source to achieve this, maximum 10 MHz.

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Section 2.15, page 2-12

Replace the Parallel Output Port - J6 in Figure 2.11a with the following:



Parallel Output Port - J6

Note 1: For board assembly revision D or later, jumper pads E43-E44 to connect FIFO Full* to J6, pin 11. Jumper E44-E45 for FIFO Half Full* on J6-11. These pads are located between the U7 and U12 FIFO's.

Caution: 1 TTL load maximum. J6-11 is supplied with no connection.

Section 2.17, page 2-16

Add the following to Figure 2.13

Model	Designation
614F	R5 - Offset for channel 0 R6 - Gain for channel 0 R12 - Offset for channel 1 R13 - Gain for channel 1

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Section 2.17, page 2-17

Replace Table 2.3 with the following:

12-bit A/D data (hex) (PC-414A,C,D,E)		Calibrator Input Voltages for A/D Full Scale Ranges			14-bit A/D data (hex) (PC-414B)		
2's Comp.	Offset Bin.	±10V	±5V	0 - 10V	2's Comp.	Offset Bin.	
F800	0000	-10.000V	-5.0000V	0.0000V	E000	0000	OFFSET Adj.
F801	0001	-9.9951V	-4.9975V	0.0024V	E004	0004	
F802	0002	-9.9902V	-4.9951V	0.0048V	E008	0008	
F804	0004	-9.9805V	-4.9902V	0.0098V	E010	0010	
F808	0008	-9.9609V	-4.9805V	0.0195V	E020	0020	
F810	0010	-9.9219V	-4.9609V	0.0391V	E040	0040	
F820	0020	-9.8438V	-4.9219V	0.0781V	E080	0080	
F840	0040	-9.6875V	-4.8438V	0.1563V	E100	0100	
F880	0080	-9.3750V	-4.6875V	0.3125V	E200	0200	
F900	0100	-8.7500V	-4.3750V	0.6250V	E400	0400	
FA00	0200	-7.5000V	-3.7500V	1.2500V	E800	0800	
FC00	0400	-5.0000V	-2.5000V	2.5000V	F000	1000	
0000	0800	0.0000V	0.0000V	5.0000V	0000	2000	
0400	0C00	5.0000V	2.5000V	7.5000V	1000	3000	
0600	0E00	7.5000V	3.7500V	8.7500V	1800	3800	
0700	0F00	8.7500V	4.3750V	9.3750V	1C00	3C00	
0780	0F80	9.3750V	4.6875V	9.6875V	1E00	3E00	
07C0	0FC0	9.6875V	4.8438V	9.8438	1F00	3F00	
07E0	0FE0	9.8438V	4.9219V	9.9219V	1F80	3F80	
07F0	0FF0	9.9219V	4.9609V	9.9609V	1FC0	3FC0	
07F8	0FF8	9.9609V	4.9805V	9.9805V	1FE0	3FE0	
07FC	0FFC	9.9805V	4.9902V	9.9902V	1FF0	3FF0	
07FE	0FFE	9.9902V	4.9951V	9.9951V	1FF8	3FF8	
07FF	0FFF	9.9951V	4.9976V	9.9976V	1FFC	3FFC	GAIN Adj.
Not applicable		9.9976V	4.9988V	9.9997V	1FFE	3FFE	GAIN Adj. (614B)

A/D Calibration Table

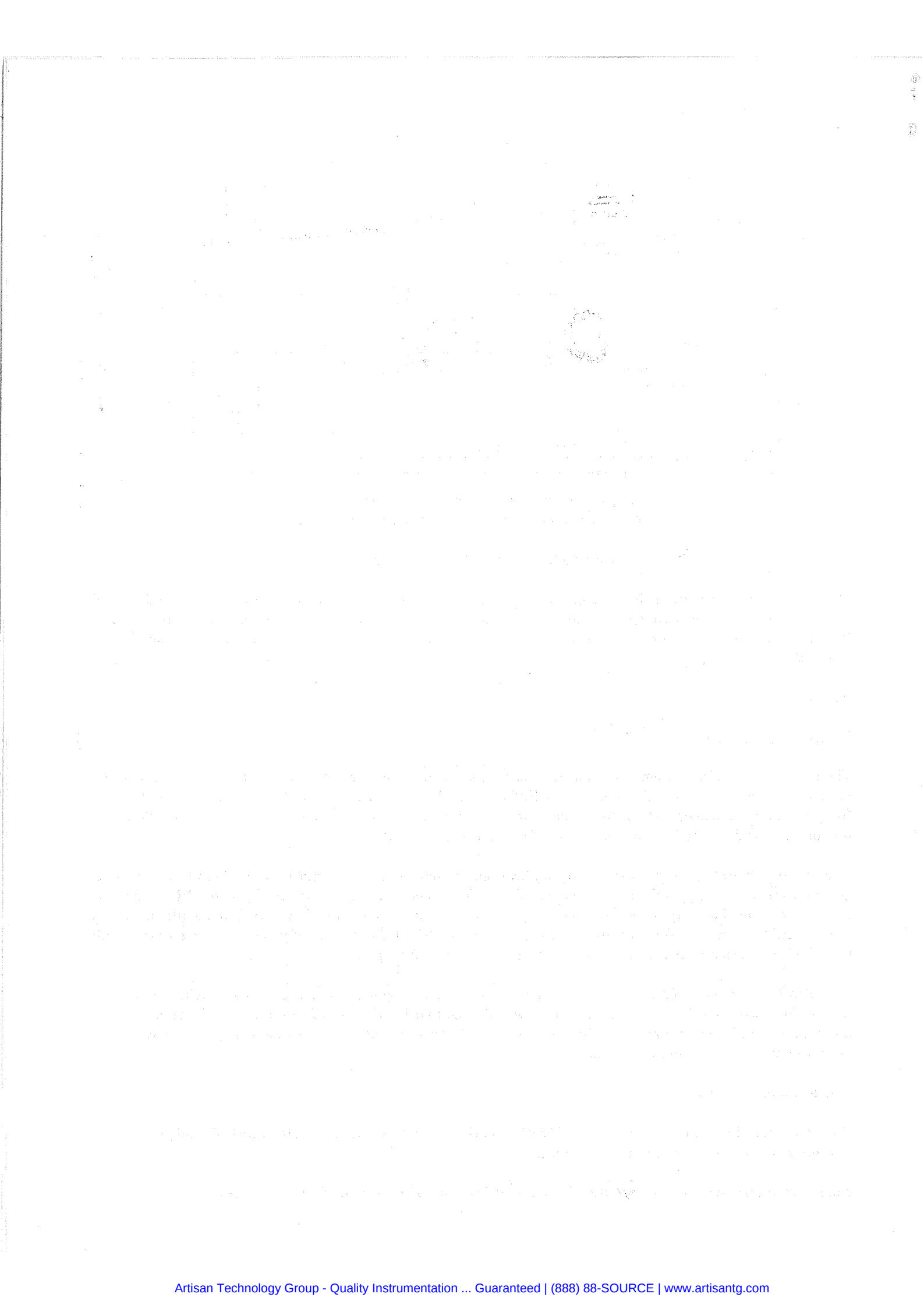
Section 3.3, page 3-3

Add the following to the end of the section.

Interrupt Source

Note that the FIFO Full Flag* (FF) is not latched. It resets as soon as the FIFO is read or is reset. For Command bits 5, 6, and 7 we recommend enabling only one interrupt at a time to positively identify the source of the interrupt. If you enable *both* the HF and FF interrupts, test FF in status bit 7 *immediately* after receiving the HF interrupt.

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ADDENDUM

TO THE

DVME-614 User's Manual

DOCUMENT NUMBER: UM-DVME-614

This addendum provides updated information for the document listed above.

Please replace page 3-3/3-4 with the attached sheet.

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Trigger Source [Bits 1,0]	00 = Scan by a write to the channel address register (normally not used). 01 = Scan by internal trigger. 10 = Scan by external TTL trigger. 11 = Scan by external analog threshold trigger.
Convert Enable [Bit 2]	0 = Disable A/D conversion (default) 1 = Enable A/D conversion
Trigger Polarity [Bit 3]	0 = Trigger when external digital trigger is high. Trigger when external analog trigger is lower than the threshold. 1 = Trigger when external digital trigger is low. Trigger when external analog trigger is higher than the threshold. Note: DVME-614 is *level* triggered not edge triggered.
Select FIFO Output Data Steering [Bit 4]	0 = Select VMEbus data register (Inhibit parallel port) 1 = Enable FIFO transfers to parallel port (Inhibit VMEbus data access)
Interrupt Source [Bits 7,6,5] These bits are OR'd.	Bit 5 = 1: Enable interrupt on Acquisition done flag. Bit 6 = 1: Enable interrupt on FIFO half full flag. Note that HF occurs when half the FIFO size plus 1 samples are converted. Bit 7 = 1: Enable interrupt on FIFO full flag. Bit 5,6,7 = 0: Disable interrupts (default)

3.4 Status Register (Read BASE + 0)

The Status Register resides at the same address location in the host processor's memory map as the Command Register but it exhibits a different bit representation. It is a byte-wide, read-only register that enables host monitoring of the DVME-614 data acquisition process.

15-8	7	6	5	4	3	2	1	0
x-x	FIFO Status			Ovr Smp Err	Xfr in Pro	Ana Trg Lvl	EOC Sts	ACQ Sts
	FF	HF	EF					

Figure 3.2 Status Register Bit Field

Acquisition Status [Bit 0]	0 = A/D scan not in progress or scan done (Counter 0 sample count was reached). 1 = A/D scan in progress (Counter 0 sample count not reached). **Important**: The ACQ flag is *not* valid until the FIFO EF (bit 5) goes high. Host software must poll bit 5 for a low to high transition before polling ACQ status.
End of A/D Conversion Status (EOC) [Bit 1]	0 = A/D conversion in progress, data invalid 1 = A/D conversion done, data valid
Analog Trigger Comparator Output [Bit 2]	0 = Analog trigger input is below reference 1 = Analog trigger input is above reference

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Transfer in Progress [Bit 3]	0 = Remote device not ready for transfer 1 = Remote device is ready for transfer

Bit 3 displays parallel port pin 6 (external Transfer Enable In) AND'ed with Command bit 4.

Oversample Error [Bit 4]	0 = No error 1 = A/D triggered before EOC is done.

Bit 4 is cleared by disabling A/D conversions (Command Register bit 2)

FIFO Status Flags [Bits 7,6,5]	Bit 5: 0=FIFO is empty, 1= FIFO not empty Bit 6: 0=FIFO is half full, 1=less than half full Bit 7: 0=FIFO is full, 1=FIFO is not full

Note the negative true coding on these bits.

3.5 Channel Address Register (Write BASE + 2)

This 8-Bit, write-only register specifies the required analog input channel as well as the number of conversions per scan. The register is organized as follows:

15-8	7	6	5 4	3 2 1 0
x-x	Auto Incr	SSH Ctrl	Not Used	Channel Addr 3 2 1 0

Figure 3.3 Channel Address Register Bit Field

Channel Address Bits [3-0]	This 4-Bit address field provides for 16 different channel specifications. Therefore only bits 1 and 0 need to be used for the 4-channel analog modules (A,B,C) on this board. All 4 bits are used for DVME-614E. Only channel 0 available on 614D.

Simultaneous Sample/Hold Control [Bit 6]	0 = Sequential or single channel mode 1 = Simultaneous Sample/Hold mode (see Section 1.3)

In SSH mode, counter 0 must be programmed with the number of SSH channels (max = 4). One trigger is required per A/D scan.

Channel Address Autoincrement [Bit 7]	0 = Single channel (no increment) 1 = Sequence channel address at A/D conversion. Must be set to 1 for simultaneous sampling on DVME-614A models.

Note: Input analog channel settling time is a major factor as regards speed, when programming the DVME-614. In sequential channel mode (bit 7 = 1), or if the channel address bits are being rewritten after each sample, then the time for a static analog signal to be present at the A/D converter input is longer than in single channel scan mode (bit 7 = 0 and no address bit alterations). This obviously decreases the sample rates on each individual channel. For typical single channel and sequential channel settling times, refer to the Functional Specifications in Section 1.4

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