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DVME-622

8/16-Channel, Fast Simultaneous VME bus Analog Output Board

FEATURES

- **8 or 16 analog outputs**
- **12-bit D/A resolution**
- **3 microsecond settling time**
- **Simultaneous update**
- **Trigger timer Interrupt**
- **Digital I/O (4-in, 3-out)**
- **Output ranges selectable per channel**



Many applications require phase-synchronous analog outputs. Examples include precision system simulation and coherent field generation in process control, audio, acoustics and sonar. The DVME-622 is a high density analog output board with up to 16 signal channels. Each Digital to Analog Converter (DAC) channel may be individually selected for full scale output ranges of 0 to +5V, 0 to +10V, ±5V, ±10V, or ±2.5V. All outputs are buffered and will deliver ±0.025% accuracy from 0 to 5 milliamps output load. The DVME-622 is installed in a host VMEbus computer.

To achieve the simultaneous update capability, each channel input register is double buffered. The registers are successively loaded by the host computer then all channels are updated by host command or trigger. If preferred, each channel may also be operated in the non-concurrent transparent mode under program control with random addressing or single channel operation.

For applications requiring a precision clock to sequence the output waveforms, the DVME-622 includes a software-programmable trigger. The trigger strobes the simultaneous update and posts a status bit or interrupt to the host computer. Upon detecting the trigger, the host may block-load the next data frame. The trigger may be derived from an internal crystal-stabilized timer or from an external timebase. The external trigger and external clock options make the DVME-622 fully synchronous with external events. The timing section also includes a spare counter, usable for any purpose.

For repeating frame scan applications, the DVME-622 includes an autoincrement mode. In this mode, memory block transfer instructions will automatically load up to 16 channels at very high speed from a buffer in the host. The DVME-622 will digitally steer each analog data word to successive DAC input registers while using the same memory data register address. The user's program simply maintains a CPU register as a downcounter to terminate each block transfer. Typically, the trigger and autoincrement modes are used together where the host loads the next block after detecting the trigger status signal from the last simultaneous update.

The combination of a precision frame clock trigger, autoincrement channel addressing and high speed simultaneous block loading make the DVME-622 ideal for artificial waveform applications. Such waveform generators continuously loop through a large RAM buffer containing a synthetic composite digitized analog signal.

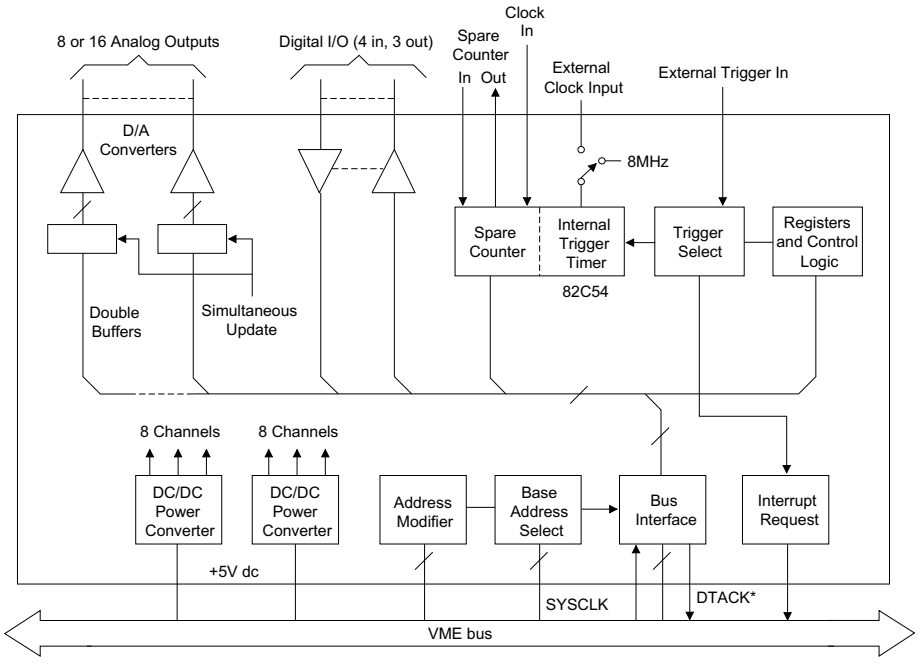


Figure 1. DVME-622 Block Diagram

Fast settling rates are another feature of the DVME-622. Full scale step response of each DAC channel is 3 microseconds. Block transfers of input data may occur faster than individual DAC channel analog settling times. Each DAC channel inut register can be updated at over 1 Megasample per second.

The DVME-622 is configured on a 6U VME compatible board. Analog signal connections are made using a front panel 25-pin "D" connector. Seven channels (4 inputs and 3 outputs) of discrete I/O are provided for general purpose control and monitoring of external logic devices. A second 25-pin "D" connector provides digital I/Os, spare counter and external clock access. The DVME-622 includes tow high efficiency DC to DC power converters to supply local analog circuits. The entire board uses only +5 Volt DC power from the VME bus. The board is compatible with all popular computer languages although the highest speed will require assembly language. A comprehensive user's manual is included with the board as well as a MS-DOS diskette containing example source programs.

SPECIFICATIONS

(typical at 25°C, unless otherwise noted)

ANALOG OUTPUTS	
Number of Channels	8 or 16
Output Configuration	Single-ended, non-isolated
Full Scale Output Ranges	0 to +5V, 0 to +10V, ±5V, ±10V, and ±2.5V, individually selectable per channel.
Output Current	±5mA min. (source or sink), short-circuit protected to ground.
Resolution	12 binary bits
Input Data Coding	Straight or offset binary, positive true coding. Data is right justified.
Output Impedance	50 milliohms
Channel Addressing Modes	Random, simultaneous or auto-increment sequential
PERFORMANCE	
Monotonicity	No missing codes
Linearity Error (after calibration)	±0.025% of FSR.
Temperature Coefficient of Gain	±5ppm typ., ±30ppm max. of FSR/°C max.
Temperature Coefficient of Zero or Offset	±20ppm of FSR/°C max.
Settling Time (FS step)	3µs max. to ±0.025% of final value. (0-5V, 0-10V, ±5V, and ±2.5V ranges). 4µs max. for ±10V range.
Settling Time (1 LSB step)	1µs to ±0.01%
Slew Rate	10V/µs min.
DIGITAL INPUT/OUTPUT	
Number of Lines	4 inputs, 3 outputs, non-isolated
Logic Levels	Compatible with TTL, TTL-LS, ALS, etc. Inputs: "0" (0.8V, "1") 2.0V Outputs: "0" (0.4V, "1") 2.4V
I/O Loading	Inputs: 1 LS load plus 10kΩ pullup to +5V. Outputs: 24mA source or sink

COUNTER/TIMER	
Function	Used as an update strobe for each multichannel DAC frame
Frequency Range	2MHz to 536.87 Sec (32-stage binary or BCD divider). Use external clock to increase range.
Frequency Stability	±50ppm/°C.
Spare Counter	16-stage binary divider usable for any purpose. Will divide input signals from 2 to 65,535. Includes counter input, output, and clock, 1 TTL-LS load, 10MHz max. clock input.
VME BUS INTERFACE	
Standards Compliance	IEEE P1014/D1.0
Architecture	Memory mapped in 8 contiguous word locations on 256-byte boundaries. A24:D16 slave.
Memory Mapping	Decodes memory address lines A23 through A08 plus six address modifiers, AM5-AM0
Address Modifier Codes	39h or 3Dh, selectable
Data Bus	16-bit transfer using VME bus SYSCLK signal to generate DTACK* with selectable delay. (Note: SYSCLK is required)
Trigger Interrupt	1 interrupt, selectable on IRQ 1-7 plus maskable programmable 8-bit vector ID.
MISCELLANEOUS	
Analog Section Adjustments	Full scale gain and zero or offset potentiometers are provided for (every 90 days) each DAC channel. See note 2.
Analog Connector [P3]	25-pin DB-25S female, incl. the external trigger input.
Digital I/O Connector [P4]	25-pin DB-25S female, incl. the connections to spare counter and external clock inputs.
Operating Temp Range	0 to +60°C
Storage Temp Range	-25 to +85°C
Relative Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 ft (0-3048 m). Forced cooling recommended.
Power Supply	+5V dc, ±5% supplied from VME bus
Requirements	2.5 Amps typ., 4.0 Amps max. (16 channels), 1.5 Amps typ., 2.5 Amps max. (8 channels.
Outline Dimensions	Double height 6U VME outline.
Weight	1.5 pounds (0.7kg)

Notes

1. Depending on the VME host, data transfers may occur at over 1 Megasample per second and will accept a host DMA controller for highest speed. When estimating your system timing, account for any interrupt (the real time clock for instance) and DRAM refresh delays. To obtain maximum VMEbus throughput, disable all host system interrupts if possible.

2. All DAC input registers reset to zero or to half scale (0800 hex) on power-up or reset depending on the unipolar/bipolar switch selection. In either case, the output voltage level is set to 0 V.

I/O REGISTER MAPPING

The memory base address may be selected anywhere using 24-bit addressing up to FFFF00h on 256-byte boundaries. At power-up or VME bus reset, all control registers contain zeroes. The DAC data register should be programmed after setting up the channel address and command mode. The 82C54 registers must be programmed in a specific sequence - discussed in the User Manual. 16-bit memory reference word instructions must be used. Do not use read-modify-write or test-and-set instructions at locations with separate co-located read and write registers. Unlisted registers are not used.

Address (hex)	Direction	Description
BASE + 0	Write	Command and Vector Register
BASE + 0	Read	Status Register
BASE + 2	Write	DAC Channel Address Register
BASE + 2	Read	Interrupt Vector Register
BASE + 4	Write	DAC Data Register
BASE + 6	Write	Simultaneous Update Register
BASE + 8	Read/Write	Counter 0 (82C54)
BASE + 0Ah	Read/Write	Counter 1 (82C54)
BASE + 0Ch	Read/Write	Counter 2 (82C54)
BASE + 0Eh	Read/Write	Control Word Register (82C54)

"x" bits are "don't care"

Command and Vector ID Register (Write BASE + 0)

15 — 8	7	6	5	4	3	2 1 0
Interrupt Vector Identification	Siml Updt Sel	Siml Updt Mode	Ext/ Int Trig	Chan Auto Incr	I N T	Digital Outport 2 1 0

Digital Outport [Bits 2, 1, 0] — Discrete digital outputs are written to these bits

Trigger Interrupt Enable [Bit 3] — 0 = Disable interrupts; 1 = Enable interrupts

The trigger causes an optional VME bus interrupt using bit 3.

Channel Address Autoincrement [Bit 4] — 0 = No channel increment; 1 = Increment channel address after a DAC data register write.

In the non-increment mode (bit 4 = 0), successive writes to the DAC data register will load into a single DAC channel selected by the last address written into the channel address register.

In autoincrement mode (bit 4 = 1), the channel address will advance after each data register write. The address will cycle around to channel 0 after reaching channel 15, modulo 16.

Trigger Source Select [Bit 5] — 0 = Internal trigger; 1 = External trigger

The trigger may be supplied either from the internal clock (counters 0 and 10 or from an external digital trigger input. In simultaneous update mode (bit 6 = 1, bit 7 = 1), the trigger strobes all DAC channels simultaneously from previously written DAC data.

Simultaneous Update Mode [Bit 6] — 0 = Update via the simultaneous update register (Write BASE + 6); 1 = Update via internal or external trigger.

Simultaneous update causes all 8 or 16 DAC channels to be loaded with data that was last written to their input registers. If command bit 6 = 0, the trigger will be inhibited.

Simultaneous Update — 0 = Transparent mode (immediate DAC conversion of input data); 1 = Hold data until update.

With bit 7 = 0, DAC analog outputs will follow their input data values as fast as those values are written. If bit 7 = 1, updating the DAC outputs will wait until the trigger or a write to the update register.

Interrupt Vector ID [Bits 15 through 8] — The actual interrupt service routine must be loaded at id x 4 + Vector Base Register.

Status Register (Read BASE + 0)

15	14	13	12	11 – 8
Update Ready Status	Over Run Error	Not Used X	Interrupt Enable Status	Current Channel Address 3 2 1 0

7	6	5	4	3 2 1 0
Simul. Update Select	Simul. Update Select	External/ Internal Trigger	Chan Addrs Auto Increment	Digital Inport 3 2 1 0

Bits 4-11 may be used to verify bits loaded into the command register.

"X" bits are not used and should be ignored.

Digital Inport [Bits 3, 2, 1, 0] — Discrete digital inputs may be read in these bits.

Status Bits [Bits 7-4] — These bits follow the corresponding bits in the command register.

Current Channel Address [Bits 11-8] — These bits indicate either the last addresswritten into the channel address register or the next channel address to be written to by the next DAC data write. These addresses will sequence from channel 0 to 15, modulo 16 in autoincrement mode.

Interrupt Enable Status [Bit 12] — 0 = Interrupts disabled; 1 = Interrupts enabled

Bit 13 — Not used.

Over Run Error [Bit 14] — In trigger update mode (command 6 = 1), this bit will be set to one if a trigger occurs before the next load of the DAC data register. Any write to the command register resets bit 14 to zero.

Update Ready Status [Bit 15] — With command bit 7 = 1, a write to the simultaneous update register will set bit 15 to one. The trigger will reset this bit to 0, indicating that the next frame of data may be loaded. If a trigger occurs before bit 15 is set to 1, the over run error bit will be set to 1.

Bit 15 is normally polled to detect the trigger after loading the data registers. Bit 15 will stay at zero if command bit 6 = 0.

Channel Address Register (Write BASE + 2)

15 - 4	3 2 1 0
Not Used	Channel Address 3 2 1 0

In non-autoincrement mode, these bits select the address of the next channel to be written to by the DAC data register.

In autoincrement mode, these bits determine the starting channel address. After each data register load, addressing is automatically sequenced. The addressing cycles around to channel 0 after reaching channel 15.

Interrupt Vector ID Register (Read BASE + 2)

15 - 8	7 - 0
Not Used	Vector ID

This register may be used to verify the vector ID code written into bits 15 through 8 of the COMMAND Register.

DAC Data Register (Write BASE + 4)

15 - 12	11 - 0
Not Used	DAC MSB DAC LSB

12-bit DAC data are right justified with the most significant bit at bit 11. In bipolar coding, bit 11 indicates polarity (0 = negative, 1 = positive).

Simultaneous Update Register (Write BASE + 6)

15 - 8	7 - 0
Not Used	x - x

This register has two separate functions. If command bit 6 = 0 and command bit 7 = 1, the analog outputs of all DAC channels will be updated at the same time by writing any value to this register. If command bit 6 = 1, writing any value to this register will set the trigger ready status flag (status bit 15) to 1. The flag will remain set until cleared to zero by the trigger. This sequence provides a handshaking to load data frames without losing samples.

ORDERING GUIDE

Model	Number of channels
DVME-622A	8
DVME-622B	16
DVME-622SRC	Setup/Config. source disk, MS-DOS compatible

Boards are fully tested, calibrated, and supplied with a user manual. The setup and configuration program is on an MS-DOS diskette. All boards are burn-in tested under power-cycled conditions and include a one year warranty

DVME-691A Screw terminal panel for 19-inch rack mount. Includes flat cables to DVME-622.

82C54 Programmable Interval Timer

[Refer to the DVME-622 User Manual for detailed programming information]

Counter Register (Read/Write BASE + 8 - Counter #0)
(Read/Write BASE + 0Ah - Counter #1)
(Read/Write BASE + 0Ch - Counter #2)

15 - 8	7	6	5	4	3	2	1	0
x - x	C07	C06	C05	C04	C03	C02	C01	C00

Control Word Register (Read/Write BASE + 0Eh)

15 - 8	7	6	5	4	3	2	1	0
x - x	SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Select Counter

SC1	SC0	
0	0	Select counter #0
0	1	Select counter #1
1	0	Select counter #2
1	1	Read back command

Read/Load

RL1	RL0	
0	0	Counter latch operation
0	1	Read/Load LSB only
1	0	Read/Load MSB only
1	1	Read/Load LSB then MSB

Mode

M2	M1	M0	
x	1	0	Rate generator
1	0	0	Software trigger
1	0	1	Hardware trigger

BCD

BCD	
0	16-bit binary count
1	4-decade binary coded decimal count

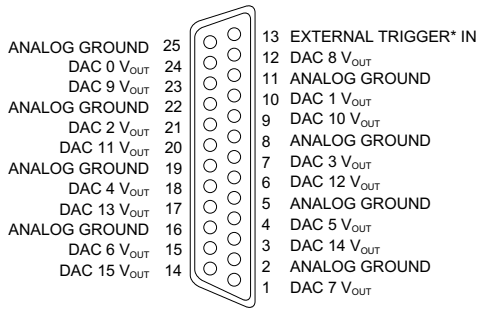


Figure 2. Analog Output Channel Connector - P3

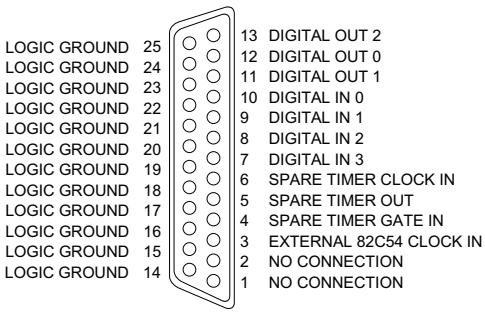


Figure 3. Digital I/O Connector - P4

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