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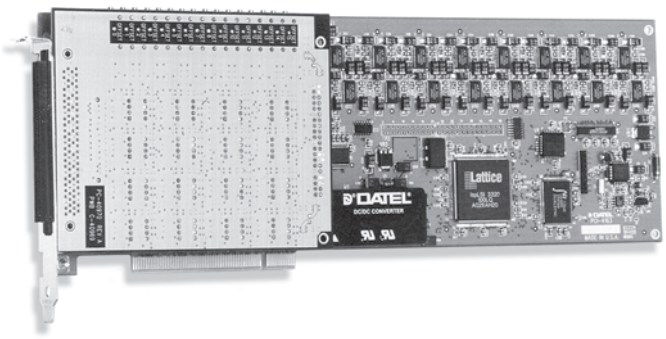
Find the *Datel PCI-4163* at our website: ***Click HERE***

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INNOVATION and EXCELLENCE

PCI-4163
Fast Differential Analog I/O Board for Desktop PCI-Bus Computers

FEATURES

- **16 differential protected analog input channels**
- **14-bit A/D conversion with on-board data memory**
- **Continuous streaming design for non-stop sampling**
- **Simultaneous sampling up to 500 KHz per channel**
- **Four on-board 16-bit analog output channels**
- **PCI bus DMA master to offload host CPU**
- **16 in, 16 out programmable digital I/O port**
- **Programmable 16-bit 10 MHz timer/counter**
- **Full Windows® DLL source code library**
- **LabVIEW® virtual instrument icons**
- **ActiveX/OLE controls for Visual BASIC, C++**



Today's high speed scientific measurement and signal processing systems have several critical needs which are met with the PCI-4163 combination analog (A/D-D/A) and digital Input/Output board for desktop PCI bus computers. First, high speed sensors often must be sampled precisely at the same time. Typical examples are phased array sensors, acoustic, seismic and sonar systems, simulators, robotics and parallel receiver channels. The PCI-4163 achieves this using sixteen separate A/D converters and input amplifiers, one per channel. Older analog multiplexer designs often introduce phase errors because channels are not sampled together.

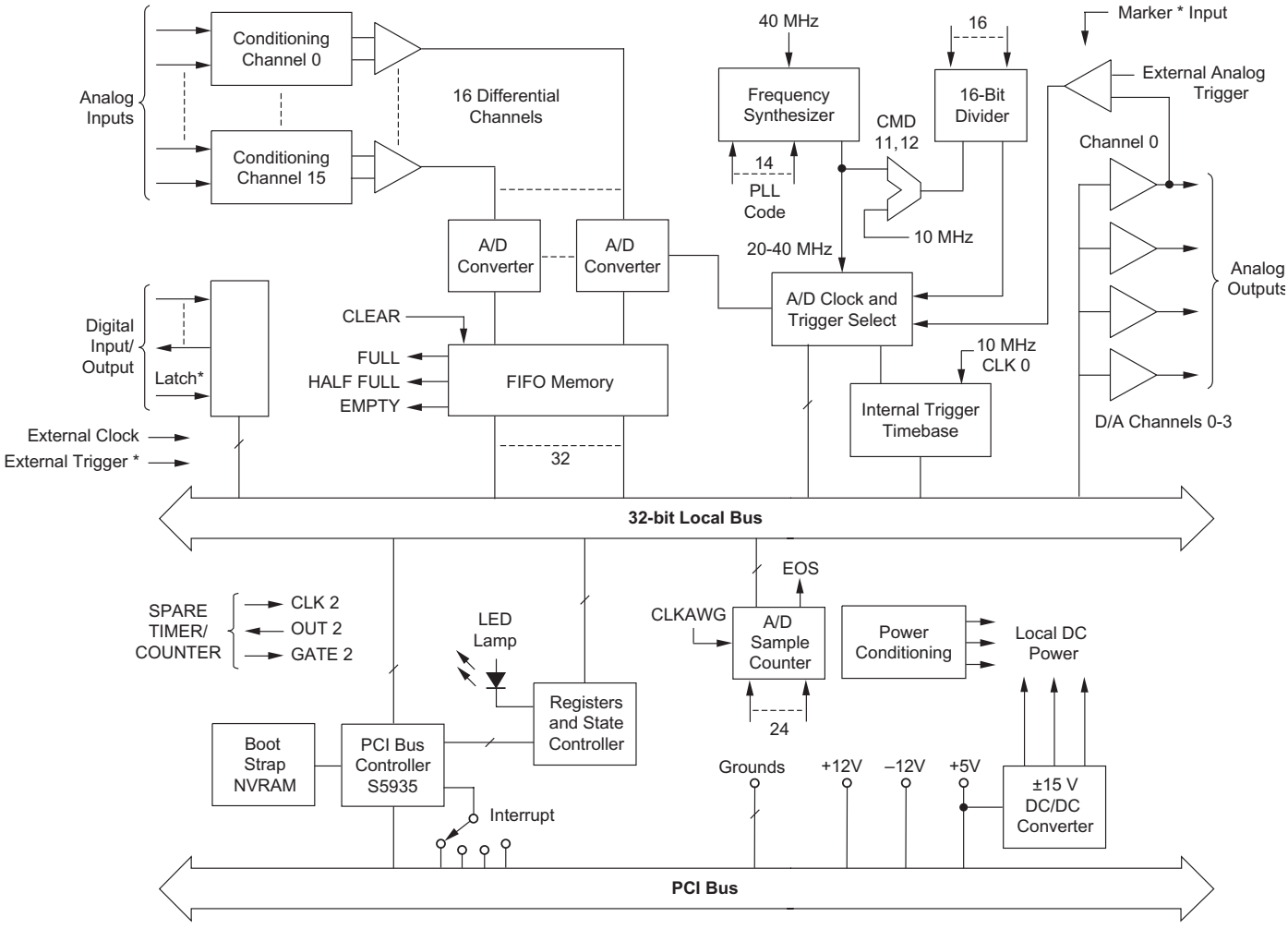


Figure 1. Simplified Block Diagram

Next, many systems use Windows or other modern multitasking systems. While very high performance, this software sometimes has random, unpredictable delays, risking possible loss of data. The PCI-4163 solves this with a local memory system for the A/D inputs which can manage itself and run automatically. The system can simultaneously read from the A/D section while writing out to the PCI bus, all without dropping samples.

Another feature to adapt the PCI-4163 to modern computer environments is the on-board bus master DMA controller for the PCI bus. The board can temporarily take over the PCI bus and perform its own block burst to host memory, all without delaying the CPU. The PCI-4163 can transfer data typically up to 60 megabytes per second. All of this capability is designed into the on-board programmable controller. The controller contains the PCI-4163's full register set which is accessed via the PCI Configuration Space.

Analog Inputs

Configured on a pluggable module, the PCI-4163's analog input section is fully differential and includes an overvoltage clamp system to protect all inputs against transient spikes. No analog input multiplexer is used. Since each high impedance channel is continuously connected to its own A/D converter, there are no settling delays or droop errors. Each channel can sample at up to 800 KHz per channel (2 channels) or 500 KHz per channel (16 channels).*

The A/D converter section may be clocked by a choice of an on-board frequency synthesizer, programmable crystal-stabilized timebase or external digital clock supplied by the user. The frequency synthesizer offers a wide range of sample rates whereas the crystal timebase is extremely stable. A/D samples are transferred in double word pairs of two adjacent channels to an on-board 32-bit wide local bus. Digitized analog samples are stored temporarily in an on-board FIFO (first in, first out) memory which is tightly integrated with the PCI bus interface and local state machine logic controller. The FIFO includes an overflow flag to indicate if the host CPU lost data.

To save memory by not sampling unwanted channels, the A/D channel addressing may be short cycled starting at channel zero. A fully programmable on-board trigger system starts each frame or the trigger may be supplied from an external user source, either level-triggered (analog) or by an external logic pulse. The frame length is set by an on-board sample counter which halts sampling when the programmed sample count is reached or can be programmed to run continuously "forever."

A special pretrigger mode collects data before an external trigger for transient event recording.

* Note - The aggregate sample rate increases for fewer selected channels. The sample interval is approximately = 1.2 µsec + (90 nsec x (number of selected channel pairs)).

DMA

The built-in Direct Memory Address (DMA) controller writes directly to PCI bus memory using very fast bus master PCI cycles. The system generates its own PCI bus destination address, maintains a count of the bytes transferred and automatically terminates when the Transfer Count reaches zero, giving a maskable interrupt to the host CPU to set up the next DMA block. On the host side, high performance DATEL device drivers look for the end of a block (either by DMA Terminal Count flag/interrupt or by frame count flag/interrupt) and automatically transfer blocks of data to kernel memory. In this manner, application software (calling DATEL's DMA device driver) maintains full control yet does not require CPU cycles to transfer each dword. Up to 16 million (2^{24}) dwords may be transferred in one block (32 million A/D samples) and the the DMA controller automatically arbitrates with other devices contending for the PCI bus, all without losing samples.

The entire system runs unattended most of the time to accomodate the non-deterministic nature of Windows' hardware servicing. This frees the CPU for important other tasks such as performing math on previously uploaded A/D blocks and/or screen displays. This combination of on-board automation and PCI bus DMA block burst operation offers true hardware multitasking.

To prevent false sampling in noisy environments using external A/D clocking, the on-board programmable overclock detector flags sample clocks which are received too early or not within the expected sample clock window. These errant clocks set a flag to indicate the presence of noise.

A marker channel input accepts an external digital bit so that A/D samples can be tagged relative to external events. Marked A/D samples are stored in the FIFO and DMA blocks within the A/D words for later analysis.

D/A's and Digital I/O

The general purpose analog output section uses four 16-bit D/A channels programmed in four 32-bit dwords with the data samples right-justified. The output range is ±10V. One D/A channel may be dedicated as a reference channel for the external analog comparator trigger.

Completing the assortment of inputs and outputs, an on-board 2 MHz parallel I/O port accepts up to 16 digital inputs or 16 digital outputs for discrete device control. The logic coding is programmable and the inport includes an external latch (strobe) input to capture transient data.

For full convenience, all I/O connections are available at the rear panel using a high density 100-pin connector. All DC power is supplied by the PCI bus. An on-board +5V-powered DC/DC converter supplies ±15V to linear sections

Spare Timer-Counter

A 16-bit timer/counter is included with a programmable divider. It accepts either an internal or external clock rate up to 10 MHz. The timer/counter may be used for any purpose.

SPECIFICATIONS

(Typical at +25°C, dynamic conditions, unless noted)

ANALOG INPUTS	
Number of input channels	16 differential inputs, non-isolated
Full scale input range	±10.00 Volts
Common mode range	Both inputs must remain within ±10 V of analog common at all times
Common mode rejection	90 dB typ., DC to 60 Hz
Overvoltage protection	±35 Volts max. sustained, no damage, power off or on <Note 16>
Input impedance	100 Megohms min.
Input bias current	50 pA
A/D CONVERTERS	
Number of A/D converters	Sixteen
A/D resolution	14 bits (1 part in 16,384)
Sample rate per channel	500 KHz max, all channels sampling simultaneously in parallel
Channel address shortcycling (software programmable)	Starting at channel zero, fewer channels may be sampled <Note 12>
Adjustments	Separate full scale and offset potentiometers are provided per A/D channel
A/D Total Harmonic Distortion	–93 dB, 100 KHz input, first 5 harmonics
A/D data format	Two's complement bipolar
A/D memory	8192 sample First-In, First-Out (FIFO) 4K x 32 <Notes 4 and 15>
A/D data packing	Two adjacent A/D channels are always transferred to the A/D FIFO
INPUT SYSTEM PERFORMANCE	
Differential nonlinearity and noise	± 1 LSB <Note 5>
Integral nonlinearity and noise	±2 LSB <Note 5>
System temperature coefficient	±20 ppm per degree C (zero) ±20 ppm per degree C (full scale)
ANALOG OUTPUTS	
Number of channels	Four single-ended, non-isolated <Note 18>
D/A resolution	16 bits, offset binary coding
Linearity	±3 LSB
Data format	The four channels are mapped on four consecutive dwords with data in bits 15-0. Bits 31-16 are not used.
Full scale output range	±10 Volts at 5 mA max. per channel.
Output load capacitance	500 pF max.
D/A settling time	10 microseconds to 0.01%, 20V step
Offset Error	±0.025% of FSR
Full Scale Error	±0.025% of FSR
Adjustments	No adjustments, the D/A's are pretrimmed.
MISCELLANEOUS	
Marker* input	External falling edge digital input sets A/D bit 31 to ONE for the next A/D clock then back to ZERO when removed. Used to tag samples to external events if enabled. <Note 11>
Rear panel connector	High density 100-pin miniature connector Robinson-Nugent part number P50E-100P1-SR1-TG <Note 13>
Frequency synthesizer output (for internal A/D clock)	20 to 40 MHz, software programmable in 2.5 KHz steps. The clock may be further divided from 2 to 65,536 using an on-board16-bit software programmable divider. Total range: 76.3 Hz to 10 MHz.
10 MHz crystal oscillator	May be used for optional internal A/D clock. Output is to the 16-bit software programmable divider (2 to 64 K).
General purpose timer/counter	Programmable timer/counter, 16-bit binary divider, up to 10 MHz, internal or external clocking, 82C54 controller
External A/D sample clock	A common clock input converts all selected A/D converters in parallel
LED Lamp	Programmable lamp on board interior, controlled by register bit <Note 2>
A/D TRIGGER AND SAMPLE COUNTER	
Function	Each trigger starts a frame of a counted number of A/D samples. The trigger is software selectable as either internal or external. Internal triggers use a 10 MHz 16-bit divider (range: 65 mSec to 5 µSec).
Trigger source	Selectable as internal trigger, external digital trigger, or external analog trigger
External analog trigger range	±10V. The reference level is set by D/A chan. 0. A positive-going level compared to the D/A causes a trigger. The user must remove the trigger before the start of the next frame.
Analog trigger hysteresis	The trigger will not retrigger until the signal has retraced approx. 25 mV from its initial level and the frame has completed
Analog trigger response	Triggering occurs within 3 microseconds of D/A threshold crossing, assuming that the analog level is within the linear operating region.
External digital trigger	External trigger must be a falling edge TTL pulse no longer than the sample count frame and 50 nSec min. <Note 7>
External trigger lockout	After a frame is started by an external trigger, additional triggers will be ignored and will not disrupt the present sampling frame. New triggers for the next frame will be acknowledged at the end of the present frame after a brief setup period (under 5 microseconds).
Sample counter	24-bit programmable counter sets the frame length, maximum 16,777,216 samples per frame. <Note 14>
Overclocking detection	External A/D clocks with a period shorter <Note 8> than the overclock detector will set an internal status bit which may be read by software. The status bit is cleared by resetting the A/D FIFO. The overclock condition will not stop A/D sampling.
Overclock range and selection	200 nSec to 65.536 mSec in 100 nSec steps. (Formed by 10 MHz counter and 16-bit programmable divider). The divider is software programmable.

PARALLEL DIGITAL I/O PORT	
Format	The parallel port consists of 16 inputs and 16 outputs. Each direction may be programmable positive or negative true by solder gaps.
Digital inport strobe	The digital inputs include an external latch input (Latch#/Follow) where data is stored on the falling edge of Latch#.The port is transparent in Follow mode. If no connection is made, a pullup resistor asserts Follow mode. The Strobe input may also set a selectable PCI bus interrupt.
Parallel port levels	Outputs: 4 TTL/LS loads. Inputs: 1 TTL load
Parallel port settling time	500 nanoseconds max.
Parallel port connector	Shared with A/D on rear-panel 100-pin connector
PCI BUS	
Data bus size	32 bits. Two A/D samples are always transferred together.
Base Address Register mapping	Reserves 256 bytes of I/O space
PCI bus interrupt	One interrupt, selectable as Int A (standard), B, C or D. This interrupt is shared between the data acquisition section and the optional DMA Terminal Count (TC = 0) state. <Note 10>
Non-DMA PCI Interrupt sources	Programmable as either A/D FIFO half full or End of Scan (sample count=0) or from parallel inport strobe input. These data acquisition interrupts may be disabled by software. <Note 10>
DMA bus mastering	The PCI-4163 will temporarily control the PCI bus in DMA mode to perform high speed automatic block transfers of A/D data. <Notes 1 and 6>
PCI Bus Controller Type	AMCC S5935
ENVIRONMENTAL, MECHANICAL	
Power required <Note 9>	+5 Vdc @ 4 Amps max. from PCI bus –12 Vdc @ 600 mA max. +12 Vdc @ 400 mA max.
Outline dimensions	Desktop PCI bus, 12.375" long x 4.125" high (PC board not including connectors). Does not interfere with adjacent boards.
Fabrication	Multi-layer, high density surface mount glass-epoxy printed circuit board. CAUTION: Do not flex the board or apply mechanical stress.
Manufacturing environment	ISO 9001 certified facility and procedures
Operating temperature range	0 to +60°C., no thermal shock, no condensation
Storage temperature range	–25°C to +85°C
Burn-in	48 hours, power and temperature cycled 2 hours, 0 to +60°C
Altitude	0 to 10,000 feet, forced cooling required
Identification code	Available in on-board non-volatile EEPROM <Note 3>

Specification Notes

[1] For DMA, the PCI-4163 must use a PCI slot which accepts bus mastering. The D/A and digital I/O sections do not use DMA.

[2] The LED lamp is located on the top edge of the board and is intended as a programmer's diagnostic and development aid for any purpose. The computer cover must be open to view the lamp. After successful loading, the device driver turns the lamp on.

[3] The PCI-4163 includes a non-volatile electrically erasable programmable memory (EEPROM) which initializes the S5935 PCI controller at power up. Spare EEPROM data area is available under user programming. The user may read or write to the EEPROM, however access must not be done during data acquisition. Improper EEPROM writes could disable the board, requiring reprogramming by DATEL.

[4] The FIFO issues three signals - empty, half full and full.

[5] The linearity specifications also include expected noise and are a system specification. Excessively noisy host computer environments may degrade these specs. The board should be positioned away from higher emission parts of the computer.

[6] The most common method to implement the A/D streaming feature is to use a pair of swapped buffers on the host side. While the board is filling one buffer via DMA, the host may concurrently process the previous alternate buffer. This streaming feature is independent of the host Operating System or language type. Streaming may occur for millions of A/D samples and is limited only by host-side storage.

[7] For highest reliability, use only a single trigger pulse during a frame. To avoid false triggering or lost data, make sure the digital trigger characteristics (ringing, impedance matching, risetime, reflections, etc.) at the board are high quality.

[8] External A/D Overclock Detection:
Since the internal overclock detector is asynchronous with the external A/D clock and has a resolution of ±100 nSec, the actual time of lockout will vary ±100 nSec for each A/D clock cycle. A short interval of less than 100 nS setup time after an A/D clock will not detect the overclock condition.

[9] For linear circuits, the PCI-4163 uses both the computer ±12V dc supply and generates additional ±15V dc power using an on-board DC/DC power converter. Some computers have limited 12V power. Check your computer carefully.

[10] Interrupts:
The S5935 includes only one PCI bus interrupt selectable on lines Int A, B, C or D. This interrupt may be selected between the DMA TC and the mailbox interrupt (both may be enabled simultaneously). Either interrupt state may be polled in the S5933. The mailbox interrupt is further subdivided by the A/D Command Register as either (but not both) the A/D FIFO half full signal or the End of Scan signal when the Sample Counter reaches zero and A/D sampling stops or the parallel inport strobe input.

The DMA TC may be either polled or selected to a PCI bus interrupt. Normally the single interrupt should remain on INT A (the default) and should only be moved if there is a verifiable conflict with another board.

[11] If the Marker input is not synchronous with the A/D clock, the marked sample may be delayed one or two samples from the expected sample. The Marker width must exceed one A/D clock period.

[12] Short cycling is available in pairs of adjacent channels down to two channels (0 and 1). A/D channel short cycling does not significantly increase the total throughput speed but does save memory storage.

[13] The mating connector (on an external flat cable) is Robinson-Nugent part number P50E-100S-TG.

DATEL offers a mating cable, model PC-100CBL which includes two 50-pin (2x25) standard flat cable header connectors.

[14] Once initially programmed, the A/D Sample Counter auto-reloads for successive triggers. The counter may be software disabled for indefinite sampling.

[15] Note that as long as host side software retrieves the data in block streaming mode, there is essentially no speed advantage to larger, more costly FIFO's.

[16] CAUTION: Instantaneous input voltages greater than ±35V may damage the board. Use external voltage clamps or other methods to avoid overvoltage. Fuses are not sufficient.

[17] "#" and "*" symbols mean negative true when associated with logic signals.

[18] The D/A's do not include on-board memory. Note that if you use the analog trigger, D/A channel 0 must be assigned as the trigger threshold comparator .

[19] CAUTION: The A/D inputs are differential and protected but they are not isolated. A bias current return path must be provided by the user. (In other words, do not connect only the positive and negative inputs). The D/A outputs are also non-isolated. Wire the analog signals properly to avoid ground loops, input saturation or damaging overvoltages.

Marker Input and Data Format

The external digital Marker input tags A/D samples relative to outside events such as a clock timebase. The Marker sets bits 15 and 31 of the data doubleword for one A/D clock cycle. The tag is now stored in the FIFO along with the A/D samples. The user may do this as often as needed. Post processing software then searches through the saved data to find each marked sample.

Markers may be asynchronous with A/D clocks but if so, the Marker must be held longer than one A/D clock to insure that the sample is marked. Depending on the phase and length of the Marker versus the A/D clock, you may get one or two marked samples. You may also hold the Marker indefinitely and, as long as A/D sampling continues, the saved Marker bits will simply record the start and end of the marked session.

The "scan sync" is located in bits 14 and 30. Scan sync indicates when the lower word corresponds to A/D channel zero. This allows the software to recover data which may have become skewed or out of sequence. User software may analyze streams of scanned A/D data seeing if every eighth DWORD contains valid Scan Sync bits.

Data is delivered as a stream from the FIFO. For multichannel inputs, the data is multiplexed by the channel address with a modulo address wrap-around at the top channel. For example, with 16 channels, the output sequence is 0, 1, 2, ... 14, 15, 0 , 1, ... And since the system always transfers two samples, the longword sequence is 0, 1 ... 2, 3 ... etc.

31	30	29	28-17	16	15	14	13	12 to 1	0
External Marker input	Scan Sync	A/D MSB bit 13	A/D bits 12-1	A/D LSB Chan N+1	External Marker input	Scan Sync	A/D MSB bit 13	A/D bits 12-1	A/D LSB Chan N
		Channel N + 1					Channel N		

Marker: 0 = no marker received, 1 = external marker bit received

Scan sync: 0 = not on channel zero, 1 = the sample in bits 13-0 is channel zero.

Channel Addressing

The PCI-4163 uses two channel addressing formats depending on the "SSH" bit 4 in the Command Register. If CMD4 = 0, the PCI-4163 will only transfer two adjacent channels with each A/D clock. The lower channel is designated in the Channel Address Register.

If CMD4 = 1, the PCI-4163 will transfer N+2 channels with each A/D clock starting from channel zero. The addressing will "short cycle" up to channel address N+1 with an address of N written into the Channel Address Register. Thus for a channel address code of four (N = 4), the board will transfer six channels (0 to 5).

Two A/D samples are always transferred per longword ("data packing"). The lower word should be an even channel and the upper word is the next sequential odd channel. The data format for A/D bits 13 to 0 and bits 29 to 16 is two's complement bipolar.



Model PC-100CBL

PCI-4163 Hardware Register Map

All addresses given below are byte addresses even though all access must use 32-bit wide DWORDS and some registers have only 8 or 16 active bits. Note that word (16-bit) or byte (8-bit) registers are right justified and occupy the lease significant bits in the doubleword. Unused higher order bits are “don’t care.” Also, some “registers” do not have data but instead each access performs a simple function such as resetting the FIFO.

Register	Direction	Address	Use PassThru Region
Command/Status Register	Read/Write	PassThru Base + 0	2
Sample Count Register	Write only	PassThru Base + 4	2
Current Sample Count	Read only	PassThru Base + 4	2
Reset A/D FIFO memory	Write only	PassThru Base + 8	2
Status 2 Register	Read only	PassThru Base + 8	2
A/D Channel Address Register	Write only	PassThru Base + 12	2
A/D FIFO Data Register	Read only	PassThru Base + 12	2
A/D Convert Enable Register	Write only	PassThru Base + 16	2
Timebase Divisor Register	Write only	PassThru Base + 20	2
Overclock Data Register	Write only	PassThru Base + 24	2
Reset Overclock Register	Read only	PassThru Base + 24	2
Digital Outport Data Register	Write only	PassThru Base + 28	2
Digital Inport Data Register	Read only	PassThru Base + 28	2
Phase Lock Loop Divisor Register	Write only	PassThru Base + 32	2
D/A Channel 0 Data Register	Write only	PassThru Base + 48	4
D/A Channel 1 Data Register	Write only	PassThru Base + 52	4
D/A Channel 2 Data Register	Write only	PassThru Base + 56	4
D/A Channel 3 Data Register	Write only	PassThru Base + 60	4
82C54 Timer 0 Data Register	Read/Write	PassThru Base + 64	4
82C54 Timer 1 Data Register	Read/Write	PassThru Base + 68	4
82C54 Timer 2 Data Register	Read/Write	PassThru Base + 72	4
82C54 Timer Control Register	Read/Write	PassThru Base + 76	4

PCI-4163 Rear Panel P4 100-position Connector Pinout

(Pins are shown as viewed from the rear panel. Pin one is at the upper left.)

Line Name (function)	Pin	Pin	Line Name (function)
Analog input channel 0 High	1	51	Analog output channel 0
Analog input channel 1 High	2	52	D/A channel 0 Sense In
Analog input channel 2 High	3	53	Analog and Digital Ground
Analog and Digital Ground	4	54	Analog output channel 1
Analog input channel 3 High	5	55	D/A channel 1 Sense In
Analog input channel 4 High	6	56	Analog and Digital Ground
Analog input channel 5 High	7	57	Analog output channel 2
Analog and Digital Ground	8	58	D/A channel 2 Sense In
Analog input channel 6 High	9	59	Analog and Digital Ground
Analog input channel 7 High	10	60	Analog output channel 3
Analog input channel 8 High	11	61	D/A channel 3 Sense In
Analog and Digital Ground	12	62	Digital In 15
Analog input channel 9 High	13	63	Digital In 14
Analog input channel 10 High	14	64	Digital In 13
Analog input channel 11 High	15	65	Digital In 12
Analog and Digital Ground	16	66	Analog and Digital Ground
Analog input channel 12 High	17	67	Digital In 11
Analog input channel 13 High	18	68	Digital In 10
Analog input channel 14 High	19	69	Digital In 9
Analog and Digital Ground	20	70	Digital In 8
Analog input channel 15 High	21	71	Analog and Digital Ground
Analog input channel 0 Low	22	72	Digital In 7
Analog input channel 1 Low	23	73	Digital In 6
Analog and Digital Ground	24	74	Digital In 5
Analog input channel 2 Low	25	75	Digital In 4
Analog input channel 3 Low	26	76	Analog and Digital Ground
Analog input channel 4 Low	27	77	Digital In 3
Analog and Digital Ground	28	78	Digital In 2
Analog input channel 5 Low	29	79	Digital In 1
Analog input channel 6 Low	30	80	Digital In 0
Analog input channel 7 Low	31	81	Analog and Digital Ground
Analog and Digital Ground	32	82	Digital Out 15
Analog input channel 8 Low	33	83	Digital Out 14
Analog input channel 9 Low	34	84	Digital Out 13
Analog input channel 10 Low	35	85	Digital Out 12
Analog and Digital Ground	36	86	Analog and Digital Ground
Analog input channel 11 Low	37	87	Digital Out 11
Analog input channel 12 Low	38	88	Digital Out 10
Analog input channel 13 Low	39	89	Digital Out 9
Analog and Digital Ground	40	90	Digital Out 8
Analog input channel 14 Low	41	91	Analog and Digital Ground
Analog input channel 15 Low	42	92	Digital Out 7
Analog and Digital Ground	43	93	Digital Out 6
+5 Vdc power out (500 mA max.)	44	94	Digital Out 5
Analog and Digital Ground	45	95	Digital Out 4
Digital Inport Latch Input	46	96	Analog and Digital Ground
Marker* Input	47	97	Digital Out 3
Analog Trigger Input	48	98	Digital Out 2
External Digital Trigger* Input	49	99	Digital Out 1
External A/D Clock Input	50	100	Digital Out 0

Software Architecture

DATEL-developed software is ideal for developers and consists of a DATEL-written device driver and Dynamic Link Library (DLL) which are installed at boot up. The DLL functions call the driver functions and are fully documented in the User Manual. The DLL's are in turn called by a menu-driven user interface. Also included is an ActiveX controls library which may be called from C++, Visual BASIC and several other systems.

The DLL is the foundation for all other high-performance applications of the PCI-4163. It fully supports PCI bus master DMA block transfers, interrupts and memory allocation.

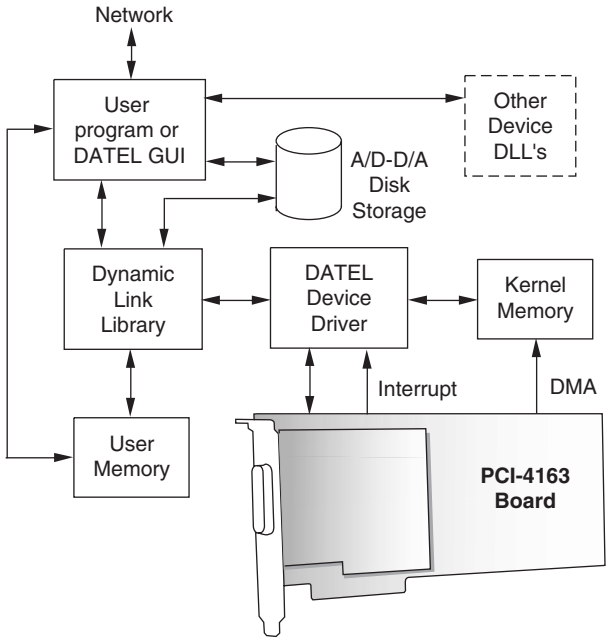
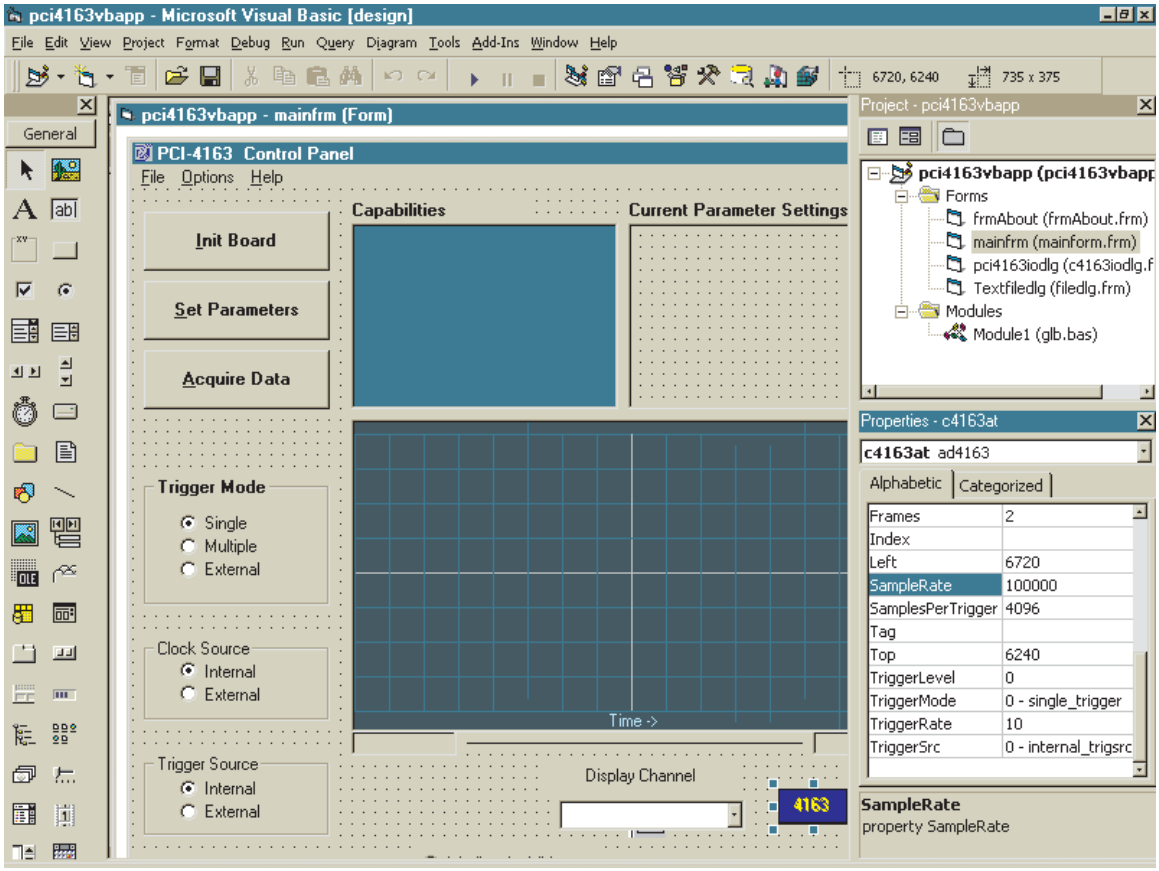


Figure 2. Software Architecture



Visual BASIC Design Form for pci4163vbapp

Trigger and Sample Count Systems

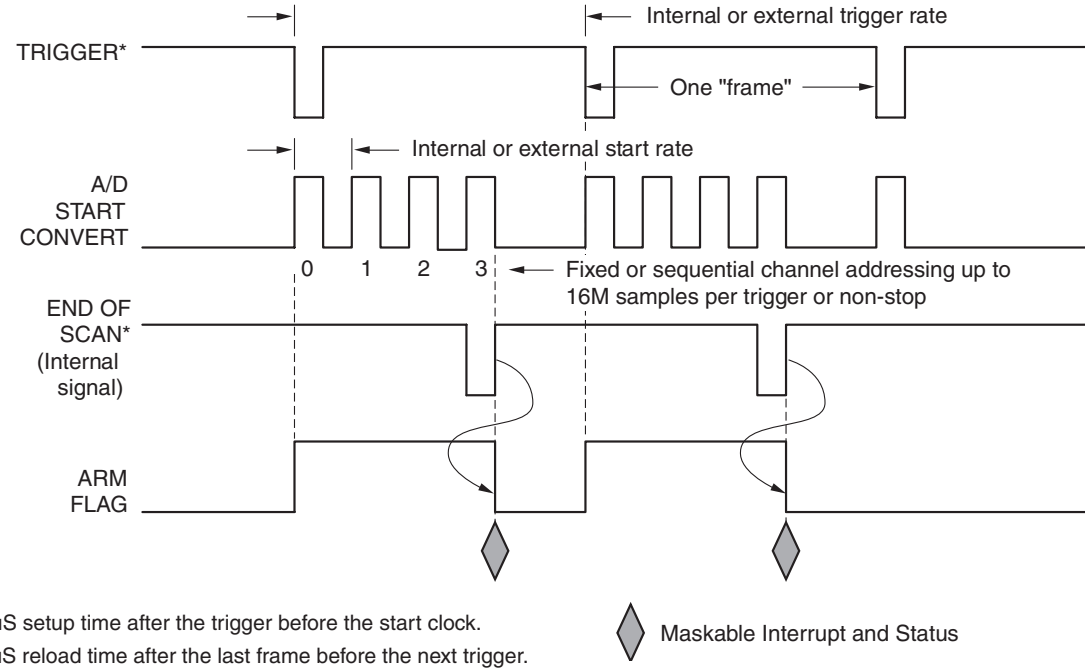
The PCI-4163 accepts one of three triggers - external analog, internal, or external digital. All three initiate identical internal actions. For the internally generated trigger, either a single trigger can be accepted (“single trigger mode”) or the trigger can repeat (“continuous trigger mode”) with a programmable delay between each trigger.

The trigger starts a frame of samples. Each frame can be up to 16,777,216 samples per channel using the 24-bit counter. The system will collect the number of samples in the sample counter then stop and wait for the next trigger. Meanwhile, the sample counter will automatically reload in anticipation of the next trigger. Data flows into the FIFO memory which will notify the host that it has data to be saved. The FIFO size is independent of the frame size, therefore FIFO flags will occur asynchronously from the sample counter.

A PCI interrupt can be generated after each frame completes or at each FIFO half full signal.

The PCI-4163 will automatically control its own channel addressing such that the address advances immediately as a sample is sent to the FIFO. In automatic sequential addressing (“autoincrement”), the frame will contain one or more scans of channels, with addresses automatically wrapping around according to the channel capacity.

The combination of programmable sample count, frame rate, A/D rate, and channel addressing mean that practically all conceivable applications can be accomplished. The basic system timing is shown in Figure 3.



Notes

1. Allow 1 µS setup time after the trigger before the start clock.
2. Allow 1 µS reload time after the last frame before the next trigger.
3. Sampling starts on the next A/D clock after the trigger. Do not make the A/D clock coincident with the trigger.

Figure 3. PCI-4163 A/D Timing Diagram

Pre/Post Trigger Transient Capture Applications

A certain class of applications requires data sampled relative to one or more external events. Data before and after the event need to be analyzed. If the exact time of those external events cannot be predicted accurately but the event can be identified with a trigger, data must be recorded continuously then processed after the event occurred. At higher sample rates, the user must use all memory storage, which has limited capacity, but is still large enough to capture the event. A ring buffer circular storage method is used in which new samples continually overwrite the oldest samples.

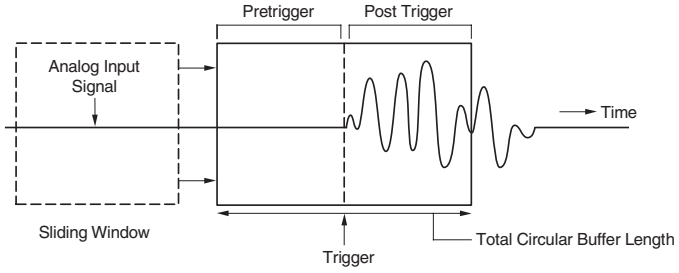


Figure 4. Transient Signal Capture

The PCI-4163 accepts either a digital or analog (threshold trip) event trigger. An on-board D/A converter sets the comparator voltage level for the analog trigger. The system stores data before and after the trigger. A post trigger sample counter selects the number of offset samples after the trigger. The number of pretrigger samples equals the total circular storage minus the post trigger size. Note that pretrigger samples in Figure 5 are skewed over the buffer tail.

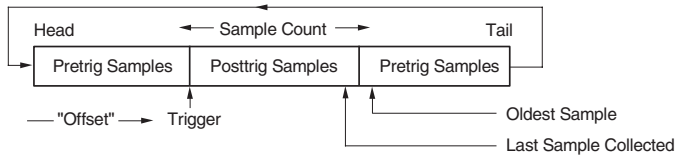


Figure 5. A/D Data Ring Buffering

A/D collection continues after the trigger until the system has stored the number of samples specified in the sample counter. The trigger sample can be found using backwards circular offset from the last sample saved. Multiple external events can be identified using a combination of the post trigger method and the marker inputs.

The PCI-4163 can access huge PCI memory. Collected A/D samples can then be saved to disk or tape.

Simultaneous Sampling Technology

The PCI-4163 employs multi-channel simultaneous sampling to collect A/D samples exactly in parallel from a single A/D start clock. Older analog multiplexer methods use a slower single A/D converter with settling delays, MUX switching transients and overload recovery problems. The PCI-4163's A/D-per-channel technology avoids skew delays in multi-sensor applications, phased-array systems and simultaneous receiver channels. This provides excellent correlation between channels and removes a significant source of phase errors found in older architectures.

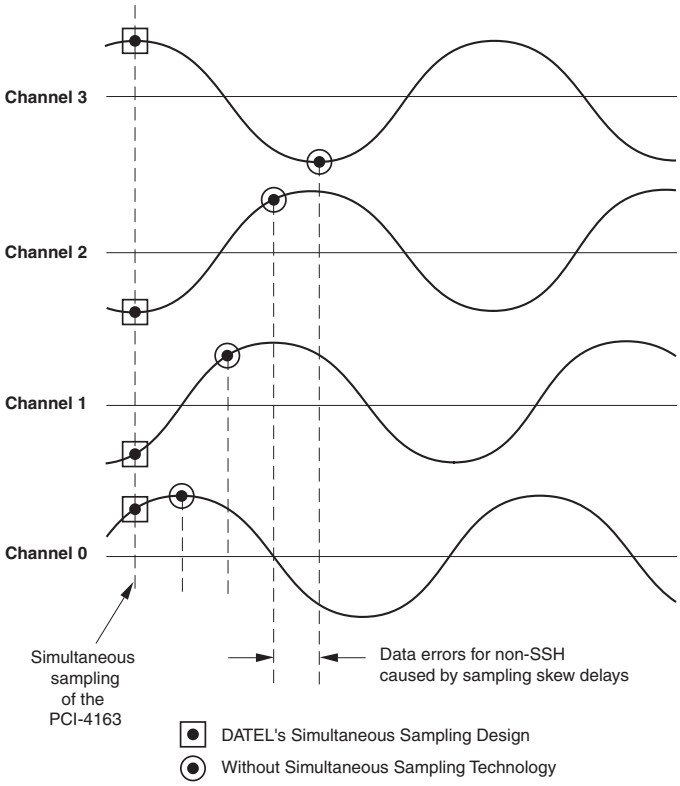


Figure 6. PCI-4163 Simultaneous Sampling

Minimum System Requirements

To run the PCI-4163 successfully, your host computer must meet or exceed the specifications below.

The basic guideline is to use a host computer which is compatible with the installed Operating System. The OS requirements are generally greater than the PCI-4163 software.

Operating System:

Windows 98SE (Second Edition).

Windows NT 4.0 with Service Pack 4 or later.

Windows 2000 (use the latest Service Pack)

Windows ME or XP

Windows 95 or 98 (first edition) are not supported.

An MS-DOS example program is included on PC-CDROMS. The PCI-4163 hardware will operate with other OS's (e.g. LINUX) or other CPU's if configured by the user and if the PCI bus is 100% compatible.

CD-ROM Drive: The CD-ROM is required for software loading of DATEL's disk. Speed is not critical.

Memory: Use the minimum memory required for the OS, plus buffer space to save data. (The PCI-4163 will actually run in a 32 Mb system). Windows normally will not allocate more than about one half the physical memory for A/D buffers.

Hard Disk: The PCI-4163 needs 20 Mb of disk to load and run the GUI plus optional disk space to save data. Higher A/D rates should use higher RPM drives (7200 RPM minimum) to stream data to disk. Two or more swapped drives are preferred or consider a RAID system.

Graphics: Any SVGA system or higher is sufficient (not critical). DATEL's software does not use any on-board graphics accelerator features.

CPU: The host processor should be at least a 266 MHz Pentium or equivalent. Higher speeds are recommended, especially if your CPU will process the data between DMA blocks. Slow CPU's will cause A/D overflow errors with increasing sample rates and/or heavier interblock processing. The PCI-4163 will operate however with minimum speed CPU's.

PCI Bus: The PCI-4163 must use a DMA bus master slot for DMA transfers. Make sure you have sufficient DC power.

Language: DATEL software is almost entirely Microsoft Visual C++ v6.0. DATEL's ActiveX/OCX controls and DLL may be called from Visual BASIC and other systems.

Compatibility: For highest performance and no lost data, close or remove all other unnecessary background tasks or processes.

Software Versions

Two versions of DATEL's software are offered. Model PC-CDROM includes binary-only executable files. PC-CDROM is included at no charge with the board purchase. Model PC-CDROMS (note the "S") contains both the source code to PC-CDROM and the binaries. Both CD-ROM disks cover Windows 98SE, NT, 2000, XP, and ME.

Software

DATEL's software for the PCI-4163 helps programmers develop their own C++ or Visual BASIC systems or for users of signal processing systems such as LabVIEW. All current Windows systems are supported starting from Windows 98 Second Edition. The source disk also contains a small MS-DOS example program.

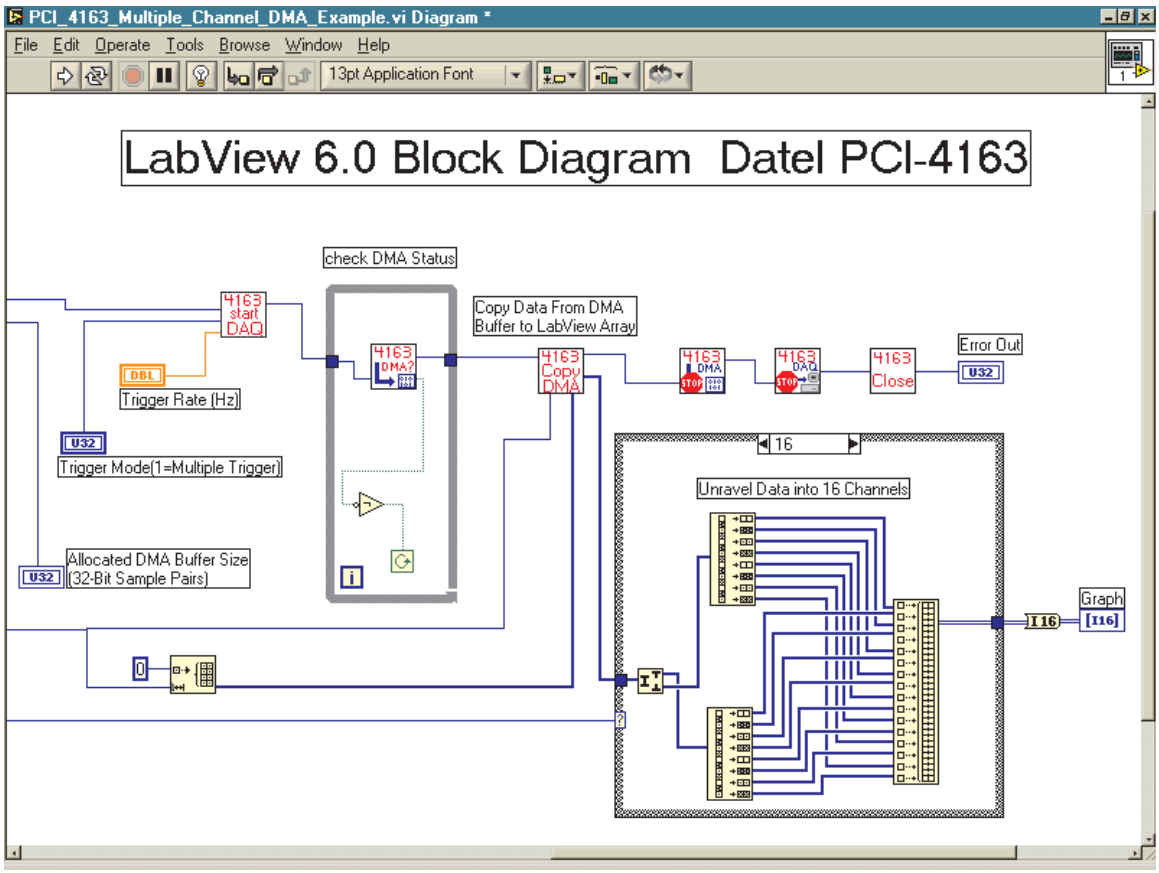
The software consists of three levels. System initialization automatically installs a memory-resident DATEL-written device driver. The driver is very high performance and talks directly to the board registers. It allocates interrupts, memory buffers, the DMA channel, etc.

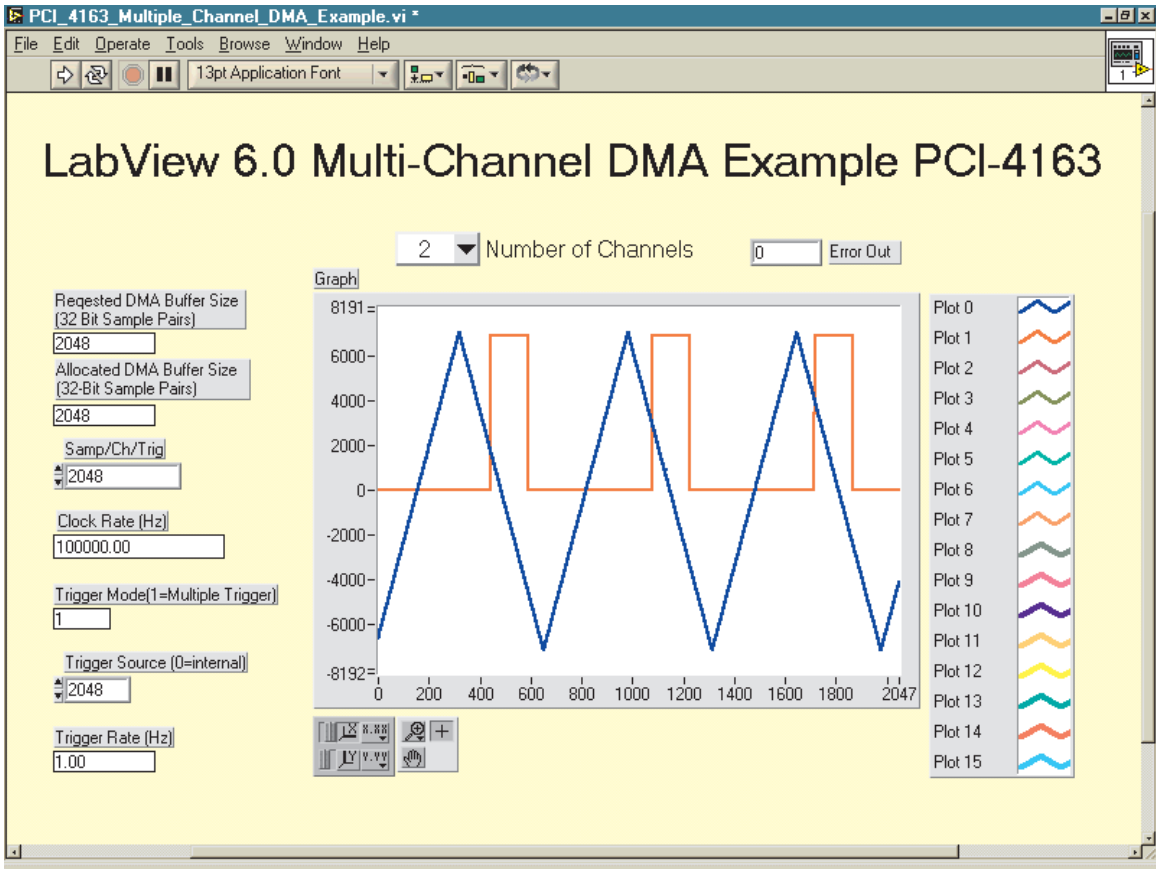
DATEL's Dynamic Link Library (DLL) for Windows offers a convenient programming interface for users and communicates with the driver so the user can avoid writing low level functions. Finally, a DATEL-written menued Graphical User Interface (GUI) calls the DLL's and forms a comprehensive programming example. While not intended to serve all conceivable applications, the GUI also sets up and self-tests the board, performs calibration, displays signal waveforms and saves data to either memory and/or disk. The output files may be used with spreadsheet, database, presentation and signal processing programs.

Source code for the DLL library and GUI are professionally written (mostly in C++), well organized and heavily commented. The sources are available on CD-ROM and the User Manual contains documentation on the functions. DATEL also offers ActiveX/OLE controls on the source disk for easy integration into Visual BASIC, C++ Builder and numerous other ActiveX packages. A Visual BASIC example is included which is based on the ActiveX controls. A series of Virtual Instrument (VI) icons is available for integration with LabVIEW 5.1 and 6.1.

The highest performance is available through the DLL's. The ActiveX controls (due to delays in the Windows messaging system), are less suitable for very high speed DMA operations.

Two versions of the CD-ROM are available. Binary executable versions of the software on CD-ROM are supplied at no charge (model PC-CDROM) with purchase of the board. The optional source code is offered on model PC-CDROMS.


PCI_4163_Multiple_Channel_DMA_Example.vi Diagram *
File Edit Operate Tools Browse Window Help
13pt Application Font
LabView 6.0 Block Diagram Datel PCI-4163
check DMA Status
4163 start DAQ
DBL
Trigger Rate (Hz)
U32
Trigger Mode(1=Multiple Trigger)
U32
Allocated DMA Buffer Size (32-Bit Sample Pairs)
4163 DMA?
Copy Data From DMA Buffer to LabView Array
4163 Copy DMA
4163 DMA
4163 DAQ
4163 Close
Error Out
U32
16
Unravel Data into 16 Channels
I16
Graph
[I16]
0

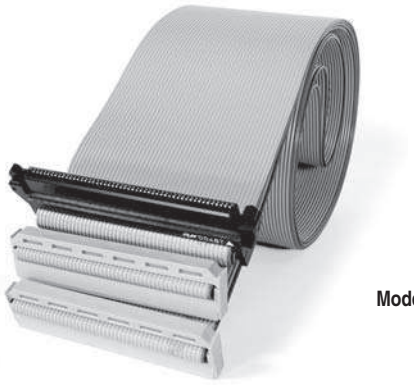

PCI_4163_Multiple_Channel_DMA_Example.vi *
File Edit Operate Tools Browse Window Help
13pt Application Font
LabView 6.0 Multi-Channel DMA Example PCI-4163
2
Number of Channels
0
Error Out
Graph
Reqested DMA Buffer Size (32 Bit Sample Pairs)
2048
Allocated DMA Buffer Size (32-Bit Sample Pairs)
2048
Samp/Ch/Trig
2048
Clock Rate (Hz)
100000.00
Trigger Mode(1=Multiple Trigger)
1
Trigger Source (0=internal)
2048
Trigger Rate (Hz)
1.00
8191
6000
4000
2000
0
-2000
-4000
-6000
-8192
0 200 400 600 800 1000 1200 1400 1600 1800 2047
Plot 0
Plot 1
Plot 2
Plot 3
Plot 4
Plot 5
Plot 6
Plot 7
Plot 8
Plot 9
Plot 10
Plot 11
Plot 12
Plot 13
Plot 14
Plot 15

Ordering Guide

Model Number	Description
PCI-4163	A/D-D/A-I/O Board. Includes PC-CDROM binary executable software disk and comprehensive User Manual with detailed register and software information.
PC-CDROMS	Optional Source code disk to PCI-4163 board.
PC-100CBL	Optional Cable assembly, three feet long. Connects from the rear panel 100-pin Robinson Nugent connector to two 50-pin (25x2) flat cable headers with 0.100-inch pin spacing.
UM-PCI-4163	Spare User Manual. One is included with board purchase.
PC-491	50-conductor screw terminal adaptor, plugs into PC-100CBL. Two PC-491's are required per PCI-4163.



PCI-4163 Comprehensive User Manual and Optional Source Code



Model PC-100CBL

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Model PC-491

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