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ST-711/732

32 A/D, 2 D/A Channel Analog Boards for MULTIBUS Microcomputers

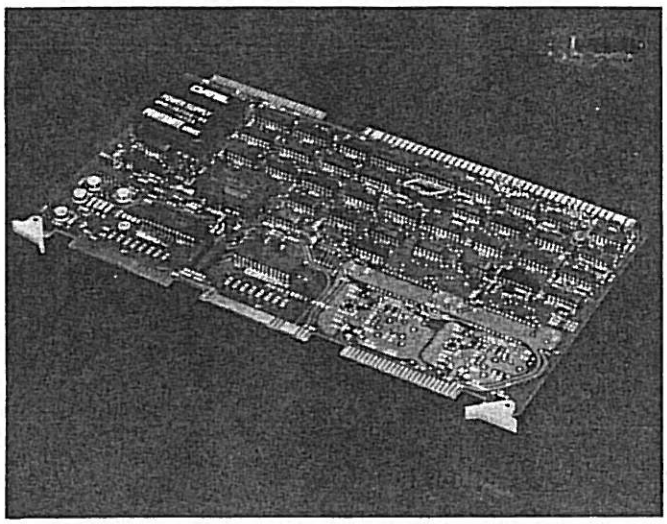
PRODUCT DATA SHEET

SPECIAL FEATURES

- **Model ST-711 — 32 Single-Ended, 16 Differential Input A/D Channels**
- **Model ST-732 — 32 Single-Ended, 16 Differential Input A/D Channels plus 2 D/A Output Channels**

COMMON FEATURES

- **Operate with all MULTIBUS compatible microcomputers using 16-, 20-, or 24-bit addressing, 8-bit data transfer**
- **Work directly from RMX-86 Analog I/O Driver operating software**
- **Include a 10-stage jumper-selected, program-gatable pacer start clock, 1 mS to 1 second, crystal-controlled**
- **A/D input accept up to 16 user-installed shunts for 4-20 mA etc., current inputs**
- **FET-Input differential amplifiers accept on-board resistor for fixed high gain up to X1000 (10 mV full scale range)**
- **Include Programmable Gain Amplifier (X1, 2, 4, 8 gains)**
- **Work with the latest 80X86 and 680X0 CPU's**
- **May be used with any language or operating system**



GENERAL DESCRIPTION

Functionally, DATEL's ST-711 and ST-732 are complete analog input systems for the MULTIBUS iSBC environment. These slide-in peripheral boards accept analog signals from up to 32 single-ended or 16 differential input channels, with the user able to reconfigure the boards using simple jumpers. In addition, the ST-732 provides two digital-to-analog output channels with current loop amplifiers

The differential input channels accept either voltage or current inputs. For current input applications, the user would install shunt resistors across each input channel into circuit pads provided .

Both boards have on-board ±15V power supplies, programmable gain amplifiers (PGA), and a 10-stage crystal pacer clock. Jumpers select the base memory address as well as control the conversion, scan, and external start interrupts.

Other important features include memory-mapped interfacing, addition of a FET input programmable differential amplifier, and complete pin-for-pin form, fit, and function identity to competitive iSBC-711/732 series A/D-D/A board systems. This last feature allows DATEL's ST-711/732 to operate directly from RMX-86 Analog I/O Drivers (Realtime Multitasking Executive Software).

For conversion control, the ST-711 includes on-board registers to store start and final A/D channel address, status bits, conversion modes and interrupt enables.

An A/D Converter auto-increment mode, which is program-selected, automatically advances the channel address after each conversion. Successive A/D samples will continue until the program-selected last channel address is reached.

The ST-732 is identical to the ST-711; both include two 12-bit hybrid DAC-HK D/A converters with input registers.

FUNCTIONAL DESCRIPTION

The A/D sections of the ST-711/732 use DATEL's hybrid technology ADC-HS combined successive approximation A/D converter and Sample/Hold Amplifier. The ADC-HS features 5 microseconds S/H acquisition time and 8 microseconds A/D conversion time and 12 bit binary resolution. System accuracy varies from ±0.05% of FSR ±1/2 LSB (10V range) to ±0.3% FSR ±1/2 LSB (10 mV range), including noise, quantization, nonlinearity, and dynamic errors.

The ST-711/732 employ DATEL's MX-1606 series fast CMOS multiplexers which incorporate ±35 Volts overvoltage protection. Input impedance is 100 meg-ohms minimum (power on) with 30 pA typical input bias current. Balanced inputs require 5 kilohms maximum source impedance to maintain accuracy and throughput rate.

All models inlcude an FET input differential amplifier which is wired as single-ended for the 32-channel models.

The standard A/D-D/A digital coding is offset binary (bipolar) but jumpers may easily be changed to straight binary (unipolar) or 2's complement (bipolar). Standard A/D-D/A analog signal ranges are ±10V full scale but may be jumper selected to ±5V, or +5V, or 10V unipolar.

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SPECIFICATIONS

(Typical at 25 °C, dynamic conditions, unless noted).

GENERAL

Configurations available

Model ST-711
32S/16D A/D channels, no D/A channels

Model ST-732
32S/16D A/D channels, 2 D/A channels

Overall System Throughput (high level signals)
23,000 samples/second

ANALOG INPUTS

Number of Channels
32 single-ended or 16 differential
(Jumper-selected. 32S supplied standard)

Channel Expansion
May expand indefinitely by using additional ST-711/732 boards with different base address. Expansion limited by board slots and power.

Input Type
High impedance voltage input, non-isolated. Differential inputs are balanced.

Current Inputs
Up to 16 differential voltage inputs may be converted to differential current inputs with shunt resistors provided and installed by the user. Pads on the board will accommodate 4-20 mA, 1-5 mA, 10-50 mA and other ranges. 4-20 mA ranges require 250Ω, 1/4W ±1% resistors, ±100 ppm/ °C max.

Input Overvoltage
±35V sustained (no damage)

Input Capacitance to Ground
5 pF - Off channels, 100 pF - On channels

Full Scale Input Ranges
±10V, ±5V, ±2.5V, ±1.25V (supplied standard, selectable by 2-bit programmable gain code). Board pads are etched for the user to install a fixed gain resistor, providing down to ±10 mV full scale range.

Programmable Gain Amplifier
Supplied, X1, X2, X4, X8 gains (see ranges above). Fixed high gain X1000 optional (see above)

Input Impedance
100 mΩ minimum, differential or to ground (power on) 1.5 kΩ minimum (power off)

Input Source Resistance for Rated Specifications
5 K Ohms maximum (balanced)
1 K Ohms maximum (unbalanced)

Input Bias Current
30 pA typical, 200 pA maximum

Overall Accuracy at +25 °C
(Including 3-sigma noise and quantization error, dynamic response errors, referred to input, after initial calibration)

Gain	Accuracy
X1	±0.05% FSR ±1/2 LSB
X2	±0.07% FSR ±1/2 LSB
X4	±0.07% FSR ±1/2 LSB
X8	±0.07% FSR ±1/2 LSB
X100*	±0.1% FSR ±1/2 LSB
X1000*	±0.3% FSR ±1/2 LSB

*Requires rewiring diff. ampl. for fixed high gain

Common Mode Voltage Range
Within ±12V of analog common (signal plus common mode)

Common Mode Rejection
At Gain = 1

0 Hz	100 dB
100 Hz	80 dB
1 KHz	60 dB

At Gain = 8

0 Hz	120 dB
100 Hz	100 dB
1 KHz	80 dB

At Gain = 1000 (Requires rewiring dif. amp. for fixed high gain)

60 Hz	100 dB

Nonlinearity
±1/2 LSB

Differential Nonlinearity
±1/2 LSB

Resolution
12 binary bits (1 part in 4096)

Multiplexer Crosstalk from Off Channels
0.01% maximum

Sample/Hold Switch Feed Through
0.01% maximum

Sample/Hold Aperture Delay Time
100 nanoseconds, maximum

System Temperature Coefficients
Gain
±25 ppm of FSR/ °C (Gain X1)
±30 ppm of FSR/ °C (Gain X2, 4, 8)
Zero
±20 µV/ °C

A/D Conversion Period
20 microseconds

Amplifier Settling Time
(Input = ±FSR pk-pk step)
8 microseconds (HL)
110 microseconds (LL)

System Throughput Rate (High Level Inputs)
23,000 samples/seconds

A/D Digital Outputs
Offset binary (bipolar) - Supplied standard
Two's complement (bipolar)
Straight Binary (unipolar)

Output Data Format
12 bit binary group compatible to SBC-Series computers. The A/D Bit 1 (MSB) may be inverted by jumper to 2's complement coding.

ANALOG OUTPUTS (ST-732 only)

Number of Channels
2 non-isolated

Full Scale Output Voltage Ranges

0 to +5V	Jumpers may be rewired
0 to +10V	by the user or by DATEL
-5 to +5V	in OEM quantities
-10 to +10V	(Supplied Standard)

Digital Input coding

Straight binary	Jumpers may be rewired by the user or by DATEL in OEM quantities (Supplied Standard)
2's Complement	
Offset Binary	

Output Impedance
200 milliohms

Output Current
±5 mA, short circuit proof to ground

Slew Rate
10 V/µS (with no Ext. Cap. Load)

Settling Time
4 microseconds to within ±1/2 LSB of final value

Accuracy at +25 °C
±50 ppm of FSR/ °C

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CURRENT LOOP OUTPUTS
(Special Quantity order)

Full Scale Current Output Range
4 to 20 mA, unipolar. (May be rewired to other ranges by the user.)
Current Loop Load Resistance
0 to 500 Ohms
Current Loop Voltage Compliance
18 to 30V dc, unipolar, provided by the user
Accuracy at +25 °C
±50 ppm of FSR/ °C

PHYSICAL

Outline Dimensions
12W x 6.75D x 0.5H inches* (305 x 171 x 13 mm)
*Cards may be stacked adjacent if standard 0.60" spacing cages are used.
Pin-for-pin and card guide compatible to the Multibus SBC-Series computers
Weight
22 ounces (0.6 kg)
Operating Temperature Range
0 to +55 °C
Storage Temperature range
-25 to +85 °C
Relative Humidity
10% to 90%, non-condensing
Altitude
0 to 15,000 feet (4600 m)

POWER CONSUMPTION

+5V dc ±5% @ 2.5 Amps. maximum
An on-board DC/DC Power Converter operated from +5V, is provided to supply regulated ±15V for linear circuits.
Programming and Architecture Type of Interface
Memory-mapped interface (I/O mapping available)
The ST-711/732 appears to the CPU as 16 consecutive memory locations with 4 unused locations
Compatibility
Pin-for-pin and card guide compatible to the Multibus, SBC-Series computers
Compatible Software
RMX-86 Analog I/O Drivers
Data Transfer - 8 bits only
The board does not make connection to BHEN/
Address Decode
16, 20, or 24 bits

Transfer Acknowledge Delay

The ST-711/732 responds with a Transfer Acknowledge (XACK) with any Read or Write Command. The XACK may be delayed to suit different processors. 16 delay steps are jumper-selected from 50 nanoseconds to 1.5 microseconds. Standard units are set to 50 nanoseconds.

Pacer Clock

Adjustable time-base consisting of a 10-stage binary divider capable of starting A/D conversions in the External Trigger Mode. Time-base periods are jumper-selected and the oscillator may be either crystal or RC controlled. The standard range is 97 microseconds to 1 second.

Interrupts

2 of 3 possible interrupts may be jumper-selected to one or both (INTA and INTB) interrupt lines. The interrupts are EOC (End of Conversion), EOS (End of Scan), and Pacer Clock. They are factory-jumpered as: INTA - EOS, INTB - EOC. Additionally, any of the 8 Multibus interrupts may be wired to any combination of the EOC, EOS Pacer Interrupts.

Memory Base Address

The 16-location starting base address is factory set at 00F700 (hex) but may be reassigned on 16-byte boundaries (LSB = 0) by altering a supplied DIP jumper plug.

Memory Address Assignments (All addresses in hex)

New Addr.	DATEL Supplied	Command	Function
Base + 0	00F700	Write	Load Command Register
Base + 0	00F700	Read	Read Status Register
Base + 1	00F701	Write	Load PGA and Ch. Addr. Register
Base + 1	00F701	Read	Read PGA and Ch. Addr. Register
Base + 2	00F702	Write	Load Last Chan. Addr. Register
Base + 3	00F703	Write	Clear Interrupts
Base + 4	00F704	Read	Read A/D Data LO Byte
Base + 5	00F705	Read	Read A/D Data HI Byte
Base + 8	00F708	Write	DAC 0 LO Byte to Hold Register
Base + 9	00F709	Write	DAC 0 HI Byte
Base + A	00F70A	Write	DAC 1 LO Byte to Hold Register
Base + B	00F70B	Write	DAC 1 HI Byte
Base + C to Base + F	00F70C/F & 00F706/7		Don't Use Don't Use

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Clear Interrupts (WRITE BASE + 3)

Bits	Function
7,6	Not Used
5	0 = Clear EOC Interrupt
4	0 = Clear EOS Interrupt
3	0 = Clear Pacer Clock Interrupt
2,1,0	Not Used

A/D CONTROL ADDRESSES

Load Command Register (WRITE BASE + 0)

Bits	Function
7	Not Used
6	Not Used
5	1 = Enable End of Conversion (EOC) Interrupt
4	1 = Enable End of Scan (EOS) Interrupt
3	0 = Clear Board Busy Status
2	1 = Enable External Trigger, 0 = pgm start
1	1 = Enable Automatic Channel Address Increment
0	1 = Enable A/D Conversion

Read Status Register (READ BASE + 0)

Bits	Function
7 (EOC)	1 = A/D Conversion Done, 0 = Data Invalid
6	1 = Scan Done
5	1 = EOC Interrupt Enabled
4	1 = EOS Interrupt Enabled
3	1 = Board is Busy
2	1 = External Trigger Enabled
1	1 = Auto-increment Enabled
0	1 = A/D Conversion Enabled

Read/Load PGA and Start Chan. Address Register (READ/WRITE BASE + 1)

Bits	Function	
7,6	00 = Gain X1 01 = Gain X2 10 = Gain X4 11 = Gain X8	The channel address auto sequences on the EOC rising edge if command 1=1
5	Not Used	
4	1 = 2^4	
3	1 = 2^3	Start Chan. Addr. Select (1 of 32)
2	1 = 2^2	
1	1 = 2^1	
0	1 = 2^0	

Load A/D Last Channel Address (WRITE BASE + 2)

Bits	Function	
7,6,5	Not Used	
4	1 = 2^4	
3	1 = 2^3	
2	1 = 2^2	Last Chan. Addr. Select (1 of 32)
1	1 = 2^1	
0	1 = 2^0	

All registers reset to zero at power up.

D/A COMMANDS

Load Hold Register with DAC LO Byte (WRITE BASE + 8 = DAC0, WRITE BASE + A = DAC1)

Bits	Function (Write this byte first)
7	DAC Bit 9
6	DAC Bit 10
5	DAC Bit 11
4	DAC Bit 12 (LSB)
3,2,1,0	Zeros

Load HI Byte to DAC; Load Hold Reg. to DAC (WRITE BASE + 9 = DAC0, WRITE BASE + B = DAC1) Enable DAC Input Register Strobe

Bits	Function* (Write this byte second)
7	DAC Bit 1 (MSB)
6	DAC Bit 2
5	DAC Bit 3
4	DAC Bit 4
3	DAC Bit 5
2	DAC Bit 6
1	DAC Bit 7
0	DAC Bit 8

*A/D-D/A convention is to label the converter's Most Significant Bit as Number 1 (MSB). (Note that D/A addressing is mapped adjacent to A/D addressing.)

A/D DATA ADDRESSES*

Read A/D Data HI Byte (READ BASE + 5)

Bits	Function (Read this byte second)
7	ADC Bit 1 (MSB)
6	ADC Bit 2
'	'
'	'
'	'
0	ADC Bit 8

Read A/D Data LO Byte (READ BASE + 4)

Bits	Function (Read this byte first)
7	ADC Bit 9
6	ADC Bit 10
5	ADC Bit 11
4	ADC Bit 12 (LSB)
3,2,1,0	Not Used, set to zeros

*Read B + 5 starts A/D conversion if command 0 = 1. Allow adequate settling time from channel address change until A/D start. Write 01h to BASE + 0 starts an A/D conversion by software.

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INPUT RANGES

Programmable Gain	Unipolar		Bipolar		Low Level Unipolar	Low Level Bipolar
X1	0 to +5V	0 to +10V	±5V	±10V	Up to +80 mV	Up to ±1V
X2	0 to +2.5V	0 to +5V	±2.5V	±5V	Up to +40 mV	Up to ±500 mV
X4	0 to +1.25V	0 to +2.5V	±1.25V	±2.5V	Up to +20 mV	Up to ±200 mV
X8	0 to +675V	0 to +1.25V	±675V	±1.25V	Up to +10 mV	Up to ±100 mV

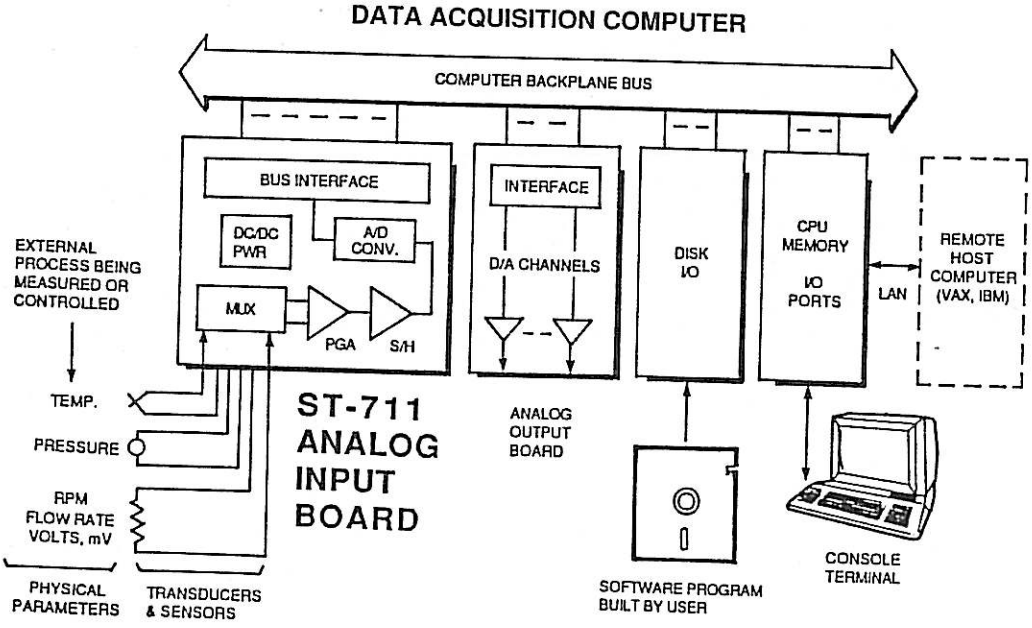
(Standard, Offset Binary)

Selected by on-board jumpers

Requires substitution by user of fixed gain resistor on the on-board differential amplifier.

Interface Connectors

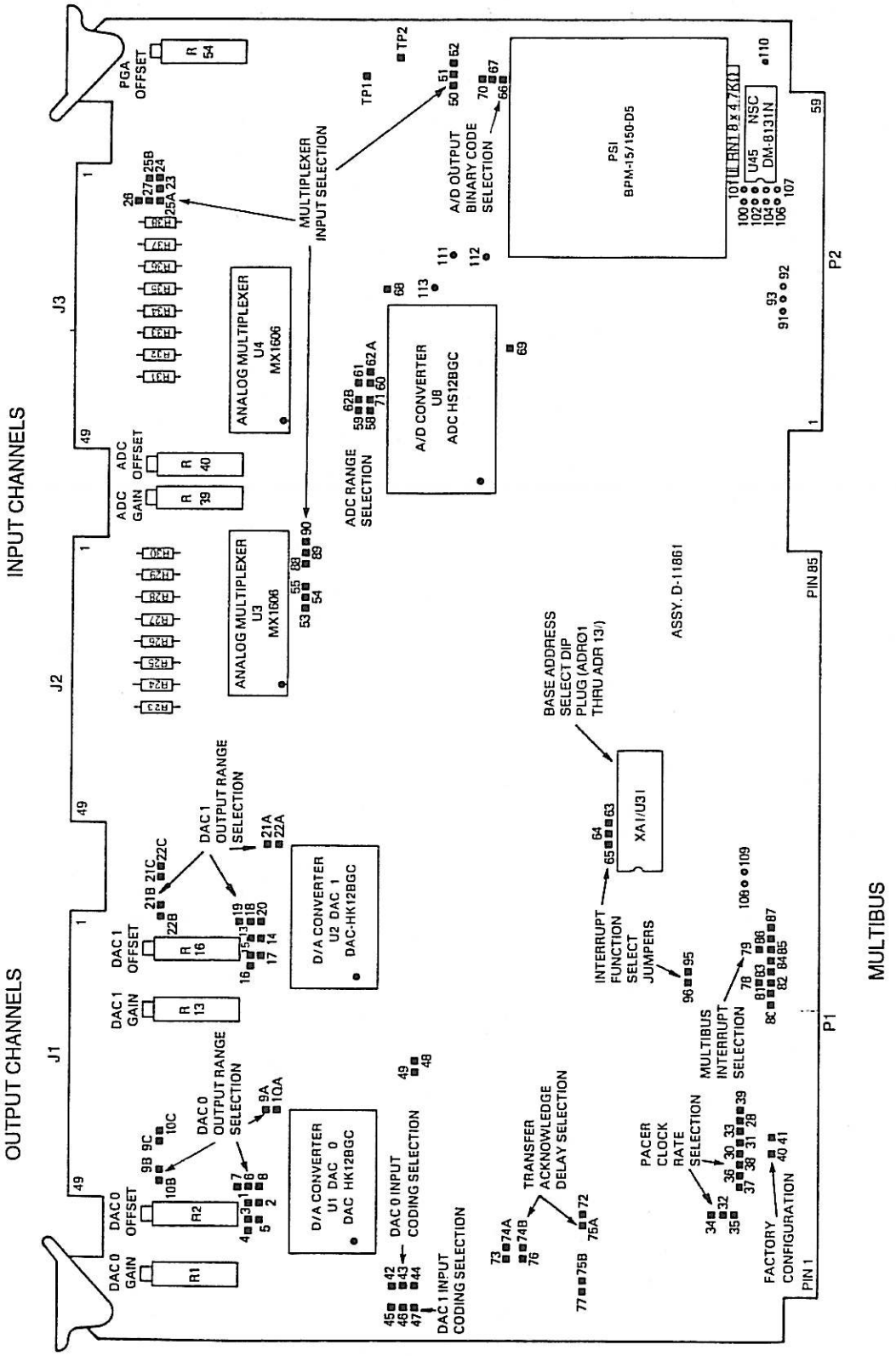
Desig.	Function	No. of Pins	Pin Spacing Centers (in)	Mating Ribbon Connectors
P1	SBC Multibus Bus Connector	86	0.156	–
P2	±15V Aux. Power (Bus)	60	0.1	–
J1	2 D/A Analog Output Channels	50	0.1	58-2076061
J2	1st 8D/16S A/D Input Channels	50	0.1	58-2076061
J3	2nd 8D/16S A/D Input Channels	50	0.1	58-2076061



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Note: Pin numbering is reversed per Intel convention.

ST-711/732 BOARD LAYOUT



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