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BU-65528 and BU-65527
Hardware Manual
MIL-STD-1553 BC/RT/MT
VME/VXI Interface Unit

MN-65527-001

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INTRODUCTION

BU-65528/BU-65527 FEATURES

- VMEbus/VXIbus COMPATIBLE INTERFACE (BU-65527 is VMEbus Compatible Only)
- UP TO 4 DUAL 1553B CHANNELS PER CARD
- 12K WORDS OF DUAL-ACCESS RAM PER CHANNEL
- 16 BIT DATA TRANSFERS, SELECTABLE 24-BIT OR 32-BIT RAM ADDRESSING
- ADVANCED COMMUNICATION ENGINE (ACE) CAPABILITIES:

BUS CONTROLLER features
- Automatic retries
- Programmable Gap times
- Frame Auto-repeat
- Programmable Response timeout

REMOTE TERMINAL features
- Programmable Command Illegalization
- Single Message, Double Buffering or Circular Buffering
- Interrupts on Individual Mode Code Commands
- BUSY bit programmable by subaddress
- Latchable RT address (BU-65528), Hardwired RT address (BU-65527)

MONITOR features
- Word Monitor
- Selective Message Monitor
- Simultaneous RT/Message Monitor
- Word-trigger Options

FUNCTIONAL OVERVIEW

The BU-65528/27 is an intelligent board interface between the MIL-STD-1553B Data Bus and a VMEbus/VXIbus system. One double Euro-card size board provides Bus Controller (BC), Remote Terminal (RT) and advanced Monitor (MT) access of up to 4 dual-redundant 1553 bus channels.

The BU-61586 Advanced Communication Engine (ACE) hybrid (BU-61585 ACE used in the BU-65527) provides complete MIL-STD-1553A, 1553B Notice 2, and STANAG 3838 (including EFAbus) protocol support, as well as 12Kx16 RAM and sophisticated control features for maximum flexibility.

The BU-65528/27 onboard logic provides interface and control of (4) dual-bus 1553 channels, appearing to the host as (4) independent devices while occupying only (1) card-cage position. Interrupts and data transfers are organized internally to reduce system overhead and simplify support-software requirements.

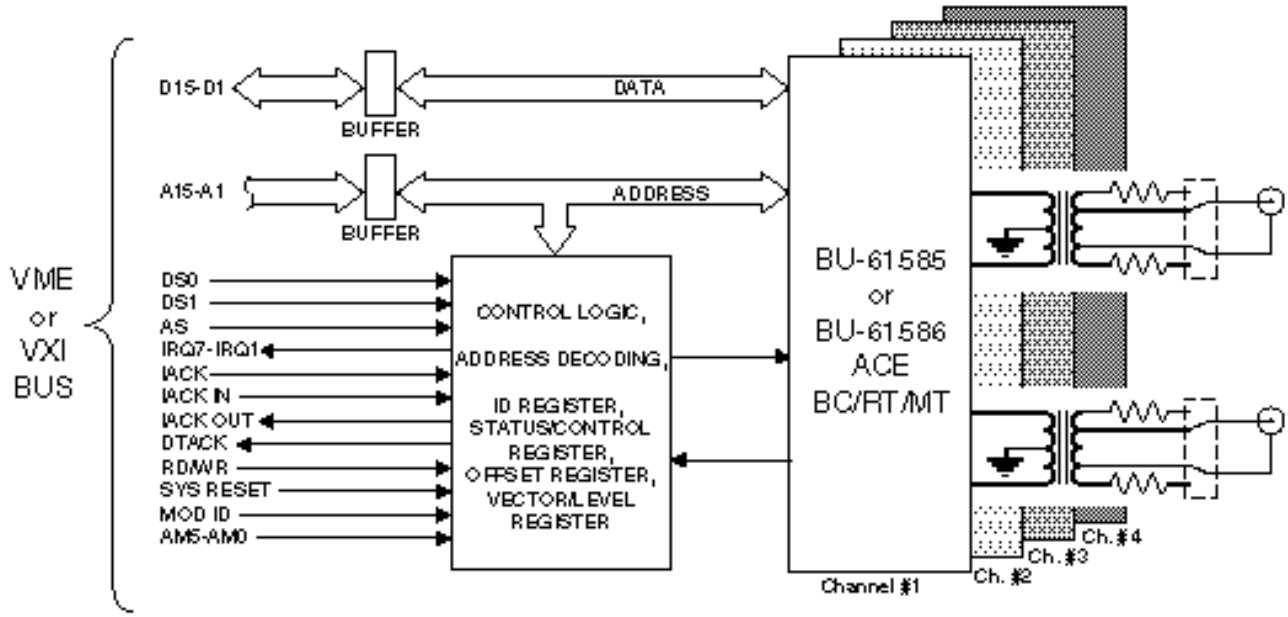


FIGURE 1. BU-65528/27 BLOCK DIAGRAM

Memory Management Architecture

A Stack Area of RAM is maintained for all three modes, providing a real-time chronology of all messages processed. In BC mode, the stack allows for the scheduling of multimessage frames. In addition to stack processing, the memory management logic performs storage, retrieval and manipulation functions involving pointer and message data structures for all three modes.

Bus Controller Architecture

One of the enhanced Bus Controller features is programmable intermessage gap time. This allows the BC intermessage gap to be programmed from a minimum of approximately 16 µs up to 65.535 ms, in increments of 1 µs.

Automatic retries may be enabled or disabled on a message-by-message basis. There are three fixed retry conditions: response timeout, format error and Status Set. The Status Set retry is programmable on an individual message basis, by means of seven masking bits in the BC Control Word. In addition, a retry may be enabled for a MIL-STD-1553A RT if the Message Error bit is set. The same masking bits are also used in defining a Status Set interrupt request. Either one or two retries may be attempted. There are six selectable retry schemes: same bus, alternate bus, same bus/same bus, same bus/alternate bus, alternate bus/same bus, and alternate bus/alternate bus.

Other BC features include automatic frame repeating with a programmable frame time, an external trigger input, programmable response timeout, interrupts for any message(s) and 1553A/B mode selection, on an individual message basis.

Remote Terminal Architecture

Memory management in the RT mode provides a number of options. In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from nonbroadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block, a double buffered configuration (two alternating Data Word blocks), or a variable-sized (128 to 8192 words) circular buffer may be allocated for data storage. In addition to helping ensure data consistency, the circular buffer feature provides a means of greatly reducing host processor overhead for bulk data transfer applications.

The double buffering mode for individual receive subaddresses serves to ensure data consistency of received data blocks. By making use of this feature, the host processor can easily access the most recent, complete received block of valid Data Words for any given subaddress.

End-of-message interrupts may be enabled either globally, following error messages, on a Tx/Rx/Bcst-subaddress and/or mode code basis, or when any particular Tx/Rx/Bcst-subaddress circular buffer reaches its lower boundary. An interrupt status register allows the host processor to determine the cause of all interrupts by means of a single READ operation.

Internal command illegalization eliminates the need for an external PROM, PLD or RAM device. The illegalization scheme allows for any subset of the 4096 possible combinations of broadcast/own address, T/R* bit, subaddress and word count/mode code to be illegalized.

The BU-65528/27 has a programmable option allowing the Busy bit to be set in the RT Status word as a function of broadcast, T/R* bit and subaddress. There is the option of requesting interrupts following messages for individual mode codes as well as for storing Data Words for the various mode codes in separate RAM locations.

Bus Monitor Architecture

Three different bus monitor modes are available: (1) a Word Monitor; (2) a Selective Message Monitor; and (3) a combined RT/Selective Message Monitor mode. The Selective Message Monitor supports message filtering, based on RT Address/T/R* bit/Subaddress, and provides separate Command Stacks and Data Stacks. The RT/Selective Monitor mode provides full RT capability for the ACE terminal's own RT address plus selective monitoring for all other RT addresses.

Similar to RT mode, the Selective Monitor Command Stack will store the Command Word, Time Tag Word, Block Status Word, and Data Block Pointer for each monitored message. Programmable size is provided for BC/RT Command Stack, Monitor Command Stack and Monitor Data Stack. The Word Monitor also provides for a programmable Trigger Word. The Trigger Word, which defines a specific Command Word, may be used to start the monitor, stop the monitor, or generate an interrupt.

Internal Time Tagging

The time tag register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 µs per LSB. The Time Tag Register may be incremented under software control, supporting self-test of the register.

For RT mode, additional options are provided to clear the Time Tag Register following a Synchronize (without data) mode command, or to load the Time Tag Register following a Synchronize (with data) mode command. Another option enables an interrupt request and a bit in the Interrupt Status Register to be set when the Time Tag Register rolls over from FFFF to 0000. Assuming the Time Tag Register is not loaded or reset, this will occur at approximately 4-second time intervals, for 64 us/LSB resolution, down to 131 ms intervals, for 2 us/LSB resolution.

Interrupts

Board-level interrupts are enabled by programming the Interrupt Request level, the Interrupt Vector word, and the interrupt condition. The Interrupt Request level and Vector word are loaded into the VECTOR/LEVEL REGISTER, and the interrupt conditions selected by the INTERRUPT MASK REGISTER.

The BU-65528/27 generates an interrupt request to the VME/VXIbus master by asserting the selected IRQ* line (LEVEL) on the system backplane and waiting for the master to respond. Upon receiving an interrupt acknowledge, the card examines the interrupt level being serviced. An equal interrupt level prompts the BU-65528/27 to place the interrupt Vector Word (or Logical address, as appropriate) on bits 7 through 0 of the system data bus and then remove the interrupt request. When Level Interrupt Mode has been selected (preferred method), further interrupts to the system are disabled until the interrupt is cleared either by an Interrupt Reset (in the START/RESET REGISTER) or by reading the INTERRUPT STATUS REGISTER (if the Interrupt Auto-clear feature is enabled).

> NOTE: It is recommended that a **level** interrupt request mode be selected via Configuration Register #2 to maintain the pending interrupt until the request has been serviced by the host.

Individual interrupts are enabled using the Interrupt Mask Register. The host processor may easily determine the cause of the interrupt through the use of the Interrupt Status Register. The Interrupt Status Register provides the current state of the interrupt conditions, and may be updated in two ways. In the standard interrupt handling mode, a particular bit in the Interrupt Status Register will be updated only if the condition exists **and** the corresponding bit in the Interrupt Mask Register is enabled. In the enhanced interrupt handling mode, a particular bit in the Interrupt Status Register will be updated if the condition exists regardless of the contents of the corresponding Interrupt Mask Register bit. The enhanced interrupt handling mode allows the host processor to define high priority conditions that will generate an interrupt, and low priority conditions that will be flagged but will not generate an interrupt.

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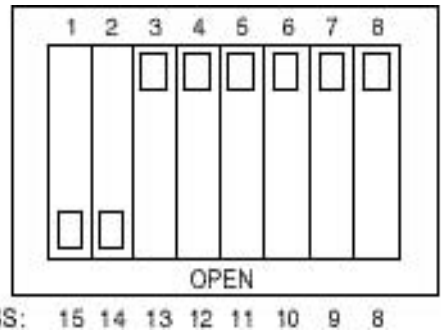
INSTALLATION

A DIP switch and a minimum number of terminal blocks simplify setup of the BU-65528/BU-65527. Non-volatile selection includes direct or transformer coupling for the 1553 bus interface, I/O register base address, and 24 or 32-bit RAM addressing. The location and factory settings of the terminal blocks and switch are shown in FIGURE 2, 3, 4. (Note: The BU-65527M does not contain user selectable terminal blocks or switches on the card).

SETUP

I/O REGISTER BASE ADDRESS SELECTION

Switch S1 (BU-65528): This DIP switch is used to program the BU-65528's 8-bit register base address. The internal registers of the BU-65528 are accessible by means of a 16-bit address ("short" or A16 address space). The switches on S1 are labeled 1 through 8. Positions 1 through 8 are used to program the logic state of the address bits 15 through 8 respectively.

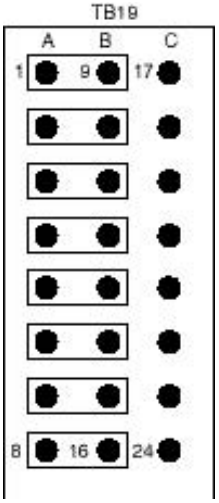


Note:
1) Placing a switch in the "ON" position will program a Logic 1.
2) Shown for the factory default setting of C000 (hex).

An open S1 switch position designates a "1" for it's corresponding register address bit, and a closed S1 switch position is a "0" for that address bit. The BU-65528 is shipped from the factory with a base register address of **1100 0000** 0000 0000 (**C0**00 Hex), with the corresponding S1 switch positions shown in FIGURE 2, 3, 4.

TB19 (BU-65527C): This Terminal Block is used to program the BU-65527C's 8-bit register base address. The internal registers of the BU-65527C are accessible by means of a 16-bit address ("short" or A16 address space). The pins on TB19 are labeled 1 through 24 with pins 1 through 8 labeled "A", pins 9 through 16 labeled "B", and pins 17 through 24 labeled "C". The positioning of the jumpers are used to program the logic state of the address bits 15 through 8, respectively. Each row represents a register base address bit as stated in the table below. For each address bit (i.e.; A15, A14,...) There are three bit settings:

- Installing a jumper from the TB19 "A" to "B" pin would enable that particular register base address bit to be programmed via the P2 connector and backplane.
- Installing a jumper from the TB19 "B" pin to "C" pin fixes that particular address bit at logic "0".
- Not installing any jumpers for a particular address bit fixes that address bit at logic "1".



Register Base Address Terminal Block TB19 Control			
TB19 Pins			**Register Base Address Bit Controlled**
A	B	C	
1	9	17	A15
2	10	18	A14
3	11	19	A13
4	12	20	A12
5	13	21	A11
6	14	22	A10
7	15	23	A9
8	16	24	A8

(Note: For the BU-65527MX card, the Register Base Address is only selectable via the P2 Connector and backplane.)

NOTE: A VXIbus system uses a logical addressing scheme to uniquely identify and organize the various devices in a system. The VXIbus Slot Zero Controller device is normally assigned a Logical Address of 0. Each VXI device's Logical Address is related to the I/O base register address, where bits 15 and 14 are both "1", and bits 13 through 8 are the device's logical address.

For the BU-65528 card, each 1553 channel is considered to be a separate VXI device. The (decimal) base register address for each individual BU-65528 **1553 channel** is defined by the equation:

Channel Base Register Address = 49152 + (V*64) where:

V = the base Logical Address of the individual 1553 channel = 4, 5, 6, 7…252 (decimal).

Note that the effective base logical address of the BU-65528 **card** = 4, 8, 12, …252 (decimal). Note that this value must be modulo 4 to accommodate a 4-channel card. Also, do **not** use a Logical Address value of 0, since this is reserved for the Slot Zero Controller.

The base address of the BU-65528 **card** is defined by the equation:

Card Base Register Address = 49152 + (C*256), where:

"C" is defined to be the upper 6 bits of the BU-65528 **card's** Logical Address, which can assume the values 1, 2, 3, ….63 (decimal). The value of "C", **which must NOT be zero**, corresponds to bits 13 through 8 of the card's I/O base address register. These six bits are specified by the setting of switch S1, positions 3 through 8 (reference Figure 2). For these switches, "OPEN" specifies a value of logic "0", while "CLOSED" specifies a value of logic "1". Since the lowest allowable base register address in a VXI system is a value of C000 (hex)

= 49152 (decimal), **this requires that switch S1 positions 1 and 2 must always be set to "OPEN" (logic "1").**

For each individual 1553 channel, the lower two bits of the logical address are defined by base register address bits 7 and 6, which designate the number of the particular 1553 channel. That is, this number assumes the value 0, 1, 2 or 3. For a 1-channel card, this value will always be 0.

NOTE: **BU-65528/27 with Multiple 1553 channels**: On the BU-65528/27X2 through BU-65528/27X4, S1 (or TB19 or the P2 Connector/backplane) selects the register base address for the first channel of these multiple-channel products. Onboard logic derives the register base address for Channel 2, 3, and 4 from the S1 or TB19 or the P2 Connector/backplane) address selected for Channel 1, with each subsequent channel's register base address at a fixed offset of 40 hex (64 bytes) from the previous channel's register base address. Thus, if Channel 1 had the default register base address of C000 hex then the Channel 2 register base address will be C000 hex + 40 hex (20 hex, word address), the Channel 3 address will be C000 hex + 80 hex (40 hex, word), and the Channel 4 address will be C000 hex + C0 hex (60 hex, word).

> The Device Logical Address for Channel 1 (noted above) can only occupy 0, 4, 8,...etc. Each additional channel used is offset by one from the previous channel, so the Logical Address of Channel 2 can be 1, 5, 9,...etc depending on the Logical Address of Channel 1. To obtain the Logical Address of Channel 3, add 1 to the Logical Address of Channel 2. To obtain the Logical Address of Channel 4, add 1 to the Logical Address of Channel 3.

A32/A24 ADDRESSING MODE SELECT

TB1 (BU-65528)/ TB2 (BU-65527C): This jumper block is used to select between A32 (VME extended) address mode and A24 (VME standard) addressing mode for the card's on-board shared RAM. Installing the jumper will select A32 (VME extended) mode . A24 (VME standard) mode will be selected when the jumper is open. (Note: BU-65527MX is factory hardwired to A24 mode addressing, call factory for A32 mode addressing.



DIRECT/TRANSFORMER COUPLING SELECTION

TB2 through TB5 (BU-65528): The choice of direct or transformer coupling is selectable by means of TB2 (for Bus A and B of the first channel), TB3 (for Bus A and B of the second channel), TB4 (for Bus A and B of the third channel), and TB5 (for Bus A and Bus B of the fourth channel).

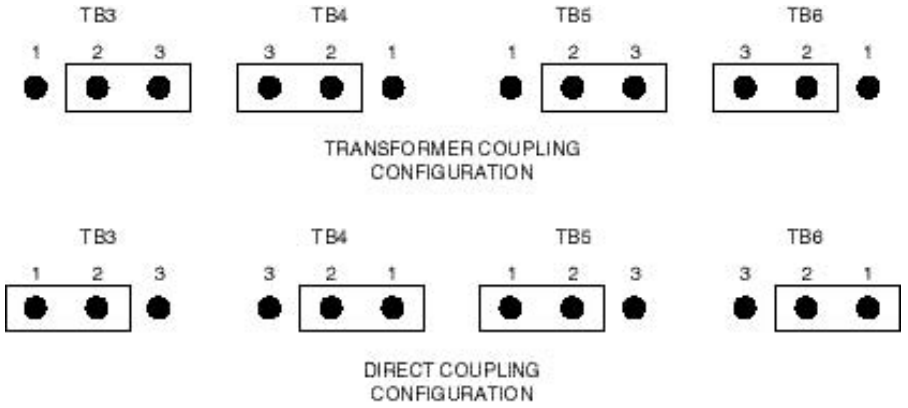
BU-65528 COUPLING TERMINAL BLOCK CONFIGURATION		

BU-65528 COUPLING TERMINAL BLOCK CONFIGURATION		
CHANNEL	TRANSFORMERS	TERMINAL BLOCKS
1	T1 and T2	TB2
2	T3 and T4	TB3
3	T5 and T6	TB4
4	T7 and T8	TB5

TB3 through TB18 (BU-65527C): The choice of direct or transformer coupling is selectable by means of TB3 thru TB6 (for Bus A and B of the first channel), TB7 thru TB10 (for Bus A and B of the second channel), TB11 thru TB14 (for Bus A and B of the third channel), and TB15 thru TB18 (for Bus A and Bus B of the fourth channel). For each channel on the board, there exists a transformer pair, or two transformers (one for each 1553 dual-redundant bus). Each of the transformers have two terminal blocks associated with it. These terminal blocks must be configured as in the figure below (figure displays terminal block setting for channel one of the four possible channels on the BU-65527C card).

BU-65527C COUPLING TERMINAL BLOCK CONFIGURATION		
CHANNEL	TRANSFORMERS	TERMINAL BLOCKS
1	T1 and T2	TB3, TB4 and TB5,TB6
2	T3 and T4	TB7, TB8 and TB9,TB10
3	T5 and T6	TB11, TB12 and TB13,TB14
4	T7 and T8	TB15, TB16 and TB17,TB18

(NOTE: For the BU-65527MX Card, transformer coupling is hardwired on the card at the factory. Call for availability non-standard direct coupling configuration).



NUMBER OF INSTALLED CHANNELS SELECT (BU-65527C Only)

TB1 (BU-65527C): The number of channels installed on the BU-65527C are configured by terminal block TB1 (Note: BU-65528/BU-65527M do not contain a user configurable terminal block for the number of channels installed on the card). The number of channels is configured at the factory and is not required to be reconfigured by the user.

NUMBER OF INSTALLED CHANNELS TERMINAL BLOCK CONFIGURATION	
CHANNELS INSTALLED	REQUIRED TERMINAL BLOCK CONNECTIONS
1	TB1-1 to TB1-2, TB1-3 to TB1-4
2	TB1-1 to TB1-2
3	TB1-3 to TB1-4
4	No TB1 Jumpers Installed

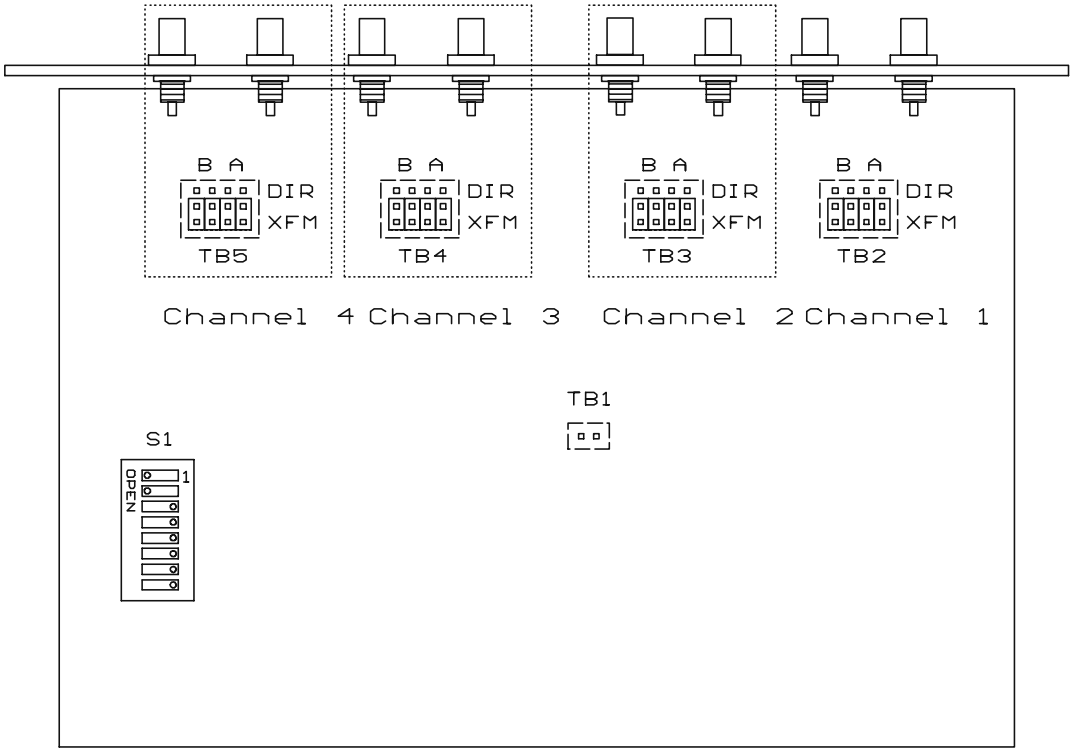


FIGURE 2. BU-65528 SETUP, SWITCH AND JUMPER LOCATIONS

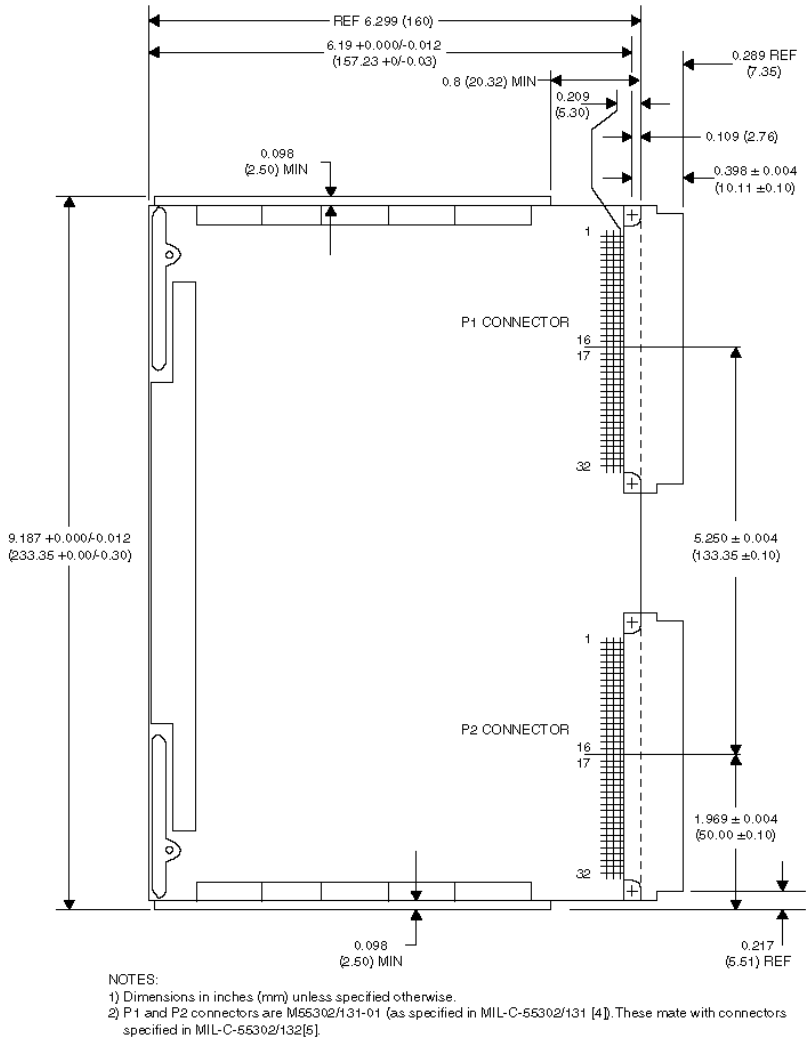


FIGURE 3. BU-65527M SETUP, SWITCH AND JUMPER LOCATIONS

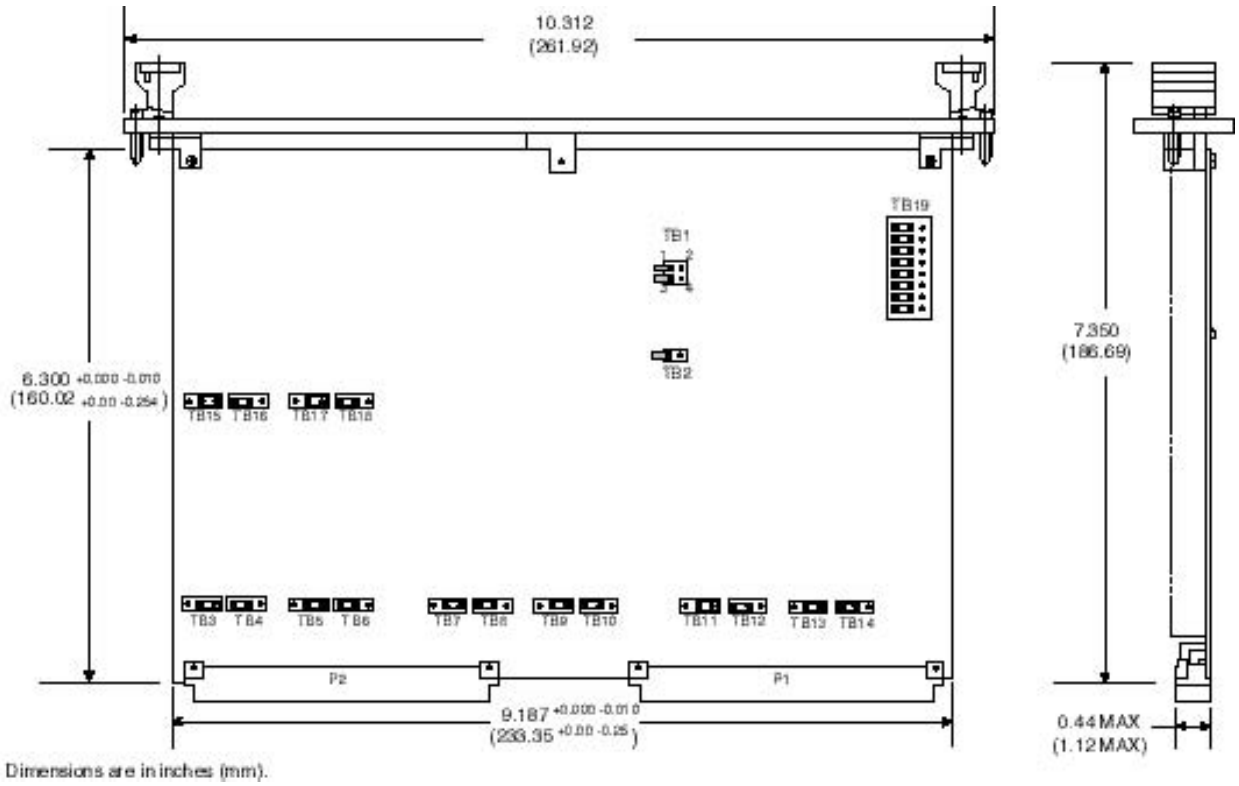


FIGURE 4. BU-65527C SETUP, SWITCH AND JUMPER LOCATIONS

INTERFACE TO MIL-STD-1553 BUS

FIGURE 5 illustrates the interface between the BU-65528/27 and a MIL-STD-1553 bus. Connections for both direct (short stub) and transformer (long stub) coupling are shown, as well as maximum cable lengths and the peak-to-peak voltage levels that appear at various points.

For both coupling configurations, the transformer on the BU-65528/27 is called the isolation transformer. For the transformer (long stub) coupled configuration, the transformer that interfaces the stub to the bus is the coupling transformer.

In accordance with MIL-STD-1553B, the turns ratio of the coupling transformer is required to be (1:1.4). For both configurations, an isolation resistor is required to be in series with each leg connecting to the 1553 bus. This protects the bus against short circuit conditions in the transformers, stubs or terminal components.

For most system applications, transformer (stub) coupling is preferred over direct coupling. Some of the advantages of transformer coupling are:

(1) Looking from the 1553 bus towards the stub, the effect of the (1.4:1) stepdown of the coupling transformer will be to **double** the impedance of the stub/terminal combination, as seen by the bus. Since the stub impedance decreases as a function of stub length due to distributed cable capacitance, this doubling effect serves to reduce the amount of impedance loading on the bus by individual terminals. For this reason, stub coupled terminals may be located up to 20 feet from the bus; the distance for direct coupled terminals is limited to 12 inches.

(2) Looking from the isolation transformer down the stub (towards the bus), the impedance seen is Z_0. Therefore, the characteristic impedance of the stub cabling (78 ohms nominal) matches the stub's load impedance, minimizing reflections back toward the transmitter.

(3) In a direct-coupled terminal, the main bus is not protected against a short circuit in the stub cabling. In the case of transformer coupling, the bus is protected against such a fault.

(4) A transformer coupled terminal provides improved DC and common mode isolation over a direct-coupled terminal.

The 1553 connectors on the front panel of the BU-65528 are either TROMPETER BJ77 or KINGS 1994-1-9 bulkhead connectors. The mating cable connectors would be TROMPETER PL75 series or equivalent. The manufacturer's catalog should be consulted for the complete part number associated with the cable type and diameter. For the BU-65527, the 1553 bus TX/RX signals are routed through the P2 connector.

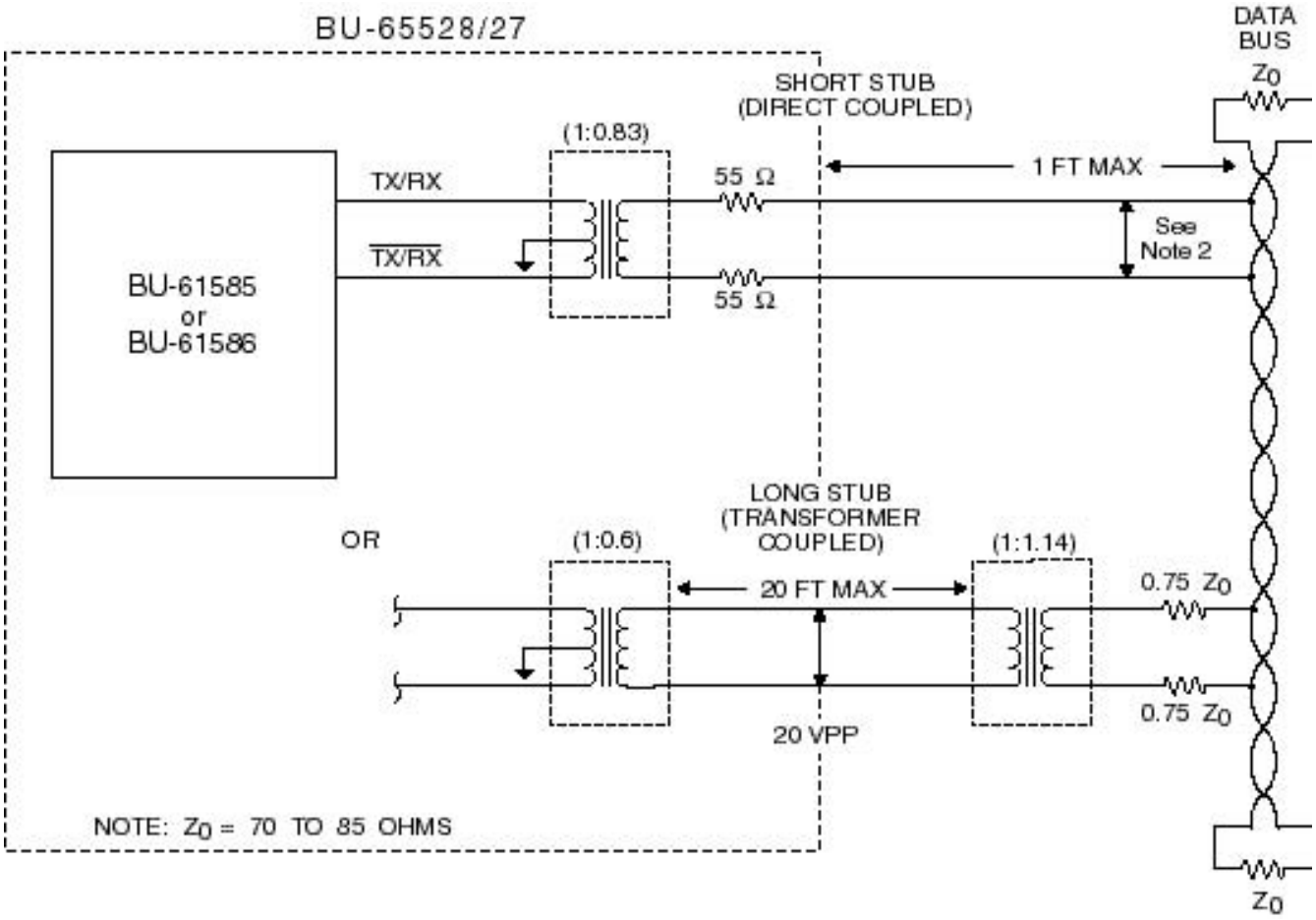


FIGURE 5. BU-65528/27 INTERFACE TO A 1553 BUS

NOTES:

(1) Shown for one of two redundant buses per channel on the BU-65528/27.

(2) Transmitted voltage level on 1553 bus is 6 V_{PP} min, 7 V_{PP} nominal, 9 V_{PP} max.

(3) Required tolerance on isolation resistors is 2%. Instantaneous power dissipation while transmitting is approximately 0.5 W (typ), 0.8 W (max).

“SIMULATED” BUS (LAB BENCH) INTERCONNECTIONS

For purposes of software development and system integration, it is generally not necessary to integrate the required couplers, terminators, etc. that comprise a complete MIL-STD-1553B bus. In most cases, a simplified electrical configuration will suffice. The interconnection methods illustrated in Figure 6 allows the BU-65528/27 to be interfaced over a "simulated bus" to simulation and test equipment. The length of this “simulated bus” should not exceed 5 feet. It is important to note that the **termination resistors indicated are necessary** (if not already present within the test/simulation equipment) in order to insure reliable communications between the BU-65528/27 and the simulation/test equipment. As illustrated in Figure 6, the 78Ω and 39Ω termination resistors should be physically located as close as possible to the test/simulation equipment.

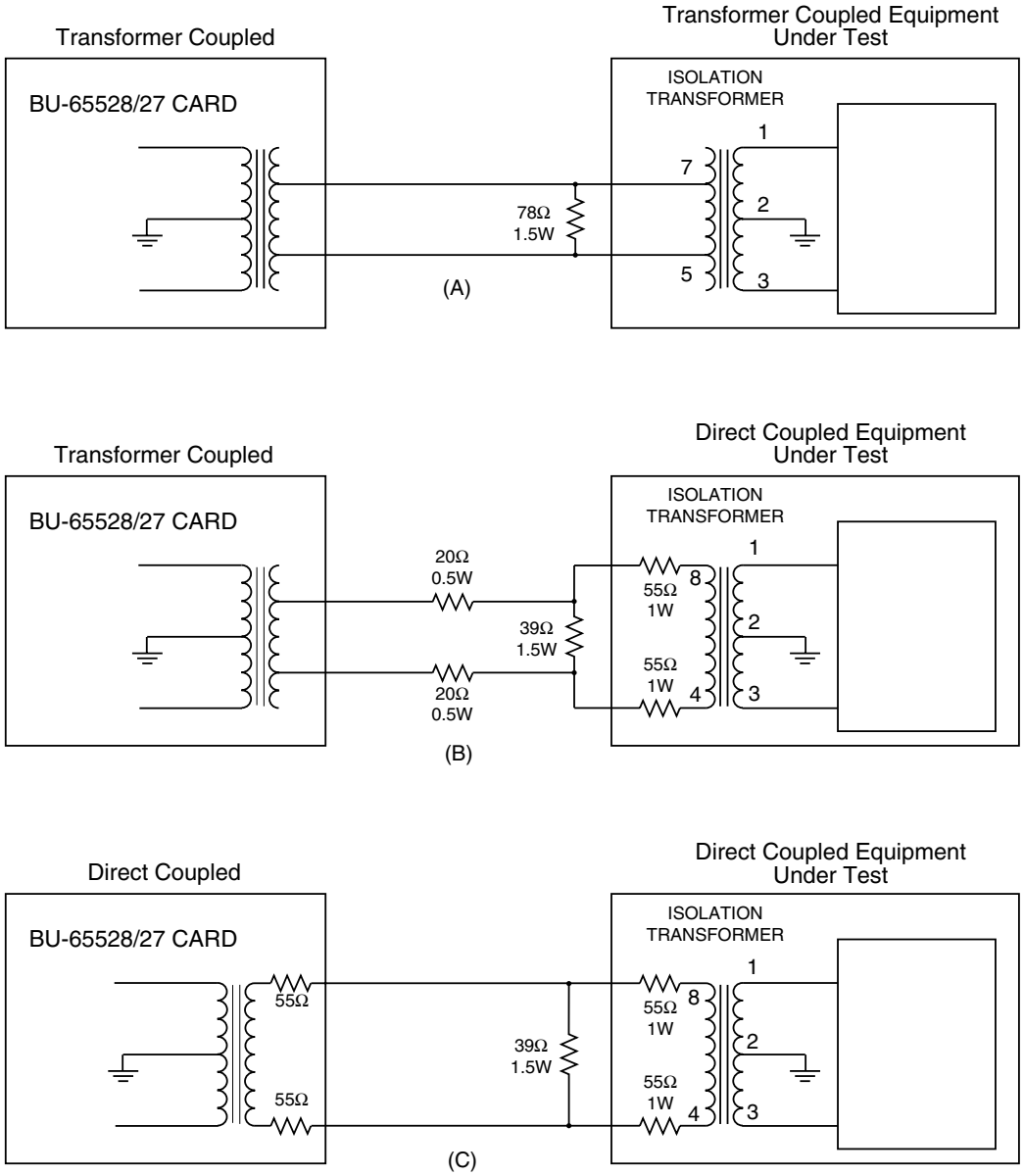


FIGURE 6. SIMULATED BUS INTERCONNECTIONS

OPERATIONAL CONSIDERATIONS

VME vs. VXI OPERATION

VXIbus (VMEbus Extensions for Instrumentation) further develops and extends the concept and capabilities of the VMEbus, with particular emphasis on support of an open instrumentation system. VXIbus stresses subsystem modularity, not only specifying hardware but also how the devices must interact within the system architecture. The VXI-defined registers provide structured information to the Resource Manager which oversees the system. The Resource Manager normally occupies the first position in the VXIbus card-cage (Slot 0). Each position of the card-cage has a MODID line connected to the P2 connector pin A30 which can be strobed by the Resource Manager to detect the presence of a device in a particular slot. The BU-65528/27 does not utilize the Module Identification line (see STATUS/CONTROL REGISTER definition).

For the BU-65528/27 user, the most significant requirement of VXI is that the interrupting device respond to an acknowledge by transferring it's 8-bit Logical Address to the Master. In addition to deriving the 16-bit Register Base address from the selected Logical Address, the Logical Address must also be loaded into the VECTOR/LEVEL REGISTER (see definition) to meet this specification.

ADDRESS MAPPING: WORDS VS. BYTES

It is important to note that with respect to the BU-65528/27, all address mapping is **word oriented**, rather than byte oriented. Although there are a few exceptions, the inherent address mapping for most standard 8-, 16-, and 32-bit microprocessors is **byte oriented**. This difference in mapping convention must be taken into account when assigning pointer values and making CPU accesses to the internal data structures (stack, lookup tables, data tables, etc.) of the BU-65528/27's shared RAM address space. That is, in terms of the CPU's memory map, the address of these data structures, relative to the base memory address, will be **double** the value of the pointer that is stored in the card's shared RAM. Thus, after reading an address of **0200 hex** in the Stack Pointer, the CPU should go to **0400 hex** to read the correct data.

ADDRESS MODIFIERS

In conjunction with the data Address bits, 6 Address Modifier lines are used by the VMEbus Master to categorize a transfer as a 16-bit, 24-bit or 32-bit address cycle. TABLE 1 lists the Address modifiers the BU-65528/27 responds to and their classification.

TABLE 1. ADDRESS MODIFIERS		
Address Mode	**MODIFIER**	**Description**
A16	29 2D	Short non-privileged access Short supervisory access
A24	39 3A 3D 3E	Standard non-privileged Data access Standard non-privileged Program access Standard supervisory Data access Standard supervisory Program access
A32	09 0A 0D 0E	Extended non-privileged Data access Extended non-privileged Program access Extended supervisory Data access Extended supervisory Program access

SOFTWARE INTERFACE: INTERNAL RAM

The software interface for each 1553 dual channel is independent of the other channels on the BU-65528/27. The register base addresses of the other channels is offset 64 bytes each from the Channel 1 Register base address selected by switch S1 (as noted in INSTALLATION Note). The Memory OFFSET ADDRESS Registers are entirely independent of each other and attention should be given to maintaining the required offset between the RAM addresses chosen for each channel (see OFFSET ADDRESS REGISTER Note).

INTERNAL REGISTERS, ADDRESS AND ACCESS

For each 1553 channel, the BU-65528 software interface to the host processor consists of 5 VXI Configuration Registers, 17 ACE internal registers for normal (non-test) operation, 8 ACE test registers, and 12K X 16 of shared memory space. All registers are 16 bits. The 64-byte register areas of a multiple-channel BU-65528/27 are contiguous. Onboard logic automatically offsets the register addresses of successive channels, based on that of Channel 1. Thus, with a Channel 1 register base byte-address of C100 hex, the first Channel 2 register would be at C140, and the first register of Channel 3 would be at C180.

The address mapping and accessibility of these registers is shown in TABLE 2, with a general register description following the table.

TABLE 2. REGISTER ADDRESS, DESCRIPTION AND READ/WRITE ACCESS

BYTE	WORD	CHANNEL 1	
0000-0001	0000	Identification Register (RD)	
0002-0003	0001	Device Type Register (RD)	
0004-0005	0002	Status/Control Register (RD/WR)	
0006-0007	0003	Offset Register (RD/WR)	
0008-0009	0004	Vector/Level Register (RD/WR)	
000A-000B	0005	Reserved	
000C-000D	0006	Reserved	**VXI**
000E-000F	0007	Reserved	**Registers**
0010-0011	0008	Interrupt Mask Register (RD/WR)	
0012-0013	0009	Configuration Register # 1 (RD/WR)	
0014-0015	000A	Configuration Register # 2 (RD/WR)	
0016-0017	000B	Start/Reset Register (WR)	
0016-0017	000B	Command Stack Pointer Register (RD)	
0018-0019	000C	BC Control Word/RT Subaddr Control Word Register (RD/WR)	
001A-001B	000D	Time Tag Register (RD/WR)	
001C-001D	000E	Interrupt Status Register (RD)	
001E-001F	000F	Configuration Register #3 (RD/WR)	
0020-0021	0010	Configuration Register #4 (RD/WR)	
0022-0023	0011	Configuration Register #5 (RD/WR)	
0024-0025	0012	RT/Monitor Data Stack Address Register (RD/WR)	
0026-0027	0013	BC Frame Time Remaining Register (RD)	
0028-0029	0014	BC Time Remaining to Next Message Register (RD)	
002A-002B	0015	BC Frame Time/RT Last Command/MT Trigger Word Register (RD/WR)	
002C-002D	0016	RT Status Word Register (RD)	
002E-002F	0017	RT BIT Word Register (RD)	
0030-0031	0018	Test Mode Register 0	
•	•	•	**ACE**
003E-003F	001F	Test Mode Register 7	**Registers**
BYTE	**WORD**	**CHANNEL 2**	
0040-0041	0020	Identification Register (RD)	
0042-0043	0021	Device Type Register (RD)	
0044-0045	0022	Status/Control Register (RD/WR)	
0046-0047	0023	Offset Register (RD/WR)	
•	•	•	
007E-007F	003F	Test Mode Register 7	
BYTE	**WORD**	**CHANNEL 3**	
0080-0081	0040	Identification Register (RD)	
0082-0083	0041	Device Type Register (RD)	
0084-0085	0042	Status/Control Register (RD/WR)	
0086-0087	0043	Offset Register (RD/WR)	
•	•	•	
00BE-00BF	005F	Test Mode Register 7	

BYTE	WORD	CHANNEL 4
00C0-00C1	0060	Identification Register (RD)
00C2-00C3	0061	Device Type Register (RD)
00C4-00C5	0062	Status/Control Register (RD/WR)
00C6-00C7	0063	Offset Register (RD/WR)
•	•	•
00FE-00FF	007F	Test Mode Register 7

The **Interrupt Mask Register** is used to enable and disable interrupt requests for various conditions.

Configuration Registers #1 and #2 are used to select the BU-65528/27's mode of operation as well as for software control of RT Status Word bits, Active Memory Area, BC Stop-on-Error, RT Memory Management mode selection, and control of the Time Tag operation.

The **Start/Reset Register** is used for "command" type functions, such as software reset, BC/MT Start as well as Interrupt Reset, Time Tag Reset, and Time Tag Register Test. The Start/Reset Register includes provisions for stopping the BC in its frame auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

The **Stack Pointer Register** allows the host CPU to determine the pointer location for the current or most recent message when the BU-65528/27 is in BC or RT modes.

The **Subaddress Control Word Register** allows the host processor access to the current or most recent Subaddress Control Word; the read/write accessibility of this register can be used as an aid for testing of the ACE hybrid.

The 16-bit **Time Tag Register** maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 us/LSB. The Time Tag Register may also be clocked by an external oscillator. The current value of the Time Tag Register is written to the Stack area of RAM during Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes.

The **Interrupt Status Register** mirrors the Interrupt Mask Register and contains a Master Interrupt bit. It allows the host processor to determine the cause of an interrupt request by means of a single READ operation.

Configuration Registers #3, **#4**, and **#5** are used to enable many of the advanced features of the BU-65528/27. These include all of the ENHANCED mode features; that is, all of the functionality beyond that of the previous generation product, the BUS-61559 series Advanced Integrated Mux Hybrid with Enhanced RT Features (AIM-HY'er). For all three modes, use of the ENHANCED Mode enables the various read-only bits in Configuration Register #1.

For BC mode, the enhanced mode features include the expanded BC Control Word and BC Block Status Word, additional STOP-ON-ERROR and STOP-ON-STATUS SET functions, frame auto-repeat,

programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message.

For RT mode, the enhanced mode features include the expanded RT Block Status Word, the combined RT/Selective Message Monitor mode, internal wrapping of the "RTFAIL*" output signal to the "RTFLAG*" input signal, double buffering for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word.

For MT mode, use of the enhanced mode enables use of both the Selective Message Monitor and the combined RT/Selective Monitor modes, as well as use of the monitor triggering capability.

The **RT/Monitor Data Stack Address Register** provides a pointer to the current address location in shared RAM used for storing Data Words in RT mode, or message words (second Command Words, Data Words, RT Status Words) in the Selective Word Monitor mode.

The **Frame Time Remaining Register** provides a read only indication of the time remaining in the current BC frame. The resolution of this register is 100 µs/LSB.

The **Message Time Remaining Register** provides a read only indication of the time remaining before the start of the next message in a BC frame. The resolution of this register is 1 µs/LSB.

The **BC Frame/RT Last Command/MT Trigger Word Register** is mode-defined.
In BC mode, it is used to program the BC frame time, for use in the FRAME AUTO-REPEAT mode. The resolution of this register is 100 µs/LSB, with a range of 6.55 seconds. In RT mode, this register stores the current (or most previous) 1553 Command Word processed by the RT. In the Monitor mode, this register is used to specify a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

The **Status Word Register** and **BIT Word Register** provide read-only indications of the BU-65528's RT Status and BIT Words.

Test Mode Registers 0-7 are used for production testing only.

IDENTIFICATION REGISTER (Register address XX00: READ only)

TABLE 3. IDENTIFICATION REGISTER	
BIT	**DESCRIPTION**
15(MSB)	DEVICE CLASS
14	DEVICE CLASS
13	CLASS ADDRESS SPACE
12	CLASS ADDRESS SPACE
11	MANUFACTURER IDENTIFICATION
•	•
•	•
•	•
0(LSB)	MANUFACTURER IDENTIFICATION

DEVICE CLASS. These two bits always read as "11", identifying the BU-65528/27 as a VXI Register-based device. (Note: Since the BU-65527X card uses the outer pin rows of the P2 Connector for device-dependent functions, it is not fully VXIbus-compliant)

ADDRESS SPACE. These two bits and the upper 4 bits of the DEVICE TYPE register are used by the VXI system Resource Manager to allocate memory to each system device, based on the addressing mode of the device. The BU-65528/27 Memory addressing mode is selected by the presence or absence of a jumper at TB1, which also affects the DEVICE TYPE register bits 15-12 and the interpretation of the OFFSET ADDRESS REGISTER.

TB1 (BU-65528) or TB2 (BU-65527C) Jumper Setting	**Addressing Mode**	**Bits 13-12**
Not Installed	A16 register, A24 Memory Access	“00"
Installed	A16 register, A32 Memory Access	“01"

(Note: The BU-65527M card is factory hardwired to A24 Addressing Mode. Contact factory for non-standard A32 Addressing Mode)

MANUFACTURER ID. This number uniquely identifies each VXIbus device manufacturer. "FE8" hex (4072 decimal) is the ID no. assigned to DDC.

DEVICE TYPE REGISTER (Register address XX02: READ only)

TABLE 4. DEVICE TYPE REGISTER	
BIT	**DESCRIPTION**
15(MSB)	REQUIRED MEMORY
14	REQUIRED MEMORY
13	REQUIRED MEMORY
12	REQUIRED MEMORY
11	MODEL CODE
•	•
•	•
•	•
0(LSB)	MODEL CODE

REQUIRED MEMORY. Contains information used by the VXI Resource Manager to determine the amount of memory on the device. These bits reflect the TB1 (BU-65528) or TB2 (BU-65527C) selection of A24 or A32 addressing mode (see IDENTIFICATION REGISTER, Address Space definition).(Note: The BU-65527M4 is hardwired for A24 addressing mode, contact factory for availability of non-standard A32 addressing mode configuration).

In A24 addressing mode, bits 15-12 read as "1000". This mode allocates 16k words of A24 address space to onboard RAM for each channel of the BU-65528/27, for a total of 64k words of memory address space required for the 4-channel BU-65528M4/BU-65527X4 model.

In A32 addressing mode, bits 15-12 read as "1111". This mode allocates 32k words of A32 address space to onboard RAM for each channel of the BU-65528/27, for a total of 128k words of memory address space required for the 4-channel BU-65528M4/BU-65527X4 model

MODEL CODE. Another source of information for the VXIbus Resource Manager's system database. These are the codes and their corresponding DDC Model numbers:

1001 1100 1111 (9CF hex) = BU-65528M1
1001 1101 1001 (9D9 hex) = BU-65528M2
1001 1110 0011 (9E3 hex) = BU-65528M3
1001 1110 1101 (9ED hex) = BU-65528M4

(Note: For BU-65527CX and BU-65527MX boards, the Device Type Register will return the same BU-65528 Model codes listed above for the BU-65528MX board)

STATUS/CONTROL REGISTER (Register address XX04: READ/WRITE)

TABLE 5. STATUS/CONTROL REGISTER	
BIT	**DESCRIPTION**
15(MSB)	A24/A32 ACTIVE/ENABLE (RD/WR)
14	MODID* (RD)
13	NOT USED
•	•
•	•
•	•
4	NOT USED
3	READY (RD)
2	PASSED (RD)
1	NOT USED
0(LSB)	RESET (WR)

A24/A32 ACTIVE/ENABLE (RD/WR). Writing a "1" at this location permits data transfers to and from the BU-65528/27 memory. A "0" here blocks access to device RAM. This bit clears to "0" on Power-up or with a RESET to bit 0 of this register, thus preventing access to the RAM.

MODID* (Read only). This bit always reads as "1", indicating to the VXI Resource Manager that the BU-65528/27 is not selectable via the Module Identification line (a pin on the P2 connector of each VXI system slot used by the Resource Manager to determine if there is a device in that slot).

READY, PASSED (Read only). These bits always read as "11". The READY and PASSED bits in this register are used in a VXI system to indicate that the device is ready to operate and that it passed self-test. The BU-65528/27 does not implement these functions.

RESET (Write only). Writing a "1" to this location:

1. Clears the STATUS/CONTROL REGISTER bit 15 to "0", blocking access to RAM;
2. Clears entire OFFSET ADDRESS REGISTER to "0";
3. Sends a MasterClear to the BU-61586 (see DDC ACE User's Guide for specific conditions produced). Note that the BU-65527CX uses the BU-61585 ACE.

OFFSET ADDRESS REGISTER (Register address XX06: READ/WRITE)

TABLE 6. OFFSET ADDRESS REGISTER		
BIT	**A24 ADDR MODE**	**A32 ADDR MODE**
15(MSB)	A23	A31
14	A22	A30
13	A21	A29
12	A20	A28
11	A19	A27
10	A18	A26
9	A17	A25
8	A16	A24
7	A15	A23
6	NOT USED	A22
5	NOT USED	A21
4	NOT USED	A20
3	NOT USED	A19
2	NOT USED	A18
1	NOT USED	A17
0(LSB)	NOT USED	A16

As noted in the descriptions of the IDENTIFICATION and DEVICE TYPE Registers, the OFFSET ADDRESS register is also affected by the TB1 (BU-65528) or TB2 (BU-65527C) selection of memory addressing mode.

In A24 standard addressing mode, OFFSET bits 15-7 correspond to device address bits 23-15. This designates a 32 K byte (16 K word) block of RAM for each channel of the card, though the BU-65528/27 actually has 24 K bytes (12 K words) of RAM per channel. The RAM will be mapped into the lower 24 K of the 32 K block, with the upper 8 K reserved.

In A32 extended addressing mode, OFFSET bits 15-0 correspond to card address bits 31-16. This mode designates a 64 K byte (32 K word) block of RAM for each channel of the card, as VXIbus specifies the minimum memory size of an A32 device to be 64 K bytes. The RAM will be mapped into the lower 24 K of the 64 K block, with the upper 40 K reserved.

Note: Care should be taken with regard to selecting the Offset Address, especially in multiple-channel cards, so that the memory address of each channel is offset by 32k bytes (if 24-bit addressing is selected) or 64K bytes (for 32-bit addressing).

VECTOR/LEVEL REGISTER (Register address XX08: READ/WRITE)

TABLE 7. VECTOR/LEVEL REGISTER	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	INT SEL2
13	INT SEL1
12	INT SEL0
11	RESERVED
10	RESERVED
9	RESERVED
8	RESERVED
7	VECTOR WORD/LOGICAL ADDRESS
•	•
•	•
•	•
0(LSB)	VECTOR WORD/LOGICAL ADDRESS

INT SEL 2-0. These 3 bits select the VME/VXI Interrupt Request line to be asserted by the BU-65528/27 when an interrupt condition occurs in the BU-65528/7.

INT SEL Bit 2/Bit 1/Bit 0	**INTERRUPT REQUEST LEVEL (IRQ* LINE ASSERTED)**
0 0 0	No interrupt request to Host
0 0 1	INTERRUPT REQUEST level 1 (IRQ1* line asserted)
0 1 0	INTERRUPT REQUEST level 2 (IRQ2* line asserted)
0 1 1	INTERRUPT REQUEST level 3 (IRQ3* line asserted)
1 0 0	INTERRUPT REQUEST level 4 (IRQ4* line asserted)
1 0 1	INTERRUPT REQUEST level 5 (IRQ5* line asserted)
1 1 0	INTERRUPT REQUEST level 6 (IRQ6* line asserted)
1 1 1	INTERRUPT REQUEST level 7 (IRQ7* line asserted)

VECTOR WORD/LOGICAL ADDRESS. This register contains the Vector word read by the Host as part of the interrupt acknowledge sequence. The Vector word is then used by the Host as the address of the interrupt handler routine. In a VXI system, these 8 bits must contain the Logical Address of the card, as selected by S1(BU-65528) or TB19(BU-65527C) on the card (see INSTALLATION). **The VXI Logical address is not automatically written** into this part of the register when the card's base register address is selected - the Logical address (see INSTALLATION Note) must be loaded into this register as part of the BU-65528/27 initialization. (Note: The BU-65527M's Logical Address is only selectable by hardwire on the P2 connector).

The bit maps and detailed definitions of the 17 ACE Hybrid operational registers are defined as follows:

INTERRUPT MASK REGISTER (Word Address XX08; RD/WR)

TABLE 8. INTERRUPT MASK REGISTER

BIT	DESCRIPTION
15(MSB)	RESERVED
14	RAM PARITY ERROR
13	BC/RT TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	RESERVED
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	BC MSG/RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

In the non-ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "0"), bits 7 through 0 of the Interrupt Mask Register are used to **both** enable interrupts for the various events/conditions **and** to enable the respective bits of the Interrupt Status Register to be set. That is, the various bits of the Interrupt Status Register will **not** become set if the corresponding bits of the Interrupt Mask Register are not set. Bits 14 through 8 are **not used** in the non-ENHANCED mode.

In the ENHANCED mode with the Enhanced Interrupts Enabled (bit 15 of Configuration Register #2 set to logic "1"), all 15 interrupts are accessible (bits 14 through 0) and the value of the Interrupt Mask Register has no effect on the operation of the Interrupt Status Register. If Enhanced Interrupts are enabled, the bits of the Interrupt Status Register **do not need to be enabled** by the corresponding bits in the Interrupt Mask Register. In the Enhanced Interrupt mode, these bits become set following the occurrence of the respective event/condition, regardless of the programming of the corresponding Interrupt Mask Register bit. In either mode, an interrupt for any of the 15 event/conditions (8 in non-ENHANCED mode) is only enabled if the respective bit of the Interrupt Mask Register (for the event/condition) has been programmed to logic "1."

An interrupt request will be issued (either a pulse or level, as determined by bit 3 of Configuration Register #2) whenever one of the interrupt request conditions occurs **and** the respective bit of the Interrupt Mask Register is set to logic "1." For a level type of request output, Interrupt Request will be cleared high after the Interrupt Status Register has been read, if bit 4 of Configuration Register #2 (INTERRUPT STATUS AUTO CLEAR) is set. Otherwise, the Interrupt Request will be reset by writing logic "1" to bit 2 (INTERRUPT RESET) of the Start/Reset Register.

The respective bits in the Interrupt Status Register will be set under either of the following two conditions:

(1) If the ACE is in its non-ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 is logic "0") **or** ENHANCED INTERRUPTS are not enabled (bit 15 of Configuration Register #2 is logic "0")) **and** the respective bit in the Interrupt Mask Register is logic "1" **and** the condition occurs.

(2) If the ACE is in its ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 is logic "1") **and** ENHANCED INTERRUPTS are enabled (bit 15 of Configuration Register #2 is logic "1") **and** the condition occurs, regardless of whether or not the respective bit in the Interrupt Mask Register is set to logic "1."

TABLE 9 summarizes the effect of the ENHANCED mode and the ENABLE INTERRUPTS bit on the operation of the Interrupt Request output (INT*) and the Interrupt Mask and Interrupt Status Registers.

TABLE 9. ENHANCED MODE INTERRUPTS

NON-ENHANCED/ ENHANCED MODE	ENHANCED INTERRUPTS ENABLED BIT (bit 15 of Configuration Register #2)	INTERRUPT REQUEST ENABLED	INTERRUPT STATUS REGISTER BIT ENABLED	ACTIVE INTERRUPT MASK AND INTERRUPT STATUS BITS
NON-ENHANCED MODE	X	If condition enabled by corresponding Interrupt Mask Register bit	If condition enabled by corresponding Interrupt Mask Register bit	7-0
ENHANCED MODE	0	If condition enabled by corresponding Interrupt Mask Register bit	If condition enabled by corresponding Interrupt Mask Register bit	7-0
ENHANCED MODE	1	If condition enabled by corresponding Interrupt Mask Register bit	Always Enabled	14-0

RAM PARITY ERROR: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1") **and** if RAM PARITY ENABLE, bit 14 of Configuration Register #2, is logic "1". Setting RAM PARITY ERROR to logic "1," enables an interrupt request to occur following a RAM parity error. Note that only the lower 8 K words of RAM contains a parity bit. Use of parity checking limits the amount of memory to 8K.

TRANSMITTER TIMEOUT: If set, enables an interrupt following a timeout of the ACE's transmitter

watchdog timer. This occurs if the ACE's encoder attempts to transmit for longer than 668 µs. This interrupt only occurs in the BC or the RT mode.

BC/RT COMMAND STACK ROLLOVER: If set, enables an interrupt following a rollover of the BC or RT stack (Command Stack 1). The size of Command Stack 1 is programmable from among 256 (64 messages), 512, 1024, and 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register #3. This interrupt only occurs in the ENHANCED mode (bit 15 of Configuration Register #3 programmed to logic "1").

MESSAGE MONITOR COMMAND STACK ROLLOVER: If set, enables an interrupt following a rollover of the Message Monitor Command Stack (Command Stack 2). This is applicable for both the Message Monitor as well as the combined RT/Message Monitor modes. The size of Command Stack 2 is programmable from among 256 (64 messages), 1024, 4096, and 16,384 words (4096 messages) by means of bits 12 and 11 of Configuration Register #3. This interrupt only occurs in the ENHANCED mode (bit 15 of Configuration Register #3 programmed to logic "1").

MONITOR DATA STACK ROLLOVER: If set, enables an interrupt following a rollover of the Word Monitor or Message Monitor Data Stack. The size of the Data Stack is programmable from among 512, 1024, 2048, 4096, 8192, 16,384, 32,768, or 65,536 words by means of bits 10, 9, and 8 of Configuration Register #3. This interrupt only occurs in the ENHANCED mode (bit 15 of Configuration Register #3 programmed to logic "1").

BC RETRY: If set, enables an interrupt following the occurrence of a retried message in BC mode. If enabled, the interrupt will occur regardless of whether the retry attempt was successful or unsuccessful.

RT ADDRESS PARITY ERROR: If set, enables an interrupt if an RT Address parity error condition is sensed. That is, if RTAD4-RTAD0 plus RTADP fail to have an odd parity sum.

TIME TAG ROLLOVER: If set, enables an interrupt if the 16-bit Time Tag Register rolls over from FFFF to 0000.

RT SUBADDRESS CIRCULAR BUFFER ROLLOVER: If this bit is set **and** the ACE is in the Enhanced Memory Management RT mode (bit 1 of Configuration Register #2 is set to logic "1") **and** the "Interrupt at Rollover" bit is set in the Subaddress Control Word for the respective Tx/Rx/Bcst subaddress, an interrupt request will be issued when the respective data lookup address pointer crosses the lower boundary of its circular buffer, resulting in a rollover. If bit 11 of Configuration Register #2 (OVERWRITE INVALID DATA) is logic "0," the RT Subaddress Circular Buffer Rollover interrupt request will be issued **immediately** after the last word at the bottom boundary of the circular buffer in the shared RAM address space (address XXXX...1111) has been read or written. If bit 11 of Configuration Register #2 is logic "1," the interrupt request will occur at the end of a transmit message or a **valid** receive message in which the

word at the bottom boundary of the circular buffer in the shared RAM address space has been read or written. For a receive message, an interrupt request will **not** be issued if bit 11 is set and there is an error in the message, even if the last word of the buffer was accessed during the message.

BC MESSAGE/RT SUBADDRESS CONTROL WORD EOM: For BC mode, if this bit is logic "1" **and** the EXPANDED BC CONTROL WORD bit (bit 12 of Configuration Register #4) is logic "1" **and** the EOM_INTERRUPT ENABLE bit (bit 4) of the respective BC Control Word is logic "1," an interrupt request will be issued at the end of the current message. For RT mode, if this bit is set **and** the ACE is in the Enhanced Memory Management RT mode **and** the "Interrupt at EOM" bit is set in the Subaddress Control Word for the respective Tx/Rx/Bcst subaddress, an interrupt will occur at the end of the current message.

BC END-OF-FRAME: If enabled, this interrupt request will be issued after an entire programmed BC message frame has been processed. That is, following the end of a message that resulted in the active area Message Count RAM location to have been incremented to FFFF (hex). Note that if BC STOP-ON-ERROR is enabled and a BC frame is aborted before the Message Count has incremented to FFFF (hex), the BC_EOM interrupt will **not** occur.

FORMAT ERROR: If enabled, will result in an interrupt request for any of the following conditions:

(1) **Loop Test Failure:** A loopback test is performed on every word transmitted by the ACE BC or RT for each message. If the received version of one or more words is decoded as invalid and/or the received version of the last transmitted word does not match the transmitted version, the loopback test is considered to have failed.

(2) **Message Error:** A Received Message contained a violation of the 1553 message validation criteria (encoding, parity, bit count, word count, etc.). For RT mode, this **does not** include an error in the received Command Word. If an invalid Command Word is detected, the entire message is ignored.

(3) **Response Timeout:** In BC or Message Monitor modes, an RT has either not responded or has responded later than the programmed value of the BC No Response Timeout time. This time is programmable for values of approximately 18.5, 22.5, 50.5, or 130 µs by means of bits 10 and 9 of Configuration Register #5. In RT mode, a response timeout occurs if the ACE is the receiving RT in an RT-to-RT transfer and the transmitting RT has not responded with its Status Word within the RT-to-RT No Response Timeout time. The RT-to-RT timeout time is programmable with the same choice of values as the BC No Response Timeout.

BC STATUS SET/RT SELECTED MODE CODE INTERRUPT/MT PATTERN TRIGGER: In BC mode, the RT Status Word received from a responding RT either contained an incorrect RT address field or one of the 8 non-RESERVED Status bits contained an unexpected bit value. The expected value for these 8 bits is normally zero (0), with one exception: If (the ACE is in its non-ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 is logic "0") **or** BROADCAST MASK ENABLE/XOR*, bit 11 of Configuration Register #4 is logic "0") **and** if the Mask Broadcast bit of the message's BC Control

Word is set, the expected value of the Broadcast Command Received bit becomes 1, rather than 0.
In RT mode, this interrupt can only occur in the ENHANCED mode (bit 15 of Configuration Register #3 is set to logic "1") **and** if Enhanced Mode Code Handling is enabled (bit 0 of Configuration Register #3 is set to logic "1"). If these two bits are set, mode code interrupts for individual broadcast-T/R bit-mode codes may be enabled by setting the appropriate bit(s) in address locations 0108-010F in the shared RAM. Reception of an enabled mode code message will then cause a mode code interrupt to occur at the end of the message.

In the Word Monitor mode, a Pattern Trigger interrupt will occur in the ENHANCED mode (bit 15 of Configuration Register #3 is set to logic "1") following the reception of a valid Command Word that matches the bit pattern programmed in the Monitor Trigger Register.

END OF MESSAGE: End of Message. If enabled, will result in an interrupt in BC, RT, and Selective Monitor modes at the completion of every message (regardless of validity).

An interrupt request will be issued (either a pulse or level, as determined by bit 3 of Configuration Register #2) whenever one of the interrupt request conditions occurs **and** the respective bit of the Interrupt Mask Register is set to logic "1." For a level type of request output, INT* will be cleared high after the Interrupt Status Register has been read, if bit 4 of Configuration Register #2 (INTERRUPT STATUS AUTO CLEAR) is set. Otherwise, the INT* level may be reset by writing logic "1" to bit 2 (INTERRUPT RESET) of the Start/Reset Register.

The respective bits in the Interrupt Status Register will be set under either of the following two conditions:

(1) If the ACE is in its non-ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 is logic "0") **or** ENHANCED INTERRUPTS are not enabled (bit 15 of Configuration Register #2 is logic "0")) **and** the respective bit in the Interrupt Mask Register is logic "1" **and** the condition occurs.

(2) If the ACE is in its ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 is logic "1") **and** ENHANCED INTERRUPTS are enabled (bit 15 of Configuration Register #2 is logic "1") **and** the condition occurs, regardless of whether or not the respective bit in the Interrupt Mask Register is set to logic "1."

CONFIGURATION REGISTER #1 (Address XX09; RD/WR)

TABLE 10. CONFIGURATION REGISTER #1

BIT	BC FUNCTION (Bits 11-0 Enhanced Mode Only) (See Note 4)	RT WITHOUT ALTERNATE STATUS (See Notes 1 and 3)	RT WITH ALTERNATE STATUS (Enhanced Mode Only and bit 5 of Cfg. Reg. #3 is logic "1") (See Notes 1 and 3)	MONITOR FUNCTION (Enhanced Mode Only, bits 12-0) (See Note 4)
15 MSB	RT/BC-MT* (Logic 0)	(Logic 1)	(Logic 1)	(Logic 0)
14	MT/BC-RT* (Logic 0)	(Logic 0)	(Logic 0)	(Logic 1)
13	CURRENT AREA B/A*	CURRENT AREA B/A*	CURRENT AREA B/A*	CURRENT AREA B/A*
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)
11	FRAME STOP-ON-ERROR	DYNAMIC BUS CONTROL ACCEPTANCE*	S10 (See Note 2)	TRIGGER ENABLED WORD
10	STATUS SET STOP-ON-MESSAGE	BUSY*	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	SERVICE REQUEST*	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	SUBSYSTEM FLAG*	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	RTFLAG* (Enhanced Mode Only)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	MESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLE/SINGLE* RETRY	NOT USED	S02	NOT USED
2	BC ENABLED (Read Only)	NOT USED	S01	MONITOR ENABLED (Read Only)
1	BC FRAME IN PROGRESS (Read Only)	NOT USED	S00	MONITOR TRIGGERED (Read Only)
0 LSB	BC MESSAGE IN PROGRESS (Read Only)	RT MESSAGE IN PROGRESS (Enhanced Mode Only) (Read Only)	RT MESSAGE IN PROGRESS (Read Only)	MONITOR ACTIVE (Read Only)

NOTES: (1) The combined RT/Message Monitor mode uses the RT WITHOUT ALTERNATE STATUS or the RT WITH ALTERNATE STATUS bit definitions **NOT** the MONITOR FUNCTION bit definitions.

(2) In the alternate RT Status Word mode, bit 10 (Message Error) may also be set for an illegalized message (Broadcast-T/R* bit-subaddress-word count/mode code).

(3) Refer to RT Status Word section in the RT operation chapter on the use of RT status word bits.

(4) Bit 7 (External Trigger Enabled)) should always be set to "0" in Enhanced BC and Enhanced MT modes.

RT/BC-MT*, MT/BC-RT*, and MMT: Selects the ACE's mode of operation as follows:

Config #1			Config #3	Mode
Bit 15	Bit 14	Bit 12	Bit 15	
0	0	X	0	Non-ENHANCED BC (See Note)
0	0	X	1	ENHANCED BC
0	1	0	X	Word Monitor
0	1	1	0	Word Monitor
0	1	1	1	Message Monitor
1	0	X	0	Non-ENHANCED RT
1	0	0	1	ENHANCED RT
1	0	1	1	Enhanced RT/ Message Monitor
1	1	X	X	Idle

NOTES: (1) Following hardware reset (MSTCLR* asserted) or software reset (by means of the Start/Reset Register), the ACE will initialize to idle (non-transmitting) **BC mode**.

(2) If the ACE is switched from RT to combined RT/Monitor mode in the middle of an RT message, the message **will be completed.**

(3) If the ACE is switched from combined RT/Monitor mode to RT mode in the middle of an RT message or Monitor message, the message **will be completed.**

(4) If the ACE is switched from either RT mode or Monitor mode to either BC mode or "Idle" mode in the middle of an RT message, the message **will be aborted.**

It should be noted that ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, must be set to logic "1", **PRIOR** to activating the ENHANCED BC or RT modes, or the Message Monitor or RT/Message Monitor modes. In addition, the ACE must be programmed for its ENHANCED mode **PRIOR** to setting bit 5 of Configuration Register #3 in order to activate RT with Alternate Status. In this instance, Configuration Register #3 must be written **TWICE**.

CURRENT AREA B/A*: Selects Current Area Pointers. Note that if bit 13 is updated during the processing of a BC frame, or while an RT or Selective Message Monitor message is in progress, the value that will be returned to the host processor will continue to be the **old** value until the BC frame or RT/MT message in progress has been completed. After the current BC frame or RT/MT message has been completed, bit 13 as read by the host CPU will toggle to its new value. If the ACE is already on-line in the Word Monitor mode, toggling this bit will have no effect. **It should be noted that Active Area selection is**

NOT related to the selection or operation of the bus channels on a dual redundant 1553 bus (Bus A vs. Bus B).

For BC mode, bits 12 through 0 are defined as follows:

MESSAGE STOP-ON-ERROR: If this bit is set, the ACE will abort the processing of messages following the end of the current message if it encounters either a word error (gap, sync, encoding, or parity error), message format error (incorrect RT Address in Status Word, high or low word count), a response timeout condition or a looptest failure.

If retries are enabled for a particular message, the retry **will** be attempted even if MESSAGE STOP-ON-ERROR is programmed to logic "1." It should be noted that the processing of subsequent BC messages in the frame **will continue** if a failed message is successfully retried.

FRAME STOP-ON-ERROR: This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This mode is invoked if bit 8 of this register, FRAME AUTO REPEAT, is programmed to logic "1." If FRAME STOP-ON-ERROR is set, the ACE will abort the processing of messages following the end of the current BC **frame** if it encounters either a word error (gap, sync, encoding, or parity error) or message format error (incorrect RT Address in Status Word, high or low word count), a response timeout condition, or a looptest failure.

If retries are enabled for a particular message, the retry **will** be attempted even if FRAME STOP-ON-ERROR is programmed to logic "1." It should be noted that the processing of subsequent BC frames **will continue** if a failed message is successfully retried.

For BC mode, bits 11 through 0 are defined in the ENHANCED BC Mode (bit 15 of Configuration Register #3 set to logic "1") as follows:

STATUS SET STOP-ON-MESSAGE: This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is set, the ACE will abort the processing of messages following the end of the current message if it encounters a "Status Set" condition in the message. A "Status Set" condition is defined as an unexpected value for one of the 8 nonreserved Status Word bits.

If bit 12 of Configuration Register #4, EXPANDED BC CONTROL WORD, is programmed to logic "0," Status Set encompasses **all 8** of the nonreserved Status Word bits. The expected value for the 8 nonreserved Status Word bits is normally zero (0), with one exception: if bit 11 of Configuration Register #4, BROADCAST MASK ENA/XOR*, is logic "0" and the MASK BROADCAST bit of the message's BC Control Word is logic "1," the expected value of the Broadcast Command Received bit becomes 1, rather than 0. If BROADCAST MASK ENA/XOR* is programmed to logic "1," the MASK BROADCAST bit of the BC Control Word is used as a mask bit, rather than performing an "XOR" operation with the Broadcast Received Status Word bit. In this instance, a Status Set condition arising from the Broadcast Command Received RT Status bit occurs when the MASK BROADCAST BC Control Word bit is logic "0" and the Broadcast Command Received RT Status Word bit is logic "1."

If EXPANDED BC CONTROL WORD is programmed to logic "1," the RT Status Word is masked by bits 14 through 9 of the BC Control Word. In this instance, the corresponding BC Control Word bit must be programmed to logic "0" in order for a "Status Set" condition to arise from the corresponding bit in the received RT Status Word. In this instance, Status Set conditions will **not** occur from Status Mask bits in the BC Control Word that are programmed to logic "1."

If a "STATUS SET" retry is enabled for a particular message, the retry **will** be attempted, even if STATUS SET STOP-ON-MESSAGE is programmed to logic "1." It should be noted that the processing of subsequent BC messages **will continue** if a message containing a STATUS SET condition is retried and the STATUS SET condition does not occur on the retry.

STATUS SET STOP-ON-FRAME: This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is set, the ACE will abort the processing of the current BC frame following the end of the frame if it encounters a "Status Set" condition in one or more messages in the frame. A "Status Set" condition is defined as described in the preceding paragraph.

If a "STATUS SET" retry is enabled for a particular message, the retry **will** be attempted, even if STATUS SET STOP-ON-MESSAGE is programmed to logic "1." It should be noted that the processing of subsequent BC frames **will continue** if a message containing a STATUS SET condition is retried and the STATUS SET condition does not occur on the retry.

FRAME AUTO-REPEAT: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is programmed to logic "0," the ACE will process its programmed BC frame one time and then halt. In this instance, the BC Stack Pointer and BC Message Count are maintained at shared RAM locations 0100 and 0101, respectively, for Area A and locations 0104 and 0105, respectively, for Area B.

If FRAME AUTO-REPEAT is programmed to logic "1," the ACE's BC frame will repeat indefinitely until either: a RESET, STOP-ON-MESSAGE, or STOP-ON-FRAME software command is invoked via the Start/Reset Register; or an enabled (MESSAGE or FRAME) STOP-ON-ERROR or STOP-ON-STATUS SET condition has occurred. In the Frame Auto-Repeat mode, just as in the "single frame" mode, the current values of the BC Stack Pointer and BC Message Count are maintained at shared RAM locations 0100 and 0101, respectively, for Area A and locations 0104 and 0105, respectively, for Area B. In addition, for the AUTO-REPEAT mode, the "initial" values which are, the values of the Stack Pointer and Message Count at the start of each frame, must also be loaded in the shared RAM to support the frame repetition: addresses 102 and 103, respectively for area A and locations 106 and 107, respectively for area B.

If the INTERNAL TRIGGER ENABLE bit of this register is set to logic "1," the BC frame will repeat with a fixed frame time as specified in the BC Frame Time Register (100 µs to 6.55 seconds).

EXTERNAL TRIGGER ENABLED: This option requires the use of an ACE Hybrid input that is not

accessible to the user. When Enhanced BC or Enhanced MT modes are selected, **this bit must be set to "0"**.

INTERNAL TRIGGER ENABLED: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit is used in conjunction with the FRAME AUTO-REPEAT bit to enable automatic frame repetition. If FRAME AUTO-REPEAT is set to logic "1" and INTERNAL TRIGGER ENABLED is set to logic "0," the ACE BC will halt the processing of messages after a single frame. **This bit configuration is not recommended**, as transmission of a single BC frame is better through use of the FRAME AUTO-REPEAT bit.

MESSAGE GAP TIMER ENABLED: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is programmed to logic "0," the ACE's intermessage gap will assume a fixed minimum value of approximately 8 to 11 µs. If this bit is programmed to logic "1," the message gap for each message will be specified by means of the third word in the respective BC message block descriptor. This time value, which specifies the time from the start of the current message to the time of the start of the subsequent message, is programmable from the minimum value (approximately 8 to 11 µs) up to 65.535 ms, in steps of 1 µs. If the programmed value of the message gap time is less than the time required to process the current message, the current message **will be processed to completion** before the subsequent message is started. In this case, the gap time between messages will assume the minimum value of approximately 8 to 11 µs.

RETRY ENABLED: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is programmed to logic "0," BC retries are disabled for **all** messages. If this bit is programmed to logic "1," automatic retry may be enabled on a message-by-message basis by setting bit 8 of the BC Control Word to logic "1" for all messages to be retried.

DOUBLE/SINGLE* RETRY: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If retries are enabled (RETRY ENABLED, bit 4 of Configuration Register #1, set to logic "1"), this bit is used to program the number of retries that will be performed (when enabled). A logic "0" will cause the ACE to perform a single retry, while a logic "1" will cause the ACE to perform up to two retries.

BC ENABLED (Read Only): This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit will return a value of logic "1" after the ACE BC has been started by means of the Start/Reset Register. This bit will continue to return a logic "1" until either: a single message frame completes, if not in FRAME AUTO-REPEAT mode; a RESET, STOP-ON-MESSAGE, or STOP-ON-FRAME software command is invoked via the Start/Reset Register; or an enabled (MESSAGE or FRAME) STOP-ON-ERROR or STOP-ON-STATUS SET condition occurs.

BC FRAME-IN-PROGRESS (Read Only): This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit will return a value of logic "1" between the time of the BC Start-of-Message (SOM) sequence for the first message of a

programmed BC frame, until the completion of the BC End-of-Message (EOM) sequence for the last programmed message of the frame. In the FRAME AUTO-REPEAT mode, BC FRAME-IN-PROGRESS will automatically return to a value of logic "1" just prior to the start of the first SOM sequence for the new frame.

BC MESSAGE-IN-PROGRESS (Read Only): This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit will return a value of logic "1" during the processing of all BC messages. This bit will transition from logic "0" to logic "1" just prior to each BC Start-of-Message (SOM) sequence and return to logic "0" following the completion of each BC End-of-Message (EOM) sequence.

For RT mode with OPTIONAL STATUS WORD ENABLE, bit 5 of Configuration Register #3, set to logic "0," the ACE's RT Status Word will comply with MIL-STD-1553B. In this mode, bits 11 through 7 and bit 0 are defined as follows:

ACCEPT DYNAMIC BUS CONTROL*: If this bit is logic "0," it enables the ACE RT to respond with the DYNAMIC BUS CONTROL ACCEPTANCE bit set in its RT Status Word in response to a Dynamic Bus Control mode code command (but **not** in response to other commands). If this register bit is logic "1," the DYNAMIC BUS CONTROL ACCEPTANCE Status Word bit will always be low.

BUSY*: If this bit is logic "0," the BUSY bit in the RT Status Word will be set (logic "1"). The ACE will not transmit any Data Words in response to a transmit command if its BUSY bit is set. If the BUSY Status Word bit is set and BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3, is programmed to logic "0," the ACE will store received Data Words in the shared RAM. However, if the BUSY bit in the RT Status Word is set and BUSY RECEIVE TRANSFER DISABLE has been programmed to logic "1," received Data Words **will not** be transferred to the ACE shared RAM.

If BUSY* is logic "1," the BUSY bit in the transmitted RT Status Word will be logic "0," unless: ENHANCED MODE is enabled (bit 15 of Configuration Register #3 is logic "1") **and** BUSY LOOKUP TABLE ENABLED (bit 13 of Configuration Register #2 is logic "1") **and** the bit corresponding to the Broadcast-T/R* bit-Subaddress fields of the current Command Word has been programmed to logic "1" in the Busy Lookup Table (address locations 0240-0247 in shared RAM).

SERVICE REQUEST*: If this bit is logic "0," the SERVICE REQUEST bit in the RT Status Word will be set. If the CLEAR SERVICE REQUEST BIT (bit 2) of Configuration Register #2 is set, the value of SERVICE REQUEST* will be automatically toggled from logic 0 to logic 1 **after** the ACE has responded to a Transmit Vector Word mode command.

SUBSYSTEM FLAG*: If this bit is logic "0," the SUBSYSTEM FLAG bit in the RT Status Word will be set.

RTFLAG*: This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If programmed to logic "0," it causes the Terminal Flag bit in the ACE's RT Status Word to be set. The Terminal Flag bit transmitted in the RT Status Word will also become set if RTFAIL-RTFLAG AUTOWRAP ENABLE, bit 2 of Configuration Register #3, is programmed to logic "1" and either a transmitter timeout (668 µs) condition had occurred **or** the ACE RT had failed its loopback test on the previous nonbroadcast message. The loopback test verifies validity (sync, encoding, bit count, parity) for the received version of every word transmitted by the ACE RT and verifies that the received version of the last transmitted word matches the transmitted version.

RT MESSAGE-IN-PROGRESS (Read Only): This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit returns a logic "1," it indicates that the ACE RT is currently processing a message. The RT MESSAGE IN PROGRESS bit is asserted to logic "1" just prior to the RT Start-of-Message (SOM) sequence, and returns to logic "0" just following the completion of the RT End-of-Message (EOM) sequence.

For RT mode with ALTERNATE STATUS WORD ENABLE, bit 5 of Configuration Register #3, set to logic "1," *all 11* bits of the ACE's RT Status Word are programmable by the host processor. The alternate Status Word may only be used in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). In this mode, bits 11 through 0 are defined as follows:

S10 through S0: For 1553A and McAir applications, direct software control over the eleven (11) lower RT Status Word bits is allowed. S10 controls the bit in bit time 9 (the first bit after the RT Address field)...S0 controls the bit in bit time 19 (LSB). Note that the logic sense of S10-S0 is the **same** (no inversion) as that of the respective transmitted RT Status Word bits. It should be noted that the Message Error Status Word bit, controlled by S10, will **also** be set if a particular command (broadcast-T/R* bit-subaddress-word count/mode code) has been illegalized.

RT MESSAGE-IN-PROGRESS (Read Only): If this bit returns a logic "1," it indicates that the ACE RT is currently processing a message. The RT-MESSAGE-IN-PROGRESS bit is asserted to logic "1" just prior to the RT Start-of-Message (SOM) sequence, and returns to logic "0" following the completion of the RT End-of-Message (EOM) sequence.

For Monitor (MT) mode with ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1," bits 11 through 0 are defined as indicated below. Note these bits have no effect in Monitor mode if ENHANCED MODE ENABLE is programmed to logic "0."

TRIGGER ENABLED: This bit must be set to logic "1" in order to activate the MT trigger logic. The

Monitor Trigger capability is applicable only for the Word Monitor mode. It is **not** applicable for the Message Monitor mode. The trigger event is a pattern match of a valid, received 1553 Command Word with the contents of the Monitor Trigger Register. The MT trigger may be used to start monitoring, stop monitoring, set a register bit, and/or result in an interrupt request.

START-ON-TRIGGER: If this bit is set, the ACE will start storing words following reception of a valid 1553 Command (or Status) Word that matches the word programmed in the Monitor Trigger Register. The word that resulted in the trigger condition will be the first word stored.

STOP-ON-TRIGGER: If this bit is set, the ACE will stop storing words following reception of a valid 1553 Command Word that matches the word programmed in the Monitor Trigger Register. The Command Word that resulted in the trigger condition will be the last word stored.

EXTERNAL TRIGGER ENABLE: This option requires the use of an ACE Hybrid input that is not accessible to the user. When Enhanced BC or Enhanced MT modes are selected, **this bit must be set to "0"**.

MONITOR ENABLED (Read Only): This bit will return a value of logic "1" whenever the ACE's monitor is in its on-line state. The ACE's MT is considered to be "on-line" after it has been started by a MT Start Command (writing a logic "1" to bit 1 of the Start/Reset Register), even if a trigger condition (if enabled) has not yet occurred.

MONITOR TRIGGERED (Read Only): This bit is applicable for the Word Monitor mode only. It is not applicable (will always return logic "0") in the Message Monitor mode. This bit reverts to logic "0" following a Word Monitor START command (writing logic "1" to bit 1 of the Start/Reset Register). This bit gets set to logic "1" after reception of a valid Command Word to the Monitor Trigger Register (bit 11). Once asserted, MONITOR TRIGGERED will remain logic "1" until either the ACE is reset or the Monitor is stopped. If the Monitor is stopped by a trigger condition (enabled by bit 9 of Configuration Register #9 set to logic "1"), MONITOR TRIGGERED will remain logic "1" until the Monitor is restarted.

MONITOR ACTIVE (Read Only): In the Word Monitor mode, this bit will return a logic "1" after the Word Monitor has been started. That is, after the Word Monitor has been started by a MT Start Command (writing a logic "1" to bit 1 of the Start/Reset Register), even if a trigger condition (if enabled) has not yet occurred. In the Message Monitor mode, MONITOR ACTIVE will return logic "1" only when the Message Monitor is currently storing the words of a selected message. MONITOR ACTIVE will return logic "0" when the monitor is in its off-line state.

CONFIGURATION REGISTER #2 (Address XX0A; RD/WR)

TABLE 11. CONFIGURATION REGISTER #2	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED INTERRUPTS
14	RAM PARITY ENABLE
13	BUSY LOOK UP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDARY DISABLE
9	TIME TAG RESOLUTION 2 (TTR2)
8	TIME TAG RESOLUTION 1 (TTR1)
7	TIME TAG RESOLUTION 0 (TTR0)
6	CLEAR TIME TAG ON SYNCHRONIZE
5	LOAD TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/PULSE* INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST
1	ENHANCED RT MEMORY MANAGEMENT
0(LSB)	SEPARATE BROADCAST DATA

ENHANCED INTERRUPTS ENABLE: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit controls the operation of the Interrupt Mask and Status Registers. If this bit is programmed to logic "0," the only interrupt conditions that may be enabled are those that are enabled by bits 7-0 in the Interrupt Mask Registers. In addition, if ENHANCED INTERRUPTS ENABLED is logic "0," the respective bit(s) in the Interrupt Status Register update **only** if the corresponding bit(s) is (are) set in the Interrupt Mask Register.

If this bit is set to logic "1" (enabled), **all 15** possible interrupt conditions may be enabled by means of bits 14-0 of the Interrupt Mask Register. In addition, if ENHANCED INTERRUPT ENABLE is logic "1," the various bits in the Interrupt Status Register may become set **regardless** of the value of the corresponding Interrupt Mask Register bits. See TABLE 10.

RAM PARITY ENABLE: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). RAM PARITY ENABLE, when set to logic "1," enables parity checking for 17-bit buffered RAM. This entails generating a 17th bit (parity bit) for ALL (both processor and 1553) RAM write accesses and parity checking for ALL RAM read accesses. If the parity check fails for any read access, an interrupt request may be issued (if enabled) and a bit set in the Interrupt Status Register.

BUSY BIT LOOKUP TABLE ENABLE: This bit is applicable only in the ENHANCED RT mode

(ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit allows the host processor to optionally set the busy bit in the RT status response, based on broadcast, and the T/R*, and subaddress fields of received Command Words. Setting this bit to logic "1" enables a lookup table in a fixed area of the RAM (hex locations 0240-0247). Placing a logic "1" in the proper bit location in the Busy table will cause the ACE RT to respond to the selected command with the BUSY bit set. Programming BUSY BIT LOOKUP TABLE ENABLE to logic "0" disables the busy bit lookup table and frees up the fixed area of RAM.

RECEIVE SUBADDRESS DOUBLE BUFFERING ENABLE: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). The receive subaddress double buffering feature supports double buffering either globally, or on a subaddress basis for individual receive (and broadcast receive) subaddresses. If RECEIVE SUBADDRESS DOUBLE BUFFERING ENABLE is programmed to a value of logic "0," the subaddress double buffering feature is disabled for **all** receive and broadcast receive subaddresses. If RECEIVE SUBADDRESS DOUBLE BUFFERING ENABLE is programmed to a value of logic "1" and ENHANCED RT MEMORY MANAGEMENT, bit 1 of this register, is programmed to logic "0," the subaddress double buffering feature will be invoked for **all** receive (and broadcast receive) subaddresses. If both ENHANCED RT MEMORY MANAGEMENT and RECEIVE SUBADDRESS DOUBLE BUFFERING ENABLE are programmed to logic "1," the subaddress double buffering feature may be invoked for individual receive (and broadcast receive) subaddresses by setting bit 15 of the respective Subaddress Control Word(s) to logic "1" and programming the appropriate "memory management" bits (MM2, MM1, MM0) to values of 000.

OVERWRITE INVALID DATA: This bit effects the operation of the RT circular buffer memory management mode. If the bit is logic 0, the ACE will update the value of the Lookup Table pointer address for the respective Tx/Rx-Bcst-subaddress following transmit messages as well as following both valid **and** invalid receive messages. In addition, if the bit is logic 0, an interrupt request for a circular buffer rollover condition (if enabled) will be issued **immediately after** the word at the lower address boundary of the respective circular buffer has been accessed. If OVERWRITE INVALID DATA is logic 1, the Lookup Table address pointer will only be updated following a transmit message or following a **valid** receive or broadcast message to the respective Rx/Bcst subaddress. If the bit is logic 1, the Lookup Table pointer **will not** be updated following an invalid receive or broadcast message. In addition, if the bit is logic 1, an interrupt request for a circular buffer rollover condition (if enabled) will occur only **following the end** of a transmit message during which the last location in the circular buffer has been read or **following the end** of a **valid** receive or broadcast message in which the last location in the circular buffer has been written to.

256-WORD BOUNDARY DISABLE: This bit controls the ACE's memory management scheme for BC message blocks and for RT data blocks for both the default (global single message) mode as well as for any individual subaddresses in the ENHANCED mode for which the "single message" or "double buffered" options are selected. If this bit is logic "0," the rollover at 256-word boundaries is enabled. That is, when the 1553 memory management logic is processing a message, its memory address will roll over from XXFF (hex) to XX00, rather than increment to (XX+1)00. If this bit is logic "1," the memory management logic will enable 256-Word boundaries to be crossed for BC Message Blocks as well as for RT Data Blocks in both the Default (bit 1 of this register = 0) and Enhanced Memory Management/Single Buffer modes. In this

instance, the address will increment from XXFF to (XX+1)00, when a 256-word boundary is encountered in the shared RAM address space. It should be noted that 256-WORD BOUNDARY DISABLE has **no effect** on the BC or RT Command Stack. That is, for the stack area of RAM in both BC and RT modes, the rollover at 256-(or 512-, 1024-, 1024-) word boundaries is **always** enforced.

It should also be noted that if 256-WORD BOUNDARY DISABLE is programmed to logic "1" in RT mode, the size for **all** circular buffers becomes **65,536 words, regardless of the programming of the respective Subaddress Control Word bits.**

It is strongly recommended that 256-WORD BOUNDARY DISABLE be programmed to logic "1" for BC mode, and to logic "0" for RT mode.

TIME TAG RESOLUTION 2,1,0: These bits allow the resolution of the time tag register to be selected by means of software control. The choices are 64 µs (default), 32 µs, 16 µs, 8 µs, 4 µs, 2 µs, and EXTERNAL CLOCK. There is also a test mode for the Time Tag register. Time Tag resolution is programmed as described in TABLE 12.

TABLE 12. TIME TAG RESOLUTION

BIT 9 TTR2	BIT 8 TTR1	BIT 7 TTR0	TIME TAG RESOLUTION
0	0	0	64 us
0	0	1	32 us
0	1	0	16 us
0	1	1	8 us
1	0	0	4 us
1	0	1	2 us
1	1	0	TEST MODE
1	1	1	INVALID

Note: In the Time Tag TEST MODE, the Time Tag Register only increments when the CPU writes a logic "1" to bit 4 of the Start/Reset Register (TIME TAG TEST CLOCK).

CLEAR TIME TAG ON SYNCHRONIZE: If this bit is set, reception of a Synchronize (without data) mode command, in RT mode, will cause the value of the internal Time Tag Register to clear to 0000.

LOAD TIME TAG ON SYNCHRONIZE: If this bit is set, reception of a Synchronize (with data) mode

command, in RT mode, will cause the Data Word from the Synchronize message to be loaded into the Time Tag Register.

INTERRUPT STATUS AUTO CLEAR: If this bit is logic "1," the value of the Interrupt Status Register will clear to 0000 **after** it has been read by the host processor. Also, if both the INTERRUPT STATUS AUTO CLEAR and LEVEL/PULSE Interrupt Request (bit 3) are logic "1," the ACE's Interrupt Request output INT* will be cleared (high) after the Interrupt Status Register has been read.

LEVEL/PULSE* INTERRUPT REQUEST: If this bit is logic "0," the BU-65528 Interrupt Request will be a pulse of approximately 500 ns width. If this register bit is logic "1," an interrupt will be requested by asserting IRQn* as a low level. If the level option is selected, the Interrupt Request will be cleared after the Interrupt Status Register has been read (provided that the INTERRUPT STATUS AUTO CLEAR [bit 4] is set), or when a "1" is written to the INTERRUPT RESET bit (bit 2) of the Start/Reset Register. The power turn-on mode for this bit is "0," enabling a pulse INT* output.

CLEAR SERVICE REQUEST: If this bit is logic "0," the Service Request RT Status word bit may controlled only by the host processor software. If the bit is logic "1," the Service Request bit may still be set and cleared under software (register) control. In addition, the SERVICE REQUEST* Configuration Register (#1) bit will automatically clear (go to logic 1) **after** the ACE RT has responded to a Transmit Vector Word mode code command. That is, if the CLEAR SERVICE REQUEST bit is set to 1 while SERVICE REQUEST* is set to 0, the ACE RT will respond with the Service Request Status bit set for all commands until the RT responds to a Transmit Vector Word command. In this instance, the ACE will respond with the Service Request **still set** in the Status Word for this message. **Following** this message, SERVICE REQUEST* in the Configuration Register automatically clears to a logic "1." It stays logic "1" (cleared) for subsequent messages until it is reasserted to a logic "0" by the host processor.

ENHANCED RT MEMORY MANAGEMENT: If this bit is logic "0," the ACE RT memory management defaults to either a **global** single Data Word buffer or double Data Word buffer for each transmit, receive, and (optionally) broadcast subaddress: single message, for all transmit subaddresses; single message, for all receive (and broadcast receive) subaddresses if RX SUBADDRESS DOUBLE BUFFER ENABLE (bit 12 of this register) is logic programmed to "0."

If ENHANCED MODE (bit 15 of Configuration Register #3 is logic "1") **and** RX SUBADDRESS DOUBLE BUFFER ENABLE are logic "1," double buffering is provided for **all** receive/broadcast subaddresses. In the single message mode, each data block is repeatedly overread or overwritten. If ENHANCED RT MEMORY MANAGEMENT is logic "1," the ACE RT memory management capability is expanded to allow for either the "single-buffer" mode, the "double buffer" (redundant mailbox) mode, or for a variable-sized circular buffer (128 to 8192 words) to be programmed on an individual basis for each transmit, receive and broadcast subaddress. Note that subaddress double buffering is applicable for receive (and broadcast) subaddresses, but **not** for transmit subaddresses.

SEPARATE BROADCAST DATA: If this bit is logic "0," the data pointers for both broadcast as well as nonbroadcast receive messages are stored in a common portion (the "receive" portion) of the RT Lookup Table. If this bit is logic "1," broadcast data is separated from nonbroadcast receive data by means of separate areas of the RT Lookup Tables provided for broadcast messages.

START/RESET REGISTER (Address XX0B; WRITE ONLY)

The Start/Reset Register is a write only register. It provides command functions for resetting the entire ACE terminal, for initiating BC or Monitor operation, for resetting the Interrupt Status Register and Interrupt Request Output and for resetting the value of the Time Tag Register. It also contains bits to facilitate testing of the Time Tag Register and to stop the ACE BC at the end of the current message or the current frame.

TABLE 13. START/RESET REGISTER

BIT	DESCRIPTION
15(MSB)	RESERVED
14	RESERVED
13	RESERVED
12	RESERVED
11	RESERVED
10	RESERVED
9	RESERVED
8	RESERVED
7	RESERVED
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0(LSB)	RESET

BC/SELECTED MT STOP-ON-MESSAGE: Writing a value of logic "1" to this bit causes the ACE to assume its off-line BC or Selected Monitor mode following the completion of the current message. If there is no message currently being processed, the ACE halts operation immediately.

BC STOP-ON-FRAME: Writing a value of logic "1" to this bit causes the ACE to assume its off-line BC mode following the completion of the current BC frame. If the ACE is currently waiting to start the next BC frame when BC STOP-ON-FRAME is written to as logic "1," the ACE will halt its BC operation immediately.

TIME TAG TEST CLOCK: When the TIME TAG RESOLUTION bits are programmed for the Time Tag Test Mode (bits 9, 8 and 7 of Configuration Register #2 are programmed to 1 1 0), writing a logic "1" to this bit will cause the value of the Time Tag register to increment by 1. In the Time Tag Test Mode, the Time Tag Register **will only** increment when a logic "1" is written to TIME TAG TEST CLOCK.

TIME TAG RESET: Writing a logic "1" to this bit causes the value of the Time Tag Register to Reset to zero (0000).

INTERRUPT RESET: Writing a "1" to this bit resets the value of the Interrupt Status Register to 0000 (except for the RT ADDRESS PARITY ERROR bit, if the condition persists). In addition, if the PULSE*/LEVEL Configuration Register bit is set to a "1," writing a "1" to this bit clears the Interrupt Request condition.

BC/MT START: When a logic "1" is written to this bit in BC mode, the ACE starts processing its programmed frame of BC messages. When a logic "1" is written to this bit in MT mode, the ACE Monitor goes on-line and starts storing received words to the shared RAM. It should be noted that an MT START command **is required** to start either the Word Monitor or the Selective Message Monitor, in the Monitor (**only**) mode. However, in the combined RT/Selective Monitor mode, an MT START command **is not** required. That is, assuming the ACE is in the ENHANCED mode, the RT and MT will go on-line **immediately** after Configuration Register #1 has been programmed for the RT/Selective Monitor mode.

RESET: This bit provides software reset capability for the ACE. When a logic "1" is written to this bit, any message in progress in BC or RT modes is immediately aborted. In Monitor mode, the ACE goes off-line **immediately** and stops storing received words. All other registers are reset to 0000 (hex); all internal states are reinitialized to their default (power turn-on) conditions.

COMMAND STACK POINTER REGISTER (Address XX0C; Read Only)

This register provides the host processor read access to the current value of the Stack Pointer in BC, RT, and Message Monitor modes.

In BC mode, the value of the Command Stack Pointer Register will be **the same** as the value of the Active Area Stack Pointer memory location.

For RT, Selective Monitor, and the combined RT/MT modes, the value read from the Stack Pointer Register will always be **four less** (modulo the command stack size) than the value read from the Active Area Stack Pointer location in the shared RAM. In RT, Selective Monitor, and combined RT/Selective Monitor modes, the value of the Stack Pointer Register is incremented by four during the Start-of-Message (SOM) sequence, from the value of the descriptor pointer for the **previous** message to the value of the descriptor pointer for the **current** message.

In the SOM sequence for the combined RT/Selective Monitor mode, the Stack Pointer Register will update to the current **RT Command Stack** pointer for RT messages, and to the **Monitor Command Stack Pointer** for Monitor messages.

In BC mode, the value of the Stack Pointer Register is incremented by four during the End-of-Message (EOM) sequence, from the descriptor pointer for the **current** message to the descriptor pointer for the **next** message.

The Stack Pointer Register is **not used** in the Word Monitor mode.

It should be noted that the BC/RT Command Stack size defaults to 256 in the non-ENHANCED mode. In the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"), the stack size is programmable for 256, 512, 1024, and 2048 words by means of bits 14 and 13 of Configuration Register #3.

TABLE 14. BC/RT COMMAND STACK POINTER REGISTER

BIT	DESCRIPTION
15(MSB)	BC/RT STACK POINTER 15
•	•
•	•
•	•
0(LSB)	BC/RT STACK POINTER 0

BC CONTROL WORD/RT SUBADDRESS CONTROL WORD REGISTER (Address XX0D; RD/WR)

As a mechanism to facilitate self-test, this register provides read/write accessibility for the current BC Control Word or RT Subaddress Control Word. While this register can **always** be read by the host CPU, it should be noted that it cannot be written by the CPU: (1) when the ACE is programmed for RT or Monitor mode, **or** (2) during the processing of a frame of messages when in BC mode. The BC CONTROL WORD/RT SUBADDRESS REGISTER **may** be written when the ACE is in "Idle" BC mode, that is, when it is programmed for BC mode (via bits 15 and 14 of Configuration Register #1) but **not** currently processing a frame of messages.

TABLE 15. BC CONTROL WORD REGISTER	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	ILLEGAL MASK (S10)
13	SERVICE REQUEST MASK (S08)
12	SUBSYS BUSY BIT MASK (S03)
11	SUBSYS FLAG BIT MASK (S02)
10	TERMINAL FLAG BIT MASK (S00)
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/B*
6	OFF LINE SELF TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-TO-RT FORMAT

TABLE 16. RT SUBADDRESS CONTROL WORD REGISTER	
BIT	**DESCRIPTION**
15(MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

TIME TAG REGISTER (Address XX0E; RD/WR)

TABLE 17. TIME TAG REGISTER	
BIT	**DESCRIPTION**
15(MSB)	TIME TAG 15
•	•
•	•
•	•
0(LSB)	TIME TAG 0

TABLE 18. TIME TAG REGISTER RESOLUTION

CONFIGURATION REGISTER #2			TIME TAG RESOLUTION	ROLLOVER TIME (MODULUS)
BIT 9 TTR2	BIT 8 TTR1	BIT 7 TTR0		
0	0	0	64 us	4.194 sec
0	0	1	32 us	2.097 sec
0	1	0	16 us	1.048 sec
0	1	1	8 us	524 ms
1	0	0	4 us	262 ms
1	0	1	2 us	131 ms
1	1	0	TEST MODE	N/A
1	1	1	INVALID	N/A

The Time Tag Register provides the output of a free-running counter. The resolution of the counter is programmable by means of bits 9, 8, and 7 of Configuration Register #2 from among 64, 32, 16, 8, 4 and 2 us/LSB. There is also a test mode in which the Time Tag register may be incremented one LSB at a time under software control for the purpose of self-test.

The Time Tag Register is reset to zero following hardware or software RESET, a TIME TAG RESET (bit 3 of the Start/Rest Register), or after the ACE has received a Synchronize (without data) mode code and bit 6 of Configuration Register #2 is logic "1." The Time Tag Register is loaded by the received Data Word following reception of a Synchronize (with data) mode code, provided that bit 5 of Configuration Register #2 is logic "1."

INTERRUPT STATUS REGISTER (Address XX0F; Read Only)

The Interrupt Status Register allows the host processor to determine the cause of an interrupt request by means of a single READ operation. There are sixteen bits in this register. This register will be cleared **after** it has been read, if the CLEAR INTERRUPT STATUS AUTO CLEAR bit (bit 4) of Configuration Register #2 is logic "1." The register will also be cleared if the host processor writes a logic "1" to the INTERRUPT RESET bit (bit 2) of the Start/Reset Register.

It should be noted that for the non-ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 programmed to logic "0"), only bits 7-0 of the Interrupt Status Register are active. In the ENHANCED MODE (bit 15 of Configuration Register #3 set to logic "1"), **and** ENHANCED INTERRUPTS enabled (bit 15 of Configuration Register logic #2 is logic "1"), all 15 bits (14-0) may become set.

It should also be noted that in the non-ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, programmed to logic "0"), bits 7 through 0 of the Interrupt Mask Register are used to **both** enable interrupts for the various events/conditions **and** to enable the respective bits of the Interrupt Status Register to be set. That is, the various bits of the Interrupt Status Register will **not** become set if the corresponding bits of the Interrupt Mask Register are not set. Bits 14-8 are not used in the non-ENHANCED mode.

The ENHANCED mode, with ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 programmed to logic "1"), supports polling (non-interrupting) applications. In this mode, the value of the Interrupt Mask Register bits has no effect on the operation of the respective Interrupt Status Register bits. If ENHANCED INTERRUPTS are enabled, the bits of the Interrupt Status Register **do not need to be enabled** by the corresponding bits in the Interrupt Mask Register. In the ENHANCED INTERRUPT mode, these bits become set following the occurrence of the respective event/condition, regardless of the status of the corresponding Interrupt Status Mask bit. In either mode, an interrupt for any of the 15 event/conditions (8 in non-ENHANCED mode) is only enabled if the respective bit of the Interrupt Mask Register (for the event/condition) has been programmed to logic "1."

TABLE 19. INTERRUPT STATUS REGISTER	
BIT	**DESCRIPTION**
15(MSB)	MASTER INTERRUPT
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	RESERVED
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

MASTER INTERRUPT: MASTER INTERRUPT will be logic "1" if any of the other 14 lower bits of the Interrupt Status Register have been programmed to logic "1."

RAM PARITY ERROR: Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") **and** ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If set to logic "1," indicates a RAM parity error.

By programming RAM PARITY ENABLE, bit 14 of Configuration Register #2 to logic "1," the ACE can be programmed to generate a single parity bit on all write accesses to 17-bit RAM. A parity check is then performed on all read accesses to the 17-bit RAM. A RAM PARITY ERROR interrupt indicates a failure of this parity check. Note that access must be limited to the lower 8 K words of RAM when parity checking is enabled.

TRANSMITTER TIMEOUT: Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") **and** ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit is set to logic "1," this indicates that the ACE's transmitter watchdog timer has timed out. This occurs if the ACE's encoder attempts to transmit for longer than 668 µs.

BC/RT COMMAND STACK ROLLOVER: Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") **and** ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit returns a value of logic "1," it

indicates a rollover of the BC/RT Command Stack. The size of the BC/RT Command Stack 1 is programmable from among 256 words (64 messages), 512, 1024, and 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register #3.

MESSAGE MONITOR COMMAND STACK ROLLOVER: Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") **and** ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit returns a value of logic "1," it indicates an interrupt following a rollover of the Message Monitor Command Stack. This is applicable for both the Message Monitor as well as the combined RT/Message Monitor modes. The size of the MT Command Stack is programmable from among 256 (64 messages), 1024, 4096, and 16,384 words (4096 messages) by means of bits 12 and 11 of Configuration Register #3.

MONITOR DATA STACK ROLLOVER: Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") **and** ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit returns a value of logic "1," it indicates a rollover of the Word Monitor or Message Monitor Data Stack. The size of the Data Stack is programmable from among 512, 1024, 2048, 4096, 8192, 16,384, 32,768, or 65,536 words by means of bits 10, 9, and 8 of Configuration Register #3.

BC RETRY: Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") **and** ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). A value of logic "1" indicates the occurrence of a retried message in BC mode. If enabled, the interrupt will occur regardless of whether the retry attempt was successful or unsuccessful. The interrupt will occur **AFTER the failed message has been retried** (either once or twice, successfully or unsuccessfully).

RT ADDRESS PARITY ERROR: Indicates that the parity sum of RTAD4-RTAD0 and RTADP is even, rather than odd, as required for the ACE to respond to messages directed to its own address in RT mode. It should be noted that if an RT ADDRESS PARITY ERROR condition occurs, the respective Interrupt Status Register bit will clear to logic "0" after the Interrupt Status Register has been read (if AUTO CLEAR is enabled) or after the INTERRUPT RESET bit in the Start/Reset Register has been written as logic "1." The RT ADDRESS PARITY ERROR bit will remain at logic "0" and will not return to logic "1" until either of the following two sequences has occurred: (1) the RT Address parity error condition goes away and then reoccurs, or (2) the RT ADDRESS PARITY ERROR bit in the Interrupt Mask Register is cleared (either by writing "0" to the register bit or by means of either a hardware or software reset to the ACE) and is then set back to logic "1," assuming that the address parity error condition persists.

TIME TAG ROLLOVER: Indicates that the 16-bit Time Tag Register has rolled over from FFFF to 0000.

RT SUBADDRESS CIRCULAR BUFFER ROLLOVER: This bit will be set at the end of a message in RT

mode, provided that the ACE is in the ENHANCED RT Memory Management mode **and** the "Interrupt at Rollover" bit is set in the Subaddress Control Word for the Tx/Rx/Bcst subaddress of the just completed message **and** the current message caused the data block Lookup Table address pointer to cross the lower boundary of the respective circular buffer, resulting in a rollover.

Note that this interrupt request will occur **immediately** when the address location at the upper boundary of a circular buffer is accessed, if OVERWRITE INVALID DATA (bit 11 of Configuration Register #2) is logic "0." If OVERWRITE INVALID DATA is logic "1," the interrupt request will occur at the end of a **valid** message in which the last location in the circular buffer was accessed. If OVERWRITE INVALID DATA is logic "1," an RT CIRCULAR BUFFER ROLLOVER **will not** occur following an invalid message.

RT SUBADDRESS CONTROL WORD EOM/BC SELECTIVE EOM: This bit will be set at the end of a message in RT mode, provided that the ACE is in the Enhanced Memory Management RT mode **and** the "Interrupt at EOM" bit is set in the Subaddress Control Word for the Tx/Rx/Bcst-subaddress of the just completed message.

This bit will also be set at the end of a message in BC mode, provided that the ACE is in the ENHANCED BC Mode **and** EXPANDED BC CONTROL WORD is enabled (bit 12 of Configuration Register #4 is logic "1") **and** the EOM INTERRUPT ENABLE bit (bit 4) in the current BC Control Word is set to logic "1."

BC END-OF-FRAME: Bus Controller End-of-Frame indicates that an entire programmed BC message frame has been completed. That is, following the end of the last message processed, the Message Count RAM location incremented to FFFF (hex). Note that if BC STOP-ON-ERROR is enabled and a BC frame is aborted before the Message Count has incremented to FFFF (hex), the BC END-OF-FRAME condition will **not** occur.

FORMAT ERROR: Indicates that a completed message, in BC, RT, or Selective Message Monitor Mode, contained one or more of the following errors:

(1) **Loop Test Failure:** A loopback test is performed on all messages transmitted by the BC or RT (except broadcast messages in RT mode). The received version of all transmitted words is checked for validity and correct sync type. In addition, a 16-bit comparison is performed on the last word transmitted by the BUS-65180 BC or RT. If **any** of these checks or comparisons do not verify, the loopback test is considered to have failed.

(2) **Message Error:** A received message contained a violation of the 1553 message validation criteria (encoding, parity, bit count, word count, etc.).

(3) **Response Timeout:** In BC mode, an RT has either not responded, or has responded later than the programmed value of the BC No Response Timeout time. In RT mode, if the ACE is the receiving RT in an RT-to-RT transfer and the transmitting RT has not responded with its Status Word within the programmed value of the RT-to-RT Response Timeout time after the Transmit Command Word.

BC STATUS SET/RT SELECTED MODE CODE INTERRUPT/MT PATTERN TRIGGER: In BC mode, the RT Status Word received from a responding RT either contained an incorrect RT address field or one of

the 8 non-RESERVED Status bits contained an unexpected bit value. The expected value for these 8 bits is normally zero (0), with one exception: If BROADCAST MASK ENABLED/XOR* (bit 11 of Configuration Register #4) is logic "0" **and** the MASK BROADCAST bit (bit 5) of the message's BC Control Word is logic "1," the expected value of the Broadcast Command Received bit becomes "1," rather than "0."

In RT mode, this interrupt can only occur in the ENHANCED mode (bit 15 of Configuration Register #3 is set to logic "1") and if Enhanced Mode Code Handling is enabled (bit 0 of Configuration Register #3 is set to logic "1"). If these two bits are set, mode code interrupts for individual broadcast-T/R bit-mode codes may be enabled by setting the appropriate bit(s) in address locations 0108-010F in the shared RAM. Reception of an enabled mode code message will then cause a MODE CODE interrupt to occur at the end of the message.

In the Word Monitor mode, a Pattern Trigger interrupt will occur in the ENHANCED mode (bit 15 of Configuration Register #3 is set to logic "1") following the reception of a valid Command Word that matches the bit pattern programmed in the Monitor Trigger Register.

END OF MESSAGE: End of Message. In BC, RT, or Selective Message Monitor mode, indicates the completion of a message (regardless of validity).

CONFIGURATION REGISTER #3 (Address XX0F; RD/WR)

TABLE 20. CONFIGURATION REGISTER #3

BIT	DESCRIPTION
15(MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/R* ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER ENABLE
2	RTFAIL*/RTFLAG* WRAP ENABLE
1	1553A MODE CODES ENABLE
0(LSB)	ENHANCED MODE CODE HANDLING

ENHANCED MODE ENABLE: If this bit in programmed to logic "0," the functionality of the ACE

defaults to that of DDC's previous generation processor-to-hybrid, the BUS-61559 Advanced Integrated Mux Hybrid with ENHANCED RT Features (AIM-HY'er). Programming this bit to logic "1" allows many of the ACE's advanced features to be enabled by means of the Interrupt Mask Register, the various Configuration Registers, as well as by the BC Control Word and RT Subaddress Control Word. These features include **all** of the functions enabled by the various bits of Configuration Registers #3, 4, and 5. If ENHANCED MODE ENABLE is programmed to logic "0," the operation of these register functions defaults to that indicated by their "logic "0"" state.

It should be noted that in order to enable any of the ENHANCED features, ENHANCED MODE ENABLED must be set to logic "1" PRIOR TO setting any of the other Configuration Register bits to enable the ENHANCED features. THIS INCLUDES ANY OF THE FEATURES ENABLED BY THE LOWER 15 bits (14-0) OF CONFIGURATION REGISTER #3, as well as features enabled by other registers. Specifically, bit 15 must first be set by writing 8000 (hex) to Configuration Register #3 BEFORE proceeding to set any of bits 14-0. When these bits are set, ENHANCED MODE ENABLE must continue to be programmed to logic "1."

In the non-ENHANCED mode, functions activated by the following register bits are active:

- Interrupt Mask Register and Interrupt Status Register, bits 7-0
- Configuration Register #1: for BC mode, bits 15-12; for RT mode (without Alternate Status only), bits 15-13 and 11-8; for Word Monitor mode, bits 15-13
- Configuration Register #2, bits 11-0
- Start/Reset Register, bits 4-0
- BC/RT Command Stack Pointer
- RT Subaddress Control Word Register
- Time Tag Register
- Interrupt Status Register bits 15 and 7-0

In the ENHANCED mode, in addition to all of the non-ENHANCED mode functions, those enabled by the following registers (or register bits) may also be activated:

- Interrupt Mask Register and Interrupt Status Register, bits 14-8
- Configuration Register #1: BC mode, bits 11-0; RT mode, bits 12 and 7-0, and the RT With Alternate Status mode; Monitor, bits 12-9, 7, 2-0; and the Message Monitor and RT/Message

Monitor modes

- Configuration Register #2, bits 15-12
- Start/Reset Register, bits 6 and 5
- BC Control Word Register *****
- Configuration Registers #3, #4, and #5
- RT/Monitor Data Stack Address Register *****
- BC Frame Time Remaining Register *****
- BC Time to Next Message Remaining Register *****
- BC Frame Time ***** /RT Last Command/Monitor Trigger Word ***** Register
- RT Status Word Register
- RT BIT Word Register
- Test Mode Registers 0-7

For all three modes, use of the ENHANCED Mode enables the various read-only bits (bits 2-0) in Configuration Register #1.

The ACE must be in the ENHANCED mode in order to enable ENHANCED INTERRUPTS (by setting bit 15 of Configuration Register #2 to logic "1").

For BC mode, the features that require ENHANCED MODE ENABLE programmed to logic "1" include the expanded BC Control Word and BC Block Status Word, additional STOP-ON-ERROR and STOP-ON-STATUS SET functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message.

For RT mode, the features that require ENHANCED MODE ENABLE programmed to logic "1" include the expanded RT Block Status Word, the combined RT/Selective Message Monitor mode, internal wrapping of the "RTFAIL*" output signal to the "RTFLAG*" input signal, the double buffering scheme for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word, and the busy bit lookup table option.

For MT mode, use of the ENHANCED Mode enables use of both the Selective Message Monitor and the combined RT/Selective Monitor modes, as well as use of the monitor triggering capability.

BC/RT COMMAND STACK SIZE 1,0: These two bits select the size of the BC/RT Command Stack. The default value for both bits is logic "0," which specifies a stack size of 256 words (64 messages). TABLE 21 illustrates the BC/RT Command Stack Sizes.

TABLE 21. BC/RT COMMAND STACK SIZE

BIT 14 BC/RT CMD STACK SIZE 1	BIT 13 BC/RT CMD STACK SIZE 0	BC/RT STACK SIZE (WORDS)
0	0	256 (64 messages)*
0	1	512 (128 messages)
1	0	1024 (256 messages)
1	1	2048 (512 messages)

*Note: default size is 256 words (64 messages)

MONITOR COMMAND STACK SIZE 1,0: These two bits select the size of the Monitor Command Stack. The default value for these two bits is logic "00," which specifies a stack size of 256 words. TABLE 22 illustrates the MT Command Stack Sizes.

TABLE 22. MONITOR COMMAND STACK SIZE

BIT 12 MT CMD STACK SIZE 1	BIT 11 MT CMD STACK SIZE 0	MONITOR STACK SIZE (WORDS)
0	0	256 (64 messages)*
0	1	1024 (256 messages)
1	0	4096 (1024 messages)
1	1	16384 (4096 messages)

*Note: default size is 256 words (64 messages)

MONITOR DATA STACK SIZE 2,1,0: These three bits select the size of the Monitor Data Stack. This stack is used in both the Word Monitor and Message Monitor modes. The default value for these three bits is logic "000," which specifies a stack size of 65,536 words. TABLE 23 illustrates the MT Data Stack Sizes.

TABLE 23. MT DATA STACK SIZE

BIT 10 MT DATA STACK SIZE 2	BIT 9 MT DATA STACK SIZE 1	BIT 8 MT DATA STACK SIZE 0	MONITOR DATA STACK SIZE (WORDS)
0	0	0	65,536 (default)
0	0	1	32,768
0	1	0	16,384
0	1	1	8,192
1	0	0	4,096
1	0	1	2,048
1	1	0	1,024
1	1	1	512

ILLEGALIZATION DISABLED: For RT mode. If this bit is programmed to logic "0," the ACE's internal RT Command illegalization feature is **enabled.** That is, shared RAM address locations 0300 to 03FF (hex) are dedicated to the illegalization function. If this bit is programmed to logic "1," the illegalization function is disabled. In this configuration, addresses 0300 through 03FF may be used for the storage of Stack or message data. This bit has no effect for BC or MT modes.

OVERRIDE MODE CODE T/R* BIT ERROR: For RT mode. If this bit is programmed to logic "0," a mode code Command Word with a T/R* bit of logic "0" and an MSB of the mode code field of "0" (receive mode codes 0 to 15) is considered an undefined Command Word. In this configuration, the ACE RT will not respond to such a command and the ACE RT's Message Error bit will be set. If this bit is programmed to logic "1," a mode code Command Word with a T/R* bit of 0 and an MSB of the mode code field of 0 will be considered a defined (reserved) mode Command Word. In this configuration, the ACE **will respond** to such a command and the Message Error bit **will not** become set.

ALTERNATE RT STATUS WORD ENABLED: For RT mode. If this bit is programmed to logic "0," only the Dynamic Bus Control Acceptance, Busy, Service Request, Subsystem Flag, and Terminal Flag RT Status Word bits are under control of the host processor, via bits 11 through 7 of Configuration Register #1. If this bit is programmed to logic "1," **all 11** RT Status Word bits are under control of the host processor, via bits 11 through 1 of Configuration Register #1.

ILLEGAL RECEIVE TRANSFER DISABLE: If this bit is programmed to logic "0" (default) and the ACE receives a receive command that has been illegalized, the ACE **WILL** store the received Data Words to the shared RAM. If this bit is programmed to logic "1" and the ACE receives a receive command that has been illegalized, the ACE **WILL NOT** store the received Data Words to the shared RAM.

BUSY RECEIVE TRANSFER DISABLE: If this bit is programmed to logic "0" (default), **and** the host processor has programmed BUSY* (bit 10 of Configuration Register #1 is logic "0") **or** the particular Command Word (broadcast, T/R* bit, subaddress) has been programmed to be busy by means of the Busy lookup table **and** the ACE RT receives a receive command, the ACE will respond with its Status Word with the BUSY bit set and

If this bit is programmed to logic "1," the host processor has programmed BUSY* to logic "0" **or** the particular Command Word (broadcast, T/R* bit, subaddress) has been programmed to be busy by means of the Busy lookup table **and** the ACE receives a receive command, the ACE will respond with its Status Word with the BUSY bit set and **WILL NOT** store the received Data Words to the shared RAM.

RTFAIL*/RTFLAG* WRAP ENABLE: Affects RT mode only. If this bit is programmed to logic "0" (default), the RTFLAG Status bit is controlled entirely by the host processor, via Configuration Register #1. If this bit is programmed to logic "1," the Terminal Flag Status Word bit will also become set if either a transmitter timeout (668 µs) condition had occurred or the ACE RT had failed its loopback test for the **previous** nonbroadcast message. The loopback test is performed on all nonbroadcast messages processed by the ACE RT. The received version of all transmitted words is checked for validity (sync and data encoding, bit count, parity) and correct sync type. In addition, a 16-bit comparison is performed on the received version of the last word transmitted by the ACE RT. If **any** of these checks or comparisons do not verify, the loopback test is considered to have failed.

1553A MODE CODES ENABLED: Affects both RT and Message Monitor modes. If this bit is programmed to logic "0" (default), the ACE considers both subaddresses 0 and 31 to be mode code subaddresses. In this configuration, the ACE RT recognizes and responds to all MIL-STD-1553B mode codes, including those with or without, Data Words. In addition, if this bit is logic "0," the ACE **will** decode for the MIL-STD-1553B "Transmit Status" and "Transmit Last Command" mode codes and **will not** update its internal RT Status Word Register as a result of these commands, with the exception of setting the Message Error bit if the command is illegalized.

If this bit is programmed to logic "1," the ACE RT or Message Monitor considers only subaddress 0 to be a mode code subaddress. Subaddress 31 is treated as a standard nonmode code subaddress. In this configuration, the ACE will consider valid and respond only to mode code commands containing **no** Data Words. In this configuration, the ACE RT will consider all mode commands followed by Data Words to be invalid and will not respond. In addition, if this bit is logic "1," the ACE will **not** decode for the MIL-STD-1553B "Transmit Status" and "Transmit Last Command" mode codes. As a result, the internal RT Status Word Register **will be updated** as a result of these commands.

ENHANCED MODE CODE HANDLING: Affects RT mode. If this bit is logic "0" (default), there is no capability to request interrupts to indicate the reception of specific mode code commands. If the bit is logic "0," mode code interrupts may be still enabled **globally** for transmit and/or receive mode codes, for subaddresses 0 and/or 31. In addition, if ENHANCED MODE CODE HANDLING is logic "0," the Data Words for individual mode codes are all mapped to the **same** address locations in the shared RAM, for

transmit and receive (and broadcast-optionally separated) subaddresses 0 and 31. Two exceptions involve the Transmit Last Command and Transmit BIT Word mode codes, in which the Data Words are accessed from internal registers.

If this bit is logic "1," there is capability to request interrupts to following the reception of messages containing specific, individual mode commands. Interrupts may be enabled for selected mode codes, as a function of broadcast/own address and the T/R* bit and mode code fields of received mode code messages. This is implemented by means of the mode code selective interrupt table, address locations 0108 through 010F in the shared RAM.

In addition, if ENHANCED MODE CODE HANDLING is logic "1," the Data Words for individual mode codes are mapped as a function of receive/transmit/broadcast and the lower four bits of the mode code field (bit 4 of the mode code field is assumed to be logic "1" for a mode code command with data). If ENHANCED MODE CODE HANDLING is logic "1," address locations 0110 through 013F are dedicated to the storage of Data Words for mode code messages.

If ENHANCED MODE CODE HANDLING is logic "0," the RT lookup table pointer to the (single word) Data Word block will be stored in the third word of the RT message descriptor in the RT Command Stack for mode code messages. If ENHANCED MODE CODE HANDLING is logic "1," **the received or transmitted Data Word** associated with a mode code message, rather than the pointer, will be stored in the third location of the message descriptor in the stack. If ENHANCED MODE CODE HANDLING is logic "1," there will be **no** word stored in the third word of the RT message descriptor for mode code messages with no Data Word.

It should be noted that ENHANCED MODE CODE HANDLING has no effect on the Data Word transmitted in response to a Transmit Last Command mode code. The Data Word in response to this command, representing the previous Command Word received by the RT, is **always** accessed from an internal register in the ACE and not from a RAM location.

CONFIGURATION REGISTER #4 (Address XX10; RD/WR)

TABLE 24. CONFIGURATION REGISTER #4	
BIT	**DESCRIPTION**
15(MSB)	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BROADCAST MASK ENABLED/XOR*
10	RETRY IF 1553A AND MESSAGE ERROR
9	RETRY IF STATUS SET
8	FIRST RETRY ALT/SAME* BUS
7	SECOND RETRY ALT/SAME* BUS
6	VALID IF MESSAGE ERROR BIT/NO DATA
5	VALID BUSY BIT/NO DATA
4	MONITOR TIME GAP OPTION
3	LATCH RT ADDRESS WITH CFG REG #5
2	TEST MODE 2
1	TEST MODE 1
0(LSB)	TEST MODE 0

Note: The ACE must be programmed for its ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 must be logic "1") PRIOR to being able to activate any of the functions enabled by Configuration Register #4.

EXTERNAL BIT WORD ENABLE: Affects RT only. If programmed to logic "0," the ACE RT will respond to a Transmit BIT Word mode command with the contents of the ACE's internal BIT Word Register as the Data Word. If programmed to logic "1," the ACE will access the BIT Data Word from a location in the shared RAM. In the latter instance, the BIT Word must be written to RAM by the host processor.

The location of the BIT Word RAM address is as follows: if ENHANCED MODE CODE HANDLING, bit 0 of Configuration Register #3, is programmed to logic "0," the BIT Word will be read from the location referenced by the active area Lookup Table pointer for transmit subaddress 0 or 31. In this configuration, it should be noted that the Data Word in response to a Transmit vector word mode command will be read from the **same** pair of address locations in which the external BIT Word is stored. If EXTERNAL BIT WORD ENABLE **and** ENHANCED MODE CODE HANDLING are **both** programmed to logic "1," the BIT Word will be read from the fixed shared RAM address location 0123.

INHIBIT BIT WORD TRANSMIT IF BUSY: Affects RT only. If programmed to logic "0" and either BUSY* (bit 10 of Configuration Register #1) is programmed to logic "0," **or** if BUSY LOOKUP TABLE (bit 13 of Configuration Register #2) is logic "1" **and** the respective bit(s) in the Busy lookup table (bit 0 of

location 0242 and/or bit 15 of location 0243) is programmed to logic "1," the ACE will respond to a Transmit BIT Word mode command with its RT Status Word with the BUSY bit set, followed by its internal or external Built-in-Test (BIT) Word. If INHIBIT BIT WORD TRANSMIT IF BUSY is programmed to logic "1" and BUSY* is programmed to logic "0" or the appropriate bit in the Busy lookup table is logic "1," the ACE will respond with its RT Status Word with the BUSY bit set, but **no** Data Word (BIT Word) will be transmitted.

MODE CODE OVERRIDE BUSY: Affects RT only. If programmed to logic "0" and BUSY* (bit 10 of Configuration Register #1) is programmed to logic "0" **or** if BUSY LOOKUP TABLE (bit 13 of Configuration Register #2) is logic "1" and the respective bit(s) in the Busy Lookup Table (bit 0 of location 0242 and/or bit 15 of location 0243) is programmed to logic "1," the ACE will transmit only its Status Word with its BUSY bit set. It will **not** transmit a following Data Word, in response to either a Transmit Vector Word mode command or a Reserved transmit mode command with data (transmit mode codes 10110 through 11111).

If programmed to logic "1" and BUSY* is programmed to logic "0" **or** if BUSY LOOKUP TABLE (bit 13 of Configuration Register #2) is logic "1" and the respective bit(s) in the Busy Lookup Table (bit 0 of location 0242 and/or bit 15 of location 0243) is programmed to logic "1," the ACE will transmit its Status Word with its BUSY bit set, **followed by a single Data Word**, in response to either a Transmit Vector Word mode command or a Reserved transmit mode command with data (transmit mode codes 10110 through 11111).

EXPANDED BC CONTROL WORD ENABLE: Affects BC mode only. If either ENHANCED MODE (bit 15 of Configuration Register #3) **or** EXPANDED BC CONTROL WORD ENABLE is programmed to logic "0," the ACE BC Control Word defaults to that of the previous generation hybrid, the BUS-61559. That is, only bits are 7, 6, 5, 2, 1, and 0 are active; in this configuration, the functions of the other bits cannot be activated. If both ENHANCED MODE **and** EXPANDED BC CONTROL WORD ENABLE are programmed to logic "1," then **all 15 bits** (bits 14 through 0) of the BC Control Word are enabled (may be activated).

BROADCAST MASK ENABLED/XOR*: Affects BC mode only. This bit effects the operation of bit 5 of the BC Control Word, MASK BROADCAST. If BROADCAST MASK ENABLED/XOR* is logic 0 and the MASK BROADCAST bit of the message's BC Control Word is logic "1," the expected value of the Broadcast Command Received Status Word bit becomes "1," rather than "0." If BROADCAST MASK ENA/XOR* is programmed to logic "1," the MASK BROADCAST bit of the BC Control Word is used as a mask bit, rather than performing an "XOR" operation with the Broadcast Received Status Word bit. In this instance, a Status Set condition arising from the Broadcast Command Received RT Status bit occurs when MASK BROADCAST is logic "0" and the Broadcast Command Received RT Status Word bit is logic "1."

RETRY IF 1553A AND MESSAGE ERROR: This bit effects the operation of BC retries. If programmed to logic "0," BC retries will result from the following conditions: no response timeout, format errors such as incorrect Status Word address, invalid word, incorrect sync type, low and high word count.
If programmed to logic "1," the BC will also retry as a result of any of the conditions listed above. In

addition, a message will also be retried if the 1553A/1553B* bit of the BC Control Word (bit 3) is programmed to logic "1" **and** the Message Error bit in the RT Status Word is logic "1."

RETRY IF STATUS SET: This bit affects the operation of BC retries. If programmed to logic "0," the BC will **not** retry a message as a result of one or more bits being set in an RT Status Word; the only exception being that if RETRY IF 1553A AND MESSAGE ERROR (bit 10 of this register) is logic "1," a message will be retried if the 1553A/1553B* bit of the BC Control Word (bit 3) is programmed to logic "1" **and** the Message Error bit in the RT Status Word is logic "1."

If RETRY IF STATUS SET is programmed to logic "1," the BC will retry a message in which a STATUS SET condition was detected. A STATUS SET condition is defined as follows: If bit 12 of Configuration Register #4, EXPANDED BC CONTROL WORD, is programmed to logic "0," STATUS SET encompasses **all 8** of the nonreserved Status Word bits. The expected value for the 8 nonreserved Status Word bits is LOGIC "0," with one exception: If bit 11 of Configuration Register #4, BROADCAST MASK ENA/XOR*, is logic 0 and the MASK BROADCAST bit of the message's BC Control Word is LOGIC "1," the expected value of the Broadcast Command Received bit becomes 1, rather than 0. If BROADCAST MASK ENA/XOR* is programmed to logic "1," the MASK BROADCAST bit of the BC Control Word is used as a mask bit, rather than performing an "XOR" operation with the Broadcast Received Status Word bit; in this instance, a Status Set condition arising from the Broadcast Command Received RT Status bit occurs when the MASK BROADCAST BC Control Word bit is logic "0" and the Broadcast Command Received RT Status Word bit is logic "1."

If EXPANDED BC CONTROL WORD is programmed to logic "1," a STATUS SET condition is defined such that the only bits that can result in a STATUS SET condition are those for which the corresponding bits in the message's BC Control Word have been programmed to logic "0."

FIRST RETRY, SECOND RETRY ALT/SAME* BUS: These two bits effect the operation of BC retries. Bit 8 selects the bus on which the first message retry (following the failed initial message) will take place. If bit 8 is logic "0," the first retry will take place on the same bus as the original message. If bit 8 is logic "1," the first retry will take place on the alternate bus from where the message was originally transmitted.

Similarly, bit 7 selects the bus for the second retry attempt. A second retry will be attempted only if DOUBLE/SINGLE* RETRY, bit 3 of Configuration Register #1, has been programmed to logic "1." The second retry only takes place after a first retry has failed. If bit 7 is logic "0," the second retry takes place on the same bus as the original message. If bit 7 is logic "1," the second retry will take place on the alternate bus from where the message was originally transmitted.

VALID IF MESSAGE ERROR BIT/NO DATA: This bit affects the BC validation criteria for RT responses. When this bit is programmed to logic "0," if an RT responds to a transmit command with the Message Error bit set in its Status Word, the response is considered valid **only** if the Status Word is followed by the requested number of Data Words. In this scenario, a response of Status Word only with Message Error bit set, followed by no Data Words is considered to be a format error.

If programmed to logic "1," an RT response to a transmit command of Status Word with the Message Error bit set followed by the requested number of Data Words is considered a valid response. In addition, in this mode, a response of Status Word with the Message Error bit set followed by **no** Data Words is also considered a valid response, rather than a format error.

VALID BUSY BIT/NO DATA: This bit effects the BC validation criteria for RT responses. When this bit is programmed to logic "0," if an RT responds to a transmit command with the BUSY bit set in its Status Word, the response is considered valid **only** if the Status Word is followed by the requested number of Data Words. In this scenario, a response of Status Word only with the BUSY bit set, followed by no Data Words is considered to be a format error.

If programmed to logic "1," an RT response to a transmit command of Status Word with the BUSY bit set followed by the requested number of Data Words is considered a valid response. In addition, in this configuration, a response of Status Word with the BUSY bit set followed by no Data Words is also considered a valid response, rather than a format error.

MONITOR TAG GAP OPTION: This bit affects the operation of the Monitor Identification Word in the Word Monitor mode. Specifically, it affects the operation of the CONTIGUOUS DATA/GAP* bit, the 8-bit GAP TIME field, and the MODE CODE* bit. If programmed to logic "0" and a word is received on the alternate bus from the previous command, the CONTIGUOUS DATA/GAP* bit will be logic "0" (even if the time frame of the current word **overlapped** that of the previous word) and the GAP TIME field will assume a value of 20 µs **greater** than the actual time gap (if any) between the end of the previous word on the alternate bus and the start of the current word on the current bus. The operation of the MODE CODE* bit in the tag word will remain unchanged from the previous AIM-HY and AIM-HY'ER components, ie a logic 1 indicates that the word is not a mode code while a logic 0 indicates that the word is a mode command.

If programmed to logic "1" and a word is received on the alternate bus from the previous command within a time frame overlapping that of the previous word, the CONTIGUOUS DATA/GAP* bit will be logic "1" and the GAP TIME field will assume a value of 0. If there is a gap in time between the end of the previous word on the alternate bus and the start of the current word on the same bus, CONTIGUOUS DATA/GAP* will assume a value of logic "0" and the 8-bit GAP TIME field will reflect the correct time between the previous and current words. It will **not** be offset (high) by 20 µs.

In addition, in this mode (bit programmed to logic "1"), the MODE CODE* bit in the monitor tag word will change function to signify the occurance of a Hand Shake failure. A hand shake failure occurs in the transparent mode when an external arbitration circuit withholds the data transfer grant signal beyond the specified timeout period. When a timeout occurs, the monitored 1553 word and tag word will be lost and the ACE will set the MODE CODE* bit in the tag word of the NEXT monitored word to indicate that a timeout occurred and a word was lost. Note that this feature is not implemented in some versions of the ACE family.

LATCH RT ADDRESS WITH CONFIG REGISTER 5: This bit is used to allow the host processor to update RT Address by writing to Configuration Register #5. A logic "0" in this bit locks the RT Address (ie. writing to Configuration Register #5 has no effect on the value of the RT address). A logic "1" in this bit unlocks the RT Address, allowing the host processor to update the RT address by writing to Configuration

Register #5. Following Power-up Reset or a device reset in the Status/Control Register, the RT address will revert to a default value of all zeros (RT Address "00000", with a parity error). Note that a software reset in the Start/Reset Register has no effect on the value of the RT address.

It should also be noted that in ENHANCED mode, the current latched values of the ACE's RT Address and RT Address parity may **always** be read from bits 5 through 0 of Configuration Register #5.

(NOTE: Only the BU-61586 ACE (BU-65528MX) is capable of RT Address latching; the BU-61585 ACE (BU-65527) only operates in the hardwired RT Address Mode).

TEST MODE 2, 1, 0: Used for test purposes only. Must be programmed to logic "000" for normal operation.

CONFIGURATION REGISTER #5 (Address XX11; RD/WR)

TABLE 25. CONFIGURATION REGISTER #5	
BIT	**DESCRIPTION**
15(MSB)	12 MHZ CLOCK SELECT
14	SINGLE-ENDED SELECT
13	EXTERNAL TX INHIBIT A
12	EXTERNAL TX INHIBIT B
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	RT ADDR LATCH/TRANSPARENT*
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0(LSB)	RT ADDRESS PARITY

NOTE: The ACE must be programmed for its ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 must be logic "1") PRIOR to being able to activate any of the functions enabled by Configuration Register #5.

CLOCK 12/16* SELECT (Read/Write): The default for CLOCK 12/16* SELECT is logic "0," enabling 16 MHz operation. **This bit must not be set to a logic "1"**.

SINGLE-ENDED SELECT : This bit is internally connected to logic "1".

EXTERNAL TX_A INHIBIT (Read Only): This bit is internally connected to logic "0".

EXTERNAL TX_B INHIBIT (Read Only): This bit is internally connected to logic "0".

EXPANDED ZERO-CROSSING ENABLED (Read/Write): This bit selects the sampling frequency of the ACE Manchester II decoders. If programmed to logic "0," the decoders sample using a **single** edge of the CLOCK input. That is, the decoder sampling frequency is either 16 MHz or 12 MHz. If programmed to logic "1," the decoders sample using **both** edges of the clock input. In this case, the decoder sampling frequency doubles to either 24 MHz or 32 MHZ. The higher sampling frequency provides improved

tolerance (about 30 to 40 ns) to input zero crossing distortion. It should be noted, however, that if the expanded zero-crossing option is used, a tighter tolerance is required for the ACE's CLOCK input. The required duty cycle range for the CLOCK input is approximately 33% to 67% if the expanded zero-crossing option is not used, and approximately 40% to 60% if expanded zero-crossing is used.

RESPONSE TIMEOUT SELECT 1, 0 (Read/Write): These two bits are used to select the value of the ACE's response timeout timer. This timer is used in BC mode, for RT mode (for messages in which the ACE is the receiving RT in an RT-to-RT transfer), and in the Message Monitor mode. The four programmable choices (approximate timeout values) are shown in TABLE 26.

TABLE 26. RESPONSE TIMEOUT SELECT

BIT 10 RESPONSE TIMEOUT SELECT 1	BIT 9 RESPONSE TIMEOUT SELECT 0	RESPONSE TIMEOUT TIME VALUE (µs)
0	0	18.5*
0	1	22.5
1	0	50.5
1	1	130

*Note: default value for non-ENHANCED mode is 18.5 µs

GAP CHECK ENABLED (Read/Write): If programmed to logic "0," the ACE does **not** check for a minimum of dead bus time prior the start of transmission by another terminal on the 1553 bus. If programmed to logic "1," the ACE **does** verify for a minimum of 2 µs of dead bus time prior to the transmission by an external BC or RT on the 1553 bus. If this minimum gap time is violated, the ACE will determine that the BC Command Word or the RT Response (Status Word) is invalid, representing a message format error.

BROADCAST DISABLED (Read/Write): Applicable to RT and Monitor modes. If the BROADCAST DISABLED bit is programmed to logic "0," the ACE will recognize RT Address 31 as the broadcast address. In this configuration, RT Address 31 **cannot** be used as the ACE's discrete RT Address. If BROADCAST DISABLED is programmed to logic "1," the ACE will **not** recognize RT Address 31 as the broadcast address. In this instance, RT Address 31 may be used as a discrete RT address.

It should be noted that for the BU-65620 digital monolithic, the value of BROADCAST DISABLED is affected by the input signal BRO_ENA. If BRO_ENA is connected to logic "0," broadcast is **disabled**. In this case, BROADCAST DISABLED will **always** return logic "1" when read. If BRO_ENA is connected to logic "1," enabling broadcast for the BU-65620 is software programmable, as described in the preceding paragraph. For BU-65170, BU-61580, BU-61585 and BU-61590, the use of broadcast is **always** software programmable, as described above.

In Word Monitor mode, bit 5 of the Monitor Identification Word, BROADCAST*, will **ALWAYS return logic "1"** (even for a Command Word to RT Address 31) if BROADCAST DISABLED has been programmed to logic "1."

RT ADDRESS LATCH/TRANSPARENT* (Read Only): This bit is internally hardwired to logic "1".

RT ADDRESS 4-0 and RTADP (Read/Write): These six bits return the values of the five RT Address bits and the RT Address parity that are latched internally within the ACE. If the parity sum of the selected RT address is not odd, the ACE will not recognize, and not respond to, a Command Word directed to the ACE's discrete RT address. It will, however, receive messages to the broadcast address (address 31), unless broadcast has been disabled.

If LATCH RT ADDRESS WITH CONFIG REG 5 (bit 3 of Configuration Register #4) is set to logic "0," writing to Configuration Register #5 has **no effect** on the value of the ACE's RT address and parity. If LATCH RT ADDRESS WITH CONFIG REG 5 is a logic "1," the Remote Terminal address will be latched internally when the host processor performs a write operation to Configuration Register #5.

It should be noted that in ENHANCED mode, the current value of the ACE's RT Address (including parity) may **always** be read from bits 5 through 0 of Configuration Register #5, for all versions of the ACE.

(NOTE: Only the BU-61586 ACE (BU-65528MX) is capable of RT Address latching; the BU-61585 ACE (BU-65527) only operates in the hardwired RT Address Mode).

RT/MONITOR DATA STACK ADDRESS (Address XX12; RD/WR)

TABLE 27. RT/MONITOR DATA STACK ADDRESS REGISTER	
BIT	**DESCRIPTION**
15(MSB)	RT/MONITOR DATA STACK ADDRESS 15
•	•
•	•
•	•
0(LSB)	RT/MONITOR DATA STACK ADDRESS 0

In RT mode, the pointer word read from the lookup table during the Start-of-Message (SOM) sequence is initially loaded into the Data Stack Address Register. The value of the register is then incremented by one (modulo the Data Stack size) after each successive Data Word accessed to/from the respective Data Word table.

In the Word Monitor mode, the Monitor Data Stack Address contains the current value of the Data Stack Pointer. In the Selective Message Monitor or combined RT/Monitor modes, this register contains the current value of the Monitor Data Stack Pointer.

BC FRAME TIME REMAINING (Address XX13; READ ONLY)

TABLE 28. BC FRAME TIME REMAINING REGISTER	
BIT	**DESCRIPTION**
15(MSB)	BC FRAME TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC FRAME TIME REMAINING 0

The BC frame time is programmable in increments of 100 µs, up to 6.55 ms.

BC MESSAGE TIME REMAINING (Address XX14; READ ONLY)

TABLE 29. BC MESSAGE TIME REMAINING REGISTER	
BIT	**DESCRIPTION**
15(MSB)	BC MESSAGE TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC MESSAGE TIME REMAINING 0

The BC Message Time Remaining has a resolution of 1 µs/LSB. The maximum range on this timer is 65.535 ms.

BC FRAME TIME/RT LAST COMMAND/MT TRIGGER REGISTER (Address XX15; RD/WR)

TABLE 30. BC FRAME TIME/RT LAST COMMAND/MT TRIGGER REGISTER	
BIT	**DESCRIPTION**
15(MSB)	BIT 15
•	•
•	•
•	•
0(LSB)	BIT 0

In BC mode, the BC frame time, used in the BC AUTO-REPEAT mode, is programmable by means of this register. The value of the BC FRAME TIME is programmable in increments of 100 µs/LSB, up to a maximum of 6.55 seconds.

In RT mode, this register stores the Command Word for the current or last message processed by the ACE RT. This register is updated at the **beginning** of each message processed by the ACE RT.

In the Word Monitor mode, this register stores the contents of the Monitor Trigger Word. This word must be supplied by the host processor. When the ACE Word Monitor is on-line, it compares the contents of this register to all valid, received Command Words. The Monitor Trigger mechanism may be used to start the Word Monitor, stop the Word Monitor, or generate interrupt requests. The trigger feature is **NOT** applicable for the Message Monitor and RT/Message Monitor modes.

RT STATUS WORD REGISTER (Address XX16; READ ONLY)

TABLE 31. RT STATUS WORD REGISTER (Shown for MIL-STD-1553B Status Word)	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPT
0(LSB)	TERMINAL FLAG

RT BIT WORD REGISTER (Address XX17; READ ONLY)

TABLE 32. RT BIT WORD REGISTER	
BIT	**DESCRIPTION**
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	CHANNEL B/A*
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

BLOCK STATUS WORD

The Block Status Word is stored in the first location of the Message Block descriptor in the Command Stack for BC, RT, Selective Monitor, and RT/Selective Monitor modes. There are two Command Stacks maintained for the RT/Selective Monitor mode: one for the RT, one for the Monitor. There is **no** Command Stack in the Word Monitor mode. For all modes except Word Monitor, the Block Status Word is updated by the ACE's 1553 memory management logic both at the beginning and at the end of the respective message. It contains information relating to whether the message is in progress or has been completed, what channel it was processed on, and whether or not there were any errors in the message.

TABLE 33. BC MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

Note: In BC mode, if a message is retried, the bits of the Block Status Word reflect the result of the latest message retry.

TABLE 34. RT MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	RT-RT FORMAT ERROR
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	CIRCULAR BUFFER ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 35. MESSAGE MONITOR MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

BC OPERATION

The BC protocol of the ACE implements all MIL-STD-1553B message formats. Message format is programmable on a message by message basis by means of individual BC Control Words and the T/R* bit of the Command Word to be transmitted. In addition to message format, the BC Control Word allows bus channel, self-test, retries, interrupts, and Status Word masking to be specified on an individual message basis. The BC performs all error checking required by MIL-STD-1553B. This includes validation of sync type and encoding, Manchester II encoding, parity, bit count, word count, and Status Word RT Address field. RT response time is verified to be less than the ACE's programmable response timeout value (17.5 to 19.5 µs default).

BC MEMORY ORGANIZATION

TABLE 36 illustrates a typical memory map for the ACE bus controller. Note that there are eight (8) fixed memory locations within the BC memory map. For each of the two global "areas" (A and B), these are the Stack Pointer and Message Counter, and the Initial Stack Pointer and Message Counter. The Stack Pointer and Message Counter must be initialized by the host processor before starting single message frames. For the frame auto-repeat mode, the Initial Stack Pointer and Initial Message Count locations must be initialized by the CPU before initializing a repetitive frame of BC messages.

TABLE 36. TYPICAL NON-ENHANCED BC MEMORY MAP
(shown for 12K RAM, ENHANCED mode)

Word ADDRESS	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101	Message Count A (fixed location)
0102	* Initial Stack Pointer A (Auto-Frame Repeat Mode)
0103	* Initial Message Count A (Auto-Frame Repeat Mode)
0104	Stack Pointer B (fixed location)
0105	Message Count B (fixed location)
0106	* Initial Stack Pointer B (Auto-Frame Repeat Mode)
0107	* Initial Message Count B (Auto-Frame Repeat Mode)
0108-012D	Message Block 1
012E-0153	Message Block 2
•	•
•	•
0ED6-0EFB	Message Block 94
0EFC-0EFF	Not Used
0F00-0FFF	Stack B
1000-1025	Message Block 95
1026-104B	Message Block 96
•	•
•	•
1DCE-1DF3	Message Block 188
•	•

* Note: Used only in the ENHANCED BC mode with Frame Auto-Repeat enabled.
The user is free to locate the BC stack and BC message blocks anywhere within the ACE's 64K word (4K or 12K internal) address space.

256-Word Boundaries

It should be noted that the BC (as well as RT) stack area of RAM will roll over at the boundary in the ACE shared RAM address space as specified by bits 14 and 13 of Configuration Register #3 (default is 256 words). The BC/RT Stack size is programmable with choices of 256 words (64 messages), 512, 1024, and 2048 words (512 messages). The default is 256 words (64 messages). That is, the value of the Stack Pointer will increment from XXFF to XX00, not to (XX+1)00. If bit 10 of Configuration Register #2, 256-WORD BOUNDARY DISABLE, is logic 0, the 256-word boundaries will also be enforced for BC message blocks.

However, if 256-WORD BOUNDARY DISABLE is programmed to logic "1," the address for BC message blocks **will not** roll over at 256-word boundaries. This allows for more efficient allocation of the shared RAM address space for storing BC message blocks.

For BC mode, it is strongly recommended that 256-WORD BOUNDARY DISABLE be programmed to logic "1."

For simplicity of illustration, the maximum message size is allocated for each BC message block in the typical BC memory map of TABLE 36. Note, that the maximum size of a BC message block is 38 words, for an RT-to-RT transfer of 32 Data Words (Control + 2 Commands + Loopback + 2 Status Words + 32 Data Words). This requires that 256-word boundaries are disabled.

Active Areas Double Buffering

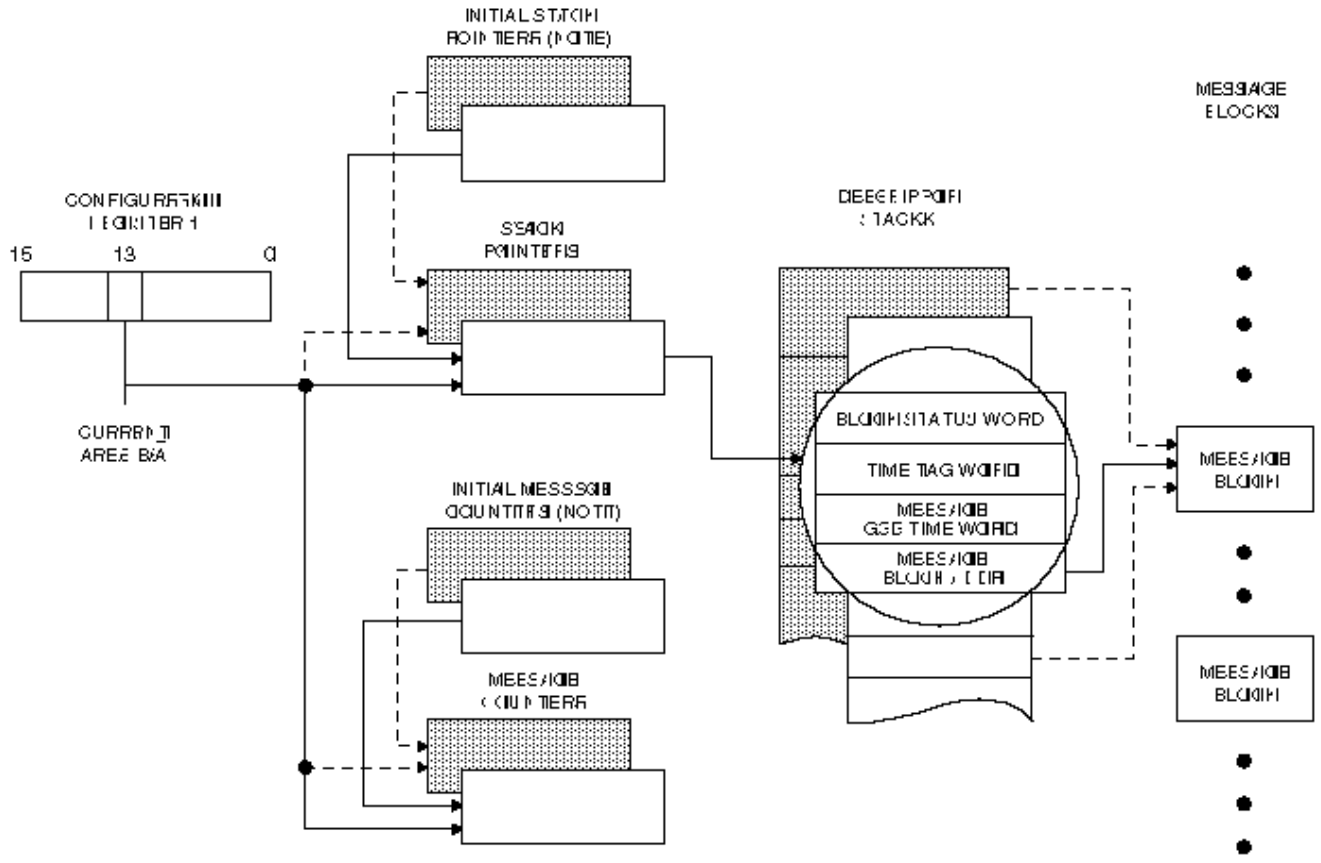
The Active Area facility provides a global mechanism for dividing the shared RAM into "active" and "nonactive" areas. At any point in time, only the various data structures within the "active" area are accessed by the internal 1553 memory management logic. It should be noted, however, that at any point in time, **both the "active" and "nonactive" areas are accessible by the host processor.**

It should be noted that if the host CPU changes the active area while a BC frame is being processed (by toggling bit 13 of Configuration Register #1), the active area **will NOT actually switch until the current BC frame has been completed.**

PROGRAMMING OF BC MESSAGE FRAMES

BC Memory Management

An overview of the ACE memory management scheme for BC mode is illustrated in FIGURE 7. The BC may be programmed to transmit multimessage frames of up to 512 unique messages. The number of messages to be processed is programmable by means of the fixed Message Count location in the shared RAM. In addition, the host processor must initialize a second fixed location as the Stack Pointer. This RAM location contains a pointer that references the four-word message block descriptor (in the Stack area of shared RAM) for each message to be processed. Each message resides in a designated message block area of the shared RAM. The starting location for each message block is specified by a pointer that is stored in the fourth location of the block descriptor for the respective message. This pointer must be loaded by the host processor before the message is processed. The first word of each BC message block is the BC Control Word.



Note: Initial Stack Pointers and Initial Message Counters are only used in BC FRAME AUTO-REPEAT Mode.

FIGURE 7. BC MEMORY MANAGEMENT

Referring to FIGURE 7, the CPU may select between global Area A and global Area B by means of bit 13 of

Configuration Register #1. In the figure, it is assumed that Area A is delineated by the nonshaded area and is the current "active" area; it can be assumed that Area B is the "nonactive" (shaded) area.

The ACE's global double buffering feature provides a relatively simple-minded mechanism for ensuring data consistency. The host processor designates the current active area by means of bit 13 of Configuration Register #1 (ACTIVE AREA B/A*). A common practice is for the host CPU to access the "nonactive" area, while allowing the ACE's 1553 protocol logic to access the "active" area. After the current message frame has been completed for the current "active" area, the host should switch ("ping-pong") the "active" and "nonactive" areas by means of ACTIVE AREA B/A*.

The use of the ACE's global double buffering feature eliminates the possibility of data inconsistency by precluding the possibility that the BC will transmit or that the CPU will read a mixture of old and new Data Words for any particular message. In addition, this technique eliminates the possibility of a contended CPU access to the ACE's shared RAM.

A variation on the global buffering scheme is the use of "multiple buffering." That is, instead of using the ACE's ACTIVE AREA B/A* feature, it is possible to program **several** message frame scenarios. This is done by positioning a number of descriptor stacks at different areas within the ACE shared RAM address space. In turn, the pointer words for the individual message block descriptors in the stacks can reference message blocks anywhere within the address space. When one message frame has been completed, the host processor need only re-assign the values of the Stack Pointer and Message Counter to initiate processing of the next BC message frame.

To process a single message frame, the "active area" stack pointer and message count locations must be initialized by the host CPU before processing each individual message frame. For the frame auto-repeat mode, the values for the initial stack pointer and initial message counter locations must be initialized. The initial pointer and counter need be initialized only **once**, prior to the processing of the first message frame.

At any point in time, the stack pointer points to the first word of the block descriptor for the current message. As illustrated in FIGURE 7, there are four words in the descriptor stack for each BC message. The first two locations are reserved for the Block Status Word and Time Tag Word. These two words are written by the ACE's BC protocol logic at the beginning and end of each message processed. The BC Block Status Word contains bits relating to message status and completion, validity, and bus channel. The time tag word reflects the contents of the ACE's Time Tag Register at the beginning (and end) of a message. The time tag register has a programmable resolution of 2 to 64 µs/LSB, in even powers of two. The Time Tag counter may also be clocked from an external oscillator.

The second two locations within the BC block descriptor must be loaded by the host processor. The Message Gap Time Word is accessed if the ACE is in ENHANCED MODE (bit 15 of Configuration Register #3 is programmed to logic "1") **and** MESSAGE GAP TIME ENABLED (bit 15 of Configuration Register #1) is programmed to logic "1." The Message Gap Time Word specifies the time **from the beginning of the current message to the beginning of the subsequent message**. Reference FIGURE 9. The resolution of the message Gap is 1 µs/LSB. The Message Block Address provides a pointer to the first word of the message block (the BC Control Word) for the respective message. The value of the active area Stack Pointer is incremented by four following each message processed by the ACE BC.

The message count (or initial message count) location must be initialized by the CPU to correspond to the **ones complement** of the number of messages to be processed in a message frame. For example, if a message frame contains one (1) message, the (Initial) Message Counter location should be loaded with a value of FFFE. The value of the (Initial) Message Counter is incremented by one at the end of each message processed.

As illustrated in FIGURE 8, the BC Control Word is the first word (word number "0") within the individual BC message block. The BC Control Word is **not** transmitted on the 1553 bus. FIGURE 8 illustrates the message block structures for all of the possible BC message formats. The words to be transmitted and received are in the order they appear in the BC message blocks. The BC Control Word is the principal control entity for individual BC messages. The bits in the BC Control Word contain information relating to the message format, bus channel, interrupt enabling, 1553A vs. 1553B error handling, off-line self-test, retries, and Status Word bit masking.

If ENHANCED BC MODE is enabled (the ACE is programmed for ENHANCED MODE **and** EXPANDED BC CONTROL WORD ENABLED, bit 12 of Configuration Register #4, is programmed to logic "1"), then **all 15** bits (bit 15 is "NOT USED") of the BC Control Word are used. If ENHANCED BC MODE is logic "0," then only bits 7,6,5,2,1, and 0 are used. This includes the 7 Status Mask bits.

The STATUS SET bits designate various RT Status Word bits as either "care" (if logic "0") or "don't care" (if logic "1"). If one or more of the designated "care" bits are set to logic "1" in a responding RT's Status Word, then item (1), and possibly items (2), (3), and (4) below will occur:

(1) The STATUS SET bit (bit 11) of the BC Block Status Word will be logic "1."

(2) If STATUS SET, bit 1 of the Interrupt Mask Register is logic "1," an interrupt request will be issued.

(3) If STATUS SET, bit 1 of the Interrupt Mask Register is logic "1" **or** ENHANCED INTERRUPTS, bit 15 of Configuration Register #2 is logic "1," then STATUS SET, bit 1 of the INTERRUPT STATUS REGISTER, will be logic "1."

(4) If RETRY ENABLED (bit 4 of Configuration Register #1) **and** RETRY IF STATUS SET (bit 9 of Configuration Register #4) **and** RETRY ENABLED (bit 8 of the BC Control Word) are all logic "1," the message will be retried.

The host CPU must write the (first) Command Word in the next location after the BC Control Word. After this word, a possible second Command Word (for RT-to-RT transfers), and Data Words to be transmitted by the BC need to be loaded by the host. In the subsequent addresses, locations must be reserved for the Loopback Word and received Status and Data Words.

Message Block Formats

In BC mode, the ACE supports all MIL-STD-1553B message formats. For each 1553B message format, the ACE requires a specific sequence of words within the BC Message Block. This includes locations for the Control, Command, and (transmitted) Data Words that are loaded by the host processor to be read from RAM by the BC protocol logic. In addition, subsequent contiguous locations must be allocated for storage of received Loopback, RT Status, and Data Words. TABLE 37 illustrates the bit mapping of the command word and TABLE 38 illustrates the bit mappings for the status word (for more information on 1553 command and status words refer to DDC's MIL-STD-1553 Designer's Guide). FIGURE 8 illustrates the organization of the BC message blocks for the various MIL-STD-1553B message formats. Note that for all of the message formats, the BC Control Word is located in the first location of the message block.

TABLE 37. MIL-STD-1553 COMMAND WORD

BIT	DESCRIPTION
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
•	•
•	•
11	REMOTE TERMINAL ADDRESS BIT 0
10	TRANSMIT/RECEIVE*
9	SUBADDRESS/MODE CODE BIT 4
•	•
•	•
6	SUBADDRESS/MODE CODE BIT 0
5	DATA WORD COUNT/MODE CODE BIT 4
•	•
•	•
0(LSB)	DATA WORD COUNT/MODE CODE BIT 0

TABLE 38. MIL-STD-1553B STATUS WORD

BIT	DESCRIPTION
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
14	REMOTE TERMINAL ADDRESS BIT 3
13	REMOTE TERMINAL ADDRESS BIT 2
12	REMOTE TERMINAL ADDRESS BIT 1
11	REMOTE TERMINAL ADDRESS BIT 0
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPTANCE
0(LSB)	TERMINAL FLAG

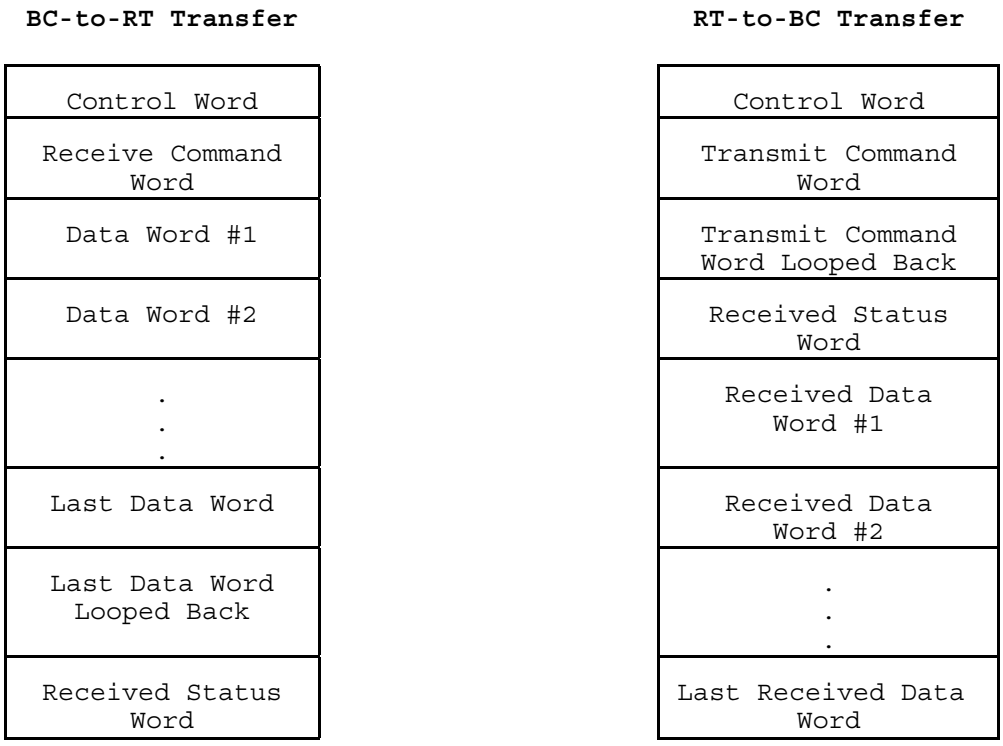


FIGURE 8. BC MESSAGE BLOCK FORMATS

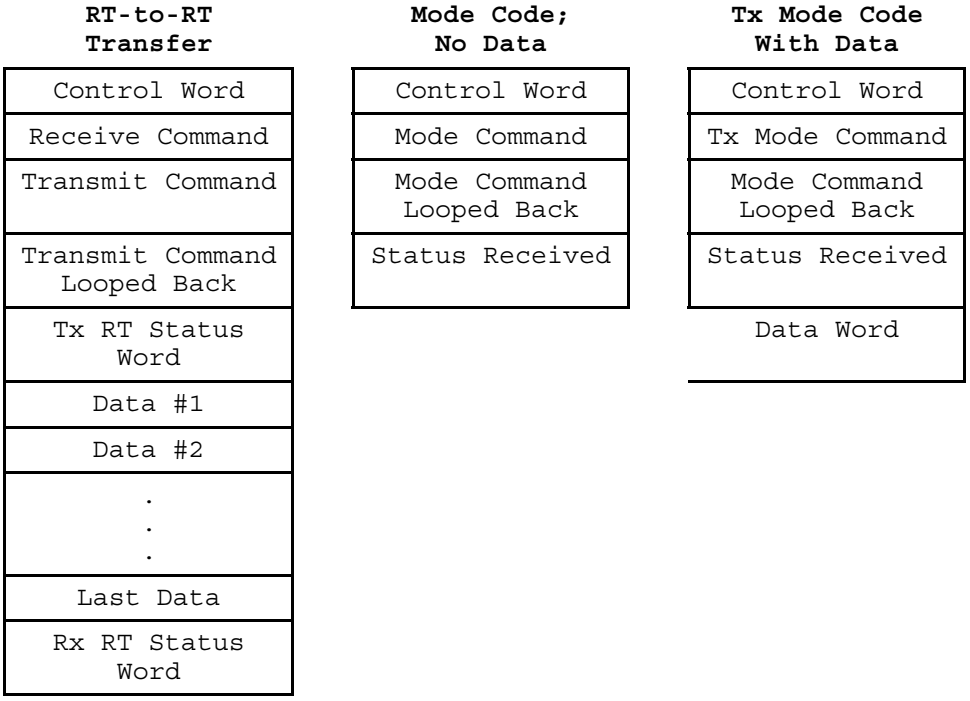


FIGURE 8. BC MESSAGE BLOCK FORMATS (cont.)

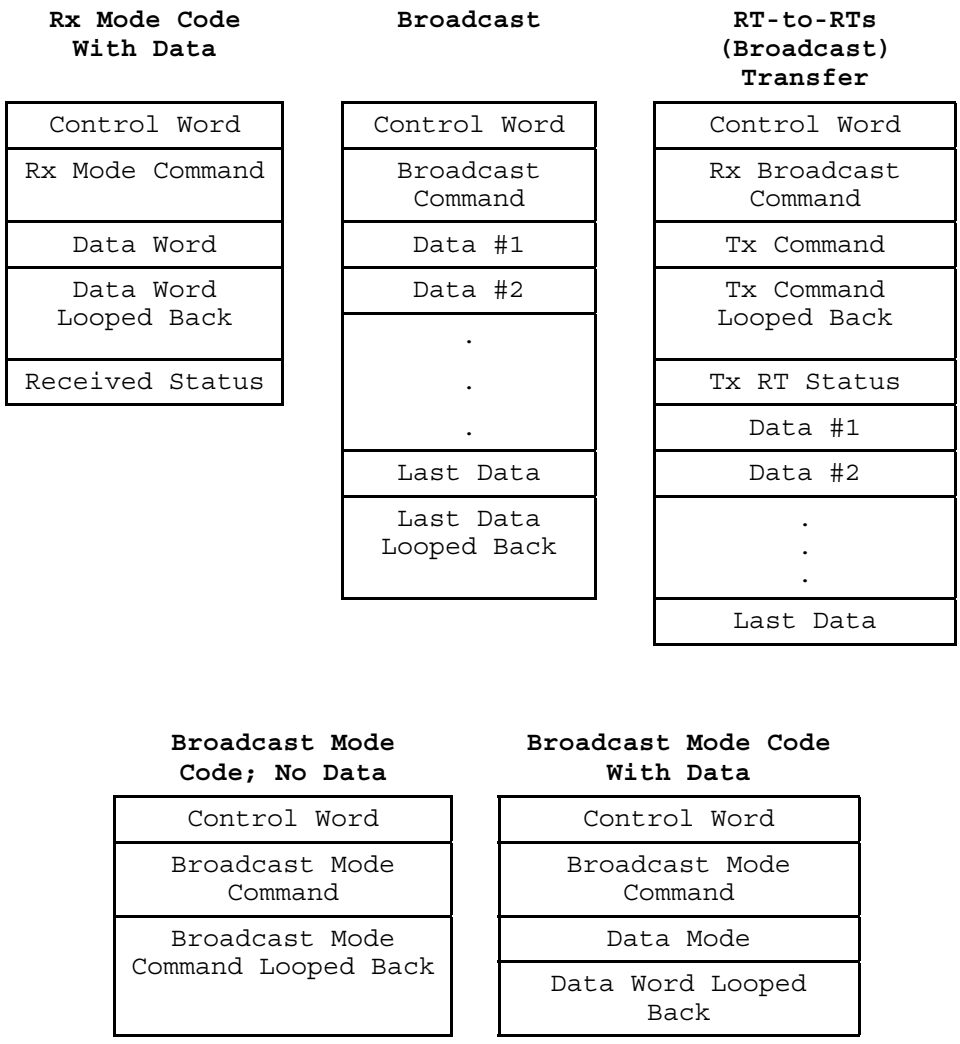


FIGURE 8. BC MESSAGE BLOCK FORMATS (cont.)

BC CONTROL WORD

For each of the BC Message Block formats, the first word in the block is the BC Control Word. The BC Control Word is **not** transmitted on the 1553 bus. Instead, it contains bits that select the active bus and message format, enable off-line self-test, and specify the "expected value" of the BROADCAST COMMAND RECEIVED RT Status bit. The bit mapping and definitions of the BC Control Word are illustrated in TABLE 39.

TABLE 39. BC CONTROL WORD REGISTER

BIT	DESCRIPTION
15(MSB)	RESERVED
14	MESSAGE ERROR MASK (S10)
13	SERVICE REQUEST BIT MASK (S08)
12	SUBSYS BUSY BIT MASK (S03)
11	SUBSYS FLAG BIT MASK (S02)
10	TERMINAL FLAG BIT MASK (S00)
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/B*
6	OFF LINE SELF TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-TO-RT FORMAT

Note: Bits 14-8, 4, and 3 are applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, are logic "1." If these two conditions are **not** met, the ACE BC utilizes its nonexpanded BC Control Word. The nonexpanded BC Control Word consists of bits 7, 6, 5, 2, 1, and 0 only.

With the nonexpanded BC Control Word, a "Status Set" condition indicates either a non-matching RT Address field **or** if **ANY** of the 8 non-Reserved RT Status bits are set. An exception is that for the Broadcast Command Received bit, a "Status Set" condition will occur if the value of the Broadcast Command Received bit in the RT Status Word is **different** than the value of the MASK BROADCAST bit.

When the expanded BC Control Word option is used, a "Status Set" condition indicates a non-matching RT Address field **or** that one or more of the RT Status Word bits, **in which the respective MASK bit(s) in the BC Control Word has been programmed to logic "0,"** is set (logic "1") in the received RT Status Word. When the Expanded BC Control Word option is used, the value of received RT Status Word bits for which the respective MASK bit is programmed for logic "1" becomes "don't care," in terms of affecting a "Status Set" condition.

MESSAGE ERROR MASK: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If MESSAGE ERROR MASK is logic "0," a Status Set condition will occur if the Message Error bit is logic "1" in the received RT Status Word. If MESSAGE ERROR MASK is logic "1," the value of the Message Error bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

SERVICE REQUEST MASK: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If SERVICE REQUEST MASK is logic "0," a Status Set condition will occur if the Service Request bit is logic "1" in the received RT Status Word. If SERVICE REQUEST MASK is logic "1," the value of the Service Request bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

BUSY MASK: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If BUSY MASK is logic "0," a Status Set condition will occur if the Busy bit is logic "1" in the received RT Status Word. If BUSY MASK is logic "1," the value of the Busy bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

SUBSYSTEM FLAG MASK: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If SUBSYSTEM FLAG MASK is logic "0," a Status Set condition will occur if the Subsystem Flag bit is logic "1" in the received RT Status Word. If SUBSYSTEM FLAG MASK is logic "1," the value of the Subsystem Flag bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

TERMINAL FLAG MASK: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If TERMINAL FLAG MASK is logic "0," a Status Set condition will occur if the Terminal Flag bit is logic "1" in the received RT Status Word. If TERMINAL FLAG MASK is logic "1," the value of the Terminal Flag bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

RESERVED BITS MASK: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If RESERVED MASK is logic "0," a Status Set condition will occur if the one or more of the 3 Reserved bits are logic "1" in the received RT Status Word. If RESERVED BITS MASK is logic "1," the value of the 3 Reserved bits in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

RETRY ENABLED: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If RETRY ENABLED is logic "0," the message will **not** be retried. If RETRY ENABLED, bit 4 of Configuration Register #1, is logic "1" **and** RETRY ENABLED is logic "1," a message will be retried as the result of a response timeout or format error condition.

If RETRY ENABLED, bit 4 of Configuration Register #1, is logic "1" **and** RETRY IF 1553A AND MESSAGE ERROR, bit 10 of Configuration Register #4 is logic "1" **and** 1553 A/B* SELECT, bit 3 of the BC Control Word, is logic "1" **and** RETRY ENABLED is logic "1," the ACE BC will attempt a message retry as the result of the Message Error bit being set in the RT Status Word.

If RETRY ENABLED, bit 4 of Configuration Register #1, is logic "1" **and** RETRY IF STATUS SET, bit 9 of Configuration Register #4 is logic "1" **and** RETRY ENABLED is logic "1," the ACE BC will attempt a message retry as the result of a "Status Set" condition in the received RT Status Word. A "Status Set" condition indicates either a nonmatching RT Address field **or** that one or more of the RT Status Word bits, **in which the respective MASK bit(s) in the BC Control Word has been programmed to logic "0,"** is set in the received RT Status Word. When the expanded BC Control Word option is used, the value of received RT Status Word bits for which the respective MASK bit is programmed for logic "1" becomes "don't care," in terms of affecting a "Status Set" condition.

The number of retry attempts is specified by DOUBLE/SINGLE* RETRY, bit 3 of Configuration Register #1: one retry if DOUBLE/SINGLE* RETRY is logic "0," two retries if DOUBLE/SINGLE* RETRY is logic "1." The channel selection (same or alternate) for the first and second retry attempts is specified by bits 8 and 7 of Configuration Register #4.

BUS CHANNEL A/B*: Selects whether the message will be processed on Channel A or Channel B. If the bit is logic "1," the message will be processed on Channel A; if the bit is logic "0," the message will be processed on Channel B.

OFF-LINE SELF-TEST: If this bit is set, it enables the off-line self-test for the respective message. In an off-line self-test message, the 1553 transmitter is inhibited; there is no activity on the external 1553 bus. The off-line self-test exercises the digital protocol portion of the ACE by routing the output of the Manchester II serial encoder directly to the decoder input of the selected bus channel. After the message has been processed, the user can determine the success or failure of the off-line self-test by reading the Loopback Word and the LOOP TEST FAIL bit of the Block Status Word.

MASK BROADCAST: If BROADCAST MASK ENABLED/XOR*, bit 11 of Configuration Register #4, is logic "0" **and** MASK BROADCAST is logic "1," the "expected value" of the Broadcast Command Received bit becomes 1, rather than 0. That is, a value of logic "**0**" (not logic "1") for the Broadcast Command Received bit in the received RT Status Word will result in a "Status Set" condition.
If ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1" **and** BROADCAST MASK

ENA/XOR* (bit 11 of Configuration Register #4) is programmed to logic "1," MASK BROADCAST is used as a mask bit, rather than performing an "XOR" operation with the Broadcast Received Status Word bit. In this instance, a Status Set condition arising from the Broadcast Command Received RT Status bit occurs when MASK BROADCAST is logic "0" and the Broadcast Command Received RT Status Word bit is logic "1." If BROADCAST MASK ENABLED/XOR* is logic "1" **and** MASK BROADCAST is logic "1," the value of the Broadcast Command Received bit in the received RT Status Word becomes "don't care" in affecting a "Status Set" condition.

EOM INTERRUPT ENABLE: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If RT/BC MESSAGE INTERRUPT, bit 4 of the Interrupt Mask Register is set, setting EOM INTERRUPT ENABLE to logic "1" will result in an Interrupt Request at the end of the current message.

1553 A/B* SELECT: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If 1553 A/B* SELECT is programmed to logic "0," the ACE BC verifies the validity of the RT response in accordance with MIL-STD-1553B. That is, it anticipates that an RT will respond to mode code commands with a T/R* bit of logic "1" and an MSB of the Mode Code field (bit 4) of logic "1" with a Status Word followed by a single Data Word. In addition, for an anticipated "1553B" response, assuming that RETRY IF STATUS SET, bit 9 of Configuration Register #4, is logic "0," the ACE BC will **not** attempt a message retry as the result of the Message Error bit being set in the RT Status Word.

If 1553 A/B* SELECT is programmed to logic "1," the ACE BC verifies the validity of the RT response in accordance with MIL-STD-1553A. That is, it anticipates that an RT will respond to mode code commands with a T/R* bit of logic "1" and an MSB of the Mode Code field (bit 4) of logic "1" with a Status Word only and no Data Word. In addition, if RETRY ENABLED, bit 4 of Configuration Register #1, is logic "1," **and** RETRY IF 1553A AND MESSAGE ERROR, bit 10 of Configuration Register #4 is logic "1," **and** RETRY ENABLED, bit 8 of the BC Control Word is logic "1," **and** 1553 A/B* SELECT is logic "1," the ACE BC **will** attempt a message retry as the result of the Message Error bit being set in the RT Status Word.

MODE CODE, BROADCAST, RT-TO-RT: Selects MIL-STD-1553B message format as follows:

BIT 2 MODE CODE	BIT 1 BROADCAST	BIT 0 RT-TO-RT	MESSAGE FORMAT
0	0	0	BC-to-RT (if T/R* bit = 0) **or** RT-to-BC (if T/R* bit = 1)
0	0	1	RT-to-RT
0	1	0	Broadcast
0	1	1	RT-to-RTs (Broadcast)
1	0	0	Mode Code
1	0	1	NOT USED

1	1	0	Broadcast Mode Code
1	1	1	NOT USED

The next word in RAM after the BC Control Word is the MIL-STD-1553B Command Word (for an RT-to-RT or RT-to-Broadcast transfer, it is the first of two Command Words). This word is read by the 1553 protocol logic and transmitted on the 1553 bus. The (first) Command Word is possibly followed by a second Command Word or Data Words to be read from RAM and transmitted. The location in RAM after the **last** transmitted word is reserved for the Loopback Word. Subsequent locations in the shared RAM are reserved for Status and possibly Data Words anticipated to be received from the responding RT(s). Assuming that the RT responds before a BC response timeout occurs, these word(s) are stored in the allocated locations in the shared RAM. If the Loopback test passes, and the RT responds before the BC Response Timer times out with a "Correct" RT Status Word (correct RT address and the "expected value" for the lower 11 bits), followed by the correct number of valid Data Words, the Block Status Word will be written to indicate "End of Message, No Errors" during the BC End-of-Message (EOM) sequence. Note that for an RT-to-RT transfer, the ACE BC checks the Status Words from **both** the transmitting and receiving RTs.

DESCRIPTOR STACK

The host processor may determine the status of individual messages by reading the first four locations of the respective descriptor block. The first location within the descriptor block contains the Block Status Word. In BC mode, the Block Status Word contains information relating to whether the message is in progress or has been completed, which bus channel it was transmitted on and whether there were any errors in the message. The bit map and bit descriptions for the BC Block Status Word are indicated below.

TABLE 40. BC MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

Note: If a message is retried, the bits of the Block Status Word reflect the result of latest message retry.

END-OF-MESSAGE (EOM): Set at the completion of a BC message, regardless of whether or not there were any errors in the message.

START-OF-MESSAGE (SOM): Set at the start of a BC message and cleared at the end of the message.

CHANNEL B/A*: This bit will be low if the message was processed on Channel A or high if the message was processed on Channel B.

ERROR FLAG: If this bit is high and one or more of bits 10, 9, and/or 8 are high, this indicates one or more of the following errors occurred in the message: Format Error, Response Timeout and/or Loop Test Fail.

STATUS SET: If set, indicates that in one of the lower 11 bits the RT Status Word received from a responding RT contained an unexpected bit value. The expected value for these 11 bits is normally zero (0), with one exception: if ENHANCED MODE ENABLE (bit 15 of Configuration Register #3) is logic "0" **or** BROADCAST MASK ENABLED/XOR* (bit 11 of Configuration Register #4) is logic "0" **and** the MASK BROADCAST bit of the message's BC Control Word is logic "1," the expected value of the Broadcast Command Received bit becomes 1, rather than 0. The value of STATUS SET is **not** affected by the values

of the other mask bits (bits 14 through 9) of the message's BC Control Word.

FORMAT ERROR: If set, indicates that the received portion of a message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the RT's status word received from a responding RT contained an incorrect RT address field.

RESPONSE TIMEOUT: If set, indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The ACE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the midbit crossing of the parity bit to the midsync crossing of the RT Status Word. In the non-ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "0"), the value of the BC Response Timeout is 17.5 to 19.5 µs. If ENHANCED MODE ENABLED is logic 1, the value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 µs (±1 µs) by means of bits 10 and 9 of Configuration Register #5.

LOOP TEST FAIL: A loopback test is performed on the transmitted portion of every message in BC mode. A validity check is performed on the received version of every word transmitted by the ACE BC. In addition, a bit-by-bit comparison is performed on the last word transmitted by the BC for each message. If either the received version of any transmitted word is invalid (sync, encoding, bit count, and/or parity error) and/or the received version of the last word transmitted by the ACE BC does not match the transmitted version, the LOOP TEST FAIL bit will be set.

It should be noted that in the non-ENHANCED mode (if ENHANCED MODE ENABLED, bit 15 of Configuration Register # 3, is logic "0"), bits 7 through 0 will always return logic "1."

MASKED STATUS SET: Applicable for ENHANCED Mode only if ENHANCED MODE ENABLED (bit 15 of Configuration Register #3, programmed to logic "1") **and** EXPANDED BC CONTROL WORD ENABLE (bit 12 of Configuration Register #4) is programmed to logic "1." It will be set if one or both of the following conditions occur: (1) If one (or more) of the Status Mask bits (14 through 9) in the BC Control Word is logic "0" **and** the corresponding bit(s) is (are) set (logic "1") in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0," any or all of the 3 Reserved Status bits being set will result in a MASKED STATUS SET condition; **and/or** (2) If BROADCAST MASK ENABLED/XOR* (bit 11 of Configuration Register #4) is logic "1" **and** the MASK BROADCAST bit of the message's BC Control Word is logic "0" **and** the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1." Refer to TABLE 43.

RETRY COUNT 1 and RETRY COUNT 0: Applicable for ENHANCED Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, programmed to logic "1") **and** EXPANDED BC CONTROL WORD (bit 12 of Configuration Register #4) set to logic "1," **and** the RETRY ENABLED bit (bit 4 of Configuration Register #1) is set to logic "1," **and** the RETRY ENABLED bit (bit 8) of the respective BC Control Word is set to logic "1." Also affected by the RETRY, IF 1553A and MESSAGE ERROR bit (bit 10) and RETRY IF STATUS SET bit (bit 9) of Configuration Register #4 and the 1553 A/B* SELECT bit (bit 3) of the BC Control Word. The number of times that a message is retried is

delineated by these two bits as follows.

RETRY COUNT 1 (bit 6)	RETRY COUNT 0 (bit 5)	Number of Retries
0	0	0
0	1	1
1	0	2
1	1	N/A

GOOD DATA BLOCK TRANSFER: Applicable for ENHANCED Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1"). Set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is **always** logic "0" following a BC-to-RT transfer, a mode code with data, or a mode code without data. The Loop Test has **no effect** on GOOD DATA BLOCK TRANSFER.

WRONG STATUS ADDRESS/NO GAP: Applicable for ENHANCED Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1"). This bit is set if either or both of the following occur: (1) The RT address field of a responding RT does not match the RT address in the Command Word; and/or (2) If the GAP CHECK ENABLED bit (bit 8) of Configuration Register #5 is set to logic "1" **and** a responding RT responds with a response time of less than 4 µs, per MIL-STD-1553B (mid-parity bit to mid-sync); i.e., less than 2 µs dead time.

WORD COUNT ERROR: Applicable for ENHANCED Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1"). Applicable for an RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. If set, indicates that a responding RT did not transmit the correct number of Data Words. Will always be logic "0" following a BC-to-RT transfer, receive mode code message, or transmit mode code without data message.

INCORRECT SYNC TYPE: Applicable for ENHANCED Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1"). If set, indicates that a responding RT responded with a Data sync in a Status Word and/or a Command/Status sync in a Data Word.

INVALID WORD: Applicable for ENHANCED Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1"). Indicates an RT responded with one or more words containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

The second location of the BC Message Block Description contains the Time Tag Word. The current value of the internal Time Tag Register is written to the Time Tag Word during both the BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences.
The third location of the BC Message Block Descriptor is RESERVED in non-ENHANCED BC mode. This location contains the value of the programmed message gap time if the ACE is in ENHANCED MODE **and** MESSAGE GAP TIME ENABLED (bit #5 of Configuration Register #1) is programmed to logic "1."

The fourth location is used to store the MESSAGE BLOCK ADDRESS Word. The MESSAGE BLOCK ADDRESS must be loaded by the host processor **before** the message is processed. It is then used as a pointer by the ACE memory management logic for accessing the start of the respective Message Block.

The two other fixed locations in the shared RAM address space that must be initialized by the host processor for nonenhanced BC mode are the Stack Pointer and Message Counter locations. The Stack Pointers are located in address locations 0100 (for Area A) and 0104 (for Area B). The Stack Pointer should be initialized to point to the first word of the Message Block Descriptor (Block Status Word) for the first message to be processed. The Message Counters are located in addresses 0101 (for Area A) and 0105 (for Area B). The Active Area Message Counter must be preloaded by the host processor with the **ones complement** of the number of messages to be processed (i.e. FFFE represents a message count of 1). The Message Counter is incremented by one following each BC message processed.

Note that if the ACE BC is programmed for FRAME AUTO-REPEAT operation, the **initial** Stack Pointer and initial Message Counter locations, rather than the Stack Pointer and Message Counter locations must be initialized.

BC Message Gap Time

The ACE contains a programmable BC message gap time with 1 µS resolution to a maximum of 65535 µS. The BC message gap time is defined as the time from the start of the current message to the start of the next message (refer to FIGURE 9). The message gap timer is enabled if ENHANCED MODE ENABLE bit (bit 15 in Configuration Register #3) is set to logic "1" **and** MESSAGE GAP TIMER ENABLE (bit 5 in Configuration Register #1) is programmed to logic "1."

The value of the programmed message gap time is stored in the third word location of the BC descriptor stack entry. If the message gap timer is disabled, this location in the descriptor stack is not used. Specifying a message gap time value that is less than the time of the current message will cause the next message to start **immediately** following the end of the current message. In this case, the message gap time defaults to the message time plus the minimum intermessage gap time, approximately 8 to 11 µS (measured from the end of the previous message to the beginning of the next message). This feature allows the BC to implement minor frame cycle times without host intervention.

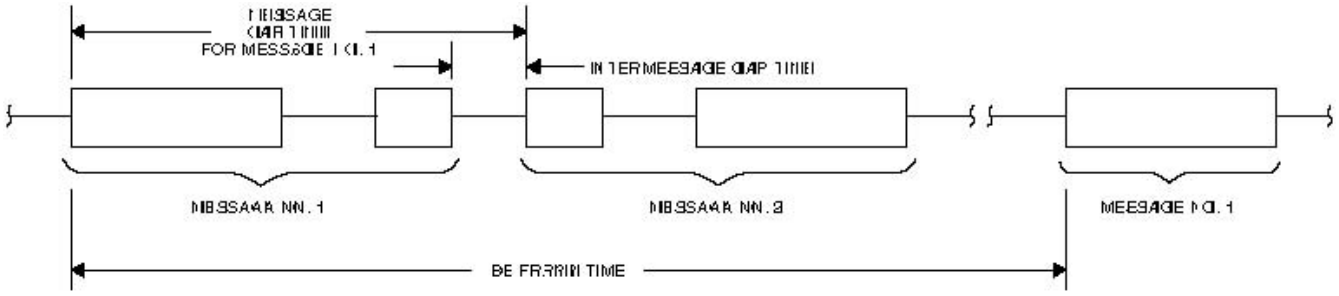


FIGURE 9. BC MESSAGE GAP TIME

BC Frame Auto-Repeat

The ACE has the capability to define a BC frame that can run continuously based on an internal frame timer, an external hardware trigger or under host processor control. The BC auto-repeat feature is available in ENHANCED BC Mode, that is, if the ENHANCED MODE ENABLE bit (bit 15 in Configuration Register #3) is programmed to logic "1."

Enabling the BC Frame Auto-Repeat mode requires that the BC Stack Pointer and BC Message Count values must be stored in the INITIAL BC STACK POINTER and INITIAL BC MESSAGE COUNTER fixed locations in RAM (word locations 0101 and 0103 for Area A or word locations 0106 and 0107 for Area B) rather than in the BC STACK POINTER and BC MESSAGE COUNT fixed locations in RAM (word locations 100 and 101 for area A or word locations 0104 and 0105 for Area B).

Upon receiving the BC trigger condition (software, internal, or external) the ACE will take the values in the INITIAL BC STACK POINTER and INITIAL BC MESSAGE COUNTER locations and copy them into the current (as specified by CURRENT AREA B/A*) BC STACK POINTER and BC MESSAGE COUNT locations, then start processing the BC frame. Two separate locations for these values are needed because the ACE will modify the STACK POINTER and MESSAGE COUNT as the current BC frame is processed.

In the Frame Auto-Repeat mode, the frame time is programmable in increments of 100 µs/LSB by means of the BC Frame Time/RT Last Command/MT Trigger Register (register address 01101). This provides a range of programmable BC Frame Times up to a maximum value of 6.5535 seconds.

Minor and Major Frames

In many systems, the BC is required to process messages to the various RTs/subaddresses at a variety of frequencies. For example, some messages may be required to be transmitted at a 5 Hz rate, others at a 10 Hz rate, 20 Hz rate,...100Hz, etc. A common mechanism for supporting varying data rates in a 1553 system is the use of minor and major frames, as illustrated in FIGURE 10.

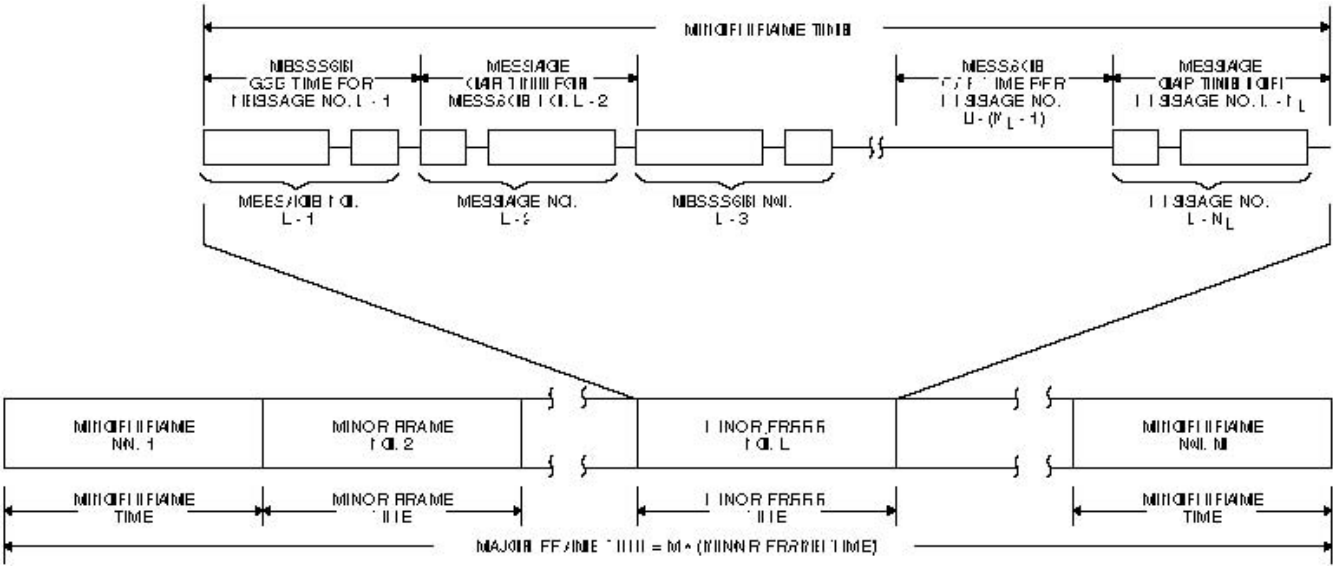


FIGURE 10. BC MAJOR AND MINOR FRAMES

In the figure, the message scenario is organized into minor frames. A major frame is comprised of multiple minor frames. If the minor frame time is assumed to be 10 ms, message rates of up to 100 Hz may be supported. That is, a 100 Hz message will appear in **every** minor frame, a 50 Hz message in every other minor frame, ... while a 1 Hz message will appear once every 100 minor frames.

Using the ACE BC architecture, minor frame structures may be composed by means of the message gap-time feature. The ACE intermessage gap-time field specifies the time from the start of the current message to the start of the subsequent message. By strategic use of the message gap times, it is possible to formulate minor frames. The minor frame time is the sum of all message gap times within a minor frame. All minor frame times are identical (e.g., 10 ms).

If the time required to process a message is longer than the programmed value of the message's message gap time, the message (including any retries) **will be processed to completion**. The resultant intermessage gap time prior to the next message will be approximately 8 to 11 ms. If automatic retries are used, it is recommended that the intermessage gap times allow time for a single or double retry, if possible. This will allow messages to be retried without overrunning the minor frame time.

The BC major frame is comprised of a group of minor frames. To implement a major frame, the frame auto-repeat mode should be used. In this way, the ACE frame time becomes the system major frame time.

BC Start Sequence and Options

The ACE offers several options for BC frame control. The ACE BC can be programmed to process either a single BC frame or repetitive frames.

The BC start sequence configuration is configured by means of bits 8, 7, and 6 of Configuration Register #1. Refer to TABLE 41. If FRAME AUTO-REPEAT (bit 8 of Configuration Register #1) is logic "0" **or** if INTERNAL TRIGGER ENABLED (bit 6 of Configuration Register #1) is logic "0," the ACE BC will process **only a single message frame.** A message frame consists of from 1 to 512 messages, in accordance with the programmed value of the Message Count or Initial Message Count location. (See TABLE 41.)

If FRAME AUTO-REPEAT is logic "1" **and** INTERNAL TRIGGER ENABLED is logic "1," then the BC is programmed for automatic repetitive frame operation. The timing diagram of FIGURE 10 illustrates the definition of the ACE's BC frame time for the frame auto-repeat mode. Note that the BC frame is defined as the time from the beginning of the first message ("message #1") for one frame to the corresponding time in the subsequent frame.

The source of the values for Stack Pointer and Message Count is programmed by means of FRAME AUTO-REPEAT. If FRAME AUTO-REPEAT is logic "0," the ACE BC protocol logic reads the active area Stack Pointer and Message Counter locations. If FRAME AUTO-REPEAT is logic "1," the BC protocol logic reads the addresses for the **Initial** Stack Pointer and **Initial** Message Counter. In the FRAME AUTO-REPEAT mode, the Stack Pointer and Message Counter locations are loaded at the beginning of every frame (from the values stored in the respective "Initial" locations) and incremented following every message processed.

For single-frame operation, or for starting the first frame for auto-repeat operation, the first message may always be initiated by means of a software BC START operation; that is, by writing 0002 (hex) to the Start/Reset Register.

TABLE 41 summarizes the various BC START sequences.

TABLE 41. BC START SEQUENCES

FRAME AUTO-REPEAT (bit 8 of Configuration Register #1)	INTERNAL TRIGGER ENABLED (bit 6 of Configuration Register #1)	BC START (/REPEAT) SEQUENCE
0	X	Single frame; start by software BC Start command; Stack Pointer and Message Count must be loaded into locations 100, 101 (or 104, 105) prior to each frame.
1	0	Single frame; start by software BC Start command; Stack Pointer and Message Count must be loaded into locations 102, 103 (or 106, 107) one time.
1	1	Repeat frame; start first frame by software BC Start command; frame repeats in accordance with internal frame timer; Stack Pointer and Message Count must be loaded into locations 102, 103 (or 106, 107) one time.

BC Interrupts

The ACE BC offers an array of conditions that can result in interrupt requests to the host CPU. These can be selected by means of the Interrupt Mask Register. It should be noted that if ENHANCED INTERRUPTS are used, the host may determine that various events have occurred by polling the Interrupt Status Register. Using ENHANCED INTERRUPTS, the various bits in the Interrupt Status Register may become set to indicate the occurrence of conditions, regardless of the programming of the Interrupt Mask Register. The use of the eight possible BC interrupt conditions is summarized as follows:

BC_END_OF_FRAME: For most BC applications, it is desirable to issue an interrupt request following the completion of a multimessage frame of messages. This may be enabled by setting the BC_END_OF_FRAME bit in the Interrupt Mask Register. In both single frame and frame auto-repeat modes, this interrupt will occur following the completion of each frame of messages.

END_OF_MESSAGE: This interrupt will occur at the end of every message. For a retried message, the interrupt will occur after the **last** retry.

BC MESSAGE INTERRUPT: Interrupts may be generated at the end of **selected** messages in ENHANCED BC Mode. This is enabled by configuring the ACE for ENHANCED BC Mode by programming

ENHANCED MODE (bit 15 in Configuration Register #3) to logic "1," **and** EXPANDED BC CONTROL WORD ENABLED (bit 12 of Configuration Register #4) for logic "1," **and** by setting the BC MESSAGE INTERRUPT bit (bit 4 in the Interrupt Mask Register) to logic "1." In this mode, an EOM interrupt will be generated if the EOM INTERRUPT ENABLE bit, bit 4 in the BC Control Word, is programmed to logic "1."

FORMAT ERROR: This interrupt request will be issued following any message containing an invalid word or wrong number of words.

RETRY: This interrupt will occur after the **last** retry attempt (whether successful or unsuccessful) for any message that is retried.

STATUS SET: This interrupt will be issued following a message with either an incorrect RT address in a Status Word and/or one or more bits set to logic "1" in the RT Status Word. In ENHANCED BC mode, Status Word bits that have been masked by the respective bits in the BC Control Word **will not** result in a STATUS SET interrupt.

COMMAND STACK ROLLOVER: This interrupt request occurs when the BC Command Stack rolls over at a predefined boundary in the ACE address space. This boundary is programmable from among 256, 512, 1024, or 2048 words.

TIME TAG ROLLOVER: This interrupt occurs when the value of the ACE's Time Tag Register counter rolls over from FFFF to 0000.

OTHER BC FUNCTIONS

Automatic Retries

The ACE BC will perform automatic retries based on no response timeout, a message error, the Message Error Status Word bit set by a MIL-STD-1553A RT, or a Status Set condition. Retries can only be enabled in the ENHANCED BC mode. This requires the ENHANCED MODE ENABLE bit (bit 15 in Configuration Register #3) to be set to logic "1." Retries are then enabled for individual messages by setting the RETRY ENABLE bit (bit 8) in the respective BC Control Word(s).

Retry Conditions. A no response timeout or a message format error will always cause a retry if retry is enabled for the current message. A retry on a "status set" condition will only occur if the RETRY IF STATUS SET bit (bit 9 in Configuration Register #4) is set to logic "1." The status set condition is based on the status mask bits in the BC Control Word. A message format error condition occurs when the RT address in the status response does not match the RT address in the command word, there is an invalid word (parity, Manchester error, etc.), there is an incorrect sync type (for both status and data words), or there is a low or high word count.

A retry will also occur if the Message Error bit in the status word response is set to logic "1" **and** the 1553 A/B* SELECT bit (bit 3 in the BC Control Word) is set to logic "1" (1553A mode) **and** the RETRY IF - 1553A AND MESSAGE ERROR bit (bit 10 in Configuration Register #5) is set to logic "1." The reason this retry is enabled for 1553A mode only is that in MIL-STD-1553B mode, the Message Error bit (S10) is used only to indicate illegal commands. MIL-STD-1553A, on the other hand, uses the Message Error bit as a means for the RT to indicate to the BC that it received a valid command, but one of the associated Data Words had a parity, Manchester encoding, or bit count error (a 1553B RT would not respond at all to this message).

Number of Retries. The ACE will attempt a maximum of two retries before it indicates a no response timeout or other retry condition. The maximum number of retries that will be attempted for any particular message is programmable by means of DOUBLE/SINGLE* RETRY, bit 3 of Configuration Register #1. If DOUBLE/SINGLE* RETRY is logic "0," one retry will be attempted; if DOUBLE/SINGLE* RETRY is logic "1," a maximum of two retries will be attempted.

Retry Channel Selection. The bus that the first retry is performed on (alternate or same, with respect to the original bus channel) is selected by the programming of the 1ST RETRY ALT/SAME* bit (bit 8 in Configuration Register #4) to logic "0" (for same bus) or to logic "1" (for alternate bus). The bus that the second retry is performed on is selected by programming the 2ND RETRY ALT/SAME* bit (bit 7 in Configuration Register #4) to logic "0" (for same bus) or to logic "1" (for alternate bus). This allows for six possible retry scenarios: same, alternate, same/same, same/alternate, alternate/same, alternate/alternate.

Retry Block Status Word Bits. The End-of-Message for a retried message occurs after the completion of message retries, not after the initial failed message, or after an unsuccessful first of two retries. The ACE

writes the Block Status Word to shared RAM during the End-of-Message transfer sequence. RETRY COUNT 1 (bit 5 in the BC Block Status Word,) indicates that one retry occurred when it is set to logic "1." A logic "1" in the RETRY COUNT 2 bit (bit 6 in the Block Status Word) indicates that two retries were attempted. A logic "0" in both RETRY COUNT 1 and RETRY COUNT 2 indicates that no retries occurred. If the second retry fails, the message is aborted and the cause of the failure is stored in the Block Status Word (no response timeout, format error, Status Set, etc).

Retry Interrupts. If enabled by the Interrupt Mask Register, the EOM and/or BC RETRY interrupt requests will be issued **AFTER** the completion of the message retries, for either **an unsuccessful retry or a successful retry.**

If a retry is enabled for a particular message, the retry **will** be attempted even if one or more of the following bits of Configuration Register #1 (bits 12 through 9) are set to logic "1": MESSAGE STOP-ON-ERROR, FRAME STOP-ON-ERROR, STATUS SET STOP-ON-MESSAGE, and STATUS SET STOP-ON-FRAME. If the retry(ies) is(are) not successful, the processing of BC messages will stop at the end of the current message or message frame. However, the processing of subsequent BC messages within a frame and/or the processing of subsequent BC frames **will continue** if a failed message is successfully retried.

BC Response Timeout

MIL-STD-1553B defines RT response time as the delay from the mid-parity zero crossing of the parity bit of the last word received from the BC (or another RT) to the mid-sync zero crossing of the RT's Status Word. In accordance with this definition, the -1553B standard specifies that
an RT must respond within 12 µs and that a BC must wait a **minimum** of 14 µs before determining that an RT "no response" has occurred.

The response timeout value for the ACE bus controller is software programmable. For the non-ENHANCED MODE (bit 15 of Configuration Register #3 is logic "0"), the value of the BC response timeout timer defaults to a nominal value of 18.5 µs. In the ENHANCED MODE, the ACE supports the use of long buses and/or repeaters by allowing the nominal value of the BC timeout to be selected from among 18.5, 22.5, 50.5, and 130 µs by means of bits 10 and 9 (RESPONSE TIMEOUT 1, 0) of Configuration Register #5. Refer to TABLE 42.

TABLE 42. BC RESPONSE TIMEOUT SELECT

BIT 10 RESPONSE TIMEOUT SELECT 1	BIT 9 RESPONSE TIMEOUT SELECT 0	RESPONSE TIMEOUT TIME VALUE (µs)
0	0	18.5*
0	1	22.5
1	0	50.5
1	1	130

*Note: Default value for non-ENHANCED mode is 18.5 µs

BC Status Word Masking

The BC mode of the ACE has the capability of masking selected Status Word bits for individual messages in a BC frame while ENHANCED MODE ENABLE (bit 15 in Configuration Register #3) **and** EXPANDED BC CONTROL WORD ENABLE (bit 12 of Configuration Register #4) are programmed to logic "1." In the non-ENHANCED mode **or** if EXPANDED BC CONTROL WORD ENABLE is logic "0," only bits 7, 6, 5, 2, 1, and 0 of the BC Control Word are operative. In this case, the only operative "Status Mask" bit in the BC Control Word is MASK BROADCAST (bit 5). If EXPANDED BC CONTROL WORD ENABLE is logic "1," **all 15** bits of the BC Control Word (bits 14 through 0), including **all** of the "Status Mask" bits (bits 14 through 9, and bit 6) are operative.

The Status Word Mask bits, in the BC Control Word, control which bits in the responding RT Status Word(s) will cause a "Status Set" condition to occur. A "Status Set" condition will cause

a bid to be set in the Block Status Word, can cause an interrupt, can halt the BC after the current message or at the end of the current BC frame, and/or initiate an automatic retry.

A logic **"1"** in the proper bit position in the BC Control Word will cause the ACE to **ignore ("don't care")** the respective RT Status Word Bit. Any designated subset of the following bits may be enabled in determining a Status Set condition: Illegal Bit (S10), Service Request Bit (S08), Subsystem Busy Bit (S03), Subsystem Flag Bit (S02), Terminal Flag Bit (S00) and/or the Reserved Bits (S09, S07-S05, S01). The Broadcast Bit (S04) can either be masked (ignored) or verified to be logic "0" or logic "1." If the corresponding mask bit is programmed to logic **"0,"** the bit **is included** in determining if a "Status Mask" condition occurs.

With the exception of the Broadcast Command Received Status Word bit, the effect of the ENHANCED MODE, EXPANDED BC CONTROL WORD ENABLE, the various "Status Mask" BC Control Word bits, and the value of the respective received RT Status Word on the "Masked Status Set" condition is summarized in TABLE 43.

TABLE 43. OPERATION OF STATUS WORD MASKING BITS
OTHER THAN BROADCAST COMMAND RECEIVED

ENHANCED MODE (bit 15 of Configuration Register #3)	EXPANDED BC CONTROL WORD ENABLED (bit 12 of Configuration Register #4)	"MASK" bit for the particular Status Word bit (in BC Control Word)	Value of the respective bit in Received RT Status Word	Masked Status Set Condition
0	X	X	X	No
O R				
X	0			
1	1	0	0	No
		0	1	Yes
		1	0	No
		1	1	No

The function of the Broadcast Mask Bit is determined by the value of the BRDCST MASK ENA/XOR* bit (bit 11 in Configuration Register #4). If the BRDCST MASK ENA/XOR* bit is programmed to logic "1," a value of logic "1" in the BC Control Word MASK BROADCAST bit (bit 5) will result in the Broadcast Command Received bit in the responding RT Status Word(s) to be ignored ("don't care"), while a logic "0" in the MASK BROADCAST bit will result in a STATUS SET condition, if the Broadcast Command Received bit in the RT Status Word is logic "1."

Programming BRDCST MASK ENA/XOR* to logic "O" will cause the ACE to compare the Broadcast Bit in the received RT Status Word to the value in the MASK BROADCAST BIT (bit 5 in the BC Control Word). In the case that they **do not match,** a "Status Set" condition will be generated. The operation of the BRDCST MASK ENA/XOR* and MASK BROADCAST bits is summarized in TABLE 44.

TABLE 44. OPERATION OF STATUS WORD MASKING BITS
(FOR BROADCAST COMMAND RECEIVED STATUS WORD BIT)

ENHANCED MODE (bit 15 of	BROADCAST MASK ENABLED/XOR* (bit 11	EXPANDED BC CONTROL WORD ENABLED (bit 12 of	MASK BROADCAST (bit 5 of BC	Value of "Broadcast Command Received"	Masked Status

Configuration Register #3)	Configuration Register #4)	Configuration Register #4)	Control Words	bit in Received RT Status Word	Set Condition
0	X	X	0	0	No
OR			0	1	Yes
1	0	X	1	0	Yes
			1	1	No
1	1	X	0	0	No
			0	1	Yes
			1	0	No
			1	1	No

The Block Status Word contains two bits describing the status set condition. The first is the STATUS SET bit (bit 11). This bit will be set to logic "1" if **any** of the bits in the status response are logic "1" regardless of the status mask. STATUS SET 2 (bit 7) will only be set to logic "1" if a bit in the Status Word response is set **and** that bit is not masked by the status mask in the BC Control Word (with the exception of the Broadcast Command Received bit "expected value" option, as described above).

An interrupt will be generated for a Status Set condition (based on the status mask criteria) in the ENHANCED BC Mode, if the BC STATUS SET bit (bit 1 in the Interrupt Status Mask) is set to logic "1." The interrupt will occur at the end of the current message (EOM), not immediately following the receipt of the Status Word (in the case of a transmit command).

A Status Set condition, in the ENHANCED BC Mode, can cause the bus controller to halt in one of two ways. First, if the MESSAGE STOP-ON-ERROR bit (bit 12 in Configuration Register #1) is set to logic "1," the BC will halt the current frame upon completion of the current message. In the FRAME AUTO-REPEAT mode, if FRAME STOP-ON-ERROR (bit 11 in Configuration Register #1) is set to logic "1," the BC will halt the current frame upon completion of the last message in the frame.

BC SOFTWARE INITIALIZATION SEQUENCE

The following software sequence is typical of the steps the host CPU should perform following power turn-on to configure the ACE for BC operation. For most applications, many of the steps indicated may be skipped.

(1) Perform a software reset, by writing a value of 0001 (hex) to the Start/Reset Register.

(2) If any of the ENHANCED mode functions (eg., use of programmable retries, message gaps, expanded BC Control Word, etc.) are to be used, invoke the ACE's ENHANCED MODE by writing a value of 8000 (hex) to Configuration Register #3.

(3) Initialize the Interrupt Mask Register. For most BC applications, the BC END-OF- FRAME interrupt should be enabled. The END-OF-MESSAGE (EOM) bit causes an interrupt request to be issued following the end of **every** completed message. BC CONTROL WORD interrupt allows interrupt requests to be issued following completion of **selected** (by means of the BC Control Word) messages. BC RETRY will result in an interrupt **after** a message is retried (either successfully or, unsuccessfully).

FORMAT ERROR will cause an interrupt request to be issued following any RT response containing either a word error (sync or Manchester encoding, bit count, or parity error) or a high or low word count error. A STATUS SET interrupt results from one of three conditions: (1) A nonmatching RT address in the Status Word from a responding RT; (2) If EXPANDED BC CONTROL WORD is not enabled, one or more of the 8 nonreserved Status Word bits is logic "1"; or (3) If EXPANDED BC CONTROL WORD is enabled, and for one or more of the RT Status Word bits the respective Status Mask bit in the BC Control Word is programmed for "care" (logic "0") **and** the value of the received RT Status Word bit is logic "1."

(4) Initialize Configuration Register #1. Bits 15 and 14 must both be initialized to logic "0" to configure the ACE for BC mode. CURRENT AREA B/A* should be designated. MESSAGE STOP-ON-ERROR, FRAME-STOP-ON-ERROR, MESSAGE-STOP-ON-STATUS SET, and FRAME-STOP-ON-STATUS SET should be selected, if desired. The STOP-ON-ERROR bits enable a "graceful halt" (at the **end** of the current message or frame) in the case of a response timeout, format error or loop test failure. The STOP-ON-STATUS SET bits enable a "graceful halt" condition for a "Status Set" condition, as defined above. It should be noted that if a message retry is enabled for a particular message, the retry will be attempted **before** the "stop" takes place. That is, if the retry is successful, the message frame will **continue** (will not stop). If the retry (one or two retries) is unsuccessful, then the processing of messages will be aborted at the end of the current message or frame.

Regardless of the programming INTERNAL TRIGGER ENABLED, a BC frame may be initiated by means of a software BC START command. If it is desired to have the programmed BC frame repeat automatically (with no CPU intervention), it is necessary to program FRAME AUTO-REPEAT **and** INTERNAL TRIGGER to logic "1."

In order to control the BC message gap times using the third word of the BC Block Descriptor, MESSAGE GAP TIME ENABLED must be programmed to logic "1." If MESSAGE GAP TIME ENABLED is logic "0," the start-of-current message to start-of-subsequent message time will default such that the BC's intermessage gap time (as defined by MIL-STD-1553B) defaults to its minimum value of approximately 9 µs.

If message retries are to be enabled by means of bit 8 of the BC Control Words (RETRY ENABLED), it is necessary to program RETRY ENABLED to logic "1." If retries are enabled, the maximum number of retries for each message (either 1 or 2) is specified by means of DOUBLE/SINGLE* RETRY.

(5) Initialize Configuration Register #2. For BC mode, it is strongly recommended that 256-WORD BOUNDARIES DISABLED be set to logic "1" in order to make best use of the ACE's address space

for BC message blocks. LEVEL/PULSE* INTERRUPT should be initialized to logic "1" if the host CPU requires a level, rather than a pulse, type of interrupt request input signal. TIME-TAG RESOLUTION 2-0 should be programmed to initialize the resolution of the Time-Tag Register. The default resolution ("000") is 64 µs/LSB.

(6) Initialize Configuration Register #3. If any of the lower 15 bits of this register or any of the other ENHANCED mode features are to be used, ENHANCED MODE ENABLED (bit 15) must be maintained at logic "1" while writing to this register. The size of the Stack may be programmed by means of bits 14 and 13. The choices for the stack size are 256 words (default, for 64 BC messages), 512, 1024, and 2048 words (2048 messages).

(7) Initialize Configuration Register #4. In order to allow the use of bits 15-8, 4, and 3 of the BC Control Word, EXPANDED BC CONTROL WORD must be set to logic "1." This includes use of the Status Word Masking function, retries, 1553A/B selection, and interrupts on a message basis. BROADCAST MASK ENABLED/XOR* should be programmed to logic "1" if it is desired to use the "MASK BROADCAST BIT" bit (bit 5) of the BC Control Word as an actual mask, rather than to specify the anticipated value of the Broadcast Command Received bit in the RT Status Word.

RETRY IF -1553A AND MESSAGE ERROR should be set if it is desired to retry messages in which the 1553A/B* SELECT bit (bit 3) of the BC Control Word is logic "1" and the Message Error bit is logic "1" in the RT Status Word. RETRY IF STATUS SET should be set to logic "1" if it is desired to retry messages in which one or more of the "unmasked" Status Word bits is logic "1" in the RT Status Word. A Status Word bit is considered "unmasked" if the corresponding "MASK" bit in the BC Control Word has been programmed to logic "0."

If VALID BUSY/NO DATA and/or VALID MESSAGE ERROR/NO DATA is set to logic "1," an RT response will be considered valid if the BUSY (MESSAGE ERROR) bit(s) is set in the RT Status Word and there are no following Data Words. Otherwise, such an RT response will be considered invalid. Message validity affects the setting of the FORMAT ERROR bit in the Block Status Word, the issuing of interrupts, and message retries.

(8) Initialize Configuration Register #5. Ensure that CLK12 SELECT bit 15 is programmed to a logic "0".

EXPANDED ZERO-CROSSING should be programmed to logic "1" to expand the Manchester decoders' tolerance for zero crossing distortion by enabling sampling at a 32 MHz (or 24 MHz) rate. RESPONSE TIMEOUT SELECT 1-0 selects the time value for the BC response timeout from among 18.5 µs (default), 22.5, 50.5, or 130 µs. If GAP CHECK ENABLED is set to logic "1," the BC will verify for a minimum bus dead time of 2 µs prior to RT responses. If this gap time is violated, the BC will set the FORMAT

ERROR bit in the Block Status Word. As a result, an ERROR interrupt may be issued and/or the message may be retried.

(9) If desired, initialize the Time-Tag Register. It should be noted that the value of the Time-Tag Register may be reset to zero simultaneous with the BC Start by writing logic "1" to the TIME-TAG

RESET bit of the Start/Reset Register as part of step (15).

(10) If using the Frame Auto-Repeat mode (FRAME AUTO-REPEAT and INTERNAL TRIGGER ENABLED bits of Configuration Register #1 programmed to logic "1"), initialize the BC Frame Time Remaining Register. This register is programmable with a resolution of 100 µs/LSB.

(11) Load the starting location of the Stack into the active area Stack Pointer RAM location. If the Frame Auto-Repeat mode is to be used, the Initial Stack Pointer RAM location for the active area should also be loaded.

(12) Initialize the Active Area Stack. For the message descriptor for each message to be processed, the Message Block Address, providing the pointer to the first word of the respective BC message block (the BC Control Word) must be written by the CPU. If the Message Gap-Time feature is used, the Message Gap-Time word must also be written for each message. The resolution of the Message Gap-Time Word is 1 µs/LSB. The programmed value of the Message Gap-Time field represents the time from the **start** of the current message to the **start** of the subsequent message. If this time is less than the time required for the current message, the gap prior to the start of the subsequent message defaults to the minimum value of approximately 9 µs.

If it is desired to poll the stack during the processing of the BC frame, it is recommended that the values of the Block Status Words be initialized to zero by the host CPU.

(13) Load the BC Control, Command, and Data Words to be transmitted into the respective BC message blocks. Optionally, the locations of the anticipated Loopback Words should be loaded with a **different** bit pattern than the last word to be transmitted by the BC. The host processor must ensure that sufficient address locations are allocated after the last word to be transmitted to accommodate the Loopback Word and anticipated received Status and Data Words.

(14) The Active Area Message Count location should be loaded with the **ones complement** of the number of messages to be processed in the frame. If the Frame Auto-Repeat mode is to be used, the Initial Message Count RAM location for the active area should be loaded.

(15) A BC frame is initiated by writing a value of 0002 hex to the START/RESET REGISTER.

Servicing In-Progress or Completed BC Frames

The end of BC messages and frames may be determined by means of either polling or interrupt techniques.

There are several polling techniques that may be used. These involve bits in either Configuration Register #1 or the Interrupt Status Register. In addition, the active area Stack Pointer and Message Count Register may be polled. The Stack Pointer increments by four at the end of each BC message. At the end of a BC frame, it will point to **4 locations beyond (modulo the stack size)** the first word of the message block descriptor (the location of the Block Status Word), for the last message of the BC frame. The Message Counter increments by one at the end of each BC message. When the frame has been completed, the Message Count location will have a value of FFFF (hex).

In the ENHANCED BC mode, the lower three bits of Configuration Register #1 may be polled as a means of determining BC status. BC ENABLED (bit 2) will return logic "1" after a BC frame has been initiated (by either a BC START command or from an external trigger) and up to the time that a single frame has completed or repeat frames have been halted. BC ENABLED will then transition to logic "0."

BC FRAME IN PROGRESS is similar to BC ENABLED, with the following exception: In the frame auto-repeat mode, BC FRAME IN PROGRESS will return logic "0" during the time following the End-of-Message (EOM) sequence for the last message of the frame, up to the beginning of the Start-of-Message (SOM) sequence for the first message of the subsequent frame.

BC MESSAGE IN PROGRESS will return logic "1" between the time of the SOM sequence and the EOM sequence for each message processed.

If ENHANCED INTERRUPTS are enabled (bit 15 of Configuration Register #2 programmed to logic "1"), and the Interrupt Mask Register is programmed to logic "0" (disabling interrupt requests from the ACE), the Interrupt Status Register may still be polled for a number of conditions in BC mode. These include BC COMMAND STACK ROLLOVER (bit 11), BC RETRY (bit 8), TIME TAG ROLLOVER (bit 6), BC MESSAGE INTERRUPT (bit 4), BC END OF FRAME (bit 3), FORMAT ERROR (bit 2), STATUS SET (bit 1), and END OF MESSAGE (bit 0).

Note that any of the conditions listed in the previous paragraph may also be used to trigger an interrupt request to the host CPU. In most systems, an interrupt request will be enabled to signify a BC END OF FRAME condition. This indicates that a BC frame has been completed. In other systems, the BC RETRY interrupt request (for **selected** messages, as programmed in the BC Control Words) or the END-OF-MESSAGE interrupt request (for **all** messages) may be used.

The FORMAT ERROR and BC RETRY interrupt conditions may be used to inform the host of any bus error conditions. STATUS SET may be used to indicate to the CPU that one of the unmasked Status Word bits has been set in a responding RT's Status Word. A particular Status Word bit may be enabled to cause a Status Set condition by programming the respective Status Mask bit BC Control Word to logic "0."

The Status Mask bits may be used in conjunction with the STATUS SET STOP-ON-MESSAGE (bit 10) bits of Configuration Register #1. In this way (or via the ERROR-STOP-ON-MESSAGE bit), the host is able to interject asynchronous messages. An example of such an asynchronous message is for the BC to process a single-message frame consisting of a Transmit Vector Word mode command following reception of an RT Status Word with the Service Request bit set. After the host has processed this message and captured the RT's Vector Word, it may then resume processing of the in-line BC frame.

Termination of BC Frames

Under most circumstances, a programmed BC frame will process all of the programmed messages in the frame. That is, the ACE BC will continue to process messages until the Message Count location has incremented to FFFF. In the frame auto-repeat mode with INTERNAL TRIGGER ENABLED, the

subsequent BC frame will automatically restart after one frame has been completed.

The ACE provides a number of mechanisms for aborting BC frames. Bits 12 through 9 of Configuration Register #1 provide mechanisms for automatically halting the ACE BC. If set to logic "1," ERROR STOP-ON-MESSAGE and STATUS SET STOP-ON-MESSAGE will cause the ACE BC to stop processing messages at the end of the **current message** if a Format Error or Status Set condition occurs. If the ACE BC is programmed for the frame auto-repeat mode, ERROR STOP-ON-FRAME and STATUS SET STOP-ON-FRAME will cause the ACE BC to stop processing messages at the end of the **current frame** if a Format Error or Status Set condition occurs.

Some of the bits in the Start/Reset Register provide a mechanism for the host CPU to terminate the processing of messages by the host BC. RESET will result in an **immediate** (that is, aborting the current message) termination of message processing. BC STOP ON MESSAGE and BC STOP-ON-FRAME will cause the ACE to terminate message processing at the **end** of the current message or frame.

BC Start- and End-of-Messages and Retry Transfer Sequences

At the start and end of each message, and prior to the processing of a message retry, the ACE performs the following sequences of transfers from/to the shared RAM:

BC Start-of-Message (SOM) Sequence

1. The Stack Pointer is read from the active area Stack Pointer location. This address is used for accessing the BC descriptor block in the active area Command Stack.

2. The Message Gap-Time word is read from the third location in the block descriptor.

3. The Message Block Pointer word is read from the fourth location in the block descriptor. This pointer provides the starting address of the BC message block (address of the BC Control Word).

4. The BC Control Word is read from the first location in the BC message block.
5. The (first) Command Word is read from the second location in the BC message block.

6. The Time-Tag word is written to the second location in the block descriptor.

7. The Block Status Word is written to the first location in the block descriptor.

BC End-of-Message (EOM) Sequence

1. The Message Count word is read from the active area Message Counter location. If the value of this word is less than FFFF (hex), the ACE (internally) increments the value by one. If the value of this word is equal to FFFF (hex), this denotes that the current message is the last message of the frame.

The current frame is terminated following the end of the current EOM sequence.

2. The Time-Tag word is written to the second location in the block descriptor.

3. The Block Status Word is written to the first location in the block descriptor.

4. The Message Count Word is written to the active area Message Counter location.

5. The value of the Stack Pointer is incremented by four. The updated value is written to the active area Stack Pointer location.

BC Message Retry Sequence

1. The Message Count word is read from the active area Message Counter location.
2. The BC Control Word is read from the first location in the BC message block.

3. The (first) Command Word is read from the second location in the BC message block.

BC Exception Conditions

In response to various message errors and other exception conditions, the ACE bus controller takes actions and provides a number of indications. TABLE 45 indicates the respective Block Status Word bits that will be set, automatic retry activity, and interrupt requests that are issued and Interrupt Status Register bits that become set as a result of these conditions.

TABLE 45. BC EXCEPTION CONDITIONS

	Block Status Word Bits	Automatic Retries (if Enabled)	Interrupts, Interrupt Status Word Bits	Other Effects
No Response	ERROR FLAG, NO RESPONSE TIMEOUT, RETRY COUNT(1,0)(if enabled)	Yes	FORMAT ERROR, BC RETRY (if enabled)	
Received Word Count Error	ERROR FLAG, WORD COUNT ERROR, FORMAT ERROR, RETRY COUNT(1,0)(if enabled)	Yes	FORMAT ERROR, BC RETRY (if enabled)	
Incorrect Received Sync Type	ERROR FLAG, INCORRECT SYNC TYPE, FORMAT ERROR, RETRY COUNT (0,1)(if enabled)	Yes	FORMAT ERROR, BC RETRY (if enabled)	
Invalid Received Word (Manchester encoding, Bit Count, or Parity)	ERROR FLAG, FORMAT ERROR, INVALID WORD, RETRY COUNT(1,0)(if enabled)	Yes	FORMAT ERROR, BC RETRY (if enabled)	Note: If the ACE BC receives an invalid Data Word, it will continue to receive (but not store) all subsequent, contiguous Data Words. It will wait until it senses an idle bus before performing an EOM or retry transfer sequence, performing a message retry, or transmitting the next message.
Wrong RT Address in Received Status Word	ERROR FLAG, WRONG STATUS ADDRESS/NO GAP, STATUS SET, RETRY COUNT(1,0)(if enabled)	Yes	STATUS SET, BC RETRY (if retry enabled for Status Set)	
Less than 2 µs gap before Status Word	ERROR FLAG, FORMAT ERROR,	Yes	FORMAT ERROR, BC RETRY (if	

TABLE 45. BC EXCEPTION CONDITIONS

	Block Status Word Bits	Automatic Retries (if Enabled)	Interrupts, Interrupt Status Word Bits	Other Effects
Response and ENHANCED MODE and GAP CHECK ENABLED, bit 7 of Configuration Register #5 is logic "1"	WRONG STATUS ADDRESS/NO GAP, RETRY COUNT(1,0)(if enabled)		enabled)	
Loop Test Fail	ERROR FLAG, LOOP TEST FAIL	No	FORMAT ERROR	
Transmitter Timeout: Transmitter attempts to transmit for longer than 668 µs	Block Status Word stored during Start-of-Message Sequence	No	BC/RT TRANSMITTER TIMEOUT	BC Frame is terminated
Non-ENHANCED mode or Expanded BC Control Word not enabled, and one or more bits set in RT Status Word	ERROR FLAG, STATUS SET, RETRY COUNT(1,0)(if RETRY IF STATUS SET, bit 9 of Configuration Register #4, is programmed to logic "1")	Yes, if RETRY IF STATUS SET, bit 9 of Configuration Register #4, is programmed to logic "1"	BC STATUS SET, BC RETRY(if retry enabled for Status Set)	
ENHANCED mode and Expanded BC Control Word enabled, and one or more bits set in RT Status Word with the corresponding STATUS SET bit(s) in the BC Control Word programmed to logic "0"	ERROR FLAG, STATUS SET, MASKED STATUS SET, RETRY COUNT(1,0)(if retry enabled for Status Set)	Yes, if RETRY IF STATUS SET, bit 9 of Configuration Register #4, is programmed to logic "1"	BC STATUS SET, BC RETRY(if retry enabled for Status Set)	
ENHANCED mode and Expanded BC Control Word enabled, and one or more bits set in RT Status Word with the corresponding STATUS SET bit(s) in the BC Control	ERROR FLAG, STATUS SET	No	None	

TABLE 45. BC EXCEPTION CONDITIONS

	Block Status Word Bits	Automatic Retries (if Enabled)	Interrupts, Interrupt Status Word Bits	Other Effects
Word programmed to logic "1" and no bits set in the RT Status Word with the corresponding STATUS SET bit(s) in the BC Control Word programmed to logic "0"				
With VALID M.E./NO DATA = "0"; in Response to a Transmit Command, Message Error bit Set in Status Word, followed by no Data Words	ERROR FLAG, STATUS SET, MASKED STATUS SET (unless using Expanded BC Control Word and the M.E. MASK bit is logic "1"), FORMAT ERROR, WORD COUNT ERROR, RETRY COUNT(1,0) (if enabled)	Yes	FORMAT ERROR, BC STATUS SET (if Expanded BC Control Word is not enabled or if the M.E. MASK bit in the BC Control Word is logic "0"), BC RETRY (if enabled)	
With VALID M.E./NO DATA = "0"; in Response to a Transmit Command, Message Error bit Set in Status Word, Followed by the Correct Number of Data Words	ERROR FLAG, STATUS SET, MASKED STATUS SET (unless using Expanded BC Control Word and the M.E. MASK bit is logic "1"), RETRY COUNT(1,0) (if retry enabled for Status Set, unless using Expanded BC Control Word and the M.E. MASK bit is logic "1")	Yes, (if retry enabled for Status Set, unless using Expanded BC Control Word and the M.E. MASK bit is logic "1")	BC STATUS SET (if Expanded BC Control Word is not enabled or if the M.E. MASK bit is logic "0"), BC RETRY (if retry enabled for Status Set, unless using Expanded BC Control Word and the M.E. MASK bit is logic "1")	

BC Off-Line and On-Line Self-Tests

The BC mode of the BU-65528 provides a number of self-test features. The internal registers and shared RAM are accessible to the host processor at all times. In addition, the ACE BC includes wraparound test provisions for both an off-line self-test and an on-line self-test.

The internal registers and shared RAM can be tested by means of host processor software routines to implement checkerboard, walking zero, walking one and counting patterns and reading back and verifying the contents of the internal RAM.

The BC off-line self-test provides a means of exercising and verifying the parallel address and data paths, encoder, serial data path, decoder, and portions of the BC message format and word count logic, protocol state machine and memory management logic. In the off-line self test, the ACE does **not** transmit on the external 1553 bus. Instead, the Manchester II encoder output is routed directly to the decoder input. The off-line self-test can be run following power turn-on as part of system self-test or when the ACE hybrid has been functioning in RT mode, as part of a software controlled response to a Reset RT mode code command. A common element of the off-line and on-line BC self-tests is the method by which loopback words are checked. In each case, the received version of all transmitted words is checked for validity (sync, encoding, parity, bit count) and the received version of the last word transmitted by the BC is compared to the transmitted version of the word. The loopback test is considered to have failed if the validity and/or comparison tests do not verify.

It is important to note that the TX_INH_A and TX_INH_B inputs must be set logic "0" in order to pass the off-line self-test. The BC off-line self-test will fail if the respective transmitter inhibit (TX_INH_A[B]) is set to logic "1." Note that writing logic "1" to these bits provides a mechanism for self-testing the transmit inhibit function.

In order to run the off-line self-test for a particular message, bit 6 in the BC Control Word (OFF-LINE SELF-TEST) must be programmed to logic "1." As the result of a nonbroadcast self-test message, the RESPONSE TIMEOUT bit of the message's Block Status Word **should be set**. Following a broadcast self-test message, the RESPONSE TIMEOUT bit **should NOT be set.** If the self-test passes, the LOOP TEST FAIL bit of the Block Status Word will not be set. The other portion of determining the success of the BC self-test is to verify that the Loopback Word contents match those of the last transmitted word.

In order to make the off-line self-test as comprehensive as possible, a large number of self-test messages should be processed. To exercise the various portions of the BC protocol and memory management logic, the message block starting address, message format, data word count and contents of the last word to be transmitted should be varied for the individual test messages.

The off-line self-test may also exercise the ERROR, EOM, BC/RT MESSAGE, and BC_EOM interrupt request features. This may be done by setting the respective bit(s) in the Interrupt Mask register. If the ACE is configured for a multimessage frame of off-line self-test messages, an interrupt will occur after every message if the EOM interrupt is enabled. Similarly, an ERROR interrupt request will occur following every nonbroadcast off-line self-test message, due to the RESPONSE TIMEOUT condition. If the BC_EOM interrupt is enabled but the EOM interrupt is not, an interrupt request will only be issued after the **last** message of the frame is processed.

The BC STOP-ON-ERROR feature may be exercised by setting the respective bit in the Configuration Register, configuring the ACE for a multimessage BC frame of off-line self-test messages and verifying that the BC stops processing messages after the first nonbroadcast message of the frame has been processed.

The message gap-time and Time-Tag features may be self-tested by programming the Message gap time(s) for a multimessage frame and verifying the elapsed time of the frame by means of the Time-Tag Register. Automatic retries can be tested since a retry will occur, if programmed, as a result of the RESPONSE TIMEOUT condition resulting from a nonbroadcast off-line self-test message.

For the BC on-line self-test, the last word transmitted on the 1553 bus is monitored by the receiver and fed back to the decoder to formulate the Loopback Word. Similar to the off-line test, the LOOP TEST FAIL bit in the Block Status Word is either set (for fail) or cleared as a result of the Loopback test and the Loopback Word is stored in the Shared RAM. In addition to the digital circuitry exercised by the off-line self-test, the on-line test verifies the operation of the transmitter, receiver, and to a large extent, the external transformers, stub and bus cabling, coupling boxes and termination resistors. Open circuits or other faults in these external components will result in signal reflections; these reflections can result in failures of the loopback test.

RT OPERATION

INTRODUCTION

The BU-65528 provides a number of programmable options for RT memory management. The choice of memory management scheme is fully programmable on a transmit/receive/broadcast basis. The RT memory management options include a single message mode, a circular buffer mode to support bulk data transfers, and a double buffering mode for individual receive subaddresses to ensure data consistency. By making use of the double buffering feature, the host processor will easily be able to access the most recent, complete received block of valid Data Words for any given subaddress. In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from non-broadcast received data.

For each transmit, receive or broadcast subaddress, either a single-message data block, a double buffered configuration (two alternating Data Word blocks), or a variable-sized (128 to 8192 words) circular buffer may be allocated for data storage. In addition to helping ensure data consistency, the circular buffer feature provides a means of greatly reducing host processor overhead for bulk data transfer applications. End-of-message interrupts may be enabled either globally, following error messages, on a Tx/Rx/Bcst-subaddress or mode code basis, or when any particular Tx/Rx/Bcst-subaddress circular buffer reaches its lower boundary. An interrupt status register allows the host processor to determine the cause of all interrupts by means of a single READ operation.

The ACE RT provides options for requesting interrupts following messages for individual mode codes as well as for storing Data Words for the various mode codes in separate RAM locations.

The circular buffer feature of the ACE is enabled by setting the ENHANCED RT MEMORY MANAGEMENT bit (bit 1 of Configuration Register #2) to logic "1." If the ENHANCED RT MEMORY MANAGEMENT option is not chosen, each T/R-subaddress is mapped to a single data block by means of its respective Lookup Table entry. In this mode, the data block for each T/R-subaddress is then repeatedly overwritten or overread.

As a programmable option, the ACE circular buffer pointers may be programmed to **not update** following the reception of invalid data blocks. This feature is enabled by setting the OVERWRITE INVALID DATA bit (bit 11) of Configuration Register #2. By so doing, retried data transmitted by the bus controller (or another RT) will automatically **overwrite** any invalid data blocks. This serves to facilitate bulk data transfers. The host processor needs only to initialize the Lookup Table Pointer, wait for a circular buffer rollover interrupt, and service the interrupt by accessing the multimessage block of valid data words. In this mode, the RT's host processor does **not** need to be concerned about servicing individual messages, retries, or errors.

Other RT options controlled by Configuration Register #2 include automatic clearing of the Service Request Status Word bit following a Transmit Vector Word mode command, and capabilities to clear and/or load the Time Tag Register following receipt of Synchronize mode commands. It should be noted that these three features, and the use of circular buffers can be used in the NON-ENHANCED mode (bit 15 of Configuration

Register #3 programmed to logic "0"), as well as in the ENHANCED mode.

Many of the advanced features of the ACE RT operate only in the ENHANCED mode (bit 15 in Configuration Register #3 programmed to logic "1"). In the ENHANCED mode, interrupts may be generated for individual mode commands, and separate fixed memory locations can be allocated for individual mode code Data Words (transmit and receive). The busy bit in the Status Word may set based on broadcast/valid RT address, transmit/receive bit, and subaddress. MIL-STD-1553B Notice 2 states that if the Busy bit is set it should be set for a particular subaddress only.

In the ENHANCED mode, the ACE provides RT subaddress double buffering. The RT subaddress double buffering mode allocates two 32-word data buffers to a selected subaddress. Received data is stored alternatively into each of these buffers. In many RT applications, the host processor needs to access only the data from the **latest** received message for a given subaddress. In this scenario, the use of the RT subaddress double buffer option serves to ensure data consistency by allowing the host processor to easily locate and read the most recent, consistent, valid data block received for the respective subaddress.

The ACE also provides a combined RT/Selective Monitor Mode. In this mode, all of the Advanced RT features are available, as well as a full selective message-based monitor. The selective message monitor mode allows the user to selectively monitor data based on RT address, T/R bit, and subaddress. The message monitor has separate command and data stacks.

RT MEMORY ORGANIZATION

A typical memory map for the ACE in RT mode is illustrated in TABLE 46. As in BC mode, the two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. In addition to the Stack Pointer, for RT mode there are several other areas of the shared RAM address space that are designated as fixed locations. These are for the Area A and Area B Lookup Tables, the Illegalization lookup table, the Busy lookup table, and the mode code data tables.

The RT Lookup tables, which provide a mechanism for mapping data blocks for individual Tx/Rx/Bcst-subaddresses to areas in the RAM, are located in address range 0140 to 01BF for Area A and address range 01C0 to 023F for Area B. The RT lookup tables include Subaddress Control Words as well as the individual Data Block Pointers. If used, address range 0300-03FF is dedicated as the illegalizing section of RAM. The actual Stack RAM area, as well as the individual data blocks, may be located in any of the non-fixed areas in the shared RAM address space.

TABLE 46(a) illustrates the typical memory map for the case in which the enhanced mode RT features are **not** used. In this instance, address locations 0280-03FF (hex) may be used for storage of Stack Data or Message Data Blocks.

TABLE 46(b) illustrates the RT memory map for the case where the advanced RT features are used.

TABLE 46. TYPICAL RT MEMORY MAP

(a) RT MEMORY MAP (Without ENHANCED MODE features enabled)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0104	Stack Pointer B (fixed location)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-025F	Data Block 0
0260-027F	Data Block 1
0280-029F	Data Block 2
02A0-02BF	Data Block 3
02C0-02DF	Data Block 4
02E0-02FF	Data Table 5
0300-03FF	Command Illegalization Table
0400-041F	Data Block 6
•	•
•	•
•	•
2FC0-2FDF	Data Block 356
2FE0-2FFF	Data Block 357

(b) MEMORY MAP (With the ENHANCED MODE features enabled)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	RT Command Stack Pointer A (fixed location)
0101-0103	RESERVED
0104	RT Command Stack Pointer B (fixed location)
0105-0107	RESERVED
0108-010F	Mode Code Selective Interrupt Table (fixed area)
0110-013F	Mode Code data (fixed area)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-0247	Busy Bit Lookup Table (fixed area)
0248-025F	(not used)
0260-027F	Data Block 0
0280-029F	Data Block
•	•
•	•
02E0-02FF	Data Block 4
0300-03FF	Command Illegalizing Table (fixed area)
0400-041F	Data Block 5
0420-043F	Data Block 6
•	•
•	•
•	•
2FE0-2FFF	Data Block 356

Note that in TABLE 46, the memory map shown for the RT ENHANCED mode (unlike the non-Enhanced mode), there is no area allocated for "Stack B." This is shown for purpose of illustration.

It should be noted that the global double buffering feature **may still be used** in conjunction with the Enhanced RT mode. However, in the Enhanced mode, it is strongly recommended that the Subaddress Double Buffering feature, rather than the "global" double buffering feature (Area A/Area B) be used as a more efficient means of ensuring data sample consistency.

Also, note that in TABLE 46, the allocated area for the RT command stack is 256 words. However, in the ENHANCED MODE, larger stack sizes are possible. In this mode, the RT Command Stack size is programmable for 256 words (64 messages), 512, 1024, or 2048 words (512 messages) by means of bits 14 and 13 of Configuration register #3. Refer to TABLE 47.

TABLE 47. RT COMMAND STACK SIZE

BIT 14 BC/RT CMD STACK SIZE 1	BIT 13 BC/RT CMD STACK SIZE 2	BC/RT STACK SIZE (WORDS)
0	0	256 (64 messages)
0	1	512 (128 messages)
1	0	1024 (256 messages)
1	1	2048 (512 messages)

RT MEMORY MANAGEMENT

In order to comply with Notice 2 of MIL-STD-1553B and to better support bulk data transfers, the ACE provides enhanced RT memory management capabilities. These features allow broadcast message data to be separated from nonbroadcast receive data, help to ensure data consistency for transmitted and received data blocks, and generally serve to off-load the host processor for real-time applications.

Active Area Double Buffering. The ACE provides a global double buffering mechanism by means of bit 13, CURRENT AREA A*/B, of Configuration Register #1. At any point in time, this allows for one stack pointer, stack area, lookup table, and set of data blocks to be designated as "active" (used for the processing of 1553 messages) and the alternate set of respective data structures to be designated as "nonactive."

Both the "active" and "nonactive" RAM areas are **always accessible** by the host processor.

TABLE 48 illustrates the RT Lookup tables. Within each lookup table, 32 locations provide optional separation of broadcast messages. The last 32 words of each table are Subaddress Control Words, one appropriated for each RT subaddress.

TABLE 48. RT LOOKUP TABLES

AREA A	AREA B	DESCRIPTION	COMMENT
0140 • • • 015F	01C0 • • • 01DF	Rx(/Bcst) SA0 • • • Rx(/Bcst) SA31	Receive (/Broadcast) Lookup Pointer Table
0160 • • • 017F	01E0 • • • 01FF	Tx SA0 • • • Tx SA31	Transmit Lookup Pointer Table
0180 • • • 019F	0200 • • • 021F	Bcst SA0 • • • Bcst SA31	Broadcast Lookup Pointer Table (Optional)
01A0 • • • 01BF	0220 • • • 023F	SACW SA0 • • • SACW SA31	Subaddress Control Word Table (Optional)

Subaddress Control Word

Referring to TABLES 49 and 50, in the Enhanced RT Memory Management mode, each of the 32 Subaddress Control Words specifies the memory management and interrupt schemes for the respective subaddress. For each Subaddress Control Word, five bits control the memory management scheme and interrupts for each of transmit, receive, and broadcast messages. In addition, bit 15 (MSB) may be used to enable subaddress double buffering for receive (and/or broadcast receive) subaddresses.

For each transmit (or receive or broadcast) subaddress, three bits are used to specify the memory management scheme. For each Rx(/Bcst) subaddress, the memory management scheme may be selected from among the single message mode (as in the nonenhanced mode), the circular buffer mode, or the double buffered mode. For each transmit subaddress, the memory management scheme may be selected from among the single message mode or the circular buffer mode. Note that the double buffered mode **is not applicable** for transmit subaddresses.

It should be noted that for mode code messages, the Subaddress Control Word is only applicable if ENHANCED MODE CODE HANDLING **is disabled.** ENHANCED MODE CODE HANDLING is disabled in the non-ENHANCED mode **or** if bit 0 of Configuration Register #3 is logic "0." ENHANCED MODE CODE HANDLING is enabled in the ENHANCED MODE by setting bit 0 of Configuration Register #3 to logic "1."

In the single buffer mode, a single data block is repeatedly overread (for transmit data) or overwritten (for receive or broadcast data). Alternatively, in the circular buffer mode, Data Words for successive messages to/from any particular Tx/Rx/Bcst subaddresses are read from or written to the **next** contiguous block of locations in the respective circular buffer.

The size of the circular buffer for each transmit, receive, or broadcast subaddress may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words. For each Tx/Rx/Bcst subaddress, two bits of the subaddress control word are used to enable interrupts. One of these bits will result in an interrupt following **every** message directed to the specific Tx/Rx/Bcst subaddress. The other of these two bits will result in an interrupt at the end of a message if the message resulted in the Lookup table pointer for the respective Tx/Rx/Bcst-subaddress crossing the lower boundary of the circular buffer, rolling over to the top of the buffer.

In the subaddress double buffered mode, a pair of 32-word data blocks are allocated for a particular receive (and/or broadcast receive) subaddress. In this mode, successive messages received to the subaddress are stored in alternating data blocks.

TABLE 49. SUBADDRESS CONTROL WORD BIT MAP

BIT	DESCRIPTION
15(MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

TABLE 50. SUBADDRESS CONTROL WORD
Memory Management Subaddress Buffer Scheme

RX DOUBLE BUFFERED ENABLED (see Note)	MM2	MM 1	MM 0	DESCRIPTION	COMMENT
0	0	0	0	Single Message	
1	0	0	0	For Receive or Broadcast: Double Buffered For Transmit: Single Message	
X	0	0	1	128-Word	Circular Buffer of Specified Size
X	0	1	0	256-Word	
X	0	1	1	512-Word	
X	1	0	0	1024-Word	
X	1	0	1	2048-Word	
X	1	1	0	4096-Word	
X	1	1	1	8192-Word	

Note: In order to utilize subaddress double buffering, the ACE must be programmed to ENHANCED MODE (bit 15 of Configuration Register #3 must be logic "1").

In order to select subaddress double buffering by means of the Subaddress Control Word, the RX SUBADDRESS DOUBLE BUFFERING ENABLE bit (bit 13) **and** the ENHANCED RT MEMORY MANAGEMENT bit (bit 1) of Configuration Register #2 must be programmed to logic "1."

If the ACE is in ENHANCED MODE **and** RX SUBADDRESS DOUBLE BUFFERING ENABLE is logic "1" **and** ENHANCED RT MEMORY MANAGEMENT is logic "0," the subaddress double buffering mode will be used for **ALL** receive (and broadcast) subaddresses.

Single Message Mode

If bit 1 of Configuration Register #2 is logic "0," the ACE memory management scheme assumes its default or non-enhanced mode. In the non-enhanced RT operation, the single message memory management mode is used for **all** receive, transmit, or broadcast subaddresses. It should be noted, that under the enhanced RT memory management scheme, the single message mode may still be used for individual receive, transmit and/or broadcast subaddresses. This is the case if the SUBADDRESS RX DOUBLE BUFFERING bit (bit 15) **and** the three applicable "memory management" bits in the respective Subaddress Control Word are logic "0."

The operation of the single message RT mode is illustrated in FIGURE 11. In the single message mode, the respective Lookup Table entry must be loaded by the host processor. At the start of each message, the lookup table entry is stored in the third address location of the respective message block descriptor in the stack area of RAM. Received Data Words are written to or transmitted Data Words are read from the Data Word Block referenced by the lookup table pointer. In the single message mode, the current lookup table pointer **is not** written to by the ACE memory management logic at the end of a message. Therefore, if a subsequent message is received for the same subaddress, the **same** Data Word block will be overwritten or overread.

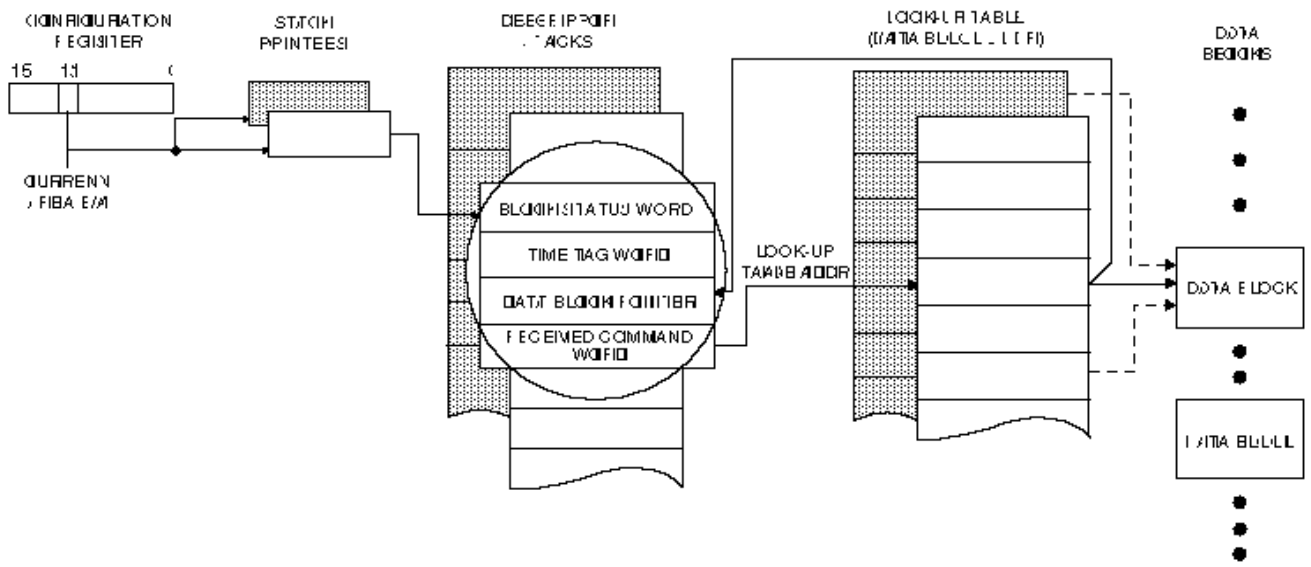


FIGURE 11. RT MEMORY MANAGEMENT-SINGLE MESSAGE MODE

256-Word Boundaries

The programming of bit 10 of Configuration Register # 2, 256-WORD BOUNDARY DISABLE, must be considered for both the default memory management mode (bit 1 of Configuration Register # 2 = 0) or for any Tx/Rx/Bcst subaddresses in the enhanced mode (bit 1 of Configuration Register # 2 = logic "1"), using the single message mode. If 256-WORD BOUNDARY DISABLE is logic 0, the operation of the address counter for accessing RT Data Word Blocks for the single buffer mode will observe 256-word boundaries in the ACE shared RAM address space. That is, if 256-WORD BOUNDARY DISABLE is logic 0, the internal Data Word address pointer will roll over from XXFF to XX00 (hex), rather than increment to (XX+1)00.

If the 256-WORD BOUNDARY DISABLE bit is set to logic "1" however, the ACE address counter **will not** roll over at 256-word boundaries. In this instance, the Data Word addresses are generated from the output of a **16-bit** counter, rather than an 8-bit counter. That is, the address counter will increment from XXFF to (XX + 1)00, rather than roll back to XX00.

RT Subaddress Double Buffering Mode

The ACE provides a double buffering mechanism for **received** data, that is optionally selectable on a subaddress basis for all receive (and/or broadcast) subaddresses. It should be noted that the Subaddress Double Buffering mode is applicable for receive data only, **not for transmit data**. Double buffering of transmit messages may be easily implemented by software techniques.

The purpose of the double buffering mode is to provide the host processor with the highest possible degree of data consistency. This is accomplished by allocating **two** 32-word data word blocks for each individual receive (and/or broadcast receive) subaddress. One of the blocks will be designated as the active 1553 block while the other will be considered inactive. The data accompanying the next receive command to that subaddress will be stored in the active block. Upon completion of the message, provided that the message was valid and Receive Double Buffering is enabled, the ACE will automatically switch the active and inactive blocks for that subaddress. This means that the latest, valid, complete data block is always readily available to the host processor.

The subaddress double buffer mode is available only in the ENHANCED MODE (bit 15 in Configuration #3 set). If the ENHANCED RT MEMORY MANAGEMENT ENABLE bit (bit 1 in Configuration Register #2) is programmed to logic "0," then the selective double buffer mode is enabled by simply setting the DOUBLE BUFFER ENABLE bit (bit 12 in Configuration Register #2) to logic "1." In this case (global double buffering), double buffering is enabled for **all** receive subaddresses (and all broadcast receive subaddresses if broadcast separation is enabled).

If ENHANCED RT MEMORY MANAGEMENT ENABLE bit is programmed to logic "1," then the double buffer mode is enabled **for selected subaddresses** by setting the DOUBLE BUFFER ENABLE bit (bit 12 in Configuration Register #2) to logic "1" **and** by the programming of the desired Subaddress Control Words. The Subaddress Control word must be programmed for receive single message mode (RX:MM2-0 (bits 7-5) set to logic "0") **and** the DOUBLE BUFFER ENABLE bit (bit 15) must be programmed to logic "1." If SEPARATE BROADCAST is enabled (bit 0 in Configuration Register #2 is set to logic "1"), then the broadcast memory management scheme should also be set to single message mode (RX:MM2-0 (bits 2-0) programmed to logic "0") if double buffering of broadcast receive commands is desired. Reference TABLE 50.

The software algorithm for reading the latest data block is to first disable double buffering for the desired subaddress. If ENHANCED RT MEMORY MANAGEMENT is not enabled (bit 1 of Configuration Register #2 programmed to logic "0"), double buffering must be disabled **FOR ALL SUBADDRESSES by setting RECEIVE SUBADDRESS DOUBLE BUFFERING ENABLE (bit 12 in Configuration Register #2) to logic "0."**

If ENHANCED RT MEMORY MANAGEMENT is enabled (the STRONGLY RECOMMENDED implementation), double buffering can be disabled on a subaddress basis by programming the DOUBLE BUFFER ENABLE bit (bit 15) of the appropriate Subaddress Control Word to logic "0." The host processor should then read the current value of the data block pointer in the lookup table. This pointer references the active Data Word block. The last consistent data block can be accessed in the **inactive** block by inverting bit 5 of the current data block pointer. The current lookup table entry should **not** be modified.

After reading the data block, the host processor should reenable double buffering by setting the RX DOUBLE BUFFER ENABLE bit (if ENHANCED MEMORY MANAGEMENT is not enabled) or by setting the RX DOUBLE BUFFER ENABLE bit (bit 15) in the appropriate Subaddress Control Word to logic "1" (if ENHANCED MEMORY MANAGEMENT is enabled).

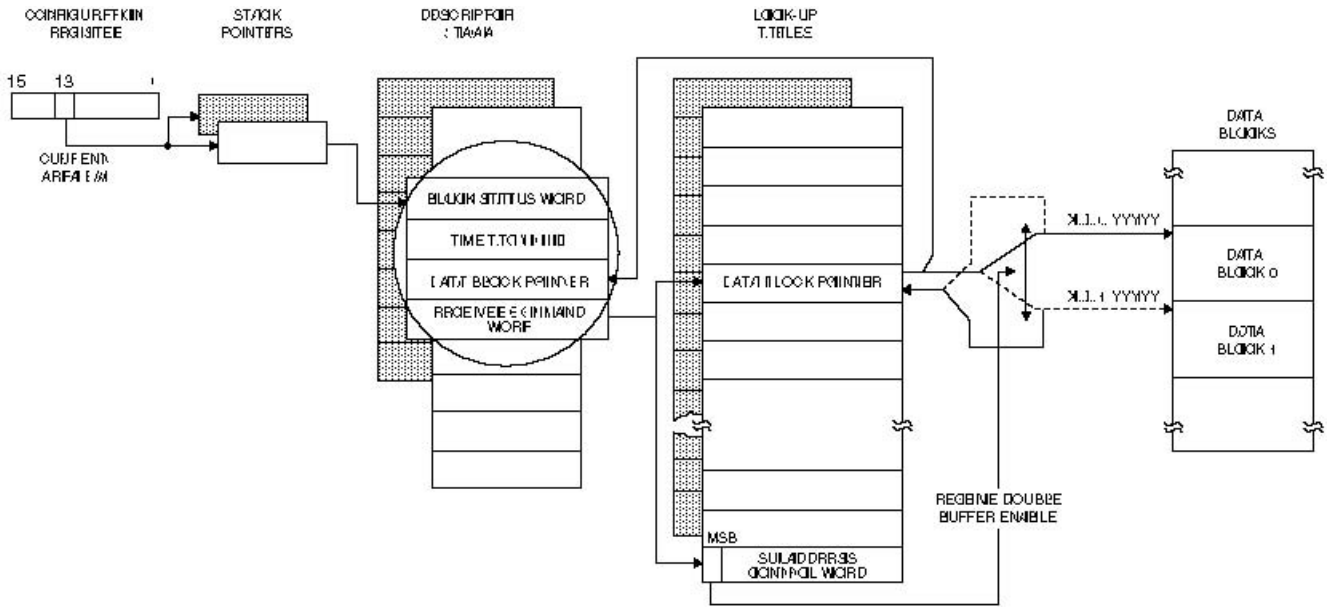


FIGURE 12. RT MEMORY MANAGEMENT-SUBADDRESS DOUBLE BUFFERING MODE

Circular Buffer Mode

In the ENHANCED RT MEMORY MANAGEMENT mode, individual transmit, receive, and broadcast subaddresses may be programmed for either the single message or circular buffer modes.

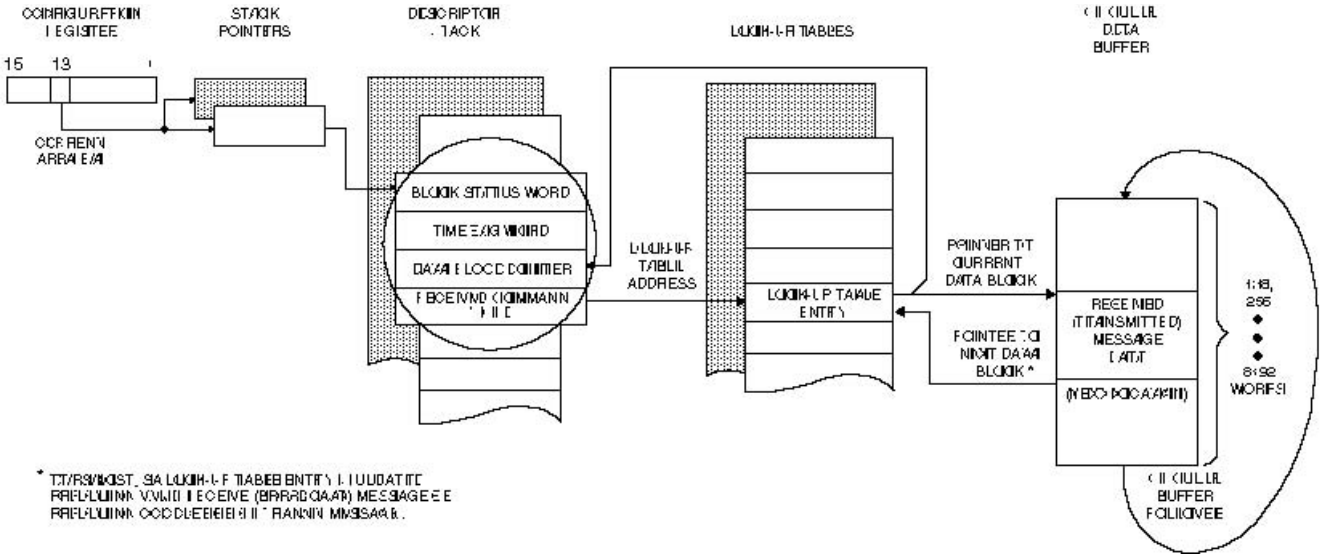


FIGURE 13. RT MEMORY MANAGEMENT -CIRCULAR BUFFER MODE

The operation of the circular buffer RT memory management mode is illustrated in FIGURE 13. As in the single message mode, the individual Lookup Table entries are initially loaded by the host processor. At the start of each message, the Lookup Table entry is stored in the third position of the respective message block descriptor in the stack area of RAM. Receive or Transmit Data Words are transferred to/from the circular buffer, starting at the location referenced by the Lookup Table pointer.

If the OVERWRITE INVALID DATA bit (bit 11) of Configuration Register #2 is logic "0," the location **after** the last word accessed for the message is stored into the respective Lookup Table location, **regardless of whether or not there were any errors in the just completed message.** By so doing, data for the **next** message for the respective Tx/Rx/Bcst subaddress will be accessed to/from the next lower contiguous block of locations in the circular buffer.

If the OVERWRITE INVALID DATA bit (bit 11) of Configuration Register #2 is logic "1," the location **after** the last word accessed for the message is stored in the respective Lookup Table location **only following a <u>valid</u> received (or transmitted) message**. Assuming that the value of the Lookup Table pointer is updated, data for the **next** message for the respective Tx/Rx/Bcst subaddress will be accessed to/from the next contiguous block of locations in the circular buffer. Assuming the OVERWRITE INVALID DATA bit is logic "1," the Lookup Table pointer will **not** be updated at the end of the message if there was an error in the message. This allows failed messages in a bulk data transfer to be retried without disturbing the circular buffer data structure, and without intervention by the RT's host processor.

It is strongly recommended that OVERWRITE INVALID DATA be programmed to logic "1" when using the circular buffer mode.

When the pointer reaches the lower boundary of the circular buffer (located at 128, 256, . . . 8192-word boundaries in the shared RAM address space), the pointer rolls back to the top boundary of the circular buffer, as shown in FIGURE 13.

It should be noted that the pointer to the start of the RT Data Word block is stored in the third location of the message block descriptor (in the stack) for the single buffer mode as well as for the circular buffer mode.

To make best use of the circular buffer feature, the OVERWRITE INVALID DATA bit (bit 11 of Configuration Register #2) **and** RX: CIRCULAR BUFFER ROLLOVER bit (bit 8) in the Subaddress Control Word should be programmed to logic "1." The host processor need initialize the circular buffer lookup table pointer, and then wait for the circular buffer rollover interrupt. After this interrupt occurs, the CPU may then read the contiguous, multimessage block of valid, received Data Words from the shared RAM. Use of the RT circular buffer feature eliminates the need for the CPU to service individual messages, or be concerned with message errors or retries.

TABLE 51 summarizes the programming of configuration register bits required to enable the various ACE RT memory management features.

TABLE 51. CFG. REG. BITS USED TO ENABLE RT MEM. MNGMNT FEATURES

FEATURE	SUBADDRESS DOUBLE BUFFER ENABLE (bit 12 of Configuration Register # 2)	OVERWRITE INVALID DATA (Configuration Register # 2, bit 11)	ENHANCED RT MEMORY MANAGEMENT (Configuration Register #2, bit 1)	SEPARATE BROADCAST (Configuration Register #2, bit 0)	ENHANCED RT MEMORY MANAGEMENT (Configuration Register #3, bit 15)
Default (power turn-on) Mode: Single Message for ALL Tx/Rx/Bcst Subaddresses	0	0	0	0	0
Single Message mode for all transmit subaddresses; Double Buffering for ALL receive (and broadcast) subaddresses	1 (See Note)	0	0	X	1 (See Note)
Broadcast Separation	X	X	X	1	X
Enable circular buffers for individual subaddresses; NOT overwriting invalid data	X	0	1	X	X
Enable circular buffers for individual subaddresses; WITH overwriting invalid data	X	1	1	X	X
Enable subaddress	1 (See Note)	X	1	X	1 (See Note)

double buffering for individual receive (and broadcast) subaddresses					

Note: In order to enable the subaddress double buffering mode, ENHANCED MODE (bit 15 of Configuration Register #3) must be programmed to logic "1" **before** SUBADDRESS DOUBLE BUFFERING ENABLED (bit 12 of Configuration Register #2) is written as logic "1."

RT STACK AND INTERRUPTS

In RT mode, the Stack area of RAM contains a real-time chronology of all messages processed by the ACE. Similar to BC mode, there is a four word block descriptor in the Stack for each message processed. The four entries to each block descriptor are the Block Status Word, Time Tag Word, the pointer to the start of the data block, and the 16-bit received Command Word. Prior to the processing of messages, the host processor should initialize the Stack Pointer. In some applications, it may also prove helpful to "zero out" the Stack area prior to receiving messages.

In RT mode, the host processor may determine that a message has been processed either by means of interrupts or by polling the Interrupt Status Register or the active area Stack Pointer memory location. The RT Command Stack Pointer increments by four (modulo the stack size) at the start of each message processed. After a message is received, the host CPU should read the Block Status Word, Time Tag, data block starting address, and Command Word received from the Message Block Descriptor in the Stack. Assuming a valid message was received, it may then read the received Data Words from the referenced Data Word block.

RT Block Status Word. The bit map and bit definitions for the RT Block Status Word are indicated below.

TABLE 52. RT MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	RT-RT FORMAT ERROR
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	CIRCULAR BUFFER ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

END-OF-MESSAGE (EOM): Set at the completion of an RT message, regardless of whether or not there were any errors in the message.

START-OF-MESSAGE (SOM): Set approximately 3-4 μs following the receipt (mid-parity bit) of the Command Word and cleared at the end of the message.

CHANNEL B/A*: This bit will be low if the message was processed on Channel A or high if the message was processed on Channel B.

ERROR FLAG: If this bit is logic "1," and one or more of bits 10, 9, and/or 8 are logic "1," this indicates one or more of the following errors have occurred in the message: Format Error Response Timeout and/or Loop Test Fail.

RT-to-RT FORMAT: Applicable for ENHANCED MODE only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1"). This bit will be set if the ACE is the **receiving** RT in an RT-to-RT transfer. Note that this bit will **not** be set if the ACE is the **transmitting** RT for an RT-to-RT transfer.

FORMAT ERROR: If set, indicates that the received portion of a message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.). This bit is a summation of bits 5, 4, 3, 2, 1, and 0.

RESPONSE TIMEOUT: If set, indicates that the ACE was the receiving RT for an RT-to-RT transfer **and** that the transmitting RT has either not responded or has responded later than the programmed value for the No Response Timeout time. The ACE's RT-to-RT No Response Timeout Time is defined as the time from the mid-bit crossing of the parity bit of the Transmit Command Word to the mid-sync crossing of the RT Status Word. In the nonenhanced mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "0"), the value of the BC Response Timeout is 17.5 to 19.5 µs. If ENHANCED MODE ENABLED is logic 1, the value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 µs (±1 µs) by means of bits 10 and 9 of Configuration Register #5.

LOOP TEST FAIL: A loopback test is performed on the transmitted portion of every nonbroadcast message in RT mode. A validity check is performed on the received version of every word transmitted by the ACE RT. In addition, a bit-by-bit comparison is performed on the last word transmitted by the RT for each message. If either the received version of any transmitted word is determined to be invalid (sync, encoding, bit count, and/or parity error) and/or the received version of the last transmitted word does not match the transmitted version, the LOOP TEST FAIL bit will be set.

CIRCULAR BUFFER ROLLOVER: Applicable for ENHANCED MODE only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1") **and** if ENHANCED RT MEMORY MANAGEMENT is enabled (bit 1 of Configuration Register # 2 is set to logic "1") **and** the circular buffer option is enabled for the Bcst/Tx/Rx-subaddress for the current message, by means of the Subaddress Control Word. This bit will be set if the lookup table address pointer crossed the upper boundary of its circular buffer, resulting in a rollover. If OVERWRITE INVALID DATA is enabled (bit 11 of Configuration Register #2 set to logic "1"), this bit will only be set following completion of a transmit message or a **valid** receive message that resulted in a rollover. If OVERWRITE INVALID DATA is disabled (bit 11 of Configuration Register #2 set to logic "0"), this bit will be set when a rollover occurs, independent of message validity.

It should be noted that in the non-ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register # 3, is logic "0"), bits 7 through 0 will always be logic "0."

ILLEGAL COMMAND WORD: Applicable for Enhanced Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, programmed to logic "1"). If this bit is set, it indicates that the message has been illegalized. A message is illegalized if (ENHANCE MODE ENABLE, bit 15 of Configuration Register #3 is logic "0" **or** ILLEGALIZATION DISABLE, bit 7 of Configuration Register #3 is logic "0") **and** the appropriate bit for the respective Broadcast-Tx/Rx-Subaddress-Word Count/Mode Code combination is set in the illegalization table, address locations 0300-03FF in the shared RAM.

WORD COUNT ERROR: Applicable for Enhanced Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, programmed to logic "1"). If set, indicates that the BC did not transmit the correct number of Data Words.

INCORRECT DATA SYNC: Applicable for Enhanced Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, programmed to logic "1"). If set, indicates that the BC transmitted a Command sync in a Data Word.

INVALID WORD: Applicable for Enhanced Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, programmed to logic "1"). Indicates the BC (or transmitting RT in an RT-to-RT transfer) transmitted with one or more words containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

RT-to-RT GAP/SYNC/ADDRESS ERROR: Applicable for Enhanced Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1"). This bit is set if the ACE RT is the receiving RT for an RT-to-RT transfer and one or more of the following occur: (1) If the GAP CHECK ENABLED bit (bit 8) of Configuration Register #5 is set to logic "1" and the transmitting RT responds with a response time of less than 4 µs, per MIL-STD-1553B (mid-parity bit to mid-sync); i.e., less than 2 µs dead time; and/or (2) There is an incorrect sync type or format error (encoding, bit count, and/or parity error) in the transmitting RT Status Word; and/or (3) The RT address field of the transmitting RT Status Word does not match the RT address in the transmit Command Word.

RT-to-RT SECOND COMMAND ERROR: Applicable for Enhanced Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, programmed to logic "1"). If the ACE is the receiving RT for an RT-to-RT transfer, this bit set indicates one or more of the following error conditions in the transmit Command Word: (1) T/R* bit = logic "0"; (2) subaddress = 00000 or 11111; and/or (3) same RT Address field as the receive Command Word.

COMMAND WORD CONTENTS ERROR: Applicable for Enhanced Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, programmed to logic "1"). Indicates a received command word is not defined in accordance with MIL-STD-1553B. This includes the following undefined Command Words: (1) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** the Command Word is a nonmode code, broadcast, transmit command; (2) The OVERRIDE MODE T/R* ERROR bit, bit 6 of Configuration Register #3, is logic "0" **and** a message with a T/R* bit of "0," a subaddress/mode field of 00000 or 11111 and a mode code field between 00000 and 01111; (3) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** a mode code command that is not permitted to be broadcast (eg. Transmit status) is sent to the broadcast address (11111).

Time Tag Word

The Time Tag Word, the second location of the message block descriptor in the RT Command Stack, is updated (written) during both the Start-of-Message (SOM) and End-of-Message (EOM) sequences. The SOM sequence occurs immediately after reception of a valid Command Word to the RT's address or the broadcast address. The EOM sequence occurs approximately 3 to 4 µs after the last word transmitted or received in a message.

During these sequences, the current value of the ACE's internal read/writable Time Tag Register (register address 05) is written to the respective RAM location. The resolution of the Time Tag counter is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB, or an externally provided clock, by means of bits 9, 8, and 7 of Configuration Register #2.

The value of the Time Tag Register will roll over from FFFF (hex) to 0000 after every 65,536 counts (LSB times). When the rollover occurs, a TIME TAG ROLLOVER interrupt request will occur, if enabled by means of the Interrupt Status Register. In addition, the TIME TAG ROLLOVER bit in the Interrupt Status Register will become set following the rollover if (1) the interrupt is enabled, or (2) ENHANCED INTERRUPTS are enabled (ENHANCED MODE **and** bit 15 of Configuration Register #2 is programmed to logic "1").

If CLEAR TIME TAG ON SYNCHRONIZE, bit 6 of Configuration Register #2, is programmed to logic "1," the value of the ACE RT Time Tag Register will be cleared to 0000 following receipt of a Synchronize (without data) mode command. If LOAD TIME TAG ON SYNCHRONIZE, bit 5 of Configuration Register #2, is programmed to logic "1," the value of the received Data Word will be loaded into the ACE RT Time Tag Register following receipt of a valid Synchronize with data mode command and the accompanying Data Word.

Data Block Pointer or Mode Data Word

The third word location within the RT message descriptor is used for two different purposes.

For nonmode code messages, or for mode code messages with ENHANCED MODE CODE HANDLING disabled (bit 15 **or** bit 0 of Configuration Register #3 programmed to logic "0"), the value read from the RT lookup table is stored in this location. This value indicates the starting location of the Data Word block for the respective message.

For mode code messages with data **and** ENHANCED MODE CODE HANDLING enabled (bit 15 **and** bit 0 of Configuration Register #3 programmed to logic "1"), the Data Word that is transmitted or received for a mode code message with data is written to this location during the RT End-of-Message (EOM) sequence.

For mode code messages without data, **no word** is written to the third location of the message block descriptor.

Command Word Received

For all messages, the received Command Word is stored in the fourth location in the message block descriptor during the RT Start-of-Message (SOM) sequence.

RT INTERRUPTS

The ACE offers a great deal of flexibility in terms of RT interrupt processing. In some systems, the transmission or reception of a message with a particular subaddress denotes the end of a complete set of consistent data. In this instance, the user should use the RT SUBADDRESS CONTROL WORD INTERRUPT in order to issue an interrupt request **only for a particular T/R-subaddress**, rather than following every message. One technique would then be for the host processor to switch the active area of shared RAM, by toggling bit 13 of Configuration Register #1 at this time.

An interrupt request for a circular buffer rollover condition (if enabled) will occur only **following the end** of a transmit message during which the last location in the circular buffer has been read **or** following the end of a **valid** receive or broadcast message in which the last location in the circular buffer has been written to.

If ENHANCED MODE CODES are enabled (ENHANCED MODE **and** bit 0 of Configuration Register #3 is logic "1"), interrupts may be enabled following receipt of specific mode code messages. These interrupts may be enabled by means of the Mode Code Selective Interrupt Tabled, address locations 0108-010F in the shared RAM.

IMPLEMENTING BULK DATA TRANSFERS

In systems involving bulk data transfers over the 1553 bus to/from the same subaddress, the host CPU should set the OVERWRITE INVALID DATA bit (bit 11) of Configuration Register #2 and enable the RT CIRCULAR BUFFER ROLLOVER interrupt request. By so doing, the routine transfer of multiple messages to the selected subaddress, **including errors and retries,** is transparent to the host processor. The ACE will issue an interrupt request only after it has received the anticipated number of valid data words to the particular subaddress. The anticipated number of words to be received (or transmitted) is programmable up to 8192 words.

RT COMMAND ILLEGALIZATION

The ACE provides an internal mechanism for RT Command Word illegalizing. The scheme utilizes a 256-word area in the ACE shared RAM space. A benefit of this feature is reduced P.C. board space requirements, by eliminating the need for an external PROM, PLD, or RAM device to perform the illegalizing function. The ACE illegalization scheme provides the maximum in flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/R* bit, subaddress, and word count/mode code to be illegalized. Another advantage of the RAM-based illegalizing technique is that it provides self-testability.

The power turn-on default condition is for RT command illegalization to be **enabled**. Command illegalization may be disabled by first setting bit 15 of Configuration Register #3, ENHANCED MODE, to logic "1" and then setting bit 7 of Configuration Register #3, ILLEGALIZATION DISABLED (while rewriting bit 15, ENHANCED MODE ENABLED, to logic "1"), to logic "1."

If command illegalization is used, address locations 0300 through 03FF are dedicated for the message illegalizing function and **must not** be used for Stack or Data Block storage. If RT command illegalization is disabled, the ACE assumes that all valid, defined, received Command Words are legal. If the illegalization option is disabled, address locations 0300 through 03FF may be used for the storage of the Descriptor Stack or Data Blocks.

It should be noted that the state of the ILLEGALIZATION DISABLED bit in Configuration Register #3 has **no effect** for Bus Controller (BC) or Monitor (MT) modes.

The ACE shared RAM allocates 256 words, address locations 0300 to 03FF (hex), for RT command illegalization. Broadcast commands are illegalized separately from nonbroadcast commands.

Commands may be illegalized down to the word count level. For example, a one-word receive command to subaddress 1 may be legal, while a two-word receive command to subaddress 1 may be illegalized.

Effects of Illegalization

If the ACE RT protocol logic determines that a nonbroadcast message has been illegalized, the ACE will respond with the Message Error bit set in the RT Status Word. If a transmit command has been illegalized, the ACE will respond with its Status Word with the Message Error bit set; **no** Data Words will be transmitted.

If a receive command has been illegalized and the ACE is in non-ENHANCED mode **or** bit 4 of Configuration Register #3, ILLEGAL RECEIVE TRANSFER DISABLE is programmed to logic "0," Data Words received in a BC-to-RT (or RT-to-RT) transfer will be stored to the shared RAM. However, if the ACE is in ENHANCED MODE **and** ILLEGAL RECEIVE TRANSFER DISABLE is programmed TO logic "1," received data words **will not** be stored to RAM.

In the case of an illegalized broadcast command, the ACE will not respond, but will set the Message Error and Broadcast Command Received bits in its internal RT Status Register. If the next message is a Transmit status or Transmit last command mode code, the ACE RT will then respond with the Message Error bit set to logic "1." For a broadcast receive command, the storage or non-storage of Data Words is controlled by the ILLEGAL RECEIVE TRANSFER DISABLE bit, as described above.

If the ACE RT is programmed for the ENHANCED MODE (bit 15 of Configuration Register #3 programmed to logic "1"), ILLEGAL COMMAND WORD, bit 6 of the RT Block Status Word, will be set to logic "1" when the Block Status Word is written to the message block descriptor in the Command Stack during both the Start-of-Message (SOM) **and** End-of-Message (EOM) transfer sequences.

Illegalization Ram Memory Map

TABLE 53. ILLEGALIZING RAM ADDRESS DEFINITION	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	LOGIC “0”
9	LOGIC “1”
8	LOGIC “1”
7	BROADCAST*/OWN ADDRESS
6	T/R*
5	SA4
4	SA3
3	SA2
2	SA1
1	SA0
0(LSB)	WC4/MC4

Notes:

(1) Address bit 7, BRDCST*/OWN ADDR, is logic "0" for broadcast commands, logic "1" for nonbroadcast commands.

(2) Address bit 6, T/R*, is high for transmit commands, low for receive commands.

(3) Bits 5 through 1, SA4 through SA0, define the command subaddress. SA4-SA0 are 00000 or 11111 for mode code commands. SA4-SA0 assume a value between 00001 and 11110 for non-mode code messages.

(4) Address bit 0, WC4/MC4, specifies the MSB of the command's Word Count/Mode Code field: Word Count for $00001 \leq$ SA4-SA0 ≤ 11110, Mode Code for SA4-SA0 = 00000 or SA4-SA0 = 11111. If WC4/MC4 is logic "0," the referenced word in the illegalization RAM is used to program command illegalization for Word Counts/Mode Codes 15 through 0. If WC4/MC4 is logic 1, the referenced word in the command illegalization RAM is used to program illegalization for Word Counts/Mode Codes 31 through 16.

The organization of the illegalization RAM table is illustrated in TABLE 54. As shown, the base address of the illegalization table is 0300 (hex). The index into the illegalizing RAM is formulated by means of

BROADCAST/OWN ADDRESS*, T/R* bit, Subaddress (4-0), and the MSB of the Word Count/Mode Code field (WC4/MC4), as defined by TABLE 53.

Commands may be illegalized down to the Word Count level. For example, a 1-word receive command to subaddress 1 can be legal, while a 2-word receive command can be illegalized.

The first 64 words of the ILLEGALIZATION table are used to illegalize Broadcast Receive Commands (two words per subaddress). The next 64 words refer to Broadcast Transmit Commands. Since nonmode code broadcast transmit commands are not defined by MIL-STD-1553B, the section of the illegalization table between (and including) address locations 0342 and 037D (hex) do **not** need to be programmed by the user. The next 64 words correspond to nonbroadcast receive commands. The final 64 words refer to nonbroadcast transmit commands. Reference TABLE 54.

For each broadcast/own address-T/R*-subaddress, **a pair** of words (32 bits) in the illegalization RAM table are allocated for the purpose of illegalizing any combination of the 32 possible word counts or mode codes.

The programming of the individual words in the illegalization table is defined by TABLE 55.

TABLE 54. ILLEGALIZATION RAM MAP

ADDRESS	DESCRIPTION
0300	Brdcst/Rx, SA 0, MC15-0
0301	Brdcst/Rx, SA 0, MC31-16
0302	Brdcst/Rx, SA 1, WC15-0
0303	Brdcst/Rx, SA 1, WC31-16
.	.
.	.
033F	Brdcst/Rx, SA 31, MC31-16
0340	Brdcst/Tx, SA 0, MC15-0
0341	Brdcst/Tx, SA 0, MC31-16
0342	Brdcst/Tx, SA 1, WC 15-0
.	.
.	.

{Note: Non-Mode Code Broadcast/Transmit Commands (SA1-30) are not defined by MIL-STD-1553B. Therefore, addresses 0342-037D **do not need to be programmed**.}

.	.
.	.

TABLE 54. ILLEGALIZATION RAM MAP (cont.)

.	.
.	.
037D	Brdcst/Tx, SA 30, WC 31-16
037E	Brdcst/Tx, SA 31, MC 15-0
037F	Brdcst/Tx, SA 31, MC 31-16
0380	Own Addr/Rx, SA 0, MC 15-0
0381	Own Addr/Rx, SA 0, MC 31-16
0382	Own Addr/Rx, SA 1, WC 15-0
0383	Own Addr/Rx, SA 1, WC 31-15
.	.
.	.
03BE	Own Addr/RX, SA 31, MC 15-0
03BF	Own Addr/Rx, SA 31, MC 31-16
03C0	Own Addr/Tx, SA 0, MC 15-0
03C1	Own Addr/Tx, SA 0, MC 31-16
03C2	Own Addr/Tx, SA 1, WC 15-0
03C3	Own Addr/Tx, SA 1, WC 31-16
.	.
.	.
03FC	Own Addr/Tx, SA 30, WC 15-0
03FD	Own Addr/Tx, SA 30, WC 31-16
03FE	Own Addr/Tx, SA 31, MC 15-0
03FF	Own Addr/TX, SA 31, MC 31-16

SUBADDRESS ILLEGALIZATION WORD 0

TABLE 55a. ILLEGALIZATION RAM WORD BIT DEFINITIONS : For even numbered addresses (WC/MC4=0)	
BIT	**DESCRIPTION**
15(MSB)	WC/MC = 15 Illegal
14	WC/MC = 14 Illegal
13	WC/MC = 13 Illegal
12	WC/MC = 12 Illegal
11	WC/MC = 11 Illegal
10	WC/MC = 10 Illegal
9	WC/MC = 9 Illegal
8	WC/MC = 8 Illegal
7	WC/MC = 7 Illegal
6	WC/MC = 6 Illegal
5	WC/MC = 5 Illegal
4	WC/MC = 4 Illegal
3	WC/MC = 3 Illegal
2	WC/MC = 2 Illegal
1	WC/MC = 1 Illegal
0(LSB)	WC/MC = 0 Illegal

SUBADDRESS ILLEGALIZATION WORD 1

TABLE 55b. ILLEGALIZATION RAM WORD BIT DEFINITIONS : For odd numbered addresses (WC/MC4=1)	
BIT	**DESCRIPTION**
15(MSB)	WC/MC = 31 Illegal
14	WC/MC = 30 Illegal
13	WC/MC = 29 Illegal
12	WC/MC = 28 Illegal
11	WC/MC = 27 Illegal
10	WC/MC = 26 Illegal
9	WC/MC = 25 Illegal
8	WC/MC = 24 Illegal
7	WC/MC = 23 Illegal
6	WC/MC = 22 Illegal
5	WC/MC = 21 Illegal
4	WC/MC = 20 Illegal
3	WC/MC = 19 Illegal
2	WC/MC = 18 Illegal
1	WC/MC = 17 Illegal
0(LSB)	WC/MC = 16 Illegal

The following should be noted with regards to TABLE 55:

(1) To illegalize a particular word count for a given broadcast/own address-T/R*-subaddress, the appropriate bit position in the respective illegalization word should be programmed to logic "1." A bit value of logic "0" designates the respective Command Word as a legal command.

(2) For subaddresses 00001 through 11110, the "GC/MC" field specifies the Word Count field of the respective Command Word. For subaddresses 00000 and 11111, the "WC/MC" field specifies the Mode Code field of the respective Command Word.

(3) Since nonmode code broadcast transmit messages are not defined by MIL-STD-1553B, the sixty (60) words in the illegalization RAM, addresses 0342 through 037D, corresponding to these commands do not need to be initialized. The ACE will **not** respond to a nonmode code broadcast transmit command, bet will **automatically** set the Message Error bit in its internal Status Word Register, regardless of whether or not corresponding bit in the illegalization RAM has been set. If the next message is a Transmit Status or Transmit Last Command mode code, the ACE will respond with its Message Error bit set.

Accessing the Illegalization Table

In order to use the illegalizing feature, the host processor should write to the 256 words of illegalizing RAM as part of the ACE'S initialization procedure, following power turn-on. After the illegalization RAM has been loaded, the host processor then has the option of reading it back in order to verify. When the illegalization RAM initialization has been completed, the host processor should put the ACE on-line in RT mode by writing to Configuration Register #1.

If desired, the host processor may periodically reread the contents of the illegalization RAM, for continual verification. The ACE's 1553 protocol logic will perform a single read access during the RT Start-of-Message (SOM) sequence. As a result of the read access, the ACE will determine if the particular Command Word has been illegalized by the host CPU. Since the illegalization RAM should not be used for stack or message data (assuming illegalization is enabled), the ACE's 1553 logic will **never** write to this section of memory.

ENHANCED MODE CODE HANDLING

The ACE includes a mechanism for storing Data Words associated with specific mode code commands in individual locations in the shared RAM. In addition, the ACE has the ability to generate selective interrupts for specific mode commands based on a lookup table. These features are enabled in the ACE RT Enhanced mode, by setting ENHANCED MODE bit (bit 15 in Configuration Register #3) to logic "1," followed by setting ENHANCED MODE CODE HANDLING bit (bit 0 in Configuration Register #3) to logic "1."

ENHANCED MODE CODE HANDLING enables three aspects of handling mode code messages:

(1) For all nonmode code messages, and for mode code messages with ENHANCED MODE CODE HANDLING disabled, the third word of the message descriptor block in the stack is reserved for the DATA BLOCK POINTER. Reference FIGURES 11, 12, and 13. The DATA BLOCK POINTER references the starting location of the Data Word block for received or transmitted data. In the case of mode code messages, the Data Word block consists of a single Data Word.

However, for mode code commands with data, if ENHANCED MODE CODE HANDLING is enabled, the third word of the message descriptor in the RT stack will contain the actual **Data Word** transmitted or received, rather than a pointer to the (single word) data block. For mode commands without data, the third word of the descriptor is **not written to**.

(2) ENHANCED MODE CODE HANDLING affects the address mapping of Data Words transmitted or received for mode code messages. With ENHANCED MODE CODE HANDLING enabled, for mode commands with Data Words associated with them (transmit and receive commands 10 to 1F hex), the ACE will read the data from or store the data to **individual (for each mode code) fixed locations** in the RAM. The address locations associated with receive mode commands are 110-11F hex. These locations are accessed based on Mode Code bits 3-0. Transmit mode code data will be read from locations 120-12F based on Mode Code bits 3-0. If the SEPARATE BROADCAST option is selected (bit 0 of Configuration Register #2 is set to logic "1"), broadcast mode code receive Data Words will be stored in locations 130-13F hex . If the SEPARATE BROADCAST option is not selected (bit 0 of Configuration Register #2 is set to logic "0"), broadcast mode receive data will be stored along with the nonbroadcast receive Data Words in locations 110-11F hex. TABLE 56 illustrates the RAM locations for each of the mode commands with data.

(3) Mode code selective interrupts are enabled in the Enhanced ACE RT Mode by setting the ENHANCED MODE CODE HANDLING bit (bit 0 of Configuration Register #3) to logic "1" **and** by setting the RT SELECTED MODE CODE INTERRUPT bit (bit 1 in the Interrupt Mask Register) to logic "1" **and** initializing the MODE COMMAND SELECTIVE INTERRUPT TABLE (locations 108-10F hex in RAM). Entries in the MODE COMMAND SELECTIVE INTERRUPT TABLE are addressed by appending the 3-bit value formed by broadcast, T/R* bit, and MODE CODE bit 4 to the base address of 108 hex. The bit location within this 16-bit word that determines if the given mode command will generate an interrupt is specified by the 4-bit value formed by MODE CODE bits 3-0. If the appropriate bit has been programmed to logic "1," the ACE will generate an interrupt at the end of the current message. Note that some of the possible Command Word combinations are invalid. As long as the Command Word meets the 1553 criteria for word validation, the interrupt will be generated at the end of the message, even if the particular command is illegal or invalid.

Refer to TABLE 57 and TABLE 58.

TABLE 56. ENHANCED MODE CODE DATA LOCATIONS

RAM LOCATION	MODE CODE
0110	UNDEFINED
0111	SYNCHRONIZE WITH DATA
0112	UNDEFINED
0113	UNDEFINED
0114	SELECTED TRANSMITTER SHUTDOWN
0115	OVERRIDE SELECTED TRANSMITTER SHUTDOWN
0116-011F	RESERVED (RECEIVE MODE CODES)
0120	TRANSMIT VECTOR WORD
0121	UNDEFINED
0122	TRANSMIT LAST COMMAND
0123	TRANSMIT BIT WORD
0124	UNDEFINED
0125	UNDEFINED
0126-012F	RESERVED (TRANSMIT MODE CODES)
0130	UNDEFINED BROADCAST
0131	BROADCAST SYNCHRONIZE WITH DATA
0132	UNDEFINED BROADCAST
0133	UNDEFINED BROADCAST
0134	BROADCAST SELECTED TRANSMITTER SHUTDOWN
0135	BROADCAST OVERRIDE SELECTED TRANSMITTER SHUTDOWN
0136-013F	RESERVED BROADCAST

TABLE 57. MODE CODE INTERRUPT LOOKUP TABLE RAM MAP

ADDRESS	DESCRIPTION
0108	Receive Mode Commands 0-15 (Undefined)
0109	Receive Mode Commands 16-31 (With Data)
010A	Transmit Mode Commands 0-15 (Without Data)
010B	Transmit Mode Commands 16-31 (With Data)
010C	Broadcast Receive Mode Commands 0-15 (Undefined)
010D	Broadcast Receive Mode Commands 16-31 (With Data)
010E	Broadcast Transmit Mode Commands 0-15 (Without Data)
010F	Broadcast Transmit Mode Commands 16-31 (Undefined/Reserved)

TABLE 58. SAMPLE MODE COMMAND INTERRUPT LOOKUP TABLE ENTRY (Shown for location 010Ah)

BIT	DESCRIPTION
15(MSB)	RESERVED MODE CODE
14	RESERVED MODE CODE
13	RESERVED MODE CODE
12	RESERVED MODE CODE
11	RESERVED MODE CODE
10	RESERVED MODE CODE
9	RESERVED MODE CODE
8	RESET REMOTE TERMINAL
7	OVERRIDE INHIBIT TERMINAL FLAG
6	INHIBIT TERMINAL FLAG
5	OVERRIDE Tx SHUTDOWN
4	TRANSMITTER SHUTDOWN
3	INITIATE SELF TEST
2	TRANSMIT STATUS
1	SYNCHRONIZE
0(LSB)	DYNAMIC BUS CONTROL

Note: A logic "1" in the selected bit position will enable that command to generate an interrupt.

BROADCAST OPTION

In RT mode, the ACE allows the use of broadcast messages as a software-programmable option. In the non-ENHANCED RT Mode, if the BROADCAST DISABLED bit (bit 7 in Configuration Register #5) is programmed to logic "0," the ACE will recognize RT Address 31 as the broadcast address. If the BROADCAST DISABLED bit is programmed to logic "1," then RT Address 31 will not be recognized as the broadcast address and may be used as a discrete terminal address. MIL-STD-1553B stipulates that RT address 31 shall **not** be assigned as a discrete terminal address.
If broadcast is enabled and the ACE RT receives a broadcast Command Word (RT address 31), followed **contiguously** by a Transmit Command Word to the ACE RT's own address, indicating an RT-to-RTs (broadcast) message, the broadcast Command Word will be superseded and the ACE RT will respond to the transmit command.

BUSY BIT

If the host CPU asserts the BUSY* bit low in Configuration Register #1, the ACE will respond to **any** command with the BUSY bit set in its RT Status Word. Similarly, if ALTERNATE RT STATUS WORD ENABLED (bit 5 of Configuration Register #3) is programmed to logic "1," then the BUSY Status Word Bit is directly controlled by means of bit 4 (S03) of Configuration Register #1. If the ACE is programmed for the non-ENHANCED mode (bit 15 of Configuration Register #3 is logic "0") **or** if BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3 is logic "0," for a receive command, Data Words **will be** written to the data block in the shared RAM referenced by the respective Lookup Table location. If the ACE is programmed for the ENHANCED mode (bit 15 of Configuration Register #3 is logic "1") **and** if BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3 is logic "1," for a nonmode code receive command, Data Words **will <u>NOT</u> be** written to the data block in the shared RAM referenced by the respective Lookup pointer.

For a nonmode code transmit command, the ACE will respond with Status/BUSY, but **no data words** will be transmitted.

If the Alternate RT Status Word option is **not selected**, the ACE may optionally set the busy bit based on broadcast/own RT address, T/R* bit, and subaddress. ALTERNATE STATUS WORD ENABLE is nonselected in the non-ENHANCED mode (bit 15 of Configuration Register #3 set to logic "0") **or** if bit 5 of Configuration Register #3, ALTERNATE STATUS WORD ENABLE, is logic "0."

Assuming that ALTERNATE STATUS WORD is **not enabled**, the ACE's "Busy by Broadcast-T/R*-Subaddress" option is available in the Enhanced RT Mode (bit 15 of Configuration Register #3 set to logic "1") only. The Busy Bit Lookup Table is enabled by setting bit 13 of Configuration Register #2, BUSY LOOKUP TABLE ENABLE, to logic "1."

The Busy Bit Lookup Table occupies eight word locations, 0240 through 0247 (hex). As illustrated in TABLE 59, the offset into the lookup table is formulated for a specific command based on BROADCAST/OWN ADDRESS*, TRANSMIT/RECEIVE*, and the MSB of the Subaddress field (SA4).

For any given BROADCAST/OWN ADDRESS*, and TRANSMIT/RECEIVE* combination, a pair of

words (32 bits) are allocated in the Busy Bit Lookup Table for the purpose of setting the busy bit in response to a command to any of the 32 possible subaddresses. The MSB (SA4) of the subaddress is used to select which word is to be used, and Subaddress bits 3 through 0 (SA3-SA0) are used to determine which of the 16 bits in the selected word is to be used to program a particular subaddress as busy. A logic "0" in the respective bit location indicates that the busy bit will not be set for that command, while a logic "1" indicates that the busy bit will be set in the next response to the next message to the selected subaddress.

If the ACE is Busy for a Transmit Vector Word mode command, a Data Word (Vector Word) will **not** be transmitted in the non-ENHANCED mode **or** if MODE COMMAND OVERRIDE BUSY, bit 13 of Configuration Register #3, is logic "0." Similarly, if the ACE is busy for a Synchronize with data mode command, the Data Word **will** be stored to shared RAM in the non-ENHANCED mode **or** if BUSY RX TRANSFER DISABLE, bit 3 of Configuration Register #3 is logic "0."

If the ACE is programmed for ENHANCED MODE **and** MODE COMMAND OVERRIDE BUSY is programmed to logic "1," then a Data Word **will** be transmitted for a Transmit Vector Word mode code. A Data Word **will** be stored for a Synchronize with data-mode code, even if the ACE is Busy **and** BUSY RECEIVE TRANSFER DISABLE is programmed to logic "1."

If the ACE is Busy for a Transmit BIT Word mode command, the Data Word (BIT Word) **will be transmitted** if the ACE is programmed for its non-ENHANCED MODE **or** if INHIBIT BIT WORD IF BUSY, bit 14 of Configuration Register #4, is logic "0." If the ACE is Busy for a Transmit BIT Word mode command, the Data Word (BIT Word) **will NOT be transmitted** if the ACE is programmed for its ENHANCED MODE **and** if INHIBIT BIT WORD IF BUSY, bit 14 of Configuration Register #4, is logic "1."

TABLE 59. BUSY BIT LOOKUP TABLE ADDRESS DEFINITION	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	LOGIC “0”
9	LOGIC “1”
8	LOGIC “0”
7	LOGIC “0”
6	LOGIC “1”
5	LOGIC “0”
4	LOGIC “0”
3	LOGIC “0”
2	BROADCAST/OWN ADDRESS*
1	T/R*
0(LSB)	SA4

Notes:

(1) Address bit 2, BRDCST/OWN ADDR*, is logic "1" for broadcast commands, logic "0" for nonbroadcast commands.

(2) Address bit 1, T/R*, is high for transmit commands, low for receive commands.

(3) Address bit 0, SA4 specifies the MSB of the command's Subaddress field.

SUBADDRESS BUSY WORD 0

TABLE 60a. BUSY BIT LOOKUP TABLE FOR DEFINITION (For SA4 = 0)	
BIT	**DESCRIPTION**
15(MSB)	SUBADDRESS 15 BUSY
14	SUBADDRESS 14 BUSY
13	SUBADDRESS 13 BUSY
12	SUBADDRESS 12 BUSY
11	SUBADDRESS 11 BUSY
10	SUBADDRESS 10 BUSY
9	SUBADDRESS 9 BUSY
8	SUBADDRESS 8 BUSY
7	SUBADDRESS 7 BUSY
6	SUBADDRESS 6 BUSY
5	SUBADDRESS 5 BUSY
4	SUBADDRESS 4 BUSY
3	SUBADDRESS 3 BUSY
2	SUBADDRESS 2 BUSY
1	SUBADDRESS 1 BUSY
0(LSB)	SUBADDRESS 0 BUSY

SUBADDRESS BUSY WORD 1

TABLE 60b. BUSY BIT LOOKUP TABLE FOR DEFINITION (For SA4 = 1)	
BIT	**DESCRIPTION**
15(MSB)	SUBADDRESS 31 BUSY
14	SUBADDRESS 30 BUSY
13	SUBADDRESS 29 BUSY
12	SUBADDRESS 28 BUSY
11	SUBADDRESS 27 BUSY
10	SUBADDRESS 26 BUSY
9	SUBADDRESS 25 BUSY
8	SUBADDRESS 24 BUSY
7	SUBADDRESS 23 BUSY
6	SUBADDRESS 22 BUSY
5	SUBADDRESS 21 BUSY
4	SUBADDRESS 20 BUSY
3	SUBADDRESS 19 BUSY
2	SUBADDRESS 18 BUSY
1	SUBADDRESS 17 BUSY
0(LSB)	SUBADDRESS 16 BUSY

RT ADDRESS INPUTS

In order for the ACE to respond as an RT to a discrete (nonbroadcast) RT address, the address of a received Command Word must match the value programmed for pins RTAD4-RTAD0, **and** RTADP must be programmed to create an **odd** parity sum with RTAD4-0. Unless broadcast is disabled (broadcast disabled bit 7 of Configuration Register #5 programmed to logic "1."), the ACE's capability to receive messages to the broadcast address, RT address 31 (11111), is not effected by the programming of RTAD4-0 and RTADP. In the ACE's RT mode, the programmed value of the RT Address is sampled approximately 2 µs after the mid-parity zero-crossing of a received Command Word.

Odd parity requires that there be **an odd number of logic "1"s in the RT address** (including the Parity bit). Therefore, RTADP should be programmed to logic "0" for RT addresses 1, 2, 4, 7, 8, 11, 13, 14, 16, 19, 21, 22, 25, 26, 28, and 31 (if broadcast is disabled). RTADP must be programmed to logic "1" for RT addresses 0, 3, 5, 6, 9, 10, 12, 15, 17, 18, 20, 23, 24, 27, 29, and 30.

To update the value held in the internal RT Address latch, the ACE needs to be programmed for the Enhanced Mode of operation (bit 15 of Configuration Register #3 programmed to logic "1"), **and** the LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5 feature enabled (bit 3 of Configuration Register #4 set to logic "1"), and **then** writing the RT address to Configuration Register #5.

It should be noted that a hardware reset, as well as a device Reset to the Status/Control Register, will clear the internal latched RT Address value to 0 (including the address parity bit).

A software reset (writing a logic "1" to bit 0 of the Start/Reset Register) or a Mode Code Reset Command has no effect on the value of the internal RT Address latch.

(NOTE: Only the BU-61586 ACE (BU-65528MX) is capable of RT Address latching; the BU-61585 ACE (BU-65527) only operates in the hardwired RT Address Mode).

RT STATUS WORD

The ACE supports two options for the host processor to program the bits of the RT Status Word:

(1) The standard or "nonalternate" Status Word. For MIL-STD-1553B applications, this option is normally used. In this configuration, the ACE automatically updates the values of the Message Error, Broadcast Command Received, and Dynamic Bus Control bits in accordance with MIL-STD-1553B. The values of the Busy, Service Request, and Subsystem Flag bits are programmable by the host CPU. In addition, the values for the Instrumentation and Reserved bits are automatically set to logic "0" in the RT's Status Word response. There is also an option for the Terminal Flag bit to be automatically set for the response to the subsequent nonbroadcast message following a failure of the ACE RT's on-line self-test.

(2) The "Alternate" status word mode. With this option, **all 11** RT Status Word bits are programmable by the host processor, by means of bits 11 through 1 of Configuration Register #1. This mode may be used to support MIL-STD-1553A, McAir, G.D. F16, or other "non-1553B"

applications.

The default (power turn-on value) is for the standard (1553B) "non-Alternate" Status Word. The ACE configures to this mode in the non-enhanced mode (bit 15 of Configuration Register #3 programmed to logic "0" **or** ALTERNATE STATUS WORD ENABLED, bit 5 of Configuration Register #3 programmed to logic "0").

To configure the ACE RT for the Alternate RT Status Word mode, the ACE must be programmed for by programming bits 15, ENHANCED MODE ENABLED, **and** bit 5, ALTERNATE STATUS WORD ENABLED, of Configuration Register #3, to logic "1."

Both options support command illegalization.

In either of the two modes, the values programmed in Configuration Register #1 are sampled approximately 4 to 5 µs after the mid-parity bit crossing of the received Command Word.

In either of the two modes, the value of the RT Status Word that was transmitted in response to the **last** nonbroadcast message processed by the ACE RT may be read from the read-only RT Status Word Register (register address 01110).

The programming of the ACE RT Status Word bits is summarized in TABLE 61.

TABLE 61. RT STATUS WORD PROGRAMMING OPTIONS

Bit Number (per MIL-STD -1553B)	Bit Function (per MIL-STD-1553B)	Operation in Standard ("non-Alternate") Status Mode	Operation in Alternate Status Mode (See Notes 8 and 9)
1-3	Sync Field	Sync Field	Sync Field
4-8	RT Address	RT Address	RT Address
9	Message Error	Set to logic "1" following an error in the Data Word portion of a received message, or for an illegalized Command Word, in accordance with MIL-STD-1553B. See Note 1.	Controlled by S10, bit 11 of Configuration Register #1. Also, set to logic "1" for illegalized Command Word, in accordance with MIL-STD-1553B. See Note 10.
10	Instrumentation	Logic "0"	Controlled by S9, bit 10 of Configuration Register #1.
11	Service Request	Controlled by means of SERVICE REQUEST*, bit 9 of Configuration Register #1. As an option, may be automatically cleared by a Transmit Vector mode command. See Note 2.	Controlled by S8, bit 9 of Configuration Register #1.
12	Reserved	Logic "0"	Controlled by S7, bit 8 of Configuration Register #1.
13	Reserved	Logic "0"	Controlled by S6, bit 7 of Configuration Register #1.
14	Reserved	Logic "0"	Controlled by S5, bit 6 of Configuration Register #1.
15	Broadcast Command Received	In compliance with MIL-STD-1553B. See Note 3.	Controlled by S4, bit 5 of Configuration Register #1.
16	Busy	Controlled by means of BUSY*, bit 10 of Configuration Register #1 and Busy Lookup Table. See Note 4.	Controlled by S3, bit 4 of Configuration Register #1. Can have an effect on received Data Words. See Note 11.
17	Subsystem Flag	Controlled by means of SUBSYSTEM FLAG*, bit 8 of Configuration Register #1, and SSFLAG* input signal. See note 5.	Controlled by S2, bit 3 of Configuration Register #1.
18	Dynamic Bus Control Accepted	Controlled in accordance with MIL-STD-1553B by means of DYNAMIC BUS CONTROL ACCEPTANCE*, bit 11 of Configuration Register #1. See Note 6.	Controlled by S1, bit 2 of Configuration Register #1.
19	Terminal Flag	In ENHANCED MODE (bit 15 of Configuration Register #3 set to logic "1"), controlled by RTFLAG*, bit 7 of Configuration Register #1. Optionally, may be automatically set as the result of a self-test failure. See Note 7.	Controlled by S0, bit 1 of Configuration Register #1. See Note 12.
20	Parity	Odd parity, per MIL-STD-1553B.	Odd parity, per MIL-STD-1553B.

Notes:

(1) For an error in the Data Word portion of a received message (sync or Manchester encoding, bit count, word count, or parity error), the ACE RT will not respond to the current message. However,

the internal Message Error bit will be set to logic "1." This value will be reflected in the read-only RT Status Word Register.
If the ACE receives a Command Word that has been illegalized by means of the illegalization table (see section on RT COMMAND ILLEGALIZATION), the ACE will respond with the Message Error bit set in its Status Word. An illegalized command will result in ILLEGAL COMMAND WORD, bit 6 of the RT Block Status Word, to be set to logic "1." For an illegalized transmit command, the ACE will transmit the Status Word only with the Message Error bit set; it will **not** transmit any Data Words. For a valid illegalized receive command, the ACE **will store** the received Data Words **unless**: the ACE is in ENHANCED MODE (bit 15 of Configuration Register #3 is logic "1") **and** ILLEGAL RECEIVE TRANSFER DISABLE, bit 4 of Configuration Register #3, is programmed to logic "1." In the latter case, received Data Words **will not** be stored to the ACE shared RAM.

In either case, if the **next** message is a Transmit Status or Transmit Last Command mode code, the ACE RT will respond to the next command with the Message Error bit set to logic "1." To all other subsequent commands, the ACE RT will respond with the Message Error bit set to logic "0."

(2) Note that programming SERVICE REQUEST* to logic **"0"** in Configuration Register #1 results in a value of logic "1" for the Service Request bit transmitted in the RT Status Word. Also, note that this bit is effected by the value programmed for CLEAR SERVICE REQUEST, bit 2 of Configuration Register #2. If CLEAR SERVICE REQUEST is logic "1," the value of SERVICE REQUEST* will automatically clear (to logic "1") **after** the ACE RT has responded to a Transmit Vector Word mode code command. That is, if CLEAR SERVICE REQUEST is logic "1" and SERVICE REQUEST is logic "0," the ACE RT will respond with the Service request bit set to logic "1" until the ACE responds to a Transmit Vector Word command. For this message, the ACE will respond with the Service Request bit still set to logic "1" in its Status Word. **Following** this message, the value of SERVICE REQUEST* clears to logic "1" and stays cleared until re-asserted to logic "0" by the host processor.

(3) In accordance with MIL-STD-1553B, the value of the internal Broadcast Command Received bit will be set to logic "1" following reception of a valid Broadcast Command Word. This value will be reflected in the read-only RT Status Word Register. If the **next** message is a Transmit status or Transmit last command mode code, the ACE RT will respond with the Broadcast command received bit set to logic "1." To all other commands, the ACE will respond with the Broadcast command received bit set to logic "0."

(4) Note that programming BUSY* to logic **"0"** in Configuration Register #1 results in a value of logic "1" for the Busy bit transmitted in the RT Status Word.

If BUSY* is programmed to logic "0" or the ACE receives a Command Word (Bcst, T/R* bit, Subaddress) that has been programmed for a BUSY response by means of the Busy lookup table (see BUSY BIT section), the ACE will respond with the Busy bit set in its Status Word.

For the response to a transmit command when Busy, the ACE will transmit the Status Word only with the Busy bit set; it will **not** transmit any Data Words. For a "Busy" receive command, the ACE **will store** the received Data Words **unless**: the ACE is in ENHANCED MODE (bit 15 of Configuration Register #3 is logic "1") **and** BUSY RECEIVE TRANSFER DISABLE, bit 3 of

Configuration Register #3, is logic "1." In the latter case, received Data Words **will not** be stored in the ACE shared RAM.
In either case, if the **next** message is a Transmit Status or Transmit last Command mode code, the ACE RT will respond with the Busy bit set to logic "1." To all other commands, the ACE will respond with the value of the Busy bit determined by the value of BUSY* in Configuration Register #1 and the programming of the Busy lookup table for **that** command (not the previous command).

(5) Note that programming SUBSYSTEM FLAG* to logic **"0"** in Configuration Register #1 results in a value of logic "1" for the Subsystem Flag bit transmitted in the RT Status Word.

The Subsystem Flag Status Word bit will also be set to logic "1" if the value of logic "0" is sampled on the SSFLAG* input signal during the RT Start-of-Message (SOM) sequence, approximately 4 µs after the mid-parity bit of the received Command Word. A possible use of the SSFLAG* input is to indicate failure of the host CPU, by connecting SSFLAG* to the output of a processor watchdog timer. Note that the value presented on SSFLAG* has **no effect** on the value of the SUBSYSTEM FLAG* bit writer or read in Configuration Register #1. Also, note that the value presented on the SSFLAG* input has no effect in the Alternate RT Status mode.

(6) In accordance with MIL-STD-1553B, the Dynamic Bus Control Acceptance Status Word bit will only be set to logic "1" if SUBSYSTEM FLAG*, bit 8 of Configuration Register #1, is programmed for a value of logic "0" **and** the ACE RT is responding to a Dynamic Bus Control mode command. For all other commands, the Dynamic Bus Control Acceptance Status Word bit will be logic "0." It should be noted that the ACE will **not** automatically switch from RT to BC mode following reception (and acceptance) of a Dynamic Bus Control mode command.

(7) In ENHANCED MODE (bit 15 of Configuration Register #3 programmed to logic "1"), the value of the transmitted RT flag Status Word bit can be set to logic "1" by programming RTFLAG*, bit 7 of Configuration Register #1, to logic "0."

Alternatively, in ENHANCED MODE, the ACE RT may be programmed to automatically transmit logic "1" for the RT Flag Status Word bit following a failure of the ACE RT's on-line self-test. In this case, if the on-line self-test for a particular message fails, the Terminal Flag Status Word bit will be set to logic "1" in the response to the **subsequent** nonbroadcast message. This is done by programming RTFAIL-RTFLAG AUTOWRAP ENABLE, bit 2 of Configuration Register #2, to logic "1."

In RT mode, the self-test is performed for every nonbroadcast message processed by the ACE. The self-test is considered to have failed under either (or both) of two circumstances:

(1)Loop Test Failure. A loopback test is performed on the transmitted portion of every nonbroadcast message. A validity check is performed on the received version of every word transmitted by the ACE. In addition, a bit-by-bit comparison is performed on the last word transmitted by the RT for each message. If either the received version of any transmitted word is determined to be invalid (sync, encoding, bit count, or parity error) and/or the received version of the last word does not match the transmitted version, the looptest is considered to have failed.

(2) Transmitter Timeout. A transmitter timeout condition occurs when the ACE's 668 µs Transmitter Watchdog Timer times out and aborts transmission on the 1553 bus. This indicates a fault in the Manchester II encoder, RT state machine, or word count logic.

(8) In the Alternate Status mode, Status Word bit positions 9 through 19 (per MIL-STD-1553B) are controlled **directly** by means of S10 through S0, bits 11 through 1 of Configuration Register #1. That is, the respective RT Status Word bit are set to logic "1" by programming the respective Configuration Register #1 bits to logic "**1**" (not logic "0").

(9) The following functions **are not applicable** in the Alternate Status Word mode:

(1) Service Request Auto-Clear (Note 2).
(2) Operation of the MIL-STD-1553B Broadcast Command Received bit (Note 3).
(3) SSFLAG* input signal (Note 5).
(4) Operation of the MIL-STD-1553B Dynamic Bus Control Acceptance bit (Note 6).
(5) Effect of the RT on-line self-test on bit 19 ("Terminal Flag," per MIL-STD-1553B) (Note 7).

(10) For an error in the Data Word portion of a received message following a valid Command Word (sync or Manchester encoding, bit count, word count, or parity error), the ACE RT will not respond to the current message. However, the internal Message Error bit will be set to logic "1." This value will be reflected in the read-only RT Status Word Register. It should be noted that the value of this bit has **no effect** on the Message Error bit in the Status Word response to the next message.

If the ACE receives a Command Word that has been illegalized by means of the illegalization table (see RT COMMAND ILLEGALIZATION section), the ACE will respond with the Message Error bit set in its Status Word. An illegalized command will result in ILLEGAL COMMAND WORD, bit 6 of the RT Block Status Word, to be set to logic "1." For an illegalized transmit command, the ACE will transmit the Status Word only with the Message Error bit set; it will **not** transmit any Data Words. For a valid illegalized receive command, the ACE **will store** the received Data Words **unless**: the ACE is in ENHANCED MODE (bit 15 of Configuration Register #3 is logic "1") **and** ILLEGAL RECEIVE TRANSFER DISABLE, bit 4 of Configuration Register #3, is logic "1." In the latter case, received Data Words **will not** be stored in the ACE shared RAM.

(11) If S3, bit 4 of Configuration Register #4, is set to logic "1," the ACE will respond to a transmit command with a Status Word (with bit 16, per MIL-STD-1553B, set to logic "1"), **followed by the**

requested number of Data Words.

If S3 is logic "1," and BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3, is programmed to logic "0," received Data Words **will be stored** to the ACE shared RAM. If both S3 **and** BUSY RECEIVE TRANSFER DISABLE are programmed to logic "1," received Data Words **will not** be stored in the ACE shared RAM.

In the Alternate Status Word mode, the Busy lookup table **will affect** the value of bit 16 ("Busy," per MIL-STD-1553B) for transmitted RT Status Words. However, the Busy lookup table **has no effect** on the transmission or storage of Data Words.

(12) In the Alternate Status Word mode, an RTFAIL condition (wraparound test failure) **will not** affect the value of the RT Flag Status Word bit, regardless of the value of the RTFAIL-RTFLAG AUTOWRAP ENABLE bit, bit 2 of Configuration Register #2.

RT-TO-RT RESPONSE TIMEOUT

The ACE's response timeout time is applicable to RT mode. When the ACE RT is the receiving RT in an RT-to-RT transfer message, the timer is used to determine that the transmitting RT has not responded in time. The value of the RT-to-RT timeout timer corresponds to the time between the mid-parity bit zero crossing of the Transmit Command Word and the mid-sync zero crossing of the transmitting RT's Status Word. In the non-ENHANCED mode, the value of this timer defaults to a nominal value of 18 µs. In order to accommodate long buses, the value of this timeout is programmable by the host processor. In the ENHANCED MODE (bit 15 of Configuration Register #3 programmed to logic "1"), the value of the RT-to-RT timeout is programmable by means of Configuration Register #5, as illustrated in TABLE 62.

TABLE 62. RT-to-RT RESPONSE TIMEOUT SELECT

BIT 10 RESPONSE TIMEOUT SELECT 1	BIT 9 RESPONSE TIMEOUT SELECT 0	RESPONSE TIMEOUT TIME VALUE (µs)
0	0	18.5
0	1	22.5
1	0	50.5
1	1	130

RT BUILT-IN TEST (BIT) WORD

The ACE RT offers two options for implementing the RT Built-In-Test (BIT) Word: an Internal BIT Word and an External BIT Word.

Using the Internal BIT Word option, the ACE RT responds to a Transmit BIT Word mode command with the Status Word, followed by the contents of the ACE RT's internal BIT Word Register. The format and bit descriptions for this word are defined in TABLE 63. With the External BIT Word option, the ACE RT responds with a BIT Word that is stored in a location in the ACE shared RAM. The value of this word is fully software programmable by the host CPU.

In the ENHANCED MODE, it should be noted that the CPU may read the value of the internal BIT Word by means of the read-only BIT Word Register, register address 0F (hex). This register may be read, regardless of whether the ACE RT is programmed to respond with the Internal or External BIT Word.

In the NON-ENHANCED mode, **or** if EXTERNAL BIT WORD ENABLE, bit 15 of Configuration Register #4, is programmed to logic "0," the BIT Word transmitted is accessed from the ACE's internal BIT Word register. This word is defined in TABLE 63.

If the ACE is programmed for ENHANCED MODE (bit 15 of Configuration Register #15 is logic "1") **and** if EXTERNAL BIT WORD ENABLE is programmed to logic "1," the BIT Word transmitted will be read from a memory location. In this case, if ENHANCED MODE CODE HANDLING is disabled

(ENHANCED MODE disabled **or** ENHANCED MODE CODE HANDLING disabled (bit 0 of Configuration Register #3 is programmed to logic "0")), the location accessed for the external BIT Word will be the address referenced by the RT lookup table pointer for subaddress 00000 or subaddress 11111. In this case, it should be noted that for a given subaddress (00000 or 1!111), the **same** Data Word will be transmitted in response to either a Transmit BIT Word **or** a Transmit vector word mode command.

If ENHANCED MODE CODES are enabled (ENHANCED MODE **and** ENHANCED MODE HANDLING enabled (bit 0 of Configuration Register #3 is programmed to logic "1")), the external BIT Word will be accessed from address location 0123.

If the ACE is Busy (either globally, or for Transmit subaddress 00000 or 11111), for a Transmit BIT Word mode command, the Data Word (BIT Word) **will be transmitted** if the ACE is programmed for its non-ENHANCED MODE **or** if INHIBIT BIT WORD IF BUSY, bit 14 of Configuration Register #4, is logic "0." If the ACE is Busy for a Transmit BIT Word mode command, the Data Word (BIT Word) **will NOT be transmitted** if the ACE is programmed for its ENHANCED MODE **and** if INHIBIT BIT WORD IF BUSY, bit 14 of Configuration Register #4, is logic "1."

The bit map and bit descriptions for the internal RT Built-in-Test (BIT) Word are indicated below.

TABLE 63. RT BIT WORD

BIT	DESCRIPTION
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	RESERVED
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	CHANNEL B/A*
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

Notes for TABLE 63: Bits 15 through 9 are cleared only following a MSTCLR* input, a software reset via the Start/Reset Register, or reception of a Reset Remote Terminal mode command. Bits 8 through 0 are updated as a result of every message processed.

TRANSMITTER TIMEOUT: Set if the ACE's failsafe timer detected a fault condition. The transmitter timeout circuit will automatically shut down the CH. A or CH. B transmitter if it transmits for longer than 668 µs. In RT mode, the ACE will terminate the processing of the current message as the result of a transmitter timeout, however, it **will respond** to the next message received.

CH. B LOOP TEST FAILURE, CH. A LOOP TEST FAILURE: A loopback test is performed on the transmitted portion of every nonbroadcast message. A validity check is performed on the received version of every word transmitted by the ACE. In addition, a bit-by-bit comparison is performed on the last word transmitted by the RT for each message. If either the received version of any transmitted word is determined to be invalid (sync, encoding, bit count, or parity error) and/or the received version of the last transmitted word does not match the transmitted version, or a failsafe timeout occurs on the respective channel, the LOOP TEST FAILURE bit for the respective bus channel will be set.

CH. B TRANSMITTER SHUTDOWN, CH. A TRANSMITTER SHUTDOWN: Indicates that the transmitter on the respective bus channel has been shut down by a Transmitter shutdown mode code command received on the alternate channel. If an Override transmitter shutdown mode code command is received on the alternate channel, this bit will revert back to logic "0."

TERMINAL FLAG INHIBITED: Set to logic "1" if the ACE's Terminal Flag RT Status bit has been disabled by an Inhibit terminal flag mode code command. Will revert to logic "0" if an Override inhibit terminal flag mode code command is received.

CH. A*/CH. B: Logic "0" if the previous message was received on CH. A, logic "1" if the previous message was received on CH. B.

HIGH WORD COUNT: Set to logic "1" if the previous message had a high word count error.

LOW WORD COUNT: Set to logic "1" if the previous message had a low word count error.

INCORRECT SYNC TYPE RECEIVED: If set, indicates that the ACE detected a Command sync in a received Data Word.

INVALID WORD: Indicates that the ACE RT received a Data Word containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

RT-to-RT GAP/SYNC/ADDRESS ERROR: This bit is set if the ACE RT is the receiving RT for an RT-to-RT transfer and one or more of the following occur: (1) If the GAP CHECK ENABLED bit (bit 8) of

Configuration Register #5 is set to logic "1" and the transmitting RT responds with a response time of less than 4 µs, per MIL-STD-1553B (mid-parity bit to mid-sync); i.e., less than 2 µs dead time; and/or (2) There is an incorrect sync type or format error (encoding, bit count, and/or parity error) in the transmitting RT Status Word; and/or (3) The RT address field of the transmitting RT Status Word does not match the RT address in the transmit Command Word.

RT-to-RT RESPONSE TIMEOUT: If set, indicates that, for the previous message, the ACE was the receiving RT for an RT-to-RT transfer **and** that the transmitting RT either did not respond or responded later than the ACE's RT-to-RT Timeout time. The ACE's RT-to-RT Response Timeout Time is defined as the time from the mid-bit crossing of the parity bit of the transmit Command Word to the mid-sync crossing of the transmitting RT Status Word. The value of the RT-to-RT Response Timeout is nominally 18.5 µs in the non-Enhanced mode, or programmable from among nominal values of 18.5, 22.5, 50.5, or 130 µs in the enhanced mode.

RT-to-RT SECOND COMMAND ERROR: If the ACE is the receiving RT for an RT-to-RT transfer, this bit set indicates one or more of the following error conditions in the transmit Command Word: (1) T/R bit = logic "0"; (2) subaddress = 00000 or 11111; (3) same RT Address field as the receive Command Word.

COMMAND WORD CONTENTS ERROR: Indicates a received command word is not defined in accordance with MIL-STD-1553B. This includes the following undefined Command Words: (1) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** the Command Word is a nonmode code, broadcast, transmit command; (2) The OVERRIDE MODE T/R* ERROR bit, bit 6 of Configuration Register #3, is logic "0" **and** a message with a T/R* bit of "0," a subaddress/mode field of 00000 or 11111 and a mode code field between 00000 and 01111; (3) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** a mode code command that is not permitted to be broadcast (eg., Transmit status) is sent to the broadcast address (11111).

RT START-OF-MESSAGE AND END-OF-MESSAGE TRANSFER SEQUENCES

Approximately 1.25 µs following the mid-parity bit crossing of a received Command Word, the ACE performs the RT Start-of-Message (SOM) sequence. Approximately 6 µs after the end of the last word transmitted by the RT (or received, for a broadcast message), the ACE performs the RT End-of-Message (EOM) Sequence. The SOM and EOM sequences consist of sequences of words read from and written to the ACE's shared RAM. The SOM and EOM sequences are summarized below:

RT Start-of-Message (SOM) Sequence.

1) If command illegalization is used, the appropriate illegalization word is read from the Illegalization lookup table.

2) The Stack Pointer address is read from the active area Stack Pointer location. This address is used for accessing the RT descriptor block in the Command Stack.

3) If the selective Busy (by Bcst, T/R* bit, subaddress) option is used, the appropriate "Busy" word is read from the Busy lookup table.

4) If ENHANCED RT MEMORY MANAGEMENT is enabled (bit 1 of Configuration Register #2 programmed to logic "1"), allowing the use of circular buffers and/or double buffering, the Subaddress Control Word is read from the Subaddress Control Word portion of the RT lookup table.

5) With the exceptions of a mode command with no Data Word or ENHANCED MODE CODE HANDLING enabled, the Data Block Address is read from the appropriate RT lookup table location.

6) The Command Word is written to the fourth location in the block descriptor.

7) With the exceptions of a mode command with no Data Word or ENHANCED MODE CODE HANDLING enabled, the Data Block address is written to the third location in the block descriptor.

8) The Time Tag word is written to the second location in the block descriptor.

9) The Block Status Word is written to the first location in the block descriptor. The value of the block status word is 4000 (SOM and all status bits cleared).

10) The value of the Stack Pointer read in step 2 is incremented by four and written to the active area Stack Pointer location.

RT End-of-Message (EOM) Sequence.

1) If the current message is using circular buffering or double buffering, the Subaddress Control Word is read from the Subaddress Control Word section of the RT lookup table.

2) If the current message is using receive subaddress double buffering, the Data Block Address is read from the RT lookup table; **or,** if the message was a mode command with data **and** ENHANCED MODE CODE HANDLING is enabled, the Data Word transmitted or received for a mode code message with data is written to the third location in the block descriptor. If ENHANCED MODE CODE HANDLING is enabled, **no** word is stored to the third location in the RT descriptor for a mode code message without data.

3) If the current message is using circular buffering or double buffering and the pointer address needs to be updated, the updated value of the pointer is written to the RT lookup table.

4) The Time Tag word is written to the second location in the block descriptor.

5) The Block Status Word is written to the first location of the block descriptor.

SUMMARY OF RT EXCEPTION CONDITIONS

In response to various message errors and other exception conditions, the ACE remote terminal takes actions and provides a number of indications. TABLE 64 indicates the respective RT response and effect on the RT Status Word, Block Status Word bits that will be set, RT Built-in-Test (BIT) Word bits, and interrupt requests that are issued and Interrupt Status Register bits that become set as a result of these conditions.

It should be noted that the responses to error conditions for Mode code messages are delineated separately, in TABLE 65.

TABLE 64. RT EXCEPTION CONDITIONS

Exception condition	RT Response, Effect on RT Status Word Register Bits	RT Block Status Word Bits (assuming Enhanced Mode)	RT Built-in-Test (BIT) Word Bits	Interrupt Conditions, Interrupt Status Register Bits (if enabled)
Invalid Command Word	No response (message ignored)	None (No SOM or EOM sequence)	No effect	None
RT Address Parity Error	RT will not receive words or respond to messages sent to its own RT address. RT **will** receive words to the broadcast address (31), unless BROADCAST DISABLED, bit 7 of Configuration Register #5, is logic "1." For a broadcast message, the Broadcast Command Received bit is set to logic "1" in the internal Status Word Register.	No Block Status Word for a message to the RT's own address. Normal Block Status Word, including EOM bit, for a broadcast message (if enabled).	None	RT ADDRESS PARITY ERROR
Command Type Sync in Data Word Following Reception of Valid Command Word	No response. MESSAGE ERROR bit set in internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, FORMAT ERROR, INCORRECT DATA SYNC, INVALID WORD	INCORRECT SYNC RECEIVED	END OF MESSAGE; FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE
Valid Command Word Followed by Reception of Invalid Data Word(s) (Manchester encoding, bit count, parity)	No response. MESSAGE ERROR bit set in internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, FORMAT ERROR, INVALID WORD	PARITY/ MANCHESTER ERROR RECEIVED	END OF MESSAGE; FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if

TABLE 64. RT EXCEPTION CONDITIONS

Exception condition	RT Response, Effect on RT Status Word Register Bits	RT Block Status Word Bits (assuming Enhanced Mode)	RT Built-in-Test (BIT) Word Bits	Interrupt Conditions, Interrupt Status Register Bits (if enabled)
				selected)
Valid Command Word Followed by Incorrect Number of Data Words	No response. MESSAGE ERROR bit set in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, FORMAT ERROR, WORD COUNT ERROR	HIGH WORD COUNT or LOW WORD COUNT	END OF MESSAGE; FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected)
ACE is receiving RT in a correct RT-to-RT transfer sequence	Normal Status Word response. If the message was received to the broadcast address, the Broadcast Command Received bit is set to logic "1" in the internal Status Word Register.	EOM, RT-to-RT FORMAT	None	END OF MESSAGE; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected) (CHECK IF SELECTED)
RT-to-RT Timeout: ACE is Receiving RT in an RT-to-RT Transfer and the transmitting RT Does Not Respond in Time	No response. MESSAGE ERROR bit set in internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, NO RESPONSE TIMEOUT	RT-to-RT, NO RESPONSE ERROR	FORMAT ERROR; END OF MESSAGE; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected) (AT SET)
ENHANCED MODE CODE disabled or ENHANCED MODE CODE HANDLING disabled; Receive valid, defined mode code message (including RESERVED mode codes).	If the message is a Transmit Status or Transmit Last Command mode code, the RT Status Word resulting from the previous message is transmitted and the internal Status Word is not updated. Otherwise, may affect the following RT Status Word bits, as applicable: MESSAGE ERROR (if illegal), BUSY (per Configuration Register #1 and Busy lookup table), DYNAMIC BUS CONTROL ACCEPTANCE, TERMINAL	EOM; if illegal command: ILLEGAL COMMAND	Any of the following may be set or cleared, as applicable: TERMINAL FLAG INHIBITED, TRANSMITTER SHUTDOWN A, TRANSMITTER	RT SUBADDRESS CONTROL WORD; EOM (if Selected)

TABLE 64. RT EXCEPTION CONDITIONS

Exception condition	RT Response, Effect on RT Status Word Register Bits	RT Block Status Word Bits (assuming Enhanced Mode)	RT Built-in-Test (BIT) Word Bits	Interrupt Conditions, Interrupt Status Register Bits (if enabled)
	FLAG. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register. The lookup table pointer value for subaddress 0 or 31 is stored in the third location of the message block descriptor. For a Transmit Last Command or Transmit BIT Word mode command (unless EXTERNAL BIT WORD is enabled), the Data Word transmitted is read from an internal register. For other mode commands with data, the Data Word is accessed from/to the location referenced by the lookup table pointer for subaddress 0 or 31.		SHUTDOWN B.	
ENHANCED MODE enabled and ENHANCED MODE CODE HANDLING enabled; Receive valid, defined mode code message (including RESERVED mode codes).	If the message is a Transmit Status or Transmit Last Command mode code, the RT Status Word resulting from the previous message is transmitted and the internal Status Word is not updated. Otherwise, affects the following RT Status Word bits, as applicable: MESSAGE ERROR (if illegal), BUSY (per Busy lookup table), DYNAMIC BUS CONTROL ACCEPTANCE, TERMINAL FLAG. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register. For a Transmit Last Command or Transmit BIT Word (unless	EOM; if illegal command: ILLEGAL COMMAND	Any of the following may be set or cleared, as applicable: TERMINAL FLAG INHIBITED, TRANSMITTER SHUTDOWN A, TRANSMITTER SHUTDOWN B.	RT MODE CODE (if selected for the particular mode command by means of the Mode Code Selective Interrupt Table, locations 0108-010F); EOM

TABLE 64. RT EXCEPTION CONDITIONS

Exception condition	RT Response, Effect on RT Status Word Register Bits	RT Block Status Word Bits (assuming Enhanced Mode)	RT Built-in-Test (BIT) Word Bits	Interrupt Conditions, Interrupt Status Register Bits (if enabled)
	EXTERNAL BIT WORD is enabled) mode command, the Data Word transmitted is read from an internal register. For other mode codes with data, the Data Word is accessed from/to the mode code Data Word table, address locations 0110-013F, which is mapped by broadcast, T/R*, and MC3-MC0. In addition, the Data Word received or transmitted will be stored in the third location in the message block descriptor.			
Loop Test Failure: **The received version of a transmitted word was determined to be invalid (encoding, bit count, parity) and/or the received version of the last word transmitted did not match the transmitted version.**	If ENHANCED MODE is enabled **and** RTFAIL-RTFLAG WRAP ENABLE, bit 2 of Configuration Register #3 is logic "1," the Terminal Flag Status Word bit will be set to logic "1" in response to the next nonbroadcast message.	EOM, ERROR FLAG, LOOP TEST FAIL	LOOP TEST FAILURE A or LOOP TEST FAILURE B	FORMAT ERROR; EOM; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected)
Transmitter Timeout: **The transmitter failsafe timer timed out after the ACE RT attempted to transmit for longer than 668 µs.**	Response is terminated as a result of the timeout. If ENHANCED MODE is enabled and RTFAIL-RTFLAG WRAP ENABLE, bit 2 of Configuration Register #3, is logic "1," the Terminal flag Status Word bit will be set to logic "1" in response to the next nonbroadcast message. A Transmitter Timeout has **no effect** on the RT responding to subsequent messages.	EOM	TRANSMITTER TIMEOUT	EOM, RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected)
ENHANCED	The RT responds with the	EOM, ILLEGAL	None	RT

TABLE 64. RT EXCEPTION CONDITIONS

Exception condition	RT Response, Effect on RT Status Word Register Bits	RT Block Status Word Bits (assuming Enhanced Mode)	RT Built-in-Test (BIT) Word Bits	Interrupt Conditions, Interrupt Status Register Bits (if enabled)
MODE and Valid receive Command Word received that has been illegalized by means of the illegalization table	Message Error bit set. The Message Error bit is set to logic "1" in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register. If ILLEGAL RECEIVE TRANSFER DISABLE, bit 4 of Configuration Register #3, is set to logic "0," received Data Words are stored to the shared RAM. If ILLEGAL RECEIVE TRANSFER DISABLE is programmed to logic "1," received Data Words are not stored to the shared RAM.	COMMAND WORD, FORMAT ERROR		SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); FORMAT ERROR; END OF MESSAGE
ENHANCED MODE and Valid transmit Command Word received that has been illegalized by means of the illegalization table	The RT responds with the Message Error bit set. No Data Words are transmitted. The Message Error bit is set to logic "1" in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ILLEGAL COMMAND WORD	None	RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE
ENHANCED MODE and RT is Busy for a valid receive Command (either globally, or in response to a particular valid receive command)	The RT responds with the Busy bit set. The Busy bit is set to logic "1" in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register. If BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3, is set to logic "0," received Data Words are stored to the shared RAM. If BUSY RECEIVE TRANSFER	EOM, ERROR FLAG, FORMAT ERROR	None	RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); FORMAT ERROR; END OF MESSAGE

TABLE 64. RT EXCEPTION CONDITIONS

Exception condition	RT Response, Effect on RT Status Word Register Bits	RT Block Status Word Bits (assuming Enhanced Mode)	RT Built-in-Test (BIT) Word Bits	Interrupt Conditions, Interrupt Status Register Bits (if enabled)
	DISABLE is programmed to logic "1," received Data Words are not stored to the shared RAM.			
ENHANCED MODE and RT is Busy for a valid Transmit Command (either globally, or in Response to a Particular Valid Transmit Command)	The RT responds with the Busy bit set. No Data Words are transmitted. The Busy bit is set to logic "1" in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ILLEGAL COMMAND WORD	None	RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE
ENHANCED MODE and the ACE RT is the receiving RT in an RT-to-RT transfer and: **GAP CHECK ENABLED, bit 8 of Configuration Register #5, is programmed to logic "1" and the transmitting RT's response time gap is less than 2 µs,** **or** **Incorrect Sync Type or Format Error (encoding, bit count and/or parity) in the transmitting RT's Status Word,** **or** **The RT Address in**	No RT response. The Message Error bit is set to logic "1" in the internal RT Status Word. If the message was received at the broadcast address, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, FORMAT ERROR, RT-RT GAP/SYNC/ ADDRESS ERROR	RT-RT GAP/SYNC/ ADDRESS ERROR	FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE

TABLE 64. RT EXCEPTION CONDITIONS

Exception condition	RT Response, Effect on RT Status Word Register Bits	RT Block Status Word Bits (assuming Enhanced Mode)	RT Built-in-Test (BIT) Word Bits	Interrupt Conditions, Interrupt Status Register Bits (if enabled)
the Transmitting RT's Status Word does not match the RT address in the transmit Command Word.				
ENHANCED MODE and the ACE RT is receiving RT in RT-to-RT Transfer and: **Error in Command Word to Transmitting RT:** **T/R* bit = 0,** **or** **subaddress = 00000, or 11111,** **or** **same RT address as receive Command Word.**	No RT response. The Message Error bit is set to logic "1" in the internal RT Status Word. If the message was received at the broadcast address, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, FORMAT ERROR, RT-RT SECOND COMMAND ERROR	RT-RT SECOND COMMAND WORD ERROR	FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE
ENHANCED MODE and ACE is Receiving RT for RT-to-RT Transfer and there is an error in the Transmitting RT's Response: sync or Manchester encoding, bit count, parity, word count. This includes a response by the transmitting RT with the	No RT response. The Message Error bit is set to logic "1" in the internal RT Status Word. If the message was received at the broadcast address, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, FORMAT ERROR, and one of the following: WORD COUNT ERROR or INCORRECT DATA SYNC or INVALID WORD	One of the following (as appropriate): HIGH WORD COUNT or LOW WORD COUNT or INCORRECT SYNC RECEIVED or PARITY/	FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected): END OF MESSAGE

TABLE 64. RT EXCEPTION CONDITIONS

Exception condition	RT Response, Effect on RT Status Word Register Bits	RT Block Status Word Bits (assuming Enhanced Mode)	RT Built-in-Test (BIT) Word Bits	Interrupt Conditions, Interrupt Status Register Bits (if enabled)
Message Error and/or Busy bits set to logic "1," followed by no Data Words.			MANCHESTER ERROR RECEIVED	
ENHANCED MODE and Command Word Contents Error: **BROADCAST DISABLED is programmed to logic "0" and Command is a non-mode code transmit broadcast command,** **or** **BROADCAST DISABLED is programmed to logic "0" and message is a broadcasted - 1553B mode code that is not permitted to be broadcast,** **or** **OVERRIDE MODE T/R* ERROR is logic "0" and a Command Word has a T/R* bit of 0, a subaddress/mode field of 00000 or 11111, and a mode code field between 00000 and 01111.**	No RT response. The Message Error bit is set to logic "1" in the internal RT Status Word. If the message was a broadcast command, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, FORMAT ERROR, COMMAND WORD CONTENTS ERROR	COMMAND WORD CONTENTS ERROR	FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected): END OF MESSAGE
Superseded	The ACE RT will abort	The Block Status Word	None	There will be no

TABLE 64. RT EXCEPTION CONDITIONS

Exception condition	RT Response, Effect on RT Status Word Register Bits	RT Block Status Word Bits (assuming Enhanced Mode)	RT Built-in-Test (BIT) Word Bits	Interrupt Conditions, Interrupt Status Register Bits (if enabled)
Message: **RT receives an incomplete message on one bus, followed by a gap with a maximum time of between 6 and 10 µs, followed by a new valid message on the same bus or alternate bus,** **or** **RT is responding to a transmit message on one bus and receives the start of a valid message on the alternate bus.**	processing of the first (superseded) message and respond in full to the second (superseding) message. If either message was broadcast, the Broadcast Command Received bit is set to logic "1" in the internal Status Word Register. If the second message was not a broadcast message, or a Transmit Status or Transmit Last Command mode code, the Broadcast Command Received bit in the internal RT Status Word Register is cleared to logic "0." If broadcast is enabled **and** the ACE RT receives a broadcast Command Word (RT address 31), followed **contiguously** by a Transmit Command Word to the ACE RT's own address, indicating an RT-to-RTs (broadcast) message, the broadcast Command Word will be superseded and the ACE RT will respond to the transmit command.	stored during the Start-of-Message (SOM) sequence for the first message remains stored in the block descriptor for that (superseded) message. This word will have an EOM bit of logic "0" and an SOM bit of logic "1." The Block Status Word for the second message will be stored at an address four locations above (modulo the stack size) that of the Block Status Word for the first message. Assuming that the second message is not itself superseded, its Block Status Word will have an EOM bit of logic "1," and an SOM bit of logic "0". All other bits will be valid for the second message.		interrupts following the first message. For the second message: RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE

SUMMARY OF RESPONSES TO MODE CODE MESSAGES

In the "1553B" Mode Codes configuration, the ACE implements all MIL-STD-1553B mode codes applicable to dual redundant bus operation. The ACE's responses to mode codes, including responses to various error conditions, are summarized below.

TABLE 65. MODE CODE SUMMARY

T/R BIT	MODE CODE	FUNCTION	DATA WORD	BROADCAST ALLOWED
0	00000-01111	Undefined (see Note 1)	No	No
1	00000	Dynamic Bus Control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	No
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag	No	Yes
1	00111	Override Inhibit Terminal Flag	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	01001-01111	RESERVED	No	TBD
1	10000	Transmit Vector Word	From Memory	No
0	10001	Synchronize with Data	To Memory (and, possibly, to Time Tag Register, see Note 2)	Yes
!	10010	Transmit Last Command	From Internal Register	No
1	10011	Transmit BIT Word	From Internal Register or RAM location (see Note 3)	No
0	10100	Selected Transmitter Shutdown (see Note 4)	To Memory	Yes
0	10101	Override Selected Transmitter Shutdown (see Note 4)	To Memory	Yes
0	10110-11111	RESERVED	Yes	TBD
1	10110-11111	RESERVED	Yes	TBD

Notes for TABLE 65:

1) Receive mode commands 00000 through 01111 are undefined per MIL-STD-1553B. If the ACE RT is not in ENHANCED MODE **or** if OVERRIDE MODE CODE T/R* BIT ERROR, bit 6 of

Configuration Register #3, is programmed to logic "0," the ACE RT will not respond and the Message Error bit will be set in the internal Status Word Register. If the ACE is in ENHANCED MODE **and** OVERRIDE MODE CODE T/R* BIT ERROR is programmed to logic "1," the ACE RT will treat the message as a RESERVED mode command. That is, it will respond with Status, with a Message Error bit of logic "0" (unless the command has been illegalized).

2) If LOAD TIME TAG ON SYNCHRONIZE, bit 5 of Configuration Register #2, is programmed to logic "1," the received Data Word is stored to the Time Tag Register.

3) In the non-ENHANCED mode, or if EXTERNAL BIT WORD ENABLE, bit 15 of Configuration Register #4, is programmed to logic "0," the BIT Word defined by TABLE 63 and stored in the ACE's BIT Word Register is transmitted. If the ACE is programmed for ENHANCED MODE (bit 15 of Configuration Register #15 is logic "1") **and** if EXTERNAL BIT WORD ENABLE is programmed to logic "1," the BIT Word transmitted will be read from a memory location. Refer to the section on the Transmit BIT Word mode command.

4) Terminal responds with Clear Status but no action is taken.

Detailed Functional Description of Mode Codes ("1553B" IMPLEMENTATION)

DYNAMIC BUS CONTROL (T/R* = 1; 00000)

MESSAGE SEQUENCE = DBC----STATUS

The ACE responds with Status. If the host processor has written a logic "0" to the DB ACCEPT* bit in Configuration Register #1 (bit 11), the DYNAMIC BUS CONTROL ACCEPTANCE bit will be logic "1" in the RT Status Word. If the ACE responds with the DYNAMIC BUS CONTROL ACCEPTANCE bit set, the ACE **remains in RT mode** until directed to switch to BC mode by the CPU.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.
2) Command Followed by Data Word. No Status response. Set Message error bit (Status Word), High Word Count (BIT Word).
3) T/R* bit set to zero. No Status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4) Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).
5) Broadcast Address. No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).

SYNCHRONIZE WITHOUT DATA WORD (T/R* = 1; 00001)

MESSAGE SEQUENCE = SYNC----STATUS

The ACE responds with Status. If sent as a broadcast, the Broadcast Received bit will be set and Status response suppressed. If the CLEAR TIME TAG ON SYNCHRONIZE option is enabled (bit 6 in Configuration Register #2 programmed to logic "1") the ACE will clear its internal time tag register to zero upon receipt of this mode code.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.
2) Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3) T/R* bit set to zero. No Status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4) Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).

TRANSMIT STATUS WORD (T/R* = 1; 00010)

MESSAGE SEQUENCE = TRANSMIT STATUS----STATUS
The Status register is **not** updated before it is transmitted and contains the resulting status from the previous command (assuming that it was not a Transmit status or Transmit last command mode command).

ERROR CONDITIONS

1. Invalid Command. No response, command ignored.
2. Command Followed by Data Word. No Status response. Set Message Error bit (Status Word)
3. T/R* bit set to zero. No Status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).
5. Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Contents Error (BIT Word).

INITIATE SELF-TEST (T/R* = 1; 00011)

MESSAGE SEQUENCE = SELF-TEST----STATUS

The ACE responds with Status. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. If the message was nonbroadcast, the normal Loopback self-test is performed on the transmitted Status Word. If the test fails, the Terminal flag bit is automatically set in the RT's internal Status Word Register. This result will be reflected in the status response to the **next** nonbroadcast message (assuming that the RTFAIL-RT FLAG WRAP ENABLE bit, bit 2, in Configuration Register #3 is programmed to logic "1"). The loopback self-test is completed approximately 5 µs after the mid-parity bit crossing of the transmitted Status Word.

ERROR CONDITIONS

1. Invalid Command. No response, command ignored.
2. Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. T/R* bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).
5. Loopback Test Fails. Set Terminal Flag bit in internal Status register (Status Word for next nonbroadcast command), Current Channel (A or B) Loop Test Failure and CH A/B Loop Test Failure (BIT Word), assert RT Fail output.

TRANSMITTER SHUTDOWN (T/R* = 1; 00100)

MESSAGE SEQUENCE = SHUTDOWN----STATUS

This command is only used with dual redundant bus systems. The ACE responds with Status. Following the Status transmission, the ACE inhibits any further transmission from the alternate redundant channel. Once shutdown, the transmitter can only be reactivated by an Override Transmitter Shutdown or Reset RT mode command, a Software Reset (writing logic "1" to bit 0 in the Start/Reset Register), or Hardware Reset (MSTRCLR input). Note that the receivers on both channels are always active, even when the transmitters are inhibited.

ERROR CONDITIONS

1. Invalid Command. No response, command ignored.
2. Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. T/R* bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

OVERRIDE TRANSMITTER SHUTDOWN (T/R* = 1; 00101)

MESSAGE SEQUENCE = OVERRIDE SHUTDOWN----STATUS

This command is only used with dual redundant bus systems. The ACE responds with Status. At the end of the Status transmission, the ACE reactivates the transmitter of the alternate redundant bus. If the command was broadcast, the Broadcast Command Received Status Word bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. Invalid Command. No response, command ignored.
2. Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. T/R* bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

INHIBIT TERMINAL FLAG BIT (T/R* = 1; 00110)

MESSAGE SEQUENCE = INHIBIT TERMINAL FLAG----STATUS

The ACE responds with Status and inhibits further setting of the Terminal Flag bit in its internal Status Word register. Once the Terminal Flag has been inhibited, it can only be reactivated by an Override Inhibit Terminal Flag or Reset RT mode code commands, or by Reset. If the command was broadcast, the Broadcast Received bit is set, the state of the Terminal Flag bit in the internal Status Word register remains unchanged and Status transmission is suppressed.

ERROR CONDITIONS

1. Invalid Command. No response, command ignored.
2. Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. T/R* bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

OVERRIDE INHIBIT TERMINAL FLAG BIT (T/R* = 1; 00111)

MESSAGE SEQUENCE = OVERRIDE INHIBIT TERMINAL FLAG---- STATUS

The ACE responds with Status and reenables the Terminal Flag bit in its internal Status register. If the command was a broadcast, the Broadcast Command Received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. Invalid Command. No response, command ignored.
2. Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. T/R* bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

RESET REMOTE TERMINAL (T/R* = 1; 01000)

MESSAGE SEQUENCE = RESET REMOTE TERMINAL----STATUS

The ACE responds with Status and internally resets. The Message Error and Broadcast Command Received bits of the internal Status register are reset to 0. The internal BIT Word Register is reset to 0. If either of the 1553 transmitters has been shut down, the shutdown condition is overridden. If the Terminal Flag bit has been inhibited, the inhibit is overridden. The receipt of this command **does not** reset any of the ACE's host programmable registers.

If the command is received as a broadcast, the Broadcast Command Received bit is set and the Status Word is suppressed. Also, if the command is received as a broadcast and the Terminal Flag bit had been set as a result of the Loopback test of the previous message, the Terminal Flag bit is not reset to zero. The resulting operation is completed approximately 8 μs after the mid-parity bit crossing of the Reset mode code command.

ERROR CONDITIONS

1. Invalid Command. No response, command ignored.
2. Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. T/R* bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

RESERVED MODE CODES (T/R*=1; 01001 - 01111)

MESSAGE SEQUENCE = RESERVED MODE CODES----STATUS

The ACE responds with status. If the command has been illegalized by means of the illegalization table, the Message Error Status Word bit will be set.

ERROR CONDITIONS

1. Invalid Command. No response, command ignored.
2. Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. T/R* bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).
4. Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

TRANSMIT VECTOR WORD (T/R* = 1; 10000)

MESSAGE SEQUENCE = TRANSMIT VECTOR WORD----STATUS/VECTOR WORD

The ACE transmits a Status Word followed by a Vector Word. If the ENHANCED MODE CODES are enabled (bit 15 in Configuration Register #3 set to logic "1") the contents of the Vector Word are obtained from RAM location 120 (hex). If ENHANCED MODE CODES are not enabled, the single word data block in the shared RAM that is referenced by the lookup table pointer for transmit subaddress 00000 or 11111.

ERROR CONDITIONS

1. Invalid Command. No response, command ignored.
2. Correct Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. T/R* bit set to zero, no Data Word. No Status response. Set Message Error bit (Status Word), and Low Word Count (BIT Word).
4. T/R* bit set to zero plus one Data Word. The ACE will respond with Status. The Data Word will be stored in RAM location 0110 (or single-word data block for subaddress 0000 or 1111).
5. Zero T/R* bit and Broadcast Address, no Data Word. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), and Low Word Count (BIT word).
6. Zero T/R* bit and Broadcast Address, plus one Data Word. No Status response. Set Broadcast Command Received bits (Status Word).
7. Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Word Contents Error (BIT word).

SYNCHRONIZE WITH DATA WORD (T/R* = 0; 10001)

MESSAGE SEQUENCE = SYNCHRONIZE COMMAND/DATA WORD----STATUS

If the ENHANCED MODE CODES are enabled (bit 15 in Configuration Register #3 set to logic "1") the received data word is stored in RAM location 0111 (hex). If ENHANCED MODE CODES are not enabled, the word is stored in the single-word data block in the shared RAM referenced by receive subaddress 00000 or 11111 in the lookup table. If the LOAD TIME TAG ON SYNCHRONIZE option is enabled (bit 5 in Configuration Register #2 set to logic "1"), the ACE will load the received 16 bit Data Word into its internal Time Tag Register upon receipt of this mode command.

ERROR CONDITIONS

1. Invalid Command. No response, command ignored.
2. Correct Command not followed by Data Word. No Status response. Set Message Error bit (Status Word), Low Word Count (BIT Word).

3. Command Followed by too many Data Words. No Status response. Set Message Error bit (Status Word), High Word Count (BIT word).
4. Command T/R* bit set to one followed by Data Word. No Status response. Set Message Error bit (Status Word), and High Word Count (BIT Word).
5. Command T/R* bit set to one not followed by Data Word. The ACE replies with Status plus one Data Word. The Data Word is read from RAM location 121 hex (or single-word data block for subaddress 0000 or 1111).
6. Command T/R* Bit set to one and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word); Set Command Word Contents Error (BIT word).

TRANSMIT LAST COMMAND (T/R = 1; 10010)

MESSAGE SEQUENCE = TRANSMIT LAST COMMAND----STATUS/LAST COMMAND

The Status register is not updated before transmission. It contains the Status from the previous command. The Data Word transmitted contains the previous valid command (providing it was not another TRANSMIT LAST COMMAND or TRANSMIT STATUS WORD mode command).

ERROR CONDITIONS

1. Invalid Command. No response, command ignored.
2. Correct Command followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count Error (Bit Word).
3. T/R* Bit set to zero, no Data Word. No Status response. Set Message Error bit (Status Word), Low Word Count (BIT Word).
4. T/R* bit set to zero plus one Data Word. The ACE will respond with Status. The Data Word is transferred to RAM location 0112 (or single-word data block for subaddress 0000 or 1111).
5. Zero T/R* Bit and Broadcast Address, no Data Word. No Status response. Set Message Error and Broadcast Received bits (Status Word), Low Word Count Error(BIT Word).
6. Zero T/R* bit and Broadcast Address, one Data Word. No Status response. Set Broadcast Received Bit (status word). The Data Word is transferred to RAM location 0132 (or single-word data block for subaddress 0000 or 1111).
7. Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Word Contents Error (BIT Word).

TRANSMIT BIT WORD (T/R* = 1; 10011)

MESSAGE SEQUENCE = TRANSMIT BIT WORD----STATUS/BIT WORD

The ACE responds with Status followed by the Built-in Test (BIT) word. In the NON-ENHANCED mode, or if EXTERNAL BIT WORD ENABLE, bit 15 of Configuration Register #4, is programmed to logic "0," the BIT Word transmitted is accessed from the ACE's internal BIT Word register. This

word is defined in TABLE 63.

If the ACE is programmed for ENHANCED MODE (bit 15 of Configuration Register #15 is logic "1") **and** if EXTERNAL BIT WORD ENABLE is programmed to logic "1," the BIT Word transmitted will be read from a memory location. In this case, if ENHANCED MODE CODES are disabled (ENHANCED MODE disabled **or** ENHANCED MODE HANDLING disabled [bit 0 of Configuration Register #3 is programmed to logic "0"]), the location accessed for the external BIT Word will be the address referenced by the RT lookup table pointer for subaddress 00000 or subaddress 11111. In this case, it should be noted that for a given subaddress (00000 or 11111), the **same** Data Word will be transmitted in response to either a Transmit BIT Word **or** Transmit vector word mode command.

If ENHANCED MODE CODES are enabled (ENHANCED MODE **and** ENHANCED MODE HANDLING enabled (bits 15 and 0 of Configuration Register #3 are programmed to logic "1"), the external BIT Word will be accessed from address location 0123.

ERROR CONDITIONS

1. Invalid Command. No response, command ignored.
2. Correct Command followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count Error (Bit Word).
3. T/R* Bit set to zero, no Data Word. No Status response. Set Message Error bit (Status Word), Low Word Count (BIT Word).
4. T/R* bit set to zero plus one Data Word. The ACE will respond with Status. The Data Word is transferred to RAM address 0113 (or single-word data block for subaddress 0000 or 1111).
5. Zero T/R* Bit and Broadcast Address, no Data Word. No Status response. Set Message Error and Broadcast Received bits (Status Word), Low Word Count Error(BIT Word).
6. Zero T/R* bit and Broadcast Address, one Data Word. No Status response. Set Broadcast Received Bit (status word). The Data Word is transferred to RAM location 0133 (or single-word data block for subaddress 0000 or 1111).
7. Broadcast Address. No Status response. Set Message Error and Broadcast Command received bits (Status Word), Command Word contents Error (BIT Word).

SELECTED TRANSMITTER SHUTDOWN (T/R* = 0; 10100)

MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN/DATA----STATUS

The Data Word received is transferred to the RAM and Status is transmitted. If ENHANCED MODE CODES are not enabled, the Data Word is written to the single-word data block referenced by the lookup table pointer for subaddress 00000 or 11111. If ENHANCED MODE CODES are enabled, the Data Word is stored at hex location 0114. No other action is taken by the ACE. No transmitters are shut down as a result of this mode command. This command is intended for use with RTs with more than one dual redundant channel. If the command was a broadcast, the Broadcast Command Received bit is set and Status transmission is suppressed.

ERROR CONDITIONS

1. Invalid Command. No response, command ignored.
2. Correct Command not followed by Data Word. No Status response. Set Message Error bit (Status Word), and Low Word Count Bit (BIT Word).
3. Command followed by too many Data Words. No Status response. Set Message Error bit (Status Word), and High Word Count Bit (BIT Word).
4. Command T/R* bit Set to one followed by one Data Word. No Status response. Set Message Error bit (Status Word), and High Word Count (BIT Word).
5. Command D/R* bit set to one not followed by Data Word. The ACE replies with Status plus one Data Word. The Data Word is read from hex RAM location 0124 (or single-word data block for subaddress 0000 or 1111).
6. Command T/R* Bit Set to One and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), and Command Contents Error (BIT Word).

OVERRIDE SELECTED TRANSMITTER SHUTDOWN (T/R* = 0; 10101)

MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN/DATA----STATUS

The Data Word received is transferred to the RAM. If ENHANCED MODE CODES are disabled, the single-word data block is referenced by the lookup table pointer for subaddress 00000 or 11111. If ENHANCED MODE CODES are enabled, the Data Word is stored in hex RAM location 0115. No transmitters that have been previously shut down are reactivated as a result of this command. No other action is taken by the ACE. This command is intended for use with RTs with more than one dual redundant channel. If the command was a broadcast, the Broadcast Command Received bit is set and Status transmission is suppressed.

ERROR CONDITIONS

1. Invalid Command. No response, command ignored.
2. Command not followed by Data Word. No Status response. Set Message Error bit (Status Word), and Low Word Count (BIT Word).
3. Command followed by too many Data Words. No Status response. Set Message Error bit (Status Word), and High Word Count bit (BIT Word).
4. Command T/R* bit Set to one followed by Data Word. No Status response. Set Message Error bit (Status Word), and High Word Count (BIT Word).
5. Command T/R* bit Set to one not followed by Data Word. The ACE replies with Status plus one Data Word. The Data Word is read from hex RAM location 0125 (or single-word data block for subaddress 0000 or 1111).
6. Command T/R* Bit Set to one and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Word Contents (BIT Word).

RESERVED MODE CODES (T/R* = 0; 10110 - 11111)
(T/R* = 1; 10110 - 11111)

MESSAGE SEQUENCE = RESERVED MODE CODE (T/R = 1)----STATUS/DATA
= RESERVED MODE CODE (T/R = 0)/DATA----STATUS

For a RESERVED receive Command, the ACE stores the Data Word to the shared RAM. If the command was a broadcast, the Broadcast Command Received bit is set and Status transmission is suppressed. For a RESERVED transmit Command Word, the ACE responds with Status plus a single Data Word. The Data Word is read from the shared RAM. The shared RAM locations are referenced by the lookup table pointers for subaddresses 0 and 31 if ENHANCED MODE CODES are disabled. If ENHANCED MODE CODES are enabled, the RAM location accessed are 0116-001F for received mode codes, 0126-012F for transmit mode codes, or 0136-013F for broadcast mode codes.

ERROR CONDITIONS (T/R = 1)

1. Invalid Command. No response, command ignored.
2. Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).
3. Broadcast Command. No Status response. Set Message Error bit (status word), and Command Word Contents Error (BIT Word).

ERROR CONDITIONS (T/R = 0)

1. Invalid Command. No response, command ignored.
2. Command not followed by contiguous Data Word. No Status response. Set Message Error bit (Status Word), and Low Word Count (BIT Word).
3. Command followed by too many Data Words. No Status response. Set Message Error bit (Status Word), and High Word Count (BIT word).

RT SOFTWARE INITIALIZATION PROCEDURE

The following software sequence is typical of the steps the host CPU should perform following power turn-on to configure the ACE for RT operation. For most applications, it is possible to skip many of the steps indicated.

(1) Perform a software reset, by writing 0001 (hex) to the Start/Reset Register.

(2) If any of the Enhanced mode functions (eg., subaddress double buffering) are to be used, invoke the ACE RT's ENHANCED MODE by writing 8000 (hex) to Configuration Register #3.

(3) Initialize the Interrupt Mask register. For many RT applications, the EOM interrupt will generally be enabled. In other instances, the RT SUBADDRESS CONTROL WORD, RT CIRCULAR BUFFER ROLLOVER, RT MODE CODE and/or FORMAT ERROR Interrupt Requests may also be enabled. The RT SUBADDRESS CONTROL WORD interrupt enables interrupt requests to be issued following messages to specified transmit, receive, or broadcast subaddresses. The RT MODE CODE interrupt enables interrupt requests to be programmed for individual mode code commands. The RT CIRCULAR BUFFER ROLLOVER interrupt may be used to provide an interrupt request following a multimessage reception or transmission of a specified number of Data Words to/from a given subaddress.

(4) Load the starting location of the Stack into the Active Area Stack Pointer location in RAM.

(5) As an option, initialize the Active Area Stack. If there is a desire to poll the Stack RAM while 1553 messages are being processed, the Block Status Word locations for the respective message block descriptors (relative address locations 0, 4, 8...[stack size -4] in the stack) should be cleared to 0000. A Block Status Word of 0000 (SOM = EOM = 0) indicates that a message has not yet been processed.

(6) Initialize the Active Area Lookup Table. The Lookup Table address for each transmit, receive, and (optionally) broadcast subaddress should be initialized as the pointer value for each respective lookup table. If the RT is going to be used in the ENHANCED RT MEMORY MANAGEMENT mode, it will also be necessary to select the memory management and interrupt options for each subaddress by initializing the Subaddress Control Words for the Active Area.
If there are several unused subaddresses for an RT, it is recommended that the Lookup Table pointers for these be initialized to the **same** value in order to conserve memory space.

(7) If ENHANCED MODE CODE HANDLING (bit 0 of Configuration Register #4) is not used, the pointers for receive subaddresses 0 and 31 (for Synchronize with Data messages) generally get loaded with the same pointer value. Similarly, the Lookup Table addresses for transmit subaddresses 0 and 31 (for Transmit Vector Word messages) generally get loaded with the same pointer value.

If ENHANCED MODE CODE HANDLING is enabled, Data Words for these mode codes are stored in locations 0111 (for Synchronize with data) and 0130 (for Transmit Vector Word).

(8) Initialize Configuration Register #2. This involves selecting use of the of the following functions:

ENHANCED RT MEMORY MANAGEMENT should be selected if it is desirable to select the circular buffer feature and/or subaddress double buffering features on an individual subaddress basis. SEPARATE BROADCAST should be set if it is necessary to comply to Notice 2 for broadcast messages. This enables **separate** lookup table pointers for nonbroadcast received and broadcast receive messages.

For RT mode, 256-WORD BOUNDARY DISABLE should normally be programmed to logic "0." If this bit is programmed to logic "1," it should be noted that the size of **all** circular buffers becomes **64K** words.

The three TIME TAG RESOLUTION bits should be programmed to select the desired resolution for the time tag register. The choices are 2, 4, 8, 16, 32, or 64 µs/LSB, or "EXTERNAL" (external clock). CLEAR TIME TAG ON SYNCHRONIZE should be programmed to logic "1" if it is desired to clear the time tag to 0000 following receipt of a synchronize (without data) mode code. Similarly, LOAD TIME TAG ON SYNCHRONIZE should be programmed to logic "1" if it is desired to load the time tag to the value of the received Data Word following receipt of a synchronize with data mode code.

ENHANCED INTERRUPTS should be enabled if the CPU needs to poll using the Interrupt Status Register and/or it is desired that one or more of the following conditions cause an interrupt: TRANSMITTER TIMEOUT, RT COMMAND STACK ROLLOVER, or RT MODE CODE interrupt. INTERRUPT STATUS AUTO CLEAR should be programmed to logic "1" if it is desired to automatically clear the Interrupt Status Register and the ACE's INT* output (for a "level" type interrupt output) after the Interrupt Status Register has been read. LEVEL/PULSE* INTERRUPT REQUEST should be programmed to logic "0" for a pulse type interrupt (500 ns) or to logic "1" for a level type interrupt.

CLEAR SERVICE REQUEST should be programmed to logic "1" if it is desired to automatically clear the Service Request Status Word bit following reception of a Transmit vector word mode command.

OVERWRITE INVALID DATA should be set to logic "1" if the circular buffer mode is used with one or more subaddresses. SUBADDRESS DOUBLE BUFFERING should be enabled, if desired. BUSY LOOKUP TABLE ENABLE should be logic "1" if there is a need for the Busy bit in the RT Status Word to be set for particular T/R*/Bcst subaddresses.

(9) Initialize Configuration Register #3. If one or more of the ENHANCED MODE features are to be used, **bit 15 must be maintained at logic "1."** The RT Stack size is programmable with choices of 256 words (default, 64 messages), 512, 1024, or 2048 words (512 messages) by bits 14 and 13. Other RT features that may be selected by this register include ILLEGALIZATION (default = "0" = enabled), ALTERNATE STATUS (allowing software programming of **all 11** Status Word bits), the choice of storing or not storing words for illegal or "BUSY" messages, and ENHANCED MODE CODE HANDLING.

If enhanced mode code handling is selected, Data Words for mode codes are stored in address locations 0110-013F, and interrupt requests for individual mode codes may be enabled by means of a

table in address locations 0108-010F. Other RT options selectable by Configuration Register #3 include 1553A MODE CODES ENABLED, and RTFAIL/RTFLAG* WRAP ENABLED. 1553A MODE CODES ENABLED causes only subaddress 00000 to be treated as a mode code subaddress. RTFAIL*/RTFLAG* WRAP ENABLE causes the RT FLAG Status bit to be automatically set following a failure of the loop test. OVERRIDE MODE CODE T/R ERROR should only be programmed to logic "1" if receive Mode Codes 0000 through 01111 are to be treated as defined mode codes.

(10) Initialize Configuration Registers #4. If EXTERNAL BIT WORD ENABLE is logic "1," the Data Word for a Transmit BIT Word mode command is accessed from a shared RAM location, rather than from an internal register. If ENHANCED MODE CODES are not enabled, the RAM location for the external BIT Word is the location pointed to by the lookup table pointer for subaddress 0 or 31. If ENHANCED MODE CODES are enabled, the external BIT Word is stored in location 0123.

INHIBIT BIT WORD IF BUSY prevents the BIT Word from being transmitted if the RT is Busy. If MODE CODE OVERRIDE BUSY is logic "1," this enables the ACE RT to transmit a Data Word in response to a Transmit Vector Word or Reserved transmit mode command, even if the RT is busy.

Set LATCH RT ADDRESS WITH C.R. #5 to logic "1," in preparation for loading the RT address into Configuration Register #5 (next step). After the RT Address has been programmed, it is suggested that LATCH RT ADDRESS WITH C.R. #5 be cleared to logic "0" to prevent an erroneous overwrite.

(11) Initialize Configuration Register #5. Load RT address into register.

The default clock frequency for the ACE is 16 MHz. To select 12 MHz operation, 12 MHZ SELECT must be programmed to logic "1."

EXPANDED ZERO-CROSSING should be set to logic "1" to expand the Manchester decoders' tolerance for zero crossing distortion by enabling a sampling rate of 32 MHz (or 24 MHz). RESPONSE TIMEOUT SELECT 1-0 selects the time value for the RT-to-RT response timeout from among 18.5 µs (default), 22.5, 50.5, or 130 µs. If GAP CHECK ENABLED is programmed to logic "1," the RT will verify for a minimum bus dead time of 2 µs prior to the transmitting RT's response in an RT-to-RT transfer, where the ACE RT is the receiving RT.

(12) If RT Illegalization is used, the CPU should initialize the Illegalization Table, address locations 0300-03FF.

(13) If the BUSY LOOKUP TABLE is enabled, select the desired subaddresses to be busy by programming the Busy table, address locations 0240 through 0247.

(14) If ENHANCED INTERRUPTS are enabled **and** ENHANCED MODE CODE HANDLING is enabled, interrupts for selective mode code messages may be enabled by programming locations 0108 through 010F.

(15) Data to be transmitted on the 1553 bus (in response to transmit commands) should be written into the

appropriate data blocks. As an option, the locations for Data Words for anticipated receive Data Words may be initialized to zero.

(16) To configure the ACE as an on-line RT, write to Configuration Register #1, setting bit 15 (MSB) to logic "1" and bit 14 to logic "0." The current active area is selected by the setting of bit 13 (0 for A, 1 for B). If ALTERNATE RT STATUS is not enabled, bits 11 through 8 should be initialized to select the values for the RT Status Word bits Dynamic Bus Control Acceptance, Busy, Service Request, and Subsystem Flag. Also, in the ENHANCED mode, the RT flag Status Word bit is programmable by bit 7. These bits must be programmed for the **logical inverse** of their desired values in the RT Status Word.

If ALTERNATE RT STATUS is enabled, bits 10 through 0 of the ACE's RT Status Word are programmable via bits 11 through 1 of Configuration Register #1. In this case, the **logical values** (non-inverted) of the intended Status Word bit values must be programmed.

SERVICING COMPLETED RT MESSAGES

The ACE RT provides a number of techniques for determining when a message has been processed. These methods support both polling-driven and interrupt-driven software.

There are several polling methods that may be used. These include:

(1) In the ENHANCED mode, the host may continuously poll RT MESSAGE IN PROGRESS, bit 0 of Configuration Register #1. This bit will return logic "0" while the ACE RT is not processing a message. During the time that the ACE RT is servicing a message (after the receipt of a Command Word), RT MESSAGE IN PROGRESS will return logic "1." When the message completes, RT MESSAGE IN PROGRESS will once again return logic "0."

(2) The CPU can poll the contents of the Stack Pointer RAM location. The active area Stack Pointer increments by four **at the beginning** of each message being processed (after receipt of a Command Word).

(3) If the host needs to determine the occurrence of a **particular** Command Word, it may do so by polling the RT Last Command Register. It should be noted that the contents of this register are updated at the **beginning** of a message being processed. The CPU may then poll the EOM (End-of-Message) bit of the Interrupt Status Register to determine when the message has been completed. See explanation below.

(4) If the ACE is programmed for the ENHANCED mode **and** ENHANCED INTERRUPTS (bit 15 of Configuration Register #2) are enabled, the CPU may poll the Interrupt Status Register. In this mode, the various bits in the Interrupt Status Register will become set **regardless** of the programming of the corresponding bits in the Interrupt Mask register.

In this mode, the ACE may determine that a message has been **completed** by polling the Interrupt

Status Register until the EOM (End-of-Message) bit returns logic "1."

In this mode, the host processor may also poll to determine when a message has been processed for a **particular** transmit, receive, or broadcast subaddress. To enable do this, ENHANCED RT MEMORY MANAGEMENT (bit 1 of Configuration Register #2) must be invoked. To cause the bit to be set for a particular Tx/RX/Bcst-subaddress, it is then necessary to set the appropriate bit ([TX:, RX:, or BCST:] INT on EOM) in the desired Subaddress Control Word to logic "1." All other Subaddress Control Word ([TX:, RX:, or BCST:] INT on EOM) bits should be programmed to logic "0." This will cause the RT SUBADDRESS CONTROL WORD EOM bit in the Interrupt Status Register to be set to logic "1" after completion of the desired message.

Similarly, the host may poll for receipt of a **particular** mode code message. This feature is enabled by invoking ENHANCED MODE CODE HANDLING (bit 0 of Configuration Register #3). The desired mode code may be selected by setting the appropriate bit in the Mode Code Selective Interrupt Table (address range 0108-010F). When the specific mode code message has been completed, the RT MODE CODE bit of the Interrupt Status Register will return logic "1."

Similarly, the Interrupt Status Register may be polled to determine the occurrence of FORMAT ERROR, CIRCULAR BUFFER ROLLOVER, and/or COMMAND STACK ROLLOVER conditions. FORMAT ERROR indicates any error in a received message, other than an invalid Command Word: sync or Manchester encoding, parity, bit count,
word count, or RT-to-RT transfer errors. CIRCULAR BUFFER ROLLOVER may be used to signal completion of a multimessage bulk data transfer. COMMAND STACK ROLLOVER occurs when the Stack rolls over at an address boundary of 256, 512, 1024, or 2048 words, as programmed in Configuration Register #3.
If interrupts are used, the normal procedure would be to **not** invoke ENHANCED INTERRUPTS. This allows the Interrupt Mask Register to be used to enable interrupts and the corresponding Interrupt Status Register bits for only **selected** condition(s), as discussed above.

RT ERROR HANDLING

As discussed above, the preferred method for handling erroneous messages is to make use of the circular buffer and/or double buffering techniques. In the case of the circular buffer mode, the OVERWRITE INVALID DATA bit should be set to logic "1." With these techniques, Data Words received and stored from invalid messages will be automatically overwritten by the ACE RT. In most systems, the bus controller will retry failed messages. By so doing, the occurrence of errors and message retries is transparent to the RT's host processor.

If necessary, the RT's host processor may ascertain the occurrence of failed messages by several methods:

(1) Determine, by polling or interrupt techniques, when a FORMAT ERROR condition occurs.

(2) Read the Block Status Words for all messages processed. Bits 12-9 and 6-0 all indicate error conditions in received messages.

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MONITOR OPERATION

The ACE terminals provide three different bus monitor modes: (1) a Word Monitor, (2) a Selective Message Monitor, (3) a combined RT/Selective Message Monitor mode. When the ACE is in Non-Enhanced Mode, the Monitor operates the same as the previous generation product, BUS-61559 Advanced Integrated Mux Hybrid with Enhanced RT features (AIM-HY'er). In ENHANCED MODE, both Selective Message Monitor and Combined RT/Selective Message Monitor modes may be activated. ENHANCED MODE also enables the Monitor triggering capability for the Word Monitor mode.

In Enhanced mode, the Word Monitor provides a programmable Trigger Word. The Trigger Word, which defines a specific Command Word, may be used to start and stop the Monitor or generate an interrupt. You may also start the Word Monitor by means of an external trigger.

The Selective Message Monitor supports message filtering, based on RT Address/T-R* bit/Subaddress, and provides separate Command and Data Stacks. The Message Monitor also stores the contents of the 16-bit Time Tag Register (see Time Tag Register for resolution programming).

The RT/Selective Message Monitor mode provides full RT capability for the ACE terminal's own RT address **PLUS** selective monitoring for all other RT addresses. Similar to RT mode, the Selective Monitor's Command Stack stores all command words, Time Tag words, Block Status words, and Data block pointers for each monitored message. The Command and Data Stacks are programmable via bits 12-8 in Configuration Register 3.

WORD MONITOR MODE

In Word Monitor Terminal mode, the ACE monitors both 1553 buses. After the software initialization and MONITOR START sequences, the ACE stores all Command, Status, and Data Words received from both buses. For each word received from either bus, **a pair** of words is stored to the ACE's shared RAM. The first word is the 16 bits of data from the received word. The second word is the Monitor Identification (ID), or "Tag" word. The ID Word contains information relating to bus channel, word validity, and interword time gaps. The data and ID words are stored in a circular buffer in the shared RAM address space.

WORD MONITOR MEMORY MAP

A typical word monitor memory map is illustrated in TABLE 66. With 12K RAM per channel, the Monitor Data Stack size should be limited to 8K. The Active Area Stack pointer provides the address where the first monitored word is stored. In the example, it is assumed that the Active Area Stack Pointer for Area A (location 0100) is initialized to 0000. The first received data word is stored in location 0000, the ID word for the first word is stored in location 0001, etc.

The current Monitor address is maintained by means of an internal counter register. This value may be read by the CPU by means of the Data Stack Address Register. It is important to note that when the counter reaches the Stack Pointer address of 0100 (for active area A) or 0104 (for active area B), the initial pointer value stored in this shared RAM location **will be overwritten** by the monitored data and ID Words. When

the internal address counter reaches an address of 1FFF, **the counter rolls over to 0000, overwriting previous monitor data**.

TABLE 66. TYPICAL WORD MT MEMORY MAP

HEX ADDRESS	FUNCTION
0000	First Received 1553 Word
0001	First Identification Word
0002	Second Received 1553 Word
0003	Second Identification Word
0004	Third Received 1553 Word
0005	Third Identification Word
•	•
•	•
0100	Stack Pointer (Fixed Location)
•	•
1FFF	•
2000	NOT USED
•	•
2FFF	NOT USED
3000	RESERVED
•	•
3FFF	RESERVED

To initialize the ACE for Word Monitor mode, the host processor should program bits 15, 14, and 12 of Configuration Register #1 to logic "0," logic "1," and logic "0" respectively. The Stack Pointer for the active area should then be loaded with the starting location of the monitor stack in the ACE shared RAM address space, also (after setting bit 15 of Configuration Register #3 to operate in enhanced mode) the MT Command Stack size (bits 11 and 12 of Config. Reg. #3) and the MT Data Stack size (bits 10, 9 and 8 of Config. Reg. #3) should be setup. The default values for the stack sizes are 256 words and 65,536 words, respectively. Finally, to start the monitor, a "Start" command should be issued by means of the Start/Reset Register.

The Monitor ID Word contains a Word Flag bit (always logic 1) plus information relating to bus channel, word validity, Command-Status/Data* sync type, and inter-word gap time information. This latter field includes a "Contiguous Data" bit as well as an 8-bit gap time field, indicating 0 to 127 µs with a resolution of 0.5 µs per LSB.

In order to take the BU-65528 monitor off-line, the host CPU must issue a RESET command to the Start/Reset Register.

The BU-65528 Identification Word is defined in TABLE 67.

TABLE 67. WORD MONITOR IDENTIFICATION WORD	
BIT	**DESCRIPTION**
15(MSB)	GAP TIME
•	•
•	•
•	•
8	GAP TIME
7	WORD FLAG
6	THIS_RT*
5	BROADCAST*
4	ERROR
3	COMMAND/DATA* SYNC
2	CHANNEL B/A*
1	CONTIGUOUS DATA/GAP*
0(LSB)	MODE_CODE*

GAP TIME: If the CONTIGUOUS DATA bit is high, these 8 bits are not used. If CONTIGUOUS DATA is low, GAP TIME indicates the time gap between the end of the previous word to the start of the current word in 0.5 us/LSB resolution, up to 127.5 us. For inter-word time gaps greater than 127.5 us, the GAP time field will indicate FF (hex). It should be noted that if the current word was received on the **alternate** bus from the previous word, the GAP TIME field will indicate approximately **20 us greater** than the actual gap time from the word on the first bus. That is, if the current word is received on the alternate bus from the previous word and the current GAP TIME is a time of less than 20 µs, this indicates that the current word **overlapped** the previous word (received on the alternate bus).

WORD FLAG: Always set to logic "1" for every Identification Word. Each location in the shared RAM where an ID Word is anticipated being stored should be initialized by the CPU to logic "0."

THIS RT*: If this bit is low, it indicates that the received word was valid, contained a Command/Status sync type, had an RT Address field matching the address on inputs RTAD4-RTAD0 and that correct odd parity was presented on RTADP. This bit will be high otherwise.

BROADCAST*: If this bit is low, it indicates that the received word was valid, contained a Command/Status sync type and an RT Address field of 31. This bit will be high otherwise.

Note: If the ACE is programmed for ENHANCED MODE **and** Broadcast has been disabled by

programming bit 7 of Configuration Register #5 to logic "1," Broadcast will **always** return logic "1."

ERROR: If this bit is low, it indicates that the received word passed all of the MIL-STD-1553 validation criteria. If this bit is high, it indicates an error in the word: either Manchester II encoding, sync, bit count or parity.

COMMAND/DATA* SYNC: If this bit is high, it indicates the word contained a Command/Status type sync. If this bit is low, it indicates that the word contained a Data type sync.

CHANNEL B/A*: If this bit is low, it indicates that the word was received on Channel A. If the bit is high, it indicates that the word was received on Channel B.

CONTIGUOUS DATA/GAP*: If this bit is high, it indicates either no gap or less than 2 µs of dead time on the bus from the end of the previous word to the start of the current word. In this case, the GAP TIME field is not used. If this bit is low, it indicates a gap time of more than 2 us from the end of the previous word to the start of the current word. In this case, the GAP TIME field **does** contain valid bus dead time information.

MODE CODE*: If this bit is low, it indicates that the received word was valid, had a Command/Status sync type and contained a subaddress field of either 0 or 31. This bit will be high otherwise.

WORD MONITOR INITIALIZATION

In Word MT mode, the active area stack pointer provides the address where the first monitored word is stored. This pointer must be written by the CPU prior to issuing a MT START command. The data for the first received word will be stored in the location pointed to by the Active Area Stack Pointer. It is important to note that both (Area A and B) Stack Pointers will be **overwritten** by received data or identification words. (See FIGURE 14)

Word Monitor Start and Stop

To start the Monitor, write the value 0002 to the Start/Reset Register (BC/MT START). To stop the Monitor from storing further words from the 1553 bus, write the value 0001 to the Start/Reset Register (RESET).

Word Monitor Software Initialization Sequence

The software procedure for initializing the BU61580 in Monitor mode is outlined as follows:

(1) Issue a software RESET by writing a value of 0001 to the Start/Reset Register.
(2) Initialize the BU-65528 to MT mode with Active Area A (the Active Area selection doesn't matter in MT mode) by writing a value of 5000 Hex to Configuration Register #1.

(3) Enable enhanced mode by writing a value of 8000 Hex to Configuration Register #3.

(4) Select Monitor Data Stack size of 8k words by loading 8300 Hex in Configuration Register #3.

(5) Write the desired location to start storing received words to the Area A Stack Pointer location, 0100.

(6) Optionally, clear the area of shared RAM where received data and ID words are anticipated to be received to values of 0000. This allows the host processor to easily determine the location of the last word received by means of the WORD FLAG bit in the ID Word.

(7) To initiate the Monitor to start storing received words, write the value 0002 to the Start/Reset Register (BC/MT START).

(8) To subsequently cause the Monitor to stop storing received words, write the value 0001 to the Start/Reset Register (RESET).

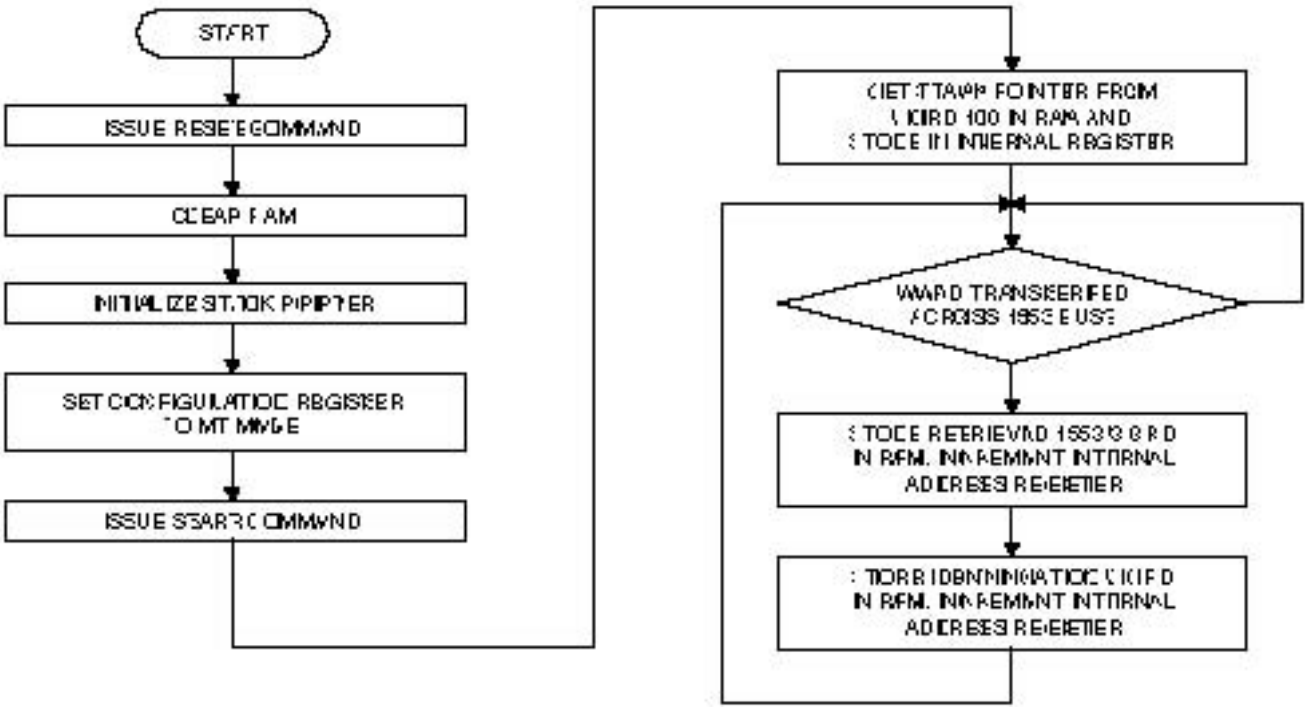


FIGURE 14. MT INITIALIZATION AND DATA STORAGE FUNCTION

DISTINGUISHING COMMAND WORDS FROM STATUS WORDS: MESSAGE RECONSTRUCTION

In the Word Monitor mode, message reconstruction entails determining when individual messages received from the 1553 bus begin and end. A critical part of this process, which must be implemented in software (either in real time or off-line), is to distinguish between Command Words and Status Words.

There probably is no universal algorithm for making an absolute "100%" determination between Command and Status Words. This would have to take into account superseding and bus switching command sequences in addition to a multiplicity of message error conditions. However, the rules listed below will prove useful in making the command/status determination for the **vast majority (greater than 99.99%)** of all "real-world" MIL-STD-1553B applications.

(1) A word containing a Command/Status sync and any sub-address field (bits 9 (MSB) through 5 (LSB)) **other than 0 or 8** is a Command Word.

(2) A word with a Command/Status sync preceded by a gap time of longer than the "response timeout" time is a Command Word. For most applications, 14 µs is probably a good starting value for the "response timeout" parameter. For applications entailing very long lengths of bus cable (several hundred feet), a longer period for the "bus timeout" parameter may be required.

(3) A word with a Command/Status type of sync received on the alternate bus from the last previous received word may be considered to be a Command Word.

(4) Two contiguous (no intervening gap time) words with Command/Status sync types, with the first of the two words preceded by a gap, are the two Command Words for an RT-to-RT transfer or RT-to-Broadcast transfer.

(5) A word with a Command/Status sync and a value of 31 (11111) for the RT Address field (bits 15 [MSB] through 11 [LSB]) is a Command Word to the Broadcast address.

(6) The next **noncontiguous** word with a Command/Status sync following a Command Word to the Broadcast address is a Command Word.

(7) The principal purpose of the CPU's Monitor software will be to reconstruct the 1553 messages. Once the parsing routine encounters a Command Word, marking the beginning of a new message, it should continue to search through the message, verifying that it conforms to one of the MIL-STD-1553B message formats (reference FIGURE 3 of MIL-STD-1553B).

If the "message reconstructor" software is parsing through a received message that is **not** an RT-to-RT transfer, a word with a Command/Status sync, and a **different** RT address than the previous word with a command/status sync may be considered to be the Command Word for the next message.

(8) If the message reconstructor software is parsing through a stream of Data Words and determines the end of a complete, valid message followed by a gap time (possibly less than the "response timeout" value), the **next** word with a command/status sync type will be a Command Word. This is regardless of whether the word contains the same RT address or a different RT address than the previous Command/Status word.

WORD MONITOR TRIGGER

In the Word Monitor mode, there is a pattern-recognition trigger and a pattern-recognition interrupt. The 16-bit compare word for both the trigger and the interrupt is stored in the MT TRIGGER WORD register. The pattern recognition interrupt is enabled by setting the MT PATT TRIG bit (bit 9) in the Interrupt Mask Register. The pattern recognition trigger is enabled by setting the TRIGGER ENABLE bit (bit 11) in Configuration Register #1 and selecting either the START-ON-TRIGGER (bit 10) or the STOP-ON-TRIGGER (bit 9) bit in Configuration Register #1.

TABLE 68. WORD MONITOR WITH TRIGGER TRUTH TABLE
(Configuration Register # 1 bits)

Start On Trigger (Bit 10)	Stop On Trigger (Bit 9)	External Trigger (Bit 7) (Note 1)	Word MT Start and Store Operation
0	0	0	Software Start, MT stores all data on the bus
0	1	0	Software Start, MT stores all data until the Command Word matches the word stored in the MT Trigger Register (MTR). This Command Word is the last word stored in the MT Stack.
1	0	0	Software Start, stores all data after a valid Command Word matches the word stored in the MT Trigger Register (MTR). This Command Word is stored in the MT Stack.
1	1	0	Software Start, stores ONLY the Command Word that matches the word stored in the MT Trigger Register.

Note: EXTERNAL TRIGGER bit requires use of an ACE Hybrid input not accessible to the user. This bit should always be set to "0".

The Word Monitor with Trigger truth table (TABLE 68) assumes the following:

1) User is in the ENHANCED MODE.
2) Word Monitor is selected in Config Reg #1 (Bit 15=0 14=1 12=0).
3) User programs the "Trigger Word" in the MT Trigger Register.
4) Trig Enable Bit (bit 11 in Config Reg # 1) is set to a logic 1.

SELECTIVE MESSAGE MONITOR MODE

The ACE provides a flexible interface that allows selective monitoring of 1553 messages based on RT Address, T/R, and Subaddress with very little host processor intervention. The Message Monitor mode of the ACE recreates all command/response messages on the 1553 bus and stores them into RAM based on a user programmable filter (RT Address, T/R, and Subaddress). This monitor can be used as a monitor alone or in a combined RT/Monitor mode. The Message Monitor contains two stacks (a command stack and a data stack) that are independent from the BC/RT command stack. The pointers for these stacks are located in fixed locations in the RAM.

The Message Monitor is enabled in the RT/Monitor mode by setting the ENHANCED MODE bit (bit 15) in Configuration Register bit #3 to a logic "1," RT/BC_L (bit 15) to logic "0," and setting MT (bit 14) and MESSAGE MONITOR ENABLE bits (bit 12) in Configuration Register #1 to logic "1."

Monitor Selection Function

While operating in Selective Message Monitor mode, upon receipt of a valid command, the ACE will reference the selective monitor lookup table (a fixed block of RAM) to determine if this command is enabled. The address for this location is determined by using the RT Address, T/R* bit, and Subaddress bit 4, of the current command, and adding it to the base address 0280(hex) (TABLE 69). The bit location within this 16-bit word is determined by subaddress bits 3..0 of the current Command Word. If the specified bit in the lookup table is logic "0" the command is not enabled and the ACE will ignore this message. If this bit is logic "1," the command is enabled and the ACE will create an entry on the monitor command stack (based on the monitor command stack pointer) and store the data associated with this command into sequential locations in the monitor data stack.

The address definition for the Selective Monitor Lookup Table is illustrated below.

TABLE 69. MESSAGE MONITOR SELECTION TABLE ADDRESS	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	LOGIC “0”
9	LOGIC “1”
8	LOGIC “0”
7	LOGIC “1”
6	RTAD_4
5	RTAD_3
4	RTAD_2
3	RTAD_1
2	RTAD_0
1	T/R*
0(LSB)	SUBADDRESS_4

For even-numbered addresses in the Selective Monitor Lookup Table (SUBADDRESS_4 = A0 = 0), bit 15 enables monitoring for subaddress 15, bit 14 enables monitoring for subaddress 14,.....bit 0 enables subaddress 0. For odd-numbered addresses in the Selective Monitor Lookup Table (SUBADDRESS_4 = A0 = 1), bit 15 enables monitoring for subaddress 31, bit 14 enables monitoring for subaddress 30,.....bit 0 enables subaddress 16. Programming a bit to logic "0" **disables** monitoring for the respective RT Address-T/R* bit-subaddress; i.e., a message will be ignored. Programming a bit to logic "1" **enables** monitoring for the respective RT Address-T/R* bit-subaddress; that is, the message will be stored.

Message Monitor Formats

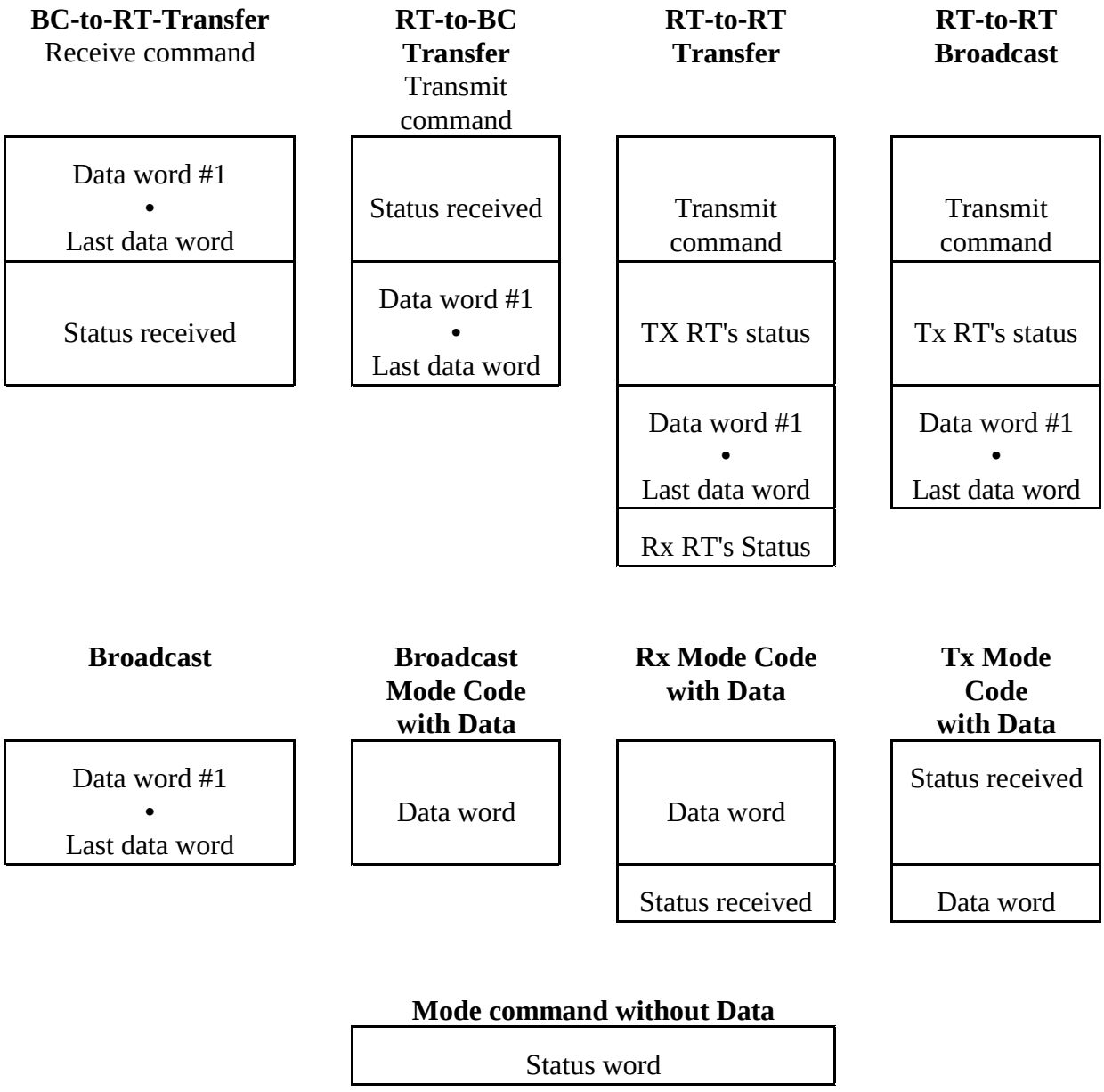
The format of the information in the data stack depends on the type of message that was processed. A BC-to-RT command transfer (receive) will store the Command Word in the monitor Command Word stack, the N Data Words followed by the receiving RT's status response in the monitor data stack.

Note: If the ACE selects the **receive** command in a RT-to-RT transfer, the RT-RT TRANSFER FORMAT bit (bit 11) of the Block Status Word will be set regardless of whether the transmit command was selected. In the case where the ACE selects only the transmit Command Word in an RT-to-RT transfer, the first word stored in the monitor data stack entry will be the second (transmit) Command Word, followed by Tx status, data and Rx status, i.e., the ACE will ignore the receive command word and status word.

Reading a monitored message from the ACE, requires the use of:

1) The Block Status Word to determine if the message was an RT-to-RT transfer.
2) The Command Word to determine the message format (transmit, receive, mode code, broadcast, etc) and word count.
3) The data pointer to the data block entry.

Refer to FIGURE 15 for a complete listing of all message monitor data stack message formats.



Note: There is no Data Stack entry for a broadcast mode command without data.

FIGURE 15. SELECTIVE MESSAGE MONITOR DATA BLOCK FORMATS

A typical memory map for the ACE in the Selective Message Monitor mode is illustrated in TABLE 70. This mode of operation defines several fixed locations in the RAM. These locations are allocated in a manner in which none of them overlap with the reserved RT locations. This allows for a combined RT/Selective Message Monitor mode. Refer to TABLE 71 for an example of a typical RT/Selective Message Monitor Memory Map.

The fixed memory map consists of two Monitor Command Stack Pointers (locations 102 and 106 hex), two Monitor Data Stack Pointers (locations 103 and 107 hex), and a Selective Message Monitor Lookup Table (locations 0280 through 02FF hex) based on RT Address, T/R*, and subaddress. The Monitor Command Stack size is assumed to be 1K words, and the Monitor Data Stack size is assumed to be 4K words.

TABLE 70. TYPICAL SELECTIVE MESSAGE MONITOR MEMORY MAP
(shown for 12K RAM for "Monitor only" mode)

ADDRESS (HEX)	DESCRIPTION
0000-0101	Not Used
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack Pointer A (fixed location)
0104-105	Not Used
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-027F	Not Used
0280-02FF	Selective Monitor Lookup Table (fixed area)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0FFF	Not Used
1000-1FFF	Monitor Data Stack A
2000-2FFF	Not Used

TABLE 71. TYPICAL RT/SELECTIVE MESSAGE MONITOR MEMORY MAP
(shown for 12K RAM for combined RT/MT mode)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	RT Command Stack A
0100	RT Command Stack Pointer A (fixed location)
0101	RESERVED
0102	Monitor Command Stack A (fixed location)
0103	Monitor Data Stack A (fixed location)
0104	Stack Pointer B (fixed location)
0105	RESERVED
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-010F	Mode Code Selective Interrupt Table (fixed area)
0110-013F	Mode Code data (fixed area)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-0247	Busy Bit Lookup Table (fixed area)
0248-025F	(not used)
0260-027F	RT Data Block 0
0280-02FF	Selective Monitor Lookup Table (fixed area)
0300-03FF	Command Illegalizing Table (fixed area)
0400-07FF	Monitor Command Stack A
0800-0FFF	Monitor Data Stack
1000-101F	Data Block 0
1020-103F	Data Block 1
•	•
•	•
2FE0-2FFF	Data Block 255

The size of the monitor command stack is programmable to 256, 1K, 4K, or 16K by bits 11 and 12 of Configuration Register #3. The Monitor Data Stack size is programmable to 512, 1K, 2K, 4K, 8K, 16K, 32K or 64K by use of bits 8 through 10 in Configuration Register #3.

Note: Ensure the sizes selected for the Monitor command stack and Monitor data stack do not exceed the 12K word onboard RAM.

Interrupts can be generated for MONITOR COMMAND STACK OVERFLOW (bit 13 of interrupt status register), MONITOR DATA STACK OVERFLOW (bit 12 of interrupt status register), or END OF MESSAGE (bit 0 of interrupt status register).

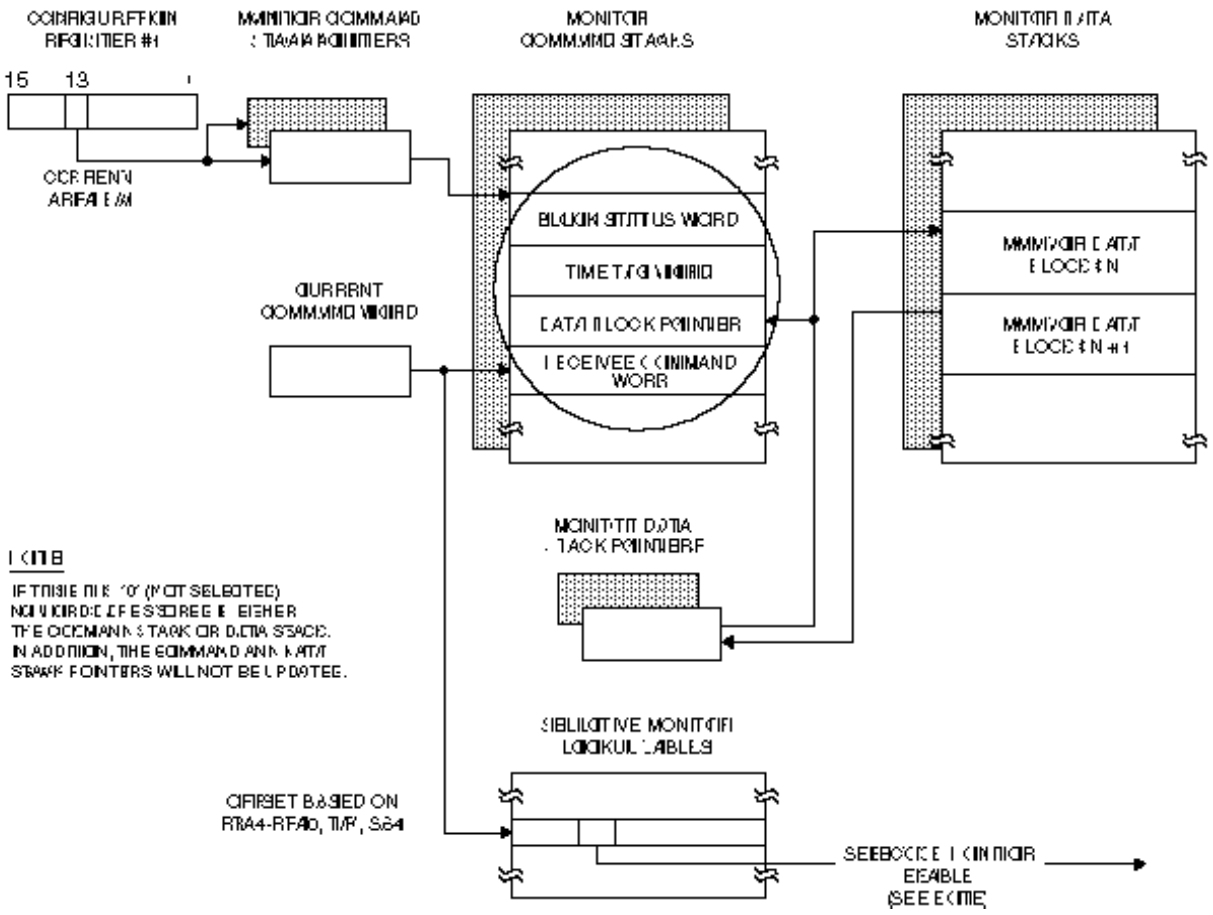


FIGURE 16. SELECTIVE MESSAGE MONITOR

Refer to FIGURE 16 for an illustration of the Selective Message Monitor operation. Upon receipt of a valid Command Word, the ACE will reference the Selective Monitor Lookup Table (a fixed block of addresses) to determine if the current command is enabled. If the current command is disabled, the ACE will ignore (and not store) the current message. If the command is enabled, the ACE will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer.

Message Monitor Block Status Word

The bit map and bit descriptions for the Message Monitor Block Status Word are indicated below.

TABLE 72. MESSAGE MONITOR MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

END-OF-MESSAGE (EOM): Set at the completion of a monitored message, regardless of whether or not there were any errors in the message.

START-OF-MESSAGE (SOM): Set approximately 3-4 µs following the receipt (mid-parity bit) of the Command Word and cleared at the end of the message.

CHANNEL B/A*: This bit will be low if the message was monitored from Channel A or high if the message was monitored on Channel B.

ERROR FLAG: If this bit is high and bit 10 and/or bit 9 is high, this indicates that either a format error, no response error occurred in the message. If this bit is high, the ACE is configured for its transparent mode of processor interface, and bits 10 and 9 are both logic "0," this indicates that a handshake failure has occurred. A handshake failure occurs under when the input signal DTGRT* is either not asserted low or is asserted low too late(later than 4 µs in 16 MHz mode, or 3.5µs in 12 MHz mode) after the time that the output signal

DTREQ* is asserted low. Alternatively, a handshake failure will occur if the host CPU fails to clear STRBD* (high) within 4 µs after the ACE has asserted its READYD* output (low). If a handshake failure occurs, a received message should be considered invalid.

RT-to-RT TRANSFER: This bit indicates that the message was an RT-to-RT transfer. The receive Command Word must be selected, and is stored in the Monitor Command Stack. The transmit Command Word is stored in the Monitor Data Stack in the location referenced by the Data Block Pointer Word in the Monitor Command Stack.

FORMAT ERROR: If set, indicates that a message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.).

RESPONSE TIMEOUT: If set, indicates that an RT has either not responded or has responded later than the programmed No Response Timeout time. The ACE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the nominal values (±1 µs) 18.5, 22.5, 50.5, and 130 µs by means of bits 10 and 9 of Configuration Register #5.

GOOD DATA BLOCK TRANSFER: Set to logic "1" following completion of a valid (error-free) message, set to logic "0" following completion of an erroneous (invalid) message.

DATA STACK ROLLOVER: If DATA STACK ROLLOVER is logic "1," indicates that the current message resulted in the value of the Monitor Data Stack Pointer rolling over, from the bottom to the top of its range. The size of the Monitor Data Stack is programmable from among 512, 1K, 2K, 4K, 8K, 16K, 32K, and 64K words by means of bits 10, 9, and 8 of Configuration Register #3.

WORD COUNT ERROR: If set, indicates that either a BC or a responding RT did not transmit with the correct number of Data Words.

INCORRECT SYNC TYPE: If set, indicates that a BC transmitted a Data sync with a Command Word or a Command/Status sync with a Data Word, or a responding RT responded with a Data sync in a Status Word and/or a Command/Status sync in a Data Word.

INVALID WORD: Indicates a BC transmitted, or an RT responded with one or more words containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

RT-to-RT GAP/SYNC/ADDRESS ERROR: This bit is set if one or more of the following occur: (1) If the GAP CHECK ENABLED bit (bit 8) of Configuration Register #5 is set to logic "1" **and** a the transmitting RT responds with a response time of less than 4 µs, per MIL-STD-1553B (mid-parity bit to mid-sync); i.e., less than 2 µs dead time; and/or (2) A responding RT for an RT-to-RT transfer responds with an invalid Status Word (encoding, bit count, and/or parity error) or a Data Word sync in its Status Word and/or; (3) The RT Address field of the command word does not match the RT address in the RT status response.

RT-to-RT SECOND COMMAND ERROR: For an RT-to-RT transfer, this bit set to logic "1" indicates one or more of the following error conditions in the second of two contiguous Command Words: (1) T/R bit = logic "0"; (2) subaddress = 00000 or 11111; (3) The RT Address in the transmit Command Word is the same as the RT Address in the receive Command Word.

COMMAND WORD CONTENTS ERROR: Indicates that a received Command Word is not defined in accordance with MIL-STD-1553B. This includes the following undefined Command Words: (1) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** the Command Word is a non-mode code, broadcast, transmit command; (2) The OVERRIDE MODE T/R* ERROR bit, bit 6 of Configuration Register #3, is logic "0" **and** a message with a the Command Word had a T/R* bit of "0," a subaddress/mode field of 00000 or 11111 and a mode code field between 00000 and 01111; (3) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** the Command Word is a broadcast command of a mode code that is not permitted to be broadcast to the broadcast address (11111).

Superseding Commands

A superseded message sequence occurs when a valid message begins on one bus, followed by a time gap, followed by a new command on the alternate bus. If both the old and the new command are to the same RT Address, the RT **must** stop processing the first command, and begin processing the new command. If the commands are to different RT Addresses, the terminal responding to the first command **must** complete processing the message and ignore the activity on the alternate bus.

The ACE selective message monitor will abort processing the first message and begin processing the new message. The only exception to this is when the ACE is operating in the combined RT/Selective Message and the first command is to the ACE's RT Address **and** the second command is to different, nonbroadcast, RT Address. As an RT, the ACE must continue processing the first command (in compliance with MIL-STD-1553), and ignore the new command to a different terminal on the alternate bus.

The ACE selective message monitor will supersede a message on the same bus except when the superseding command may be interpreted as a status word. Hence, a RT status response with the wrong RT address in the status word will NOT appear to the ACE selective message monitor as a new command, but rather will appear to be a bad status word.

When a message is superseded, a normal Start Of Message (SOM) sequence is performed on the new (superseding) message. Note that an End Of Message (EOM) sequence is NOT executed on the original

(superseded) message. This will result in a command stack entry with the Start Of Message (SOM) bit in the block status word set to logic "1" and the End Of Message (EOM) bit set to logic "0." The host processor can distinguish between a message in progress and a superseded message by the value of the monitor command stack pointer. If the monitor command stack pointer has incremented beyond the command stack entry in question and the block status word indicates an SOM state, then the message must have been superseded.

SELECTIVE MESSAGE MONITOR START- AND END-OF-MESSAGE TRANSFER SEQUENCES

Approximately 1.25 µs following the mid-parity bit crossing of a received Command Word, the ACE performs the Selective Monitor Start-of-Message (SOM) sequence. After the first two steps of the SOM sequence, the ACE determines if the message is "selected" (to be stored); this is a function of the RT address, T/R bit, and Subaddress fields of the received Command Word. Approximately 6 µs after the end of the last word received for a selected message, the ACE performs the MT End-of-Message (EOM) Sequence. The MT SOM and EOM sequences consist of sequences of words read from and written to the ACE's shared RAM. The Monitor SOM and EOM sequences are summarized below:

MT Start-of-Message (SOM) Sequence.

1. Corresponding to the RT address, T/R* bit, and subaddress of the received Command Word, the appropriate Monitor Selection word is read from the Monitor Selection table.

2. The Monitor Command Stack Pointer is read from the active area Monitor Command Stack Pointer location. This address is used to locate the first word of message's block descriptor in the Monitor Command Stack. If the result of step 1 indicated that the message is "selected" (to be stored), continue to step 3. If the message is not "selected," the SOM sequence is terminated.

3. The Monitor Data Stack Pointer is read from the active area Monitor Data Stack Pointer location.

4. The Command Word is written to the fourth location in the descriptor block.

5. The Data Stack Pointer is read from the active area Data Stack Pointer location. This value is used for locating the first location for the current message in the Monitor Data Stack.

6. The Time Tag word is written to the second location in the descriptor block.

7. The Block Status Word is written to the first location in the descriptor block.

8. The value of the Command Stack Pointer read in step 2 is incremented by four and written to the active area Stack Pointer.

MT End-of-Message (EOM) Sequence.

1. The address of the last word stored in the Data Stack is incremented by one (modulo the Data Stack size) and written to the active area Data Stack Pointer location.

2. The Time Tag word is written to the second location in the block descriptor.

3. The Block Status Word is written to the first location in the block descriptor.

SELECTIVE MESSAGE MONITOR PROGRAMMING SEQUENCE (assuming 4K RAM using End-of-Message (EOM) interrupt)

INITIALIZATION

1) Write 0001h to START/RESET Register to reset the device.
2) Write 8000h to CONFIGURATION REGISTER #3 to enable ENHANCED MODE features.
3) Write 8D00h to CONFIGURATION REGISTER #3 to configure the device for ENHANCED MODE enabled, a 1K Monitor Command Stack size and a 2K Monitor Data Stack size.
4) Write 5000h to CONFIGURATION REGISTER #1 to place the device in the Selective Message Monitor mode.
5) Write 0400h to RAM location 0102h to initialize the Monitor Command Stack Pointer.
6) Write 0800h to RAM location 0103h to initialize the Monitor Data Stack Pointer.
7) Initialize the Selective Monitor Lookup Table in RAM locations 0280h to 02FFh. Note that programming FFFFh in all 128 locations will program the ACE to monitor ALL commands.
8) Write 0010h to CONFIGURATION REGISTER #2 to enable interrupt auto clear function.
9) Write 0001h to INTERRUPT MASK register to enable End Of Message (EOM interrupt.
10) Initialize the software variable stkptr to 0400h. This will act as an indicator of the next message that is to be serviced.
11) Write 0002h to START/RESET register to start the monitor.

Notes: The order in which steps 3-10 are executed does not matter.

SERVICING TECHNIQUE

Define an Interrupt Service Routine that will do the following:

a) Read and save value of INTERRUPT STATUS register.
b) Verify that Interrupt Status is 0001h (EOM occurred).
c) Read and store value of RAM location 0102h (Monitor Command Stack Pointer). This value will be referred to as MTCMDPTR.
d) repeat the following sequence until (stkptr = MTCMDPTR) or [(((stkptr + 4) mod stack size) = MTCMDPTR) and (Block status word has som set)]:
    i) Block Status Word = RAM location stkptr.
    ii) Time Tag = RAM location stkptr + 1.
    iii) Data pointer = RAM location stkptr + 2.
    iv) Command Word = RAM location stkptr + 3.
    v) Status and Data words are stored sequentially in RAM locations starting at the value of data

pointer, the number of words and message format is determined by reading bit 11 of the Block Status Word and the contents of the Command Word. If bit 11 of the Block Status Word is logic "1," the message was an RT-to-RT transfer. In addition, you must check for a 2K data stack rollover when reading words from the data stack.

vi) Store and/or use message information must be based on application requirements.

vii) stkptr = (stkptr + 4) modulo 1024. Increment to next message to be serviced, with a 1k rollover.

e) Exit Interrupt Service Routine.

SPECIFICATION TABLE FOR THE BU-65528/BU-65527

TABLE 73. SPECIFICATION TABLE

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATINGS				
Supply Voltage				
• +5 V Supply Voltage	-0.3		7.0	V
• -12 V Supply Voltage	-18.0		+0.3	V
RECEIVER				
Threshold Voltage, Transformer Coupled, meas. on Stub			0.860	V_{P-P}
Common Mode Voltage			10	V_{PEAK}
TRANSMITTER				
Differential Output Voltage				
• Direct Coupled Across 35 ohms, Measured on Bus	6	7	9	V_{P-P}
• Transformer Coupled 70 ohms, Measured on Stub	18	20	27	V_{P-P}
Differential Output Noise (Direct Coupled)			10	$mV_{P-P,diff}$
Output Offset Voltage, Direct Coupled Across 35 ohms	-90		90	mV
Rise/Fall Time	100		300	nsec
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
• +5 V	4.5		5.5	V
• -12 V	-12.6		-11.4	V
Current Drain (Note 1)				
• BU-65528M1/27X1				
• +5 V		600	823	mA
• -12 V				
• Idle		30	60	mA
• 25% Duty Transmitter Cycle		80	108	mA
• 100% Duty Transmitter Cycle		230	255	mA
• BU-65528M2/27X2				
• +5 V		0.8	1.06	A
• -12 V				
• Idle		60	120	mA
• 25% Duty Transmitter Cycle		160	216	mA
• 100% Duty Transmitter Cycle		460	510	mA
• BU-65528M3/27X3				
• +5 V		0.9	1.47	A
• -12 V				
• Idle		90	180	mA
• 25% Duty Transmitter Cycle		160	216	mA
• 100% Duty Transmitter Cycle		460	510	mA
• BU-65528M4/27X4				
• +5 V		1.2	1.71	A
• -12 V				
• Idle		0.120	0.24	A
• 25% Duty Transmitter Cycle		0.320	0.43	A

TABLE 73. SPECIFICATION TABLE

PARAMETER	MIN	TYP	MAX	UNITS
• 100% Duty Transmitter Cycle		0.920	1.02	A
POWER DISSIPATION				
• BU-65528M1/27X1				
• Idle		3.4	4.8	W
• 25% Duty Transmitter Cycle		3.7	5.1	W
• 100% Duty Transmitter Cycle		4.5	5.9	W
• BU-65528M2/27X2				
• Idle		4.7	6.8	W
• 25% Duty Transmitter Cycle		5.3	7.3	W
• 100% Duty Transmitter Cycle		7.0	8.9	W
• BU-65528M3/27X3				
• Idle		5.6	9.5	W
• 25% Duty Transmitter Cycle		6.4	10.3	W
• 100% Duty Transmitter Cycle		9.0	12.8	W
• BU-65528M4/27X4				
• Idle		7.4	11.5	W
• 25% Duty Transmitter Cycle		8.6	12.5	W
• 100% Duty Transmitter Cycle		12.0	15.8	W
1553 MESSAGE TIMING				
RT Response Time	4		7	µs
Completion of CPU Write (BC Start-to-Start of First BC Message)		2.5		µs
BC Intermessage Gap (Note 2)		9.5		µs
BC/RT/MT Response Timeout (Note 3)				
• 18.5 nominal	17.5	18.5	19.5	µs
• 22.5 nominal	21.5	22.5	23.5	µs
• 50.5 nominal	49.5	50.5	51.5	µs
• 130.0 nominal	127	130	131	µs
Transmitter Watchdog Timeout		668		µs
ENVIRONMENT				
BU-65528/65527C				
Operating Component Temperature (ambient)	0		+70	°C
Storage Temperature	-20		+65	°C
BU-65527M				
Operating Temperature (measured at the card guides)	-55		+85	°C
Maximum Component junction temperatures			+130	°C
Storage Temperature	-55		+125	°C
Vibration	Random vibration, $0.1g^2$/Hz from 20 Hz to 2000 Hz			
Shock	40g, 11ms, half sine			
Operating humidity	0 to 95% non-condensing			
Non-operating humidity	100% condensing			
PHYSICAL CHARACTERISTICS				
Size				
• "B" Size	6.3 X 9.2 X 0.6			in

TABLE 73. SPECIFICATION TABLE

PARAMETER	MIN	TYP	MAX	UNITS
	(160.0 X 233.7 X 15.2)			(mm)
PHYSICAL CHARACTERISTICS (cont'd)				
Weight				
• BU-65528, 65527C		13.5 (383.1)		oz (g)
• BU-65527M		20 (567)		oz (g)

Notes:

(1) Assumes all installed 1553 channels (1, 2, 3, 4) on card are transmitting at the specified duty cycle on only one of the dual-redundant MIL-STD-1553A/B Notice 2 data buses.

(2) Typical value for minimum intermessage gap time. Under software control, may be lengthened to 65,535 μS (minus message time), in increments of 1 μS.

(3) Software-programmable options (up to 4) are listed. Includes RT-to-RT Timeout (mid-parity of Transmit command to mid-Sync of Transmitting RT's Status).

TABLE 74. BU-65528 P1 AND P2 PIN CONNECTIONS

P1 PIN DEFINITIONS						P2 PIN DEFINITIONS					
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	D0	B1		C1	D8	A1		B1		C1	
A2	D1	B2		C2	D9	A2		B2		C2	
A3	D2	B3		C3	D10	A3		B3		C3	
A4	D3	B4		C4	D11	A4		B4	A24	C4	
A5	D4	B5		C5	D12	A5		B5	A25	C5	
A6	D5	B6		C6	D13	A6		B6	A26	C6	
A7	D6	B7		C7	D14	A7		B7	A27	C7	
A8	D7	B8		C8	D15	A8		B8	A28	C8	
A9	GND	B9		C9	GND	A9		B9	A29	C9	
A10		B10		C10		A10		B10	A30	C10	
A11	GND	B11		C11		A11		B11	A31	C11	
A12	DS1*	B12		C12	SYSRST*	A12		B12	GND	C12	
A13	DS0*	B13		C13		A13		B13	+5V	C13	
A14	WRITE*	B14		C14	AM5	A14		B14		C14	
A15	GND	B15		C15	A23	A15		B15		C15	
A16	DTACK*	B16	AM0	C16	A22	A16		B16		C16	
A17	GND	B17	AM1	C17	A21	A17		B17		C17	
A18	AS*	B18	AM2	C18	A20	A18		B18		C18	
A19	GND	B19	AM3	C19	A19	A19		B19		C19	
A20	IACK*	B20	GND	C20	A18	A20		B20		C20	
A21	IACKIN*	B21		C21	A17	A21		B21		C21	
A22	IACKOUT*	B22		C22	A16	A22		B22		C22	
A23	AM4	B23	GND	C23	A15	A23		B23		C23	
A24	A7	B24	IRQ7*	C24	A14	A24		B24		C24	
A25	A6	B25	IRQ6*	C25	A13	A25		B25		C25	
A26	A5	B26	IRQ5*	C26	A12	A26		B26		C26	
A27	A4	B27	IRQ4*	C27	A11	A27		B27		C27	
A28	A3	B28	IRQ3*	C28	A10	A28		B28		C28	
A29	A2	B29	IRQ2*	C29	A9	A29		B29		C29	
A30	A1	B30	IRQ1*	C30	A8	A30		B30		C30	
A31	-12V	B31		C31		A31		B31	GND	C31	
A32	+5V	B32	+5V	C32	+5V	A32		B32	+5V	C32	

TABLE 75. BU-65527CX and BU-65527MX P1 AND P2 PIN CONNECTIONS

P1 PIN DEFINITIONS						P2 PIN DEFINITIONS					
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	D0	B1		C1	D8	A1	IOADR11	B1		C1	IOADR13
A2	D1	B2		C2	D9	A2	IOADR12	B2		C2	IOADR14
A3	D2	B3		C3	D10	A3	IOADR10	B3		C3	IOADR15
A4	D3	B4		C4	D11	A4	GND	B4	A24	C4	GND
A5	D4	B5		C5	D12	A5	RTAD0_CH3	B5	A25	C5	RTAD3_CH3
A6	D5	B6		C6	D13	A6	RTAD1_CH3	B6	A26	C6	RTAD4_CH3
A7	D6	B7		C7	D14	A7	RTAD2_CH3	B7	A27	C7	RTADP_CH3
A8	D7	B8		C8	D15	A8	BUS3_A+	B8	A28	C8	BUS3_B+
A9	GND	B9		C9	GND	A9	BUS3_A-	B9	A29	C9	BUS3_B-
A10		B10		C10		A10	+5V	B10	A30	C10	+5V
A11	GND	B11		C11		A11	RTAD0_CH2	B11	A31	C11	RTAD3_CH2
A12	DS1*	B12		C12	SYSRST*	A12	RTAD1_CH2	B12	GND	C12	RTAD4_CH2
A13	DS0*	B13		C13		A13	RTAD2_CH2	B13	+5V	C13	RTADP_CH2
A14	WRITE*	B14		C14	AM5	A14	BUS2_A+	B14		C14	BUS3_B+
A15	GND	B15		C15	A23	A15	BUS2_A-	B15		C15	BUS3_B-
A16	DTACK*	B16	AM0	C16	A22	A16	GND	B16		C16	GND
A17	GND	B17	AM1	C17	A21	A17	RTAD0_CH1	B17		C17	RTAD3_CH1
A18	AS*	B18	AM2	C18	A20	A18	RTAD1_CH1	B18		C18	RTAD4_CH1
A19	GND	B19	AM3	C19	A19	A19	RTAD2_CH1	B19		C19	RTADP_CH1
A20	IACK*	B20	GND	C20	A18	A20	BUS1_A+	B20		C20	BUS1_B+
A21	IACKIN*	B21		C21	A17	A21	BUS1_A-	B21		C21	BUS1_B-
A22	IACKOUT*	B22		C22	A16	A22	+5V	B22		C22	+5V
A23	AM4	B23	GND	C23	A15	A23	RTAD0_CH1	B23		C23	RTAD3_CH4
A24	A7	B24	IRQ7*	C24	A14	A24	RTAD1_CH1	B24		C24	RTAD4_CH4
A25	A6	B25	IRQ6*	C25	A13	A25	RTAD2_CH1	B25		C25	RTADP_CH4
A26	A5	B26	IRQ5*	C26	A12	A26	BUS4_A+	B26		C26	BUS4_B+
A27	A4	B27	IRQ4*	C27	A11	A27	BUS4_A-	B27		C27	BUS4_B-
A28	A3	B28	IRQ3*	C28	A10	A28	GND	B28		C28	GND
A29	A2	B29	IRQ2*	C29	A9	A29	+5V	B29		C29	+5V
A30	A1	B30	IRQ1*	C30	A8	A30	IOADR9	B30		C30	IOADR8
A31	-12V	B31		C31		A31	SSFLAG_CH1	B31	GND	C31	SSFLAG_CH3
A32	+5V	B32	+5V	C32	+5V	A32	SSFLAG_CH2	B32	+5V	C32	SSFLAG_CH4

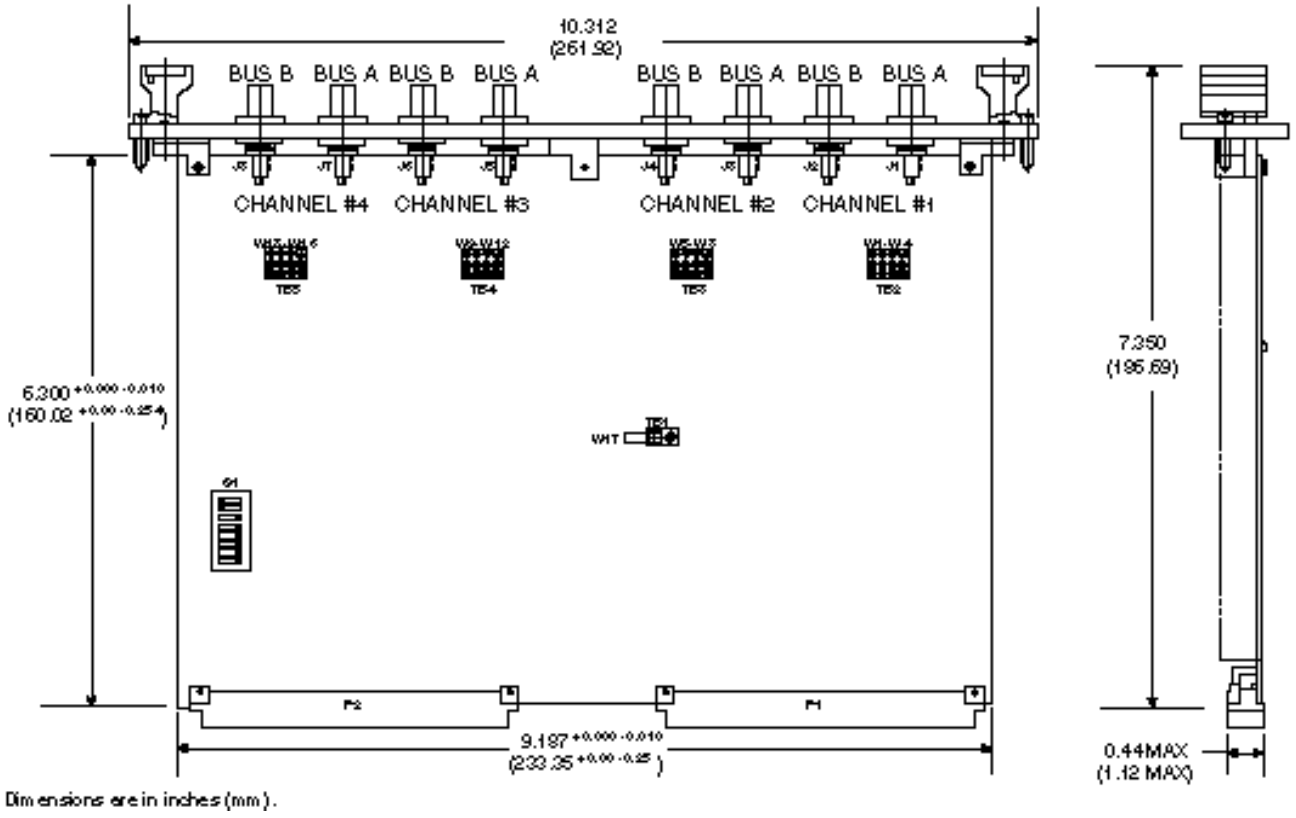


FIGURE 17. BU-65528 MECHANICAL OUTLINE

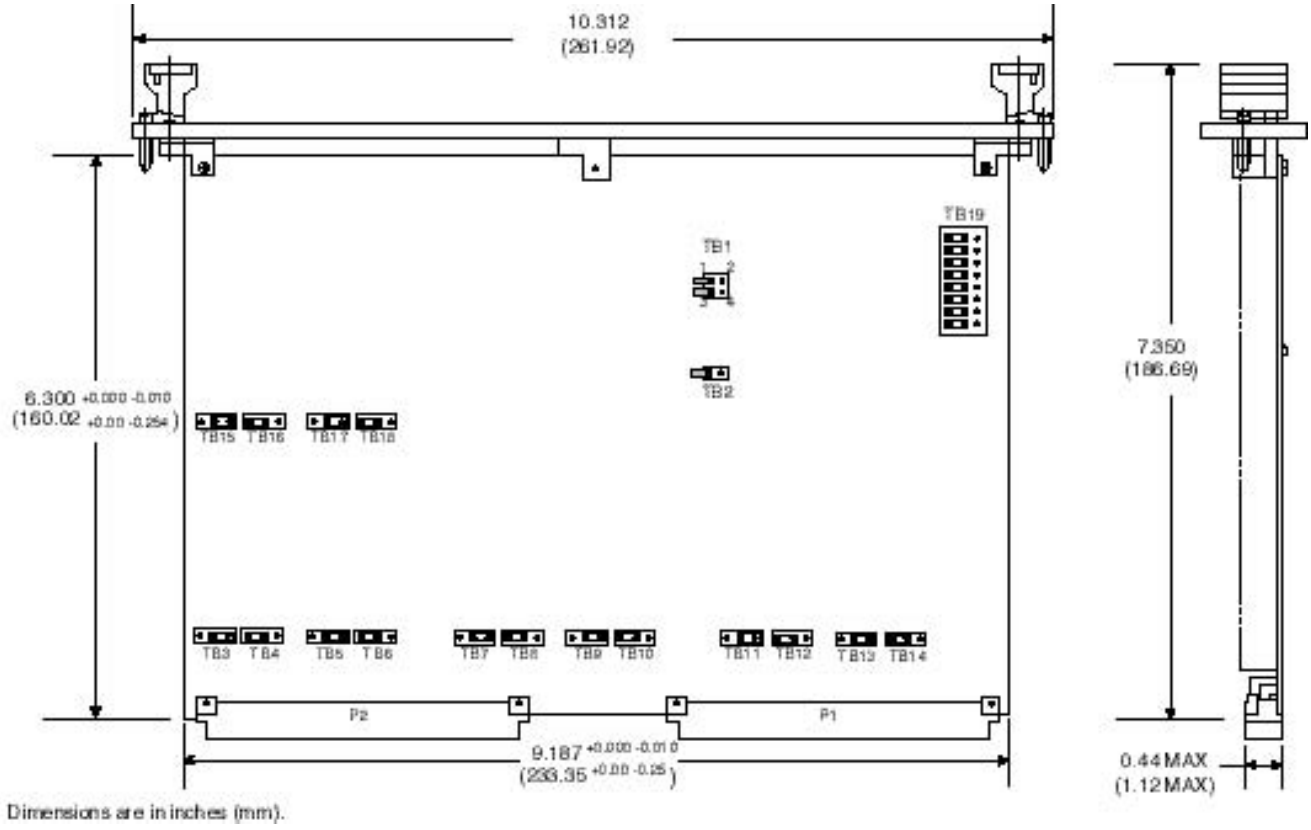


FIGURE 18. BU-65527C MECHANICAL OUTLINE

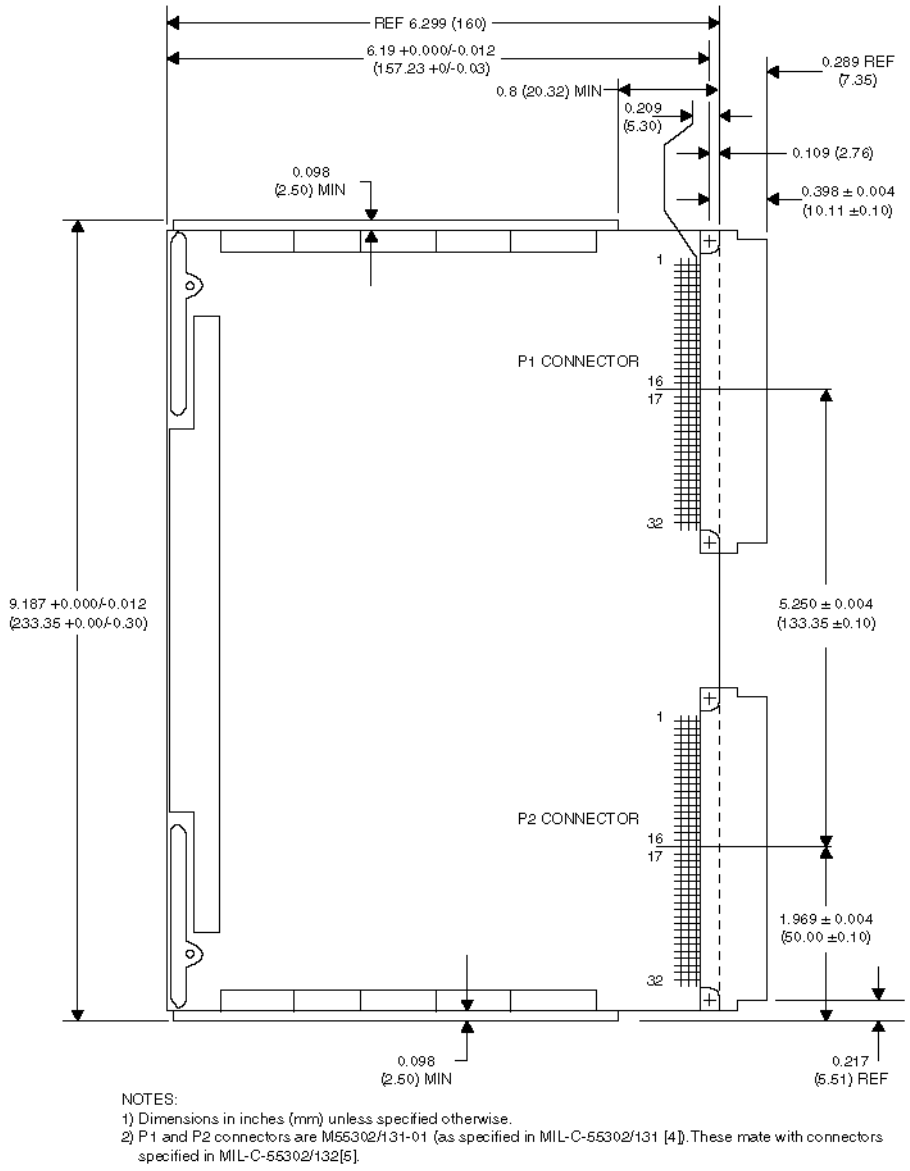


FIGURE 19. BU-65527M MECHANICAL OUTLINE

FEATURE COMPARISON MATRIX FOR BU-65528/27

Feature Comparison for BU-65528/27 VME/VXI MIL-STD-1553 BC/RT/MT Interface Cards			
FEATURES	**BU-65527CX**	**BU-65527MX**	**BU-65528MX**
ACE Component	BU-61585	BU-61585	BU-61586
Shared RAM	12K x 16	12K x 16	12K x 16
RT Address	Hardwired on Backplane	Hardwired on Backplane	Latchable
VME/VXI Compatibility	VME Only	VME Only	VME/VXI
Cooling	Air-Cooled	Conduction-Cooled	Air-Cooled
Wedge Locks	No	Yes	No
Operating Component Temp. Range	-300: 0 to +70°C	-200: -55 to +85°C	-300: 0 to +70°C
Register Base Address Selection	User selectable thru terminal blocks or backplane hardwired	User selectable thru backplane hardwired	User selectable thru DIP switch
1553 Bus Coupling	User selectable thru terminal blocks for transformer or direct coupling	Factory hardwired for transformer coupling (call for direct coupling)	User selectable thru terminal blocks for transformer or direct coupling
1553 Bus Access	Via P2 Connector and backplane	Via P2 Connector and backplane	Via Bus Connectors on top panel
A24/A32 Mode Addressing	User selectable thru terminal block	Factory hardwired for A24 addressing mode (call for A32 addressing mode)	User selectable thru terminal block
Number of Channels	X = 1, 2, 3, or 4 User selectable at time of purchase. Number of channels factory set by terminal block based on order.	X = 1, 2, 3, or 4 User selectable at time of purchase. Number of channels factory hardwired based on order.	X = 1, 2, 3, or 4 User selectable at time of purchase. Number of channels factory set by terminal block based on order.
Weight	13.5 oz. (Fully populated)	20.0 oz. (Fully populated)	13.5 oz. (Fully populated)
Conformal Coating	No	Yes	No
MTBF @ 35°C Ground Benign	393 Khrs	1.845Mhrs	393 Khrs

ORDERING INFORMATION

BU- 65528M3-300

Temperature Range

2 = -55 to +85°C (for BU-65527MX)
3 = 0 to 70°C (for BU-65527CX, BU-65528MX)

Board Configuration

1 = 1 Dual Redundant 1553 Channel
2 = 2 Dual Redundant 1553 Channel
3 = 3 Dual Redundant 1553 Channel
4 = 4 Dual Redundant 1553 Channel

Product Type

65527M = Conduction Cooled VME MIL-STD-1553 Interface Unit
65527C = Air Cooled Standard VME MIL-STD-1553 Interface Unit
65528M = Air Cooled Standard VME/VXI MIL-STD-1553 Interface Unit with RT Address Latch, Top Panel Bus Connectors

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