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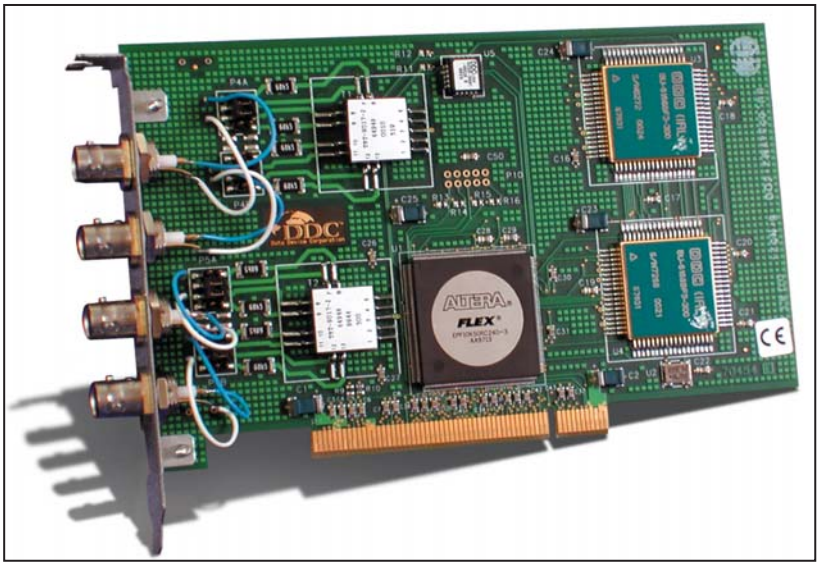
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Find the *DDC BU65549M1* at our website: *Click HERE*

BU-65549 Data Sheet

MIL-STD-1553 BC/RT/MT PCI INTERFACE CARD



DESCRIPTION

The BU-65549 provides full, intelligent interfacing between a PCI bus and one or two independent dual redundant MIL-STD-1553B Data Buses. Software controls the operation of each channel as either a 1553 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT).

The board features DDC's Mini-ACE® Plus hybrids. As such, each channel includes dual transceivers and encoders/decoders, complete 1553B protocol, 64K words of shared RAM and memory management logic for all three modes.

Background Mode Operation prevents inadvertent access to the card during power-on self-test.

On-board Interrupt Mask and Interrupt Status Registers support flexible operation for both interrupt and polling applications.

The memory management scheme for RT mode provides an option for separation of broadcast data plus a circular buffer option for individual RT subaddresses to offload the PC host CPU.

Additional features include a wrap-around Built-In-Test, register programmable interrupt level, software programmable RT address selection and a free "C" software subroutine library. Its full compliance with MIL-STD-1553A and B makes it an excellent choice for real-time simulation, test, and system integration applications.

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FEATURES

- PCI Interface Card
- 1553B Notice 2 Dual Redundant BC/RT/MT (STANAG 3838 Compliant)
- Single or Dual Channel
- 64K X 16 Shared RAM per Channel
- Free "C" Runtime Libraries for Windows® 9x/2000/XP, Windows NT® and Linux
- Free Windows 9x/2000/XP and Windows NT Graphical User Interface
- Programmable BC Gap Times
- BC Frame Auto-Repeat
- Flexible RT Data Buffering
- Monitor Command Filtering
- Simultaneous RT/Monitor
- Flexible Interrupt Generation

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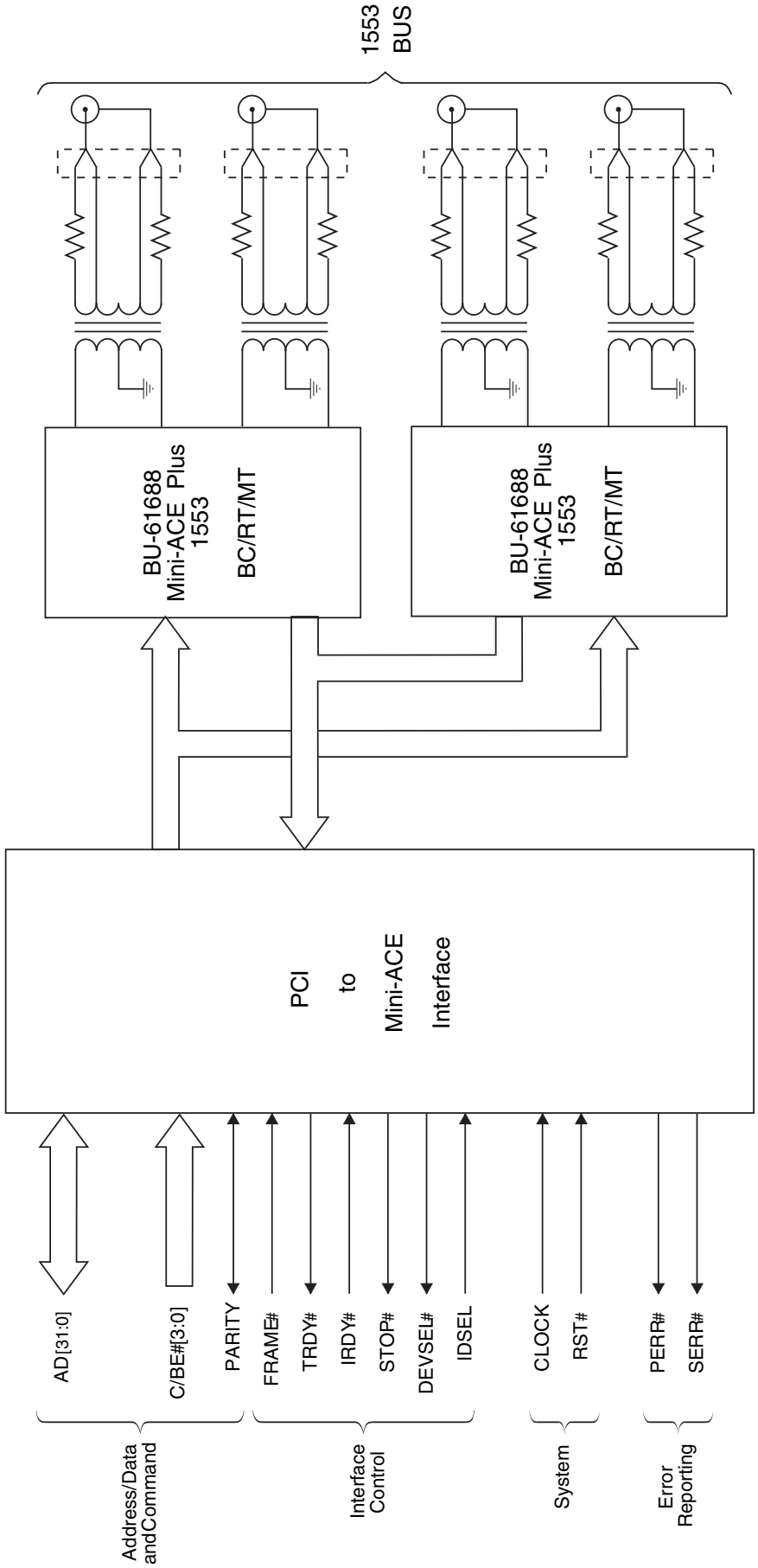


FIGURE 1. BU-65549 BLOCK DIAGRAM

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TABLE 1. BU-65549 SPECIFICATIONS				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
ABSOLUTE MAXIMUM RATINGS				
+5 V Supply Voltage	-0.3		6.0	V
RECEIVER				
Threshold Voltage, Transformer Coupled, Measured on Stub	0.2		0.860	V_{P-P}
Common-Mode Voltage			10	V_{PEAK}
TRANSMITTER				
Differential Output Voltage				
■ Direct Coupled Across 35 ohms, Measured on Bus	6	7	9	V_{P-P}
■ Transformer Coupled, Measured on Stub	18	21	27	V_{P-P}
Output Noise, Differential (Direct Coupled)			10	mV_{P-P}, diff
Output Offset Voltage, Direct Coupled Across 35 ohms	-90		90	mV
Rise/Fall Time	100		300	nsec
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
■ + 5 V	4.75	5.0	5.5	V
Current Drain				
■BU-65549M1				
Idle		0.30	0.5	A
25% Transmitter Duty Cycle		0.43	0.65	A
50% Transmitter Duty Cycle		0.55	0.80	A
100% Transmitter Duty Cycle		0.80	1.10	A
■BU-65549M2				
Idle		0.48	0.8	A
25% Transmitter Duty Cycle		0.73	1.10	A
50% Transmitter Duty Cycle		0.98	1.40	A
100% Transmitter Duty Cycle		1.48	2.00	A
POWER DISSIPATION				
BU-65549M1				
■ Idle		1.50	2.80	W
■ 25% Duty Cycle		1.80	3.29	W
■ 50% Transmitter Duty Cycle		2.10	3.78	W
■100% Transmitter Duty Cycle		2.70	4.75	W
BU-65549M2				
■ Idle		2.40	4.40	W
■ 25% Duty Cycle		3.00	5.40	W
■ 50% Transmitter Duty Cycle		3.60	6.40	W
■ 100% Transmitter Duty Cycle		4.80	8.40	W
1553 MESSAGE TIMING				
RT Response Time	4		7	µsec
Completion of CPU Write (BC Start-to Start of FIRST BC Message)		2.5		µsec
BC Intermessage Gap (See Note 1)		9.5		µsec
BC/RT/MT Response Timeout (See Note 2)				
■ 18.5 nominal	17.5	18.5	19.5	µsec
■ 22.5 nominal	21.5	22.5	23.5	µsec
■ 50.5 nominal	49.5	50.5	51.5	µsec
■ 128.0 nominal	127	128	129	µsec
Transmitter Watchdog Timeout		668		µsec
THERMAL				
Operating Temperature	0		55	°C
Storage Temperature	-20		65	°C
PHYSICAL CHARACTERISTICS				
Size	6.80 x 4.50 (172.7 x 114.3)			in (mm)
Weight	6.0 (170)			oz (g)

TABLE 1 notes:
1. Under software control, minimum intermessage gap time may be lengthened to (65,535 ms minus message time), in increments of 1 µs.
2. Software programmable (4 options). Includes RT-to-RT Timeout (Mid-Parity of Transmit Command to Mid-Sync of Transmitting RT Status).

FUNCTIONAL OVERVIEW

GENERAL

The BU-65549 provides a user-friendly interface between the serial MIL-STD-1553B Notice 2 Bus and a PCI bus. The operating modes of the BU-65549 are controlled through the use of 24 on-board registers. 1553 message traffic is stored and retrieved using the shared, memory mapped, on-board 64K words of RAM. The various registers that control and operate the BU-65549 include the Configuration Registers, Start/Reset Register, Time Tag Register, Interrupt Mask Register, Interrupt Status Register, Subaddress Control Word Register, Memory Base Address Register, and Control/RT Address Register. The Configuration Registers define the operating mode and memory management features. The Start/Reset Register provides various reset and BC/MT start functions. The Interrupt Mask Register enables desired interrupts, with the interrupt priority level being register controlled. The cause of interrupts may be determined by a single read operation, by means of the Interrupt Status Register. The Control/RT Address Register is used to program the RT address and miscellaneous functions. The Time Tag Register features programmable resolution and is used to time tag messages in BC or RT modes. The Memory Base Address Register supports a software programmable base memory address and controls the background mode operation.

The BU-65549's 64K x 16 of static RAM per channel is shared by the PC host and the 1553 Bus with memory arbitration handled automatically by the BU-65549.

In addition to storing the 1553 message data, the RAM implements the Stacks and Look-Up Tables required for the different modes of operation. For RT mode, there is a programmable option to separate broadcast message data from non-broadcast data, providing compliance to MIL-STD-1553B Notice 2. In addition, for RT mode, there is the choice of storing either a single message, a double buffer data structure or a circular buffer data structure for each transmit or receive subaddress. The size of the circular buffer is programmable up to 8192 words, on a Tx/Rx/Bcst-subaddress basis. A global double buffering mechanism is available to prevent partially updated information from being transferred to or from the 1553 Bus.

The BU-65549 supports programmable command illegalization for RT mode. This allows individual Command Words to be illegalized as a function of T/$\overline{R}$ bit, subaddress, and word count/mode code. Since the illegalization scheme is RAM based, it is inherently self-testable.

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A Descriptor Stack is maintained in BC, RT and MT modes. This records the status of each message, the time the message was transmitted or received, and contains either the received 1553 command and Data Block Pointer (in RT or MT mode) or the actual address of the 1553 message block (in BC mode). In RT mode, a Lookup Table is provided to define the addresses of the data blocks to to be used when receiving or transmitting messages for the individual subaddresses.

The BU-65549 RT mode is multiprotocol, supporting MIL-STD-1553A, MIL-STD-1553B Notice 2, STANAG 3838, and the McAir A3818, A5232, and A5690 protocols.

The BU-65549 implements three monitor modes: a word monitor, a selective message monitor, and a combined RT/selective message monitor.

MEMORY MANAGEMENT

The BU-65549 incorporates complete memory management and processor interface logic. The software interface to the host processor is implemented by means of 24 onboard registers and 64K words of RAM. For all three modes, a stack area of RAM is maintained. In BC mode, the stack allows for the scheduling of multi-message frames. For all three modes, the stack provides a real-time chronology of all messages processed. In addition to the stack processing, the memory management logic performs storage, retrieval, and manipulation functions involving pointer and message data structures for all three modes.

The BU-65549 provides a number of programmable options for RT mode memory management. In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from non-broadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block, a subaddress-specific double-buffered configuration or a variable-sized (128 to 8192 words) circular buffer may be allocated for data storage. In addition to helping ensure data consistency, the circular buffer feature provides a means of greatly reducing host processor overhead for bulk data transfer applications. End-of-message interrupts may be enabled either globally, following error messages, on a Tx/Rx/Bcst-subaddress basis, or when any particular Tx/Rx/Bcst-subaddress circular buffer reaches its lower boundary.

INTERRUPTS

Individual events are enabled by the Interrupt Mask Register. The host processor may easily determine the cause of the interrupt by reading the Interrupt Status Register. The Interrupt Status Register provides the current state of the interrupt conditions. The Interrupt Status Register may be updated in two ways. In the standard interrupt handling mode, a particular bit in the Interrupt Status Register will be updated only if the condition exists and the corresponding bit in the Interrupt Mask Register is enabled. In the enhanced interrupt handling mode, a particular bit in the Interrupt Status Register will be updated if the condition exists regardless of the contents of the corresponding Interrupt Mask Register bit. In any case, the respective Interrupt Mask Register bit enables an interrupt for a particular condition.

The BU-65549 provides maskable interrupts and 15-bit Interrupt Status Register for end of message, end of BC message list, erroneous messages, Status Set (BC mode), Time Tag Register Rollover, RT Address Parity Error conditions, BC retry, data stack rollover, command stack rollover, transmitter watchdog timeout, or RAM parity error. The Interrupt Status Register allows the host processor to determine the cause of all interrupts by means of a single read operation.

INTERNAL COMMAND ILLEGALIZATION

The BU-65549 offers the option to illegalize commands in RT mode. The illegalization architecture allows for any subset of the 4096 possible combinations of broadcast/own address, $T/\overline{R}$ bit, subaddress, and word count/mode code to be illegalized. The BU-65549 illegalization scheme is under software control of the host processor. As a result, it is inherently self-testable.

INTERNAL TIME TAG

The BU-65549 includes an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 µs per LSB. For each message processed, the value of the Time Tag register is loaded into the second location of the respective descriptor stack entry (“TIME TAG WORD”) for both BC and RT modes.

Additional options are provided to clear the Time Tag Register following a Synchronize (without data) mode command or load the Time Tag Register following a Synchronize (with data) mode command. Another option enables an interrupt request and a bit in the Interrupt Status Register to be set when the Time Tag Register rolls over from FFFF to 0000(hex). Assuming the Time Tag Register is not loaded or reset, this will occur at approximately 4-second time intervals, for 64 µs/LSB resolution, down to 131 ms intervals, for 2 µs/LSB resolution. Another programmable option for RT mode is for the Service Request Status Word bit to be automatically cleared following the BU-65549's response to a Transmit Vector Word mode command.

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ADDRESSING, INTERNAL REGISTERS, MEMORY MANAGEMENT, AND INTERRUPTS

ADDRESSING THE BU-65549

The BU-65549 makes use of two memory mapped I/O spaces; one for the ACE's registers and the other for the ACE's shared memory. The memory base addresses of these I/O spaces are specified by the base address registers within the BU-65549's PCI Device Configuration Header. These registers are typically programmed by the PCI bus enumerator which is a part of the operating system running on the host computer.

The memory base address of the ACE's registers is specified by Base Address Register 0 in the BU-65549's PCI Device Configuration Header. The single channel BU-65549M1 implements a Base Address 0 register which specifies a memory mapped register space of 128 bytes while the dual channel BU-65549M2 implements a register space of 256 bytes (128 bytes per channel). TABLE 2 illustrates the address map for the BU-65549's memory mapped register space.

MEMORY ADDRESS MAP

The memory base address of the ACE's shared RAM is specified by Base Address Register 1 in the BU-65549's PCI Device Configuration Header. The single channel BU-65549M1 implements a shared RAM size of 128K bytes (64K words) while the dual channel BU-65549M2 implements a shared RAM size of 256K bytes (64K words per channel). TABLE 3 illustrates the address map for the BU-65549's memory mapped shared RAM space.

Read or writes of the ACE's shared RAM may be either word (16-bit) or double word (32-bit) transfers. Byte (8-bit) write transfers are not permitted. Byte (8-bit) read transfers will return the same data as a word (16-bit) read.

REGISTER MAP

The software interface of the BU-65549 to the host processor consists of 17 internal operational registers for normal operation, an additional 8 test registers, plus 64Kx16 of shared memory per channel. Both the registers and the shared memory reside in the ISA memory space.

Each ACE register is 16 bits. Registers must be accessed using word (16-bit) transfers. ACE Registers cannot be accessed using double-word (32-bit) transfers. Byte (8-bit) write transfers are not permitted. Byte (8-bit) read transfers will return the same data as word reads.

There is an additional register, at PCI bus address offset 0800, used to designate the card configuration (ACE memory size) and which ACE channel(s) have issued interrupt requests.

TABLE 2. REGISTER ADDRESS MAP

	ADDRESS		DESCRIPTION
	PCI BUS	ACE OFFSET	
CHANNEL 1	0000	0000	Interrupt Mask Register (RD/WR)
	0002	0001	Configuration Register #1 (RD/WR)
	0004	0002	Configuration Register #2 (RD/WR)
	0006	0003	Start/Reset Register (WR)
	0006	0003	BC/RT Command Stack Pointer Register (RD)
	0008	0004	BC Control Word/RT Subaddress Control Word Register (RD/WR)
	000A	0005	Time Tag Register (RD/WR)
	000C	0006	Interrupt Status Register (RD)
	000E	0007	Configuration Register #3 (RD/WR)
	0010	0008	Configuration Register #4 (RD/WR)
	0012	0009	Configuration Register #5 (RD/WR)
	0014	000A	Data Stack Address Register (RD/WR)
	0016	000B	BC Frame Time Remaining Register (RD)*
	0018	000C	BC Frame Time Remaining to Next Message Register (RD)*
	001A	000D	BC Frame Time*/RT Last Command/MT Trigger Word* Register (RD/WR)
	001C	000E	RT Status Word Register (RD)
	001E	000F	RT BIT Word Register (RD)
CHANNEL 2	0080	0000	Interrupt Mask Register (RD/WR)
	0082	0001	Configuration Register #1 (RD/WR)
	0084	0002	Configuration Register #2 (RD/WR)
	0086	0003	Start/Reset Register (WR)
	0086	0003	BC/RT Command Stack Pointer Register (RD)
	0088	0004	BC Control Word/RT Subaddress Control Word Register (RD/WR)
	:	:	
	009C	000E	RT Status Word Register (RD)
	009E	000F	RT BIT Word Register (RD)
CHANNEL 1 & 2	0800	-	Configuration / Master Interrupt Register

Notes:
1. PCI addresses are specified as the 'BYTE' offset within the BU-65549 register Space

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TABLE 3. SHARED RAM SPACE ADDRESS MAP	
PCI ADDRESS	**DESCRIPTION**
00000	ACE Channel #1 RAM Location 0000
00002	ACE Channel #1 RAM Location 0001
00004	ACE Channel #1 RAM Location 0002
: :	
1FFFE	ACE Channel #1 RAM Location FFFF
20000	ACE Channel #2 RAM Location 0000
20002	ACE Channel #2 RAM Location 0001
20004	ACE Channel #2 RAM Location 0002
: :	
3FFFE	ACE Channel #2 RAM Location FFFF

Notes:
1. PCI addresses are specified as the 'BYTE' offset within the BU-65549 shared RAM space.
2. ACE addresses are specified as the 'WORD' offset within the ACE's internal shared RAM.

ACE memory transfers may be either 32-bit or 16-bit. Write transfers may be in bursts of up to 32 words.

Definition of the address mapping and accessibility for the BU-65549's 17 nontest ACE registers, and the ACE test registers, is as follows:

Interrupt Mask Register: Used to enable and disable interrupt requests for various conditions.

Configuration Registers #1 and #2: Used to select the BU-65549's mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-on-Error, RT Memory Management mode selection, and control of the Time Tag operation.

Start/Reset Register: Used for "command" type functions, such as software reset, BC/MT Start, Interrupt Reset, Time Tag Reset, and Time Tag Register Test. The Start/Reset Register includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

BC/RT Command Stack Pointer Register: Allows the host CPU to determine the pointer location for the current or most recent message when the BU-65549 is in BC or RT modes.

BC Control Word/RT Subaddress Control Word Register: In BC mode, allows host access to the current or most recent BC Control Word. The BC Control Word contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. In RT mode, this register allows host access to the current or most recent Subaddress Control Word. The Subaddress Control Word is used to select the memory management scheme and enable interrupts for the current message.

Time Tag Register: Maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of RAM.

Interrupt Status Register: Mirrors the Interrupt Mask Register and contains a Master Interrupt bit. It allows the host processor to determine the cause of an interrupt request by means of a single read access.

Configuration Registers #3, #4, and #5: Used to enable many of the BU-65549's advanced features. These include all of the Enhanced mode features. For all three modes (BC, RT and MT), use of the Enhanced Mode also enables the various read-only bits in Configuration Register #1.

For BC mode, the Enhanced mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message.

For RT mode, the Enhanced mode features include the expanded RT Block Status Word, the combined RT/Selective Message Monitor mode, internal wrapping of the internal $\overline{\text{RTFAIL}}$ signal to the $\overline{\text{RTFLAG}}$ RT Status Word bit, the double buffering scheme for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word. For MT mode, use of Enhanced mode enables use of the Selective Message Monitor, the combined RT/Selective Monitor mode, and the monitor triggering capability.

MT Data Stack Address Register: Used to point to the current address location in shared RAM used for storing message words (second Command Words, Data Words, RT Status Words) in the Selective Word Monitor mode.

Frame Time Remaining Register: Provides a read only indication of the time remaining in the current BC frame. The resolution of this register is 100 µs/LSB.

Message Time Remaining Register: Provides a read only indication of the time remaining before the start of the next message in a BC frame. The resolution of this register is 1 µs/LSB.

BC Frame Time / RT Last Command / MT Trigger Word Register: In BC mode, this register is used to program the BC frame time, for use in the frame auto-repeat mode. The resolution of this register is 100 µs/LSB, with a range of 6.55 seconds;

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in RT mode, this register stores the current (or most previous) 1553 Command Word processed by the ACE RT; in the Word Monitor mode, this register specifies a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

Status Word Register and BIT Word Registers: Provides read-only indications of the BU-65549's RT Status and BIT Words.

Test Mode Registers 0-7: These registers may be used to facilitate self-testing of the BU-65549.

ACE SOFTWARE

The BU-65549 is supplied with software Runtime Libraries for Windows 9x/2000/XP, Windows NT and Linux. There is also GUI support with the ACE Menu under Windows 9x/2000/XP and Windows NT. This software is provided with the card at no extra cost.

ACE MENU OVERVIEW

The ACE Menu for Windows provides a Graphical User Interface (GUI) to the ACE series of board level products, such as the BU-65549. For the two-channel version of the card (BU-65549M2), each channel may be independently programmed to function in Bus Controller (BC), Remote Terminal (RT), Monitor Terminal (MT) mode. Each channel can only run in one mode at a time. Each mode has its own run screen.

The ACE Menu provides the necessary functionality for creating messages and assembling the messages into a frame for use by the BC function. The parameters for each message, including the command word, data words, and bus selection are modifiable from the ACE Menu. Setup screens are available for setting other operational parameters such as Response Timeout, Retries and Stop-On criteria. Adding these messages to a frame structure creates a BC frame. The ACE Menu allows a frame to be a composition of many minor frames, where each minor frame will represent the same amount of time, but is not restricted to having the same number of messages. The minor frame time is operator programmable. The number of minor frames times the minor frame time represents the Major Frame time. Once the frame is complete, the BC Run screen can be used to control the processing of the BC Frame. This screen displays operational status and provides controls for setting the minor frame time, the number of frames to send, and the communication stack setup. The Stack setup allows the user to set the name and size of the stack file where the 1553 bus traffic will be stored, and may be viewed at a later time.

Communication information is saved in stack files (*.asf). The run screens allow configuration of the stack file location and size. All run modes provide the stack view capability. After running the card, the generated stack file can be viewed by opening the stack viewer. Within each of the operating mode tool bars and menus, there is an open stack button that allows quick access to the stack file open dialog. Once opened, the stack file can be searched for any type of message or error. These stack files are compatible with the previous version stack files for both the Windows 9x/2000/XP, Windows NT and Windows 3.xx ACE Menu programs.

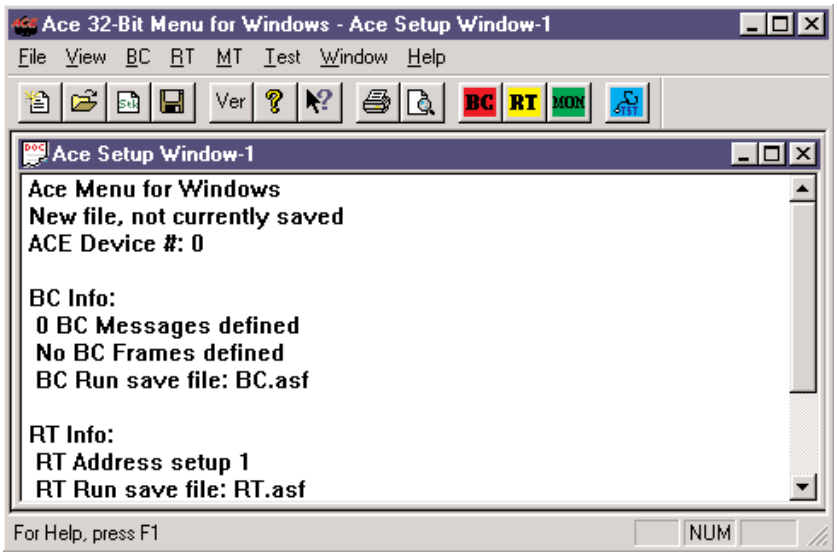


FIGURE 2. ACE SETUP WINDOW

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The Remote Terminal mode operation allows setting the hardware to respond to a specified RT address. The setup for a RT is much simpler than that of a BC. The bulk of the setup is used to specify the data that should be returned based on the sub-address set in the message command word. The data edit screen provides controls to select the sub-address and enter the data. Once all of the sub-address responses have been determined, the operation of the RT is controlled in the Setup screen. The controls available here are the RT Address, Remote Terminal to Remote Terminal timeout, and status word bits set. Finally, the RT Run screen will provide options for setting the Remote Terminal Address, and the Stack File.

Monitor operation is also provided. The ACE Menu monitor is a full message monitor that will monitor the 1553 bus traffic, decode the messages (command and data) and save the information to a Stack File. The monitor is capable of filtering the message information based on Remote Terminal address, Sub-address, and Transmit/Receive for each message. When all of the appropriate filtering has been established, the Response Timeout option may be set. The timeout option instructs the Monitor as to how long it must wait before declaring a no response message. The Run Monitor screen has controls that allow setting the Stack File requirements, and to provide access to the Monitor Trigger capabilities. The monitor is capable of triggering its capture based on any combination of the command word bits, or based on any of the error bits in the RT Status Word.

Finally, a Stack View capability is provided for each of the modes (BC, RT, and MT). From the Stack Button, a stack file can be selected, and viewed on the screen. Once the stack file is displayed, there is a capability of 'Finding' any message that was captured. The stack file contains information pertaining to the Storage Date, time and number of messages. It also contains the data portion of the messages, all pertinent status information, and text describing the error type.

The stack file can be searched by message command word, any data word, or any MIL-STD-1553 error. Each of the search criteria may be combined with a mask to allow searching for a family of command or data words. The search direction is selectable between up and down.

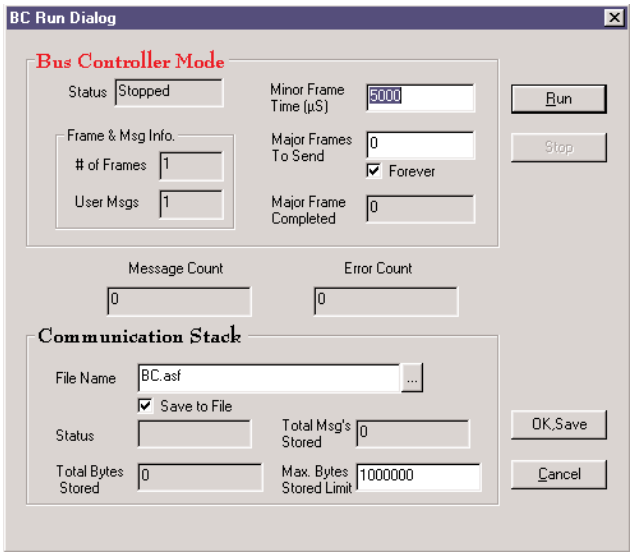


FIGURE 3. BC RUN DIALOG WINDOW

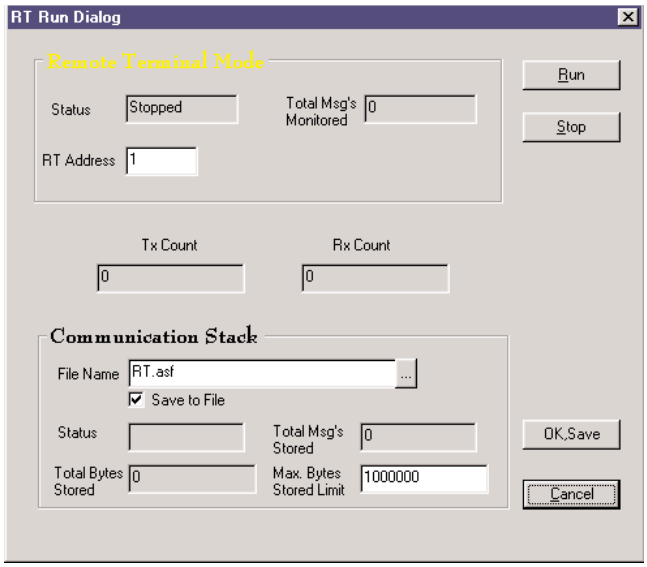


FIGURE 4. RT RUN DIALOG WINDOW

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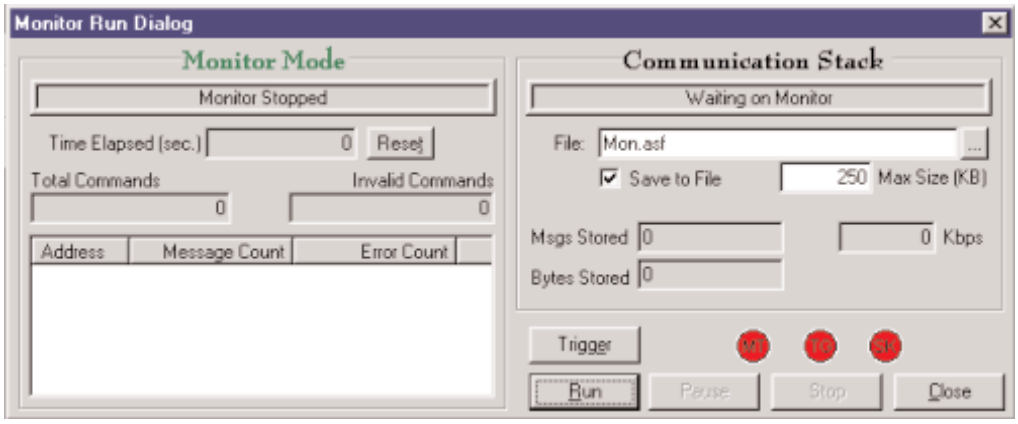


FIGURE 5. MONITOR MODE WINDOW

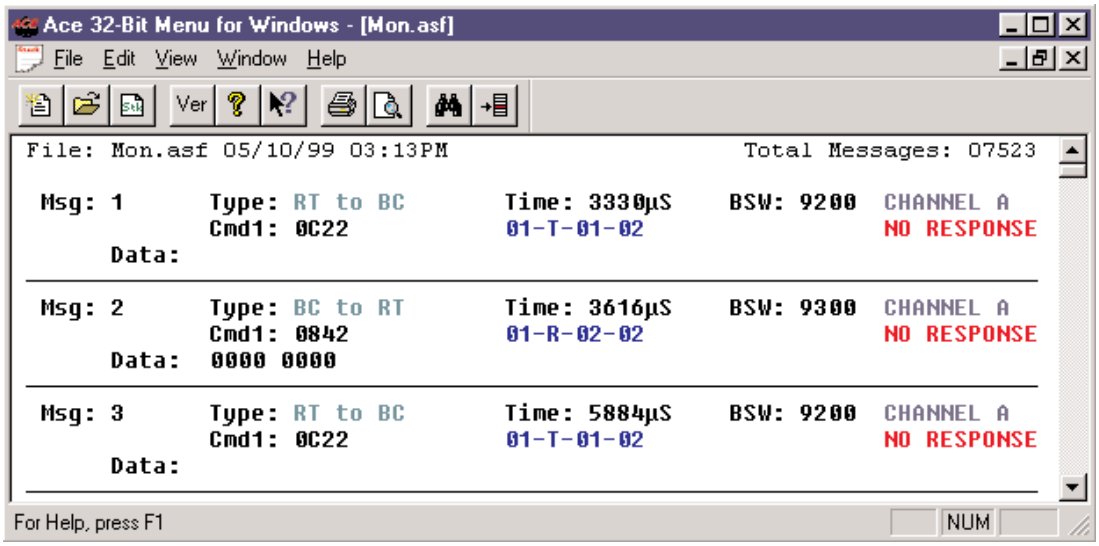


FIGURE 6. MONITOR MODE - STACK VIEW

ACE RUNTIME LIBRARIES

The Runtime Libraries for the BU-65549 come in a 32-bit version to support 32-bit Windows. Using the Runtime Library, applications may be created that are capable of controlling the card in either the BC, RT or MT mode. The newest version of this Runtime Library supports C and Visual Basic programming. Included with the ACE Runtime Library are sample applications for Bus Controller, Remote Terminal, and Monitor mode control. There are also sample programs for self-test and loop back tests. The self-test program tests and reports any errors found with the major portions of the hardware including registers, RAM, interrupt generation, and the protocol unit. The loop back tests force the BU-65549 card to communicate with itself. This test verifies the protocol unit and the transceivers to a greater degree than is performed by the Selftst2 program. The source for all of the test and sample programs is provided free of charge. These source programs may be used as a starting point for custom applications.

The following source code represents the simplicity of writing code for the BU-65549 PCI card. This program sends 10 words of data to RT 1 sub-address 5 on channel ‘A’, followed by a 32 word transmit to RT 6 sub-address 1 on channel 'A'. It then receives 5 words from RT 8 sub-address 4 on channel 'A', followed by a 32 word receive from RT 7 sub-address 2 on channel 'A'. Note that the creation of a 32-word message requires only that the data be defined in a buffer, and then a single function call to BuSendData(…) be made. Similarly, to receive data from a RT, a buffer must be defined, and a call to BuGetData(…) will be made. This encapsulated functionality relieves the application developer from having to know the details of the 1553 protocol hardware and registers.

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The following code is from the BCDEMO1.C sample program supplied with the BU-65549 hardware.

```
#include <stdio.h>
#include <stdlib.h>
#include <stdace.h>

void main ()
{
  BuConf_t  Conf; /* ACE library configuration type */
  BuError_t Err;  /* ACE library error status type  */

  U16BIT data[ 32] ={  0X0000,0x1111,0x2222,0x3333,0x4444,0x5555,0x6666,0x7777,
0x8888,0x9999,0xAAAA,0xBBBB,0xCCCC,0xDDDD,0xEEEE,0xFFFF,
0x0001,0x0002,0x0004,0x0008,0x0010,0x0020,0x0040,0x0080,
0x0100,0x0200,0x0400,0x0800,0x1000,0x2000,0x4000,0x8000} ;

  /* display revision info */
  printf("%s\n\n",BuRev());
  printf("\nThis BC Demo sets the Ace card in BC mode and sends a few messages.\n\n");

  /* setup configuration for device X and open ACE library */
  printf("Choose the logical device # of your BC:> ");
  scanf("%d",&Conf.ConfDev);

  Err=BuOpen32(&Conf);
  if(Err) {
          printf("BuError %d %s\n",Err,BuErrorStr(Err));
          return;
  }

  /* opens bus controller mode */
  BuBCOpen();

  /* send 10 words to rt 5 sa 1 on channel A */
  Err=BuBCSendData(CW_CHANNELA,5,1,data,10);
  printf("%s\n",BuErrorStr(Err));

  /* send 32 words to rt 6 sa 1 on channel A
     added this [ 01-SEP-1995]  to test 32 word case */
  Err=BuBCSendData(CW_CHANNELA,6,1,data,32);
  printf("%s\n",BuErrorStr(Err));

  /* receive 5 words from rt 8 sa 4 on channel A */
  Err=BuBCGetData(CW_CHANNELA,8,4,data,5);
  printf("%s\n",BuErrorStr(Err));

  /* display data */
  if(!Err){ int x;for(x=0;x<5;x++)printf("%04x ",data[ x] );printf("\n");}

  /* receive 32 words from rt 7 sa 2 on channel A
     added this [ 01-SEP-1995]  to test 32 word case */
  Err=BuBCGetData(CW_CHANNELA,7,2,data,32);
  printf("%s\n",BuErrorStr(Err));

  /* display data */
  if(!Err){ int x;for(x=0;x<32;x++)printf("%04x ",data[ x] );}

  /* closes bus controller mode */
  BuBCClose();

  /* must call at end of ACE library use */
  BuClose();

}
```


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TABLE 4. INTERRUPT MASK REGISTER (READ/WRITE 00H)	
BIT	**DESCRIPTION**
15 (MSB)	RESERVED
14	LOGIC "0"
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	RT MODE CODE/MT PATTERN TRIGGER
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	STATUS SET
0 (LSB)	END OF MESSAGE

TABLE 5. CONFIGURATION REGISTER #1 (READ/WRITE 01H)				
BIT	**BC FUNCTION (Enhanced Mode Only Bits 11-0)**	**RT WITHOUT ALTERNATE STATUS**	**RT WITH ALTERNATE STATUS (Enhanced Only)**	**MONITOR FUNCTION (Enhanced mode only bits 12-0)**
15 (MSB)	RT/$\overline{\text{BC-MT}}$ (logic 0)	(logic 1)	(logic 1)	(logic 0)
14	MT/$\overline{\text{BC-RT}}$ (logic 0)	(logic 0)	(logic 0)	(logic 1)
13	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/A	CURRENT AREA A/B	CURRENT AREA B/A
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)
11	FRAME STOP-ON-ERROR	$\overline{\text{DYNAMIC BUS CONTROL ACCEPTANCE}}$	S10	TRIGGER ENABLED WORD
10	STATUS SET STOP-ON-MESSAGE	$\overline{\text{BUSY}}$	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	$\overline{\text{SERVICE REQUEST}}$	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	$\overline{\text{SUBSYSTEM FLAG}}$	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	$\overline{\text{RTFLAG}}$ (Enhanced Mode Only)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	INTERMESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLED/$\overline{\text{SINGLE}}$ RETRY	NOT USED	S02	NOT USED
2	BC ENABLED	NOT USED	S01	MONITOR ENABLED(Read Only)
1	BC FRAME IN PROGRESS (Read Only)	NOT USED	S00	MONITOR TRIGGERED (Read Only)
0 (LSB)	BC MESSAGE IN PROGRESS (Read Only)	RT MESSAGE IN PROGRESS (Enhanced mode only, Read Only)	RT MESSAGE IN PROGRESS (Read Only)	MONITOR ACTIVE (Read Only)

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TABLE 6. CONFIGURATION REGISTER #2 (READ/WRITE 02H)	
BIT	**DESCRIPTION**
15 (MSB)	ENHANCED INTERRUPTS
14	LOGIC “0”
13	BUSY LOOKUP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDARY DISABLE
9	TIME TAG RESOLUTION 2(TTR2)
8	TIME TAG RESOLUTION 1 (TTR1)
7	TIME TAG RESOLUTION 0 (TTR0)
6	CLEAR TIME TAG ON SYNCHRONIZE
5	LOAD TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/$\overline{\text{PULSE}}$ INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST
1	ENHANCED RT MEMORY MANAGEMENT
0 (LSB)	SEPARATE BROADCAST DATA

TABLE 7. START/RESET REGISTER (WRITE 03H)	
BIT	**DESCRIPTION**
15 (MSB)	RESERVED
•	•
•	•
•	•
7	RESERVED
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0 (LSB)	RESET

TABLE 8. BC/RT COMMAND STACK POINTER REG. (READ 03H)	
BIT	**DESCRIPTION**
15 (MSB)	COMMAND STACK POINTER 15
•	•
•	•
•	•
0 (LSB)	COMMAND STACK POINTER 0

TABLE 9. BC CONTROL WORD REGISTER (READ/WRITE 04H)	
BIT	**DESCRIPTION**
15 (MSB)	RESERVED
14	M.E. MASK
13	SERVICE REQUEST BIT MASK
12	SUBSYS BUSY BIT MASK
11	SUBSYS FLAG BIT MASK
10	TERMINAL FLAG BIT MASK
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/$\overline{\text{B}}$
6	OFF LINE SELF TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0 (LSB)	RT-RT FORMAT

TABLE 10. RT SUBADDRESS CONTROL WORD REGISTER (READ/WRITE 04H)	
BIT	**DESCRIPTION**
15 (MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0 (LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

TABLE 11. TIME TAG REGISTER (READ/WRITE 05H)	
BIT	**DESCRIPTION**
15 (MSB)	TIME TAG 15
•	•
•	•
•	•
0 (LSB)	TIME TAG 0

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TABLE 12. INTERRUPT STATUS REGISTER (READ/WRITE 06H)

BIT	DESCRIPTION
15 (MSB)	MASTER INTERRUPT
14	RESERVED
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	RT MODE/MT PATTERN TRIGGER
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	STATUS SET
0 (LSB)	END OF MESSAGE

TABLE 13. CONFIGURATION REGISTER #3 (READ/WRITE 07H)

BIT	DESCRIPTION
15 (MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/$\overline{R}$ ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER DISABLE
2	FAIL-FLAG WRAP ENABLE
1	1553A MODE CODES ENABLE
0 (LSB)	ENHANCED MODE CODE HANDLING

TABLE 14. CONFIGURATION REGISTER #4 (READ/WRITE 08H)

BIT	DESCRIPTION
15 (MSB)	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BROADCAST MASK ENABLE/$\overline{XOR}$
10	RETRY IF -A AND M.E.
9	RETRY IF STATUS SET
8	1ST RETRY ALT/$\overline{SAME}$ BUS
7	2ND RETRY ALT/$\overline{SAME}$ BUS
6	VALID M.E./NO DATA
5	VALID BUSY/NO DATA
4	MT TAG GAP OPTION
3	LATCH RT ADDRESS WITH CONFIG #5
2	TEST MODE 2
1	TEST MODE 1
0 (LSB)	TEST MODE 0

TABLE 15. CONFIGURATION REGISTER #5 (READ/WRITE 09H)

BIT	DESCRIPTION
15 (MSB)	12MHZ CLOCK SELECT
14	LOGIC “0”
13	EXTERNAL TX INHIBIT A, read only
12	EXTERNAL TX INHIBIT B, read only
11	EXPANDED CROSSING ENABLE
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	LOGIC “1”
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0 (LSB)	RT ADDRESS PARITY

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TABLE 16. MONITOR DATA STACK ADDRESS REGISTER (READ/WRITE 0AH)	
BIT	**DESCRIPTION**
15 (MSB)	MONITOR DATA STACK ADDRESS 15
•	•
•	•
•	•
0 (LSB)	MONITOR DATA STACK ADDRESS 0

TABLE 17. BC FRAME TIME REMAINING REGISTER (READ/WRITE 0BH)	
BIT	**DESCRIPTION**
15 (MSB)	BC FRAME TIME REMAINING 15
•	•
•	•
•	•
0 (LSB)	BC FRAME TIME REMAINING 0
Note: resolution = 100 µs per LSB	

TABLE 18. BC MESSAGE TIME REMAINING REGISTER (READ/WRITE 0CH)	
BIT	**DESCRIPTION**
15 (MSB)	BC MESSAGE TIME REMAINING 15
•	•
•	•
•	•
0 (LSB)	BC MESSAGE TIME REMAINING 0
Note: resolution = 1 µs per LSB	

TABLE 19. BC FRAME TIME/RT LAST COMMAND/MT TRIGGER REGISTER (READ/WRITE 0DH)	
BIT	**DESCRIPTION**
15 (MSB)	BIT 15
•	•
•	•
•	•
0 (LSB)	BIT 0

TABLE 20. RT STATUS REGISTER (READ 0EH)	
BIT	**DESCRIPTION**
15 (MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPT
0 (LSB)	TERMINAL FLAG

TABLE 21. RT BIT WORD REGISTER (READ 0FH)	
BIT	**DESCRIPTION**
15 (MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	CHANNEL B/$\overline{A}$
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNCH/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0 (LSB)	COMMAND WORD CONTENTS ERROR

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TABLES 22 TO 25 ARE NOT REGISTERS, BUT THEY ARE WORDS STORED IN RAM:

TABLE 22. BC MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15 (MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0 (LSB)	INVALID WORD

TABLE 23. RT MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15 (MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0 (LSB)	COMMAND WORD CONTENTS ERROR

TABLE 24. WORD MONITOR IDENTIFICATION WORD

BIT	DESCRIPTION
15 (MSB)	GAP TIME (MSB)
•	•
•	•
•	•
8	GAP TIME (LSB)
7	WORD FLAG
6	$\overline{\text{THIS RT}}$
5	$\overline{\text{BROADCAST}}$
4	ERROR
3	COMMAND/$\overline{\text{DATA}}$
2	CHANNEL B/$\overline{A}$
1	CONTIGUOUS DATA/$\overline{\text{GAP}}$
0 (LSB)	$\overline{\text{MODE CODE}}$

TABLE 25. MESSAGE MONITOR MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15 (MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0 (LSB)	COMMAND WORD CONTENTS ERROR

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BUS CONTROLLER (BC) ARCHITECTURE

The BC protocol of the BU-65549 implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of bits in the BC Control Word and the T/$\overline{R}$ bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The BU-65549's BC response timeout value is programmable with choices of 18, 22, 50, and 130 µs. The longer response timeout values allow for operation over long buses and/or the use of repeaters.

FIGURE 7 illustrates BC intermessage gap and frame timing. The BU-65549 may be programmed to process BC frames of up to 512 messages with no processor intervention. It is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled using a programmable BC frame timer. The internal BC frame time is programmable up to 6.55 seconds in increments of 100 µs. In addition to BC frame time, message gap time, defined as the start of the current message to the start of the subsequent message, is programmable on an individual message basis. The time between individual successive messages is programmable up to 65.5 ms, in increments of 1 µs.

BC MEMORY ORGANIZATION

TABLE 26 illustrates a typical memory map for BC mode. It is important to note that the only fixed locations for the BU-65549 in the Standard (non-frame Auto-Repeat) BC mode are for the two Stack Pointers (address locations 0100 (hex) and 0104) and for the two Message Count locations (0101 and 0105). Enabling the Frame Auto-Repeat mode will reserve four more memory locations for use in the Enhanced BC mode; these locations are for the two Initial Stack Pointers (address locations 102 (hex)

TABLE 26. TYPICAL BC MEMORY ORGANIZATION (SHOWN FOR 64K RAM)

ADDRESS (note 2)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101	Message Count A (fixed location)
0102	Initial Stack Pointer A (see note 1) (Auto-Frame Repeat Mode)
0103	Initial Message Count A (see note 1) (Auto-Frame Repeat Mode)
0104	Stack Pointer B
0105	Message Count B
0106	Initial Stack Pointer B (see note 1) (Auto-Frame Repeat Mode)
0107	Initial Message Count B (see note 1) (Auto-Frame Repeat Mode)
0108-012D	Message Block 0
012E-0153	Message Block 1
0154-0179	Message Block 2
•	•
•	•
•	•
238-25D	Message Block 8
25E-25F	Not Used
260-27F	Registers
280-2A5	Message Block 9
2A6-2CB	Message Block 10
2CC-2F2	Message Block 11
•	•
•	•
•	•
FED8-FEFD	Message Block 1709
FEFE-FEFF	Not Used
FF00-FFFF	Stack B

Notes:
1. Used only in the Enhanced BC mode with Frame Auto-Repeat enabled.
2. Address represents the word offset from the memory base address in the shared RAM address space.

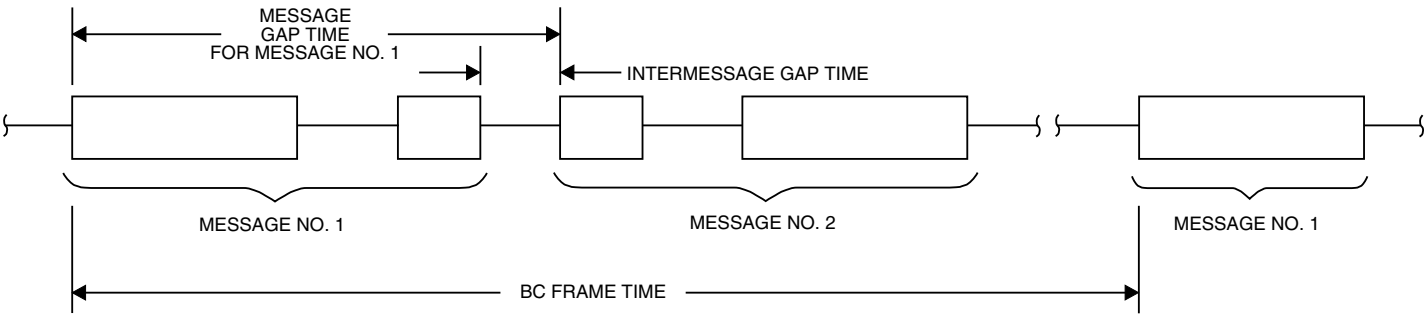


FIGURE 7. BC MESSAGE GAP AND FRAME TIMING

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and 106) and for the Initial Message Count locations (103 and 107). The user is free to locate the Stack and BC Message Blocks anywhere else within the 64K shared RAM address space.

For simplicity of illustration, assume the allocation of the maximum length of a BC message for each message block in the typical BC memory map of TABLE 26. The maximum size of a BC message block is 38 words, for an RT-to-RT transfer of 32 Data Words (Control + 2 Commands + Loopback + 2 Status Words + 32 Data Words).

Note, however, that this example assumes the disabling of the 256-word boundaries.

BC MEMORY MANAGEMENT

FIGURE 8 illustrates the BU-65549's BC memory management scheme. One of the BC memory management features is the global double buffering mechanism. This provides for two sets of the various BC mode data structures: the Stack Pointer and Message Counter locations, Descriptor Stack areas, and BC message blocks. Bit 13 of Configuration Register #1 selects the current active area. At any point in time, the BU-65549's internal 1553 memory management logic may access only the various data structures within the "active" area; it will not change to the alternate area until a restart occurs. FIGURE 8 delineates the "active" and "inactive" areas by the nonshaded and shaded areas, respectively; however, at any point in time, **both the "active" and "nonactive" areas are accessible by the host processor**. In many applications, the host processor will access the "nonactive" area, while the 1553 bus processes the "active" area messages.

The BC may be programmed to transmit multimessage frames of up to 512 messages. The number of messages to be processed is programmable by the Active Area Message Count location in the shared RAM, initialized by the host processor. In addition, the host processor must initialize another location, the Active Area Stack Pointer. The Stack Pointer references the four-word message block descriptor in the Stack area of shared RAM for each message to be processed. The BC Stack size is programmable with choices of 256, 512, 1024, and 2048 words.

In the BC Frame Auto-Repeat mode, the Initial Stack Pointer and Initial Message Counter locations must be loaded by the host prior to the processing of the first frame. The single frame mode does not use these two locations.

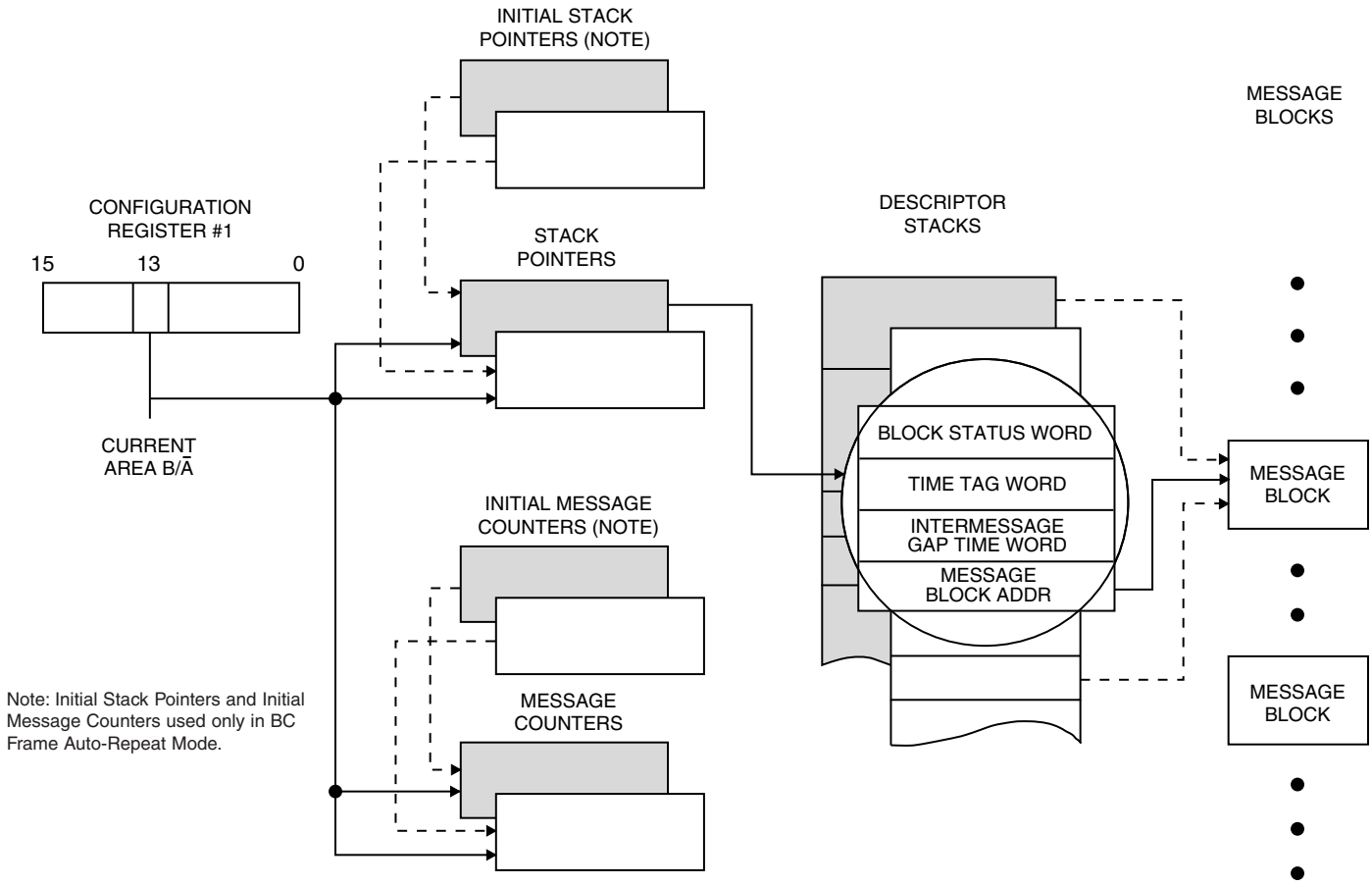


FIGURE 8. BC MODE MEMORY MANAGEMENT

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The third and fourth words of the BC block descriptor are the Intermessage Gap Time and the Message Block Address for the respective message. These two memory locations must be written by the host processor prior to the start of message processing. Use of the Intermessage Gap Time is optional. The Block Address pointer specifies the starting location for each message block. The first word of each BC message block is the BC Control Word.

At the start and end of each message, the Block Status and Time Tag Words write to the message block descriptor in the stack. The Block Status Word includes indications of message in process or message completion, bus channel, Status Set, response timeout, retry count, Status address mismatch, loop test (on-line self-test) failure, and other error conditions. TABLE 22 illustrates the bit mapping of the BC Block Status word. The 16-bit Time Tag Word will reflect the current contents of the internal Time Tag Register. This read/writable register, which operates for all three modes, has programmable resolution of from 2 to 64 µs/LSB.

BC MESSAGE BLOCK FORMATS AND BC CONTROL WORD

In BC mode, the BU-65549 supports all MIL-STD-1553 message formats. For each 1553 message format, the BU-65549 mandates a specific sequence of words within the BC Message Block. This includes locations for the Control, Command and (transmitted) Data Words that are to be read from RAM by the BC protocol logic. In addition, subsequent contiguous locations must be allocated for storage of received Loopback, RT Status and Data Words. FIGURE 9 illustrates the organization of the BC message blocks for the various MIL-STD-1553 message formats.

Note that for all of the message formats, the BC Control Word is located in the first location of the message block.

For each of the BC Message Block formats, the first word in the block is the BC Control Word. The BC Control Word is not transmitted on the 1553 bus. Instead, it contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. The bit mapping and definitions of the BC Control Word are illustrated in TABLE 9.

The BC Control Word is followed by the Command Word to be transmitted, and subsequently by a second Command Word (for an RT-to-RT transfer), followed by Data Words to be transmitted (for Receive commands). The location after the last word to be transmitted is reserved for the Loopback Word. The Loopback Word is an on-line self-test feature. The subsequent locations

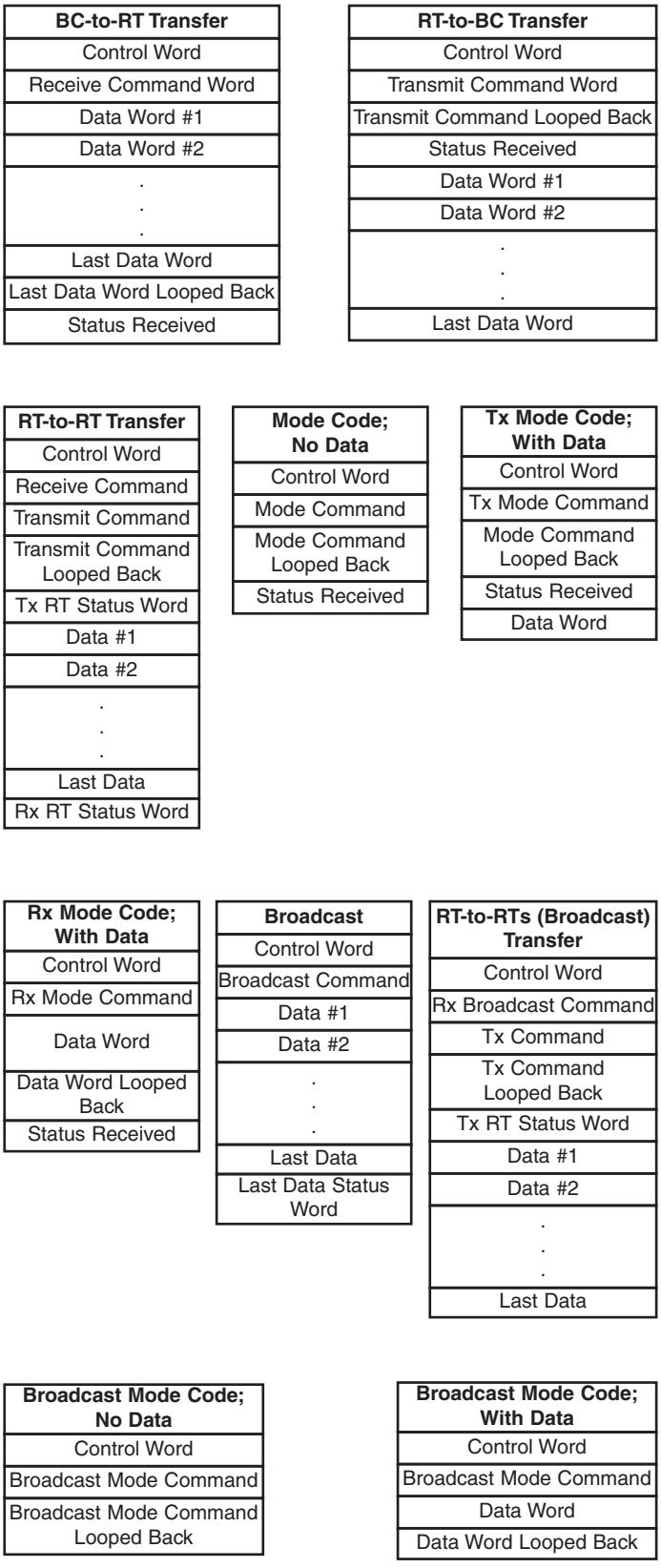


FIGURE 9. BC MESSAGE BLOCK FORMATS

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after the Loopback Word are reserved for received Status Words and Data Words (for Transmit commands).

AUTOMATIC RETRIES

The BU-65549 BC can be set to implement automatic message retries. When enabled, retries will occur, following response timeout or format error conditions. As additional options, retries may be enabled when the Message Error Status Word bit is set by a 1553A RT or following a “Status Set” condition. For a failed message, either one or two message retries will occur, and the bus channel (same or alternate) is independently programmable for the first and second retry attempts. Retries may be enabled or disabled on an individual message basis.

BC INTERRUPTS

BC interrupts may be enabled by the Interrupt Mask Register for Stack Rollover, Retry, End-of-Message (global), End-of-Message (in conjunction with the BC Control Word for individual messages), response timeout, message error, end of BC frame, and Status Set conditions. The definition of “Status Set” is programmable on an individual message basis by means of the BC Control Word. This allows for masking (“care/don't care”) for the individual RT Status Word bits received.

REMOTE TERMINAL (RT) ARCHITECTURE

The RT protocol design of the BU-65549 represents DDC's fifth generation implementation of a 1553 RT. One of the salient features of the ACE's RT architecture is its true multiprotocol functionality. This includes programmable options for support of MIL-STD-1553A, the various McAir protocols, and MIL-STD-1553B Notice 2. The BU-65549 RT response time is 2 to 5 µs dead time (4 to 7 µs per 1553B), providing compliance to all the 1553 protocols. Additional multiprotocol features of the BU-65549 include options for full software control of RT Status and Built-in-Test (BIT) words. Alternatively, for 1553B applications, these words may be formulated in real time by the BU-65549 protocol logic.

The BU-65549 RT protocol design implements all the MIL-STD-1553B message formats and dual redundant mode codes. This design is based largely on previous generation products that have passed SEAFAC testing for MIL-STD-1553B compliance. The ACE RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. Other key features of the BU-65549 RT include a set of interrupt conditions, internal command illegalization, and programmable busy by subaddress.

RT MEMORY ORGANIZATION

TABLE 27 illustrates a typical memory map for the BUS-65549 in RT mode. As in BC mode, the two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. Besides the Stack Pointer, for RT mode there are several other areas of the ACE address space designated as fixed locations. All RT modes of operation require the Area A (and may use Area B) Lookup Tables. Also allocated, are several fixed locations for optional features: Command Illegalization Lookup Table, Mode Code Selective Interrupt Table, Mode Code Data Table, and Busy Bit Lookup Table. It should be noted that any unenabled optional fixed locations may be used for general purpose storage (data blocks).

TABLE 27. TYPICAL RT MEMORY MAP (SHOWN FOR 64K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101-0103	RESERVED
0104	Stack Pointer B (fixed location)
0105-0107	RESERVED
0108-010F	Mode Code Selective Interrupt Table (fixed area)
0110-013F	Mode Code Data (fixed area)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-0247	Busy Bit Lookup Table (fixed area)
0248-025F	(not used)
0260-027F	Registers
0280-02FF	Data Block 0-3
0300-03FF	Command Illegalizing Table (fixed area)
0400-041F	Data Block 4
0420-043F	Data Block 5
•	•
•	•
•	•
2FE0-2FFF	Data Block 255
3000-FFFF	Approximately 1600 more data blocks(or monitor stacks)

Notes:
1. Address represents the word offset from the memory base address in the shared RAM address space.

The RT Lookup tables, which provide a mechanism for mapping data blocks for individual Tx/Rx/Bcst-subaddresses to areas in the RAM, occupy address range locations are 0140 to 01BF for Area A (and 01C0 to 023F for Area B). The RT lookup tables include Subaddress Control Words and the individual Data Block Pointers. If used, address range 0300-03FF will be dedicated as the illegalizing section of RAM. The actual Stack RAM area and the individual data blocks may be located in any of the nonfixed areas in the shared RAM address space.

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TABLE 28. RT LOOK-UP TABLES

AREA A	AREA B	DESCRIPTION	COMMENT
0140 . . . 015F	01C0 . . . 01DF	Rx(/Bcst)_SA0 . . . Rx(/Bcst)_SA31	Receive (/Broadcast) Lookup Table
0160 . . . 017F	01E0 . . . 01FF	Tx_SA0 . . . Tx_SA31	Transmit Lookup Table
0180 . . . 019F	0200 . . . 021F	Bcst_SA0 . . . Bcst_SA31	Broadcast Lookup Table (Optional)
01A0 . . . 01BF	0220 . . . 023F	SACW_SA0 . . . SACW_SA31	Subaddress Control Word Lookup Table (Optional)

Note: Address represents the word offset from the memory base address in the common memory address space.

TABLE 29. SUBADDRESS CONTROL WORD MEMORY MANAGEMENT SUBADDRESS BUFFER SCHEME

MM2	MM1	MM0	DESCRIPTION	COMMENT
0	0	0	Single Message or Double Buffered	
0	0	1	128-Word	Circular Buffer of Specified Size
0	1	0	256-Word	
0	1	1	512-Word	
1	0	0	1024-Word	
1	0	1	2048-Word	
1	1	0	4096-Word	
1	1	1	8192-Word	

RT MEMORY MANAGEMENT

One of the salient features of the ACE series products is the flexibility of its RT memory management architecture. The RT architecture allows the memory management scheme for each transmit, receive, or broadcast subaddress to be programmable on a subaddress basis. Also, in compliance with MIL-STD-1553B Notice 2, the BU-65549 provides an option to separate data received from broadcast messages from non-broadcast received data.

Besides supporting a global double buffering scheme (as in BC mode), the ACE RT provides a pair of 128-word Lookup Tables for memory management control, programmable on a subaddress basis (refer to TABLE 28). The 128-word tables include 32-word tables for transmit message pointers and receive message pointers. There is also a third, optional Lookup Table for broadcast message pointers, providing Notice 2 compliance, if necessary. For most applications, the subaddress tables provide more flexible buffering than the global scheme and current Area B tables are not used.

The fourth section of each of the RT Lookup Tables stores the 32 Subaddress Control Words (refer to TABLE 10 and TABLE 29). The individual Subaddress Control Words may be used to select the RT memory management option and interrupt scheme for each transmit, receive, and (optionally) broadcast subaddress.

For each transmit subaddress, there are two possible memory management schemes: (1) single message; and (2) circular buffer. The use of a single buffer type is recommended for transmitting messages. For each receive (and optionally broadcast) subaddress, there are three possible memory management schemes: (1) single message; (2) double buffered; and (3) circular buffer. For each transmit, receive and broadcast subaddress, there are two interrupt conditions programmable by the respective Subaddress Control Word: (1) after every message to the subaddress; (2) after a circular buffer rollover. An additional table in RAM may be used to enable interrupts following selected mode code messages.

When using the circular buffer scheme for a given subaddress, the size of the circular buffer is programmable by three bits of the Subaddress Control Word (see TABLE 29). The options for circular buffer size are 128, 256, 512, 1024, 2048, 4096, and 8192 Data Words.

SINGLE MESSAGE MODE

FIGURE 10 illustrates the RT Single Message memory management scheme. When operating the BU-65549 in its default configuration, the Single Message scheme is implemented for all transmit, receive, and broadcast subaddresses. In the Single Message mode (also in the Double Buffer and Circular Buffer modes), there is a global double buffering scheme, controlled by bit 13 of Configuration Register #1. This selects from between the two sets of the various data structures shown in the figure: the Stack Pointers (fixed addresses), Descriptor Stacks (user defined addresses), RT Lookup Tables (fixed addresses), and RT data word blocks (user defined addresses). FIGURES 10, 11, and 12 delineate the “active” and “nonactive” areas by the non-shaded and shaded areas, respectively.

As shown, the ACE stores the Command Word from each message received in the fourth location within the message descriptor (in the stack) for the respective message. The T/$\overline{R}$ bit, subaddress field, and (optionally) broadcast/own address, index into the active area Lookup Table, to locate the data block pointer for the current message. The BU-65549 RT memory management logic then accesses the data block pointer to locate the starting address for the Data Word block for the current message. The maximum size for an RT Data Word block is 32 words.

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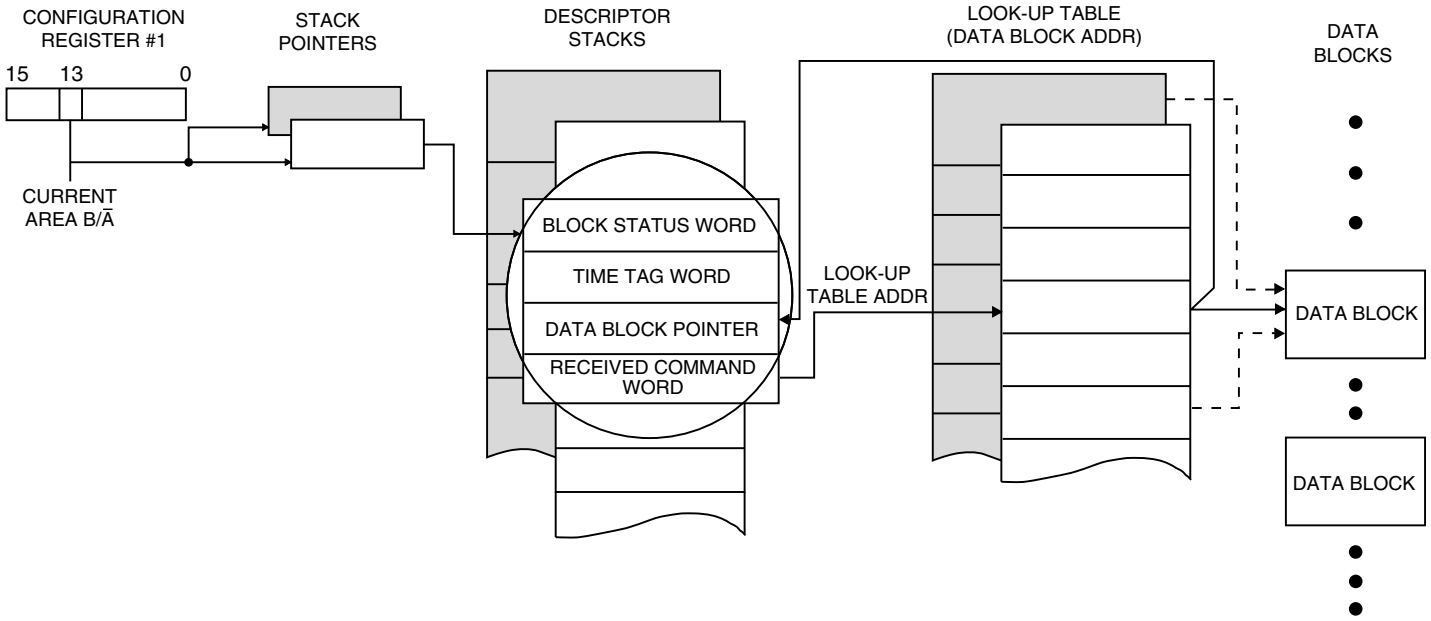


FIGURE 10. RT MEMORY MANAGEMENT : SINGLE MESSAGE MODE

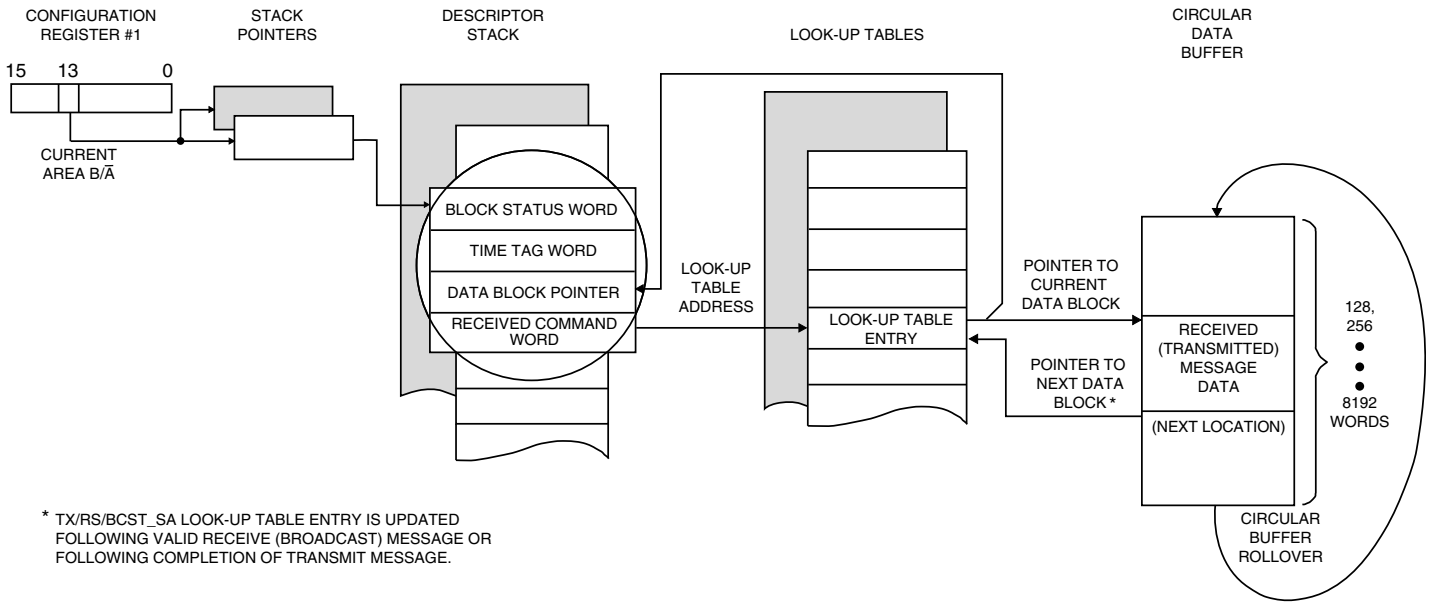


FIGURE 11. RT MEMORY MANAGEMENT : CIRCULAR BUFFER MODE

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To implement a data wraparound subaddress, as required by Notice 2 of MIL-STD-1553B, the Single Message scheme should be used to define the transmit and receive pointer for the wrap-around subaddress to the same data block. Notice 2 recommends subaddress 30 as the wraparound subaddress.

CIRCULAR BUFFER MODE

FIGURE 11 illustrates the RT circular buffer memory management scheme. The circular buffer mode facilitates bulk data transfers. The size of the RT circular buffer, shown on the right side of the figure, is programmable from 128 to 8192 words (in even powers of 2) by the respective Subaddress Control Word. As in the single message mode, the host processor initially loads the individual Lookup Table entries. At the start of each message, the ACE stores the Lookup Table entry in the third position of the respective message block descriptor in the stack area of RAM, as in the Single Message mode. The ACE transfers Receive or Transmit Data Words to (from) the circular buffer, starting at the location referenced by the Lookup Table pointer.

At the end of a valid (or, optionally, invalid) message, the value of the Lookup Table entry updates to the next location after the last address accessed for the current message. As a result, Data Words for the next message directed to the same Tx/Rx(/Bcst) subaddress will be accessed at the next contiguous block of address locations within the circular buffer. As a recommended option, the Lookup Table pointers may be programmed to not update following an invalid receive (or broadcast) message. This allows the 1553 bus controller to retry the failed message, resulting in the valid (retried) data overwriting the invalid data. This eliminates overhead for the PC host processor. When the pointer reaches the lower boundary of the circular buffer (located at 128, 256, . . . 8192-word boundaries in the BU-65549 address space), the pointer moves to the top boundary of the circular buffer, as FIGURE 11 shows.

SUBADDRESS DOUBLE BUFFERING MODE

For receive (and broadcast) subaddresses, the BU-65549 RT offers a third memory management option, Subaddress Double Buffering. Subaddress double buffering provides a means of ensuring data consistency. FIGURE 12 illustrates the RT Subaddress Double Buffering scheme. Like the Single Message and Circular Buffer modes, the Double Buffering mode may be selected on a subaddress basis by means of the Subaddress Control Word. The purpose of the Double Buffering mode is to provide the host processor with a convenient means of accessing the most recent, valid data received to a given subaddress. This serves to ensure the highest possible degree of data sample consistency by allocating two 32-bit Data Word blocks for each individual receive (and/or broadcast) subaddress.

At a given point in time, one of the two blocks will be designated as the “active” 1553 data block while the other will be designated as the “inactive” block. The Data Words from the next receive message to that subaddress will be stored in the “active” block. Upon completion of the message, provided that the message was valid and Subaddress Double Buffering is enabled, the BU-65549 will automatically switch the “active” and “inactive” blocks-for the respective subaddress. The ACE accomplishes this by toggling bit 5 of the subaddress's Lookup Table Pointer and rewriting the pointer. As a result, the most recent valid block of received Data Words will always be readily accessible to the host processor.

As a means of ensuring data sample consistency, the host processor is able to reliably access the most recent valid, received Data Word block by performing the following sequence:

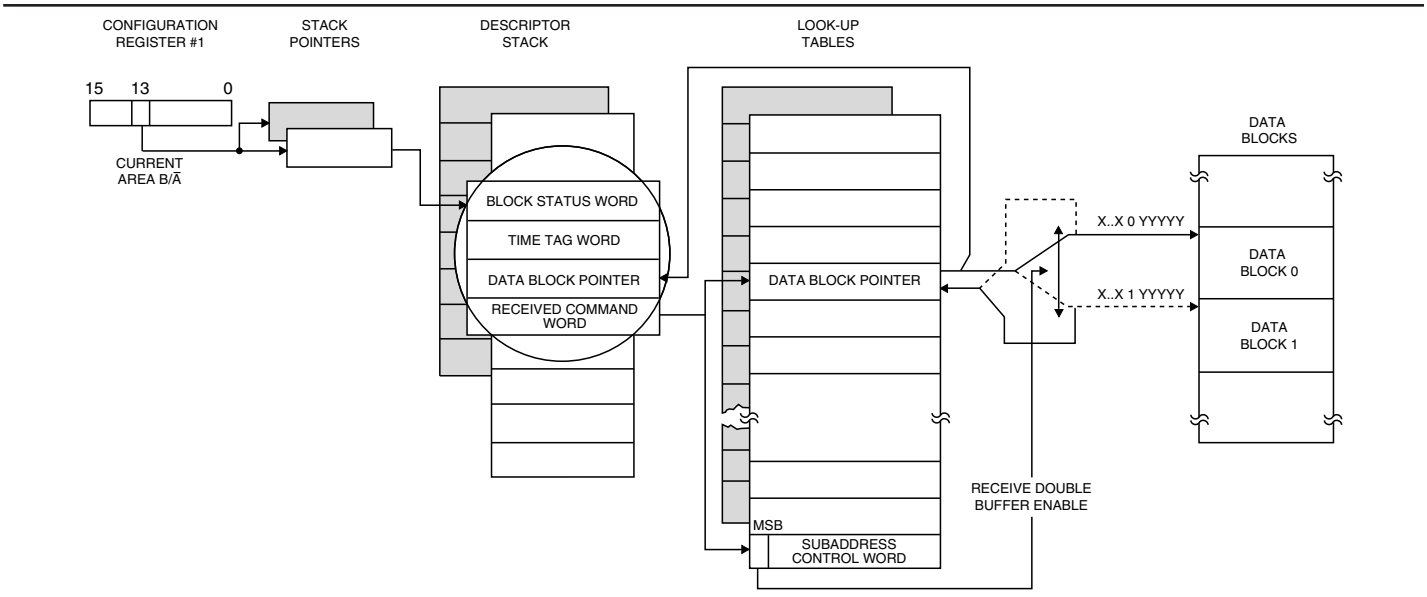


FIGURE 12. RT MEMORY MANAGEMENT : SUBADDRESS DOUBLE BUFFERING MODE

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(1) Disable the double buffering for the respective subaddress by the Subaddress Control Word. That is, temporarily switch the subaddress's memory management scheme to the Single Message mode.

(2) Read the current value of the receive (or broadcast) subaddress's Lookup Table pointer. This points to the current "active" data word block. By inverting bit 5 of this pointer value, it is possible to locate the start of the "inactive" data word block. This block will contain the data words received during the most recent valid message to the subaddress.

(3) Read out the words from the "inactive" (most recent) Data Word Block.

(4) Re-enable the Double Buffering mode for the respective subaddress by the Subaddress Control Word.

RT INTERRUPTS

As in BC mode, the BU-65549 RT provides a number of maskable interrupt conditions. RT interrupt conditions include End of (every) Message, Message Error, Selected Subaddress (Subaddress Control Word) Interrupt, Circular Buffer Rollover, Selected Mode Code Interrupt, and Descriptor Stack Rollover.

DESCRIPTOR STACK

At the beginning and end of each message, the BU-65549 RT updates a 4-word message descriptor in the active area stack. The RT stack size is programmable, with choices of 256, 512, 1024, and 2048 words. FIGURES 10, 11, and 12 show the four words: Block Status Word, Time Tag Word, Data Block Pointer, and the 1553 received Command Word. The RT Block Status Word includes indications of message in-progress or message complete, bus channel, RT-to-RT transfer and RT-to-RT transfer errors, message format error, loop test (self-test) failure, circular buffer rollover, illegal command, and other error conditions. TABLE 23 shows the bit mapping of the RT Block Status Word.

As in BC mode, the Time Tag Word stores the current contents of the BU-65549's read/writable Time Tag Register. The resolution of the Time Tag Register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. Also, incrementing of the Time Tag counter may be from an external clock source or via software command. For the BU-65549M2 card, there are separate, and independent time tag registers for the two bus channels.

The ACE stores the contents of the accessed lookup table location for the current message, indicating the starting location of the data word block, as the data block pointer. This serves as a convenience in locating stored message data blocks. The third word will contain the data block pointer, or optionally mode code data. The ACE stores the full 16-bit 1553 Command Word in the fourth location of the RT message descriptor.

RT COMMAND ILLEGALIZATION

The BU-65549 provides an internal mechanism for RT command illegalization (setting of the Message Error bit in the status response). In addition, there is a means for allowing the setting of the Busy Status Word bit to be only for a programmed subset of the transmit/receive/broadcast subaddresses.

The illegalization scheme uses a 256-word area in the BU-65549's address space. The BU-65549's illegalization scheme provides maximum flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/$\overline{R}$ bit, subaddress, and word count/mode code to be illegalized.

PROGRAMMABLE BUSY

The BU-65549 RT provides a software controllable means for setting the busy status word bit as a function of subaddress. By means of a Busy lookup table in the BU-65549 address space, it is possible to set the Busy bit based on command broadcast/own address, T/$\overline{R}$ bit, and subaddress. Another programmable option allows received Data Words to be either stored or not stored for receive messages when the Busy bit is set.

OTHER RT FUNCTIONS

The BU-65549 allows each channel's programmed RT Address to be read by the host processor. Also, there are options for the RT FLAG Status Word bit to be set under software control and/or automatically following a failure of the loopback self-test. Other software controllable RT options include software programmable RT Status and RT BIT words, automatic clearing of the Service Request Status Word bit following a Transmit Vector Word mode command, capabilities to clear and/or load the Time Tag Register following receipt of Synchronize mode commands, options regarding Data Word transfers for the Busy and/or Message Error (Illegal) Status Word bits, and for handling of 1553A and reserved mode codes.

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MONITOR (MT) ARCHITECTURE

The BU-65549 provides three bus monitor (MT) modes:

(1) A Word Monitor mode.

(2) A Selective Message Monitor mode.

(3) A Simultaneous RT / Selective Message Monitor mode.

The strong recommendation for new applications is the use of the Selective Message Monitor, rather than the Word Monitor. Besides providing monitor filtering based on RT Address, T/$\overline{R}$ bit, and Subaddress, the Message Monitor eliminates the need to determine the start and end of messages by software. Such software tends to entail a high degree of CPU overhead.

WORD MONITOR

In the Word Monitor mode, the BU-65549 monitors both 1553 buses. After initializing the Word Monitor and putting it online the BU-65549 stores all Command, Status, and Data Words received from both buses. For each word received from either bus, the BU-65549 stores a pair of words in RAM. The first word is the 16 bits of data from the received word. The second word is the Monitor Identification (ID), or "Tag" word. The ID Word contains information relating to bus channel, sync type, word validity, and inter-word time gaps. The BU-65549 stores data and ID words in a circular buffer in the shared RAM address space. TABLE 24 shows the bit mapping for the Monitor ID word. The starting location for storage should be loaded to location 0100h. Subsequently, this value is overwritten as the monitor fills the available RAM and rolls over to 0000h.

MONITOR TRIGGER WORD

There is a Trigger Word Register that provides additional flexibility for the Word Monitor mode. The BU-65549 stores the value of the 16-bit Trigger Word in the MT Trigger Word Register. The contents of this register represent the value of the Trigger Command Word. The BU-65549 has programmable options to start or stop the Word Monitor, and/or to issue an interrupt request following receipt of the Trigger command word from the 1553 bus.

SELECTIVE MESSAGE MONITOR MODE

The BU-65549 Selective Message Monitor provides features to greatly reduce the software and processing burden of the host CPU. The Selective Message Monitor implements monitoring of messages from a dual 1553 bus, with the monitor filtering based on the RT Address, T/$\overline{R}$ bit, and subaddress fields of received 1553 command words. The Selective Message Monitor mode greatly simplifies the host processor software by distinguishing between command and status words. The Selective Message Monitor maintains two stacks in the BU-65549 RAM: a Command Stack and a Data Stack.

SIMULTANEOUS RT/MESSAGE MONITOR MODE

The Selective Message Monitor may function as a purely passive monitor or may be programmed to function as a simultaneous RT/Monitor. The RT/Monitor mode provides complete Remote Terminal (RT) operation for the BU-65549's programmed RT address, and bus monitor capability for the other 30 non-broadcast RT addresses. This allows the BU-65549 to simultaneously operate as a full function RT and "snoop" on all or a subset of the bus activity involving the other RTs on a bus. This type of operation is sometimes needed to implement a backup bus controller. The combined RT/Selective Monitor maintains three stack areas in the BU-65549 address space: an RT Command Stack, a Monitor Command Stack, and a Monitor Data Stack. The pointers for the various stacks have fixed locations in the BU-65549 address space.

SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION

TABLE 30 illustrates a typical memory map for the ACE in the Selective Message Monitor mode. This mode of operation defines several fixed locations in the RAM. These locations are allocated in a manner that is compatible with the combined RT/Selective Message Monitor mode. The fixed locations in the memory map consist of two Monitor Command Stack Pointers (location 102H and 106H), two Monitor Data Stack Pointers (locations 103H and 107H), and a Selective Message Monitor Lookup Table (0280-02FFH). The Monitor lookup table provides message filtering based on RT Address, T/$\overline{R}$, and subaddress. TABLE 30 assumes a Monitor Command Stack size of 1K words, and a Monitor Data Stack size of 2K words.

FIGURE 13 illustrates the Selective Message Monitor operation. Upon receipt of a valid Command Word, the BU-65549 will reference the Selective Monitor Lookup Table (a fixed block of addresses) to check for the selection status (disabled/enabled) of the current command. If disabled, the BU-65549 will ignore (and not store) the current message; if enabled, the BU-65549 will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer.

Similar to RT mode, the BU-65549 stores a Block Status Word, 16-bit Time Tag Word, and Data Block Pointer in the Message Descriptor, along with the received 1553 Command Word following reception of a valid, selected Command Word. The BU-65549 writes the Block Status and Time Tag Words at both the start and end of the message. The Monitor Block Status Word contains indications of message in-progress or message complete, bus channel, Monitor Data Stack Rollover, RT-to-RT transfer and RT-to-RT transfer errors, message format error, and other error conditions.

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TABLE 25 shows the Message Monitor Block Status Word. The Data Block Pointer references the first word stored in the Monitor Data Stack (the first word following the command word) for the current message. The BU-65549 will then proceed to store the subsequent words from the message (possible second command word, data word(s), status word(s)) into consecutive locations in the Monitor Data Stack.

Note: If the Monitor lookup table is set to capture only a subset of subaddresses for an RT, there may be confusing results where an array of command and data words have been rejected and the following status word has the bit pattern of a valid command word.

The size of the Monitor Command Stack is programmable to 256, 1K, 4K, or 16K words. The Monitor Data Stack size is programmable to 512, 1K, 2K, 4K, 8K, 16K, 32K, or 64K words.

Monitor interrupts may be enabled for Monitor Command Stack Rollover, Monitor Data Stack Rollover, and/or End-of-Message conditions. In addition, in the Word Monitor mode there may be an interrupt enabled for a Monitor Trigger condition.

TABLE 30. TYPICAL SELECTIVE MESSAGE MONITOR MEMORY MAP (SHOWN FOR 64K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-0101	Not Used
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack Pointer A (fixed location)
0104-0105	Not Used
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0260-027F	Registers
0280-02FF	Selective Monitor Lookup Table (fixed area)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0BFF	Monitor Command Stack B
0C00-0FFF	Not Used
1000-1FFF	Monitor Data Stack A
2000-FFFF	Available for more or larger stacks

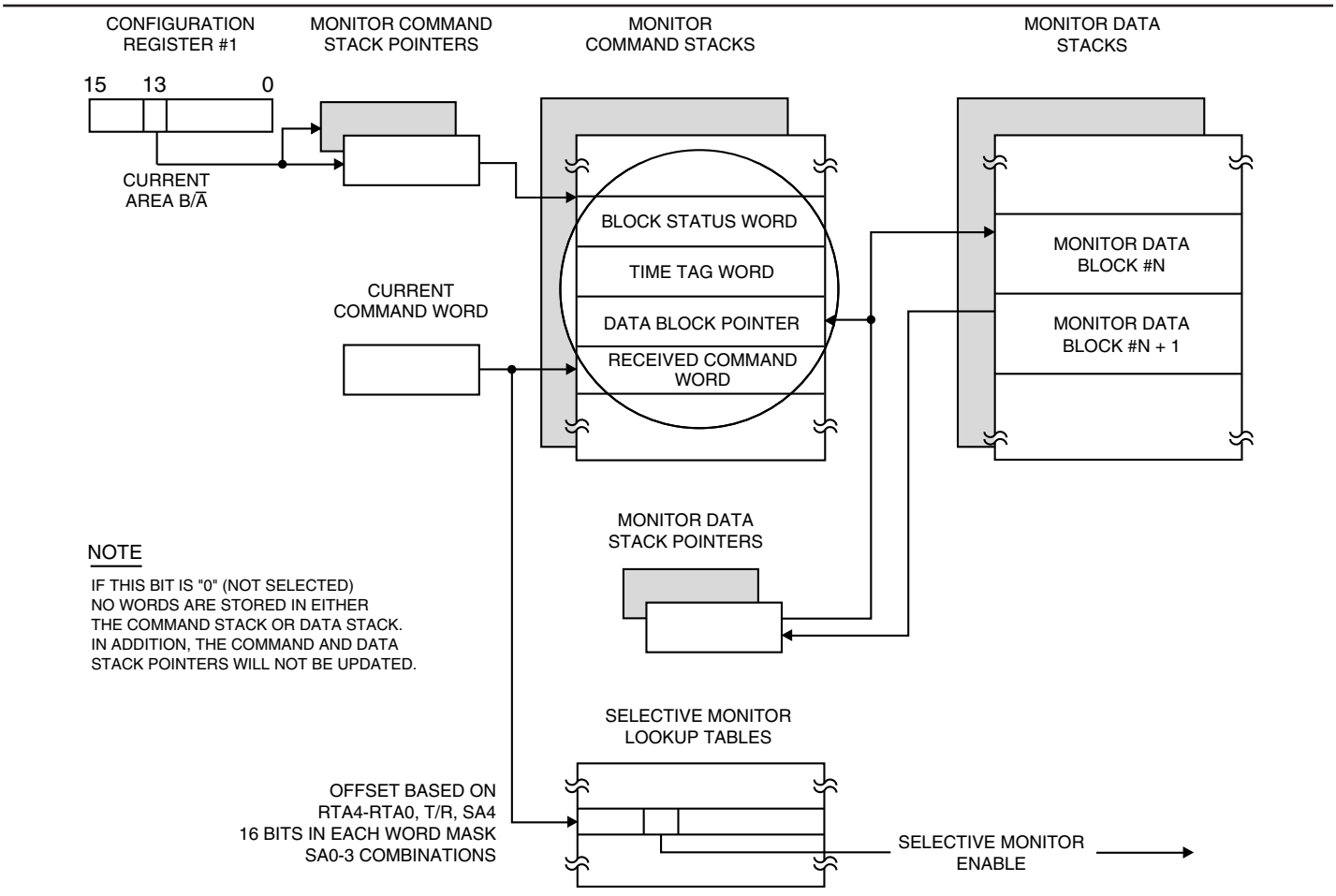


FIGURE 13. SELECTIVE MESSAGE MONITOR MEMORY MANAGEMENT

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INTERFACE TO MIL-STD-1553 BUS

FIGURE 14 illustrates the interface from the BU-65549 to a 1553 bus for either transformer (long stub) or direct (short stub) coupling, plus the peak-to-peak voltage levels that appear at various points (when transmitting).

Jumpers allow for either transformer or direct coupling to be selected.

Both coupling configurations require the use of an isolation transformer that interfaces directly to the card. For the transformer (long stub) coupling configuration, a second transformer, referred to as a coupling transformer, is required. In accordance with MIL-STD-1553B, the turns ratio of the coupling transformer is 1.0 to 1.4.

Alternative suitable termination methods may be used if two terminals are directly connected.

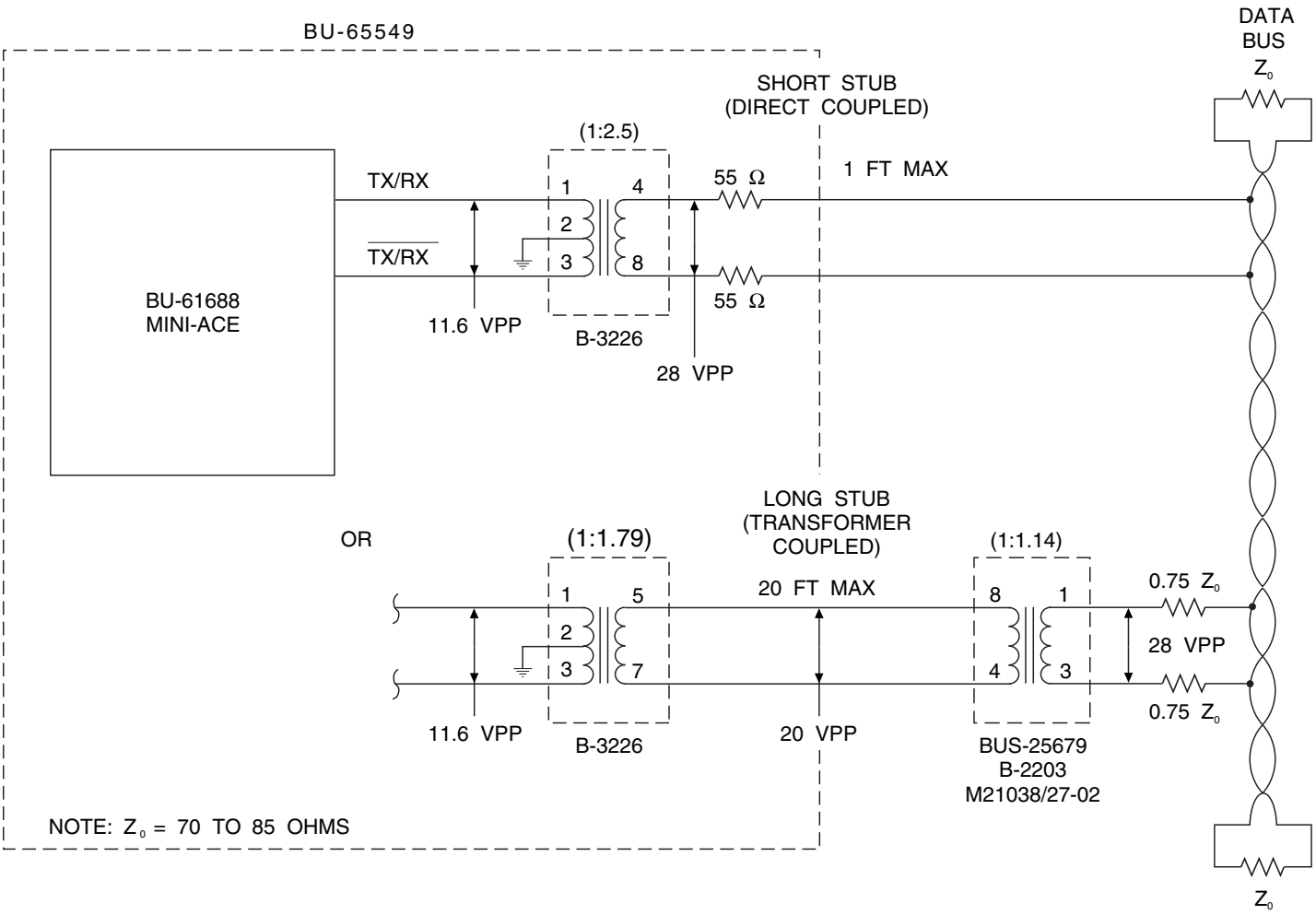


FIGURE 14. BU-65549 INTERFACE TO A MIL-STD-1553 BUS (ONE CHANNEL SHOWN)

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INSTALLING JUMPERS

Jumper blocks are used to select between transformer and direct coupling configurations as follows:

Direct coupling: install jumpers from pin 9 to 10 and pin 15 to 16.

Transformer coupling: install jumpers from 11 to 12 and pin 13 to 14.

P4A: Channel 1-A Coupling option. Install jumpers for coupling configuration as described above.

P4B: Channel 1-B Coupling option. Install jumpers in same locations as on ***P4A***.

P5A: Channel 2-A Coupling option. Install jumpers in same locations as on ***P4A***.

P5B: Channel 2-B Coupling option. Install jumpers in same locations as on ***P4A***.

Drawing not to scale. Dimensions in inches (mm).

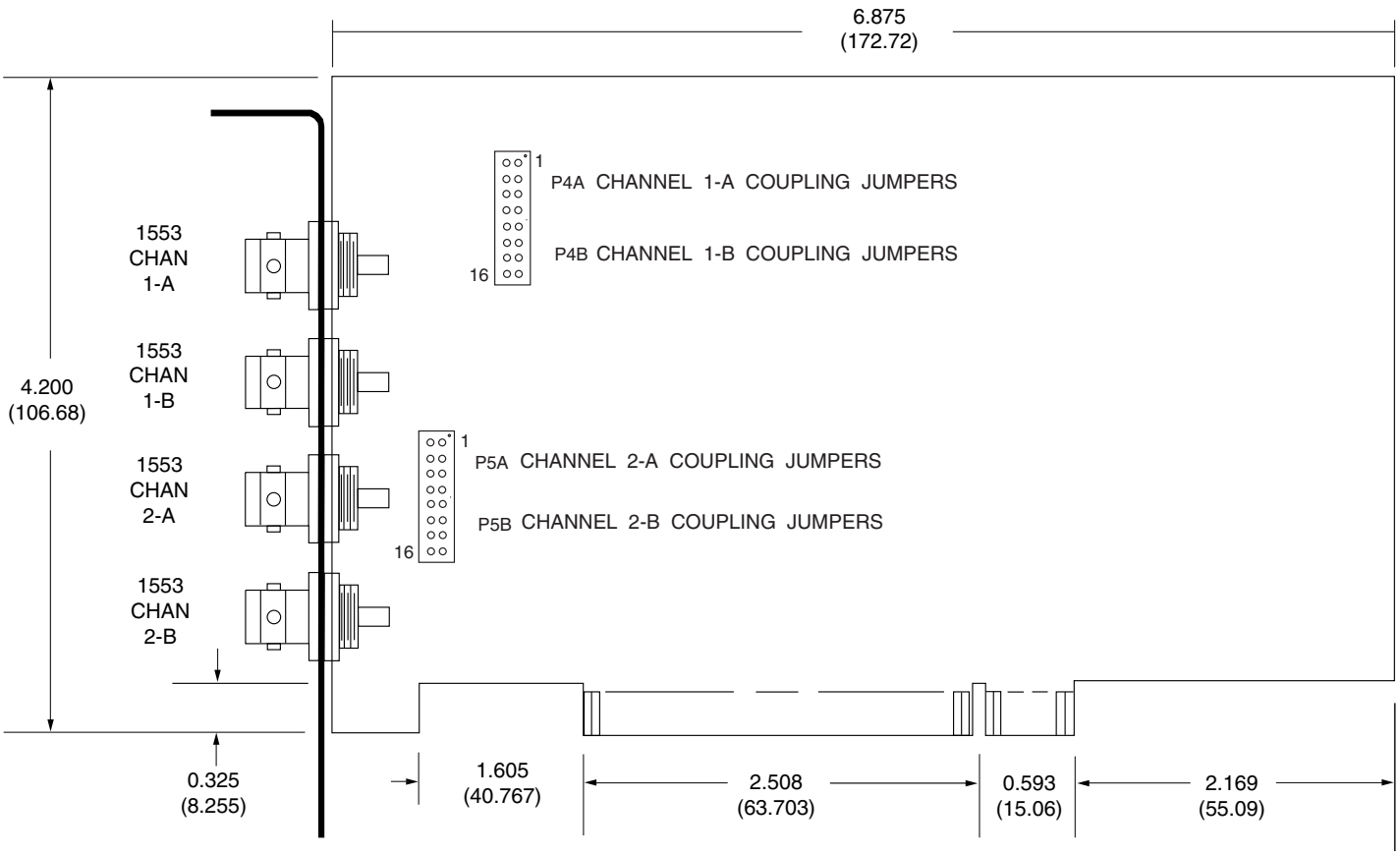


FIGURE 15. MECHANICAL OUTLINE (WITH JUMPER LOCATIONS)

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CE MARK CERTIFICATION

This product carries the CE MARK signifying conformance to the requirements of COUNCIL DIRECTIVE 89/336 EEC.
The supporting test (report) is on file at DDC, New York, USA and is available for on-site review.

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DECLARATION OF CONFORMITY

We Data Device Corporation
105 Wilbur Place
Bohemia, NY 11716-2482

declare under our sole responsibility that the product(s)
BU-65549

to which this declaration relates is in conformity with the following standard(s) or other normative document(s):

EN 55022-1: 1998 CLASS B; Conducted Emissions (150kHz to 30MHz)
CLASS B; Radiated Emissions (30MHz to 1GHz)

EN 50082-1: 1997 EN 61000-4-2:1995; Electrostatic Discharge
EN 61000-4-3:1997; Radiation Immunity
ENV 50204:1994; Radiated Immunity, Pulsed
EN 61000-4-4:1995; EFT/Burst, Power and I/O Leads
EN 61000-4-5:1995; Surge Immunity, Power Leads
EN 61000-4-6:1996; Conducted Immunity, Power and I/O Leads
EN 61000-4-11:1994; Voltage Dips and Interrupts

following the provisions of COUNCIL DIRECTIVE 89/336 EEC

Place Bohemia, NY USA

(Signature)

Date May 2, 2000

Joseph Saber
(Full Name)

Director, Product Assurance
(Position)

DDC-PAF-634A
04/05/2000

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ORDERING INFORMATION

BU-65549MX-300

- Temperature Range:
  - 3 = 0 to 55 °C
- Number of Channels:
  - 1 = One Dual Redundant 1553 Channel
  - 2 = Two Dual Redundant 1553 Channels

Note: The above products contain tin-lead solder.

INCLUDED SOFTWARE:

- BUS-69080S1 32-Bit "C" Library (Linux)
- BUS-69082S0 32-bit “C” Library (Windows 9x)
- BUS-69083S0 32-bit “C” Library (Windows 2000/XP and Windows NT)
- BUS-69084S0 32-bit Menu (Windows 9x)
- BUS-69085S0 32-bit Menu (Windows 2000/XP and Windows NT)

OPTIONAL SOFTWARE:

- BU-69404DM-64VM 32-bit *dataMARS:* Data Monitoring, Analysis, and Replay; with Virtual Panels and Multiplex

STANDARD DDC PROCESSING FOR DISCRETE MODULES/PC BOARD ASSEMBLIES		
TEST	**METHOD(S)**	**CONDITION(S)**
INSPECTION / WORKMANSHIP	IPC-A-610	Class 3
ELECTRICAL TEST	DDC ATP	—

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