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BU-65549
Hardware Manual
MIL-STD 1553 BC/RT/MT
PCI Interface Card

MN-65549-001

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RECORD OF CHANGE

Revision	Date	Pages	Description
A	5/1/1999	All	Original Issue
B	6/2005	8	Updated Figure 4
C	3/2010	6	Mating connector statement removed.

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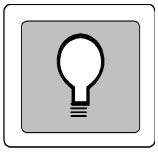
HOW TO USE THIS MANUAL

This manual uses typographical and iconic conventions to assist the reader in understanding the content. This section will define the text formatting and icons used in the rest of the manual. This manual is formatted with a „Scholar Margin' where many tips, symbols or icons will be located.

Text Usage

- **BOLD**– text that is written in bold letters indicates important information and table, figure, and chapter references.
- ***BOLD ITALIC***– will designate DDC Part Numbers.
- `Courier New`– is used to indicate code examples.
- <…> - Indicates user entered text or commands.

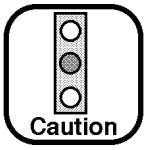
Symbols and icons



The Idea/Tip icon will be used to identify a handy bit of supplementary information that may be useful to the user.



The Note icon signifies important supplementary information that will be useful to the user.



The Caution icon identifies important information that presents a possibility of damage to the product if not heeded.

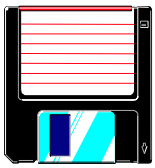


Much stronger than a Caution, the Warning icon presents information pertaining to hazards that will cause damage to the product and possible injury to the user.



The Reference icon indicates that there is related material in this manual or in another specified document.

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The Disk Icon describes information that is related to software.

Special Handling and Cautions

The ***BU-65549*** uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.



- Turn off power to the PC and unplug from wall.
- **NEVER** insert or remove card with power turned on.
- Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.
- Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

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INTRODUCTION

The ***BU-65549*** provides full, intelligent interfacing between the dual redundant MIL-STD-1553 Data Bus and a PCI Bus (refer to Figure 2 on page 4). Software controls the ***BU-65549's*** operation as a 1553 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT). The ***BU-65549*** is packaged on a half-size IBM PC/AT printed circuit board with a PCI bus interface. The board features one or two of DDC's Mini-Advanced Communication Engine + (Mini-ACE+) terminals. Each terminal provides dual transceiver and encoder/decoders, complete 1553B protocol, 64K words of shared RAM and memory management logic for all three modes.

Background Mode Operation prevents inadvertent access to the card during power-on self-test. On-board Interrupt Mask and Interrupt Status Registers support flexible operation for both interrupt and polling applications. The memory management scheme for RT mode provides an option for separation of broadcast data plus a circular buffer option for individual RT sub-addresses to off-load the demands on the PC host processor. Other features of the board include:

- Plug-and-Play (PnP) compatible for easy installation
- One or Two 1553 terminals on a single board
- 64K words of shared memory per 1553 terminal
- Wrap-around Built-In-Test
- Register Programmable Interrupt Level
- Programmable BC Gap Times
- BC Frame Auto-Repeat
- Automatic BC Retries
- Flexible RT Data Buffering
- Monitor Command Filtering
- Simultaneous RT/Monitor Mode
- Flexible Interrupt Generation
- Programmable Illegalization

What is included in this manual?

This manual contains a detailed installation guide for the ***BU-65549*** PCI Card and a basic overview of the software supplied with the card. Library, DLL, and Driver installations for Windows® 95, and Windows NT® will be covered in the following sections.



The ACE Library Software provides a level of abstraction such that it is not necessary to understand the operation of the Mini-ACE+ chip set. This manual provides an introduction to the ACE Library. Complete documentation for the ACE Library is provided in **the *BUS-69080/69082/69083* Software Manual**. For those who are interested in detailed information on the operation of the control registers and memory mapped data structures, a copy of the

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ACE User's Guide may be obtained from the DDC web site at **www.ddc-web.com**.

TECHNICAL SUPPORT

In the event that problems arise beyond the scope of this manual, you can visit the DDC website and review the FAQ page. If you still have questions you can get in touch with DDC by calling:

Customer support:

1-800-DDC-5757, ext. 7257

Headquarters:

1-631-567-5600, ext. 7257

Regional Offices:

Northern New Jersey:
(908) 687-0441 Fax: (908) 687-0470
West Coast:
(714) 895-9777 Fax: (714) 895-4988
Southeast:
(703) 450-7900 Fax: (703) 450-6610
Europe:
44 (1635) 811140 Fax: 44 (1635) 32264
Asia/Pacific:
81 (3) 3814-7688 Fax: 81 (3) 3814-7689

Or by faxing 1-631-567-5758 to the attention of DATA BUS Applications

DDC also has an Internet World Wide Web site, which allows customers to easily download new revisions of software and documentation. The Internet address is **www.ddc-web.com**.

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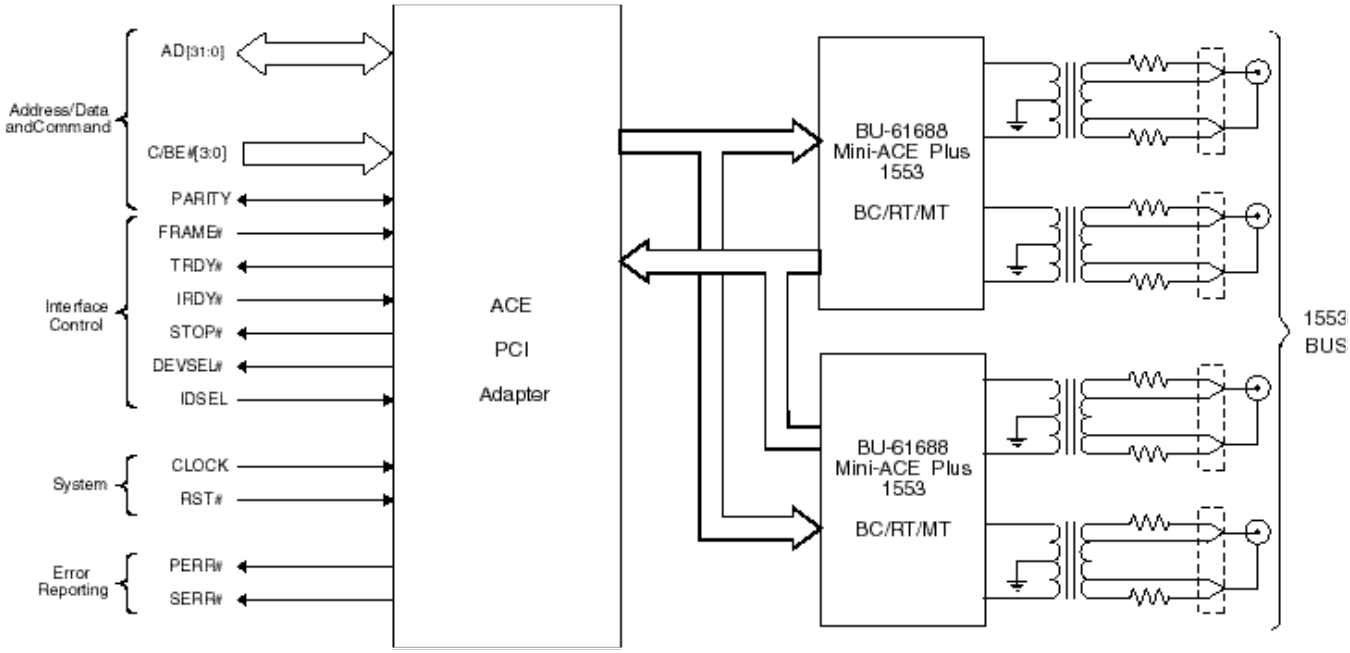
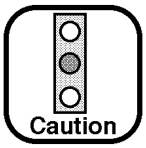


Figure 1 - BU-65549 BLOCK DIAGRAM

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HARDWARE INSTALLATION





The ***BU-65549*** card may be inserted into any PCI compatible slot. When installing the card, the following should be observed:

- **NEVER** insert or remove the card with the power turned on.
- **ALWAYS** take proper precautions to guard against static damage. Use a wrist strap if available, or ensure proper static grounding by touching the power supply cover **WITH POWER OFF**.
- Insert the card at a slight angle so that the triax connectors first protrude from the rear opening and then gently press the card into the motherboard connector. Secure with proper hardware.
- Make sure that adjacent cabling and wiring do no hinder the airflow around the card.

The ***BU-65549*** contains jumper blocks that allow for transformer or direct coupling for each bus connection. There are no jumpers or switches to be set for address and interrupt selection. This card is designed as a Plug-and-Play device and as such, these parameters can only be changed using the Control Panel application provided with the software (refer to Figure 2).

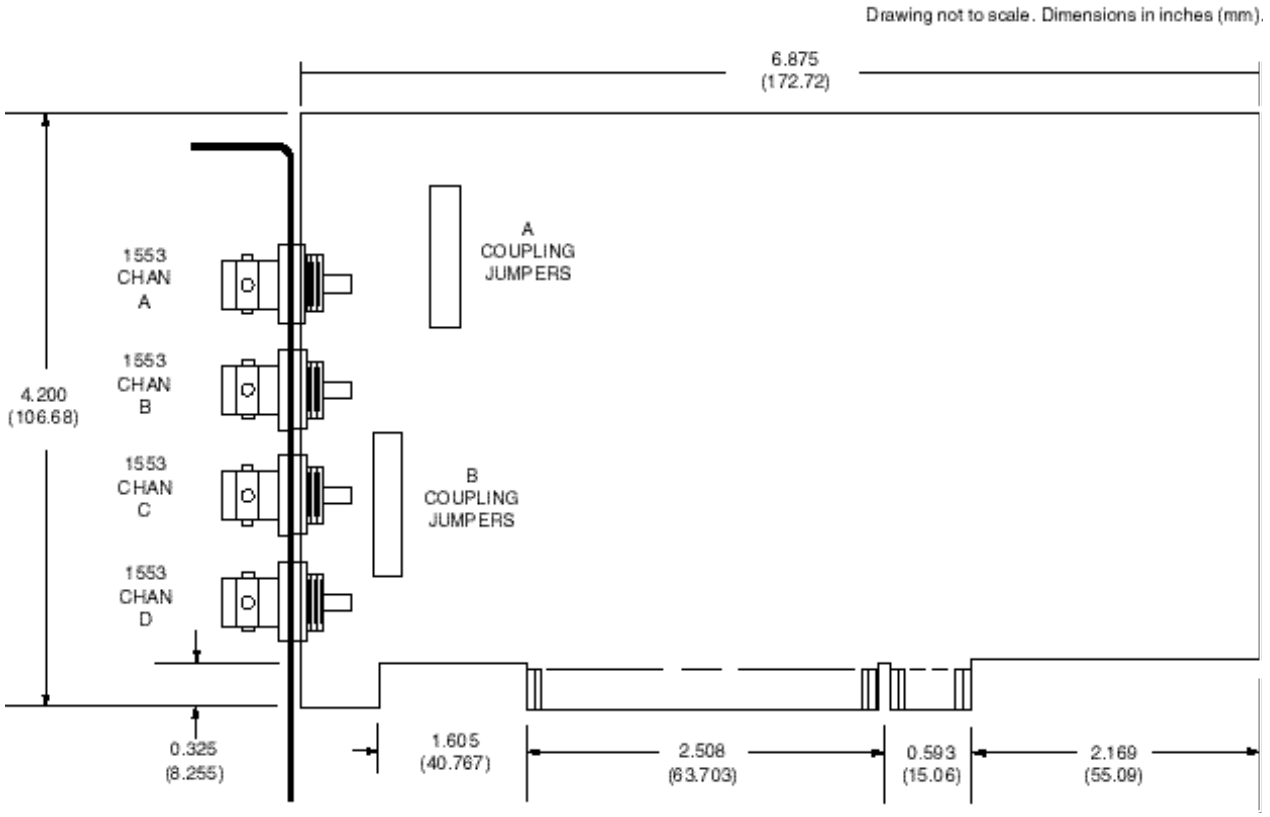


Figure 2 - BU-65549 Diagram

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HARDWARE CONFIGURATION

The ***BU-65549*** is a true PCI device, and as such does not require any jumpers or switches to set the Base address or interrupt values. The job of configuration for Plug-and-Play PCI configuration is performed by the PC BIOS. During the initial power on boot process, the BIOS performs an enumeration of the PCI bus and locates a configuration in the system that satisfies the card requirements. The card communicates to BIOS how much memory it requires, the interrupts that it supports, and any other operating parameters that the system needs to know by way of configuration registers built into the card. These registers are configured at the factory to contain the optimum values for the operation of the ***BU-65549***. There is no longer any need for the user to provide a specific memory location or size, or have to juggle interrupts to get their 1553 card installed. The PCI allows for shared interrupts, which are implemented in the ***BU-65549***. The device driver that is provided with the hardware can determine which of the two ACE devices on the ***BU-65549*** generated the interrupt, and acts accordingly. The base memory address is no longer required to be located in the first megabytes of RAM. In fact, BIOS will usually place the device as high in memory as possible. This makes hardware installation much easier than in the past.

BUS COUPLING MODE

The ***BU-65549*** can be interfaced to a MIL-STD-1553 bus in either Direct or Transformer-coupled mode. The two modes are configured via two jumper blocks labeled JP3 and JP4 on the card (refer to Figure 2 on page 4).
JP3: Terminal 1, 1553 Channel A and B coupling option. Install jumpers on pins 1, 4, 7 and 10 for direct-coupled connections or on pins 2, 3, 8 and 9 for transformer-coupled connections. Pins 5 and 6 have no connection. Pin 1 is located at the top, farthest away from the PCI bus connector. The pin descriptions are as follows:

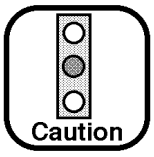
Pin No	Function
1	Bus A - Direct Coupled Positive
2	Bus A - Transformer Coupled Positive (factory default)
3	Bus A - Transformer Coupled Negative (factory default)
4	Bus A - Direct Coupled Negative
5	N/C
6	N/C
7	Bus B - Direct Coupled Positive
8	Bus B - Transformer Coupled Positive (factory default)
9	Bus B - Transformer Coupled Negative (factory default)
10	Bus B - Direct Coupled Negative

JP4: Terminal 2, 1553 Channel A and B coupling option. Same as **JP3** but applies to the second ACE terminal (if applicable) on the card.

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TRIAX CONNECTORS

The triax connectors are standard BJ77 types manufactured by Trompeter Electronics Inc. The mating connector required on the stub cable is Trompeter PL75 or equivalent. The connectors may be configured for transformer coupling or direct coupling as described in the BUS COUPLING MODE section. The ***BU-65549*** card should be connected to a bus as specified by MIL-STD-1553B, refer to Figure 3 on page 7 for further information on interfacing to a 1553 data bus.



Due to heat dissipation limitations, the triax connectors should NOT be shorted for more than a few seconds while transmitting. The connector's center pin is positive during the first half of a command sync. The upper most connector corresponds to Bus A (Bus A Terminal 1), and the lower most connector corresponds to Bus D (Bus B of Terminal 2). Refer to Diagram on page 4.

INTERFACE TO A MIL-STD-1553 BUS

Figure 3 on page 7 illustrates the interface from the ***BU-65549*** to a 1553 bus for either transformer (long stub) or direct (short stub) coupling, plus the peak-to-peak voltage levels that appear at various points (when transmitting). Note that this diagram is applicable for each of the two terminals available on the card. Each ***BU-65549*** terminal/channel pair can be switched to use either transformer or direct coupling by configuring the correct jumper (refer to BUS COUPLING MODE on page 5).

Both transformer- and direct-coupling configurations require the use of an isolation transformer that is located on the ***BU-65549*** card. For the transformer (long stub) coupling configuration, a second transformer (referred to as a bus-coupling transformer) is required. In accordance with MIL-STD-1553B, the turns ratio of the coupling transformer is 1.0:1.4.

Both coupling configurations also require an isolation resistor to be placed in series with each leg of the transformer connecting to the 1553 bus; this protects the bus against short circuit conditions in the transformers, stubs, or terminal components. For the direct-coupled mode, these isolation resistors are supplied on the ***BU-65549*** card. For the transformer-coupled mode, the bus coupler supplies these resistors.

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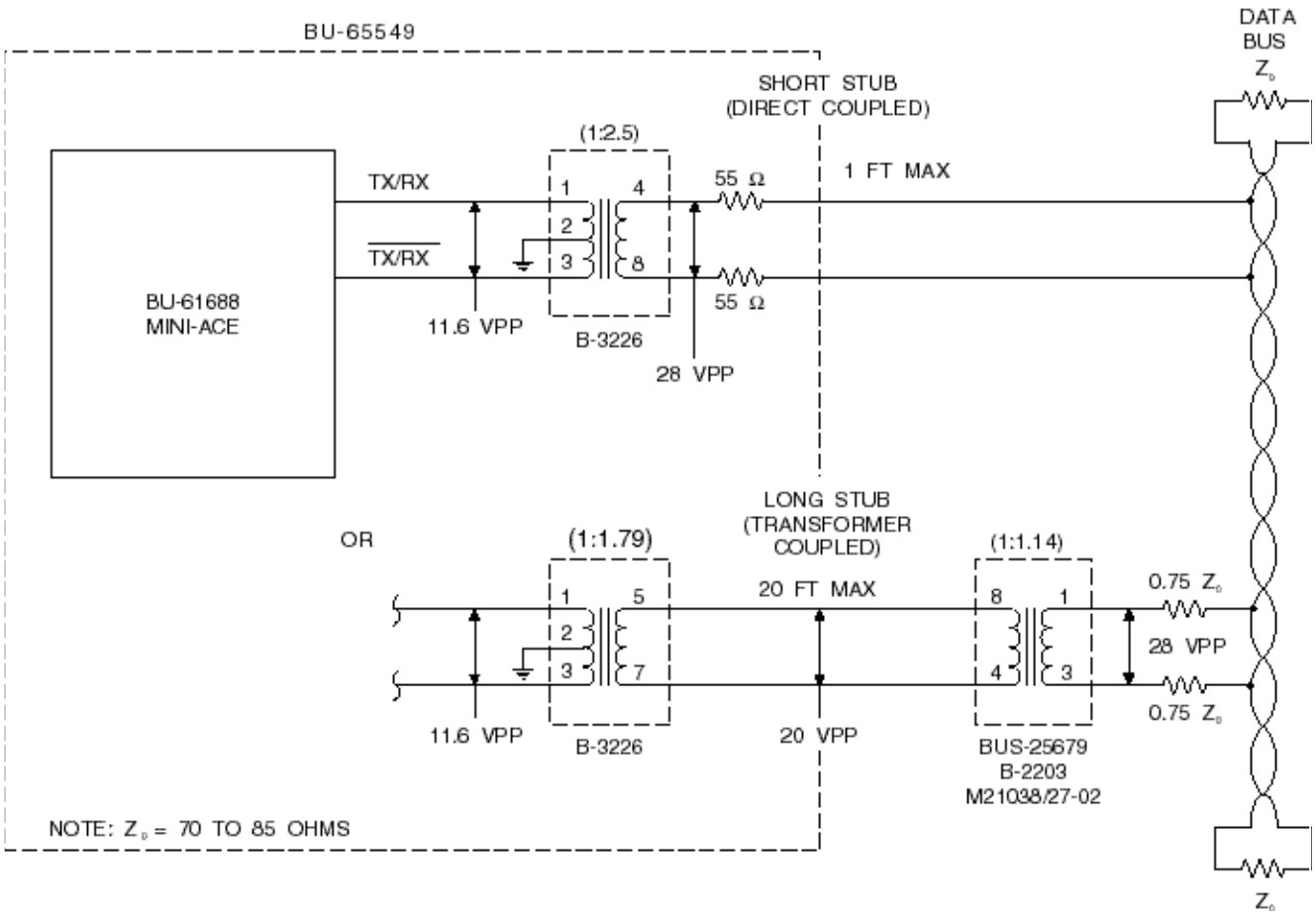


Figure 3 - BU-65549 INTERFACE TO A MIL-STD-1553 BUS

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“SIMULATED BUS” (LAB BENCH) INTERCONNECTIONS

For purposes of software development and system integration, it is generally not necessary to integrate with the required couplers, terminators, etc. that comprise a complete MIL-STD-1553B bus. In most instances, a simplified electrical configuration will suffice. The interconnection methods illustrated in Figure 4 allow the 65549 PCI Card to be interfaced over a “simulated bus” to simulation and test equipment. The length of this “simulated bus” should not exceed 5 feet.

It is important to note that the **termination resistors indicated are necessary** (if not already present within the test/simulation equipment) in order to ensure reliable communications between the 65549 PCI Card and the simulation/test equipment. As illustrated in Figure 4, the 78 ohm and 39 ohm termination resistors should be physically located as close as possible to the test/simulation equipment.

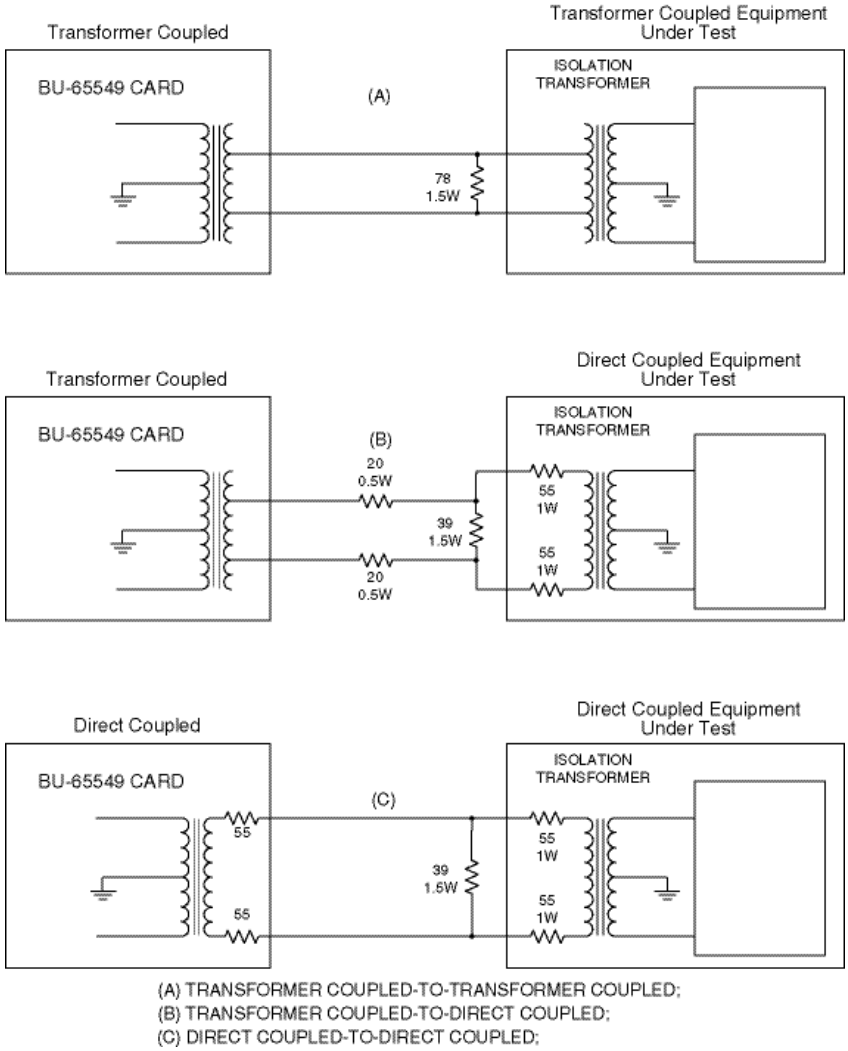


Figure 4. Simulated Bus Interconnections

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SOFTWARE INSTALLATION



16-bit not supported

The ***BU-65549*** PCI Card is supplied with Runtime Libraries for Windows 95/98 and Windows NT, and Windows Menu software for Windows 95/98 and Windows NT. Please note that the 16-bit versions of the library and menu are not supplied and they are not supported for the PCI version of the ACE hardware. The basic installation is listed below.

- Windows 95/98 will recognize new hardware and ask for a driver disk.
- Insert Disk 1 into floppy drive to install the device driver.
- Run the **setup.exe** program.
- Supply the necessary information during setup.
- Access the ACE Manager applet from the control panel and adjust the default settings if required. You must select a device number.
- Reboot the computer.

For detailed instructions, please refer to the following paragraphs.

Table 1 - ACE SOFTWARE

Part Number	Description	Requirements	Price
BUS-69082	32-Bit Windows 95 DLL/VxD	Win 95/98 8 Meg RAM 486 or better CPU 2.5 Meg Disk	Included with Hardware
BUS-69083	32-Bit Windows NT DLL/VxD	Win NT 8 Meg RAM 486 or better CPU 2.5 Meg Disk	Included with Hardware
BUS-69084	32-Bit Windows 95 Menu	Win 95/98 8 Meg RAM 486 or better CPU 1.0 Meg Disk	Included with Hardware
BUS-69085	32-Bit Windows NT Menu	Win NT 8 Meg RAM 486 or better CPU 1.0 Meg Disk	Included with Hardware

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ACE RUNTIME LIBRARY

The ACE Runtime Library is supplied for Windows 95/98 and Windows NT. The Windows 95/98/NT version includes sample files and utilities and must be installed under either Windows 95/98 or Windows NT. Both versions include the source and executable for the examples. The user is free to use the example source code, in part or in its entirety.

32-BIT ACE Drivers and Libraries for Windows 95/98 (*BUS-69082*)

INSTALLATION

Once the drivers have been correctly installed, the new software libraries may be installed. The installation of the 32-bit software and menus use the Installshield® utility. This allows for a consistent user interface when installing and removing software. If you are not familiar with this utility, follow the instructions below. If you wish to remove any of the 32-bit ACE products, you can use the START/SETTINGS/CONTROL PANEL/Add/Remove Software utility.

The driver installation will be initiated automatically the first time the PC is powered up after the hardware has been installed. When the BIOS enumerator discovers the new hardware, it will signal the system that new hardware has been found, and then the system (Windows 95/98) will instruct the user to provide a disk with the appropriate drivers.

With the drivers loaded, the libraries may be loaded next. Insert disk 1 of the ***BUS-69082*** disk set into the floppy drive and run setup.exe from the Start/Run selection. Installshield will proceed with the installation.



You **must** accept the license agreement by pressing the „YES' button.

The next screen presents the default selection for the install directory. Click the „BROWSE' button or type in the desired directory or select it from the directory tree to change the installation directory.

The next screen will present the default group that the software will be selectable from.

Finally, the Library software will be copied to the selected directory on the hard drive.

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FINAL INSTALLATION PROCEDURES

After you have installed the hardware drivers, and the software libraries, and re-started your computer, there is one more installation step to perform.

- Click into „Control Panel' (START/SETTINGS/CONTROL PANEL).
- Now double click on the „**ACE MANAGER**' icon. This will show all of the DDC devices you have installed in the computer. For each device entry you must select a Device Number. You do this by double clicking on the device part number, and then selecting 0, 1, 2, or 3 for the device.
- Select OK and you are ready to go.

Please refer to the section „Testing the Installation' on page 18.

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32-BIT ACE Drivers and Libraries for Windows NT (*BUS-69083*)

INSTALLATION

The installation for the new ACE library and drivers is slightly different for Windows NT than it is for Windows 95/98. Windows NT 4.0 will not automatically recognize the ***BU-65549*** even though it is a PnP PCI format. The drivers will be installed with the rest of the ACE Runtime Library when disk 1 is inserted and the SETUP.EXE program is run.

If this is a new installation, skip to the next paragraph. If you are updating an existing installation, the first step is to remove the existing WinRT driver. If there is a possibility that other software, such as the DDC IDEA software is installed, you can change the driver to run in the manual mode. Entering the CONTROL PANEL/DRIVERS applet enables access to the WinRT driver start-up control. Scroll to the bottom of the driver list to find the WinRT driver entry, and highlight it (single click). Once WinRT is highlighted, select the device to manual start or delete the device by using the buttons on the right side of the dialog box.

After the WinRT driver modification is complete and the hardware is installed in the PC, you can install the drivers and library by inserting the disk marked DISK 1, and running the SETUP.EXE program. This will install the system files, the library files and the control panel ACE NT MANAGER applet. When the setup program is running, a dialog will be presented to the user to select the card type to install. If the computer has multiple ACE cards, select one type now, the others may be installed using the ACE NT MANAGER applet.

When the setup.exe program is complete, you must reboot the computer.

FINAL INSTALLATION PROCEDURES

The final steps in installing the new ACE software require the device number selection for each installed card. This is performed in the control panel **ACE Manager For Windows NT** applet. Access the control panel and double click on the ACE Manager for Windows NT applet. This applet has been changed slightly to accommodate the new features and multiple cards correctly. When the applet is opened, it will contain one card, and the status will show appropriately good or bad. Refer to Figure 5 on page 13.
There will be four buttons to the left side of the dialog box, and a status window in the center. The four buttons are **MODIFY**, **DRIVERS**, **DELETE**, **CLOSE**.

- The **Modify** button presents a dialog that allows the interrupt, base address, and I/O parameters to be selected and modified.
- The **Drivers** button presents a dialog that shows all of the installed cards in the status window, and contains 4 buttons, **START**, **STOP**, **NEW**, **CLOSE**. This selection provides the capability to start or stop a driver, and add a new card and driver entry.

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- The **Delete** button will delete the presently selected (highlighted) card in the status window. A confirmation dialog will be presented to the user prior to deleting the card and driver.
- The **Close** button closes the ACE Manager dialog and saves all changes made.

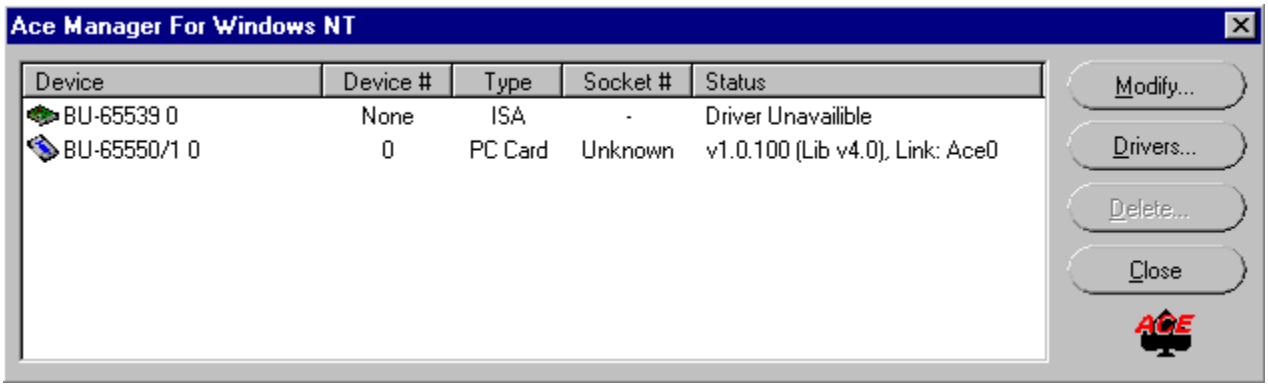


Figure 5 - ACE Manager for Windows NT

ACE MANAGER MODIFY BUTTON

Run the Windows NT **Administrative Tools \ NT Diagnostics** prior to following the procedures below. This application will provide good insight to the available resources for IO Port, Memory Address and Interrupts. Once all of the available resources are located, follow the procedures below in order to modify the settings for an existing installed card. Please note that the PCI card has no modifiable parameters. This card is enumerated by BIOS and the parameters are passed to the device driver via Windows NT.

- Click on the **Modify** button.
- Select the appropriate card type from the Tabbed list. **ACEPCCRDX** indicates the entries for the PCMCIA cards, **ACEISAX** indicates the entries for the ISA cards, and **ACEPCIX** indicates the entries for the PCI cards. In each case the 'X' will be a number from 0 through 3.
- Once the appropriate tab has been selected, the modifiable properties will be presented in a group of three edit boxes, and in the case of ***the BU-65539*** one check box.

ACEISA Configuration

If the device being modified is of the type ACEISA, then the text edit entries available will be **IO Port**, **Memory Address** and **Interrupt**, and the check box will allow for **Automatic Configure**. If the Automatic Configure box is checked, then the Memory Address and the Interrupt entries will be disabled. Refer to Figure 6 on page 14.

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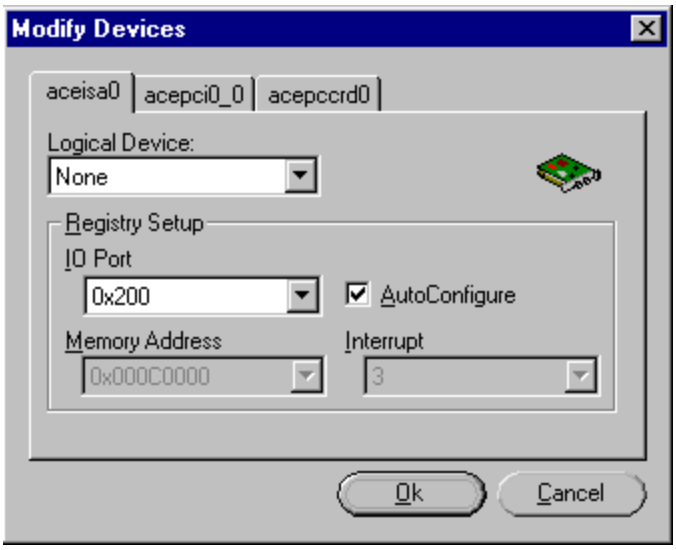


Figure 6 - Modify Devices, ACEISA

IO Port

The present ISA board requires an IO Port that will be used to programmatically set the Memory Address and the Interrupt. Two contiguous 8-bit IO port addresses must be available for the ISA card, allowing 16-bit access. For example, the default IO Ports are 0x390 and 0x391 as defined by the default switch settings of SW3. The IO Port may be selected from a drop-down list of possible values. The list provides selectable values ranging from 0x200 to 0x390.

Automatic Configure



multiple ISA cards

If the Automatic Configure box is checked, then the Memory Address and the Interrupt edit boxes will be disabled indicating that the system will automatically select these values from the available assets at that time.
NOTE: if multiple ***BU-65539*** cards are installed under Windows NT, then the Automatic Configure box **must not** be checked. The memory address and interrupt will have to be manually configured by the user. The memory address will have to be set to the same value for each of the ***BU-65539*** cards installed. These cards are able to share the same memory address space. The interrupts **must be** different.

Memory Address

The memory address tells the driver where in the upper memory to place the shared memory of the ***BU-65539*** card. The ISA card requires one entire segment of PC memory space equaling 64K bytes. This entry allows for a selection from the drop-down list box of 0x000C0000, 0x000D0000, or 0x000E0000. These are the only values that fit all of the criteria for the ***BU-65539***, but in most cases, the 0x000C0000 location will not be available as the video card usually uses the lower half segment of this location. If more

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that one ***BU-65539*** card is installed in the PC, they may all be set to the same memory address.

Interrupt

The interrupt is the last configurable entry for the ***BU-65539*** card. This drop-down list box provides a choice of interrupts 3 through 15. The user should use the available interrupts as provided by NT Diagnostics.
If more than one ***BU-65539*** card is installed, each must have its own interrupt.

ACEPCCARD Configuration

If the device being modified is of the type ACEPCCARD, then the text edit entries available will be **Memory Address**, **Interrupt**, and **Size**. Please note that presently, only one PC Card (PCMCIA) may be configured at a time. This is due to the operation of the device driver and Windows NT. The PC card comes in three memory configurations, 4K words, 12K words, and 64K words. In all three cases, the card will require one half segment in upper memory. Refer to Figure 7 on page 15.

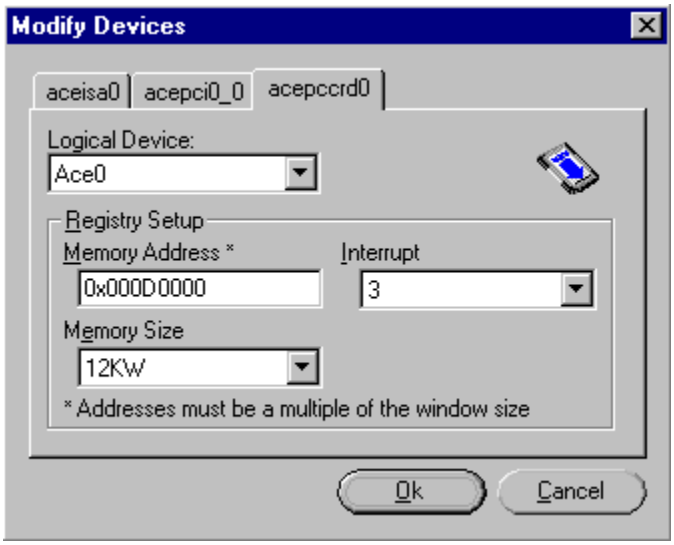


Figure 7 - Modify Devices, ACEPCCRD

Memory Address

The memory address tells the driver where in the upper memory to place the shared memory of the PC card. The PC card requires one half of an entire segment of PC memory space equaling 32K bytes. There is no drop-down list for this entry. The user must enter the memory address by typing in the appropriate value. Examples of the memory address are 0x000C8000, 0x000D0000, or 0x000D80000. It is up to the user to verify that the selected addresses are unused by other devices by running the NT Diagnostics, and by manually ascertaining the requirements of any other devices that may be installed in the PC.

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Interrupt

The ACEPCCRD device must have a uniquely assigned interrupt. The selection is available from a drop-down list, with values ranging from 3 through 15. As with the other resource selections, the selected interrupt must not be used by any other device in the PC. The list of used interrupts is viewable from the NT Diagnostics application.

Size

As stated previously, the ACEPCCRD comes in three memory sizes, 4K words, 12K words, and 64K words. The configuration of the size can be selected from the drop-down list box, which provides a choice of 4K, 12K or 64K. As a reference, refer to the table below for the card part numbers and the appropriate size selections.

Table 2 - Card Memory Requirements

Card P/N	Memory Size
BU-65550M2-300	12K
BU-65550M2-6XX ***BU-65551M2-300***	4K
BU-65552M2-300	64K

ACEPCI Configuration

There are no user configurable settings for the PCI cards. These cards are enumerated and configured by BIOS and Windows, and the parameters are reported to the device driver for the card. Refer to Figure 8 on page 16.



Figure 8 - Modify Devices, ACEPCI

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Windows NT provides the capability for any user that has Administrator rights to start or stop a device driver. The ACE Manager now provides this capability from the Drivers dialog. An additional capability includes adding a new instance of a driver. This is useful when new cards are installed into the PC. To enter this dialog, click the Drivers button on the main ACE Manager dialog. When the device dialog is open, it provides three radio buttons for the selection of the active device, a **Start** button, a **Stop** button, a **New** button, and a **Close** button. Refer to Figure 9 on page 17.

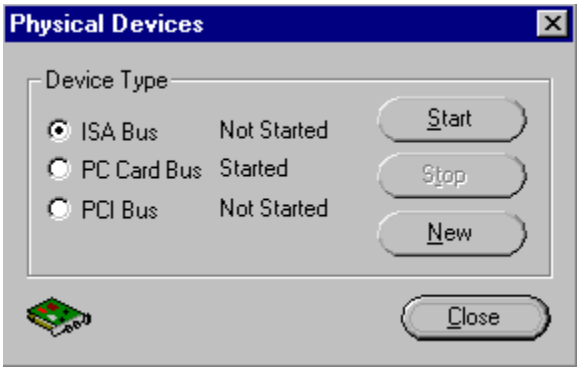


Figure 9 - Physical Devices Control Panel

Device Radio Buttons

The three device radio buttons allow for the selection of one of the device drivers loaded into the Windows NT system. These are the ACEISA, ACEPCCRD, and ACEPCI. The ACEISA radio button enables actions to be directed to the ISA card device drivers. The ACEPCCD radio button enables actions to be directed to the PC card device drivers, and the ACEPCI radio button enables actions to be directed to the PCI card device drivers.

Start

The start button allows the user start the device driver that has been enabled by the selection of one of the device radio buttons. Once the device driver has been started, all of the correctly configured devices controlled by this driver will be operable.

Stop

The stop button allows the user to stop the device driver that has been enabled by the selection of one of the device radio buttons. Once the device driver has been stopped, all of the devices controlled by this driver will become inoperable.

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New

When a new device is added to the PC, a new instance of the device driver must be installed. For example, you may have a PC with one installed ***BU-65539*** ISA card that is installed and correctly configured. Then, some time later you if add a ***BU-65549*** PCI card, you will have to install an instance of the ACEPCI driver. This would be performed by selecting the ACEPCI device radio button, and then clicking on the New button. If you want to add a second ***BU-65539*** ISA card you would have to add another instance of the ACEISA device driver.



After installing the new instance of the device driver, you must access the ACE Manager Modify dialog to ensure that the device is configured correctly. Please refer to section the ACE Manager Modify Button on page 13.

Close

When the Close button is clicked, all changes will be saved, and the Drivers dialog will be closed. Processing will then continue from the ACE Manager dialog.

ACE MANAGER DELETE BUTTON

If a hardware device is removed from the PC or is not needed any longer, the device driver instance may be deleted from the system. Highlighting the device in the ACE Manager Status window, and then clicking on the Delete button will cause this device to be deleted. When the delete button is clicked, a confirmation dialog will be presented to the user. This will enable the user to cancel an accidental delete command.



If a device has been deleted and is subsequently needed again, a new driver instance would have to be created and configured. Please refer to the sections ACE Manager Device Button on page 17 and ACE Manager Modify Button on page 13

ACE MANAGER CLOSE BUTTON

Pressing the ACE Manager Close button will cause all changes to be saved, and the ACE Manager dialog to be closed. This action will return to the previous process.

Testing the Installation

Once the hardware and software are installed, you can test the installation by running one of the sample programs that is shipped with the software. Follow the steps below to test the installation.

- From a Command prompt, change to the directory „<disk>:\Program Files\Data Device Corporation\ACE45\EXE'.

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- Run the selftst2.exe program with the command line `< SELFTST2 0 >`. This program requires a device parameter. The 0 indicates that the hardware is defined as 0 in the ACE Manager applet. This parameter will be modified as required per the installation. If you have more than one device installed in the system, then running SELFTST2 with the appropriate parameter, 0, 1, 2 or 3 should test each of the cards individually.

If all went well, you should have passed all elements of the test, and are now ready to use your 1553 card/software.

If you didn't pass SELFTST2.EXE, refer to the section Troubleshooting the **Installation** on page 19 of this manual or visit the Data Device Corp www Site at **www.ddc-web.com**.

Troubleshooting the Installation

In most cases, the installation should complete without any problems, and running the self-test should result in all tests passing. The usual problems that result from incorrect resource selection are not relevant since BIOS and Windows configure the PCI bus. There are however, some situations that can cause problems during the installation. The most common of these are listed below.

A BU-107 error is returned when an attempt to run selftst2 or any of the other sample programs. This fault is almost always related to the lack of a device number. Reference Final Installation Procedures on page 11 for Windows 95/98 or page 12 for Windows NT.

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ACE WINDOWS MENU

The ACE Menu is a powerful user interface to the MIL-STD-1553 bus and runs on top of the Windows GUI (graphical user interface). The ACE Menu for Windows 95/98 and Windows NT are included as standard software supplied with the ***BU-65549***. The ACE Menu software, setup files, and stack files are 100% compatible with all other ACE based 1553 PC boards supplied by DDC.

When using the ACE Menu, the user has full control of the Bus Controller, Remote Terminal, Monitor and Self-Test functions from an easy to use interface. Using the intuitively designed controls in this menu, the user has the capability of setting up messages, minor frames, major frames, timing, filtering and many other functions required by the beginning and advanced MIL-STD-1553 user. Without programming a line of code, the ACE Menu enables the user to quickly get started using the ACE family products.

32-BIT ACE Menu Software (*BUS-69084* / *BUS-69085*)

The ACE Menu for Windows 95/98/NT is a native 32-bit program that provides a simple to use Graphical User Interface. This GUI will help the user quickly setup and run Bus Controller, Remote Terminal or Monitor sessions on a PC equipped with a ***BU-65549*** PCI card or any of the other DDC 1553 PC cards. This software requires the successful installation of the ACE 32-bit drivers and the ***BU-65549*** hardware.

The ACE 32-bit Menu is supplied on two 3.25 inch, 1.44 Meg floppies and requires approximately 4 Meg of hard disk space. The installation uses Installshield, which provides a standard user interface for installation and removal of software products.

As a general guide, all active programs should be closed during installation of any software. Once all programs have been terminated, you may proceed with installation. During installation, it will be assumed that the floppy drive used is the A: drive and the target drive for installation is denoted as “C:”. If your system requirements are different, please substitute the appropriate values.

INSTALL ACE MENU FOR WINDOWS 95/98 AND NT

Note that the text is written for Windows 95/98, if the user is installing for Windows NT the substitution of Windows NT for Windows 95/98 should be made.

- Place the install disk in the A: drive of your system. Click the START button and then select RUN. When the RUN window appears, enter A:\SETUP.EXE in the edit window, or you may use the BROWSE button

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to obtain the setup program on A: drive. Next click the OK button to continue.

- The next window will be the DDC CORPORATION banner and InstallShield setup.
- After InstallShield has successfully setup, you will see a window containing „ACE MENU for Windows 95' and an InstallShield welcome. Click NEXT to continue, or CANCEL to halt installation.
- You will now have to agree to a license for use. If you select YES, you will be bound by the license, if you select NO, then installation will halt, and if you select BACK, InstallShield will take you back to the previous screen.
- Next, select the installation destination drive and directory. The default value for this entry is „C:\Program Files\Data Device Corp\ACEMenu'. You may use the BROWSE button to select an existing drive and directory. The NEXT button continues the installation, the BACK button takes you back to the license agreement, and the CANCEL button halts installation.
- Select a program folder that will contain the program and help files for the ACE Menu. This folder will show up in the START/PROGRAMS popup window, with the same name that is entered here. The default value for this entry is „Data Device Corporation'. The NEXT button continues the installation, the BACK button takes you back to the directory selection window, and the CANCEL button halts installation.
- At this point, the files required for ACE Menu will be copied to the hard drive and the folders will be created.
- The last window to be displayed is SETUP COMPLETE. Click the FINISH button to complete the Installshield setup.

You do not have to reboot the system for this installation.



Please note that if you are installing the new version of the ACE Menu over the old version, you should ensure that the old version was removed with the uninstall utility provided in the control panel application „ADD / REMOVE PROGRAMS'. If the old version is not removed there is a possibility that the old ACE Menu will be run with the new drivers. This will create a situation where the driver will report that the hardware could not be opened. You will have to manually remove the entry in the startup menu. This may be performed by accessing START / SETTINGS / TASKBAR… then click the „Start Menu Programs' tab. From here you should click the „Advanced' button, and then expand the „Programs' folder entry. Finally, highlight the „ACE Menu for Windows 95' folder, and press the delete button.



You are now ready to run ACE Menu for Windows 3.0. Select „**START/PROGRAMS/Data Device Corporation/ACE Menu for Windows 3.0/ACE Menu for Windows'**. This will start the menu program and you should see the „Ace32 Windows Application' window appear. To insure everything is working correctly, access the FILE menu and click the NEW menu entry. Now you should click the TEST button or select Test from the menu. Next click the ALL button. This will perform a basic test of the ACE hardware registers, protocol, memory, and interrupts. If the test passes, then

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you are ready for operation. If the test fails, check the installation of the ACE library and drivers.

From here you should refer to the ACE Menu User's guide, Help and ReadMe files.

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OTHER CONSIDERATIONS FOR INSTALLATION

System Resources

When using Windows 95 or NT, the user decisions pertaining to system resources (memory and interrupts) go away because BIOS defines these parameters during the computer boot process. The user has the control only to view these resources; there is no mechanism for user modification of these parameters.

Configuration Files

Unlike the previous versions of the ACE boards (***BU-65539*** and ***BU-65550/51***), the ***BU-65549*** PCI design does not incorporate any configuration files. All of the information needed for device configuration is located in the system registry.

Memory Base Address Selection

The ***BU-65549*** card needs 64K words (128K bytes) for each ACE terminal installed on the board. BIOS will assign all of the memory required by the card 64K words (128K words for a dual ACE card) from an area of addressable memory space well above the last word of RAM. This search for a free memory location is generally started at the top of memory space (4Gig). BIOS will reliably locate the memory needed for the interface, and during Windows Boot, will pass this information to Windows. There is no user intervention required for the configuration process.

Extended Memory Managers

Extended Memory Managers have no effect on the operation of the PCI devices installed in a PC.

Excluding Memory

Because the PCI card is placed in memory that can not be impacted by RAM or any other device, there is no requirement to exclude memory for either EMM386.EXE, or Windows.

Interrupt Level Selection

The interrupt request level (IRQ) is selected by BIOS during the power up boot process. Since the PCI interrupts are shared, there should be no problems with conflicts.

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SOFTWARE DEVELOPMENT LIBRARIES

The software development libraries supplied with the ***BU-65549*** are written in „C'. The Libraries for Microsoft and Borland Compilers supporting Windows 95/98 and Windows NT 32-bit applications are provided in the .\ACE45\LIB directory.

All of the 32-bit examples are supplied as both executable and source. The 32-bit source is written in „C', and found in the .\ACE45\SAMPLES subdirectory. The 32-bit executables are found in the .\ACE45\EXE directory. Additionally, as new samples are created, they will be placed on the DDC web site at www.ddc-web.com.

16-BIT ACE RUNTIME LIBRARY

The 16-bit version of the ACE Runtime Library is not supported for the ***BU-65549*** PCI card.

32-BIT ACE RUNTIME LIBRARY



The ***BUS-69082*** and ***BUS-69083*** ACE Runtime Libraries provide the framework for developing near "real-time" applications for the ***BU-65549*** PCI Card. The library, written in C, supports Windows 95/98/NT 32-bit applications using development tools from both Microsoft and Borland. For detailed information on the ACE Runtime Library and its Dynamic Link Library (DLL) refer to the „***BUS-69080***, ***69082***, ***69083*** ACE RUNTIME LIBRARY SOFTWARE MANUAL.'

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REFERENCE

ADDRESSING, INTERNAL REGISTERS, MEMORY MAP, INTERRUPTS

The ***BU-65549*** makes use of the memory space available on the PCI bus. The 64K words of shared ram and 24 internal ACE registers for each ACE terminal are memory mapped into the PCI memory space (refer to Table 3 and Table 4 respectively). The ***BU-65549*** contains an internal set of PCI configuration registers that are accessible by BIOS during the power on boot process. These registers help BIOS determine the interrupt, address space and PCI bus access requirements of the ***BU-65549***.



A good reference to PCI architecture is provided in the book "PCI System Architecture". Refer to PCI System Architecture on page 63.

All data communication between the ***BU-65549*** and the host processor via the PCI is performed over a 32-bit bus. This improves the data rate by moving two 16-bit words at a time from ACE memory to the host CPU memory. Transferring two words at a time reduces by half the number of reads and writes needed to process each message. This 32-bit transfer could present a minor problem when reading the ***BU-65549*** ACE registers. If the information of only one register (16 bits) is desired and the PCI bus reads two registers (32 bits), then the contents of the unwanted register would be ignored. It must be remembered, however, that in many cases, reading or writing a register in the ACE will cause an automatic response. For example, clearing the Interrupt Status register after reading. This automatic response is known as a side effect of the operation. If, in this case, the Interrupt Status Register was not of interest, then the host CPU would ignore the data transferred over the PCI bus, the Interrupt Status Register would normally clear itself, and the data that was ignored would be lost. In order to prevent this, the PCI access to ***BU-65549*** ACE registers is limited to a single 16-bit transfer. The upper 16 data lines of the PCI bus will be defined as don't care, and only one register will be accessed for each transfer. This access restriction can be seen in the following two tables (Table 3 and Table 4).

The software interface for each of the ***BU-65549*** ACE devices consists of 17 internal memory mapped registers for normal operation, an additional 8 registers used for test, and 64K x 16 bits of shared memory. Both the registers and the shared memory reside in the PCI memory address space.

PCI RAM ACCESS

The access to the shared RAM on the ***BU-65549*** card is shown in the Table 3 on page 26. This table shows that each RAM location in the ACE is a 16-bit word. This word is accessed by a byte offset from the beginning of the shared RAM, as listed in the second column. The first word in the RAM has a byte offset of 0x0000, and the last word in RAM has a byte offset of 0x1FFFE. The first column shows that the PCI will access two ACE words in a single

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read or write access. This shows that PCI address 0x00000 + RAM Base Address will read/write ACE words 0 and 1, while PCI address 0x00004 + RAM Base Address will read/write ACE words 2 and 3. This two-word access is important to device drivers and the system, but is invisible to the user at the application level.

Table 3 - Shared Ram Space Address Map

PCI ADDRESS (add to base addr)	BYTE OFFSET ADDRESS	DESCRIPTION (Each location = 16-bit word)
00000	00000	ACE Channel #1 RAM Location 0000 (0)
00000	00002	ACE Channel #1 RAM Location 0001 (1)
00004	00004	ACE Channel #1 RAM Location 0002 (2)
00004	00006	ACE Channel #1 RAM Location 0003 (3)
…	…	…
1FFFC	1FFFE	ACE Channel #1 RAM Location FFFF (64K)
20000	20000	ACE Channel #2 RAM Location 0000 (0)
20000	20002	ACE Channel #2 RAM Location 0001 (1)
20004	20004	ACE Channel #2 RAM Location 0002 (2)
20004	20006	ACE Channel #2 RAM Location 0003 (3)
…	…	…
3FFFC	3FFFE	ACE Channel #2 RAM Location FFFF (64K)

PCI REGISTER ACCESS

The ***BU-65549*** ACE Registers are mapped into system memory space by BIOS during the BOOT process. The software and hardware must ensure that only one register is read or written at a time. This is due to possible non-recoverable read data loss if the transfer is interrupted. In some cases, a register will be cleared when read, and if the read transfer is interrupted, a retry of the read will result in incorrect data, which is known as a Side Effect. It is important that register reads and writes are consistent. Therefore, every access to a register on the ***BU-65549*** will be forced to a 16-bit word transfer. Table 4 on page 27 identifies the register, its offset in the ACE, and the PCI bus address needed to access it. Note that the PCI address reads up to 32 bits at a time, but all access is byte addressed.

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Table 4 - Register Address Mapping

HEX ADDRESS		DESCRIPTION / ACCESSIBILITY
PCI BUS (add to base)	**ACE OFFSET**	
CHANNEL 1		
0000	0000	Interrupt Mask Register (RD/WR)
0002	0001	Configuration Register #1 (RD/WR)
0004	0002	Configuration Register #2 (RD/WR)
0006	0003	Start/Reset Register (WR)
0006	0003	BC/RT Command Stack Pointer Register (RD)
0008	0004	BC control Word/RT Sub-address Control Word Register (RD/WR)
000A	0005	Time Tag Register (RD/WR)
000C	0006	Interrupt Status Register (RD)
000E	0007	Configuration Register #3 (RD/WR)
0010	0008	Configuration Register #4 (RD/WR)
0012	0009	Configuration Register #5 (RD/WR)
0014	000A	Data Stack Address Register (RD/WR)
0016	000B	BC Frame Time Remaining Register (RD)*
0018	000C	BC Frame Time Remaining to Next Message Register (RD)*
001A	000D	BC Frame Time */RT Last command/MT Trigger Word* Register (RD/WR)
001C	000E	RT Status Word Register (RD)
001E	000F	RT BIT Word Register (RD)
CHANNEL 2		
0080	0000	Interrupt Mask Register (RD/WR)
0082	0001	Configuration Register #1 (RD/WR)
0084	0002	Configuration Register #2 (RD/WR)
0086	0003	Start/Reset Register (WR)
0086	0003	BC/RT Command Stack Pointer Register (RD)
0088	0004	BC control Word/RT Sub-address Control Word Register (RD/WR)
008A	0005	Time Tag Register (RD/WR)
008C	0006	Interrupt Status Register (RD)
…	…	…
009E	000F	RT BIT Word Register (RD)

Note: All PCI addresses are assumed to be **BYTE** offsets, all ACE addresses are assumed to be **WORD** offsets

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Brief Register Definition

A brief definition of the address mapping and accessibility for the ***BU-65549's*** 17 non-test registers, and the test registers can be found in the following paragraphs. For a more detailed description of the meaning and use of these registers, please refer to the ACE User's Guide.

INTERRUPT MASK REGISTER (TABLE 5 PAGE 31)

Used to enable and disable interrupt requests for various conditions. (RD/WR)

CONFIGURATION REGISTERS#1 (TABLE 6, PAGE 31) AND #2 (TABLE 7, PAGE 32)

Used to select the ***BU-65549's*** mode of operation, and for software control of RT Status Word Bits, Active Memory Area, BC Stop-on-Error, RT Memory Management mode selection, and control of the Time Tag operation. (RD/WR)

START/RESET REGISTER (TABLE 8 PAGE 32)

Used for "command" type functions, such as software reset, BC/MT Start, Interrupt Reset, Time Tag Reset, and Time Tag Register Test. The Start/Reset Register includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame. (WR)

BC/RT COMMAND STACK POINTER REGISTER (TABLE 9 PAGE 32)

This register points to the location where the current (prior to EOM) or next message will be stored in BC or RT modes. (RD)

BC CONTROL WORD/RT SUB-ADDRESS CONTROL WORD REGISTER (TABLE 10 PAGE 32, AND TABLE 11 PAGE 32)

In BC mode, this register provides host access to the current or most recent BC Control Word. The BC Control Word contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or 1553B error handling. In RT mode, this register allows host access to the current or most recent Sub-address Control Word. The Sub-address Control Word is used to select the memory scheme and enable interrupts for the current message. The read/write accessibility can be used as an aid for testing the ACE. (RD/WR)

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TIME TAG REGISTER (TABLE 12 PAGE 32)

Maintains the value of the real-time clock. The resolution of this register is programmable to a least significant bit weight of 2, 4, 8, 16, 32, or 64 µs/LSB. Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of RAM. (RD/WR)

INTERRUPT STATUS REGISTER (TABLE 13 PAGE 33)

The interrupt status register contains a Master Interrupt bit (bit 15) and a one-for-one copy of each of the bits in the interrupt mask. If an interrupt occurs, then the bit in the interrupt status register will be set. This register is automatically cleared if bit 4 of Configuration Register #2 is set. It allows the host processor to determine the cause of an interrupt request by means of a single READ operation. (RD)

CONFIGURATION REGISTERS#3 (TABLE 14 PAGE 33), #4 (TABLE 15 PAGE 33), AND #5 (TABLE 16 PAGE 33)

Used to enable many of the ***BU-65549's*** advanced features. These registers include all of the enhanced mode features; that is, all of the functionality beyond that of the previous generation product (the ***BUS-65529*** AIM/AIM-HY'er). For all three modes (BC/RT/MT), use of the Enhanced Mode enables the various read-only bits in Configuration Register #1.

For BC mode, the enhanced mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message.

For RT mode, the enhanced mode features include the expanded RT Block Status Word, the combined RT/Selective Message Monitor mode, and the internal wrapping of the "RTFAIL*" output signal to the "RTFLAG*" RT Status Word bit. The double-buffering scheme for individual receive (broadcast) sub-addresses, and the alternate (fully software programmable) RT Status Word are also provided by this register.

For MT mode, use of the enhanced mode enables the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

DATA STACK ADDRESS REGISTER (TABLE 17 PAGE 33)

The data stack address register points to the current address location in shared RAM that is used to store message words (second Command Words, Data Words, RT Status Words) in the Selective Word Monitor mode.

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FRAME TIME REMAINING REGISTER (TABLE 18 PAGE 34)

Provides a read only indication of the time remaining in the current BC frame. The resolution of this register is **100 µs/LSB**.

MESSAGE TIME REMAINING REGISTER (TABLE 19 PAGE 34)

Provides a read only indication of the time remaining before the start of the next message in BC frame. The resolution of this register is **1 µs/LSB**.

BC FRAME/RT LAST COMMAND/MT TRIGGER WORD REGISTER (TABLE 20 PAGE 34)

In BC mode, this register programs the BC frame time for use in the frame auto-repeat mode. The resolution of this register is **100 µs/LSB**, with a maximum range of **6.55 seconds**. In RT mode, this register stores the current (or most previous) 1553 Command Word that was processed by the ACE RT; in the Word Monitor mode, this register specifies a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

STATUS WORD REGISTER AND BIT WORD REGISTERS (TABLE 21 PAGE 34 AND TABLE 22 PAGE 34)

Provide read-only indications of the ***BU-65549's*** RT Status and BIT Words.

TEST MODE REGISTERS 0-7

These registers may be used to facilitate built-in testing of the ***BU-65549*** using the ACE test vectors and the program SELFTST4.EXE. This program is provided with the installation of the ACE Runtime Libraries (***BUS-69082*** and ***BUS-69083***).

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Table 5 - Interrupt Mask Register

(READ/WRITE 00h)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	RAM PARITY ERROR
13	BC/RT TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAILURE
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUB-ADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	STATUS SET/RT MODE CODE/MT PAT. TRIGGER
0(LSB)	END OF MESSAGE

Table 6 - Configuration Register #1

(READ/WRITE 01h)				
BIT	**BC FUNCTION (Bits 11-0 Enhanced Mode Only)**	**RT WITHOUT ALTERNATE STATUS**	**RT WITH ALTERNATE STATUS (Enhanced Mode Only)**	**MONITOR FUNCTION (Enhanced Mode Only, bits 12-0)**
15 MSB	RT/BC-MT* (Logic 0)	(Logic 1)	(Logic 1)	(Logic 0)
14	MT/BC-RT* (Logic 0)	(Logic 0)	(Logic 0)	(Logic 1)
13	CURRENT AREA B/A*	CURRENT AREA B/A*	CURRENT AREA B/A*	CURRENT AREA B/A*
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)
11	FRAME STOP-ON-ERROR	DYNAMIC BUS CONTROL ACCEPTANCE*	S10	TRIGGER ENABLED WORD
10	STATUS SET STOP-ON-MESSAGE	BUSY*	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	SERVICE REQUEST*	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	SUBSYSTEM FLAG*	S07	NOT USED
7	EXTERNAL TRIGGER EN	RTFLAG* (enhanced mode only)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER EN. ENABLED	NOT USED	S05	NOT USED
5	INTER-MESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLE/SINGLE* RETRY	NOT USED	S02	NOT USED
2	BC ENABLED (read only)	NOT USED	S01	MONITOR ENABLED (read only)
1	BC FRAME IN PROGRESS (read only)	NOT USED	S00	MONITOR TRIGGERED (read only)
0 LSB	BC MESSAGE IN PROGRESS (read only)	RT MESSAGE IN PROGRESS (enhanced mode only) (read only)	RT MESSAGE ON PROGRESS (read only)	MONITOR ACTIVE (read only)

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Table 7 - Configuration Register #2

(READ/WRITE 02h)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED INTERRUPTS
14	LOGIC “0"
13	BUSY LOOK UP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDARY DISABLE
9	TIME TAG RESOLUTION 2 (TTR2)
8	TIME TAG RESOLUTION 1 (TTR1)
7	TIME TAG RESOLUTION 0 (TTR0)
6	CLEAR TIME TAG ON SYNCHRONIZE
5	LOAD TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/PULSE* INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST
1	ENHANCED RT MEMORY MANAGEMENT
0(LSB)	SEPARATE BROADCAST DATA

Table 8 - Start/Reset Register

(WRITE 03h)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
…	…
7	RESERVED
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0(LSB)	RESET

Table 9 - BC/RT Command Stack Pointer Register

(READ 03h)	
BIT	**DESCRIPTION**
15(MSB)	COMMAND STACK POINTER 15
…	…
0(LSB)	COMMAND STACK POINTER 0

Table 10 - BC Control Word Register

(READ/WRITE 04h, not *BU-65170*)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	MESSAGE ERROR MASK (ME)
13	SERVICE REQUEST BIT MASK
12	SUBSYSTEM BUSY BIT MASK
11	SUBSYSTEM FLAG BIT MASK
10	TERMINAL FLAG BIT MASK
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/B*
6	OFF LINE SELF TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-TO-RT FORMAT

Table 11 - RT Sub-address Control Word

(READ/WRITE 04h)	
BIT	**DESCRIPTION**
15(MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

Table 12 - Time Tag Register

(READ 05h)	
BIT	**DESCRIPTION**
15(MSB)	TIME TAG 15
…	…
0(LSB)	TIME TAG 0

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Table 13 - Interrupt Status Register

(READ/WRITE 06h)	
BIT	**DESCRIPTION**
15(MSB)	MASTER INTERRUPT
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAILURE
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUB-ADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PAT. TRIG TRIGGER
0(LSB)	END OF MESSAGE

Table 14 - Configuration Register #3

(READ/WRITE 07h)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/R* ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER ENABLE
2	RTFAIL-FLAG WRAP ENABLE
1	1553A MODE CODES ENA
0(LSB)	ENHANCED MODE CODE HANDLING

Table 15 - Configuration Register #4

(READ/WRITE 08h)	
BIT	**DESCRIPTION**
15(MSB)	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BROADCAST MASK ENA/XOR*
10	RETRY IF -A AND M.E.
9	RETRY IF STATUS SET
8	1ST RETRY ALT/SAME* BUS
7	2ND RETRY ALT/SAME* BUS
6	VALID M.E./NO DATA
5	VALID BUSY/NO DATA
4	MT TAG GAP OPTION
3	LATCH RT ADDR WITH CONFIG #5
2	TEST MODE 2
1	TEST MODE 1
0(LSB)	TEST MODE 0

Table 16 - Configuration Register #5

(READ/WRITE 09h)	
BIT	**DESCRIPTION**
15(MSB)	12 MHZ CLOCK SELECT
14	LOGIC “0"
13	EXTERNAL TX INHIBIT A, read only 65170/61580X6
12	EXTERNAL TX INHIBIT B, read only 65170/61580X6
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	RT ADDR LATCH/TRANSPARENT*
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0(LSB)	RT ADDRESS PARITY

Table 17 - Monitor Data Stack Address Register

(READ/WRITE 0Ah)	
BIT	**DESCRIPTION**
15(MSB)	MONITOR DATA STACK ADDRESS 15
…	…
0(LSB)	MONITOR DATA STACK ADDRESS 0

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Table 18 - BC Frame Time Remaining Register

(READ/WRITE 0Bh)	
BIT	**DESCRIPTION**
15(MSB)	BC FRAME TIME REMAINING 15
…	…
0(LSB)	BC FRAME TIME REMAINING 0

NOTE: Resolution = 100 µs per LSB

Table 19 - BC Message Time Remaining Register

(READ 0Ch)	
BIT	**DESCRIPTION**
15(MSB)	BC MESSAGE TIME REMAINING 15
…	…
0(LSB)	BC MESSAGE TIME REMAINING 0

NOTE: Resolution = 1 µs per LSB

Table 20 - BC Frame Time/RT Last Command/MT Trigger Register

(READ/WRITE 0Dh)	
BIT	**DESCRIPTION**
15(MSB)	BIT 15
…	…
0(LSB)	BIT 0

Table 21 - RT Status Word Register

(READ 0Eh)	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPT
0(LSB)	TERMINAL FLAG

Table 22 - RT Bit Word Register

(READ 0Fh)	
BIT	**DESCRIPTION**
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	CHANNEL B/A*
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLES 23 To 26 are not registers, they are WORDS stored in RAM:

Table 23 - BC Mode Block Status Word

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

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Table 24 - RT Mode Block Status Word

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

Table 25 - Word Monitor Identification Word

BIT	DESCRIPTION
15(MSB)	GAP TIME
…	…
8	GAP TIME
7	WORD FLAG
6	THIS_RT*
5	BROADCAST*
4	ERROR
3	COMMAND/DATA*
2	CHANNEL B/A*
1	CONTIGUOUS DATA/GAP*
0(LSB)	MODE_CODE*

Table 26 - Message Monitor Mode Block Status Word

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

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THEORY OF OPERATION

The following sections describe the basic software architecture of the BC, RT, and MT modes of operation for the ***BU-65549***. For a more detailed description of the low-level operation of the 1553 interface please refer to the ACE User's Guide. In general, the explanation is for one of the ACE's on the board. All definitions can be extrapolated to the second ACE.

Bus Controller (BC) Architecture

The BC protocol of the ***BU-65549*** implements all MIL-STD-1553B message formats. The message format is programmable on a message-by-message basis by means of bits in the BC Control Word and the T/R* bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and interrupt requests may be enabled or disabled for each message. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The ***BU-65549's*** BC response timeout value is programmable with choices of 18, 22, 50, and 130 μs. The longer response timeout values allow for operation over long buses and/or the use of repeaters.

Figure 10 on page 36 illustrates BC message gap and frame timing. The ***BU-65549*** may be programmed to process BC frames of up to 512 messages with no processor intervention. It is also possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally using a programmable BC frame timer, or from an external trigger input. The internal BC frame time is programmable up to 6.55 seconds in increments of 100 μs. In addition to BC frame time the message gap time (defined as the start of the current message to the start of the next message) is programmable on an individual message basis. The time between individual successive messages is programmable up to 65.5 ms, in increments of 1 μs.

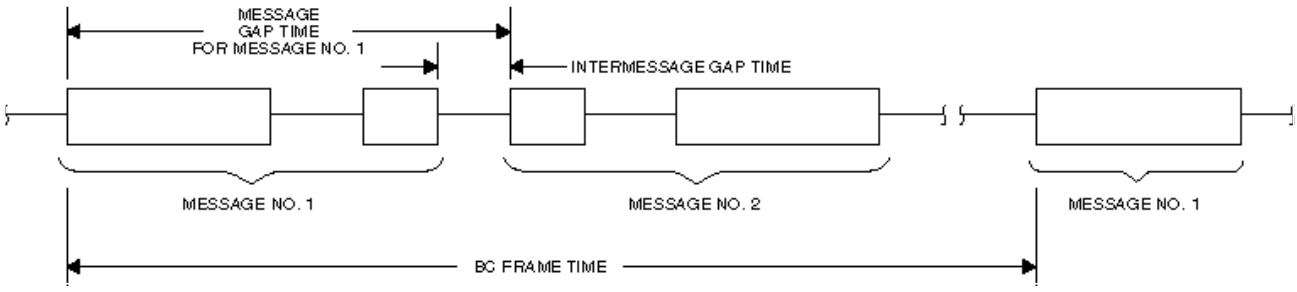


Figure 10 - BC Intermessage Gap and Frame Timing

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BC Memory Organization

Table 27 on page 38 illustrates a Typical BC Memory Map. It is important to note that the only fixed locations for the ***BU-65549*** in the Standard BC mode are the two Stack Pointers (offset locations 0100h and 0104h for each ACE) and the two Message Count locations (0101h and 0105h). Enabling the Frame Auto-Repeat mode will reserve four more memory locations for use in the Enhanced BC mode; these locations are used for the two Initial Stack Pointers (address locations 0102h and 0106h) and for the Initial Message Count locations (0103h and 0107h). The user is free to locate the Stack and BC Message Blocks anywhere else within the 64K x 16 shared RAM address space. For simplicity of illustration, assume allocation for the maximum length BC message for each message block in Table 27. The maximum size of a BC message block is 38 words for a RT-to-RT transfer of 32 Data Words (Control + 2 Commands + Loopback + 2 Status Words + 32 Data Words).

Note that this example assumes the disabling of the 256-word boundaries.

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Table 27 - Typical BC Memory Organization

ADDRESS (HEX) (see note 2)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101	Message Count A (fixed location)
0102	Initial Stack Pointer A (see note 1) (Auto-Frame Repeat Mode)
0103	Initial Message Count A (see note 1) (Auto-Frame Repeat Mode)
0104	Stack Pointer B (fixed location)
0105	Message Count B (fixed location)
0106	Initial Stack Pointer B (see note 1) (Auto-Frame Repeat Mode)
0107	Initial Message Count B (see note 1) (Auto-Frame Repeat Mode)
0108-012D	Message Block 0
012E-0153	Message Block 1
0154-0179	Message Block 2
. . .	. . .
0238-025D	Message Block 8
025E-025F	Not Used
0260-027F	Reserved For Registers
0280-02A5	Message Block 9
. . .	. . .
7EBE-7EE3	Message Block 846
7EE4-7EFF	Not Used
7F00-7FFF	Stack B

Notes:
1) Used only in the Enhanced BC mode with Frame Auto-Repeat enabled.
2) Address represents the word offset from the memory base address in the common memory address space.
3) The PCI address of ACE #1 is 00000, and the PCI address of ACE #2 is 20000

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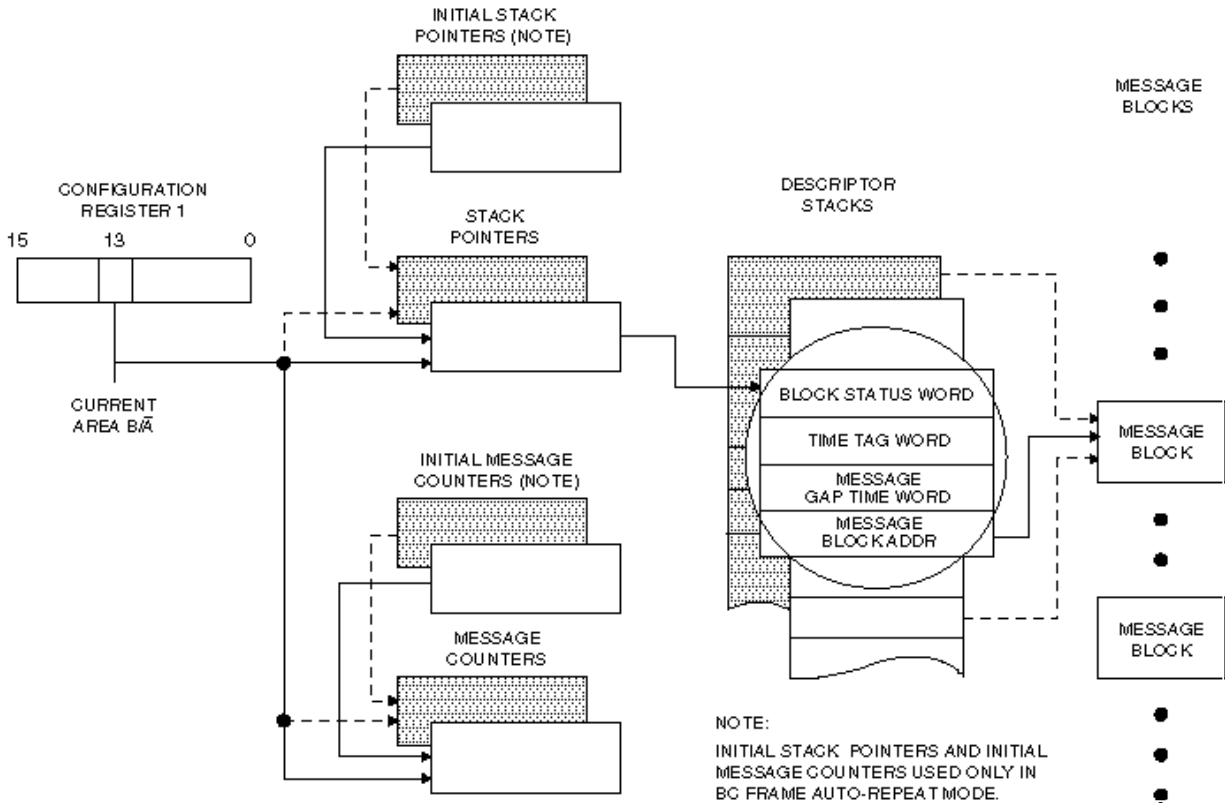


Figure 11 - BC Mode Memory Management

BC Memory Management

Figure 11 on page 39 illustrates the ***BU-65549's*** BC memory management scheme. One of the features of the BC memory management is the global double-buffering mechanism. This provides for two independent sets of the various BC mode data structures: Stack Pointer and Message Counter locations, Descriptor Stack areas, and BC message blocks. Bit 13 of Configuration Register #1 (Table 6, page 31) selects the current active area. At any point in time, the ***BU-65549's*** internal 1553-memory management logic may access only the "active" area data structures. Figure 11 on page 39 depicts the "active" and "inactive" areas by the non-shaded and shaded areas, respectively. At all times **both** the "active" and "inactive" areas are accessible by the host processor**.** In most applications, the host processor will access the "inactive" area, while the 1553 bus processes the "active" area messages.

The BC may be programmed to transmit multi-message frames of up to 512 messages. The number of messages to be processed is programmable by the Active Area Message Count location in the shared RAM (locations 0101h or 0105h), which is initialized by the host processor. In addition, the host processor must initialize the Active Area Stack Pointer (locations 0100h or 0104h). The Stack Pointer references the four-word message block descriptor

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in the Stack area of shared RAM for each message to be processed. The BC Stack size is programmable with choices of 256, 512, 1024, and 2048 words.

In the BC Frame Auto-Repeat mode, the host must load the Initial Stack Pointer and Initial Message Counter locations prior to the processing of the first frame. The single-frame mode does not use these two locations.

The third and fourth words of the BC block descriptor are the Message Gap Time and the Message Block Address for the respective message. The host processor must write these two memory locations prior to the start of message processing. Use of the Message Gap Time is **optional**. The Block Address pointer specifies the starting location for each message block. The first word of each BC message block is the BC Control Word.

At the start and end of each message, the Block Status and Time Tag Words are written to the message block descriptor in the stack. The Block Status Word provides indications of „message in process' or „message completion', bus channel, Status Set, response timeout, retry count, Status address mismatch, loop test (on-line self-test) failure, and other error conditions. Table 23 on page 34 illustrates the bit mapping of the BC Block Status word. The 16-bit Time Tag Word will reflect the current contents of the internal Time Tag Register. This read/write register, which operates for all three modes, has programmable resolution of from 2 μs/LSB to 64 μs/LSB. In addition, the Time Tag register may be clocked from an external source.

BC Message Block Formats and BC Control Word

In BC mode, the ***BU-65549*** supports all MIL-STD-1553 message formats. For each 1553 message format, the ***BU-65549*** mandates a specific sequence of words within the BC Message Block. This includes locations for the Control, Command and (transmitted) Data Words that are to be read from RAM by the BC protocol logic. In addition, subsequent contiguous locations must be allocated for storage of received Loopback, RT Status and Data Words. Table 28 on page 41 illustrates the organization of the BC message blocks for the various MIL-STD-1553 message formats. Note that for each message format, the BC Control Word is located in the first location of the message block.

For each of the BC Message Block formats, the first word in the block is the BC Control Word. The BC Control Word is not transmitted on the 1553 bus. Instead, it contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. The bit mapping and definitions of the BC Control Word are illustrated in Table 10 on page 32.

The BC Control Word is followed by the Command Word to be transmitted, and subsequently by a second Command Word (for a RT-to-RT transfer), followed by Data Words to be transmitted (for Receive commands). The location after the last word to be transmitted is reserved for the Loopback Word. The Loopback Word is an on-line self-test feature. The subsequent

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locations after the Loopback Word are reserved for received Status Words and Data Words (for Transmit commands).

Table 28 - BC Message Block Formats

BC-to-RT Transfer
Control Word
Receive Command Word
Data Word #1
Data Word #2
Last Data Word
Last Data Word Looped Back
Status Received

RT-to-BC Transfer
Control Word
Transmit Command Word
Transmit Command Looped Back
Status Received
Data Word #1
Data Word #2
Last Data Word

RT-to-RT Transfer
Control Word
Receive Command
Transmit Command
Transmit Command Looped Back
TX RT Status Word
Data #1
Data #2
Last Data
RX RT Status Word

Mode Code; No Data
Control Word
Mode Command Looped Back
Status Received

TX Mode Code With Data
Control Word
TX Mode Command
Mode Command Looped Back
Status Received
Data Word

RX Mode Code with Data
Control Word
RX Mode Command
Data word
Data Word Looped Back
Status Received

Broadcast
Control Word
Broadcast Command
Data #1
Data #2
. . .
Last Data
Last Data Looped Back

RT-to-RT (Broadcast) Transfer
Control Word
RX Broadcast Command
TX Command
TX command Looped Back
TX RT Status
Data #1
Data #2
. . .
Last Data

Broadcast Mode Code With no Data
Control Word
Broadcast Mode command
Broadcast Mode Command Looped Back

Broadcast Mode Code With Data
Control Word
Broadcast Mode Command
Data Word
Data Word Looped Back

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Automatic Retries

The ***BU-65549*** BC can be configured to implement automatic message retries. When enabled, retries will occur following response timeout or format error conditions. As an additional option, retries may be enabled when the Message Error Status Word bit is set by a 1553A RT or following a “Status Set” condition. For a failed message, either one or two message retries will occur. The bus channel that the retried message is to be sent on is independently programmable for the first and second retries. Retries may be enabled or disabled on an individual message basis.

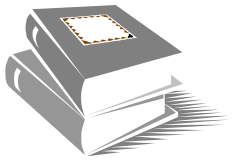
BC Interrupts

Setting the appropriate Interrupt Mask Register bits can enable BC interrupts. The definition of the individual bits is shown in Table 5 on page 31 and described in more detail in the „ACE User’s Guide’. The definition of “Status Set” is programmable on an individual message basis by means of the BC Control Word. This allows masking of the individual RT Status Word bits. The Interrupt Status Register will report that an interrupt has occurred by setting the appropriate bit. This will occur whether or not the interrupt mask register bit is set. If the mask register bit is not set, then the interrupt condition will not be reported via interrupt to the system.

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REMOTE TERMINAL (RT) ARCHITECTURE

The RT protocol design of the ***BU-65549*** represents DDC's fifth generation implementation of a 1553 RT. One of the salient features of the ACE's RT architecture is its true multi-protocol functionality. This includes programmable options for support of MIL-STD-1553A, the various McAir protocols, and MIL-STD-1553B Notice 2. The ***BU-65549*** RT response time is 2 to 5 µs dead time (4 to 7 µs per 1553B), providing compliance to all the 1553 protocols. Additional multi-protocol features of the ***BU-65549*** include options for full software control of RT Status and Built-in-Test (BIT) words. Alternatively, for 1553B applications, these words may be formulated in real-time by the ***BU-65549*** protocol logic.



The ***BU-65549*** RT protocol design implements all of the MIL-STD-1553B message formats and dual redundant mode codes. This design is based largely on previous generation products that have passed SEAFAC testing for MIL-STD-1553B compliance. The ACE RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. Other key features of the ***BU-65549*** RT include a set of interrupt conditions, internal command Illegalization, and programmable busy bit by sub-address.

All RT functions and addresses are described for one of the ACE terminals available on the ***BU-65549*** card. These capabilities can be implied for both of the ACE devices available on the card.

RT Memory Organization

Table 29 on page 44 illustrates a typical memory map for the ***BU-65549*** in RT mode. As in BC mode, the two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100h for the Area A Stack Pointer and address 0104h for the Area B Stack Pointer. Besides the Stack Pointer, for RT mode there are several other areas of the ACE address space designated as fixed locations. All RT modes of operation require the Area A and Area B Lookup Tables. There are also several fixed locations allocated for optional features such as Command Illegalization Lookup Table, Mode Code Selective Interrupt Table, Mode Code Data Table, and Busy Bit Lookup Table. It should be noted that optional fixed locations might be used for general purpose storage (data blocks) if they are not being used.

The RT Lookup tables provide a mechanism for mapping data blocks for Transmit, Receive, and Broadcast sub-addresses to separate areas in the RAM. These areas occupy fixed address range locations 014h0 to 01BFh for Area A and 01C0h to 023Fh for Area B. The RT lookup tables include Sub-address Control Words and the individual Data Block Pointers. If used, address range 0300h-03FFh will be dedicated as the illegalizing section of RAM. The actual Stack RAM area and the individual data blocks may be located in any of the non-fixed areas in the shared RAM address space.

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Table 29 - Typical RT Memory Map (shown for 12K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101-0103	RESERVED
0104	Stack Pointer B (fixed location)
0105-0107	RESERVED
0108-010F	Mode Code Selective Interrupt Table (fixed area)
0110-013F	Mode Code Data (fixed area)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-0247	Busy Bit Lookup Table (fixed area)
0248-025F	(not used)
0260-027F	Data Block 0
0280-02FF	Data Blocks 1-4
0300-03FF	Command Illegalizing Table (fixed area)
0400-041F	Data Block 5
0420-043F	Data Block 6
. . .	. . .
2FE0-2FFF	Data Block 356
3000-7FFF	Approximately 600 more data blocks (or monitor stacks)

Note: Address represents the WORD offset from the memory base address in the common memory address space.

RT Memory Management

Another salient feature of the ACE series products is the flexibility of its RT memory management architecture. The RT architecture allows the memory management scheme for each transmit, receive, or broadcast sub-address to be programmable on a sub-address basis. Also, in compliance with MIL-STD-1553B Notice 2, the ***BU-65549*** provides an option to separate data received from broadcast messages from non-broadcast received data.

Besides supporting a global double-buffering scheme (as in BC mode), the ACE RT provides a pair of 128-word Lookup Tables for memory management control, programmable on a sub-address basis (Table 30 on page 45). The 128-word table includes 32-word entries for transmit message pointers and receive message pointers. There is also a third, optional Lookup Table for broadcast message pointers, providing Notice 2 compliance, if necessary.

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The fourth section of each of the RT Lookup Tables stores the 32 Sub-address Control Words (Table 11 page 32 and Table 30 page 45). The individual Sub-address Control Words may be used to select the RT memory management option and interrupt scheme for each transmit, receive, and (optionally) broadcast sub-address.

For each transmit sub-address, there are two possible memory management schemes: (1) single message; and (2) circular buffer. For each receive (and optionally broadcast) sub-address, there are three possible memory management schemes: (1) single message; (2) double buffered; and (3) circular buffer. For each transmit, receive and broadcast sub-address, there are two interrupt conditions programmable by the respective Sub-address Control Word: (1) after every message to the sub-address or (2) after a circular-buffer rollover. An additional table in RAM may be used to enable interrupts following selected mode code messages.

When using the circular-buffer scheme for a given sub-address, the size of the circular buffer is programmable by three bits of the Sub-address Control Word (see Table 30 page 45). The options for circular buffer size are 128, 256, 512, 1024, 2048, 4096, and 8192 Data Words.

Table 30 - RT Look-up Tables and Sub-Address Control Word

RT Lookup Table			
AREA A	**AREA B**	**DESCRIPTION**	**COMMENT**
0140 … 015F	01C0 … 01DF	Rx(/Bcst)_SA0 … Rx(/Bcst)_SA31	Receive (/Broadcast) Lookup Table
0160 … 017F	01E0 … 01FF	Tx_SA0 … Tx_SA31	Transmit Lookup Table
0180 … 019F	0200 … 021F	Bcst_SA0 … Bcst_SA31	Broadcast Lookup Table (Optional)
01A0 … 01BF	0220 … 023F	SACW_SA0 … SACW_SA31	Sub-address Control Word Table (Optional)

Sub-Address Control Word Scheme				
MM2	**MM1**	**MM0**	**DESCRIPTION**	**COMMENT**
0	0	0	Single Message or Double Buffered	
0	0	1	128-Word	Circular Buffer of Specified Size
0	1	0	256-Word	
0	1	1	512-Word	
1	0	0	1024-Word	
1	0	1	2048-Word	
1	1	0	4096-Word	
1	1	1	8192-Word	

Note: Address represents the word offset from the memory base address in the common memory address space.

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SINGLE-MESSAGE MODE

Figure 12 on page 47 illustrates the RT Single-Message memory management scheme. When operating the ***BU-65549*** in default power up mode, the Single-Message scheme is implemented for **all** transmit, receive, and broadcast sub-addresses. In the Single-Message mode (also in the Double- and Circular-Buffer modes), there is a global double-buffering scheme, controlled by bit 13 of Configuration Register #1. This selects one of the two sets of the various data structures shown in the figure: the Stack Pointers (fixed addresses), Descriptor Stacks (user defined addresses), RT Lookup Tables (fixed addresses), and RT Data Word blocks (user defined addresses). Figure 12, Figure 13, and Figure 14 delineate the "active" and "inactive" areas by the non-shaded and shaded areas, respectively.

As shown, the ACE stores the Command Word from each message received, in the fourth location within the message descriptor (in the stack) for the respective message. The T/R* bit, sub-address field, and (optionally) broadcast/own address, index into the active area Lookup Table, to locate the data block pointer for the current message. The ***BU-65549*** RT memory management logic then accesses the data block pointer to locate the starting address for the Data Word block for the current message. The maximum size for a RT Data Word block is 32 words.

For a particular sub-address in the Single-Message mode, the data blocks for receive/broadcast sub-addresses will be overwritten, and the transmit sub-addresses will be overread. In the single-message mode, it is possible to access multiple data blocks for the same sub-address. This, however, requires the intervention of the host processor to update the respective Lookup Table pointer.

To implement a data wraparound sub-address, as required by Notice 2 of MIL-STD-1553B, the Single-Message scheme should be used for the wraparound sub-address. Notice 2 recommends sub-address for this requirement.

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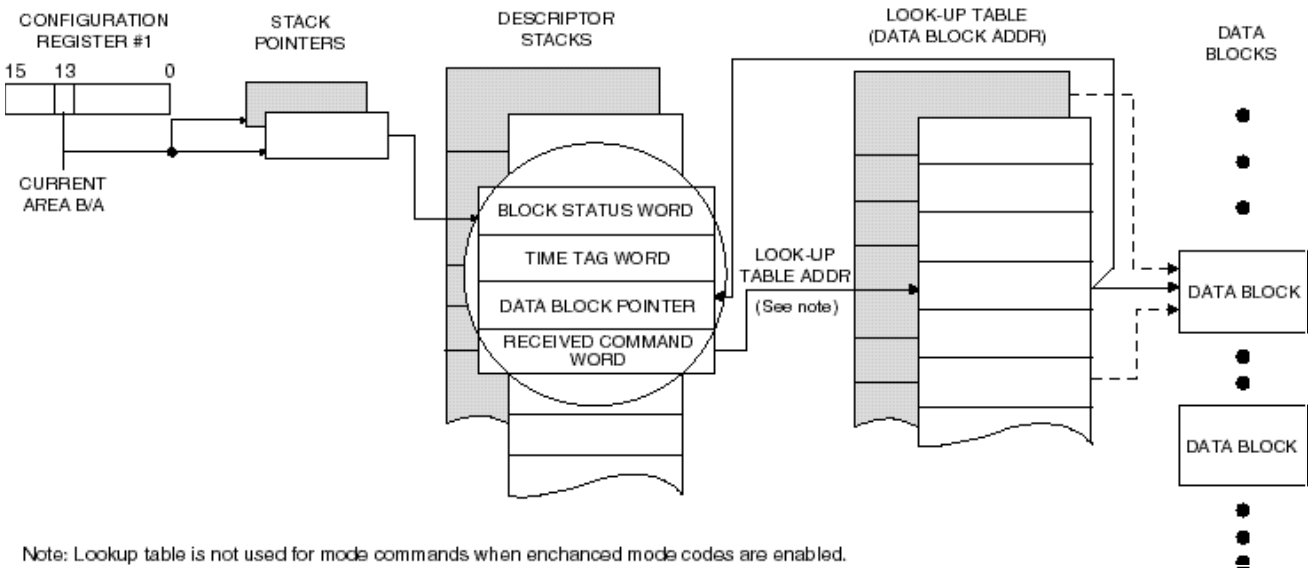


Figure 12 - RT Memory Management: Single-Message Mode

CIRCULAR-BUFFER MODE

Figure 13 on page 48 illustrates the „RT circular-buffer„ management scheme. The circular-buffer mode facilitates bulk data transfers. The size of the RT circular buffer, shown on the right side of the figure, is programmable from 128 to 8192 words (in even powers of 2) for the respective Sub-address Control Word. As in the single-message mode, the host processor initially loads the individual Lookup Table entries. At the start of each message, the ACE stores the Lookup Table entry in the third position of the respective message block descriptor in the stack area of RAM. The ACE transfers Receive or Transmit Data Words through this buffer, starting at the location referenced by the Lookup Table pointer.



At the end of a valid (or, optionally, invalid) message, the value of the Lookup Table entry is automatically updated to the next location following the last address accessed for the current message. As a result, data words for the next message directed to the same sub-address will be accessed from the next contiguous block of address locations within the circular buffer. As a recommended option, the Lookup Table pointers may be programmed to **not** update following an invalid receive (or broadcast) message. This allows the 1553 bus controller to retry the failed message, resulting in the valid (retried) data overwriting the invalid data. This eliminates overhead for the RT's host processor. When the pointer reaches the lower boundary of the circular buffer (located at 128, 256, . . . 8192 word boundaries in the ***BU-65549*** address space), the pointer moves to the top boundary of the circular buffer, as shown in Figure 13.

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Implementing Bulk Data Transfers

The use of the Circular-Buffer scheme is ideal for bulk data transfers. A bulk data transfer is defined as multiple messages to/from the same sub-address. The recommendation for such applications is to enable the circular-buffer interrupt request. By so doing, the routine transfer of multiple messages to the selected sub-address, **including errors and retries,** is transparent to the RT's host processor. By strategically initializing the sub-address Lookup Table pointer prior to the start of the bulk transfer, the ***BU-65549*** may be configured to issue an interrupt request only after it has received the anticipated number of valid Data Words to the designated sub-address.

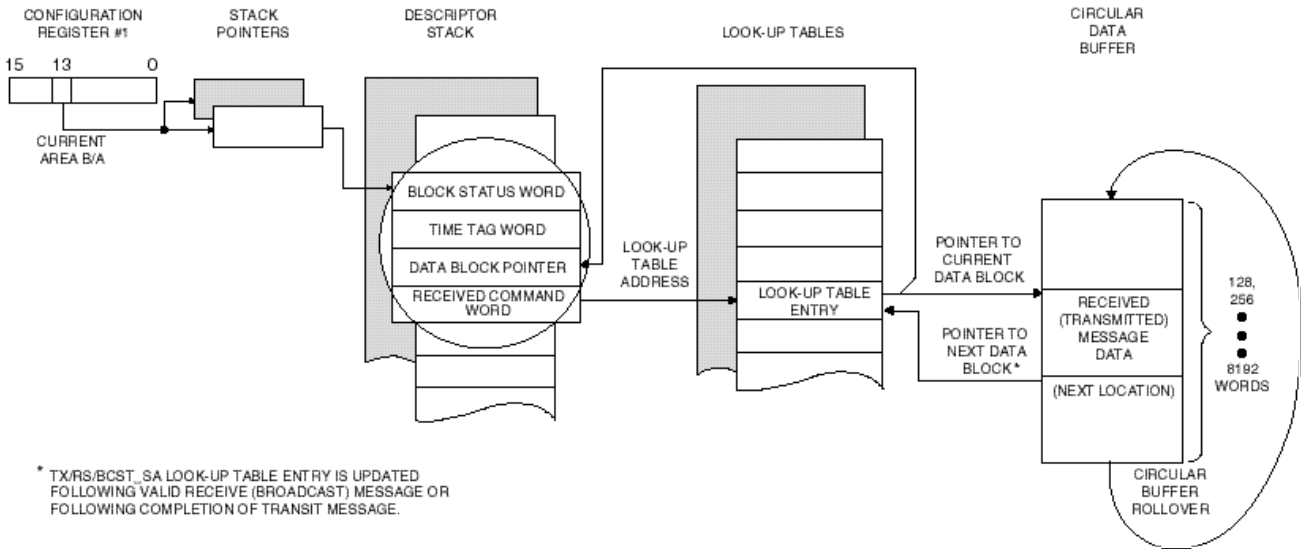


Figure 13 - RT Memory Management: Circular-Buffered Mode

SUB-ADDRESS DOUBLE-BUFFERING MODE

For receive (and broadcast) sub-addresses, the ***BU-65549*** RT offers a third memory management option, Sub-address Double Buffering. This mode provides a means of ensuring data consistency. Figure 14 on page 49 illustrates the RT Sub-address Double-Buffering scheme. Like the Single-Message and Circular-Buffer modes, the Double-Buffering mode may be selected on a sub-address basis by means of the Sub-address Control Word. The purpose of the Double-Buffering mode is to provide the host processor a convenient means of accessing the most recent, valid data received by a given sub-address. This serves to ensure the highest possible degree of data consistency by allocating **two** data blocks of 32 words for each individual receive (and/or broadcast) sub-address.

At any point in time, one of the two blocks will be designated as the "active" 1553 data block while the other will be designated as the "inactive" block. The Data Words from the next receive message to that sub-address will be stored

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by the ACE into the "active" block. Upon completion of the message, provided that the message was valid and Sub-address Double Buffering is enabled, the ***BU-65549*** will automatically switch the "active" and "inactive" blocks for the respective sub-address. The ACE accomplishes this by toggling bit 5 of the sub-address Lookup Table Pointer and rewriting the pointer. As a result, the most recent valid block of received Data Words will always be readily accessible to the host processor. As a means of ensuring data consistency, the host processor is able to reliably access the most recent valid, received Data Word block by performing the following sequence:

- Disable double buffering for the respective sub-address by the Sub-address Control Word by temporarily switching the sub-address memory management scheme to the Single-Message mode.
- Read the current value of the receive (or broadcast) sub-address Lookup Table pointer. This points to the "active" Data Word block. By inverting bit 5 of this pointer value, it is possible to locate the start of the "inactive" Data Word block. This block will contain the Data Words received during the most recent valid message to the sub-address.
- Read out the words from the "inactive" Data Word Block.
- Re-enable the Double-Buffering mode for the respective sub-address by accessing the Sub-address Control Word.

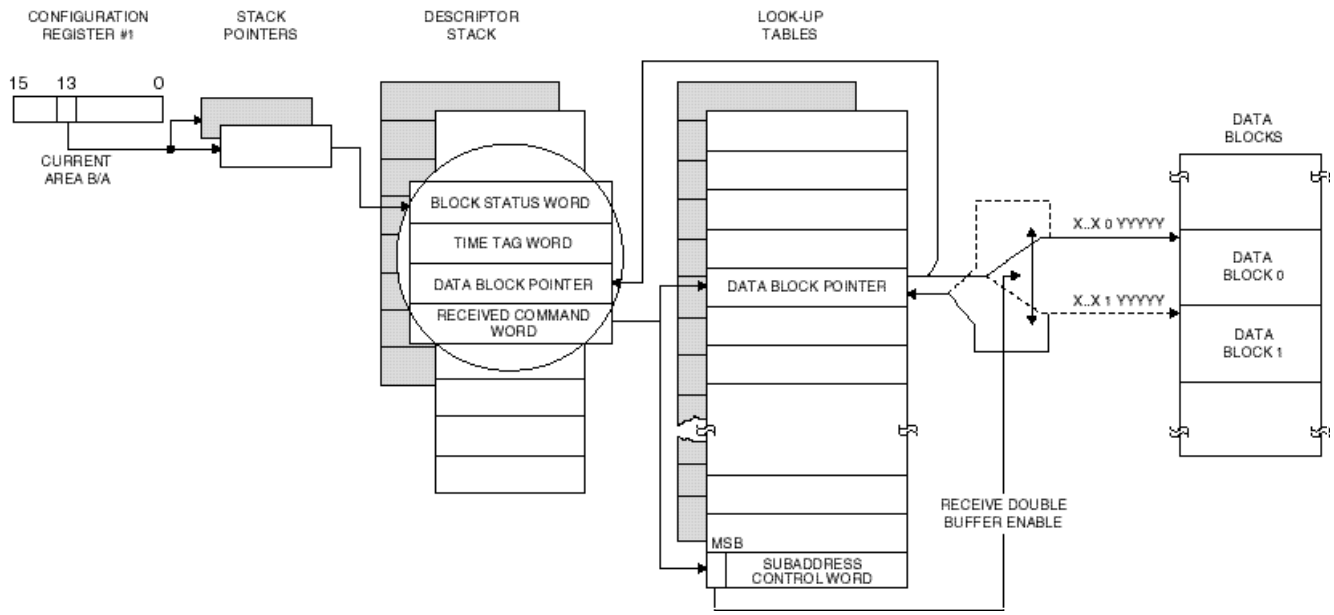


Figure 14 - RT Memory Management: Sub-address Double-Buffering Mode

RT Interrupts

As in BC mode, the ***BU-65549*** RT provides many interrupts that may be masked. RT interrupt conditions include „End of Message', Message Error, Selected Sub-address (Sub-address Control Word) Interrupt, Circular-Buffer Rollover, Selected Mode Code Interrupt, and Stack Rollover.

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Descriptor Stack

At the beginning and end of each message, the ***BU-65549*** RT updates the four-word message descriptor in the active area stack. The RT stack size is programmable, with choices of 256, 512, 1024, and 2048 words. Figure 12, Figure 13, and Figure 14 show the four words: Block Status Word, Time Tag Word, Data Block Pointer, and the 1553 received Command Word. The RT Block Status Word includes indications of message in-progress or message complete, bus channel, RT-to-RT transfer and RT-to-RT transfer errors, message format error, loop test (self-test) failure, circular-buffer rollover, illegal command, and other error conditions. Table 24 on page 35 shows the bit mapping of the RT Block Status Word.

As in BC mode, the Time Tag Word stores the current contents of the ***BU-65549's*** Time Tag Register. The resolution of the Time Tag Register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. The Time Tag counter may be incremented from an external source or via software command.

The third entry in the Descriptor Stack is a pointer to the Data Block area that the message was written to. The ACE fills this entry with the contents of the Lookup Table location for the current message. This serves as a convenience in locating stored message data blocks.

The ACE stores the full 16-bit 1553 Command Word in the fourth location of the RT message descriptor.

RT Command Illegalization

The ***BU-65549*** provides an internal mechanism for RT command illegalization. In addition, there is a means to allow the Busy bit in the Status Word to be enabled for only a programmed subset of the transmit/receive/broadcast sub-addresses.

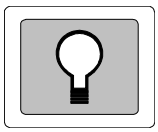
The illegalization scheme uses a 256-word area in the ***BU-65549's*** address space. A benefit of this feature is the reduction of printed circuit board requirements, by eliminating the need for an external PROM, PLD, or RAM device that does the illegalizing function. The ***BU-65549's*** illegalization scheme provides maximum flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/R* bit, sub-address, and word count/mode code to be illegalized. Another advantage of the RAM-based illegalization technique is that it provides for a high degree of self-test ability.

ADDRESSING THE ILLEGALIZATION TABLE

Table 31 on page 52 illustrates the addressing scheme of the illegalization RAM. As shown, the base address of the illegalizing RAM is word address 0300 (hex) in the shared RAM. The ACE formulates the index into the

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Illegalizing Table based on the values of BROADCAST/OWN ADDRESS*, T/R* bit, Sub-address, and the MSB of the Word Count/Mode Code field (WC/MC4) of the current Command Word. When the value created from this combination is added to offset address 0x0300, the 16-bit word will represent the legalizing bits for the 16 high or low word possibilities for the specific word count. For example, if it is desired to make word count 22 illegal for a non-broadcast, transmit message to RT address 10 and sub-address 5, but all other word counts legal, value 0x0040 would be programmed into location 0x03CB.



BROADCAST*/OWN = 1
T/R* = 1
SUB-ADDRESS = 00101
WORD COUNT MSB = 1
Word count 22 is located at the 7th bit position = 0x0040
Offset address = 0x0300 + 0x00CB = 0x03CB

The internal RAM has 256 words reserved for command illegalization. Broadcast commands may be illegalized separately from non-broadcast receive commands and mode commands.

Commands may be illegalized down to the word count level. For example, a one-word receive command to sub-address 1 may be defined as legal, while a two-word receive command to sub-address 1 may be defined as illegal.

The first 64 words of the Illegalization Table refer to broadcast receive commands (two words per sub-address). The next 64 words refer to broadcast transmit commands. Since non-mode code „broadcast transmit' commands are by definition invalid, this section of the table (except for sub-addresses 0 and 31) does **not** need to be initialized by the user. The next 64 words correspond to non-broadcast receive commands. The final 64 words refer to non-broadcast transmit commands. Messages with Word Count/ Mode Code (WC/MC) fields between 0 and 15 may be defined as illegal by setting the corresponding data bits for the respective even-numbered address locations in the illegalization table. Likewise, messages with WC/MC fields between 16 and 31 may be illegalized by setting the corresponding data bits for the respective odd-numbered address locations in the illegalization table.

The following should be noted with regards to command illegalization:

- To illegalize a particular word count for a given broadcast/own address*, T/R*, sub-address, the appropriate bit position in the respective illegalization word should be set to logic 1. A bit value of logic 0 designates the respective Command Word as a legal command. The ***BU-65549*** will respond to an illegalized non-broadcast command with the Message Error bit set in its RT Status Word.

- For sub-addresses 00001 through 11110, the "WC/MC" field specifies the Word Count field of the respective Command Word. For sub-addresses

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00000 and 11111, the “WC/MC” field specifies the Mode Code field of the respective Command Word.

- Since non-mode code broadcast transmit messages are not defined by MIL-STD-1553B, the 60 words in the illegalization RAM, addresses 0342h through 037Dh, corresponding to these commands do not need to be initialized. The ***BU-65549*** will **not** respond to a non-mode code broadcast transmit command, but will automatically set the Message Error bit in its internal Status Register, regardless of whether or not a corresponding bit in the illegalization RAM has been set. If the next message is a Transmit Status or Transmit Last Command mode code, the ***BU-65549*** will respond with its Message Error bit set.

Table 31 - Illegalizing Ram Address Definition

BIT	DESCRIPTION
15(MSB)	0
14	0
13	0
12	0
11	0
10	0
9	1
8	1
7	BROADCAST*/OWN ADDRESS
6	T/R*
5	SA4
4	SA3
3	SA2
2	SA1
1	SA0
0(LSB)	WC4/MC4

Programmable Busy

As a means of providing compliance with Notice 2 of MIL-STD-1553B, the ***BU-65549*** RT provides a software controllable means for setting the Busy Status Word bit as a function of sub-address. By using a Busy Lookup Table in the ***BU-65549*** address space, it is possible to set the Busy bit based on command broadcast/own address, T/R* bit, and sub-address. Refer to „Addressing The Illegalization Table’ on page 50 for calculating the table address. Another programmable option allows received Data Words to be either stored or not stored for messages when the Busy bit is set.

Other RT Functions

The ***BU-65549*** allows the RT address to be programmed by the host processor. There are also options for the RT FLAG Status Word bit to be set under software control and automatically following a failure of the loop back

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self-test. Other software controllable RT options include software programmable RT Status and RT BIT words, automatic clearing of the Service Request Status Word bit following a Transmit Vector Word mode command, and the capability to clear and load the Time Tag Register following receipt of Synchronize mode commands. Options regarding Data Word transfers for the Busy and Message Error (Illegal) Status Word bits, and for handling of 1553A and reserved mode codes may also be programmed within the RT.

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MONITOR (MT) ARCHITECTURE

The ***BU-65549*** provides three bus monitor (MT) modes:

- The default „Word Monitor' mode.
- A Selective Message Monitor mode.
- A Simultaneous Remote Terminal/Selective Message Monitor mode.

Besides providing monitor filtering based on RT Address, the T/R* bit, and Sub-address, the Selective Message Monitor eliminates the need to determine the start and end of messages by software. This mode will automatically process the signals it sees on the bus as messages, and store the message information in the command and data stacks for easy retrieval.

Word Monitor

In the Word Monitor mode, the ***BU-65549*** monitors both 1553 buses. After initializing the Word Monitor and putting it on-line the ***BU-65549*** stores all Command, Status, and Data Words received from both buses. For each word received from either bus, the ***BU-65549*** stores a pair of words in RAM. The first word is the 16 bits of data from the received word. The second word is the Monitor Identification (ID), or "Tag" word. The ID Word contains information relating to bus channel, sync type, word validity, and inter-word time gaps. The ***BU-65549*** stores data and ID words in a circular buffer in the shared RAM address space. Table 25 on page 35 shows the bit mapping for the Monitor ID word.

MONITOR TRIGGER WORD

There is a Trigger Word Register that provides additional flexibility for the Word Monitor mode. The ***BU-65549*** stores the value of the 16-bit Trigger Word in the MT Trigger Word Register. The contents of this register represent the value of the Trigger Command Word. The ***BU-65549*** has programmable options to start or stop the Word Monitor, and to issue an interrupt request following receipt of the Trigger Command Word from the 1553 bus.

Selective Message Monitor Mode

The ***BU-65549*** Selective Message Monitor provides features to greatly reduce the software and processing burden of the host CPU. The Selective Message Monitor implements selective monitoring of messages from a dual 1553 bus, with the monitor filtering based on the RT Address, T/R* bit, and Sub-address fields of received 1553 Command Words. The Selective Message Monitor mode greatly simplifies the host processor software by distinguishing between Command and Status Words. The Selective Message Monitor maintains two stacks in the ***BU-65549*** RAM: a Command Stack and a Data Stack.

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SIMULTANEOUS RT/MESSAGE MONITOR MODE

The Selective Message Monitor may function as a purely passive monitor or may be programmed to function as a simultaneous RT/Monitor. The RT/Monitor mode provides complete Remote Terminal (RT) operation for the ***BU-65549's*** programmed RT address and bus monitor capability for the other 30 non-broadcast RT addresses. This allows the ***BU-65549*** to simultaneously operate as a full function RT and "snoop" on all or a subset of the bus activity involving the other RT's on the bus. This operation is possible for both of the ACE devices on the ***BU-65549***. This type of operation is sometimes needed to implement a backup bus controller. The combined RT/Selective Monitor maintains three stack areas in the ***BU-65549*** address space: a RT Command Stack, a Monitor Command Stack, and a Monitor Data Stack. The pointers for the various stacks in each of the ACE devices have fixed locations in the ***BU-65549*** address space.

SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION

Table 32 on page 56 illustrates a typical memory map for the ACE in the Selective Message Monitor mode. This mode of operation defines several fixed locations in the RAM. These locations are allocated in a manner that is compatible with the combined RT/Selective Message Monitor mode. The fixed memory map consists of two Monitor Command Stack Pointers (location 0102h and 0106h), two Monitor Data Stack Pointers (locations 0103h and 0107h), and a Selective Message Monitor Lookup Table (0280h-02FFh) based on RT Address, T/R*, and sub-address. The memory assignment assumes a Monitor Command Stack size of 1K words, and a Monitor Data Stack size of 2K words.

Refer to Figure 15 on page 57 for an illustration of the Selective Message Monitor operation. Upon receipt of a valid Command Word, the ***BU-65549*** will reference the Selective Monitor Lookup Table (a fixed block of addresses) to check for the condition (disabled/enabled) of the current command. If disabled, the ***BU-65549*** will ignore (and not store) the current message; if enabled, the ***BU-65549*** will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer.

Similar to RT mode, The ACE stores a Block Status Word, 16-bit Time Tag Word, and Data Block Pointer in the Message Descriptor, along with the received 1553 Command Word following reception of the Command Word. The ACE writes the Block Status and Time Tag Words at both the start and end of the message. The Monitor Block Status Word contains indications of message in-progress or message complete, bus channel, Monitor Data Stack Rollover, RT-to-RT transfer and RT-to-RT transfer errors, message format error, and other error conditions. Table 26 (page 35) shows the Message Monitor Block Status Word. The Data Block Pointer references the first word stored in the Monitor Data Stack (the first word following the Command Word) for the current message. The ***BU-65549*** will then proceed to store the subsequent words from the message [possible second Command Word, Data

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Word(s), Status Word(s)] into consecutive locations in the Monitor Data Stack.

The size of the Monitor Command Stack is programmable to 256, 1K, 4K, or 16K words. The Monitor Data Stack size is programmable to 512, 1K, 2K, 4K, 8K, 16K, 32K, or 64K words.

Monitor interrupts may be enabled for Monitor Command Stack Rollover, Monitor Data Stack Rollover, and/or End-of-Message conditions. In addition, in the Word Monitor mode there may be an interrupt enabled for a Monitor Trigger condition.

Table 32 - Typical Selective Message Monitor Memory Map (shown for 12K RAM)

ACE ADDRESS OFFSET (HEX)	DESCRIPTION
0000-0101	Not Used
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack A (fixed location)
0104-0105	Not Used
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-027F	Not Used
0280-02FF	Selective Monitor Lookup Table (fixed area)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0BFF	Monitor Command Stack B
0C00-0FFF	Not Used
1000-1FFF	Monitor Data Stack A
2000-2FFF	Monitor Data Stack B

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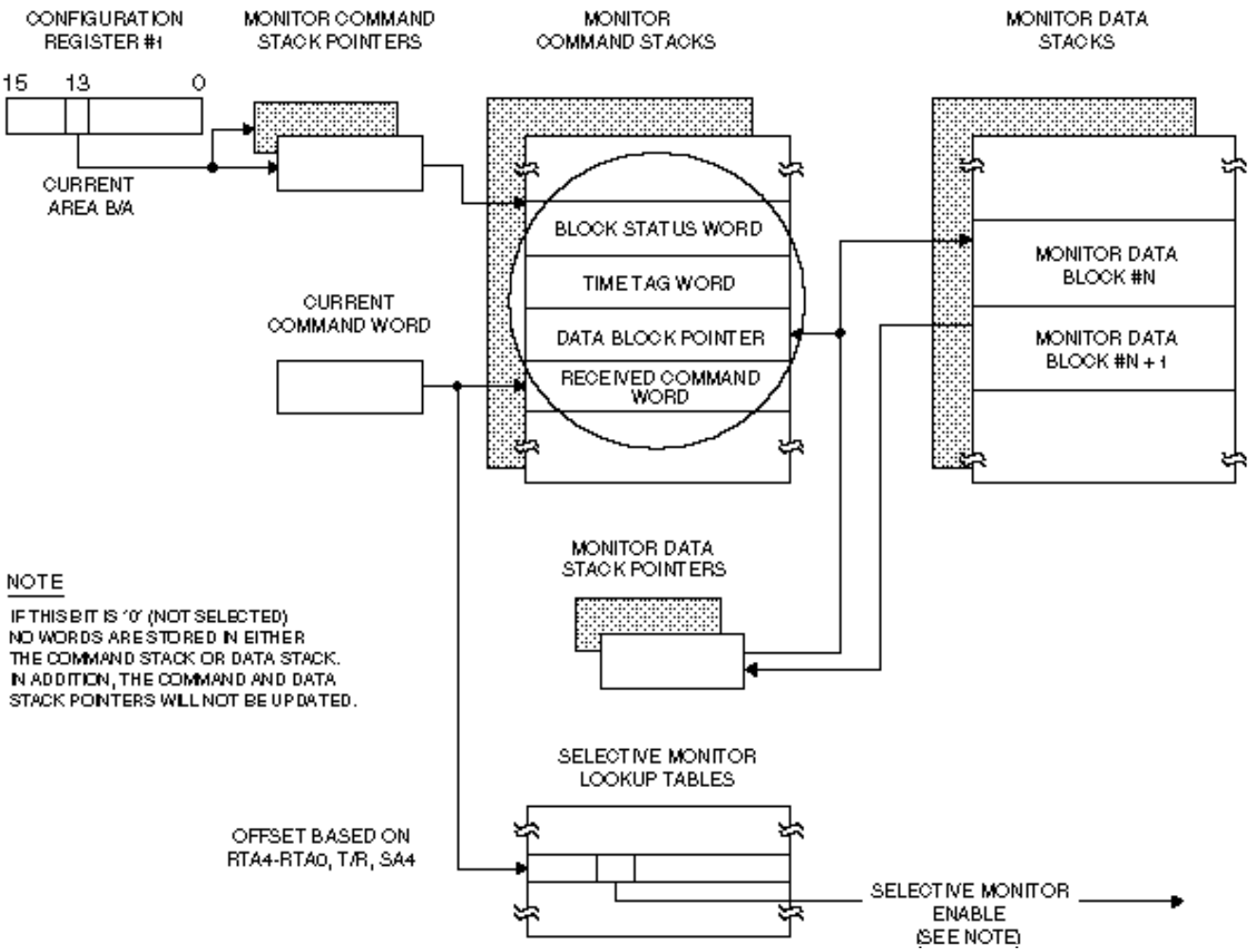


Figure 15 - Selective Message Monitor Memory Management

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Table 33 - Specification Table

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATINGS				
V_{CC} Supply Voltage	-0.3	5.0	7.0	V
RECEIVER				
Threshold Voltage, Transformer Coupled	0.200		0.860	V_{P-P}
Common-Mode Voltage (Note 3)			10	V_{PEAK}
TRANSMITTER				
Differential Output Voltage				
• Direct Coupled Across 35 ohms	6	7	9	V_{P-P}
• Transformer Coupled Across 70 ohms	18	21	27	V_{P-P}
Output noise, Differential (Direct Coupled)			10	$mV_{P-P\ dif}$
Output Offset Voltage, Transformer Coupled Across 70	-250		250	mV
Rise/Fall Time	100	150	300	nsec.
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
• +5 V	4.5		5.5	V
+5v Current Drain (BU-65549M1-300)				
Idle			0.500	A
25% Transmitter Duty Cycle			0.650	A
50% Duty Cycle			0.800	A
100% Duty Cycle			1.100	A
+5V Current Drain (BU-65549M2-300)				
Idle			0.800	A
25% Transmitter Duty Cycle			1.100	A
50% Duty Cycle			1.400	A
100% Duty Cycle			2.000	A
POWER DISSIPATION				
Total PC Card, BU-65549M1-300				
• Idle			2.515	W
• 25% Duty Cycle			3.250	W
• 50% Duty Cycle			4.000	W
• 100% Duty Cycle			5.500	W
Total PC Card, BU-65549M2-300				
• Idle			4.000	W
• 25% Duty Cycle			5.500	W
• 50% Duty Cycle			7.000	W
• 100% Duty Cycle			10.00	W
1553 MESSAGE TIMING				
RT Response Time (Note 1)	4		7	µs
Completion of CPU Write (BC Start-to-Start of first BC Message)		2.5		µs
1553 MESSAGE TIMING				
BC Intermessage Gap (Note 2)		9.5		µs
BC/RT/MT Response Timeout (Note 4)				
• 18.5 nominal	17.5	18.5	19.5	µs
• 22.5 nominal	21.5	22.5	23.5	µs
• 50.5 nominal	49.5	50.5	51.5	µs
• 128.0 nominal	127	128	129	µs
Transmitter Watchdog Timeout		668		µs
THERMAL				
Operating Temperature	0		55	°C
Storage Temperature	-20		65	°C
PHYSICAL CHARACTERISTICS				
Size		6.875 X 4.200 (172.72 X 106.68)		in (mm)
Weight		5.6 (159)		oz (g)

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Table 33 notes:

(1) Typical value for minimum intermessage gap time. Under software control, may be lengthened to 65,535 μs minus message time (in increments of 1 μs).

(2) Software programmable (4 options). Includes RT-to-RT Timeout (measured Mid-Parity of Transmit Command to Mid-Sync of Transmitting RT Status).

(3) Assumes a common-mode voltage within the frequency range of dc to 2Mhz, applied to pins of the isolation transformer on the stub side (either direct or transformer coupled), referenced to hybrid ground. Use a DDC recommended transformer or other transformer that provides an equivalent minimum CMRR.

(4) Software programmable (4 options). Includes RT-to-RT Timeout (Mid-Parity of Transmit Command to Mid-Sync of Transmitting RT Status).

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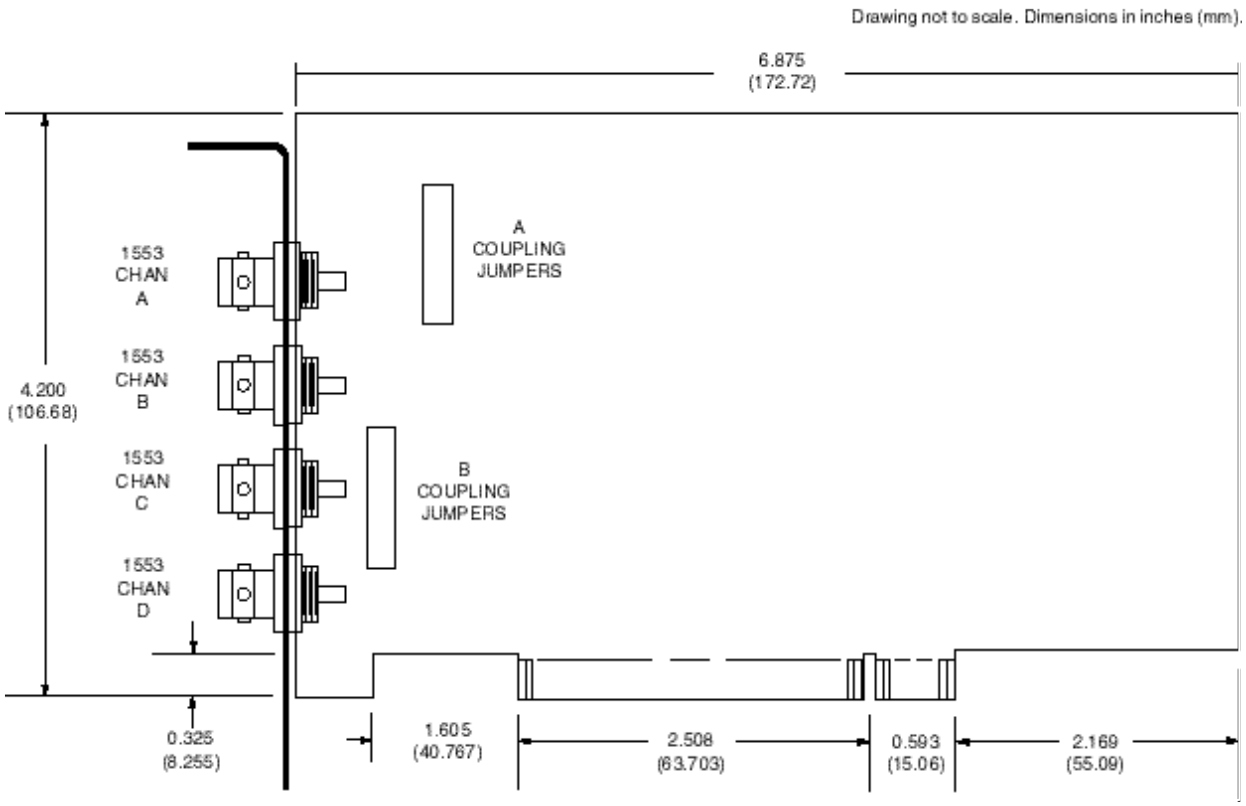


Figure 16 - Mechanical Outline Drawing

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GLOSSARY

SEAFAC Testing

Testing performed by a US Government Agency located at Wright-Patterson Air Force Base. This testing validated the operation of military systems, including the 1553 data links. This testing is no longer performed.

Active

The active areas of the ACE memory are those locations that are currently available for use by the ACE. There are some situations, such as Double-Buffered RT messages, where one buffer is for use by the ACE, while the other buffer is designated for use by the Host CPU.

Bus Coupling

The coupling mode of a bus may be either direct or transformer coupled. Direct-coupled terminals will have an isolation transformer at the 1553 terminal, and must be no greater than 1 foot from the 1553 bus. A transformer-coupled terminal will have an isolation transformer at the 1553 terminal, a transformer coupler at the bus, and my be connected to the bus with no more that 20 feet of 1553 bus cable.

Driver

This is the lower level software that provides access to the hardware. Windows NT and Windows 95 applications must use this level of software to access the hardware. The drivers for the ***BU-65549*** are supplied with the card and installed according to the installation instructions.

Enumeration

Enumeration is the process that BIOS performs to determine the identification and resource requirements of all PCI devices that are used in the computer. Many of these PCI devices are not plug-in cards. They could be the disk driver controller, timers, memory bridges, etc.

ESD

Electrostatic Discharge (ESD) is caused by a potential difference in the static charge (accumulated electrons) between two objects. This is most commonly identified by an emitted spark when the two objects are moved into close proximity. Under normal conditions, the voltage potential needed to create a spark of 1 centimeter in air is 25000 volts. Obviously the generated spark will cause major catastrophic damage to many of the parts used on the ***BU-65549*** board, but the spark is not the only cause of ESD damage. If the potential difference between an object and the conductive wires of the ***BU-65549*** or

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any of the semiconductor devices is large enough (e.g., greater than 1000 volts), damage will be caused to the devices without the generation of a spark.

Inactive

The inactive areas of ACE memory are those locations that are designated for use by the Host CPU. These areas will not be written or read by the ACE device until the Host CPU releases them by toggling the applicable area control bit. This would be bit 15 of the Sub-address control word in the case of double-buffered RT messages.

RTL

The Runtime Library supplies the programming API (Application Programming Interface) to access the ***BU-65549*** software functions. When these functions are used in a C program, compiled and linked with the proper library file (ACE4.LIB) an executable file will be created that can be used to operate the ***BU-65549***.

Side Effects

When used in reference to ACE access, side effects are defined as unexpected actions to a performed operation. This can be seen in the access of the Interrupt Status Register. The ACE can be configured to clear this register when it is read. This would be known as a side effect. If the host CPU tries to access this register, and it is read, but the PCI transfer is halted, the CPU will have to try the read again. The second time it reads this register it will have been cleared by the previous read, and therefore report erroneous data.

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APPENDIX A – REFERENCES

PCI System Architecture

Third Edition, copyright © 1995 by MindShare, Inc. Written by Tom Shanley and Don Anderson. Published by Addison-Wesley Publishing Company

ACE User's Guide

ACE Series BC/RT/MT Advanced Communication Engine Integrated 1553 Terminal User's Guide, Data Device Corporation, Revision J.

ACE Runtime Library Software Manual

Data Device Corporation, Revision D

MIL-STD-1553 Designer's Guide

Data Device Corporation, Sixth Edition

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