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ACE/Mini-ACE Series BC/RT/MT
Advanced Communication Engine
Integrated 1553 Terminal User's Guide

BU-65170, BU-61580, BU-61585, BU-61590,
BU-65178, BU-61588, BU-65179, BU-61688,
BU-61689, BU-61582 (BU-63825), BU-61583
(BU-63925), BU-65620 and BU-65621
(#MN-65170XX-001)

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CHANGE RECORD

REV	DATE	PAGES	COMMENTS
J	02/99	B-4 - B-8	Transformer Specifications updated
J-1	03/99	355, 356	Typo correction: Figures 81 and 82 reversed
J-2	06/28/99	252	Table 80 updated
J-3 (Initial release to DDF-72671)	03/03	23, 51, 53, 103, 136, 213, 214, 224, 257, 281, 350, B-2-8, F4	Corrections to bit 4 description, corrections to address 101 in Table 43, corrections to bit 0 in Table 54a, updated isolation transformers sections, updated fiber optic section, corrected Figure 32, corrected Figure 46, updated pin listings, typo in Appendix F.
K	03/04	All	Converted to MS Word format, updated BETA transformer details, corrected CPU Writing RAM/Reg (Transparent mode) timing diagram and table, corrected CPU Reading RAM/Reg (Transparent mode) timing table, updated order info/DDC processing table, modified transmit last command and circular buffer mode descriptions in RT operation section, modified bus monitor architecture description in Functional overview section, updated gull wing and flat pack Mini-ACE mechanical outlines, tables and figures renumbered as needed.
L	05/05	212, 213	Modified Figure 21 Graphic, Modified para in “Simulated Bus” (Lab Bench) Interconnections
M	06/07	122, 215	Added warning and note under figure 11. Changed (c) under figure 21.
N	04/08	All	Extensive changes due to SP’ACE and SP’ACE II.
P	05/09	2	Added paragraph about the BU-63825(925) (Sp’ACE II). Updated general layout of manual.
R	11/10		Updated Tables 114, 115, 128, 129, & 130, and Figures 62, 63, & 64, updated notes for Tables 114 & 115

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1 PREFACE

This manual uses typographical conventions to assist the reader in understanding the content. This section will define the text formatting used in the rest of the manual.

1.1 Text Usage

- **BOLD** – text that is written in bold letters indicates important information and table, figure, and chapter references.
- ***BOLD ITALIC*** – will designate DDC Part Numbers.
- `Courier New –` is used to indicate code examples.

<…> - Indicates user entered text or commands.

1.2 SPECIAL HANDLING AND CAUTIONS



The ***ACE/Mini-ACE series*** uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.

1.3 SPECIAL NOTES

Unless otherwise noted, an asterisk after a signal name (i.e., MSTCLR*) denotes an active low signal.

1.4 TRADEMARKS

All trademarks are the property of their respective owners.

1.5 Technical Support

In the event that problems arise beyond the scope of this manual, you can get in touch with DDC by calling:

Customer support:

1-800-DDC-5757, ext. 7771

Headquarters:

1-631-567-5600, ext. 7771

Fax: 1-631-567-5758 to the attention of DATA BUS Applications.

Regional Offices:

USA & Canada:

East of the Mississippi River:

Tel: (631) 567-5600 Fax: (631) 567-7358

West of the Mississippi River:

Tel: (714) 895-9777 Fax: (714) 895-4988

Europe:

Tel: 44 (1635) 811140 Fax: 44 (1635) 32264

Asia/Pacific:

Tel: 81 (3) 3814-7688 Fax: 81 (3) 3814-7689

DDC also has an Internet World Wide Web site, which allows customers to easily download new revisions of software and documentation. The Internet address is **www.ddc-web.com**.

2 OVERVIEW

2.1 ACE and Mini-ACE/Mini-ACE Plus FEATURES

- Fully Integrated 1553A/B Notice 2, STANAG 3838 Interface Terminal
- Small Ceramic Package
- RT or BC/RT/MT in Same Footprint
- Flexible Processor/Memory Interface
  - 8- or 16-Bit Buffered
  - 16-Bit Transparent
  - 16-Bit DMA
  - Supports "Zero Wait" Interface
- 4K, 8K, 12K, 64K(Mini-ACE Plus) Words of Internal RAM, Externally Expandable to
  64K x 16
- Transceiver Options
  - +5V Only (BU-65170X3; BU-61580X3; BU-65178/79X3; BU-61588X3; BU-61688/89X3; 63825X3; 63925X3)
  - +5V, -15V (BU-65170X1; 61580X1; 61582X1; 63825X1)
  - +5V, -12V (BU-65170X2; 61580X2; 61583X1; 63925X1)
  - Universal (McAir/1553): +5V, ±12V to ±15V (BU- 61590X5)
  - Transceiverless (BU-65620X0/Digital Monolithic; BU-65178X0; BU-61588X0)
  - 20Vpp Minimum Output Stub Voltage for MIL-STD-1760 Applications
- Advanced BC Features
  - Automatic Retries
  - Programmable Gap Times
  - Frame Auto-Repeat
  - Programmable Response Time-out
- Advanced RT Features
  - Programmable Command Illegalization
  - Choice of Single Message, Double Buffering, and Circular Buffering
  - Interrupts on Individual Mode Codes
  - BUSY Bit Programmable by Subaddress
  - Boot up as RT with BUSY Bit Set for MIL-STD-1760 Applications (BU-65179)
- Advanced Monitor Features
  - Word Monitor
  - Selective Message Monitor

  - Simultaneous RT/Message Monitor
  - Trigger Options

- Option for Radiation Hardening and Space Level Screening

2.2 DESCRIPTION

DDC's ACE series of terminals (See Table XX) comprise a complete integrated interface between a host processor and MIL-STD-1553 bus, providing complete multiprotocol support of MIL-STD-1553A/B/McAir and STANAG 3838.

The ACE series terminal provides the ultimate flexibility in interfacing to a host processor and internal/external RAM while minimizing board space and "glue" logic.

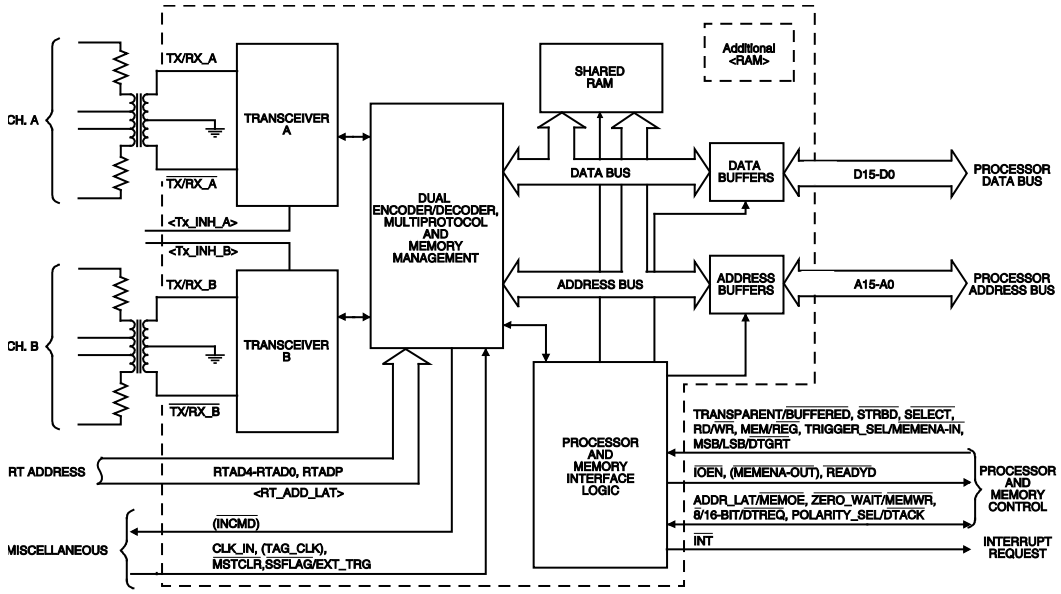
The advanced functional architecture of ACE series terminals incorporates a multiplicity of architectural enhancements, allowing for flexible operation while offloading the host processor, ensuring data consistency, and supporting bulk data transfers.

The entire ACE series of terminals incorporate protocol, memory management and processor interface logic. Most feature dual-redundant, integrated transceivers as well as varying amounts of internal buffered RAM with multiple packaging options.

Ordering options include operation over the full military temperature range of -55°C to +125°C, MIL-PRF-38534C screening, and +5 volt (only), +5/-15V, or +5/-12V transceivers, making these terminals ideal for demanding military and industrial processor-to-1553 applications

The BU-63825/925 Space Advanced Communication Engine (Sp'ACE II) is a radiation hardened version of the BU-61580/81 ACE terminal providing both functional and software compatibility with the standard BU-61580/81 product in the same 1.9 $inch^2$ package footprint.

TABLE 1. ACE Terminals					
Part Number	**Family**	**Functional Capability**	**Clock**	**RAM**	**Package**
BU-65170	ACE	RT-Only	12/16	4K x 16	1.9 in²
BU-65171	ACE	RT-Only w/ RT_LATCH	12/16	4K x 16	1.9 in²
BU-61580	ACE	BC/RT/MT	12/16	4K x 16	1.9 in²
BU-61581	ACE	BC/RT/MT w/ RT_LATCH	12/16	4K x 16	1.9 in²
BU-61585	ACE	BC/RT/MT	12/16	4K x 16	1.9 in²
BU-61586	ACE	BC/RT/MT w/ RT_LATCH	12/16	8K x 17	1.9 in²
BU-61582/63825	Sp'ACE / Sp'ACE II	BC/RT/MT	12/16	16K x 16	1.9 in²
BU-61583/63925	Sp'ACE / Sp'ACE II	BC/RT/MT w/ RT_LATCH	12/16	16K x 16	1.9 in²
BU-65620	ACE Monolithic	BC/RT/MT	12/16	4K x 16	2.48 in²
BU-65621	Sp'ACE Monolithic	BC/RT/MT	12/16	None	0.9025 in²
BU-61590	Universal Terminal	BC/RT/MT	12/16	4K x 16	3.78 in²
BU-61592	Universal Terminal	BC/RT/MT	12/16	8K x 16	3.78 in²
BU-65178	Mini-ACE	RT-Only	12/16	4K x 16	1.0 in²
BU-61588	Mini-ACE	BC/RT/MT	12/16	4K x 16	1.0 in²
BU-65179	Mini-ACE+	RT-Only w/ RT_BOOT	10/12/16/20	4K x 16	1.0 in²
BU-61688	Mini-ACE+	BC/RT/MT	12/16	64K x 16	1.0 in²
BU-61689	Mini-ACE+	BC/RT/MT	10/20	64K x 16	1.0 in²



( ) denotes not available on the Mini-ACE and Mini-ACE Plus.

< > denotes only available on transceiverless SP'ACE/SP'ACE II, ACE and SP'ACE digital monolithics, and all Mini-ACE series hybrids.

FIGURE 1. ACE/Mini-ACE SERIES BLOCK DIAGRAM

3 FUNCTIONAL OVERVIEW

DDC's ACE/Mini-ACE series of Integrated BC/RT/MT hybrids provide a complete, flexible interface between a microprocessor and a MIL-STD-1553A, B Notice 2, McAir, or STANAG 3838 bus, implementing Bus Controller (BC), Remote Terminal (RT) and Monitor Terminal (MT) modes. Packaged in a single 1.9 square inch 70-pin DIP, surface mountable flat pack, or J-lead package, the BU-65170 and BU-61580 ACE series terminals contain dual low-power transceivers and encoder/decoders, complete BC/RT/MT multi-protocol logic, memory management and interrupt logic, 4K x 16 of shared static RAM and a direct, buffered interface to a host processor bus (refer to block diagram, FIGURE 1). The BU-61585 is identical to the BU-61580, except it contains an additional 8K x 17 of internal RAM. The BU-61590, packaged in a 1.8 x 2.1 inch ceramic plug-in or flat pack package, includes a 1553/McAir "Universal" transceiver to provide compliance to both MIL-STD-1553 and McAir standards. The BU-65620, packaged in a 1.575 inch square PGA or 1.01 inch square flat pack, is a digital monolithic that can be used for fiber optic (MIL-STD-1773) applications. The BU-61582 (BU-63825) is radiation hardened version of the BU-61580.

In addition to smaller packaging, the 1.0 square inch 72-pin quad flat pack, 81-pin grid array, or 72-pin gull lead, the Mini-ACE series terminals add additional features such as 4K (BU-65178/61588/65179) or 64K (BU-61688/61689) words of internal RAM, 10/20 MHz operation (BU-65179/61689), and RT Boot-up mode with BUSY bit set (BU-65179) for MIL-STD-1760 applications.

The ACE/Mini-ACE terminals contain internal address latches and bidirectional data buffers to provide a direct interface to a host processor bus. The ACE/Mini-ACE may be interfaced directly to both 16-bit and 8-bit microprocessors in a buffered shared RAM configuration. **(Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)** In addition, the ACE/Mini-ACE may connect to a 16-bit processor bus via a Direct Memory Access (DMA) interface. The ACE includes 4K words of buffered RAM (64K words buffered RAM available in specific models of Mini-ACE series hybrids). Alternatively, the ACE/Mini-ACE may be interfaced to as much as 64K words of external RAM in either the shared RAM or DMA configurations.

The ACE/Mini-ACE RT mode is multiprotocol, supporting MIL-STD-1553A, MIL-STD-1553B Notice 2, and STANAG 3838 (including EFAbus). In addition, the BU-61590 "Universal" ACE supports the McAir A3818, A5232, and A5690, General Dynamics, and Grumman protocols. The memory management scheme for RT mode provides an option for separation of broadcast data, and programmable BUSY by

Subaddress, in compliance with 1553B Notice 2. Both double buffer and circular buffer options are programmable by subaddress. These features serve to ensure data consistency and to off-load the host processor for bulk data transfer applications.

The ACE/Mini-ACE series implements three monitor modes: a word monitor, a selective message monitor, and a combined RT/selective monitor.

Other features include options for automatic retries and programmable intermessage gap for BC mode, an internal Time Tag Register, an Interrupt Status Register and internal command illegalization for RT mode.

3.1 TRANSCEIVERS

The transceiver front end of the BU-65170/61580X1(X2) ACE hybrids is implemented by means of low-power bipolar analog monolithic and thick-film hybrid technology. The transceiver requires +5V and -15V (-12V) only (no +15V/+12V is required) and includes voltage source transmitters. The voltage source transmitters provide superior line driving capability for long cables and heavy amounts of bus loading. In addition, the monolithic transceivers in the BU-65170/61580D1 provide a minimum stub voltage level of 20 volts peak-to-peak transformer coupled, making them suitable for MIL-STD-1760 applications. Refer to specification table for a listing of ACE/Mini-ACE part numbers that meet 1760 requirements of 20 volts minimum.

The 5-volt dual transceiver front end of the BU-65170/61580X3(X6) and Mini-ACE terminals are implemented by means of fully monolithic transceiver chips. Besides requiring a very low idle current and eliminating the need for an additional power supply, the use of a 5-volt (only) transceiver entails the use of step-up, rather than step-down, isolation transformers. This provides the advantage of a higher terminal input impedance than is possible for a 15-volt or 12-volt transceiver. As a result, there is greater margin for the input impedance test, mandated for 1553 validation testing. This allows for longer cable lengths between an LRU's system connector and the isolation transformers of an embedded 1553 terminal. The receiver sections of the ACE/Mini-ACE series terminals are fully compliant to MIL-STD-1553B in terms of overvoltage protection, threshold, common mode rejection, and bit error rate.

The BU-61590 incorporates a thick-film transceiver capable of fulfilling the sinusoidal transmitter requirements of the McAir A3818, A5690, and A5232 protocols. The power supply requirements for the BU-61590 are +5V and ±12V to ±15V.

The ACE/Mini-ACE receiver sections are fully compliant with MIL-STD-1553B in terms of front end overvoltage protection, threshold, common mode rejection, and word error rate. In addition, the receiver filters and threshold circuits have been designed for optimal operation with the ACE/Mini-ACE's Manchester II decoders.

3.2 J' DIGITAL MONOLITHIC

The J' digital monolithic represents the cornerstone element of the ACE family of terminals. The development of the J' chip represented the fifth generation of 1553 protocol and interface design for DDC. Over the years, DDC's 1553 protocol and interface design has evolved from: (1) discrete component sets, consisting of multiple hybrids (with a large number of chips inside the hybrids) and programmable logic devices, to (2) multiple custom ASICs to perform the functions of encoder/decoder and RT protocol within a single hybrid, to (3) the BUS-61553 Advanced Integrated Mux Hybrid (AIM-HY) series, containing, in addition to a dual monolithic/thick film transceiver and discrete RAM chips, a custom protocol chip and a separate custom memory management/processor interface chip; (4) the BUS-61559 Advanced Integrated Mux Hybrids with Enhanced RT Features (AIM-HY'er); the AIM-HY'er series includes memory management and processor interface functions beyond those of the AIM-HY series; (5) the full integration of the J' chip.

The J' chip consists of: dual encoder/decoder, complete protocol for Bus Controller (BC), 1553A/B/McAir Remote Terminal (RT), and Monitor (MT) modes; memory management and interrupt logic; a flexible, buffered interface to a host processor bus and optional external RAM; and 4K words of on-chip RAM. Reference FIGURE 1. In addition to realizing **all** of the protocol, memory management and interface functions of the earlier AIM-HY'er series, the J' chip includes a large number of enhancements to facilitate hardware and software design, and to further off-load the 1553 terminal's host processor.

The BU-61580, BU-61581, BU-65170, BU-65171, BU-61585, BU-61586, BU-61590, and BU-65620 make use of the J' monolithic. The BU-61582 (BU-63825), BU-61583 (BU-63925), and BU-65621, on the other hand, are based on the J-Rad (M-Rad) monolithic. The J-Rad chip is actually a radiation hardened version of the J' monolithic. As such, the J-Rad possesses all the enhanced hardware and software features of the ACE. The M-Rad chip features a J-Rad "compatibility" mode.

3.3 DECODERS

The default mode of operation for the ACE terminals requires a 16 MHz clock input. If needed, a software programmable option allows the device to be operated from a 12 MHz clock input. Most current 1553 decoders sample using a 10 MHz or 12 MHz clock. In the 16 MHz mode (default following a hardware or software reset), the ACE decoders sample 1553 serial data using the 16 MHz clock. In both the 12 MHz and the 16 MHz modes, the decoders can be programmed to sample using **both** clock edges; this provides a sampling rate of 32 MHz or 24 MHz. The faster sampling rate for the J s Manchester II decoders provides superior performance in terms of bit error rate and zero-crossing distortion tolerance.

The default mode of operation for the Mini-ACE series terminals varies depending on the model purchased. The default mode for the BU-65178, BU-61588, and BU-61688 requires a 16 MHz clock input. If needed, a software programmable option allows the device to be operated from a 12 MHz clock input. The default mode for the BU-61689 requires a 20 MHz clock input. If needed, a software programmable option allows the device to be operated from a 10 MHz clock input. For the Mini-ACE series terminals, the decoders will always sample using both clock edges for superior bit error rate and zero-crossing distortion tolerance.

Lastly, the BU-65179 Mini-ACE Plus RT-only terminal expands the decoding clock selection capability even further by enabling the user to pin select between 10, 12, 16, 20 MHz operation. As in other Mini-ACE series terminals, the decoders will always sample using both clock edges for superior bit error rate and zero-crossing distortion tolerance.

For interfacing to fiber optic transceivers for MIL-STD-1773 applications, the transceiverless BU-65620P0(F0) can be used. These versions provide a pin programmable option for a **direct** interface to the single-ended outputs of a fiber optic receiver. No external logic is needed.

3.4 INTERNAL TIME TAGGING

The ACE/Mini-ACE series includes an internal read/writable Time Tag Register. The time tag register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 µs per LSB. The Time Tag Register may also be incremented by means of an external clock oscillator (not available on Mini-ACE/Mini-ACE Plus terminals). Another option allows the Time Tag Register to be incremented under software control. This supports self-test for the Time Tag Register.

For each message processed, the value of the Time Tag Register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for BC, RT, and Message Monitor modes.

For RT mode, additional options are provided to clear the Time Tag Register following a Synchronize (without data) mode command or load the Time Tag Register following a Synchronize (with data) mode command. Another option enables an interrupt request and a bit in the Interrupt Status Register to be set when the Time Tag Register rolls over from FFFF to 0000. Assuming the Time Tag Register is not loaded or reset, this will occur at approximately 4-second time intervals, for 64 us/LSB resolution, down to 131 ms intervals, for 2 us/LSB resolution.

Another programmable option for RT mode is that the Service Request Status Word bit can be automatically cleared following the ACE/Mini-ACE's response to a Transmit Vector Word mode command.

3.5 INTERRUPTS

The ACE/Mini-ACE series components provide a number of programmable options for interrupt generation and handling. The interrupt output pin ($\overline{\text{INT}}$) has two software programmable modes of operation. The interrupt output may be a pulse or a level output that is cleared under software control. In addition, for the BU-61590 and BU-65620, the level output may be cleared by the interrupt acknowledge input ($\overline{\text{IACK}}$).

Individual interrupts are enabled using the Interrupt Mask Register. The host processor may easily determine the cause of the interrupt through the use of the Interrupt Status Register. The Interrupt Status Register provides the current state of the interrupt conditions. The Interrupt Status Register may be updated in two ways. In the standard interrupt handling mode, a particular bit in the Interrupt Status Register will be updated only if the condition exists **and** the corresponding bit in the Interrupt Mask Register is enabled. In the enhanced interrupt handling mode, a particular bit in the Interrupt Status Register will be updated if

the condition exists regardless of the contents of the corresponding Interrupt Mask Register bit. The enhanced interrupt handling mode allows the host processor to define high priority conditions that will generate an interrupt, and low priority conditions that will be flagged but will not generate an interrupt.

3.6 CLOCK INPUT

The ACE terminals require an external 16 MHz or 12 MHz clock input. The clock frequency is software programmable. The Mini-ACE series terminals require an external 20, 16, 12, or 10 MHz clock input depending on the specific terminal purchased. All internal timing is derived from this clock. The short-term and long-term accuracy requirements of the input clock frequency must support 1 MHz data transmission in compliance with MIL-STD-1553B (or MIL-STD-1553A).

3.7 PROCESSOR INTERFACE

The ACE/Mini-ACE series terminals provide a variety of configurations for interfacing to a host processor and external RAM. These configurations are listed as follows:

1) 16-bit buffered mode

2) 16-bit transparent mode

3) 8-bit buffered mode. (Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode.) One enhancement for the ACE/Mini-ACE 8-bit and 16-bit buffered modes allows for direct interfacing to processors that do not have a "wait state" (strobe/acknowledge) type of handshake. The Intel 8051 8-bit microcontroller series and Analog Device's ADSP-2101 DSP processor are examples of these.

4) 16-bit DMA mode. The DMA type of interface saves P.C. board space for some applications by allowing the ACE terminals to interface directly to external system RAM and a processor, without requiring external buffers.

3.8 MEMORY MANAGEMENT ARCHITECTURE

The ACE/Mini-ACE terminals incorporate complete memory management and processor interface logic. For all three modes, a stack area of RAM is maintained. In BC mode, the stack allows for the scheduling of multimessage frames; for all three modes, the stack provides a real-time chronology of all messages processed. In addition to the stack processing, the memory management logic performs storage, retrieval and manipulation functions involving pointer and message data structures for all three modes.

3.9 BUS CONTROLLER ARCHITECTURE

The ACE/Mini-ACE Bus Controller (BC) provides a number of advanced architectural features. One of the enhanced BC features of the ACE/Mini-ACE series terminals is programmable intermessage gap time. This allows the BC intermessage gap to be programmed from a minimum of approximately 16 µs (the value for BUS-61559) up to 65.535 ms, in increments of 1 µs.

A second salient feature for BC mode is the implementation of automatic retries. Retries may be enabled or disabled on a message-by-message basis. There are three fixed retry conditions: response timeout, format error and Status Set. The Status Set retry is programmable on an individual message basis, by means of seven masking bits in the BC Control Word. In addition, a retry may be enabled for a MIL-STD-1553A RT if the Message Error bit is set. The same masking bits are also used in defining a Status Set interrupt request. Either one or two retries may be attempted. There are six selectable retry schemes: same bus, alternate bus, same bus/same bus, same bus/alternate bus, alternate bus/same bus, and alternate bus/alternate bus.

Other BC features include automatic frame repetition with a programmable frame time, an external trigger input, programmable response timeout, interrupts for any message(s) and 1553A/B mode selection, on an individual message basis.

3.10 REMOTE TERMINAL ARCHITECTURE

The ACE/Mini-ACE series RT incorporates a number of advanced features. A major attribute of the ACE/Mini-ACE series RT is its multiprotocol functionality. This includes programmable options for support of MIL-STD-1553A, MIL-STD-1553B, and the McAir A3818, A5232, and A5690 protocols. The RT response time will be 2 to 5 µs dead time, providing compliance to 1553A/B and McAir. Additional

multiprotocol features of the ACE series include fully programmable Built-In-Test (BIT) and RT Status Words.

The ACE/Mini-ACE provides a number of programmable options for RT mode memory management. In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from nonbroadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block, a double buffered configuration (two alternating Data Word blocks), or a variable-sized (128 to 8192 words) circular buffer may be allocated for data storage. In addition to helping ensure data consistency, the circular buffer feature provides a means of greatly reducing host processor overhead for bulk data transfer applications.

The double buffering mode for individual receive subaddresses serves to ensure data consistency of received data blocks. By making use of this feature, the host processor can easily access the most recent, complete received block of valid Data Words for any given subaddress.

End-of-message interrupts may be enabled either globally, following error messages, on a Tx/Rx/Bcst-subaddress and/or mode code basis, or when any particular Tx/Rx/Bcst-subaddress circular buffer reaches its lower boundary. An interrupt status register allows the host processor to determine the cause of all interrupts by means of a single READ operation.

The ACE/Mini-ACE terminals implement internal command illegalization for RT mode. The internal illegalization eliminates the need for an external PROM, PLD or RAM device. The illegalization scheme allows for any subset of the 4096 possible combinations of broadcast/own address, $T/\overline{R}$ bit, subaddress and word count/mode code to be illegalized.

The ACE/Mini-ACE RT also has a programmable option allowing the Busy bit to be set in the RT Status word as a function of broadcast, $T/\overline{R}$ bit and subaddress. The ACE/Mini-ACE RT provides options for requesting interrupts following messages for individual mode codes as well as for storing Data Words for the various mode codes in separate RAM locations.

3.11 BUS MONITOR ARCHITECTURE

The ACE/Mini-ACE provides three different bus monitor modes: (1) a Word Monitor, (2) a Selective Message Monitor, and (3) a combined RT/Selective Message Monitor mode. The Selective Message Monitor supports message filtering, based on RT Address/$T/\overline{R}$ bit/Subaddress, and provides separate Command Stacks and Data Stacks. The

RT/Selective Monitor mode provides full RT capability for the ACE/Mini-ACE terminal's own RT address plus selective monitoring for all other RT addresses.

When using the Enhanced Mini-ACE runtime library some post processing is performed which merges the discrete RT and MT stacks into a combined RT/MT stack that contains all selectively monitored activity on the 1553 data bus. For more information on this operation see the BU-69090 Enhanced Mini-ACE Runtime Library Software Manual.

Note: *For an RT-RT transfer command where the Enhanced Mini-ACE device is in RT/MT mode and is the* ***receiving*** *RT in the data transfer.*

1) The Monitor does not log any data as the device is busy servicing the receive command. The RT stack has the RT-RT Transfer bit set in the Block Status Word of the receiving RT indicating that the received command is part of an RT-RT transfer command initiated by the BC.

Note: *For an RT-RT transfer command where the Enhanced Mini-ACE device is in RT/MT mode and is the* ***transmitting RT*** *in the data transfer.*

2) The monitor stack contains a command with the block status word set to 0x4000, which indicates a SOM. The RT-RT Transfer bit is **not** set in the Block Status Word for this command. The monitor sees this as a transmit command in the command word part of the stack entry. A second entry is placed in the monitor command stack for this one RT-RT command. This entry has the following bits set in the Block Status Word: EOM, Error Flag, Format Error, Command Word Contents Error and the RT-RT Transfer bit is **not** set in the Block Status Word for this command.

Similar to RT mode, the Selective Monitor Command Stack will store the Command Word, Time Tag Word, Block Status Word, and Data Block Pointer for each monitored message. Programmable size is provided for BC/RT Command Stack, Monitor Command Stack and Monitor Data Stack. The ACE/Mini-ACE Word Monitor also provides for a programmable Trigger Word. The Trigger Word, which defines a specific Command Word, may be used to start the monitor, stop the monitor, or generate an interrupt. The ACE/Mini-ACE word monitor may also be configured to start monitoring based on an external trigger input.

4 SOFTWARE INTERFACE

4.1 POWER TURN-ON/INITIALIZATION STATE

The ACE/Mini-ACE is placed in its power turn-on, or initialization state, following either a hardware or software reset. A hardware reset, which generally occurs following power turn-on, is caused by asserting the $\overline{\text{MSTCLR}}$ input to logic "0" for at least 100 ns. A software reset occurs when the host CPU writes a logic "1" to RESET, bit 0 of the Start/Reset Register. In addition, the ACE/Mini-ACE's RT protocol logic will be reset approximately 2 µs following the midparity bit zero crossing of a received Reset remote terminal mode code Command Word.

The state of the ACE/Mini-ACE's internal logic following a hardware, software, or "Reset RT" reset is summarized in TABLE 2.

TABLE 2. RESET CONDITIONS

	Following Hardware Reset ($\overline{\text{MSTCLR}}$ input)	**Following Software Reset (bit 0 of Start/Reset Register)**	**Following Reception of a 1553B Reset remote terminal mode command**
1553 Message Activity in Progress	Message Activity Aborted	Message Activity Aborted	Message Activity Continues
Interrupt Mask Register	Cleared to 0000	Cleared to 0000	No change
Configuration Registers	All cleared to 0000	All cleared to 0000	No change
Transmitter Inhibited Conditions (from mode command), Terminal Flag Inhibited Condition, and Message Error and Broadcast Command Received bits (if 1553A MODE CODES **are not** enabled).	Transmitters are re-enabled (if inhibited); Terminal Flag bit re-enabled (if inhibited); Message Error and Broadcast Command Received RT Status Word bits are cleared to logic “0”.	Transmitters are re-enabled (if inhibited); Terminal Flag bit re-enabled (if inhibited); Message Error and Broadcast Command Received RT Status Word bits are cleared to logic “0”.	Transmitters are re-enabled (if inhibited); Terminal Flag bit re-enabled (if inhibited); Message Error bit cleared to logic "0," unless Reset RT mode command is illegalized; Broadcast Command Received bit cleared to "0," unless the Reset RT mode command is received to address 11111. Bits 15 through 9 in the RT BIT Word are cleared to logic "0."

TABLE 2. RESET CONDITIONS			
	Following Hardware Reset ($\overline{\text{MSTCLR}}$ input)	**Following Software Reset (bit 0 of Start/Reset Register)**	**Following Reception of a 1553B Reset remote terminal mode command**
Transmitter Inhibited Condition (from mode command), Terminal Flag Inhibited Condition, and Message Error and Broadcast Command Received bits (if 1553A MODE CODES **are** enabled).	Transmitters are re-enabled (if inhibited); Terminal Flag bit re-enabled (if inhibited); Message Error and Broadcast Command Received RT Status Word bits are cleared to logic “0”.	Transmitters are re-enabled (if inhibited); Terminal Flag bit re-enabled (if inhibited); Message Error and Broadcast Command Received RT Status Word bits are cleared to logic “0”.	No change
Address and Data uses	Revert to High impedance state Immediately	No change	No change
RT Address Parity	Clears to 00000 0	No change	No change

4.2 OVERALL ADDRESS MAPPING: WORDS VS. BYTES

It is important to note that with respect to the ACE/Mini-ACE's address bus, A15 through A0, all address mapping is **word oriented**, rather than byte oriented. Although there are a few exceptions (a significant one being the MIL-STD-1750A instruction set architecture), the inherent address mapping for most standard 8-, 16-, and 32-bit microprocessors is **byte oriented**. This difference in mapping convention must be taken into account when assigning pointer values and making CPU accesses to the ACE/Mini-ACE's internal data structures (stack, lookup tables, data tables, etc.) in the ACE/Mini-ACE's shared RAM address space. That is, in terms of the CPU's memory map, the address of these data structures, relative to the ACE/Mini-ACE's base memory address, will be **double** the value of the pointer that is stored in the ACE/Mini-ACE's shared RAM.

For interfacing to most 16-bit microprocessors, the processor's A1 signal connects to the ACE/Mini-ACE's A0 pin, processor A2 connects to the ACE/Mini-ACE's A1 pin, etc. For interfacing to an 8-bit microprocessor **(Please see Appendix G for Product Advisory regarding SP’ACE and SP’ACE II operating in 8-bit Buffered Non-Zero Wait Mode)**, the processor A0 output connects to the ACE/Mini-ACE's MSB/LSB input, the processor's A1 output connects to the ACE/Mini-ACE's A0 pin, processor A2 connects to the ACE/Mini-ACE's A1 pin, etc.

While the ACE/Mini-ACE's internal shared RAM is intended primarily for the buffering of 1553 messages and related pointer data, it is important

to noted that there is **no restriction** prohibiting the use of this RAM for general purpose program memory or "scratchpad" data memory.

4.3 SOFTWARE INTERFACE: INTERNAL RAM

The ACE/Mini-ACE series presents a memory mapped software interface to its host microprocessor. The maximum size of the ACE/Mini-ACE address space is 64K words of internal/external plus 24 additional address locations allocated for internal registers. For most applications, the memory portion of the ACE/Mini-ACE address space is limited to the ACE's 4K, 8K, or 12K words of internal RAM. The BU-65170/71/78/79 and BU-61580/81/88 versions of the ACE/Mini-ACE series have 4K words of internal RAM. The BU-61688/89 contain 64K words of internal RAM. The BU-61590 version has 8K words of internal RAM.

The BU-61585/86 versions of the ACE have 12K words of internal RAM. The BU-61585 and BU-61586 may be configured for either 8K x 17 or 12K x 16 of internal RAM. The 8K x 17 option provides the capability to internally perform parity generation and checking on all RAM accesses. If this option is used, the 8K x 17 of RAM must be assigned to the **lower 8K word locations (0000-1FFF)**, not the upper 8K locations (1000-2FFF). For the BU-61585/86, the upper 4K words, address locations 2000-2FFF, are 16-bit RAM, not 17-bit RAM.

4.4 INTERNAL REGISTERS ADDRESS AND BIT MAPPING

The software interface of the ACE/Mini-ACE to the host processor consists of 17 internal registers for normal operation, an additional 8 test registers, plus 64K x 16 of shared memory address space. The ACE/Mini-ACE's 4K x 16, 12K x 16, or 64Kx16 of internal RAM resides in this address space.

The address mapping and accessibility for the ACE's 17 nontest registers and the test registers is defined in TABLE 3.

TABLE 3. REGISTER ADDRESSES					
ADDRESS INPUTS					REGISTER
A4	A3	A2	A1	A0	DESCRIPTION / ACCESSIBILITY
0	0	0	0	0	Interrupt Mask Register (RD/WR)
0	0	0	0	1	Configuration Register #1 (RD/WR)
0	0	0	1	0	Configuration Register #2 (RD/WR)
0	0	0	1	1	Start/Reset Register (WR)
0	0	0	1	1	Command Stack Pointer Register (RD)
0	0	1	0	0	BC Ctrl Word[1]/RT Subaddr Control[2] Word Register (RD/WR)
0	0	1	0	1	Time Tag Register (RD/WR)
0	0	1	1	0	Interrupt Status Register (RD)
0	0	1	1	1	Configuration Register #3 (RD/WR)
0	1	0	0	0	Configuration Register #4 (RD/WR)
0	1	0	0	1	Configuration Register #5 (RD/WR)
0	1	0	1	0	RT/Monitor Data Stack Address Register (RD/WR)[1]
0	1	0	1	1	BC Frame Time Remaining Register (RD)[1, 3]
0	1	1	0	0	BC Time Remaining to Next Message Register (RD)[1]
0	1	1	0	1	BC Frame Time[1] /RT Last Command[2] /MT Trigger Word Register (RD/WR)[1]
0	1	1	1	0	RT Status Word Register (RD)
0	1	1	1	1	RT BIT Word Register (RD)
1	0	0	0	0	Test Mode Register 0
1	0	0	0	1	Test Mode Register 1
1	0	0	1	0	Test Mode Register 2
1	0	0	1	1	Test Mode Register 3
1	0	1	0	0	Test Mode Register 4
1	0	1	0	1	Test Mode Register 5
1	0	1	1	0	Test Mode Register 6
1	0	1	1	1	Test Mode Register 7
1	1	0	0	0	Reserved
thru					
1	1	1	1	1	Reserved

1. BC or Monitor functions not available on BU-65170/78/79 RT.
2. May only be written while ACE/Mini-ACE is programmed to the idle mode of operation.
3. Returns a Logic “0” on BU-65170/1, 61580/1/5, 65620, and 61590.

QUICK REFERENCE: REGISTER AND OTHER BIT MAPS

TABLE 4. INTERRUPT MASK REGISTER (READ/WRITE 00h)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	RAM PARITY ERROR
13	BC/RT TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAILURE
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	BC MSG/RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

TABLE 5. CONFIGURATION REGISTER #1 (READ/WRITE 01h)				
BIT	**BC FUNCTION (Bits 11-0 Enhanced Mode Only)**	**RT WITHOUT ALTERNATE STATUS**	**RT WITH ALTERNATE STATUS (Enhanced Mode Only)**	**MONITOR FUNCTION (Enhanced Mode Only, bits 12-0)**
15 MSB	RT/$\overline{\text{BC – MT}}$ (Logic 0)	(Logic 1)	(Logic 1)	(Logic 0)
14	RT/$\overline{\text{BC – MT}}$ (Logic 0)	(Logic 0)	(Logic 0)	(Logic 1)
13	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)
11	FRAME STOP-ON-ERROR	$\overline{\text{DYNAMIC BUS CONTROL ACCEPTANCE}}$	S10	TRIGGER ENABLED WORD
10	STATUS SET STOP-ON-MESSAGE	$\overline{\text{BUSY}}$	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	$\overline{\text{SERVICE REQUEST}}$	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	$\overline{\text{SUBSYSTEM FLAG}}$	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	$\overline{\text{RT FLAG}}$ (enhanced mode only)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	INTER-MESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLE/$\overline{\text{SINGLE}}$ RETRY	NOT USED	S02	NOT USED
2	BC ENABLED (read only)	NOT USED	S01	MONITOR ENABLED (read only)
1	BC FRAME IN PROGRESS (read only)	NOT USED	S00	MONITOR TRIGGERED (read only)
0 LSB	BC MESSAGE IN PROGRESS (read only)	RT MESSAGE IN PROGRESS (enhanced mode only) (read only)	RT MESSAGE IN PROGRESS (read only)	MONITOR ACTIVE (read only)

TABLE 6. CONFIGURATION REGISTER #2 (READ/WRITE 02h)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED INTERRUPTS
14	RAM PARITY ENABLE
13	BUSY LOOK UP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDR DISBL
9	TIME TAG RESOLUTION 2(TTR2)
8	TIME TAG RESOLUTION 1(TTR1)
7	TIME TAG RESOLUTION 0(TTR0)
6	CLEAR TIME TAG ON SYNCHRONIZE
5	LOAD TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/PULSE INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST
1	ENHANCED RT MEMORY MANAGEMENT
0 (LSB)	SEPARATE BROADCAST DATA

TABLE 7. START/RESET REGISTER (WRITE 03H) DESCRIPTION	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
•	•
•	•
•	•
7	RESERVED
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0 (LSB)	RESET

TABLE 8. BC/RT COMMAND STACK POINTER REGISTER (READ 03h)	
BIT	**DESCRIPTION**
15(MSB)	COMMAND STACK POINTER 15
•	•
•	•
•	•
0(LSB)	COMMAND STACK POINTER 0

TABLE 9. BC CONTROL WORD REGISTER (READ/WRITE 04h)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	MESSAGE ERROR MASK
13	SERVICE REQUEST BIT MASK
12	SUBSYS BUSY BIT MASK
11	SUBSYS FLAG BIT MASK
10	TERMINAL FLAG BIT MASK
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL $A/\overline{B}$
6	OFF LINE SELF TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-TO-RT FORMAT

TABLE 10. RT SUBADDRESS CONTROL WORD (READ/WRITE 04h)	
BIT	**DESCRIPTION**
15(MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

TABLE 11. TIME TAG REGISTER (READ/WRITE 05h)	
BIT	**DESCRIPTION**
15(MSB)	TIME TAG 15
•	•
•	•
•	•
0(LSB)	TIME TAG 0

TABLE 12. INTERRUPT STATUS REGISTER (READ/WRITE 06h)	
BIT	**DESCRIPTION**
15(MSB)	MASTER INTERRUPT
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAILURE
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	BC CONTROL WORD/ RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

TABLE 13. CONFIGURATION REGISTER #3 (READ/WRITE 07h)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE $T/\overline{R}$ ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER ENABLE
2	$\overline{\text{RT FAIL}}/\overline{\text{RT FLAG}}$ WRAP
1	1553A MODE CODES ENABLE
0(LSB)	ENHANCED MODE CODE HANDLING

TABLE 14. CONFIGURATION REGISTER #4 (READ/WRITE 08h)	
BIT	**DESCRIPTION**
15(MSB)	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BRAODCASTMASKENA/$\overline{\text{XOR}}$
10	RETRY IF -A AND M.E.
9	RETRY IF STATUS SET
8	1ST RETRY ALT/$\overline{\text{SAME BUS}}$
7	2ND RETRY ALT/$\overline{\text{SAME BUS}}$
6	VALID M.E./NO DATA
5	VALID BUSY/NO DATA
4	MT TAG GAP OPTION
3	LATCH RT ADDR WITH CONFIG. REG. #5
2	TEST MODE 2
1	TEST MODE 1
0(LSB)	TEST MODE 0

TABLE 15. CONFIGURATION REGISTER #5 (READ/WRITE 09h)	
BIT	**DESCRIPTION**
15(MSB)	12 MHZ CLOCK SELECT (10 MHZ CLOCK SELECT for BU-61689)
14	SINGLE-ENDED SELECT
13	EXTERNAL TX INHIBIT A
12	EXTERNAL TX INHIBIT B
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	RT ADDR LATCH/$\overline{\text{TRANSPARENT}}$
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0(LSB)	RT ADDRESS PARITY

TABLE 16. RT/MONITOR DATA STACK ADDRESS REGISTER (READ/WRITE 0Ah)	
BIT	**DESCRIPTION**
15(MSB)	RT/MONITOR DATA STACK ADDRESS 15
•	•
•	•
•	•
0(LSB)	RT/MONITOR DATA STACK ADDRESS 0

TABLE 17. BC FRAME TIME REMAINING REGISTER (READ/WRITE 0Bh)

BIT	DESCRIPTION
15(MSB)	BC FRAME TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC FRAME TIME REMAINING 0

NOTE: Resolution = 100 µs per LSB

TABLE 18. BC MESSAGE TIME REMAINING REGISTER (READ 0Ch)

BIT	DESCRIPTION
15(MSB)	BC MESSAGE TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC MESSAGE TIME REMAINING 0

NOTE: Resolution = 1 µs per LSB

TABLE 19. BC FRAME TIME/RT LAST COMMAND/MT TRIGGER REGISTER (READ/WRITE 0Dh)

BIT	DESCRIPTION
15(MSB)	BIT 15
•	•
•	•
•	•
0(LSB)	BIT 0

TABLE 20. RT STATUS WORD REGISTER (READ 0Eh)

BIT	DESCRIPTION
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPT
0(LSB)	TERMINAL FLAG

TABLE 21. RT BIT WORD REGISTER (READ 0Fh)

BIT	DESCRIPTION
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	CHANNELB / $\overline{A}$
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLES on this page are not registers, but they are words stored in RAM:

TABLE 22. BC MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNELB/$\overline{A}$
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

TABLE 23. RT MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNELB/$\overline{A}$
12	ERROR FLAG
11	RT-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 24. 1553 COMMAND WORD	
BIT	**DESCRIPTION**
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
•	•
•	•
•	•
11	REMOTE TERMINAL ADDRESS BIT 0
10	TRANSMIT RECEIVE
9	SUBADDRESS/MODE CODE BIT 4
•	•
•	•
•	•
5	SUBADDRESS/MODE CODE BIT 0
4	DATA WORD COUNT/MODE CODE BIT 4
•	•
•	•
•	•
0(LSB)	DATA WORD COUNT/MODE CODE BIT 0

TABLE 25. WORD MONITOR IDENTIFICATION WORD	
BIT	**DESCRIPTION**
15(MSB)	GAP TIME
•	•
•	•
•	•
8	GAP TIME
7	WORD FLAG
6	$\overline{\text{THISRT}}$
5	$\overline{\text{BROADCAST}}$
4	ERROR
3	COMMAND/$\overline{\text{DATA}}$
2	CHANNELB/$\overline{A}$
1	CONTIGUOUSDATA/$\overline{\text{GAP}}$
0(LSB)	$\overline{\text{MODE_CODE}}$

TABLE 26. MESSAGE MONITOR MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNELB/$\overline{A}$
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 27. 1553B STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
14	REMOTE TERMINAL ADDRESS BIT 3
13	REMOTE TERMINAL ADDRESS BIT 2
12	REMOTE TERMINAL ADDRESS BIT 1
11	REMOTE TERMINAL ADDRESS BIT 0
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPTANCE
0(LSB)	TERMINAL FLAG

The Interrupt Mask Register is used to enable and disable interrupt requests for various conditions. Configuration Registers #1 and #2 are used to select the ACE'/Mini-ACEs mode of operation as well as for software control of RT Status Word bits, Active Memory Area, BC Stop-on-Error, RT Memory Management mode selection, and control of the Time Tag operation.

The Start/Reset Register is used for "command" type functions, such as software reset, BC/MT Start as well as Interrupt Reset, Time Tag Reset, and Time Tag Register Test. The Start/Reset Register includes provisions for stopping the BC in its frame auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

The Stack Pointer Register allows the host CPU to determine the pointer location for the current or most recent message when the ACE/Mini-ACE is in BC or RT modes.

The Subaddress Control Word Register allows the host processor access to the current or most recent Subaddress Control Word; the read/write accessibility of this register can be used as an aid for testing of the ACE/Mini-ACE.

The 16-bit Time Tag Register maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 us/LSB. The Time Tag Register may also be clocked by an external oscillator. The current value of the Time Tag Register is written to the Stack area of RAM during Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes.

The Interrupt Status Register mirrors the Interrupt Mask Register and contains a Master Interrupt bit. It allows the host processor to determine the cause of an interrupt request by means of a single READ operation.

Configuration Registers #3, #4, and #5 are used to enable many of the ACE/Mini-ACE's advanced features. These include all of the ENHANCED mode features; that is, all of the functionality beyond that of the previous generation product, the BUS-61559 series Advanced Integrated Mux Hybrid with Enhanced RT Features (AIM-HY'er). For all three modes, use of the ENHANCED Mode enables the various read-only bits in Configuration Register #1.

For BC mode, the enhanced mode features include the expanded BC Control Word and BC Block Status Word, additional STOP-ON-ERROR and STOP-ON-STATUS SET functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message.

For RT mode, the enhanced mode features include the expanded RT Block Status Word, the combined RT/Selective Message Monitor mode, internal wrapping of the "$\overline{\text{RTFAIL}}$" output signal to the "$\overline{\text{RTFAIL}}$" input signal, double buffering for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word.

For MT mode, use of the enhanced mode enables use of both the Selective Message Monitor and the combined RT/Selective Monitor modes, as well as use of the monitor triggering capability.

The RT/Monitor Data Stack Address Register provides a pointer to the current address location in shared RAM used for storing Data Words in RT mode, or message words (second Command Words, Data Words, RT Status Words) in the Selective Word Monitor mode.

The Frame Time Remaining Register provides a read only indication of the time remaining in the current BC frame. The resolution of this register is 100 µs/LSB.

The Message Time Remaining Register provides a read only indication of the time remaining before the start of the next message in a BC frame. The resolution of this register is 1 µs/LSB.

The register at register address 0D is used differently in different modes of operation. In BC mode, it is used to program the BC frame time, for use in the FRAME AUTO-REPEAT mode. The resolution of this register is 100 µs/LSB, with a range of 6.55 seconds. In RT mode, this register stores the current (or most previous) 1553 Command Word processed by the ACE/Mini-ACE RT. In the Monitor mode, this register is used to specify a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

The Status Word Register and BIT Word Register provide read-only indications of the ACE/Mini-ACE's RT Status and BIT Words.

The ACE/Mini-ACE also includes a set of test registers. These registers may be used to facilitate production or maintenance testing of the ACE/Mini-ACE and systems incorporating the ACE/Mini-ACE.

The bit maps and detailed definitions of the 17 operational registers are defined in TABLE 28:

4.5 INTERRUPT MASK REGISTER (Register Address 00000; READ/WRITE)

TABLE 28. INTERRUPT MASK REGISTER (READ/WRITE 00h)

BIT	DESCRIPTION
15(MSB)	RESERVED
14	RAM PARITY ERROR
13	BC/RT TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAILURE
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	BC MSG/RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

In the non-ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "0"), bits 7 through 0 of the Interrupt Mask Register are used to **both** enable interrupts for the various events/conditions **and** to enable the respective bits of the Interrupt Status Register to be set. That is, the various bits of the Interrupt Status Register will **not** become set if the corresponding bits of the Interrupt Mask Register are not set. Bits 14 through 8 are **not used** in the non-ENHANCED mode.

In the ENHANCED mode with the Enhanced Interrupts Enabled (bit 15 of Configuration Register #2 set to logic "1"), all 15 interrupts are accessible (bits 14 through 0) and the value of the Interrupt Mask Register has no effect on the operation of the Interrupt Status Register. If Enhanced Interrupts are enabled, the bits of the Interrupt Status Register **do not need to be enabled** by the corresponding bits in the Interrupt Mask Register. In the Enhanced Interrupt mode, these bits become set following the occurrence of the respective event/condition, regardless of the programming of the corresponding Interrupt Mask Register bit. In either mode, an interrupt for any of the 15 event/conditions (8 in non-ENHANCED mode) is only enabled if the respective bit of the Interrupt Mask Register (for the event/condition) has been programmed to logic "1."

TABLE 29 summarizes the effect of the ENHANCED mode and the ENABLE INTERRUPTS bit on the operation of the Interrupt Request output ($\overline{\text{INT}}$) and the Interrupt Mask and Interrupt Status Registers.

TABLE 29. ENHANCED MODE INTERRUPTS				
NON-ENHANCED/ ENHANCED MODE	**ENHANCED INTERRUPTS ENABLED BIT (BIT 15 OF CONFIGURATION REGISTER #2)**	**INTERRUPT REQUEST ENABLED**	**INTERRUPT STATUS REGISTER BIT ENABLED**	**ACTIVE INTERRUPT MASK AND INTERRUPT STATUS BITS**
NON-ENHANCED MODE	X	If condition enabled by corresponding Interrupt Mask Register bit	If condition enabled by corresponding Interrupt Mask Register bit	7-0
ENHANCED MODE	0	If condition enabled by corresponding Interrupt Mask Register bit	If condition enabled by corresponding Interrupt Mask Register bit	7-0
ENHANCED MODE	1	If condition enabled by corresponding Interrupt Mask Register bit	Always Enabled	14-0

RAM PARITY ERROR: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1") **and** if RAM PARITY ENABLE, bit 14 of Configuration Register #2, is logic "1". RAM PARITY ERROR allows an interrupt request to be issued as the result of a RAM parity error during a read access.

Note: *It is important to note that for the BU-65170, BU-65178, BU-65179, BU-61580, BU-61588, BU-61590, BU-61688, and BU-61689 ACE/Mini-ACE products, there is NO 17-bit buffered RAM. Therefore, for these products, RAM parity is NOT implemented. RAM PARITY ERROR must be set to logic "0" for these products.*

For the BU-61585 ACE terminal and the BU-65620 digital monolithic, setting RAM PARITY ERROR to logic "1," enables an interrupt request to occur following a RAM parity error. The BU-61585 includes 8K x 17 of internal RAM. RAM parity may also be utilized with the BU-65620 digital monolithic, using external 17-bit wide RAM on the "buffered" side of the BU-65620.

TRANSMITTER TIMEOUT: If set, enables an interrupt following a timeout of the ACE's transmitter watchdog timer. This occurs if the ACE's encoder attempts to transmit for longer than 668 µs. This interrupt only occurs in the BC or the RT mode.

BC/RT COMMAND STACK ROLLOVER: If set, enables an interrupt following a rollover of the BC or RT stack (Command Stack 1). The size of Command Stack 1 is programmable from among 256 (64 messages), 512, 1024, and 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register #3. This interrupt only occurs in the ENHANCED mode (bit 15 of Configuration Register #3 programmed to logic "1").

MESSAGE MONITOR COMMAND STACK ROLLOVER: If set, enables an interrupt following a rollover of the Message Monitor Command Stack (Command Stack 2). This is applicable for both the Message Monitor as

well as the combined RT/Message Monitor modes. The size of Command Stack 2 is programmable from among 256 (64 messages), 1024, 4096, and 16,384 words (4096 messages) by means of bits 12 and 11 of Configuration Register #3. This interrupt only occurs in the ENHANCED mode (bit 15 of Configuration Register #3 programmed to logic "1").

MONITOR DATA STACK ROLLOVER: If set, enables an interrupt following a rollover of the Word Monitor or Message Monitor Data Stack. The size of the Data Stack is programmable from among 512, 1024, 2048, 4096, 8192, 16,384, 32,768, or 65,536 words by means of bits 10, 9, and 8 of Configuration Register #3. This interrupt only occurs in the ENHANCED mode (bit 15 of Configuration Register #3 programmed to logic "1").

HANDSHAKE FAILURE: If set, enables an interrupt following a handshake timeout during a transfer between the 1553 protocol section and the RAM. A Handshake Failure can only occur in the transparent configuration of the ACE host interface. There are two conditions that can cause a Handshake Failure (For both conditions, the maximum allotted time is 4.4 µs for a 20 MHz clock input, 4.0 µs for a 16 MHz clock input, 3.5 µs for a 12 MHz clock input, and 3.2 µs for a 10 MHz clock input):

1) When the Data Transfer Grant ($\overline{\text{DTGRT}}$) input is not asserted within the allotted time after the ACE's Data Transfer Request ($\overline{\text{DTREQ}}$) output has been asserted.

2) When the $\overline{\text{STRBD}}$ input signal is held low too long at the end of a processor transfer cycle (as indicated by the falling edge of $\overline{\text{READYD}}$). $\overline{\text{STRBD}}$ asserted low for too long will **not** result in a HANDSHAKE-FAILURE condition in the buffered mode configuration.

BC RETRY: If set, enables an interrupt following the occurrence of a retried message in BC mode. If enabled, the interrupt will occur regardless of whether the retry attempt was successful or unsuccessful.

RT ADDRESS PARITY ERROR: If set, enables an interrupt if an RT Address parity error condition is sensed. That is, if RTAD4-RTAD0 plus RTADP fail to have an odd parity sum.

TIME TAG ROLLOVER: If set, enables an interrupt if the 16-bit Time Tag Register rolls over from FFFF to 0000.

RT SUBADDRESS CIRCULAR BUFFER ROLLOVER: If this bit is set **and** the ACE/Mini-ACE is in the Enhanced Memory Management RT mode (bit 1 of Configuration Register #2 is set to logic "1") **and** the

"Interrupt at Rollover" bit is set in the Subaddress Control Word for the respective Tx/Rx/Bcst subaddress, an interrupt request will be issued when the respective data lookup address pointer crosses the lower boundary of its circular buffer, resulting in a rollover. If bit 11 of Configuration Register #2 (OVERWRITE INVALID DATA) is logic "0," the RT Subaddress Circular Buffer Rollover interrupt request will be issued **immediately** after the last word at the bottom boundary of the circular buffer in the shared RAM address space (address XXXX...1111) has been read or written. If bit 11 of Configuration Register #2 is logic "1," the interrupt request will occur at the end of a transmit message or a **valid** receive message in which the word at the bottom boundary of the circular buffer in the shared RAM address space has been read or written. For a receive message, an interrupt request will **not** be issued if bit 11 is set and there is an error in the message, even if the last word of the buffer was accessed during the message.

BC MESSAGE/RT SUBADDRESS CONTROL WORD EOM: For BC mode, if this bit is logic "1" **and** the EXPANDED BC CONTROL WORD bit (bit 12 of Configuration Register #4) is logic "1" **and** the EOM_INTERRUPT ENABLE bit (bit 4) of the respective BC Control Word is logic "1," an interrupt request will be issued at the end of the current message. For RT mode, if this bit is set **and** the ACE is in the Enhanced Memory Management RT mode **and** the "Interrupt at EOM" bit is set in the Subaddress Control Word for the respective Tx/Rx/Bcst subaddress, an interrupt will occur at the end of the current message.

BC END-OF-FRAME: If enabled, this interrupt request will be issued after an entire programmed BC message frame has been processed. That is, following the end of a message that resulted in the active area Message Count RAM location to have been incremented to FFFF (hex). Note that if BC STOP-ON-ERROR is enabled and a BC frame is aborted before the Message Count has incremented to FFFF (hex), the BC_EOM interrupt will **not** occur.

FORMAT ERROR: If enabled, will result in an interrupt request for any of the following conditions:

1) **Loop Test Failure:** A loopback test is performed on every word transmitted by the ACE/Mini-ACE BC or RT for each message. If the received version of one or more words is decoded as invalid and/or the received version of the last transmitted word does not match the transmitted version, the loopback test is considered to have failed.

2) **Message Error:** A Received Message contained a violation of the 1553 message validation criteria (encoding, parity, bit count, word count, etc.). For RT mode, this **does not** include an error in the received Command Word. If an invalid Command Word

is detected, the entire message is ignored.

3) **Response Timeout:** In BC or Message Monitor modes, an RT has either not responded or has responded later than the programmed value of the BC No Response Timeout time. This time is programmable for values of approximately 18.5, 22.5, 50.5, or 130 µs by means of bits 10 and 9 of Configuration Register #5. In RT mode, a response timeout occurs if the ACE is the receiving RT in an RT-to-RT transfer and the transmitting RT has not responded with its Status Word within the RT-to-RT No Response Timeout time. The RT-to-RT timeout time is programmable with the same choice of values as the BC No Response Timeout.

BC STATUS SET/RT SELECTED MODE CODE INTERRUPT/MT PATTERN TRIGGER: In BC mode, the RT Status Word received from a responding RT either contained an incorrect RT address field or one of the 8 non-RESERVED Status bits contained an unexpected bit value. The expected value for these 8 bits is normally zero (0), with one exception: If (the ACE is in its non-ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 is logic "0") **or** BROADCAST MASK ENABLE/$\overline{\text{XOR}}$, bit 11 of Configuration Register #4 is logic "0") **and** if the Mask Broadcast bit of the message's BC Control Word is set, the expected value of the Broadcast Command Received bit becomes 1, rather than 0.

In RT mode, this interrupt can only occur in the ENHANCED mode (bit 15 of Configuration Register #3 is set to logic "1") **and** if Enhanced Mode Code Handling is enabled (bit 0 of Configuration Register #3 is set to logic "1"). If these two bits are set, mode code interrupts for individual broadcast-T/R bit-mode codes may be enabled by setting the appropriate bit(s) in address locations 0108-010F in the shared RAM. Reception of an enabled mode code message will then cause a mode code interrupt to occur at the end of the message.

In the Word Monitor mode, a Pattern Trigger interrupt will occur in the ENHANCED mode (bit 15 of Configuration Register #3 is set to logic "1") following the reception of a valid Command Word that matches the bit pattern programmed in the Monitor Trigger Register.

END OF MESSAGE: End of Message. If enabled, will result in an interrupt in BC, RT, and Selective Monitor modes at the completion of every message (regardless of validity).

An interrupt request will be issued (either a pulse or level, as determined by bit 3 of Configuration Register #2) whenever one of the interrupt request conditions occurs **and** the respective bit of the Interrupt Mask Register is set to logic "1." For a level type of request output, $\overline{\text{INT}}$ will be

cleared high after the Interrupt Status Register has been read, if bit 4 of Configuration Register #2 (INTERRUPT STATUS AUTO CLEAR) is set. Otherwise, the $\overline{\text{INT}}$ level may be reset by writing logic "1" to bit 2 (INTERRUPT RESET) of the Start/Reset Register.

The respective bits in the Interrupt Status Register will be set under either of the following two conditions:

1) If the ACE/Mini-ACE is in its non-ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 is logic "0") **or** ENHANCED INTERRUPTS are not enabled (bit 15 of Configuration Register #2 is logic "0")) **and** the respective bit in the Interrupt Mask Register is logic "1" **and** the condition occurs.

2) If the ACE/Mini-ACE is in its ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 is logic "1") **and** ENHANCED INTERRUPTS are enabled (bit 15 of Configuration Register #2 is logic "1") **and** the condition occurs, regardless of whether or not the respective bit in the Interrupt Mask Register is set to logic "1."

4.6 CONFIGURATION REGISTER #1 (Register Address 00001; READ/WRITE)

TABLE 30. CONFIGURATION REGISTER #1 (READ/WRITE 01h)

BIT	BC FUNCTION (BITS 11-0 ENHANCED MODE ONLY)	RT WITHOUT ALTERNATE STATUS (SEE NOTES 1 AND 3)	RT WITH ALTERNATE STATUS (ENHANCED MODE ONLY AND BIT 5 OF CFG. REG. #3 IS LOGIC '1') (SEE NOTES 1 AND 3)	MONITOR FUNCTION (ENHANCED MODE ONLY, BITS 12-0)
15 MSB	MT/$\overline{BC-RT}$ (Logic 0)	(Logic 1)	(Logic 1)	(Logic 0)
14	MT/$\overline{BC-RT}$ (Logic 0)	(Logic 0)	(Logic 0)	(Logic 1)
13	CURRENT AREA B/$\overline{A}$	CURRENT AREA B/$\overline{A}$	CURRENT AREA B/$\overline{A}$	CURRENT AREA B/$\overline{A}$
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)
11	FRAME STOP-ON-ERROR	$\overline{\text{DYNAMIC BUS CONTROL ACCEPTANCE}}$	S10 (See Note 2)	TRIGGER ENABLED WORD
10	STATUS SET STOP-ON-MESSAGE	$\overline{\text{BUSY}}$	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	$\overline{\text{SERVICE REQUEST}}$	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	$\overline{\text{SUBSYSTEM FLAG}}$	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	$\overline{\text{RTFLAG}}$ (Enhanced Mode Only)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	INTER-MESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLE/$\overline{\text{SINGLE}}$ RETRY	NOT USED	S02	NOT USED
2	BC ENABLED (Read Only)	NOT USED	S01	MONITOR ENABLED (Read Only)
1	BC FRAME IN PROGRESS (Read Only)	NOT USED	S00	MONITOR TRIGGERED (Read Only)
0 LSB	BC MESSAGE IN PROGRESS (Read Only)	RT MESSAGE IN PROGRESS (Enhanced Mode Only) (Read Only)	RT MESSAGE IN PROGRESS (Read Only)	MONITOR ACTIVE (Read Only)

Notes:
(1) The combined RT/Message Monitor mode uses the RT WITHOUT ALTERNATE STATUS or the RT WITH ALTERNATE STATUS bit definitions NOT the MONITOR FUNCTION bit definitions.
(2) In the alternate RT Status Word mode, bit 10 (Message Error) may also be set for an illegalized message (Broadcast-$T/\overline{R}$ bit-subaddress-word count/mode code).
(3) Refer to RT Status Word section in the RT operation chapter on the use of RT status word bits.

RT/$\overline{\text{BC}}$–$\overline{\text{MT}}$, MT/$\overline{\text{BC}}$–$\overline{\text{RT}}$, and MMT: Selects the ACE/Mini-ACE's mode of operation as follows:

TABLE 31. MODE SELECTION

CONFIG #1			CONFIG #3	MODE
BIT 15	BIT 14	BIT 12	BIT 15	
0	0	X	0	Non-ENHANCED BC (See Note)
0	0	X	1	ENHANCED BC
0	1	0	X	Word Monitor
0	1	1	0	Word Monitor
0	1	1	1	Message Monitor
1	0	X	0	Non-ENHANCED RT
1	0	0	1	ENHANCED RT
1	0	1	1	Enhanced RT/Message Monitor
1	1	X	X	Idle

Notes:

(1) Following hardware reset ($\overline{\text{MSTCLR}}$ asserted) or software reset (by means of the Start/Reset Register), the ACE/Mini-ACE will initialize to idle (non-transmitting) **BC mode**.

(2) For a BU-61580/81/85/86/88/90, BU-65620, BU-61688/89, if the ACE/Mini-ACE is switched from RT to combined RT/Monitor mode in the middle of an RT message, the message **will be completed.**

(3) For a BU-61580/81/85/86/88/90, BU-65620, BU-61688/89, if the ACE/Mini-ACE is switched from combined RT/Monitor mode to RT mode in the middle of an RT message or Monitor message, the message **will be completed.**

(4) For a BU-61580/81/85/86/90 or BU-65620, if the ACE is switched from either RT mode or Monitor mode to either BC mode or "Idle" mode in the middle of an RT message, the message **will be aborted.**

(5) For a BU-61580/81/85/86/90 or BU-65620, if the ACE is switched from non-enhanced RT mode to "Idle" mode there is **no effect.**

(6) For a BU-61580/81/85/86/88/90, BU-65620, or BU-61688/89, if the ACE/Mini-ACE is switched from (enhanced or non-enhanced) BC mode to “Idle” mode in the middle of a message, the message **will be aborted.**

It should be noted that ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, must be set to logic "1," **PRIOR** to activating the ENHANCED BC or RT modes, or the Message Monitor or RT/Message Monitor modes. In addition, the ACE/Mini-ACE must be programmed for its ENHANCED mode **PRIOR** to setting bit 5 of Configuration Register #3 in order to activate RT with Alternate Status. In this instance, Configuration Register #3 must be written **TWICE**.

CURRENT AREA B/$\overline{\text{A}}$: Selects Current Area Pointers. Note that if bit 13 is updated during the processing of a BC frame, or while an RT or Selective Message Monitor message is in progress, the value that will be returned to the host processor will continue to be the **old** value until the BC frame or RT/MT message in progress has been completed. After the current BC frame or RT/MT message has been completed, bit 13 as read by the host CPU will toggle to its new value. If the ACE is already on-line in the Word Monitor mode, toggling this bit will have no effect. **It should be noted that Active Area selection is NOT related to the selection**

or operation of the bus channels on a dual redundant 1553 bus (Bus A vs. Bus B).

For BC mode, bits 12 through 0 are defined as follows:

MESSAGE STOP-ON-ERROR: If this bit is set, the ACE/Mini-ACE will abort the processing of messages following the end of the current message if it encounters either a word error (gap, sync, encoding, or parity error), message format error (incorrect RT Address in Status Word, high or low word count) , a response timeout condition or a looptest failure.

If retries are enabled for a particular message, the retry **will** be attempted even if MESSAGE STOP-ON-ERROR is programmed to logic "1." It should be noted that the processing of subsequent BC messages in the frame **will continue** if a failed message is successfully retried.

FRAME STOP-ON-ERROR: This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This mode is invoked if bit 8 of this register, FRAME AUTO REPEAT, is programmed to logic "1." If FRAME STOP-ON-ERROR is set, the ACE will abort the processing of messages following the end of the current BC **frame** if it encounters either a word error (gap, sync, encoding, or parity error) or message format error (incorrect RT Address in Status Word, high or low word count) , a response timeout condition, or a looptest failure.

If retries are enabled for a particular message, the retry **will** be attempted even if FRAME STOP-ON-ERROR is programmed to logic "1." It should be noted that the processing of subsequent BC frames **will continue** if a failed message is successfully retried.

For BC mode, bits 11 through 0 are defined in the ENHANCED BC Mode (bit 15 of Configuration Register #3 set to logic "1") as follows:

STATUS SET STOP-ON-MESSAGE: This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is set, the ACE will abort the processing of messages following the end of the current message if it encounters a "Status Set" condition in the message. A "Status Set" condition is defined as an unexpected value for one of the 8 nonreserved Status Word bits.

If bit 12 of Configuration Register #4, EXPANDED BC CONTROL WORD, is programmed to logic "0," Status Set encompasses **all 8** of the nonreserved Status Word bits. The expected value for the 8 nonreserved Status Word bits is normally zero (0), with one exception: if bit 11 of Configuration Register #4, BROADCAST MASK ENA/$\overline{\text{XOR}}$, is

logic "0" and the MASK BROADCAST bit of the message's BC Control Word is logic "1," the expected value of the Broadcast Command Received bit becomes 1, rather than 0. If BROADCAST MASK ENA/ $\overline{\text{XOR}}$ is programmed to logic "1," the MASK BROADCAST bit of the BC Control Word is used as a mask bit, rather than performing an "XOR" operation with the Broadcast Received Status Word bit. In this instance, a Status Set condition arising from the Broadcast Command Received RT Status bit occurs when the MASK BROADCAST BC Control Word bit is logic "0" and the Broadcast Command Received RT Status Word bit is logic "1."

If EXPANDED BC CONTROL WORD is programmed to logic "1," the RT Status Word is masked by bits 14 through 9 of the BC Control Word. In this instance, the corresponding BC Control Word bit must be programmed to logic "0" in order for a "Status Set" condition to arise from the corresponding bit in the received RT Status Word. In this instance, Status Set conditions will **not** occur from Status Mask bits in the BC Control Word that are programmed to logic "1."

If a "STATUS SET" retry is enabled for a particular message, the retry **will** be attempted, even if STATUS SET STOP-ON-MESSAGE is programmed to logic "1." It should be noted that the processing of subsequent BC messages **will continue** if a message containing a STATUS SET condition is retried and the STATUS SET condition does not occur on the retry.

STATUS SET STOP-ON-FRAME: This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is set, the ACE will abort the processing of the current BC frame following the end of the frame if it encounters a "Status Set" condition in one or more messages in the frame. A "Status Set" condition is defined as described in the preceding paragraph.

If a "STATUS SET" retry is enabled for a particular message, the retry **will** be attempted, even if STATUS SET STOP-ON-MESSAGE is programmed to logic "1." It should be noted that the processing of subsequent BC frames **will continue** if a message containing a STATUS SET condition is retried and the STATUS SET condition does not occur on the retry.

FRAME AUTO-REPEAT: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is programmed to logic "0," the ACE will process its programmed BC frame one time and then halt. In this instance, the BC Stack Pointer and BC Message Count are maintained at shared RAM locations 0100 and 0101, respectively, for Area A and locations 0104 and 0105, respectively, for Area B.

If FRAME AUTO-REPEAT is programmed to logic "1," the ACE/Mini-ACE's BC frame will repeat indefinitely until either: a RESET, STOP-ON-MESSAGE, or STOP-ON-FRAME software command is invoked via the Start/Reset Register; or an enabled (MESSAGE or FRAME) STOP-ON-ERROR or STOP-ON-STATUS SET condition has occurred. In the Frame Auto-Repeat mode, just as in the "single frame" mode, the current values of the BC Stack Pointer and BC Message Count are maintained at shared RAM locations 0100 and 0101, respectively, for Area A and locations 0104 and 0105, respectively, for Area B. In addition, for the AUTO-REPEAT mode, the "initial" values which are, the values of the Stack Pointer and Message Count at the start of each frame, must also be loaded in the shared RAM to support the frame repetition: addresses 102 and 103, respectively for area A and locations 106 and 107, respectively for area B.

If the INTERNAL TRIGGER ENABLE bit of this register is set to logic "1," the BC frame will repeat with a fixed frame time as specified in the BC Frame Time Register (100 µs to 6.55 seconds). Alternatively, if the EXTERNAL TRIGGER ENABLE bit of this register is set to logic "1," each repetitive BC frame may be initiated by means of an external pulse delivered to the ACE's EXT_TRIG input. If both the INTERNAL TRIGGER ENABLE and the EXTERNAL TRIGGER ENABLE bits are set, the initial frame will be initiated by the EXT_TRIG input and all subsequent frames will be initiated by the internal frame timer.

EXTERNAL TRIGGER ENABLED: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is logic "0," the ACE/Mini-ACE BC may only be started by means of a "START" software command to the Start/Reset Register. If this bit is set to logic "1," the ACE/Mini-ACE BC frame may be initiated by an external signal delivered to the EXT_TRIG input as well as by means of a software command via the Start/Reset Register. If the FRAME AUTO-REPEAT **and** INTERNAL TRIGGER ENABLE, **and** EXTERNAL TRIGGER ENABLE bits are set, the initial frame will be initiated by the EXT_TRIG input and all subsequent frames will be initiated by the internal frame timer.

INTERNAL TRIGGER ENABLED: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit is used in conjunction with the FRAME AUTO-REPEAT bit to enable automatic frame repetition. If FRAME AUTO-REPEAT is set to logic "1" and INTERNAL TRIGGER ENABLED is set to logic "0," the ACE/Mini-ACE BC will halt the processing of messages after a single frame; in this scenario, a repetitive frame may still be retriggered by means of an external signal delivered to EXT_TRIG, provided that EXTERNAL TRIGGER ENABLE has been programmed to logic "1." If INTERNAL TRIGGER ENABLE is set to logic "1," the BC frame will repeat with a

fixed frame time as specified in the BC Frame Time Register (100 µs to 6.55 seconds). If both the INTERNAL TRIGGER ENABLE and the EXTERNAL TRIGGER ENABLE bits are set, the initial frame will be initiated by the EXT_TRIG input and all subsequent frames will be initiated by the internal frame timer.

MESSAGE GAP TIMER ENABLED: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is programmed to logic "0," the ACE/Mini-ACE's intermessage gap will assume a fixed minimum value of approximately 8 to 11 µs. If this bit is programmed to logic "1," the message gap for each message will be specified by means of the third word in the respective BC message block descriptor. This time value, which specifies the time from the start of the current message to the time of the start of the subsequent message, is programmable from the minimum value (approximately 8 to 11 µs) up to 65.535 ms, in steps of 1 µs. If the programmed value of the message gap time is less than the time required to process the current message, the current message **will be processed to completion** before the subsequent message is started. In this case, the gap time between messages will assume the minimum value of approximately 8 to 11 µs.

RETRY ENABLED: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is programmed to logic "0," BC retries are disabled for **all** messages. If this bit is programmed to logic "1," automatic retry may be enabled on a message-by-message basis by setting bit 8 of the BC Control Word to logic "1" for all messages to be retried.

DOUBLE/$\overline{\text{SINGLE}}$ RETRY: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If retries are enabled (RETRY ENABLED, bit 4 of Configuration Register #1, set to logic "1"), this bit is used to program the number of retries that will be performed (when enabled). A logic "0" will cause the ACE/Mini-ACE to perform a single retry, while a logic "1" will cause the ACE to perform up to two retries.

BC ENABLED (Read Only): This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit will return a value of logic "1" after the ACE/Mini-ACE BC has been started by means of either the Start/Reset Register or a signal delivered to EXT_TRIG. This bit will continue to return a logic "1" until either: a single message frame completes, if not in FRAME AUTO-REPEAT mode; a RESET, STOP-ON-MESSAGE, or STOP-ON-FRAME software command is invoked via the Start/Reset Register; or an enabled (MESSAGE or FRAME) STOP-ON-ERROR or STOP-ON-STATUS SET condition occurs.

BC FRAME-IN-PROGRESS (Read Only): This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit will return a value of logic "1" between the time of the BC Start-of-Message (SOM) sequence for the first message of a programmed BC frame, until the completion of the BC End-of-Message (EOM) sequence for the last programmed message of the frame. In the FRAME AUTO-REPEAT mode, BC FRAME-IN-PROGRESS will automatically return to a value of logic "1" just prior to the start of the first SOM sequence for the new frame.

BC MESSAGE-IN-PROGRESS (Read Only): This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit will return a value of logic "1" during the processing of all BC messages. This bit will transition from logic "0" to logic "1" just prior to each BC Start-of-Message (SOM) sequence and return to logic "0" following the completion of each BC End-of-Message (EOM) sequence.

For RT mode with ALTERNATE STATUS WORD ENABLE, bit 5 of Configuration Register #3, set to logic "0," the ACE/Mini-ACE's RT Status Word will comply with MIL-STD-1553B. In this mode, bits 11 through 7 and bit 0 are defined as follows:

DYNAMIC BUS CONTROL ACCEPTANCE: If this bit is logic "0," it enables the ACE/Mini-ACE RT to respond with the DYNAMIC BUS CONTROL ACCEPTANCE bit set in its RT Status Word in response to a Dynamic Bus Control mode code command (but **not** in response to other commands). If this register bit is logic "1," the DYNAMIC BUS CONTROL ACCEPTANCE Status Word bit will always be low.

$\overline{\text{BUSY}}$: If this bit is logic "0," the BUSY bit in the RT Status Word will be set (logic "1"). The ACE/Mini-ACE will not transmit any Data Words in response to a transmit command if its BUSY bit is set. If the BUSY Status Word bit is set and BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3, is programmed to logic "0," the ACE will store received Data Words in the shared RAM. However, if the BUSY bit in the RT Status Word is set and BUSY RECEIVE TRANSFER DISABLE has been programmed to logic "1," received Data Words **will not** be transferred to the ACE/Mini-ACE shared RAM.

If $\overline{\text{BUSY}}$ is logic "1," the BUSY bit in the transmitted RT Status Word will be logic "0," unless: ENHANCED MODE is enabled (bit 15 of Configuration Register #3 is logic "1") **and** BUSY LOOKUP TABLE ENABLED (bit 13 of Configuration Register #2__s logic "1") **and** the bit corresponding to the Broadcast-$T/\overline{R}$ bit-Subaddress fields of the current Command Word has been programmed to logic "1" in the Busy Lookup Table (address locations 0240-0247 in shared RAM).

SERVICE REQUEST: If this bit is logic "0," the SERVICE REQUEST bit in the RT Status Word will be set. If the CLEAR SERVICE REQUEST BIT (bit 2) of Configuration Register #2 is set, the value of $\overline{\text{SERVICE REQUEST}}$ will be automatically toggled from logic 0 to logic 1 **after** the ACE has responded to a Transmit Vector Word mode command.

SUBSYSTEM FLAG: If this bit is logic "0," the SUBSYSTEM FLAG bit in the RT Status Word will be set. The Subsystem Flag Status Word bit will also be set whenever the $\overline{\text{SSFLAG}}$ input Signal to the ACE/Mini-ACE is asserted low. It should be noted that the sense of the $\overline{\text{SSFLAG}}$ input pin **does not** effect the status of the $\overline{\text{SUBSYSTEM FLAG}}$ register bit.

$\overline{\text{RTFLAG}}$: This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If programmed to logic "0," it causes the Terminal Flag bit in the ACE/Mini-ACE's RT Status Word to be set. The Terminal Flag bit transmitted in the RT Status Word will also become set if RTFAIL-RTFLAG AUTOWRAP ENABLE, bit 2 of Configuration Register #3, is programmed to logic "1" and either a transmitter timeout (668 µs) condition had occurred **or** the ACE/Mini-ACE RT had failed its loopback test on the previous nonbroadcast message. The loopback test verifies validity (sync, encoding, bit count, parity) for the received version of every word transmitted by the ACE/Mini-ACE RT and verifies that the received version of the last transmitted word matches the transmitted version.

RT MESSAGE-IN-PROGRESS (Read Only): This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit returns a logic "1," it indicates that the ACE/Mini-ACE RT is currently processing a message. The RT MESSAGE IN PROGRESS bit is asserted to logic "1" just prior to the RT Start-of-Message (SOM) sequence, and returns to logic "0" just following the completion of the RT End-of-Message (EOM) sequence.

For RT mode with ALTERNATE STATUS WORD ENABLE, bit 5 of Configuration

Register #3, set to logic "1," *all 11* bits of the ACE's RT Status Word are programmable by the host processor. The alternate Status Word may only be used in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). In this mode, bits 11 through 0 are defined as follows:

S10 through S0: For 1553A and McAir applications, direct software control over the eleven (11) lower RT Status Word bits is allowed. S10 controls the bit in bit time 9 (the first bit after the RT Address field)...S0 controls the bit in bit time 19 (LSB). Note that the logic sense of S10-S0

is the **same** (no inversion) as that of the respective transmitted RT Status Word bits. It should be noted that the Message Error Status Word bit, controlled by S10, will **also** be set if a particular command (broadcast-$T/\overline{R}$ bit-subaddress-word count/mode code) has been illegalized.

RT MESSAGE-IN-PROGRESS (Read Only): If this bit returns a logic "1," it indicates that the ACE/Mini-ACE RT is currently processing a message. The RT-MESSAGE-IN-PROGRESS bit is asserted to logic "1" just prior to the RT Start-of-Message (SOM) sequence, and returns to logic "0" following the completion of the RT End-of-Message (EOM) sequence.

For Monitor (MT) mode with ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1," bits 11 through 0 are defined as indicated below. Note these bits have no effect in Monitor mode if ENHANCED MODE ENABLE is programmed to logic "0."

TRIGGER ENABLED: This bit must be set to logic "1" in order to activate the MT trigger logic. The Monitor Trigger capability is applicable only for the Word Monitor mode. It is **not** applicable for the Message Monitor mode. The trigger event is either a pattern match of a valid, received 1553 Command Word with the contents of the Monitor Trigger Register or an external pulse presented to the ACE/Mini-ACE's EXT_TRIG input. EXTERNAL TRIGGER ENABLED must also be programmed to logic "1" to allow use of the EXT_TRIG input signal. The MT trigger may be used to start monitoring, stop monitoring, set a register bit, and/or result in an interrupt request.

START-ON-TRIGGER: If this bit is set, the ACE/Mini-ACE will start storing words following reception of a valid 1553 Command (or Status) Word that matches the word programmed in the Monitor Trigger Register. The word that resulted in the trigger condition will be the first word stored.

STOP-ON-TRIGGER: If this bit is set, the ACE/Mini-ACE will stop storing words following reception of a valid 1553 Command Word that matches the word programmed in the Monitor Trigger Register. The Command Word that resulted in the trigger condition will be the last word stored.

EXTERNAL TRIGGER ENABLE: If this bit is set to logic "1," it allows an external signal delivered to the ACE/Mini-ACE's EXT_TRIG input pin to serve as a monitor trigger.

MONITOR ENABLED (Read Only): This bit will return a value of logic "1" whenever the ACE/Mini-ACE's monitor is in its on-line state. The ACE/Mini-ACE's MT is considered to be "on-line" after it has been

started by a MT Start Command (writing a logic "1" to bit 1 of the Start/Reset Register), even if a trigger condition (if enabled) has not yet occurred.

MONITOR TRIGGERED (Read Only): This bit is applicable for the Word Monitor mode only. It is not applicable (will always return logic "0") in the Message Monitor mode. This bit reverts to logic "0" following a Word Monitor START command (writing logic "1" to bit 1 of the Start/Reset Register). This bit gets set to logic "1" after an enabled trigger condition has occurred. The two trigger conditions, which are enabled by means of bits 11 and 7 of Configuration Register #1, are reception of a valid Command Word to the Monitor Trigger Register (bit 11) or receipt of an EXT_TRIG signal, if enabled. Once asserted, MONITOR TRIGGERED will remain logic "1" until either the ACE/Mini-ACE is reset or the Monitor is stopped. If the Monitor is stopped by a trigger condition (enabled by bit 9 of Configuration Register #9 set to logic "1"), MONITOR TRIGGERED will remain logic "1" until the Monitor is restarted.

MONITOR ACTIVE (Read Only): In the Word Monitor mode, this bit will return a logic "1" after the Word Monitor has been started. That is, after the Word Monitor has been started by a MT Start Command (writing a logic "1" to bit 1 of the Start/Reset Register), even if a trigger condition (if enabled) has not yet occurred. In the Message Monitor mode, MONITOR ACTIVE will return logic "1" only when the Message Monitor is currently storing the words of a selected message. MONITOR ACTIVE will return logic "0" when the monitor is in its off-line state.

4.7 CONFIGURATION REGISTER #2 (Register Address 00010; READ/WRITE)

TABLE 32. CONFIGURATION REGISTER #2 (READ/WRITE 02h)

BIT	DESCRIPTION
15(MSB)	ENHANCED INTERRUPTS
14	RAM PARITY ENABLE
13	BUSY LOOK UP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDR DISBL
9	TIME TAG RESOLUTION 2 (TTR2)
8	TIME TAG RESOLUTION 1 (TTR1)
7	TIME TAG RESOLUTION 0 (TTR0)
6	CLEAR TIME TAG ON SYNCHRONIZE
5	LOAD TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/PULSE INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST
1	ENHANCED RT MEMORY MANAGEMENT
0(LSB)	SEPARATE BROADCAST DATA

ENHANCED INTERRUPTS ENABLE: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit controls the operation of the Interrupt Mask and Status Registers. If this bit is programmed to logic "0," the only interrupt conditions that may be enabled are those that are enabled by bits 7-0 in the Interrupt Mask Registers. In addition, if ENHANCED INTERRUPTS ENABLED is logic "0," the respective bit(s) in the Interrupt Status Register update **only** if the corresponding bit(s) is (are) set in the Interrupt Mask Register.

If this bit is set to logic "1" (enabled), **all 15** possible interrupt conditions may be enabled by means of bits 14-0 of the Interrupt Mask Register. In addition, if ENHANCED INTERRUPT ENABLE is logic "1," the various bits in the Interrupt Status Register may become set **regardless** of the value of the corresponding Interrupt Mask Register bits.

RAM PARITY ENABLE: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). RAM PARITY ENABLE, when set to logic "1," enables parity checking for 17-bit buffered RAM. This entails generating a 17th bit (parity bit) for ALL (both processor and 1553) RAM write accesses and parity checking for ALL RAM read accesses. If the parity check fails for any read access, an interrupt request may be issued (if enabled) and a bit set in the Interrupt Status Register.



Note: *It is important to note that for the BU-65170/78/79, BU-61580/88, BU-61590, BU- 61688/89 ACE/Mini-ACE products, there is NO 17-bit buffered RAM. For these products, RAM parity is not implemented.*

Therefore, RAM PARITY ENABLE must be set to logic "0" for these products.

The RAM parity feature may be utilized with the BU-61585 version of the ACE or with the BUS-65620 digital monolithic. The BU-61585 contains an internal 8K x 17 RAM and supports RAM parity generation and checking. The BU-65620 supports RAM parity generation and checking by interfacing external 17-bit RAM (64K x 17 max) to the "buffered" side of the BU-65620.

BUSY BIT LOOKUP TABLE ENABLE: This bit is applicable only in the ENHANCED RT mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit allows the host processor to optionally set the busy bit in the RT status response, based on broadcast, and the T/$\overline{R}$, and subaddress fields of received Command Words. Setting this bit to logic "1" enables a lookup table in a fixed area of the RAM (hex locations 0240-0247). Placing a logic "1" in the proper bit location in the Busy table will cause the ACE/Mini-ACE RT to respond to the selected command with the BUSY bit set. Programming BUSY BIT LOOKUP TABLE ENABLE to logic "0" disables the busy bit lookup table and frees up the fixed area of RAM.

RECEIVE SUBADDRESS DOUBLE BUFFERING ENABLE: This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). The receive subaddress double buffering feature supports double buffering either globally, or on a subaddress basis for individual receive (and broadcast receive) subaddresses. If RECEIVE SUBADDRESS DOUBLE BUFFERING ENABLE is programmed to a value of logic "0," the subaddress double buffering feature is disabled for **all** receive and broadcast receive subaddresses. If RECEIVE SUBADDRESS DOUBLE BUFFERING ENABLE is programmed to a value of logic "1" and ENHANCED RT MEMORY MANAGEMENT, bit 1 of this register, is programmed to logic "0," the subaddress double buffering feature will be invoked for **all** receive (and broadcast receive) subaddresses. If both ENHANCED RT MEMORY MANAGEMENT and RECEIVE SUBADDRESS DOUBLE BUFFERING ENABLE are programmed to logic "1," the subaddress double buffering feature may be invoked for individual receive (and broadcast receive) subaddresses by setting bit 15 of the respective Subaddress Control Word(s) to logic "1" and programming the appropriate "memory management" bits (MM2, MM1, MM0) to values of 000.

OVERWRITE INVALID DATA: This bit effects the operation of the RT circular buffer memory management mode. If the bit is logic 0, the ACE will update the value of the Lookup Table pointer address for the respective Tx/Rx-Bcst-subaddress following transmit messages as well as following both valid **and** invalid receive messages. In addition, if the

bit is logic 0, an interrupt request for a circular buffer rollover condition (if enabled) will be issued **immediately after** the word at the lower address boundary of the respective circular buffer has been accessed. If OVERWRITE INVALID DATA is logic 1, the Lookup Table address pointer will only be updated following a transmit message or following a **valid** receive or broadcast message to the respective Rx/Bcst subaddress. If the bit is logic 1, the Lookup Table pointer **will not** be updated following an invalid receive or broadcast message. In addition, if the bit is logic 1, an interrupt request for a circular buffer rollover condition (if enabled) will occur only **following the end** of a transmit message during which the last location in the circular buffer has been read or **following the end** of a **valid** receive or broadcast message in which the last location in the circular buffer has been written to.

256-WORD BOUNDARY DISABLE: This bit controls the ACE/Mini-ACE's memory management scheme for BC message blocks and for RT data blocks for both the default (global single message) mode as well as for any individual subaddresses in the ENHANCED mode for which the "single message" or "double buffered" options are selected. If this bit is logic "0," the rollover at 256-word boundaries is enabled. That is, when the 1553 memory management logic is processing a message, its memory address will roll over from XXFF (hex) to XX00, rather than increment to (XX+1)00. If this bit is logic "1," the memory management logic will enable 256-Word boundaries to be crossed for BC Message Blocks as well as for RT Data Blocks in both the Default (bit 1 of this register = 0) and Enhanced Memory Management/Single Buffer modes. In this instance, the address will increment from XXFF to (XX+1)00, when a 256-word boundary is encountered in the shared RAM address space. It should be noted that 256-WORD BOUNDARY DISABLE has **no effect** on the BC or RT Command Stack. That is, for the stack area of RAM in both BC and RT modes, the rollover at 256-(or 512-, 1024-, 1024-) word boundaries is **always** enforced.



It should also be noted that if 256-WORD BOUNDARY DISABLE is programmed to logic "1" in RT mode, the size for all circular buffers becomes 65,536 words, regardless of the programming of the respective Subaddress Control Word bits.

Note: *It is strongly recommended that 256-WORD BOUNDARY DISABLE be programmed to logic "1" for BC mode, and to logic "0" for RT mode.*

TIME TAG RESOLUTION 2,1,0: These bits allow the resolution of the time tag register to be selected by means of software control. The choices are 64 µs (default), 32 µs, 16 µs, 8 µs, 4 µs, 2 µs, and EXTERNAL CLOCK. There is also a test mode for the Time Tag register. Time Tag resolution is programmed as described in TABLE 33.

TABLE 33. TIME TAG RESOLUTION			
BIT 9 TTR2	BIT 8 TTR1	BIT 7 TTR0	TIME TAG RESOLUTION
0	0	0	64 µs
0	0	1	32 µs
0	1	0	16 µs
0	1	1	8 µs
1	0	0	4 µs
1	0	1	2 µs
1	1	0	TEST MODE
1	1	1	EXTERNAL CLOCK

Note: In the Time Tag TEST MODE, the Time Tag Register only increments when the CPU writes a logic "1" to bit 4 of the Start/Reset Register (TIME TAG TEST CLOCK).

CLEAR TIME TAG ON SYNCHRONIZE: If this bit is set, reception of a Synchronize (without data) mode command, in RT mode, will cause the value of the internal Time Tag Register to clear to 0000.

LOAD TIME TAG ON SYNCHRONIZE: If this bit is set, reception of a Synchronize (with data) mode command, in RT mode, will cause the Data Word from the Synchronize message to be loaded into the Time Tag Register.

INTERRUPT STATUS AUTO CLEAR: If this bit is logic "1," the value of the Interrupt Status Register will clear to 0000 **after** it has been read by the host processor. Also, if both the INTERRUPT STATUS AUTO CLEAR and LEVEL/PULSE Interrupt Request (bit 3) are logic "1," the ACE/Mini-ACE's Interrupt Request output $\overline{\text{INT}}$ will be cleared (high) after the Interrupt Status Register has been read.

LEVEL/$\overline{\text{PULSE}}$ INTERRUPT REQUEST: If this bit is logic "0," the Interrupt Request output, $\overline{\text{INT}}$, will be a negative pulse of approximately 500 ns width. If this register bit is logic "1," an interrupt will be requested by asserting $\overline{\text{INT}}$ as a low level. If the level option is selected, $\overline{\text{INT}}$ will be reset high after the Interrupt Status Register has been read (provided that the INTERRUPT STATUS AUTO CLEAR [bit 4] is set), or when a "1" is written to the INTERRUPT RESET bit (bit 2) of the Start/Reset Register. In addition, for the BU-65620 digital monolithic or the BU-61590 universal ACE terminal, $\overline{\text{INT}}$ may also be cleared to logic "1" by presenting a low level on the $\overline{\text{IACK}}$ (Interrupt Acknowledge) input. The power turn-on mode for this bit is "0," enabling a pulse $\overline{\text{INT}}$ output.

CLEAR SERVICE REQUEST: If this bit is logic "0," the Service Request RT Status word bit may be controlled only by the host processor software. If the bit is logic "1," the Service Request bit may still be set and cleared under software (register) control. In addition, the $\overline{\text{SERVICE REQUEST}}$ Configuration Register (#1) bit will automatically clear

(go to logic 1) **after** the ACE/Mini-ACE RT has responded to a Transmit Vector Word mode code command. That is, if the CLEAR SERVICE REQUEST bit is set to 1 while $\overline{\text{SERVICE REQUEST}}$ is set to 0, the ACE/Mini-ACE RT will respond with the Service Request Status bit set for all commands until the RT responds to a Transmit Vector Word command. In this instance, the ACE will respond with the Service Request **still set** in the Status Word for this message. **Following** this message, $\overline{\text{SERVICE REQUEST}}$ in the Configuration Register automatically clears to a logic "1." It stays logic "1" (cleared) for subsequent messages until it is reasserted to a logic "0" by the host processor.

ENHANCED RT MEMORY MANAGEMENT: If this bit is logic "0," the ACE/Mini-ACE RT memory management defaults to either a **global** single Data Word buffer or a double Data Word buffer for each transmit, receive, and (optionally) broadcast subaddress: single message, for all transmit subaddresses; single message, for all receive (and broadcast receive) subaddresses if RX SUBADDRESS DOUBLE BUFFER ENABLE (bit 12 of this register) is logic programmed to "0."

If ENHANCED MODE (bit 15 of Configuration Register #3 is logic "1") **and** RX SUBADDRESS DOUBLE BUFFER ENABLE are logic "1," double buffering is provided for **all** receive/broadcast subaddresses. In the single message mode, each data block is repeatedly overread or overwritten. If ENHANCED RT MEMORY MANAGEMENT is logic "1," the ACE/Mini-ACE RT memory management capability is expanded to allow for either the "single-buffer" mode, the "double buffer" (redundant mailbox) mode, or for a variable-sized circular buffer (128 to 8192 words) to be programmed on an individual basis for each transmit, receive and broadcast subaddress. Note that subaddress double buffering is applicable for receive (and broadcast) subaddresses, but **not** for transmit subaddresses.

SEPARATE BROADCAST DATA: If this bit is logic "0," the data pointers for both broadcast as well as nonbroadcast receive messages are stored in a common portion (the "receive" portion) of the RT Lookup Table. If this bit is logic "1," broadcast data is separated from nonbroadcast receive data by means of separate areas of the RT Lookup Tables provided for broadcast messages.

4.8 START/RESET REGISTER (Register Address 00011; WRITE ONLY)

The Start/Reset Register is a write only register. It provides command functions for resetting the entire ACE terminal, for initiating BC or Monitor operation, for resetting the Interrupt Status Register and Interrupt Request Output and for resetting the value of the Time Tag Register. It also contains bits to facilitate testing of the Time Tag Register and to stop the ACE BC at the end of the current message or the current frame.

TABLE 34. START/RESET REGISTER (WRITE 03h)

BIT	DESCRIPTION
15(MSB)	RESERVED
14	RESERVED
13	RESERVED
12	RESERVED
11	RESERVED
10	RESERVED
9	RESERVED
8	RESERVED
7	RESERVED
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0(LSB)	RESET

BC/SELECTED MT STOP-ON-MESSAGE: Writing a value of logic "1" to this bit causes the ACE/Mini-ACE to assume its off-line BC or Selected Monitor mode following the completion of the current message. If there is no message currently being processed, the ACE/Mini-ACE halts operation immediately.

BC STOP-ON-FRAME: Writing a value of logic "1" to this bit causes the ACE/Mini-ACE to assume its off-line BC mode following the completion of the current BC frame. If the ACE/Mini-ACE is currently waiting to start the next BC frame when BC STOP-ON-FRAME is written to as logic "1," the ACE/Mini-ACE will halt its BC operation immediately.

TIME TAG TEST CLOCK: When the TIME TAG RESOLUTION bits are programmed for the Time Tag Test Mode (bits 9, 8 and 7 of Configuration Register #2 are programmed to 1 1 0), writing a logic "1" to this bit will cause the value of the Time Tag register to increment by 1. In the Time Tag Test Mode, the Time Tag Register **will only** increment when a logic "1" is written to TIME TAG TEST CLOCK.

TIME TAG RESET: Writing a logic "1" to this bit causes the value of the Time Tag Register to Reset to zero (0000).

INTERRUPT RESET: Writing a "1" to this bit resets the value of the Interrupt Status Register to 0000 (except for the RT ADDRESS PARITY ERROR bit, if the condition persists). In addition, if the $\overline{\text{PULSE}}$/LEVEL Configuration Register bit is set to a "1," writing a "1" to this bit clears the $\overline{\text{INT}}$ output to logic "1."

BC/MT START: When a logic "1" is written to this bit in BC mode, the ACE/Mini-ACE starts processing its programmed frame of BC messages. When a logic "1" is written to this bit in MT mode, the ACE/Mini-ACE Monitor goes on-line and starts storing received words to the shared RAM. It should be noted that an MT START command **is required** to start either the Word Monitor or the Selective Message Monitor, in the Monitor (**only**) mode. However, in the combined RT/Selective Monitor mode, an MT START command **is not** required. That is, assuming the ACE/Mini-ACE is in the ENHANCED mode, the RT and MT will go on-line **immediately** after Configuration Register #1 has been programmed for the RT/Selective Monitor mode.

RESET: This bit provides software reset capability for the ACE/Mini-ACE. When a logic "1" is written to this bit, any message in progress in BC or RT modes is immediately aborted. In Monitor mode, the ACE goes off-line **immediately** and stops storing received words. All other registers are reset to 0000 (hex); all internal states are reinitialized to their default (power turn-on) conditions.

4.9 COMMAND STACK POINTER REGISTER (Register Address 00011; Read Only)

This register provides the host processor read access to the current value of the Stack Pointer in BC, RT, and Message Monitor modes.

In BC mode, the value of the Command Stack Pointer Register will be **the same** as the value of the Active Area Stack Pointer memory location.

For RT, Selective Monitor, and the combined RT/MT modes, the value read from the Stack Pointer Register will always be **four less** (modulo the command stack size) than the value read from the Active Area Stack Pointer location in the shared RAM. In RT, Selective Monitor, and combined RT/Selective Monitor modes, the value of the Stack Pointer Register is incremented by four during the Start-of-Message (SOM) sequence, from the value of the descriptor pointer for the **previous** message to the value of the descriptor pointer for the **current** message.

In the SOM sequence for the combined RT/Selective Monitor mode, the Stack Pointer Register will update to the current **RT Command Stack**

pointer for RT messages, and to the **Monitor Command Stack Pointer** for Monitor messages.

In BC mode, the value of the Stack Pointer Register is incremented by four during the End-of-Message (EOM) sequence, from the descriptor pointer for the **current** message to the descriptor pointer for the **next** message.

The Stack Pointer Register is **not used** in the Word Monitor mode.

It should be noted that the BC/RT Command Stack size defaults to 256 in the non-ENHANCED mode. In the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"), the stack size is programmable for 256, 512, 1024, and 2048 words by means of bits 14 and 13 of Configuration Register #3.

TABLE 35. BC/RT COMMAND STACK POINTER REGISTER (READ 03h)

BIT	DESCRIPTION
15(MSB)	COMMAND STACK POINTER 15
•	•
•	•
•	•
0(LSB)	COMMAND STACK POINTER 0

4.10 BC CONTROL WORD/RT SUBADDRESS CONTROL WORD REGISTER (Register Address 00100; Read/Write)

As a mechanism to facilitate self-test, this register provides read/write accessibility for the current BC Control Word or RT Subaddress Control Word. While this register can **always** be read by the host CPU, it should be noted that it cannot be written by the CPU: (1) when the ACE/Mini-ACE is programmed for RT or Monitor mode, **or** (2) during the processing of a frame of messages when in BC mode. The BC CONTROL WORD/RT SUBADDRESS REGISTER **may** be written when the ACE/Mini-ACE is in "Idle" BC mode, that is, when it is programmed for BC mode (via bits 15 and 14 of Configuration Register #1) but **not** currently processing a frame of messages.

TABLE 36. BC CONTROL WORD REGISTER (READ/WRITE 04h)

BIT	DESCRIPTION
15(MSB)	RESERVED
14	M. E. MASK
13	SERVICE REQUEST BIT MASK
12	SUBSYS BUSY BIT MASK
11	SUBSYS FLAG BIT MASK
10	TERMINAL FLAG BIT MASK
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/$\overline{B}$
6	OFF LINE SELF TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-TO-RT FORMAT

TABLE 37. RT SUBADDRESS CONTROL WORD (READ/WRITE 04h)

BIT	DESCRIPTION
15(MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

4.11 TIME TAG REGISTER (Register Address 00101; READ/WRITE)

TABLE 38. TIME TAG REGISTER (READ/WRITE 05h)	
BIT	**DESCRIPTION**
15(MSB)	TIME TAG 15
•	•
•	•
•	•
0(LSB)	TIME TAG 0

TABLE 39. TIME TAG REGISTER RESOLUTION				
CONFIGURATION REGISTER #2			TIME TAG RESOLUTION	ROLLOVER TIME (MODULUS)
BIT 9 TTR2	BIT 8 TTR1	BIT 7 TTR0		
0	0	0	64 µs	4.194 sec
0	0	1	32 µs	2.097 sec
0	1	0	16 µs	1.048 sec
0	1	1	8 µs	524 ms
1	0	0	4 µs	262 ms
1	0	1	2 µs	131 ms
1	1	0	TEST MODE	N/A
1	1	1	EXTERNAL CLOCK	N/A

The Time Tag Register provides the output of a free-running counter. The resolution of the counter is programmable by means of bits 9, 8, and 7 of Configuration Register #2 from among 64, 32, 16, 8, 4 and 2 us/LSB. There is also a test mode in which the Time Tag register may be incremented one LSB at a time under software control for the purpose of self-test. In addition, the time tag register may be clocked from an external source, by means of the TAG_CLK input. **Note:** The Mini-ACE series does not contain a TAG_CLK input pin for use with an external clock source.

The Time Tag Register is reset to zero following hardware or software RESET, a TIME TAG RESET (bit 3 of the Start/Rest Register), or after the ACE has received a Synchronize (without data) mode code and bit 6 of Configuration Register #2 is logic "1." The Time Tag Register is loaded by the received Data Word following reception of a Synchronize (with data) mode code, provided that bit 5 of Configuration Register #2 is logic "1."

4.12 INTERRUPT STATUS REGISTER (Register Address 00110; Read Only)

The Interrupt Status Register allows the host processor to determine the cause of an interrupt request by means of a single READ operation. There are sixteen bits in this register. This register will be cleared **after** it has been read, if the CLEAR INTERRUPT STATUS AUTO CLEAR bit (bit 4) of Configuration Register #2 is logic "1." The register will also be cleared if the host processor writes a logic "1" to the INTERRUPT RESET bit (bit 2) of the Start/Reset Register.

The following considerations are necessary when reading the Interrupt Status Register in 8-bit zero wait mode, 8-bit non-zero wait mode and 16-bit zero wait mode. This is to ensure that subsequent interrupt events after a triggering read of an ISR result in bit(s) being set in the respective ISR (i.e. to avoid interrupting events becoming “lost”).

- For 8-bit zero wait mode, the address of the Interrupt Status Register *must* be used for the triggering read transfer prior to the actual read of data.
- For the first read, data is either “thrown away”, or possibly used (if data is used, then it is for a memory or register address presented on an *earlier* triggering transfer).
- For the second read (non-triggering), the register address presented does not matter (for the case of SP’ACE II, this must be a *register*, rather than memory address).
- For the third read (triggering), the register address presented on *this* transfer must *not* be that of the ISR. This is to avoid an inadvertent clearing of the indication of a new interrupt, which would be “missed” by a subsequent read of the Interrupt Status Register.

Alternatively, this address can either be register address 0x0000 or that of some other register or memory address to be read next. Ideally, the host should be reading the values of Interrupt Status Register as an atomic instruction, meaning that interrupts should be disabled during this time, to avoid the possibility of the processor being interrupted in the middle of this read(s).

- For 8-bit non-zero wait mode, for reading an ISR, that ISR address must be presented on the triggering (first) transfer. The address presented on the subsequent non-triggering read is a “don’t care”. The only exception is for the case of SP’ACE II, where the address for the non-triggering read must be a *register* read, rather than a memory read, with a suggested register address of 0x0000.

- For 16-bit zero wait mode, all transfers are triggering. However, it is important that for the operation in which the ISR value is actually read – that is, the read transfer *after* the ISR address has been presented – that some register or memory address *other than* that of the ISR be presented. This an be register address 0x0000, or some other register or memory address.

The 16 bits of this register are: MASTER INTERRUPT, RAM PARITY ERROR, TRANSMITTER TIMEOUT, BC/RT COMMAND STACK ROLLOVER, MONITOR COMMAND STACK ROLLOVER, MONITOR DATA STACK ROLLOVER, HANDSHAKE FAILURE, BC RETRY, RT ADDRESS PARITY ERROR, TIME TAG ROLLOVER, RT SUBADDRESS CIRCULAR BUFFER ROLLOVER, RT SUBADDRESS CONTROL WORD END-OF-MESSAGE (EOM) or SELECTED BC END-OF-MESSAGE (EOM), BC_END_OF FRAME, FORMAT ERROR, BC STATUS SET/RT SELECTED MODE CODE INTERRUPT/MONITOR PATTERN TRIGGER, AND EOM.

It should be noted that for the non-ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 programmed to logic "0"), only bits 7-0 of the Interrupt Status Register are active. In the ENHANCED MODE (bit 15 of Configuration Register #3 set to logic "1"), **and** ENHANCED INTERRUPTS enabled (bit 15 of Configuration Register logic #2 is logic "1"), all 15 bits (14-0) may become set.

It should also be noted that in the non-ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, programmed to logic "0"), bits 7 through 0 of the Interrupt Mask Register are used to **both** enable interrupts for the various events/conditions **and** to enable the respective bits of the Interrupt Status Register to be set. That is, the various bits of the Interrupt Status Register will **not** become set if the corresponding bits of the Interrupt Mask Register are not set. Bits 14-8 are not used in the non-ENHANCED mode.

The ENHANCED mode, with ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 programmed to logic "1"), supports polling (non-interrupting) applications. In this mode, the value of the Interrupt Mask Register bits has no effect on the operation of the respective Interrupt Status Register bits. If ENHANCED INTERRUPTS are enabled, the bits of the Interrupt Status Register **do not need to be enabled** by the corresponding bits in the Interrupt Mask Register. In the ENHANCED INTERRUPT mode, these bits become set following the occurrence of the respective event/condition, regardless of the status of the corresponding Interrupt Status Mask bit. In either mode, an interrupt for any of the 15 event/conditions (8 in non-ENHANCED mode) is only enabled if the respective bit of the Interrupt Mask Register (for the event/condition) has been programmed to logic "1."

TABLE 40. INTERRUPT STATUS REGISTER (READ/WRITE 06h)	
BIT	**DESCRIPTION**
15(MSB)	MASTER INTERRUPT
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAILURE
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	BC CONTROL WORD/ RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

MASTER INTERRUPT: If ENHANCED INTERRUPTS are enabled (bit 15 of Configuration Register #2 set to logic “1”) then the MASTER INTERRUPT will only be asserted when any of the other 15 lower bits of the Interrupt Status Register have been set to logic “1” (i.e. this bit reflects the state of the interrupt request output from the ACE/Mini-ACE. A logic “1” indicates that an interrupt request has been issued.

RAM PARITY ERROR: Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") **and** ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If set to logic "1," indicates a RAM parity error. **This bit is NOT applicable for BU-65170/78/79, BU-61580/88, BU-61590, and BU-61688/89.** It is applicable with the BU-61585 and BU-65620 versions of the ACE. The BU-61585 contains internal 8K x 17 RAM. The BU-65620 can be interfaced to up to 64K words of external 17-bit "buffered" RAM.

By programming RAM PARITY ENABLE, bit 14 of Configuration Register #2 to logic "1," the BU-61585 and BU-65620 versions of the ACE can be programmed to generate a single parity bit on all write accesses to 17-bit RAM. A parity check is then performed on all read accesses to the 17-bit RAM. A RAM PARITY ERROR interrupt indicates a failure of this parity check.

TRANSMITTER TIMEOUT: Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") **and** ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit is set to logic "1," this indicates that the ACE/Mini-ACE's transmitter watchdog timer has

timed out. This occurs if the ACE/Mini-ACE's encoder attempts to transmit for longer than 668 µs.

BC/RT COMMAND STACK ROLLOVER: Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") **and** ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit returns a value of logic "1," it indicates a rollover of the BC/RT Command Stack. The size of the BC/RT Command Stack 1 is programmable from among 256 words (64 messages), 512, 1024, and 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register #3.

MESSAGE MONITOR COMMAND STACK ROLLOVER: Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") **and** ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit returns a value of logic "1," it indicates an interrupt following a rollover of the Message Monitor Command Stack. This is applicable for both the Message Monitor as well as the combined RT/Message Monitor modes. The size of the MT Command Stack is programmable from among 256 (64 messages), 1024, 4096, and 16,384 words (4096 messages) by means of bits 12 and 11 of Configuration Register #3.

MONITOR DATA STACK ROLLOVER: Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") **and** ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit returns a value of logic "1," it indicates a rollover of the Word Monitor or Message Monitor Data Stack. The size of the Data Stack is programmable from among 512, 1024, 2048, 4096, 8192, 16,384, 32,768, or 65,536 words by means of bits 10, 9, and 8 of Configuration Register #3.

HANDSHAKE FAILURE: Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") **and** ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If set, enables an interrupt following a handshake timeout during a transfer between the 1553 protocol section and the RAM. A Handshake Failure can only occur in the transparent mode. There are two conditions that can cause a Handshake Failure. For both conditions, the allotted time is 4.4 µs for a 20 MHz clock input, 4.0 µs for a 16 MHz clock, 3.5 µs for a 12 MHz clock, and 3.2 µs for 10 MHz clock input.

1) When the Data Transfer Grant (DTGRT) input is not asserted within the allotted time after the Data Transfer Request

(DTREQ) output is asserted.

2) When the $\overline{\text{STRBD}}$ input signal is held at logic "0" for longer than the allotted time after the ACE/Mini-ACE's $\overline{\text{READYD}}$ output is asserted low at the end of a CPU transfer cycle.

BC RETRY: Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") **and** ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). A value of logic "1" indicates the occurrence of a retried message in BC mode. If enabled, the interrupt will occur regardless of whether the retry attempt was successful or unsuccessful. The interrupt will occur **AFTER the failed message has been retried** (either once or twice, successfully or unsuccessfully).

RT ADDRESS PARITY ERROR: Indicates that the parity sum of RTAD4-RTAD0 and RTADP is even, rather than odd, as required for the ACE to respond to messages directed to its own address in RT mode. It should be noted that if an RT ADDRESS PARITY ERROR condition occurs, the respective Interrupt Status Register bit will clear to logic "0" after the Interrupt Status Register has been read (if AUTO CLEAR is enabled) or after the INTERRUPT RESET bit in the Start/Reset Register has been written as logic "1." The RT ADDRESS PARITY ERROR bit will remain at logic "0" and will not return to logic "1" until either of the following two sequences has occurred: (1) the RT Address parity error condition goes away and then reoccurs, or (2) the RT ADDRESS PARITY ERROR bit in the Interrupt Mask Register is cleared (either by writing "0" to the register bit or by means of either a hardware or software reset to the ACE/Mini-ACE) and is then set back to logic "1," assuming that the address parity error condition persists.

TIME TAG ROLLOVER: Indicates that the 16-bit Time Tag Register has rolled over from FFFF to 0000.

RT SUBADDRESS CIRCULAR BUFFER ROLLOVER: This bit will be set at the end of a message in RT mode, provided that the ACE is in the ENHANCED RT Memory Management mode **and** the "Interrupt at Rollover" bit is set in the Subaddress Control Word for the Tx/Rx/Bcst subaddress of the just completed message **and** the current message caused the data block Lookup Table address pointer to cross the lower boundary of the respective circular buffer, resulting in a rollover.

Note that this interrupt request will occur **immediately** when the address location at the upper boundary of a circular buffer is accessed, if OVERWRITE INVALID DATA (bit 11 of Configuration Register #2) is logic "0." If OVERWRITE INVALID DATA is logic "1," the interrupt request will occur at the end of a **valid** message in which the last location in the circular buffer was accessed. If OVERWRITE INVALID

DATA is logic "1," an RT CIRCULAR BUFFER ROLLOVER **will not** occur following an invalid message.

BC CONTROL WORD/RT SUBADDRESS CONTROL WORD EOM: This bit will be set at the end of a message in RT mode, provided that the ACE is in the Enhanced Memory Management RT mode **and** the "Interrupt at EOM" bit is set in the Subaddress Control Word for the Tx/Rx/Bcst-subaddress of the just completed message. This bit will also be set at the end of a message in BC mode, provided that the ACE/Mini-ACE is in the ENHANCED BC Mode **and** EXPANDED BC CONTROL WORD is enabled (bit 12 of Configuration Register #4 is logic "1") **and** the EOM INTERRUPT ENABLE bit (bit 4) in the current BC Control Word is set to logic "1."

BC END-OF-FRAME: Bus Controller End-of-Frame indicates that an entire programmed BC message frame has been completed. That is, following the end of the last message processed, the Message Count RAM location incremented to FFFF (hex). Note that if BC STOP-ON-ERROR is enabled and a BC frame is aborted before the Message Count has incremented to FFFF (hex), the BC END-OF-FRAME condition will **not** occur.

FORMAT ERROR: Indicates that a completed message, in BC, RT, or Selective Message Monitor Mode, contained one or more of the following errors:

1) **Loop Test Failure:** A loopback test is performed on all messages transmitted by the BC or RT (except broadcast messages in RT mode). The received version of all transmitted words is checked for validity and correct sync type. In addition, a 16-bit comparison is performed on the last word transmitted by the BC or RT. If **any** of these checks or comparisons do not verify, the loopback test is considered to have failed.

2) **Message Error:** A received message contained a violation of the 1553 message validation criteria (encoding, parity, bit count, word count, etc.).

3) **Response Timeout:** In BC mode, an RT has either not responded, or has responded later than the programmed value of the BC No Response Timeout time. In RT mode, if the ACE/Mini-ACE is the receiving RT in an RT-to-RT transfer and the transmitting RT has not responded with its Status Word within the programmed value of the RT-to-RT Response Timeout time after the Transmit Command Word.

BC STATUS SET/RT SELECTED MODE CODE INTERRUPT/MT PATTERN TRIGGER: In BC mode, the RT Status Word received from a responding RT either contained an incorrect RT address field or one of the 8 non-RESERVED Status bits contained an unexpected bit value. The expected value for these 8 bits is normally zero (0), with one exception: If BROADCAST MASK ENABLED/$\overline{\text{XOR}}$ (bit 11 of Configuration Register #4) is logic "0" **and** the MASK BROADCAST bit (bit 5) of the message's BC Control Word is logic "1," the expected value of the Broadcast Command Received bit becomes "1," rather than "0."

In RT mode, this interrupt can only occur in the ENHANCED mode (bit 15 of Configuration Register #3 is set to logic "1") and if Enhanced Mode Code Handling is enabled (bit 0 of Configuration Register #3 is set to logic "1"). If these two bits are set, mode code interrupts for individual broadcast-T/R bit-mode codes may be enabled by setting the appropriate bit(s) in address locations 0108-010F in the shared RAM. Reception of an enabled mode code message will then cause a MODE CODE interrupt to occur at the end of the message.

In the Word Monitor mode, a Pattern Trigger interrupt will occur in the ENHANCED mode (bit 15 of Configuration Register #3 is set to logic "1") following the reception of a valid Command Word that matches the bit pattern programmed in the Monitor Trigger Register.

END OF MESSAGE: End of Message. In BC, RT, or Selective Message Monitor mode, indicates the completion of a message (regardless of validity).

4.13 CONFIGURATION REGISTER #3 (Register Address 00111; READ/WRITE)

TABLE 41. CONFIGURATION REGISTER #3

(READ/WRITE 07h)

BIT	DESCRIPTION
15(MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE $T/\overline{R}$ ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER ENABLE
2	$\overline{\text{RTFAIL}}/\overline{\text{RTFLAG}}$ WRAP ENABLE
1	1553A MODE CODES ENABLE
0(LSB)	ENHANCED MODE CODE HANDLING

ENHANCED MODE ENABLE: If this bit in programmed to logic "0," the functionality of the ACE/Mini-ACE defaults to that of DDC's previous generation processor-to-hybrid, the BUS-61559 Advanced Integrated Mux Hybrid with ENHANCED RT Features (AIM-HY'er). Programming this bit to logic "1" allows many of the ACE/Mini-ACE's advanced features to be enabled by means of the Interrupt Mask Register, the various Configuration Registers, as well as by the BC Control Word and RT Subaddress Control Word. These features include **all** of the functions enabled by the various bits of Configuration Registers #3, 4, and 5. If ENHANCED MODE ENABLE is programmed to logic "0," the operation of these register functions defaults to that indicated by their "logic "0"" state.

For the BU-65620 digital monolithic, it should be noted that the input signal $\overline{\text{ENHANCED_MODE_ENA}}$ must be connected to logic "0" to enable the ENHANCED Mode to be used. If the BU-65620's $\overline{\text{ENHANCED_MODE_ENA}}$ input is connected to logic "1," it will not be possible to program the BU-65620 for ENHANCED mode, and the ENHANCED MODE ENABLE register bit will always return logic "0" when read.

For the SP'ACE and SP'ACE II family of components (BU-61582 {BU-63825}, BU-61583 {BU-63925}, BU-65621) enhanced mode is always enabled and as such, this bit has no effect.

Note: *It should be noted that in order to enable any of the ENHANCED features, ENHANCED MODE ENABLED must be set to logic "1" PRIOR TO setting any of the other Configuration Register bits to enable the ENHANCED features. THIS INCLUDES ANY OF THE FEATURES ENABLED BY THE LOWER 15 bits (14-0) OF CONFIGURATION REGISTER #3, as well as features enabled by other registers. Specifically, bit 15 must first be set by writing 8000 (hex) to Configuration Register #3 BEFORE proceeding to set any of bits 14-0. When these bits are set, ENHANCED MODE ENABLE must continue to be programmed to logic "1."*

In the non-ENHANCED mode, functions activated by the following register bits are active:

- Interrupt Mask Register and Interrupt Status Register, bits 7-0
- Configuration Register #1: for BC mode, bits 15-12; for RT mode (without Alternate Status only), bits 15-13 and 11-8; for Word Monitor mode, bits 15-13
- Configuration Register #2, bits 11-0
- Start/Reset Register, bits 4-0
- BC/RT Command Stack Pointer
- RT Subaddress Control Word Register
- Time Tag Register
- Interrupt Status Register bits 15 and 7-0

In the ENHANCED mode, in addition to all of the non-ENHANCED mode functions, those enabled by the following registers (or register bits) may also be activated:

- Interrupt Mask Register and Interrupt Status Register, bits 14-8
- Configuration Register #1: BC mode, bits 11-0; RT mode, bits 12 and 7-0, and the RT With Alternate Status mode; Monitor, bits 12-9, 7, 2-0; and the Message Monitor and RT/Message Monitor modes
- Configuration Register #2, bits 15-12
- Start/Reset Register, bits 6 and 5
- BC Control Word Register [1]
- Configuration Registers #3, #4, and #5
- RT/Monitor Data Stack Address Register [1]
- BC Frame Time Remaining Register [1]
- BC Time to Next Message Remaining Register [1]

- BC Frame Time [1] /RT Last Command/Monitor Trigger Word [1] Register
- RT Status Word Register
- RT BIT Word Register
- Test Mode Registers 0-7

Note: *1. BC and Monitor Functions not implemented for BU-65170 RT*

For all three modes, use of the ENHANCED Mode enables the various read-only bits (bits 2-0) in Configuration Register #1.

The ACE/Mini-ACE must be in the ENHANCED mode in order to enable ENHANCED INTERRUPTS (by setting bit 15 of Configuration Register #2 to logic "1").

For BC mode, the features that require ENHANCED MODE ENABLE programmed to logic "1" include the expanded BC Control Word and BC Block Status Word, additional STOP-ON-ERROR and STOP-ON-STATUS SET functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message.

For RT mode, the features that require ENHANCED MODE ENABLE programmed to logic "1" include the expanded RT Block Status Word, the combined RT/Selective Message Monitor mode, internal wrapping of the "$\overline{\text{RTFAIL}}$" output signal to the "$\overline{\text{RTFLAG}}$" input signal, the double buffering scheme for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word, and the busy bit lookup table option.

For MT mode, use of the ENHANCED Mode enables use of both the Selective Message Monitor and the combined RT/Selective Monitor modes, as well as use of the monitor triggering capability.

BC/RT COMMAND STACK SIZE 1,0: These two bits select the size of the BC/RT Command Stack. The default value for both bits is logic "0," which specifies a stack size of 256 words (64 messages). TABLE 42 illustrates the BC/RT Command Stack Sizes.

TABLE 42. BC/RT COMMAND STACK SIZE		
BIT 14 BC/RT CMD STACK SIZE 1	**BIT 13 BC/RT CMD STACK SIZE 0**	**BC/RT STACK SIZE (WORDS)**
0	0	256 (64 messages)[1]
0	1	512 (128 messages)
1	0	1024 (256 messages)
1	1	2048 (512 messages)

Note: Default size is 256 words (64 messages)

MONITOR COMMAND STACK SIZE 1,0: These two bits select the size of the Monitor Command Stack. The default value for these two bits is logic "00," which specifies a stack size of 256 words. TABLE 43 illustrates the MT Command Stack Sizes.

TABLE 43. MONITOR COMMAND STACK SIZE		
BIT 12 MT CMD STACK SIZE 1	**BIT 11 MT CMD STACK SIZE 0**	**MONITOR STACK SIZE (WORDS)**
0	0	256 (64 messages)[1]
0	1	1024 (256 messages)
1	0	4096 (1024 messages)
1	1	16384 (4096 messages)

Note: 1. Default size is 256 words (64 messages)

MONITOR DATA STACK SIZE 2,1,0: These three bits select the size of the Monitor Data Stack. This stack is used in both the Word Monitor and Message Monitor modes. The default value for these three bits is logic "000," which specifies a stack size of 65,536 words. TABLE 44 illustrates the MT Data Stack Sizes.

TABLE 44. MT DATA STACK SIZE			
BIT 10 MT DATA STACK SIZE 2	**BIT 9 MT DATA STACK SIZE 1**	**BIT 8 MT DATA STACK SIZE 0**	**MONITOR DATA STACK SIZE (WORDS)**
0	0	0	65,536 (default)
0	0	1	32,768
0	1	0	16,384
0	1	1	8,192
1	0	0	4,096
1	0	1	2,048
1	1	0	1,024
1	1	1	512

ILLEGALIZATION DISABLED: For RT mode. If this bit is programmed to logic "0," the ACE/Mini-ACE's internal RT Command illegalization feature is **enabled.** That is, shared RAM address locations 0300 to 03FF (hex) are dedicated to the illegalization function. If this bit is programmed to logic "1," the illegalization function is disabled. In this configuration, addresses 0300 through 03FF may be used for the storage of Stack or message data. This bit has no effect for BC or MT modes.

It should be noted that for the BU-65620 digital monolithic, the value of ILLEGALIZATION DISABLED is affected by the input signal EXT_ILL_ENA. If EXT_ILL_ENA is connected to logic "0," illegalization is **disabled**. In this case, ILLEGALIZATION DISABLED will **always** return logic "1" when read. If EXT_ILL_ENA is connected to logic "1," enabling illegalization for the BU-65620 is software programmable, as described in the preceding paragraph. For BU-65170/78/79, BU-61580, BU-61585/88, BU-61590, and BU-61688/89, the use of illegalization is **always** software programmable, as described above.

OVERRIDE MODE CODE $T/\overline{R}$ BIT ERROR: For RT mode. If this bit is programmed to logic "0," a mode code Command Word with a $T/\overline{R}$ bit of logic "0" and an MSB of the mode code field of "0" (receive mode codes 0 to 15) is considered an undefined Command Word. In this configuration, the ACE/Mini-ACE RT will not respond to such a command and the AC/Mini-ACE RT's Message Error bit will be set. If this bit is programmed to logic "1," a mode code Command Word with a $T/\overline{R}$ bit of 0 and an MSB of the mode code field of 0 will be considered a defined (reserved) mode Command Word. In this configuration, the ACE/Mini-

ACE **will respond** to such a command and the Message Error bit **will not** become set.

ALTERNATE RT STATUS WORD ENABLED: For RT mode. If this bit is programmed to logic "0," only the Dynamic Bus Control Acceptance, Busy, Service Request, Subsystem Flag, and Terminal Flag RT Status Word bits are under control of the host processor, via bits 11 through 7 of Configuration Register #1. If this bit is programmed to logic "1," **all 11** RT Status Word bits are under control of the host processor, via bits 11 through 1 of Configuration Register #1.

ILLEGAL RECEIVE TRANSFER DISABLE: If this bit is programmed to logic "0" (default) and the ACE/Mini-ACE receives a receive command that has been illegalized, the ACE **WILL** store the received Data Words to the shared RAM. If this bit is programmed to logic "1" and the ACE receives a receive command that has been illegalized, the ACE/Mini-ACE **WILL NOT** store the received Data Words to the shared RAM.

BUSY RECEIVE TRANSFER DISABLE: If this bit is programmed to logic "0" (default), **and** the host processor has programmed $\overline{\text{BUSY}}$ (bit 10 of Configuration Register #1 is logic "0") **or** the particular Command Word (broadcast, $\text{T}/\overline{\text{R}}$ bit, subaddress) has been programmed to be busy by means of the Busy lookup table **and** the ACE/Mini-ACE RT receives a receive command, the ACE/Mini-ACE will respond with its Status Word with the BUSY bit set and **WILL** store the received Data Words to the shared RAM.

If this bit is programmed to logic "1," the host processor has programmed $\overline{\text{BUSY}}$ to logic "0" **or** the particular Command Word (broadcast, $\text{T}/\overline{\text{R}}$ bit, subaddress) has been programmed to be busy by means of the Busy lookup table **and** the AC/Mini-ACE receives a receive command, the ACE/Mini-ACE will respond with its Status Word with the BUSY bit set and **WILL NOT** store the received Data Words to the shared RAM.

RTFAIL/$\overline{\text{RTFLAG}}$ WRAP ENABLE: Affects RT mode only. If this bit is programmed to logic "0" (default), the RTFLAG Status bit is controlled entirely by the host processor, via Configuration Register #1. If this bit is programmed to logic "1," the Terminal Flag Status Word bit will also become set if either a transmitter timeout (668 µs) condition had occurred or the ACE RT had failed its loopback test for the **previous** nonbroadcast message. The loopback test is performed on all nonbroadcast messages processed by the ACE/Mini-ACE RT. The received version of all transmitted words is checked for validity (sync and data encoding, bit count, parity) and correct sync type. In addition, a 16-bit comparison is performed on the received version of the last word transmitted by the ACE/Mini-ACE RT. If **any** of these checks or comparisons do not verify, the loopback test is considered to have failed.

1553A MODE CODES ENABLED: Affects both RT and Message Monitor modes. If this bit is programmed to logic "0" (default), the ACE considers both subaddresses 0 and 31 to be mode code subaddresses. In this configuration, the ACE/Mini-ACE RT recognizes and responds to all MIL-STD-1553B mode codes, including those with or without, Data Words. In addition, if this bit is logic "0," the ACE/Mini-ACE **will** decode for the MIL-STD-1553B "Transmit Status" and "Transmit Last Command" mode codes and **will not** update its internal RT Status Word Register as a result of

these commands, with the exception of setting the Message Error bit if the command is illegalized.

If this bit is programmed to logic "1," the ACE/Mini-ACE RT or Message Monitor considers only subaddress 0 to be a mode code subaddress. Subaddress 31 is treated as a standard nonmode code subaddress. In this configuration, the ACE/Mini-ACE will consider valid and respond only to mode code commands containing **no** Data Words. In this configuration, the ACE/Mini-ACE RT will consider all mode commands followed by Data Words to be invalid and will not respond. In addition, if this bit is logic "1," the ACE/Mini-ACE will **not** decode for the MIL-STD-1553B "Transmit Status" and "Transmit Last Command" mode codes. As a result, the internal RT Status Word Register **will be updated** as a result of these commands.

ENHANCED MODE CODE HANDLING: Affects RT mode. If this bit is logic "0" (default), there is no capability to request interrupts to indicate the reception of specific mode code commands. If the bit is logic "0," mode code interrupts may be still enabled **globally** for transmit and/or receive mode codes, for subaddresses 0 and/or 31. In addition, if ENHANCED MODE CODE HANDLING is logic "0," the Data Words for individual mode codes are all mapped to the **same** address locations in the shared RAM, for transmit and receive (and broadcast-optionally separated) subaddresses 0 and 31. Two exceptions involve the Transmit Last Command and Transmit BIT Word mode codes, in which the Data Words are accessed from internal registers.

If this bit is logic "1," there is capability to request interrupts to following the reception of messages containing specific, individual mode commands. Interrupts may be enabled for selected mode codes, as a function of broadcast/own address and the $T/\overline{R}$ bit and mode code fields of received mode code messages. This is implemented by means of the mode code selective interrupt table, address locations 0108 through 010F in the shared RAM.

In addition, if ENHANCED MODE CODE HANDLING is logic "1," the Data Words for individual mode codes are mapped as a function of receive/transmit/broadcast and the lower four bits of the mode code field

(bit 4 of the mode code field is assumed to be logic "1" for a mode code command with data). If ENHANCED MODE CODE HANDLING is logic "1," address locations 0110 through 013F are dedicated to the storage of Data Words for mode code messages.

If ENHANCED MODE CODE HANDLING is logic "0," the RT lookup table pointer to the (single word) Data Word block will be stored in the third word of the RT message descriptor in the RT Command Stack for mode code messages. If ENHANCED MODE CODE HANDLING is logic "1," **the received or transmitted Data Word** associated with a mode code message, rather than the pointer, will be stored in the third location of the message descriptor in the stack. If ENHANCED MODE CODE HANDLING is logic "1," there will be **no** word stored in the third word of the RT message descriptor for mode code messages with no Data Word.

It should be noted that ENHANCED MODE CODE HANDLING has no effect on the Data Word transmitted in response to a Transmit Last Command mode code. The Data Word in response to this command, representing the previous Command Word received by the RT, is **always** accessed from an internal register in the ACE and not from a RAM location.

4.14 CONFIGURATION REGISTER #4 (Register Address 01000; READ/WRITE)

TABLE 45. CONFIGURATION REGISTER #4 (READ/WRITE 08h)

BIT	DESCRIPTION
15(MSB)	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BROADCAST MASK ENABLED/ $\overline{\text{XOR}}$
10	RETRY IF 1553A AND MESSAGE ERROR
9	RETRY IF STATUS SET
8	FIRST RETRY ALT/ $\overline{\text{SAME}}$ BUS
7	SECOND RETRY ALT/ $\overline{\text{SAME}}$ BUS
6	VALID IF MESSAGE ERROR BIT/NO DATA
5	VALID BUSY BIT/NO DATA
4	MONITOR TIME GAP OPTION
3	LATCH RT ADDRESS WITH CFG REG #5
2	TEST MODE 2
1	TEST MODE 1
0(LSB)	TEST MODE 0

Note: *The ACE/Mini-ACE must be programmed for its ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 must be logic "1") PRIOR to being able to activate any of the functions enabled by Configuration Register #4.*

EXTERNAL BIT WORD ENABLE: Affects RT only. If programmed to logic "0," the ACE/Mini-ACE RT will respond to a Transmit BIT Word mode command with the contents of the ACE/Mini-ACE's internal BIT Word Register as the Data Word. If programmed to logic "1," the ACE/Mini-ACE will access the BIT Data Word from a location in the shared RAM. In the latter instance, the BIT Word must be written to RAM by the host processor.

The location of the BIT Word RAM address is as follows: if ENHANCED MODE CODE HANDLING, bit 0 of Configuration Register #3, is programmed to logic "0," the BIT Word will be read from the location referenced by the active area Lookup Table pointer for transmit subaddress 0 or 31. In this configuration, it should be noted that the Data Word in response to a Transmit vector word mode command will be read from the **same** pair of address locations in which the external BIT Word is stored. If EXTERNAL BIT WORD ENABLE **and** ENHANCED MODE CODE HANDLING are **both** programmed to logic "1," the BIT Word will be read from the fixed shared RAM address location 0123.

INHIBIT BIT WORD TRANSMIT IF BUSY: Affects RT only. If programmed to logic "0" and either $\overline{\text{BUSY}}$ (bit 10 of Configuration Register #1) is programmed to logic "0," **or** if BUSY LOOKUP TABLE (bit 13 of Configuration Register #2) is logic "1" **and** the respective bit(s) in the Busy lookup table (bit 0 of location 0242 and/or bit 15 of location 0243) is programmed to logic "1," the ACE/Mini-ACE will respond to a Transmit BIT Word mode command with its RT Status Word with the BUSY bit set, followed by its internal or external Built-in-Test (BIT) Word. If INHIBIT BIT WORD TRANSMIT IF BUSY is programmed to logic "1" and $\overline{\text{BUSY}}$ is programmed to logic "0" or the appropriate bit in the Busy lookup table is logic "1," the ACE/Mini-ACE will respond with its RT Status Word with the BUSY bit set, but **no** Data Word (BIT Word) will be transmitted.

MODE CODE OVERRIDE BUSY: Affects RT only. If programmed to logic "0" and $\overline{\text{BUSY}}$ (bit 10 of Configuration Register #1) is programmed to logic "0" **or** if BUSY LOOKUP TABLE (bit 13 of Configuration Register #2) is logic "1" and the respective bit(s) in the Busy Lookup Table (bit 0 of location 0242 and/or bit 15 of location 0243) is programmed to logic "1," the ACE/Mini-ACE will transmit only its Status Word with its BUSY bit set. It will **not** transmit a following Data Word, in response to either a Transmit Vector Word mode command or a Reserved transmit mode command with data (transmit mode codes 10110 through 11111).

If programmed to logic "1" and $\overline{\text{BUSY}}$ is programmed to logic "0" **or** if BUSY LOOKUP TABLE (bit 13 of Configuration Register #2) is logic "1" and the respective bit(s) in the Busy Lookup Table (bit 0 of location 0242 and/or bit 15 of location 0243) is programmed to logic "1," the ACE/Mini-ACE will transmit its Status Word with its BUSY bit set, **followed by a**

single Data Word, in response to either a Transmit Vector Word mode command or a Reserved transmit mode command with data (transmit mode codes 10110 through 11111).

EXPANDED BC CONTROL WORD ENABLE: Affects BC mode only. If either ENHANCED MODE (bit 15 of Configuration Register #3) **or** EXPANDED BC CONTROL WORD ENABLE is programmed to logic "0," the ACE/Mini-ACE BC Control Word defaults to that of the previous generation hybrid, the BUS-61559. That is, only bits are 7, 6, 5, 2, 1, and 0 are active; in this configuration, the functions of the other bits cannot be activated. If both ENHANCED MODE **and** EXPANDED BC CONTROL WORD ENABLE are programmed to logic "1," then **all 15 bits** (bits 14 through 0) of the BC Control Word are enabled (may be activated).

BROADCAST MASK ENABLED/$\overline{\text{XOR}}$: Affects BC mode only. This bit effects the operation of bit 5 of the BC Control Word, MASK BROADCAST. If BROADCAST MASK ENABLED/$\overline{\text{XOR}}$ is logic 0 and the MASK BROADCAST bit of the message's BC Control Word is logic "1," the expected value of the Broadcast Command Received Status Word bit becomes "1," rather than "0." If BROADCAST MASK ENABLED/$\overline{\text{XOR}}$ is programmed to logic "1," the MASK BROADCAST bit of the BC Control Word is used as a mask bit, rather than performing an "XOR" operation with the Broadcast Received Status Word bit. In this instance, a Status Set condition arising from the Broadcast Command Received RT Status bit occurs when MASK BROADCAST is logic "0" and the Broadcast Command Received RT Status Word bit is logic "1."

RETRY IF 1553A AND MESSAGE ERROR: This bit effects the operation of BC retries. If programmed to logic "0," BC retries will result from the following conditions: no response timeout, format errors such as incorrect Status Word address, invalid word, incorrect sync type, low and high word count.

If programmed to logic "1," the BC will also retry as a result of any of the conditions listed above. In addition, a message will also be retried if the 1553A/$\overline{\text{1553B}}$ bit of the BC Control Word (bit 3) is programmed to logic "1" **and** the Message Error bit in the RT Status Word is logic "1."

RETRY IF STATUS SET: This bit affects the operation of BC retries. If programmed to logic "0," the BC will **not** retry a message as a result of one or more bits being set in an RT Status Word; the only exception being that if RETRY IF 1553A AND MESSAGE ERROR (bit 10 of this register) is logic "1," a message will be retried if the 1553A/$\overline{\text{1553B}}$ bit of the BC Control Word (bit 3) is programmed to logic "1" **and** the Message Error bit in the RT Status Word is logic "1."

If RETRY IF STATUS SET is programmed to logic "1," the BC will retry a message in which a STATUS SET condition was detected. A STATUS SET condition is defined as follows: If bit 12 of Configuration Register #4, EXPANDED BC CONTROL WORD, is programmed to logic "0," STATUS SET encompasses **all 8** of the nonreserved Status Word bits. The expected value for the 8 nonreserved Status Word bits is LOGIC "0," with one exception: If bit 11 of Configuration Register #4, BROADCAST MASK ENABLED/$\overline{\text{XOR}}$, is logic 0 and the MASK BROADCAST bit of the message's BC Control Word is LOGIC "1," the expected value of the Broadcast Command Received bit becomes 1, rather than 0. If BROADCAST MASK ENABLED/$\overline{\text{XOR}}$ is programmed to logic "1," the MASK BROADCAST bit of the BC Control Word is used as a mask bit, rather than performing an "XOR" operation with the Broadcast Received Status Word bit; in this instance, a Status Set condition arising from the Broadcast Command Received RT Status bit occurs when the MASK BROADCAST BC Control Word bit is logic "0" and the Broadcast Command Received RT Status Word bit is logic "1."

If EXPANDED BC CONTROL WORD is programmed to logic "1," a STATUS SET condition is defined such that the only bits that can result in a STATUS SET condition are those for which the corresponding bits in the message's BC Control Word have been programmed to logic "0."

FIRST RETRY, SECOND RETRY ALT/$\overline{\text{SAME}}$ BUS: These two bits effect the operation of BC retries. Bit 8 selects the bus on which the first message retry (following the failed initial message) will take place. If bit 8 is logic "0," the first retry will take place on the same bus as the original message. If bit 8 is logic "1," the first retry will take place on the alternate bus from where the message was originally transmitted.

Similarly, bit 7 selects the bus for the second retry attempt. A second retry will be attempted only if DOUBLE/$\overline{\text{SINGLE}}$ RETRY, bit 3 of Configuration Register #1, has been programmed to logic "1." The second retry only takes place after a first retry has failed. If bit 7 is logic "0," the second retry takes place on the same bus as the original message. If bit 7 is logic "1," the second retry will take place on the alternate bus from where the message was originally transmitted.

VALID IF MESSAGE ERROR BIT/NO DATA: This bit affects the BC validation criteria for RT responses. When this bit is programmed to logic "0," if an RT responds to a transmit command with the Message Error bit set in its Status Word, the response is considered valid **only** if the Status Word is followed by the requested number of Data Words. In this scenario, a response of Status Word only with Message Error bit set, followed by no Data Words is considered to be a format error.

If programmed to logic "1," an RT response to a transmit command of Status Word with the Message Error bit set followed by the requested number of Data Words is considered a valid response. In addition, in this mode, a response of Status Word with the Message Error bit set followed by **no** Data Words is also considered a valid response, rather than a format error.

VALID BUSY BIT/NO DATA: This bit affects the BC validation criteria for RT responses. When this bit is programmed to logic "0," if an RT responds to a transmit command with the BUSY bit set in its Status Word, the response is considered valid **only** if the Status Word is followed by the requested number of Data Words. In this scenario, a response of Status Word only with the BUSY bit set, followed by no Data Words is considered to be a format error.

If programmed to logic "1," an RT response to a transmit command of Status Word with the BUSY bit set followed by the requested number of Data Words is considered a valid response. In addition, in this configuration, a response of Status Word with the BUSY bit set followed by no Data Words is also considered a valid response, rather than a format error.

MONITOR TAG GAP OPTION: This bit affects the operation of the Monitor Identification Word in the Word Monitor mode. Specifically, it affects the operation of the CONTIGUOUS DATA/$\overline{\text{GAP}}$ bit, the 8-bit GAP TIME field, and the $\overline{\text{MODE_CODE}}$ bit. If programmed to logic "0" and a word is received on the alternate bus from the previous command, the CONTIGUOUS DATA/$\overline{\text{GAP}}$ bit will be logic "0" (even if the time frame of the current word **overlapped** that of the previous word) and the GAP TIME field will assume a value of 20 µs **greater** than the actual time gap (if any) between the end of the previous word on the alternate bus and the start of the current word on the current bus. The operation of the $\overline{\text{MODE_CODE}}$ bit in the tag word will remain unchanged from the previous AIM-HY and AIM-HY'ER components, i.e., a logic 1 indicates that the word is not a mode code while a logic 0 indicates that the word is a mode command.

If programmed to logic "1" and a word is received on the alternate bus from the previous command within a time frame overlapping that of the previous word, the CONTIGUOUS DATA/$\overline{\text{GAP}}$ bit will be logic "1" and the GAP TIME field will assume a value of 0. If there is a gap in time between the end of the previous word on the alternate bus and the start of the current word on the same bus, CONTIGUOUS DATA/$\overline{\text{GAP}}$ will assume a value of logic "0" and the 8-bit GAP TIME field will reflect the correct time between the previous and current words. It will **not** be offset (high) by 20 µs.

In addition, in this mode (bit programmed to logic "1"), the $\overline{\text{MODE_CODE}}$ bit in the monitor tag word will change function to signify the occurrence of a Hand Shake failure. A hand shake failure occurs in the transparent mode when an external arbitration circuit withholds the data transfer grant signal beyond the specified timeout period. When a timeout occurs, the monitored 1553 word and tag word will be lost and the ACE/Mini-ACE will assert the $\overline{\text{MODE_CODE}}$ bit in the tag word of the NEXT monitored word to indicate that a timeout occurred and a word was lost. Note that this feature is not implemented in some versions of the ACE family. However, this feature is implemented in all Mini-ACE series terminals.

LATCH RT ADDRESS WITH CONFIG REGISTER 5: This bit **is not** applicable for BU-65170, BU-61580, and BU-61585. It **is** applicable for BU-65171, BU-61581, and BU-61586. It is also applicable for the BU-65620 digital monolithic, BU-61590 universal terminal, BU-65178/79, BU-61588, and BU-61688/89, if the input signal RT_AD_LAT is connected to logic "1."

This bit affects the capability to latch the RT address from the pins RTAD4-RTAD0 and RTADP by writing to Configuration Register #5. If the signal RT_AD_LAT is logic "0," the ACE/Mini-ACE's RT Address will continuously track the inputs RTAD4-RTAD0 and RTADP. When RT_AD_LAT is connected to logic "1" (internally, for BU-65171, BU-61581, and BU-61586; externally, for BU-65620 and BU-61590, BU-65178/79, BU-61588, and BU-61688/89), the RT Address (and parity) register bits assume their power turn-on default value of "00000 0" and are updated only when the CPU writes to Configuration Register #5.

If LATCH RT ADDRESS WITH CONFIG REG 5 is logic "0," writing to Configuration Register #5 has **no effect** on the value of the internal latched RT address and parity. If RT_AD_LAT is logic "1" and LATCH RT ADDRESS WITH CONFIG REG 5 is programmed to logic "1," the RT Address is in the latched mode and the logic values presented on the inputs RTAD4-RTAD0, RTADP will be latched internally when the host processor performs a write operation to Configuration Register #5.

Note: *To implement a read/writable software programmable RT Address, it is suggested that RTAD4 be connected to D5 on the CPU data bus, RTAD3 to D4.....RTAD0 to D1, and RTADP to D0.*

For the BU-65620, BU-61590, BU-65178/79, BU-61588, and BU-61688/89, it should be noted that the signals presented on RTAD4-RTAD0 and RTADP may also be latched on the rising edge of the RT_AD_LAT input. For the BU-65171, BU-61581, and BU-61586 the only mechanism for updating the RT Address latch is through the use of the Latch RT Address with Configuration Register #5 feature.

It should also be noted that in ENHANCED mode, the current latched values of the ACE/Mini-ACE's RT Address and RT Address parity may **always** be read from bits 5 through 0 of Configuration Register #5. This is for **all versions of the ACE/Mini-ACE**, regardless of whether the RT Address is currently in its latched or transparent mode.

TEST MODE 2, 1, 0: Used for test purposes only. Must be programmed to logic "000" for normal operation. The different test modes are defined as follows:

TABLE 46. TEST MODES

TEST MODE 2	TEST MODE 1	TEST MODE 0	MODE
0	0	0	Normal Operation
0	0	1	Decoder Test
0	1	0	Encoder Test
0	1	1	Protocol Test
1	0	0	Failsafe Timer Test
1	0	1	Register Test
1	1	0	RESERVED
1	1	1	Test Mode

4.15 CONFIGURATION REGISTER #5 (Register Address 01001; READ/WRITE)

TABLE 47. CONFIGURATION REGISTER #5 (READ/WRITE 09h) [1]

BIT	DESCRIPTION
15(MSB)	12 MHZ CLOCK SELECT (10 MHZ CLOCK SELECT for BU-61689)
14	SINGLE-ENDED SELECT
13	EXTERNAL TX INHIBIT A
12	EXTERNAL TX INHIBIT B
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	RT ADDR LATCH/ $\overline{\text{TRANSPARENT}}$
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0(LSB)	RT ADDRESS PARITY

Note: 1. The ACE/Mini-ACE must be programmed for its ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 must be logic "1") PRIOR to being able to activate any of the functions enabled by Configuration Register #5.

12 MHz CLOCK SELECT (10 MHz CLOCK SELECT for the BU-61689) (Read/Write): For all versions of the ACE, the frequency of the clock input signal, CLOCK_IN, can be software programmable. For BU-65170, BU-61580, BU-61585, and BU-61590, the signal $\overline{\text{CLK_SEL}}$ is connected internally to logic "0," allowing the clock frequency to be software programmable. For the BU-65620 digital monolithic, $\overline{\text{CLK_SEL}}$ is an input signal. If $\overline{\text{CLK_SEL}}$ is connected to logic "1," the BU-65620 clock frequency **must** be 16 MHz (**not** software programmable). If $\overline{\text{CLK_SEL}}$ is connected to logic "0," the clock frequency is software programmable, as described below.

The default for 12 MHZ CLOCK SELECT (10 MHz CLOCK SELECT for the BU-61689) is logic "0," enabling 16 MHz operation. If the programmable clock select option is enabled ($\overline{\text{CLK_SEL}}$ is connected either internally or externally to logic "0") **and** 12 MHZ CLOCK SELECT (10 MHz CLOCK SELECT for the BU-61689) is programmed to logic "1," the frequency of the ACE CLOCK input will be 12 MHz.

For BU-65620, if $\overline{\text{CLK_SEL}}$ is connected to logic "1", 12 MHZ CLOCK SELECT (10 MHz CLOCK SELECT for the BU-61689) will **always** return logic "0" when read. For BU-65170, BU-61580, BU-61585, and BU-

61590, or for BU-65620 with $\overline{\text{CLK_SEL}}$ connected to logic "0,"12 MHZ CLOCK SELECT (10 MHz CLOCK SELECT for the BU-61689) will return the most recent value written when read.

For the Mini-ACE series terminals, the clock frequency capability has been expanded to add 10 MHz or 20 MHz operation depending on the specific model purchased. For all versions of the Mini-ACE, the frequency of the clock input signal, CLOCK_IN, is user selectable. The BU-65178(16/12MHz), BU-61588(16/12 MHz), BU-61688(16/12 MHz), and BU-61689(20/10 MHz) are software selectable, while the BU-65179(20/16/12/10 MHz) is pin selectable. For BU-65178, BU-61588, and BU-61688/89, the signal $\overline{\text{CLK_SEL_1}}$ is connecting internally to either logic "0" or logic “1" to allow software selection of either 20/10 MHz or 16/12 MHz, respectively (internal signal $\overline{\text{CLK_SEL_0}}$ has no function on these terminals).

For the BU-65179 (RT-only), $\overline{\text{CLK_SEL_1}}$/$\overline{\text{CLK_SEL_0}}$ are connected to address bits A15/A14 to enable pin selection of clock frequencies 20/16/12/10 MHz. Additionally, the BU-65179 connects internal signal RT_BOOT_L OPTIONAL MODE to address bit A12. The RT_BOOT_L OPTIONAL MODE signal (A12) allows the user to configure the BU-65179 to boot up as a RT with the BUSY bit set for MIL-STD-1760 applications.

When the RT_BOOT_L OPTIONAL MODE input signal (A12) is set to logic “0", the user may select from 20/16/12/10 MHz operation using CLK_SEL_1/CLK_SEL_0 (A15/A14) as specified in the table below.

When the RT_BOOT_L OPTIONAL MODE input signal (A13) is set to logic “1", the user must configure the BU-65179 as a RT using the Mini-ACE configuration registers (Refer to the RT Operation section of this manual for RT configuration information). In this case, the user must select between 20/10 MHz (CLK_SEL_1 = “0") or 16/12 MHz operation (CLK_SEL_1 = “1") using the CLK_SEL_1 (A15) input signal as stated in the table below. To select between 20MHz or 10MHz operation (CLK_SEL_1 = “0") and between 16MHz or 12MHz operation (CLK_SEL_1 = “1"), the user must write to the 12 MHZ CLOCK SELECT (10 MHZ CLOCK SELECT for the BU-61689), Bit 15 of Configuration #5, as stated in the table below.

TABLE 48. CLOCK FREQUENCY SELECTION							
Terminal P/N		RT_BOOT_L A12 (NOTE 1,3)	CLK_SEL 1 A15 (NOTE 1)	CLK_SEL 0 A14 (NOTE 1)	Configuration Register # 5 (Bit 15) (NOTE 2)		Frequency
					Write	Read	
BU-65179		0	0	0	X	1	10 MHz
		0	0	1	X	0	20 MHz
		0	1	0	X	1	12 MHz
		0	1	1	X	0	16 MHz
	BU-61689	1	0	X	0	0	20 MHz
		1	0	X	1	1	10 MHz
	BU-65178 BU-61588 BU-61688	1	1	X	0	0	16 MHz
		1	1	X	1	1	12 MHz

X = not utilized
NOTE 1: Refers to address bit. A13 is not utilized for configuration.
NOTE 2: ACE/Mini-ACE must be configured for ENHANCED MODE to use this bit.
NOTE 3: When RT_BOOT_L is connected to logic “1", terminal will boot up in ”idle” mode and user must configure to RT mode. When RT_BOOT_L is connected to logic “0", terminal boots up as RT with BUSY bit set (MIL-STD-1760 applications).

SINGLE-ENDED SELECT : Read only bit for the ACE/Mini-ACE Series of components (65170/78/79, 61580, 61585/88, 65620, 61688/89, etc.). Read/Write bit for SP'ACE and SP’ACE II Series of components (61582 {63825}, 61583 {63925}, 65621).

For the ACE/Mini-ACE series, this bit reflects the status of the $\overline{\text{SNGL_END}}$ input. For BU-65170/78/79, BU-61580, BU-61585/88, BU-61590, BU-61688/89, the signal $\overline{\text{SNGL_END}}$ is connected internally to logic "1." This enables the internal Manchester II decoders to accept a double-ended input from a MIL-STD-1553 (electrical) receiver. For BU-65170/78/79, BU-61580, BU-61585/88, BU-61590, and BU-61688/89, SINGLE-ENDED SELECT will **always** return a value of logic "0" when read. For the BU-65620 digital monolithic, $\overline{\text{SNGL_END}}$ is an input signal.

For BU-65620, if $\overline{\text{SNGL_END}}$ input is connected to logic "0," this register bit will return a logic "1" when read and the BU-65620 Manchester decoder inputs will be configured to accept single-ended input signals (e.g., MIL-STD-1773 fiber optic receiver outputs). If the BU-65620 $\overline{\text{SNGL_END}}$ input is connected to logic "1," this register bit will return a logic "0" and the BU-65620 decoder inputs will be configured to accept

standard double-ended Manchester bi-phase input signals (i.e., MIL-STD-1553 receiver outputs).

For the SP'ACE and SP'ACE II series, this Read/Write bit is used to select between single and double ended receiver mode. Writing a Logic "0" to this bit selects the default double-ended mode. Writing a Logic "1" to this bit enables the single ended receiver mode.

EXTERNAL TX_A INHIBIT (Read Only): EXT_TXINH_A is an input signal for the BU-6517XX**6** and BU-6158XX**6**, BU-65178/79X**3**, BU-61588X**3**, BU-61688/89X**3**, the BU-61590, and the BU-65620. It is not pinned out on other versions of the BU-65170, BU-61580, and BU-61585. On these versions, EXT_TXINH_A is internally connected to logic "0." If logic "0," indicates that the input EXT_TXINH_A is connected to logic "0" and, therefore, the channel A transceiver is enabled and not externally inhibited. If logic "1," indicates that EXT_TXINH_A is connected to logic "1." In this instance, the Channel A transmitter is being externally inhibited. There will be no output from the ACE/Mini-ACE on Bus A if the Channel A transmitter is inhibited. In addition, the ACE/Mini-ACE will **fail** its BC off-line self-test if the TX_INH input for the respective channel is connected to logic "1."

EXTERNAL TX_B INHIBIT (Read Only): EXT_TXINH_A is an input signal for the BU-6517XX**6** and BU-6158XX**6**, BU-65178/79X**3**, BU-61588X**3**, BU-61688/89X**3**, the BU-61590, and the BU-65620. It is not pinned out on other versions of the BU-65170, BU-61580, and BU-61585. On these versions, EXT_TXINH_B is internally connected to logic "0." A logic "0" indicates that the input EXT_TXINH_B is connected to logic "0" and, therefore, the channel B transceiver is enabled and not externally inhibited; logic "1," indicates that EXT_TXINH_B is connected to logic "1." In this instance, the Channel B transmitter is being externally inhibited. There will be no output from the ACE/Mini-ACE on Bus B if the Channel B transmitter is inhibited. In addition, the ACE/Mini-ACE will **fail** its BC off-line self-test if the TX_INH input for the respective channel is connected to logic "1."

EXPANDED ZERO-CROSSING ENABLED (Read/Write): This bit selects the sampling frequency of the ACE Manchester II decoders. If programmed to logic "0," the decoders sample using a **single** edge of the CLOCK input. That is, the decoder sampling frequency is either 16 MHz or 12 MHz. If programmed to logic "1," the decoders sample using **both** edges of the clock input. In this case, the decoder sampling frequency doubles to either 24 MHz or 32 MHZ. The higher sampling frequency provides improved tolerance (about 30 to 40 ns) to input zero crossing distortion. It should be noted, however, that if the expanded zero-crossing option is used, a tighter tolerance is required for the ACE's CLOCK input. The required duty cycle range for the CLOCK input is approximately 33% to 67% if the expanded zero-crossing option is not

used, and approximately 40% to 60% if expanded zero-crossing is used. **Note: For Mini-ACE series terminals, expanded zero crossing is always internally enabled allowing decoder sampling of 40MHz (20MHz clock), 32MHz (16MHz clock), 24MHz (12MHz clock), and 20MHz (10MHz clock). It is strongly recommended that Expanded Crossing be enabled for both 12 and 16 MHz operation for ACE terminals.**

RESPONSE TIMEOUT SELECT 1, 0 (Read/Write): These two bits are used to select the value of the ACE/Mini-ACE's response timeout timer. This timer is used in BC mode, for RT mode (for messages in which the ACE/Mini-ACE is the receiving RT in an RT-to-RT transfer), and in the Message Monitor mode. The four programmable choices (approximate timeout values) are shown in TABLE 49.

TABLE 49. RESPONSE TIMEOUT SELECT

BIT 10 RESPONSE TIMEOUT SELECT 1	BIT 9 RESPONSE TIMEOUT SELECT 0	RESPONSE TIMEOUT TIME VALUE (s)
0	0	18.5 [1]
0	1	22.5
1	0	50.5
1	1	130

Note: 1. Default value for non-ENHANCED mode is 18.5 µs

GAP CHECK ENABLED (Read/Write): For MIL-STD-1553B applications it is strongly recommended that this bit be programmed for a value of Logic “0”. If programmed to logic "0," the ACE/Mini-ACE does **not** check for a minimum of dead bus time prior the start of transmission by another terminal on the 1553 bus. If programmed to logic "1," the ACE/Mini-ACE **does** verify for a minimum of 2 µs of dead bus time prior to the transmission by an external BC or RT on the 1553 bus. If this minimum gap time is violated, the ACE/Mini-ACE will determine that the BC Command Word or the RT Response (Status Word) is invalid, representing a message format error.

BROADCAST DISABLED (Read/Write): Applicable to RT and Monitor modes. If the BROADCAST DISABLED bit is programmed to logic "0," the ACE/Mini-ACE will recognize RT Address 31 as the broadcast address. In this configuration, RT Address 31 **cannot** be used as the ACE/Mini-ACE's discrete RT Address. If BROADCAST DISABLED is programmed to logic "1," the ACE/Mini-ACE will **not** recognize RT Address 31 as the broadcast address. In this instance, RT Address 31 may be used as a discrete RT address.

It should be noted that for the BU-65620 digital monolithic, the value of BROADCAST DISABLED is affected by the input signal BRO_ENA. If BRO_ENA is connected to logic "0," broadcast is **disabled**. In this case, BROADCAST DISABLED will **always** return logic "1" when read. If BRO_ENA is connected to logic "1," enabling broadcast for the BU-65620 is software programmable, as described in the preceding paragraph. For BU-65170/78/79, BU-61580, BU-61585/88, BU-61590, and BU-61688/89, the use of broadcast is **always** software programmable, as described above.

In Word Monitor mode, bit 5 of the Monitor Identification Word, $\overline{\text{BROADCAST}}$, will **ALWAYS return logic "1"** (even for a Command Word to RT Address 31) if BROADCAST DISABLED has been programmed to logic "1."

RT ADDRESS LATCH/$\overline{\text{TRANSPARENT}}$ (Read only): This bit reflects the logic sense of the signal RT_AD_LAT. RT_AD_LAT is internally hardwired to logic "0" for BU-65170, BU-61580, and BU-61585. It is internally hardwired to logic "1" for BU-65171, BU-61581, and BU-61586. RT_AD_LAT is brought out to an external pin for BU-65620, BU-61590, BU-65178/79, BU-61588, and BU-61688/89. If this bit is logic "0," this indicates that the ACE/Mini-ACE's RT Address will continuously track the inputs RTAD4-RTAD0 and RTADP. When a logic "1" level is applied to the RT_AD_LAT input, the ACE/Mini-ACE RT Address inputs may be optionally latched under software control.

If LATCH RT ADDRESS WITH CONFIG REG 5 (bit 3 of Configuration Register #4) is set to logic "0", writing to Configuration Register #5 has **no effect** on the value of the ACE/Mini-ACE's RT address and parity. If RT_AD_LAT is logic "1" **and** LATCH RT ADDRESS WITH CONFIG REG 5 is logic "1", the logic values presented on the inputs RTAD4-RTAD0 and RTADP will be latched internally when the host processor performs a write operation to Configuration Register #5. It should be noted that in ENHANCED mode, the current value of the ACE/Mini-ACE's RT Address (including parity) may **always** be read from bits 5 through 0 of Configuration Register #5, for all versions of the ACE/Mini-ACE.

RT ADDRESS 4-0 and RTADP (Read Only; Optional Write via RTAD4-RTAD0 and RTADP inputs): These six bits return the values of the five RT Address bits and the RT Address parity that are latched internally within the ACE/Mini-ACE. If the parity sum of RTAD4-0 and RTADP is not odd, the ACE/Mini-ACE will not recognize, and not respond to, a Command Word directed to the ACE/Mini-ACE's discrete RT address. It will, however, receive messages to the broadcast address (address 31), unless broadcast has been disabled.

If the signal RT_AD_LAT is logic "0," the ACE/Mini-ACE's internal RT Address and RT Address Parity will continuously track the inputs

RTAD4-RTAD0 and RTADP. RT_AD_LAT is internally hardwired to logic "0" for BU-65170, BU-61580, and BU-61585. It is hardwired to logic "1" for BU-65171, BU-61581, and BU-61586. RT_AD_LAT is brought out to an external pin for BU-65620, BU-61590, BU-65178/79, BU-61588, and BU-61688/89.

For BU-65620, BU-61590, BU-65178/79, BU-61588, and BU-61688/89, the inputs presented on RTAD4-RTAD0 and RTADP become latched internally when RT_AD_LAT transitions from logic "0" to logic "1."

If LATCH RT ADDRESS WITH CONFIG REG 5 is logic "0", writing to Configuration Register #5 will have **no effect** on the value of the internal latched RT Address and address parity. If RT_AD_LAT is logic "1" and LATCH RT ADDRESS WITH CONFIG REG 5 is programmed to logic "1," the logic values presented on the inputs RTAD4-RTAD0 and RTADP will be latched internally when the host processor performs a write operation to Configuration Register #5. During such an operation, the RT Address and parity are sampled from the RTAD4-0 and RTADP inputs and **not** from the data bus, D15 through D0.

To implement a read/writable software programmable RT Address, it is suggested that RTAD4 be connected to D5, RTAD3 to D4.....RTAD0 to D1, and RTADP to D0.

RT/MONITOR DATA STACK ADDRESS (Register Address 01010; READ/WRITE)

TABLE 50. RT/MONITOR DATA STACK ADDRESS REGISTER (READ/WRITE 0Ah)

BIT	DESCRIPTION
15(MSB)	RT/MONITOR DATA STACK ADDRESS 15
•	•
•	•
•	•
0(LSB)	RT/MONITOR DATA STACK ADDRESS 0

In RT mode, the pointer word read from the lookup table during the Start-of-Message (SOM) sequence is initially loaded into the Data Stack Address Register. The value of the register is then incremented by one (modulo the Data Stack size) after each successive Data Word accessed to/from the respective Data Word table.

In the Word Monitor mode, the Monitor Data Stack Address contains the current value of the Data Stack Pointer. In the Selective Message Monitor or combined RT/Monitor modes, this register contains the current value of the Monitor Data Stack Pointer.

4.16 BC FRAME TIME REMAINING (Register Address 01011; READ ONLY)

TABLE 51. BC FRAME TIME REMAINING REGISTER (READ ONLY 0Bh)	
BIT	**DESCRIPTION**
15(MSB)	BC FRAME TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC FRAME TIME REMAINING 0

The BC frame time is programmable in increments of 100 µs, up to 6.55 ms.

(**Note:** For some older models of ACE, this register may return all zeros, “00".)

4.17 BC MESSAGE TIME REMAINING (Register Address 01100; READ ONLY)

TABLE 52. BC MESSAGE TIME REMAINING REGISTER (READ ONLY 0Ch)	
BIT	**DESCRIPTION**
15(MSB)	BC MESSAGE TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC MESSAGE TIME REMAINING 0

The BC Message Time Remaining has a resolution of 1 µs/LSB. The maximum range on this timer is 65.535 ms.

4.18 BC FRAME TIME/RT LAST COMMAND/MT TRIGGER REGISTER (Register Address 01101; READ/WRITE)

TABLE 53. BC FRAME TIME/RT LAST COMMAND/MT TRIGGER REGISTER (READ/WRITE 0Dh)	
BIT	**DESCRIPTION**
15(MSB)	BIT 15
•	•
•	•
•	•
0(LSB)	BIT 0

In BC mode, the BC frame time, used in the BC AUTO-REPEAT mode, is programmable by means of this register. The value of the BC FRAME TIME is programmable in increments of 100 µs/LSB, up to a maximum of 6.55 seconds.

In RT mode, this register stores the Command Word for the current or last message processed by the ACE/Mini-ACE RT. This register is updated at the **beginning** of each message processed by the ACE/Mini-ACE RT.

In the Word Monitor mode, this register stores the contents of the Monitor Trigger Word. This word must be supplied by the host processor. When the ACE/Mini-ACE Word Monitor is on-line, it compares the contents of this register to all valid, received Command Words. The Monitor Trigger mechanism may be used to start the Word Monitor, stop the Word Monitor, or generate interrupt requests. The trigger feature is **NOT** applicable for the Message Monitor and RT/Message Monitor modes.

4.19 RT STATUS WORD REGISTER (Register Address 01110; READ ONLY)

TABLE 54. RT STATUS WORD REGISTER (Shown for MIL-STD-1553B) (READ 0Eh)	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPT
0(LSB)	TERMINAL FLAG

4.20 RT BIT WORD REGISTER (Register Address 01111; READ ONLY)

TABLE 55. RT BIT WORD REGISTER **(READ 0Fh)**	
BIT	**DESCRIPTION**
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	CHANNEL B / $\overline{A}$
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

4.21 BLOCK STATUS WORD

The Block Status Word is stored in the first location of the Message Block descriptor in the Command Stack for BC, RT, Selective Monitor, and RT/Selective Monitor modes. There are two Command Stacks maintained for the RT/Selective Monitor mode: one for the RT, one for the Monitor. There is **no** Command Stack in the Word Monitor mode. For all modes except Word Monitor, the Block Status Word is updated by the ACE/Mini-ACE's 1553 memory management logic both at the beginning and at the end of the respective message. It contains information relating to whether the message is in progress or has been completed, what channel it was processed on, and whether or not there were any errors in the message table .

TABLE 56. BC MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

Note: If a message is retried in BC mode, the bits of the Block Status Word reflect the result of the latest message retry.

TABLE 57. RT MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B / $\overline{A}$
12	ERROR FLAG
11	RT-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 58. MESSAGE MONITOR MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B / $\overline{A}$
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

5 BC OPERATION

The BC protocol of the ACE/Mini-ACE implements all MIL-STD-1553B message formats. Message format is programmable on a message by message basis by means of individual BC Control Words and the T/$\overline{R}$ bit of the Command Word to be transmitted. In addition to message format, the BC Control Word allows bus channel, self-test, retries, interrupts, and Status Word masking to be specified on an individual message basis. The BC performs all error checking required by MIL-STD-1553B. This includes validation of sync type and encoding, Manchester II encoding, parity, bit count, word count, and Status Word RT Address field. RT response time is verified to be less than the ACE/Mini-ACE's programmable response timeout value (17.5 to 19.5 µs default).

5.1 BC MEMORY ORGANIZATION

TABLE 59 illustrates a typical memory map for the Mini-ACE/ACE Bus Controller. Note that there are eight (8) fixed memory locations within the BC memory map. For each of the two global "areas" (A and B), these are the Stack Pointer and Message Counter, and the Initial Stack Pointer and Message Counter. The Stack Pointer and Message Counter must be initialized by the host processor before starting single message frames. For the frame auto-repeat mode, the Initial Stack Pointer and Initial Message Count locations must be initialized by the CPU before initializing a repetitive frame of BC messages.

TABLE 59. TYPICAL NON-ENHANCED BC MEMORY MAP (shown for 4K RAM, ENHANCED mode)

ADDRESS(HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101	Message Count A (fixed location)
0102	Initial Stack Pointer A (Auto-Frame Repeat Mode)[1]
0103	Initial Message Count A (Auto-Frame Repeat Mode)[1]
0104	Stack Pointer B (fixed location)
0105	Message Count B (fixed location)
0106	Initial Stack Pointer B (Auto-Frame Repeat Mode)[1]
0107	Initial Message Count B (Auto-Frame Repeat Mode)[1]
0108-012D	Message Block 0
012E-0153	Message Block 1
• • •	• • •
0ED6-0EFB	Message Block 93
0EFC-0EFF	Not Used
0F00-0FFF	Stack B

Note: 1. Used only in the ENHANCED BC mode with Frame Auto-Repeat enabled. The user is free to locate the BC stack and BC message blocks anywhere within the ACE's 64K word (4K or 12K internal) address space.

5.1.1 256-Word Boundaries

It should be noted that the BC (as well as RT) stack area of RAM will roll over at the boundary in the ACE/Mini-ACE shared RAM address space as specified by bits 14 and 13 of Configuration Register #3 (default is 256 words). The BC/RT Stack size is programmable with choices of 256 words (64 messages), 512, 1024, and 2048 words (512 messages). The default is 256 words (64 messages). That is, the value of the Stack Pointer will increment from XXFF to XX00, not to (XX+1)00. If bit 10 of Configuration Register #2, 256-WORD BOUNDARY DISABLE, is logic 0, the 256-word boundaries will also be enforced for BC message blocks.

However, if 256-WORD BOUNDARY DISABLE is programmed to logic "1," the address for BC message blocks **will not** roll over at 256-word boundaries. This allows for more efficient allocation of the shared RAM address space for storing BC message blocks.



Note *For BC mode, it is strongly recommended that 256-WORD BOUNDARY DISABLE be programmed to logic "1."*

For simplicity of illustration, the maximum message size is allocated for each BC message block in the typical BC memory map of TABLE 59. Note, that the maximum size of a BC message block is 38 words, for an RT-to-RT transfer of 32 Data Words (Control + 2 Commands + Loopback + 2 Status Words + 32 Data Words). This requires that 256-word boundaries are disabled.

5.1.2 Active Areas Double Buffering

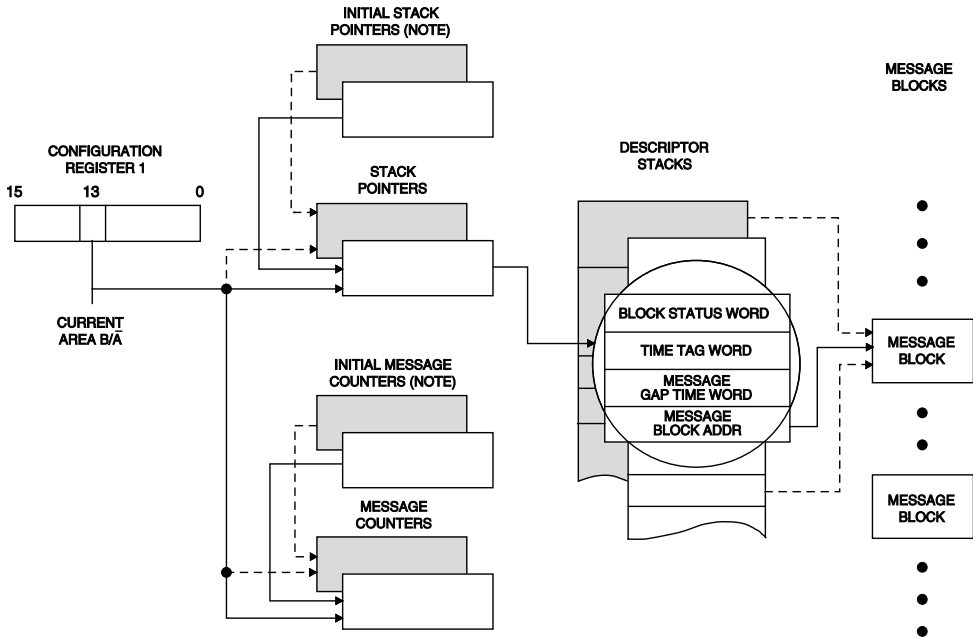
The Active Area facility provides a global mechanism for dividing the shared RAM into "active" and "nonactive" areas. At any point in time, only the various data structures within the "active" area are accessed by the internal 1553 memory management logic. It should be noted, however, that at any point in time, **both the "active" and "nonactive" areas are accessible by the host processor.**

It should be noted that if the host CPU changes the active area while a BC frame is being processed (by toggling bit 13 of Configuration Register #1), the active area **will NOT actually switch until the current BC frame has been completed.**

5.2 PROGRAMMING OF BC MESSAGE FRAMES

5.2.1 BC Memory Management

An overview of the AC/Mini-ACE memory management scheme for BC mode is illustrated in FIGURE 2. The BC may be programmed to transmit multimessage frames of up to 512 unique messages. The number of messages to be processed is programmable by means of the fixed Message Count location in the shared RAM. In addition, the host processor must initialize a second fixed location as the Stack Pointer. This RAM location contains a pointer that references the four-word message block descriptor (in the Stack area of shared RAM) for each message to be processed. Each message resides in a designated message block area of the shared RAM. The starting location for each message block is specified by a pointer that is stored in the fourth location of the block descriptor for the respective message. This pointer must be loaded by the host processor before the message is processed. The first word of each BC message block is the BC Control Word.



NOTE:
Initial stack pointers and initial message counters used only in BC frame auto-repeat mode.

FIGURE 2. BC MEMORY MANAGEMENT

Referring to FIGURE 2, the CPU may select between global Area A and global Area B by means of bit 13 of Configuration Register #1. In the

figure, it is assumed that Area A is delineated by the nonshaded area and is the current "active" area; it can be assumed that Area B is the "nonactive" (shaded) area.

The ACE/Mini-ACE's global double buffering feature provides a relatively simple-minded mechanism for ensuring data consistency. The host processor designates the current active area by means of bit 13 of Configuration Register #1 (ACTIVE AREA B/$\overline{A}$). A common practice is for the host CPU to access the "nonactive" area, while allowing the ACE/Mini-ACE's 1553 protocol logic to access the "active" area. After the current message frame has been completed for the current "active" area, the host should switch ("ping-pong") the "active" and "nonactive" areas by means of ACTIVE AREA B/$\overline{A}$.

The use of the ACE/Mini-ACE's global double buffering feature eliminates the possibility of data inconsistency by precluding the possibility that the BC will transmit or that the CPU will read a mixture of old and new Data Words for any particular message. In addition, this technique eliminates the possibility of a contended CPU access to the ACE/Mini-ACE's shared RAM.

A variation on the global buffering scheme is the use of "multiple buffering." That is, instead of using the ACE/Mini-ACE's ACTIVE AREA B/$\overline{A}$ feature, it is possible to program **several** message frame scenarios. This is done by positioning a number of descriptor stacks at different areas within the ACE/Mini-ACE shared RAM address space. In turn, the pointer words for the individual message block descriptors in the stacks can reference message blocks anywhere within the address space. When one message frame has been completed, the host processor need only re-assign the values of the Stack Pointer and Message Counter to initiate processing of the next BC message frame.

To process a single message frame, the "active area" stack pointer and message count locations must be initialized by the host CPU before processing each individual message frame. For the frame auto-repeat mode, the values for the initial stack pointer and initial message counter locations must be initialized. The initial pointer and counter need be initialized only **once**, prior to the processing of the first message frame.

At any point in time, the stack pointer points to the first word of the block descriptor for the current message. As illustrated in FIGURE 2, there are four words in the descriptor stack for each BC message. The first two locations are reserved for the Block Status Word and Time Tag Word. These two words are written by the ACE/Mini-ACE's BC protocol logic at the beginning and end of each message processed. The BC Block Status Word contains bits relating to message status and completion, validity, and bus channel. The time tag word reflects the contents of the ACE's Time Tag Register at the beginning (and end) of a message. The

time tag register has a programmable resolution of 2 to 64 µs/LSB, in even powers of two. The Time Tag counter may also be clocked from an external oscillator.

The second two locations within the BC block descriptor must be loaded by the host processor. The Message Gap Time Word is accessed if the ACE is in ENHANCED MODE (bit 15 of Configuration Register #3 is programmed to logic "1") **and** MESSAGE GAP TIME ENABLED (bit 05 of Configuration Register #1) is programmed to logic "1." The Message Gap Time Word specifies the time **from the beginning of the current message to the beginning of the subsequent message**. Reference FIGURE 6. The resolution of the message Gap is 1 µs/LSB. The Message Block Address provides a pointer to the first word of the message block (the BC Control Word) for the respective message. The value of the active area Stack Pointer is incremented by four following each message processed by the ACE BC.

The message count (or initial message count) location must be initialized by the CPU to correspond to the **ones complement** of the number of messages to be processed in a message frame. For example, if a message frame contains one (1) message, the (Initial) Message Counter location should be loaded with a value of FFFE. The value of the (Initial) Message Counter is incremented by one at the end of each message processed.

As illustrated in FIGURE 3, FIGURE 4, and FIGURE 5, the BC Control Word is the first word (word number "0") within the individual BC message block. The BC Control Word is **not** transmitted on the 1553 bus. These figures illustrate the message block structures for all of the possible BC message formats. The words to be transmitted and received are in the order they appear in the BC message blocks. The BC Control Word is the principal control entity for individual BC messages. The bits in the BC Control Word contain information relating to the message format, bus channel, interrupt enabling, 1553A vs. 1553B error handling, off-line self-test, retries, and Status Word bit masking.

If ENHANCED BC MODE is enabled (the ACE is programmed for ENHANCED MODE **and** EXPANDED BC CONTROL WORD ENABLED, bit 12 of Configuration Register #4, is programmed to logic "1"), then **all 15** bits (bit 15 is "NOT USED") of the BC Control Word are used. If ENHANCED BC MODE is logic "0," then only bits 7,6,5,2,1, and 0 are used. This includes the 7 Status Mask bits.

The STATUS SET bits designate various RT Status Word bits as either "care" (if logic "0") or "don't care" (if logic "1"). If one or more of the designated "care" bits are set to logic "1" in a responding RT's Status Word, then item (1), and possibly items (2), (3), and (4) below will occur:

1) The STATUS SET bit (bit 11) of the BC Block Status Word will be logic "1."

2) If STATUS SET, bit 1 of the Interrupt Mask Register is logic "1," an interrupt request will be issued.

3) If STATUS SET, bit 1 of the Interrupt Mask Register is logic "1" **or** ENHANCED INTERRUPTS, bit 15 of Configuration Register #2 is logic "1," then STATUS SET, bit 1 of the INTERRUPT STATUS REGISTER, will be logic "1."

4) If RETRY ENABLED (bit 4 of Configuration Register #1) **and** RETRY IF STATUS SET (bit 9 of Configuration Register #4) **and** RETRY ENABLED (bit 8 of the BC Control Word) are all logic "1," the message will be retried.

The host CPU must write the (first) Command Word in the next location after the BC Control Word. After this word, a possible second Command Word (for RT-to-RT transfers), and Data Words to be transmitted by the BC need to be loaded by the host. In the subsequent addresses, locations must be reserved for the Loopback Word and received Status and Data Words.

5.2.2 Message Block Formats

In BC mode, the ACE/Mini-ACE supports all MIL-STD-1553B message formats. For each 1553B message format, the ACE/Mini-ACE requires a specific sequence of words within the BC Message Block. This includes locations for the Control, Command, and (transmitted) Data Words that are loaded by the host processor to be read from RAM by the BC protocol logic. In addition, subsequent contiguous locations must be allocated for storage of received Loopback, RT Status, and Data Words. TABLE 60 illustrates the bit mapping of the command word and TABLE 61 illustrates the bit mappings for the status word (for more information on 1553 command and status words refer to DDC's MIL-STD-1553 Designer's Guide). FIGURE 3, FIGURE 4, and FIGURE 5 illustrates the organization of the BC message blocks for the various MIL-STD-1553B message formats. Note that for all of the message formats, the BC Control Word is located in the first location of the message block.

TABLE 60. MIL-STD-1553 COMMAND WORD	
BIT	**DESCRIPTION**
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
•	•
•	•
11	REMOTE TERMINAL ADDRESS BIT 0
10	TRANSMIT RECEIVE
9	SUBADDRESS/MODE CODE BIT 4
•	•
•	•
5	SUBADDRESS/MODE CODE BIT 0
4	DATA WORD COUNT/MODE CODE BIT 4
•	•
•	•
0(LSB)	DATA WORD COUNT/MODE CODE BIT 0

TABLE 61. MIL-STD-1553B STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
14	REMOTE TERMINAL ADDRESS BIT 3
13	REMOTE TERMINAL ADDRESS BIT 2
12	REMOTE TERMINAL ADDRESS BIT 1
11	REMOTE TERMINAL ADDRESS BIT 0
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPTANCE
0(LSB)	TERMINAL FLAG

BC-to-RT Transfer

Control Word
Receive Command Word
Data Word #1
Data Word #2
• • •
Last Data Word
Last Data Word Looped Back
Received Status Word

RT-to-BC Transfer

Control Word
Transmit Command Word
Transmit Command Word Looped Back
Received Status Word
Received Data Word #1
Received Data Word #2
• • •
Last Received Data Word

FIGURE 3. BC MESSAGE BLOCK FORMATS (1 of 3)

RT-to-RT Transfer

Control Word
Receive Command
Transmit Command
Transmit Command Looped Back
Tx RT Status Word
Data #1
Data #2
• • •
Last Data
Rx RT Status Word

Mode Code; No Data

Control Word
Mode Command
Mode Command Looped Back
Status Received

Tx Mode Code With Data

Control Word
Tx Mode Command
Mode Command Looped Back
Status Received
Data Word

FIGURE 4. BC MESSAGE BLOCK FORMATS (2 of 3)

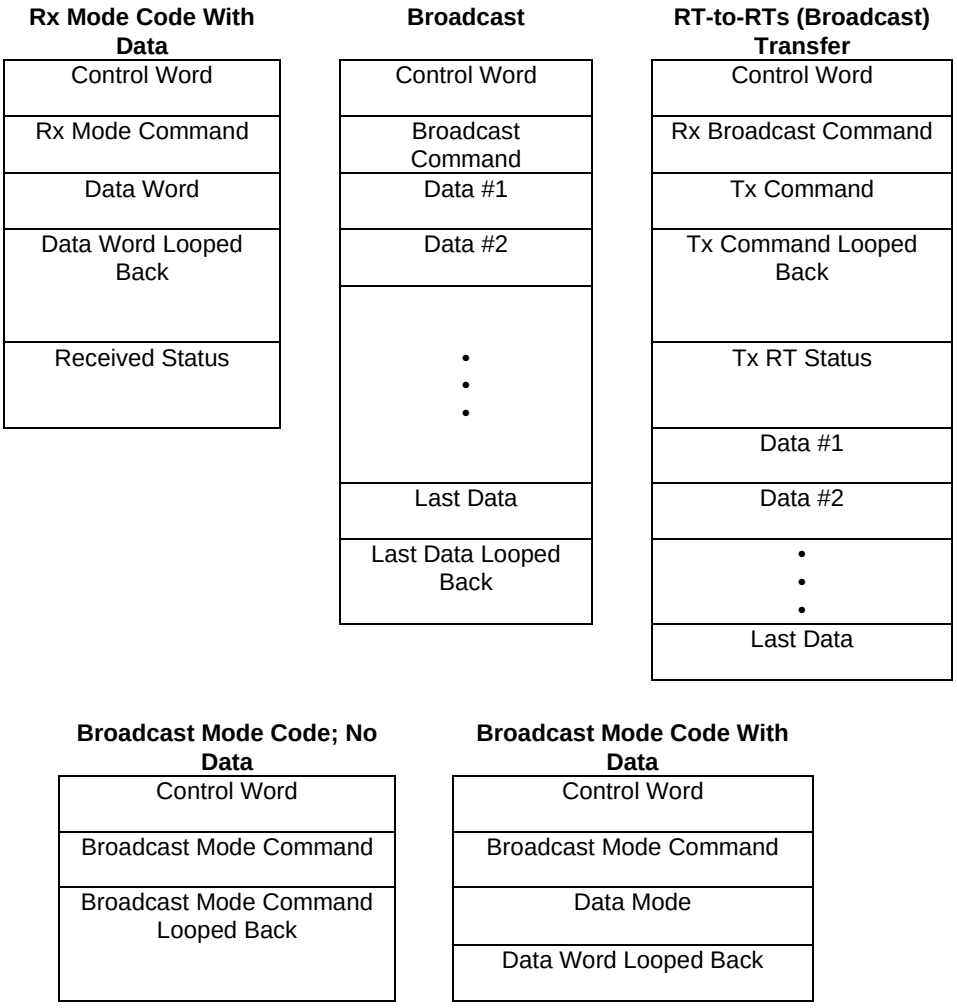


FIGURE 5. BC MESSAGE BLOCK FORMATS (3 of 3)

5.3 BC CONTROL WORD

For each of the BC Message Block formats, the first word in the block is the BC Control Word. The BC Control Word is **not** transmitted on the 1553 bus. Instead, it contains bits that select the active bus and message format, enable off-line self-test, and specify the "expected value" of the BROADCAST COMMAND RECEIVED RT Status bit. The bit mapping and definitions of the BC Control Word are as shown in TABLE 62.

TABLE 62. BC CONTROL WORD REGISTER (READ/WRITE 04h)

BIT	DESCRIPTION
15(MSB)	RESERVED
14	MESSAGE ERROR MASK (S10)
13	SERVICE REQUEST BIT MASK (S08)
12	SUBSYS BUSY BIT MASK (S03)
11	SUBSYS FLAG BIT MASK (S02)
10	TERMINAL FLAG BIT MASK (S00)
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/$\overline{B}$
6	OFF LINE SELF TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-TO-RT FORMAT

Note: Bits 14-8, 4, and 3 are applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, are logic "1." If these two conditions are **not** met, the ACE BC utilizes its nonexpanded BC Control Word. The nonexpanded BC Control Word consists of bits 7, 6, 5, 2, 1, and 0 only.

With the nonexpanded BC Control Word, a "Status Set" condition indicates either a non-matching RT Address field **or** if **ANY** of the 8 non-Reserved RT Status bits are set. An exception is that for the Broadcast Command Received bit, a "Status Set" condition will occur if the value of the Broadcast Command Received bit in the RT Status Word is **different** than the value of the MASK BROADCAST bit.

When the expanded BC Control Word option is used, a "Status Set" condition indicates a non-matching RT Address field **or** that one or more of the RT Status Word bits, **in which the respective MASK bit(s) in the BC Control Word has been programmed to logic "0,"** is set (logic "1") in the received RT Status Word. When the Expanded BC Control Word option is used, the value of received RT Status Word bits for which the

respective MASK bit is programmed for logic "1" becomes "don't care," in terms of affecting a "Status Set" condition.

MESSAGE ERROR MASK: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If MESSAGE ERROR MASK is logic "0," a Status Set condition will occur if the Message Error bit is logic "1" in the received RT Status Word. If MESSAGE ERROR MASK is logic "1," the value of the Message Error bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

SERVICE REQUEST MASK: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If SERVICE REQUEST MASK is logic "0," a Status Set condition will occur if the Service Request bit is logic "1" in the received RT Status Word. If SERVICE REQUEST MASK is logic "1," the value of the Service Request bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

BUSY MASK: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If BUSY MASK is logic "0," a Status Set condition will occur if the Busy bit is logic "1" in the received RT Status Word. If BUSY MASK is logic "1," the value of the Busy bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

SUBSYSTEM FLAG MASK: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If SUBSYSTEM FLAG MASK is logic "0," a Status Set condition will occur if the Subsystem Flag bit is logic "1" in the received RT Status Word. If SUBSYSTEM FLAG MASK is logic "1," the value of the Subsystem Flag bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

TERMINAL FLAG MASK: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If TERMINAL FLAG MASK is logic "0," a Status Set condition will occur if the Terminal Flag bit is logic "1" in the received RT Status Word. If TERMINAL FLAG MASK is logic "1," the value of the

Terminal Flag bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

RESERVED BITS MASK: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If RESERVED MASK is logic "0," a Status Set condition will occur if the one or more of the 3 Reserved bits are logic "1" in the received RT Status Word. If RESERVED BITS MASK is logic "1," the value of the 3 Reserved bits in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

RETRY ENABLED: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If RETRY ENABLED is logic "0," the message will **not** be retried. If RETRY ENABLED, bit 4 of Configuration Register #1, is logic "1" **and** RETRY ENABLED is logic "1," a message will be retried as the result of a response timeout or format error condition.

If RETRY ENABLED, bit 4 of Configuration Register #1, is logic "1" **and** RETRY IF 1553A AND MESSAGE ERROR, bit 10 of Configuration Register #4 is logic "1" **and** 1553 A/$\overline{B}$ SELECT, bit 3 of the BC Control Word, is logic "1" **and** RETRY ENABLED is logic "1," the ACE BC will attempt a message retry as the result of the Message Error bit being set in the RT Status Word.

If RETRY ENABLED, bit 4 of Configuration Register #1, is logic "1" **and** RETRY IF STATUS SET, bit 9 of Configuration Register #4 is logic "1" **and** RETRY ENABLED is logic "1," the ACE BC will attempt a message retry as the result of a "Status Set" condition in the received RT Status Word. A "Status Set" condition indicates either a nonmatching RT Address field **or** that one or more of the RT Status Word bits, **in which the respective MASK bit(s) in the BC Control Word has been programmed to logic "0,"** is set in the received RT Status Word. When the expanded BC Control Word option is used, the value of received RT Status Word bits for which the respective MASK bit is programmed for logic "1" becomes "don't care," in terms of affecting a "Status Set" condition.

The number of retry attempts is specified by DOUBLE/$\overline{\text{SINGLE}}$ RETRY, bit 3 of Configuration Register #1: one retry if DOUBLE/$\overline{\text{SINGLE}}$ RETRY is logic "0," two retries if DOUBLE/$\overline{\text{SINGLE}}$ RETRY is logic "1." The channel selection (same or alternate) for the first and second retry attempts is specified by bits 8 and 7 of Configuration Register #4.

BUS CHANNEL A/$\overline{B}$: Selects whether the message will be processed on Channel A or Channel B. If the bit is logic "1," the message will be processed on Channel A; if the bit is logic "0," the message will be processed on Channel B.

OFF-LINE SELF-TEST: If this bit is set, it enables the off-line self-test for the respective message. In an off-line self-test message, the 1553 transmitter is inhibited; there is no activity on the external 1553 bus. The off-line self-test exercises the digital protocol portion of the ACE/Mini-ACE by routing the output of the Manchester II serial encoder directly to the decoder input of the selected bus channel. After the message has been processed, the user can determine the success or failure of the off-line self-test by reading the Loopback Word and the LOOP TEST FAIL bit of the Block Status Word.

MASK BROADCAST: If BROADCAST MASK ENABLED/$\overline{XOR}$, bit 11 of Configuration Register #4, is logic "0" **and** MASK BROADCAST is logic "1," the "expected value" of the Broadcast Command Received bit becomes 1, rather than 0. That is, a value of logic "**0**" (not logic "1") for the Broadcast Command Received bit in the received RT Status Word will result in a "Status Set" condition.

If ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1" **and** BROADCAST MASK ENA/$\overline{XOR}$ (bit 11 of Configuration Register #4) is programmed to logic "1," MASK BROADCAST is used as a mask bit, rather than performing an "XOR" operation with the Broadcast Received Status Word bit. In this instance, a Status Set condition arising from the Broadcast Command Received RT Status bit occurs when MASK BROADCAST is logic "0" and the Broadcast Command Received RT Status Word bit is logic "1." If BROADCAST MASK ENABLED/$\overline{XOR}$ is logic "1" **and** MASK BROADCAST is logic "1," the value of the Broadcast Command Received bit in the received RT Status Word becomes "don't care" in affecting a "Status Set" condition.

EOM INTERRUPT ENABLE: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic "1." If RT/BC MESSAGE INTERRUPT, bit 4 of the Interrupt Mask Register is set, setting EOM INTERRUPT ENABLE to logic "1" will result in an Interrupt Request at the end of the current message.

1553 A/$\overline{B}$ SELECT: Applicable only if ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "1" **and** EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, is logic

"1." If 1553 A/$\overline{B}$ SELECT is programmed to logic "0," the ACE BC verifies the validity of the RT response in accordance with MIL-STD-1553B. That is, it anticipates that an RT will respond to mode code commands with a T/$\overline{R}$ bit of logic "1" and an MSB of the Mode Code field (bit 4) of logic "1" with a Status Word followed by a single Data Word. In addition, for an anticipated "1553B" response, assuming that RETRY IF STATUS SET, bit 9 of Configuration Register #4, is logic "0," the ACE/Mini-ACE BC will **not** attempt a message retry as the result of the Message Error bit being set in the RT Status Word.

If 1553 A/$\overline{B}$ SELECT is programmed to logic "1," the ACE/Mini-ACE BC verifies the validity of the RT response in accordance with MIL-STD-1553A. That is, it anticipates that an RT will respond to mode code commands with a T/$\overline{R}$ bit of logic "1" and an MSB of the Mode Code field (bit 4) of logic "1" with a Status Word only and no Data Word. In addition, if RETRY ENABLED, bit 4 of Configuration Register #1, is logic "1," **and** RETRY IF 1553A AND MESSAGE ERROR, bit 10 of Configuration Register #4 is logic "1," **and** RETRY ENABLED, bit 8 of the BC Control Word is logic "1," **and** 1553 A/$\overline{B}$ SELECT is logic "1," the ACE BC **will** attempt a message retry as the result of the Message Error bit being set in the RT Status Word. In addition, if 1553 A/$\overline{B}$ SELECT is programmed to logic “1", then mode commands with the T/R equaling 0 will have no data words associated with them.

MODE CODE, BROADCAST, RT-TO-RT: Selects MIL-STD-1553B message format as follows:

TABLE 63. MIL-STD-1553B MESSAGE FORMAT SELECTION

BIT 2 MODE CODE	BIT 1 BROADCAST	BIT 0 RT-TO-RT	MESSAGE FORMAT
0	0	0	BC-to-RT (if T/$\overline{R}$ bit = 0) **or** RT-to-BC (if T/$\overline{R}$ bit = 1)
0	0	1	RT-to-RT
0	1	0	Broadcast
0	1	1	RT-to-RTs (Broadcast)
1	0	0	Mode Code
1	0	1	NOT USED
1	1	0	Broadcast Mode Code
1	1	1	NOT USED

The next word in RAM after the BC Control Word is the MIL-STD-1553B Command Word (for an RT-to-RT or RT-to-Broadcast transfer, it is the first of two Command Words). This word is read by the 1553 protocol logic and transmitted on the 1553 bus. The (first) Command Word is possibly followed by a second Command Word or Data Words to be read from RAM and transmitted. The location in RAM after the **last** transmitted word is reserved for the Loopback Word. Subsequent locations in the shared RAM are reserved for Status and possibly Data Words anticipated to be received from the responding RT(s). Assuming that the RT responds before a BC response timeout occurs, these word(s) are stored in the allocated locations in the shared RAM. If the Loopback test passes, and the RT responds before the BC Response Timer times out with a "Correct" RT Status Word (correct RT address and the "expected value" for the lower 11 bits), followed by the correct number of valid Data Words, the Block Status Word will be written to indicate "End of Message, No Errors" during the BC End-of-Message (EOM) sequence. Note that for an RT-to-RT transfer, the ACE/Mini-ACE BC checks the Status Words from **both** the transmitting and receiving RTs.

5.4 DESCRIPTOR STACK

The host processor may determine the status of individual messages by reading the first four locations of the respective descriptor block. The first location within the descriptor block contains the Block Status Word. In BC mode, the Block Status Word contains information relating to whether the message is in progress or has been completed, which bus channel it was transmitted on and whether there were any errors in the message. The bit map and bit descriptions for the BC Block Status Word are indicated below.

TABLE 64. BC MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

Note: 1. In BC mode, if a message is retried, the bits of the Block Status Word reflect the result of the latest message retry.

END-OF-MESSAGE (EOM): Set at the completion of a BC message, regardless of whether or not there were any errors in the message.

START-OF-MESSAGE (SOM): Set at the start of a BC message and cleared at the end of the message.

CHANNEL B/$\overline{A}$: This bit will be low if the message was processed on Channel A or high if the message was processed on Channel B.

ERROR FLAG: If this bit is high and one or more of bits 10, 9, and/or 8 are high, this indicates one or more of the following errors occurred in the message: Format Error, Response Timeout and/or Loop Test Fail.

If this bit is logic "1," the ACE is configured for its transparent mode of processor interface, and bits 11 through 7 are all logic "0," this indicates that a Handshake Failure has occurred. A Handshake Failure occurs when the input signal $\overline{DTGRT}$ is either not asserted low or is asserted low too late after the time that the output signal $\overline{DTREQ}$ is asserted low. A Handshake Failure also occurs in transparent mode if the CPU asserts the $\overline{STRBD}$ input for longer than 4 µs with a 16 MHz clock, or 3.5 µs with a 12 MHz clock after the ACE/Mini-ACE has asserted its $\overline{READYD}$ output low. If a Handshake Failure occurs, the message should be considered invalid. The ACE/Mini-ACE will immediately terminate processing of a BC frame following occurrence of a Handshake Failure.

STATUS SET: If set, indicates that in one of the lower 11 bits the RT Status Word received from a responding RT contained an unexpected bit value. The expected value for these 11 bits is normally zero (0), with one exception: if ENHANCED MODE ENABLE (bit 15 of Configuration Register #3) is logic "0" **or** BROADCAST MASK ENABLED/$\overline{XOR}$ (bit 11 of Configuration Register #4) is logic "0" **and** the MASK BROADCAST bit of the message's BC Control Word is logic "1," the expected value of the Broadcast Command Received bit becomes 1, rather than 0. The value of STATUS SET is **not** affected by the values of the other mask bits (bits 14 through 9) of the message's BC Control Word.

FORMAT ERROR: If set, indicates that the received portion of a message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the RT's status word received from a responding RT contained an incorrect RT address field.

RESPONSE TIMEOUT: If set, indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The ACE/Mini-ACE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the midbit crossing of the parity bit to

the midsync crossing of the RT Status Word. In the non-ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "0"), the value of the BC Response Timeout is 17.5 to 19.5 µs. If ENHANCED MODE ENABLED is logic 1, the value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 µs (±1 µs) by means of bits 10 and 9 of Configuration Register #5.

LOOP TEST FAIL: A loopback test is performed on the transmitted portion of every message in BC mode. A validity check is performed on the received version of every word transmitted by the ACE/Mini-ACE BC. In addition, a bit-by-bit comparison is performed on the last word transmitted by the BC for each message. If either the received version of any transmitted word is invalid (sync, encoding, bit count, and/or parity error) and/or the received version of the last word transmitted by the ACE/Mini-ACE BC does not match the transmitted version, the LOOP TEST FAIL bit will be set.

It should be noted that in the non-ENHANCED mode (if ENHANCED MODE ENABLED, bit 15 of Configuration Register # 3, is logic "0"), bits 7 through 0 will always return logic "1."

MASKED STATUS SET: Applicable for ENHANCED Mode only if ENHANCED MODE ENABLED (bit 15 of Configuration Register #3, programmed to logic "1") **and** EXPANDED BC CONTROL WORD ENABLE (bit 12 of Configuration Register #4) is programmed to logic "1." It will be set if one or both of the following conditions occur: (1) If one (or more) of the Status Mask bits (14 through 9) in the BC Control Word is logic "0" **and** the corresponding bit(s) is (are) set (logic "1") in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0," any or all of the 3 Reserved Status bits being set will result in a MASKED STATUS SET condition; **and/or** (2) If BROADCAST MASK ENABLED/$\overline{\text{XOR}}$ (bit 11 of Configuration Register #4) is logic "1" **and** the MASK BROADCAST bit of the message's BC Control Word is logic "0" **and** the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1." Refer to TABLE 68 and TABLE 69.

RETRY COUNT 1 and RETRY COUNT 0: Applicable for ENHANCED Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, programmed to logic "1") **and** EXPANDED BC CONTROL WORD (bit 12 of Configuration Register #4) set to logic "1," **and** the RETRY ENABLED bit (bit 4 of Configuration Register #1) is set to logic "1," **and** the RETRY ENABLED bit (bit 8) of the respective BC Control Word is set to logic "1." Also affected by the RETRY, IF 1553A and MESSAGE ERROR bit (bit 10) and RETRY IF STATUS SET bit (bit 9) of Configuration Register #4 and the 1553 A/$\overline{\text{B}}$ SELECT bit (bit 3) of the BC

Control Word. The number of times that a message is retried is delineated by these two bits as shown in TABLE 65.

TABLE 65. DETERMINING THE NUMBER OF MESSAGE RETRIES

RETRY COUNT 1 (bit 6)	RETRY COUNT 0 (bit 5)	Number of Retries
0	0	0
0	1	1
1	0	N/A
1	1	2

GOOD DATA BLOCK TRANSFER: Applicable for ENHANCED Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1"). Set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is **always** logic "0" following a BC-to-RT transfer, a mode code with data, or a mode code without data. The Loop Test has **no effect** on GOOD DATA BLOCK TRANSFER. The GOOD DATA BLOCK TRANSFER may be used to determine if the transmitting portion of an RT-to-RT transfer was error free. An RT-to-RT transfer with both the ERROR FLAG and GOOD BLOCK TRANSFER bits set in Block Status Word indicates that the transmitting RT responded correctly, but their was an error detected in the receiving portion of the message.

WRONG STATUS ADDRESS/NO GAP: Applicable for ENHANCED Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1"). This bit is set if either or both of the following occur: (1) The RT address field of a responding RT does not match the RT address in the Command Word; and/or (2) If the GAP CHECK ENABLED bit (bit 8) of Configuration Register #5 is set to logic "1" **and** a responding RT responds with a response time of less than 4 µs, per MIL-STD-1553B (mid-parity bit to mid-sync); i.e., less than 2 µs dead time.

WORD COUNT ERROR: Applicable for ENHANCED Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1"). Applicable for an RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. If set, indicates that a responding RT did not transmit the correct number of Data Words. Will always be logic "0" following a BC-to-RT transfer, receive mode code message, or transmit mode code without data message.

INCORRECT SYNC TYPE: Applicable for ENHANCED Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set

to logic "1"). If set, indicates that a responding RT responded with a Data sync in a Status Word and/or a Command/Status sync in a Data Word.

INVALID WORD: Applicable for ENHANCED Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1"). Indicates an RT responded with one or more words containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

The second location of the BC Message Block Description contains the Time Tag Word. The current value of the internal Time Tag Register is written to the Time Tag Word during both the BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences.

The third location of the BC Message Block Descriptor is RESERVED in non-ENHANCED BC mode. This location contains the value of the programmed message gap time if the ACE is in ENHANCED MODE **and** MESSAGE GAP TIME ENABLED (bit #5 of Configuration Register #1) is programmed to logic "1."

The fourth location is used to store the MESSAGE BLOCK ADDRESS Word. The MESSAGE BLOCK ADDRESS must be loaded by the host processor **before** the message is processed. It is then used as a pointer by the ACE memory management logic for accessing the start of the respective Message Block.

The two other fixed locations in the shared RAM address space that must be initialized by the host processor for nonenhanced BC mode are the Stack Pointer and Message Counter locations. The Stack Pointers are located in address locations 0100 (for Area A) and 0104 (for Area B). The Stack Pointer should be initialized to point to the first word of the Message Block Descriptor (Block Status Word) for the first message to be processed. The Message Counters are located in addresses 0101 (for Area A) and 0105 (for Area B). The Active Area Message Counter must be preloaded by the host processor with the **ones complement** of the number of messages to be processed (i.e. FFFE represents a message count of 1). The Message Counter is incremented by one following each BC message processed.

Note that if the ACE/Mini-ACE BC is programmed for FRAME AUTO-REPEAT operation, the **initial** Stack Pointer and initial Message Counter locations, rather than the Stack Pointer and Message Counter locations must be initialized.

5.4.1 BC Message Gap Time

The ACE/Mini-ACE contains a programmable BC message gap time with 1 µs resolution to a maximum of 65535 µs. The BC message gap time is

defined as the time from the start of the current message to the start of the next message (refer to FIGURE 6). The message gap timer is enabled if ENHANCED MODE ENABLE bit (bit 15 in Configuration Register #3) is set to logic "1" **and** MESSAGE GAP TIMER ENABLE (bit 5 in Configuration Register #1) is programmed to logic "1."

The value of the programmed message gap time is stored in the third word location of the BC descriptor stack entry. If the message gap timer is disabled, this location in the descriptor stack is not used. Specifying a message gap time value that is less than the time of the current message will cause the next message to start **immediately** following the end of the current message. In this case, the message gap time defaults to the message time plus the minimum intermessage gap time, approximately 8 to 11 µs (measured from the end of the previous message to the beginning of the next message). This feature allows the BC to implement minor frame cycle times with no host processor intervention.

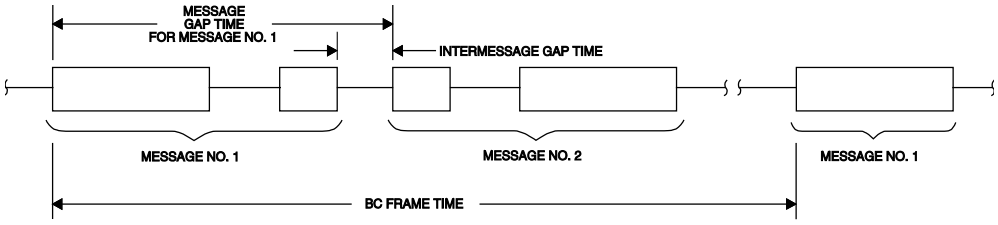


FIGURE 6. BC MESSAGE GAP TIME

5.4.2 BC Frame Auto-Repeat

The ACE/Mini-ACE has the capability to define a BC frame that can run continuously based on an internal frame timer, an external hardware trigger or under host processor control. The BC auto-repeat feature is available in ENHANCED BC Mode, that is, if the ENHANCED MODE ENABLE bit (bit 15 in Configuration Register #3) is programmed to logic "1."

Enabling the BC Frame Auto-Repeat mode requires that the BC Stack Pointer and BC Message Count values must be stored in the INITIAL BC STACK POINTER and INITIAL BC MESSAGE COUNTER fixed locations in RAM (word locations 0102 and 0103 for Area A or word locations 0106 and 0107 for Area B) rather than in the BC STACK POINTER and BC MESSAGE COUNT fixed locations in RAM (word locations 100 and 101 for area A or word locations 0104 and 0105 for Area B).

Upon receiving the BC trigger condition (software, internal, or external) the ACE/Mini-ACE will take the values in the INITIAL BC STACK POINTER and INITIAL BC MESSAGE COUNTER locations and copy them into the current (as specified by CURRENT AREA B/$\overline{A}$) BC STACK POINTER and BC MESSAGE COUNT locations, then start processing the BC frame. Two separate locations for these values are needed because the ACE will modify the STACK POINTER and MESSAGE COUNT as the current BC frame is processed.

In the Frame Auto-Repeat mode, the frame time is programmable in increments of 100 µs/LSB by means of the BC Frame Time/RT Last Command/MT Trigger Register (register address 01101). This provides a range of programmable BC Frame Times up to a maximum value of 6.5535 seconds.

5.4.3 Minor and Major Frames

In many systems, the BC is required to process messages to the various RTs/subaddresses at a variety of periodicities. For example, some messages may be required to be transmitted at a 5 Hz rate, others at a 10 Hz rate, 20 Hz rate,...100Hz, etc. A common mechanization for supporting varying data rates in a 1553 system is the use of minor and major frames, as illustrated in FIGURE 7.

In the figure, the message scenario is organized into minor frames. A major frame is comprised of multiple minor frames. If the minor frame time is assumed to be 10 ms, message rates of up to 100 Hz may be supported. That is, a 100 Hz message will appear in every minor frame, a 50 Hz message in every other minor frame, ... while a 1 Hz message will appear once every 100 minor frames.

Using the ACE/Mini-ACE BC architecture, minor frame structures may be composed by means of the message gap-time feature. The ACE/Mini-ACE message gap time field specifies the time from the start of the current message to the start of the subsequent message. By strategic use of the message gap times, it is possible to formulate minor frames. The minor frame time is the sum of all message gap times within a minor frame. All minor frame times are identical (e.g., 10 ms).

If the time required to process a message is longer than the programmed value of the message's message gap time, the message (including any retries) will be processed to completion. The resultant message gap time prior to the next message will be approximately 8 to 11 ms. If automatic retries are used, it is recommended that the message gap times allow time for a single or double retry, if possible. This will allow messages to be retried without overrunning the minor frame time.

The BC major frame is comprised of a group of minor frames. To implement a major frame, the frame auto-repeat mode should be used.

In this way, the ACE/Mini-ACE frame time becomes the system major frame time. As an alternative, it may be desirable to synchronize the start of the major frame from a timing mechanism that is external to the ACE/Mini-ACE. In this instance, INTERNAL TRIGGER ENABLE should be programmed to logic "0" and EXTERNAL TRIGGER ENABLE should be programmed to logic "1." In this configuration, the start of the major frame will be triggered by a rising edge on the EXT_TRIG input.

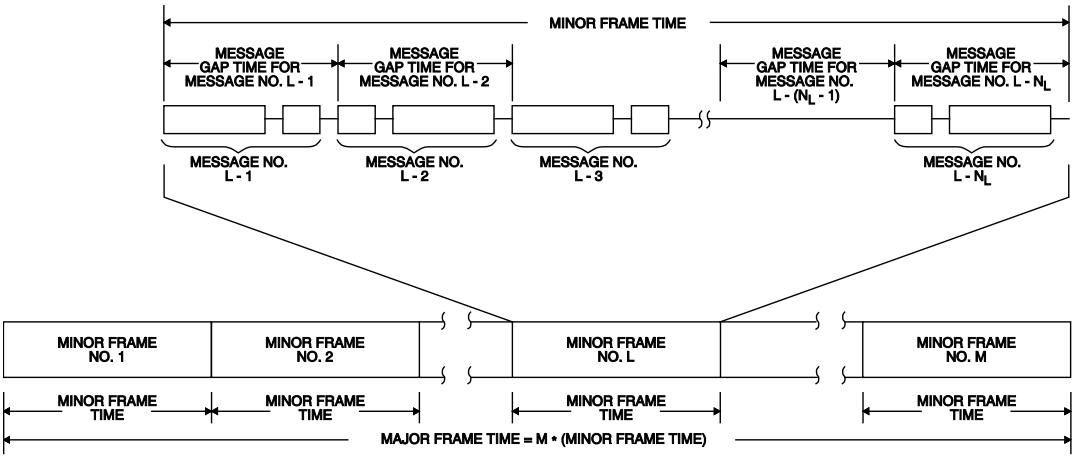


FIGURE 7. BC MAJOR AND MINOR FRAMES

5.4.4 BC Start Sequence and Options

The ACE/Mini-ACE offers several options for BC frame control. The ACE/Mini-ACE BC can be programmed to process either a single BC frame or repetitive frames. In addition, the start of the first BC frame may be initiated by either a software BC Start command or by a low-to-high ("0" to "1") transition on the EXT_TRIG input.

The BC start sequence configuration is configured by means of bits 8, 7, and 6 of Configuration Register #1. If FRAME AUTO-REPEAT (bit 8 of Configuration Register #1) is logic "0" **or** if INTERNAL TRIGGER ENABLED (bit 6 of Configuration Register #1) is logic "0," the ACE/Mini-ACE BC will process **only a single message frame.** A message frame consists of from 1 to 512 messages, in accordance with the programmed value of the Message Count or Initial Message Count location. For more information refer to TABLE 66.

If FRAME AUTO-REPEAT is logic "1" **and** INTERNAL TRIGGER ENABLED is logic "1," then the BC is programmed for automatic repetitive frame operation. The timing diagram of FIGURE 6 illustrates the definition of the ACE/Mini-ACE's BC frame time for the frame auto-repeat mode. Note that the BC frame is defined as the time from the

beginning of the first message ("message #1") for one frame to the corresponding time in the subsequent frame.

The source of the values for Stack Pointer and Message Count is programmed by means of FRAME AUTO-REPEAT. If FRAME AUTO-REPEAT is logic "0," the ACE BC protocol logic reads the active area Stack Pointer and Message Counter locations. If FRAME AUTO-REPEAT is logic "1," the BC protocol logic reads the addresses for the **Initial** Stack Pointer and **Initial** Message Counter. In the FRAME AUTO-REPEAT mode, the Stack Pointer and Message Counter locations are loaded at the beginning of every frame (from the values stored in the respective "Initial" locations) and incremented following every message processed.

For single-frame operation, or for starting the first frame for auto-repeat operation, the first message may always be initiated by means of a software BC START operation; that is, by writing 0002 (hex) to the Start/Reset Register. In addition, if EXTERNAL TRIGGER ENABLED (bit 7 of Configuration Register #1) is logic "1," the first BC frame may be initiated by means of an external signal; that is, by presenting a low-to-high transition on the ACE's EXT_TRIG input.

TABLE 66 summarizes the various BC START sequences.

TABLE 66. BC START SEQUENCES

FRAME AUTO-REPEAT (BIT 8 OF C.R. #1)	EXTERNAL TRIGGER ENABLED (BIT 7 OF C.R. #1)	INTERNAL TRIGGER ENABLED (BIT 6 OF C.R. #1)	BC START (REPEAT) SEQUENCE
0	0	X	Single frame; start by software BC Start command; Stack Pointer and Message Count must be loaded into locations 100, 101 (or 104, 105) prior to each frame.
0	1	X	Single frame; start by either software BC Start command or via EXT_TRIG input; Stack Pointer and Message Count must be loaded into locations 100, 101 (or 104, 105) prior to each frame.
1	0	0	Single frame; start by software BC Start command; Stack Pointer and Message Count must be loaded into locations 102, 103 (or 106, 107) one time.
1	0	1	Repeat frame; start first frame by software BC Start command; frame repeats in accordance with internal frame timer; Stack Pointer and Message Count must be loaded into locations 102, 103 (or 106, 107) one time.
1	1	0	Single frame; start by either software BC start or via EXT_TRIG input; Stack Pointer and Message Count must be loaded into locations 102, 103 (or 106, 107) one time.
1	1	1	Repeat frame; first frame initiated by either software BC Start command or via EXT_TRIG input; frames repeat in accordance with internal frame timer; Stack Pointer and Message Count must be loaded into locations 102, 103 (or 106, 107) one time.

5.4.5 BC Interrupts

The ACE/Mini-ACE BC offers an array of conditions that can result in interrupt requests to the host CPU. These can be selected by means of the Interrupt Mask Register. It should be noted that if ENHANCED INTERRUPTS are used, the host may determine that various events have occurred by polling the Interrupt Status Register. Using ENHANCED INTERRUPTS, the various bits in the Interrupt Status Register may become set to indicate the occurrence of conditions, regardless of the programming of the Interrupt Mask Register. The use of the eight possible BC interrupt conditions is summarized as follows:

BC_END_OF_FRAME: For most BC applications, it is desirable to issue an interrupt request following the completion of a multimessage frame of messages. This may be enabled by setting the BC_END_OF_FRAME bit in the Interrupt Mask Register. In both single frame and frame auto-repeat modes, this interrupt will occur following the completion of each frame of messages.

END_OF_MESSAGE: This interrupt will occur at the end of every message. For a retried message, the interrupt will occur after the **last** retry.

BC MESSAGE INTERRUPT: Interrupts may be generated at the end of **selected** messages in ENHANCED BC Mode. This is enabled by configuring the ACE/Mini-ACE for ENHANCED BC Mode by programming ENHANCED MODE (bit 15 in Configuration Register #3) to logic "1," **and** EXPANDED BC CONTROL WORD ENABLED (bit 12 of Configuration Register #4) for logic "1," **and** by setting the BC MESSAGE INTERRUPT bit (bit 4 in the Interrupt Mask Register) to logic "1." In this mode, an EOM interrupt will be generated if the EOM INTERRUPT ENABLE bit, bit 4 in the BC Control Word, is programmed to logic "1."

FORMAT ERROR: This interrupt request will be issued following any message containing an invalid word or wrong number of words.

RETRY: This interrupt will occur after the **last** retry attempt (whether successful or unsuccessful) for any message that is retried.

STATUS SET: This interrupt will be issued following a message with either an incorrect RT address in a Status Word and/or one or more bits set to logic "1" in the RT Status Word. In ENHANCED BC mode, Status Word bits that have been masked by the respective bits in the BC Control Word **will not** result in a STATUS SET interrupt.

COMMAND STACK ROLLOVER: This interrupt request occurs when the BC Command Stack rolls over at a predefined boundary in the

ACE/Mini-ACE address space. This boundary is programmable from among 256, 512, 1024, or 2048 words.

TIME TAG ROLLOVER: This interrupt occurs when the value of the ACE/Mini-ACE's Time Tag Register counter rolls over from FFFF to 0000.

5.5 OTHER BC FUNCTIONS

Automatic Retries

The ACE/Mini-ACE BC will perform automatic retries based on no response timeout, a message error, the Message Error Status Word bit set by a MIL-STD-1553A RT, or a Status Set condition. Retries can only be enabled in the ENHANCED BC mode. This requires the ENHANCED MODE ENABLE bit (bit 15 in Configuration Register #3) to be set to logic "1." Retries are then enabled for individual messages by setting the RETRY ENABLE bit (bit 8) in the respective BC Control Word(s).

Retry Conditions. A no response timeout or a message format error will always cause a retry if retry is enabled for the current message. A retry on a "status set" condition will only occur if the RETRY IF STATUS SET bit (bit 9 in Configuration Register #4) is set to logic "1." The status set condition is based on the status mask bits in the BC Control Word. A message format error condition occurs when the RT address in the status response does not match the RT address in the command word, there is an invalid word (parity, manchester error, etc.), there is an incorrect sync type (for both status and data words), or there is a low or high word count.

A retry will also occur if the Message Error bit in the status word response is set to logic "1" **and** the 1553 A/$\overline{B}$ SELECT bit (bit 3 in the BC Control Word) is set to logic "1" (1553A mode) **and** the RETRY IF - 1553A AND MESSAGE ERROR bit (bit 10 in Configuration Register #5) is set to logic "1." The reason this retry is enabled for 1553A mode only is that in MIL-STD-1553B mode, the Message Error bit (S10) is used only to indicate illegal commands. MIL-STD-1553A, on the other hand, uses the Message Error bit as a means for the RT to indicate to the BC that it received a valid command, but one of the associated Data Words had a parity, Manchester encoding, or bit count error (a 1553B RT would not respond at all to this message).

Number of Retries. The ACE/Mini-ACE will attempt a maximum of two retries before it indicates a no response timeout or other retry condition. The maximum number of retries that will be attempted for any particular message is programmable by means of DOUBLE/$\overline{\text{SINGLE}}$ RETRY, bit 3 of Configuration Register #1. If DOUBLE/$\overline{\text{SINGLE}}$ RETRY is logic "0,"

one retry will be attempted; if DOUBLE/$\overline{\text{SINGLE}}$ RETRY is logic "1," a maximum of two retries will be attempted.

Retry Channel Selection. The bus that the first retry is performed on (alternate or same, with respect to the original bus channel) is selected by the programming of the 1ST RETRY ALT/$\overline{\text{SAME}}$ bit (bit 8 in Configuration Register #4) to logic "0" (for same bus) or to logic "1" (for alternate bus). The bus that the second retry is performed on is selected by programming the 2ND RETRY ALT/$\overline{\text{SAME}}$ bit (bit 7 in Configuration Register #4) to logic "0" (for same bus) or to logic "1" (for alternate bus). This allows for six possible retry scenarios: same, alternate, same/same, same/alternate, alternate/same, alternate/alternate.

Retry Block Status Word Bits. The End-of-Message for a retried message occurs after the completion of message retries, not after the initial failed message, or after an unsuccessful first of two retries. The ACE/Mini-ACE writes the Block Status Word to shared RAM during the End-of-Message transfer sequence. RETRY COUNT 1 (bit 5 in the BC Block Status Word,) indicates that one retry occurred when it is set to logic "1." A logic "1" in the RETRY COUNT 2 bit (bit 6 in the Block Status Word) indicates that two retries were attempted. A logic "0" in both RETRY COUNT 1 and RETRY COUNT 2 indicates that no retries occurred. If the second retry fails, the message is aborted and the cause of the failure is stored in the Block Status Word (no response timeout, format error, Status Set, etc).

Retry Interrupts. If enabled by the Interrupt Mask Register, the EOM and/or BC RETRY interrupt requests will be issued **AFTER** the completion of the message retries, for either **an unsuccessful retry or a successful retry.**

If a retry is enabled for a particular message, the retry **will** be attempted even if one or more of the following bits of Configuration Register #1 (bits 12 through 9) are set to logic "1": MESSAGE STOP-ON-ERROR, FRAME STOP-ON-ERROR, STATUS SET STOP-ON-MESSAGE, and STATUS SET STOP-ON-FRAME. Assuming that MESSAGE or FRAME STOP-ON-ERROR is set and that the retry(ies) is(are) not successful, the processing of BC messages will stop at the end of the current message or message frame. However, the processing of subsequent BC messages within a frame and/or the processing of subsequent BC frames **will continue** if a failed message is successfully retried.

BC Response Timeout

MIL-STD-1553B defines RT response time as the delay from the mid-parity zero crossing of the parity bit of the last word received from the BC (or another RT) to the mid-sync zero crossing of the RT's Status Word. In accordance with this definition, the -1553B standard specifies that an

RT must respond within 12 µs and that a BC must wait a **minimum** of 14 µs before determining that an RT "no response" has occurred.

The response timeout value for the ACE/Mini-ACE bus controller is software programmable. For the non-ENHANCED MODE (bit 15 of Configuration Register #3 is logic "0"), the value of the BC response timeout timer defaults to a nominal value of 18.5 µs. In the ENHANCED MODE, the ACE/Mini-ACE supports the use of long buses and/or repeaters by allowing the nominal value of the BC timeout to be selected from among 18.5, 22.5, 50.5, and 130 µs by means of bits 10 and 9 (RESPONSE TIMEOUT 1, 0) of Configuration Register #5. Refer to TABLE 67.

TABLE 67. BC RESPONSE TIMEOUT SELECT

BIT 10 RESPONSE TIMEOUT SELECT 1	BIT 9 RESPONSE TIMEOUT SELECT 0	RESPONSE TIMEOUT TIME VALUE (µs)
0	0	18.5 [1]
0	1	22.5
1	0	50.5
1	1	130

Note: 1. Default value for non-ENHANCED mode is 18.5 µs

5.5.1 BC Status Word Masking

The BC mode of the ACE/Mini-ACE has the capability of masking selected Status Word bits for individual messages in a BC frame while ENHANCED MODE ENABLE (bit 15 in Configuration Register #3) **and** EXPANDED BC CONTROL WORD ENABLE (bit 12 of Configuration Register #4) are programmed to logic "1." In the non-ENHANCED mode **or** if EXPANDED BC CONTROL WORD ENABLE is logic "0," only bits 7, 6, 5, 2, 1, and 0 of the BC Control Word are operative. In this case, the only operative "Status Mask" bit in the BC Control Word is MASK BROADCAST (bit 5). If EXPANDED BC CONTROL WORD ENABLE is logic "1," **all 15** bits of the BC Control Word (bits 14 through 0), including **all** of the "Status Mask" bits (bits 14 through 9, and bit 6) are operative.

The Status Word Mask bits, in the BC Control Word, control which bits in the responding RT Status Word(s) will cause a "Status Set" condition to occur. A "Status Set" condition will cause a bit to be set in the Block Status Word, can cause an interrupt, can halt the BC after the current message or at the end of the current BC frame, and/or initiate an automatic retry.

A logic **"1"** in the proper bit position in the BC Control Word will cause the ACE/Mini-ACE to **ignore ("don't care")** the respective RT Status Word Bit. Any designated subset of the following bits may be enabled in determining a Status Set condition: Illegal Bit (S10), Service Request Bit (S08), Subsystem Busy Bit (S03), Subsystem Flag Bit (S02), Terminal Flag Bit (S00) and/or the Reserved Bits (S09, S07-S05, S01). The Broadcast Bit (S04) can either be masked (ignored) or verified to be logic "0" or logic "1." If the corresponding mask bit is programmed to logic **"0,"** the bit **is included** in determining if a "Status Mask" condition occurs.

With the exception of the Broadcast Command Received Status Word bit, the effect of the ENHANCED MODE, EXPANDED BC CONTROL WORD ENABLE, the various "Status Mask" BC Control Word bits, and the value of the respective received RT Status Word on the "Masked Status Set" condition is summarized in TABLE 68.

TABLE 68. OPERATION OF STATUS MASKING

ENHANCED MODE (bit 15 of Configuration Register #3)	EXPANDED BC CONTROL WORD ENABLED (bit 12 of Configuration Register #4)	"MASK" bit for the particular Status Word bit (in BC Control Word)	Value of the respective bit in Received RT Status Word	Masked Status Set Condition
0	X	X	X	No
or				
X	0			
1	1	0	0	No
		0	1	Yes
		1	0	No
		1	1	No

The function of the Broadcast Mask Bit is determined by the value of the BRDCST MASK ENA/$\overline{\text{XOR}}$ bit (bit 11 in Configuration Register #4). If the BRDCST MASK ENA/$\overline{\text{XOR}}$ bit is programmed to logic "1," a value of logic "1" in the BC Control Word MASK BROADCAST bit (bit 5) will result in the Broadcast Command Received bit in the responding RT Status Word(s) to be ignored ("don't care"), while a logic "0" in the MASK BROADCAST bit will result in a STATUS SET condition, if the Broadcast Command Received bit in the RT Status Word is logic "1."

Programming BRDCST MASK ENA/$\overline{\text{XOR}}$ to logic “0” will cause the ACE to compare the Broadcast Bit in the received RT Status Word to the value in the MASK BROADCAST BIT (bit 5 in the BC Control Word). In

the case that they **do not match,** a "Status Set" condition will be generated. The operation of the BRDCST MASK ENA/$\overline{\text{XOR}}$ and MASK BROADCAST bits is summarized in TABLE 69.

TABLE 69. OPERATION OF STATUS MASKING (Including Broadcast Command Received)

ENHANCED MODE (BIT 15 OF CONFIGURATION REGISTER #3)	BROADCAST MASK ENABLED/ $\overline{\text{XOR}}$ (BIT 11 CONFIGURATION REGISTER #4)	EXPANDED BC CONTROL WORD ENABLED (BIT 12 OF CONFIGURATION REGISTER #4)	MASK BROADCAST (BIT 5 OF BC CONTROL WORDS)	VALUE OF "BROADCAST COMMAND RECEIVED" BIT IN RECEIVED RT STATUS WORD	MASKED STATUS SET CONDITION
0	X	X	0	0	No
	or		0	1	Yes
			1	0	Yes
1	0	X	1	1	No
1	1	X	0	0	No
			0	1	Yes
			1	0	No
			1	1	No

The Block Status Word contains two bits describing the status set condition. The first is the STATUS SET bit (bit 11). This bit will be set to logic "1" if **any** of the bits in the status response are logic "1" regardless of the status mask. STATUS SET 2 (bit 7) will only be set to logic "1" if a bit in the Status Word response is set **and** that bit is not masked by the status mask in the BC Control Word (with the exception of the Broadcast Command Received bit "expected value" option, as described above).

An interrupt will be generated for a Status Set condition (based on the status mask criteria) in the ENHANCED BC Mode, if the BC STATUS SET bit (bit 1 in the Interrupt Status Mask) is set to logic "1." The interrupt will occur at the end of the current message (EOM), not immediately following the receipt of the Status Word (in the case of a transmit command).

A Status Set condition, in the ENHANCED BC Mode, can cause the bus controller to halt in one of two ways. First, if the MESSAGE STOP-ON-ERROR bit (bit 12 in Configuration Register #1) is set to logic "1," the BC will halt the current frame upon completion of the current message. In the FRAME AUTO-REPEAT mode, if FRAME STOP-ON-ERROR (bit 11 in Configuration Register #1) is set to logic "1," the BC will halt the current frame upon completion of the last message in the frame.

5.6 BC SOFTWARE INITIALIZATION SEQUENCE

The following software sequence is typical of the steps the host CPU should perform following power turn-on to configure the ACE/Mini-ACE for BC operation. For most applications, many of the steps indicated may be skipped.

1) Perform a software reset, by writing a value of 0001 (hex) to the Start/Reset Register.

2) If any of the ENHANCED mode functions (e.g., use of programmable retries, message gaps, expanded BC Control Word, etc.) are to be used, invoke the ACE/Mini-ACE's ENHANCED MODE by writing a value of 8000 (hex) to Configuration Register #3.

3) Initialize the Interrupt Mask Register. For most BC applications, the BC END-OF- FRAME interrupt should be enabled. The END-OF-MESSAGE (EOM) bit causes an interrupt request to be issued following the end of **every** completed message. BC CONTROL WORD interrupt allows interrupt requests to be issued following completion of **selected** (by means of the BC Control Word) messages. BC RETRY will result in an interrupt **after** a message is retried (either successfully or, unsuccessfully).

   FORMAT ERROR will cause an interrupt request to be issued following any RT response containing either a word error (sync or Manchester encoding, bit count, or parity error) or a high or low word count error. A STATUS SET interrupt results from one of three conditions: (1) A nonmatching RT address in the Status Word from a responding RT; (2) If EXPANDED BC CONTROL WORD is not enabled, one or more of the 8 nonreserved Status Word bits is logic "1"; or (3) If EXPANDED BC CONTROL WORD is enabled, and for one or more of the RT Status Word bits the respective Status Mask bit in the BC Control Word is programmed for "care" (logic "0") **and** the value of the received RT Status Word bit is logic "1."

4) Initialize Configuration Register #1. Bits 15 and 14 must both be initialized to logic "0" to configure the ACE for BC mode. CURRENT AREA B/$\overline{A}$ should be designated. MESSAGE STOP-ON-ERROR, FRAME-STOP-ON-ERROR, MESSAGE-STOP-ON-STATUS SET, and FRAME-STOP-ON-STATUS SET should be selected, if desired. The STOP-ON-ERROR bits enable a "graceful halt" (at the **end** of the current message or frame) in the case of a response timeout, format error or loop test failure. The STOP-ON-STATUS SET bits enable a

"graceful halt" condition for a "Status Set" condition, as defined above. It should be noted that if a message retry is enabled for a particular message, the retry will be attempted **before** the "stop" takes place. That is, if the retry is successful, the message frame will **continue** (will not stop). If the retry (one or two retries) is unsuccessful, then the processing of messages will be aborted at the end of the current message or frame.

If it is desired to initiate a BC frame using the EXT_TRIG input, EXTERNAL TRIGGER ENABLED must be programmed to logic "1." Regardless of the programming of EXTERNAL TRIGGER ENABLED and INTERNAL TRIGGER ENABLED, a BC frame may be initiated by means of a software BC START command. If it is desired to have the programmed BC frame repeat automatically (with no CPU intervention), it is necessary to program FRAME AUTO-REPEAT **and** INTERNAL TRIGGER to logic "1." If it desirable to start the first BC frame via the EXT_TRIG input and have the frame automatically repeat subsequently, FRAME AUTO-REPEAT, INTERNAL TRIGGER ENABLED and EXTERNAL TRIGGER ENABLED must be programmed to logic "1."

In order to control the BC message gap times using the third word of the BC Block Descriptor, MESSAGE GAP TIME ENABLED must be programmed to logic "1." If MESSAGE GAP TIME ENABLED is logic "0," the start-of-current message to start-of-subsequent message time will default such that the BC's intermessage gap time (as defined by MIL-STD-1553B) defaults to its minimum value of approximately 9 µs.

If message retries are to be enabled by means of bit 8 of the BC Control Words (RETRY ENABLED), it is necessary to program RETRY ENABLED to logic "1." If retries are enabled, the maximum number of retries for each message (either 1 or 2) is specified by means of DOUBLE/$\overline{\text{SINGLE}}$ RETRY.

5) Initialize Configuration Register #2. For BC mode, it is strongly recommended that 256-WORD BOUNDARIES DISABLED be set to logic "1" in order to make best use of the ACE/Mini-ACE's address space for BC message blocks. LEVEL/$\overline{\text{PULSE}}$ INTERRUPT should be initialized to logic "1" if the host CPU requires a level, rather than a pulse, type of interrupt request input signal. TIME-TAG RESOLUTION 2-0 should be programmed to initialize the resolution of the Time-Tag Register. The default resolution ("000") is 64 µs/LSB.

6) Initialize Configuration Register #3. If any of the lower 15 bits of this register or any of the other ENHANCED mode features are

to be used, ENHANCED MODE ENABLED (bit 15) must be maintained at logic "1" while writing to this register. The size of the Stack may be programmed by means of bits 14 and 13. The choices for the stack size are 256 words (default, for 64 BC messages), 512, 1024, and 2048 words (512 messages).

7) Initialize Configuration Register #4. In order to allow the use of bits 15-8, 4, and 3 of the BC Control Word, EXPANDED BC CONTROL WORD must be set to logic "1." This includes use of the Status Word Masking function, retries, 1553A/B selection, and interrupts on a message basis. BROADCAST MASK ENABLED/$\overline{\text{XOR}}$ should be programmed to logic "1" if it is desired to use the "MASK BROADCAST BIT" bit (bit 5) of the BC Control Word as an actual mask, rather than to specify the anticipated value of the Broadcast Command Received bit in the RT Status Word.

   RETRY IF -1553A AND MESSAGE ERROR should be set if it is desired to retry messages in which the 1553A/$\overline{\text{B}}$ SELECT bit (bit 3) of the BC Control Word is logic "1" and the Message Error bit is logic "1" in the RT Status Word. RETRY IF STATUS SET should be set to logic "1" if it is desired to retry messages in which one or more of the "unmasked" Status Word bits is logic "1" in the RT Status Word. A Status Word bit is considered "unmasked" if the corresponding "MASK" bit in the BC Control Word has been programmed to logic "0."

   If VALID BUSY/NO DATA and/or VALID MESSAGE ERROR/NO DATA is set to logic "1," an RT response will be considered valid if the BUSY (MESSAGE ERROR) bit(s) is set in the RT Status Word and there are no following Data Words. Otherwise, such an RT response will be considered invalid. Message validity affects the setting of the FORMAT ERROR bit in the Block Status Word, the issuing of interrupts, and message retries.

8) Initialize Configuration Register #5. The default clock frequency for the ACE is 16 MHz. To select 12 MHz operation, 12 MHZ SELECT must be programmed to logic "1."

   EXPANDED ZERO-CROSSING should be programmed to logic "1" to expand the Manchester decoders' tolerance for zero crossing distortion by enabling sampling at a 32 MHz (or 24 MHz) rate (Mini-ACE series terminals are always enabled for EXPANDED ZERO-CROSSING). RESPONSE TIMEOUT SELECT 1-0 selects the time value for the BC response timeout from among 18.5 µs (default), 22.5, 50.5, or 130 µs. If GAP CHECK ENABLED is set to logic "1," the BC will verify for a

minimum bus dead time of 2 µs prior to RT responses. If this gap time is violated, the BC will set the FORMAT ERROR bit in the Block Status Word. As a result, an ERROR interrupt may be issued and/or the message may be retried.

9) If desired, initialize the Time-Tag Register. It should be noted that the value of the Time-Tag Register may be reset to zero simultaneous with the BC Start by writing logic "1" to the TIME-TAG RESET bit of the Start/Reset Register as part of step (15).

10) If using the Frame Auto-Repeat mode (FRAME AUTO-REPEAT and INTERNAL TRIGGER ENABLED bits of Configuration Register #1 programmed to logic "1"), initialize the BC Frame Time Register. This register is programmable with a resolution of 100 µs/LSB.

11) Load the starting location of the Stack into the active area Stack Pointer RAM location. If the Frame Auto-Repeat mode is to be used, the Initial Stack Pointer RAM location for the active area should also be loaded.

12) Initialize the Active Area Stack. For the message descriptor for each message to be processed, the Message Block Address, providing the pointer to the first word of the respective BC message block (the BC Control Word) must be written by the CPU.

    If the Message Gap-Time feature is used, the Message Gap-Time word must also be written for each message. The resolution of the Message Gap-Time Word is 1 µs/LSB. The programmed value of the Message Gap-Time field represents the time from the **start** of the current message to the **start** of the subsequent message. If this time is less than the time required for the current message, the gap prior to the start of the subsequent message defaults to the minimum value of approximately 9 µs.

    If it is desired to poll the stack during the processing of the BC frame, it is recommended that the values of the Block Status Words be initialized to zero by the host CPU.

13) Load the BC Control, Command, and Data Words to be transmitted into the respective BC message blocks. Optionally, the locations of the anticipated Loopback Words should be loaded with a **different** bit pattern than the last word to be transmitted by the BC. The host processor must ensure that sufficient address locations are allocated after the last word to be transmitted to accommodate the Loopback Word and

anticipated received Status and Data Words.

14) The Active Area Message Count location should be loaded with the **ones complement** of the number of messages to be processed in the frame. If the Frame Auto-Repeat mode is to be used, the Initial Message Count RAM location for the active area should be loaded.

15) If EXTERNAL TRIGGER ENABLED is programmed to logic "0," a BC frame must be initiated by performing a BC START operation. This is invoked by writing a value of 0002 (hex) to the Start/Reset Register. If EXTERNAL TRIGGER ENABLED is programmed to logic "1," a BC frame may be initiated either by a BC START operation or by applying a rising edge on the EXT_TRIG input.

5.7 BC PSEUDO CODE EXAMPLE

The following example illustrates the programming steps necessary to initialize the ACE Bus Controller and initiate a frame of messages.

As illustrated in FIGURE 8, the example consists of three messages: a BC-to-RT transfer, an RT-to-RT transfer, and a Synchronize with data mode code message.

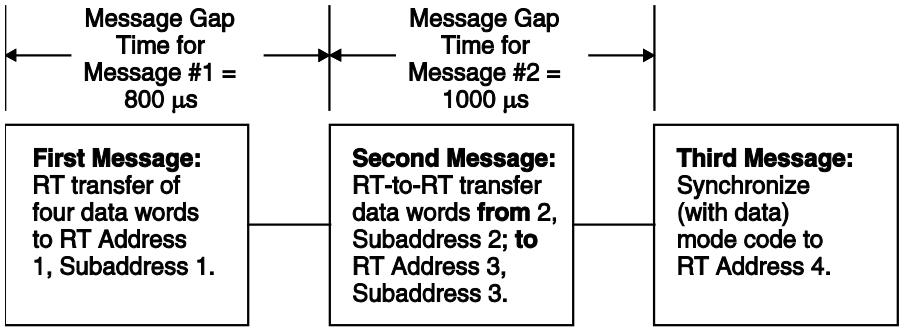


FIGURE 8. MESSAGE SEQUENCE FOR BC PSEUDO CODE EXAMPLE

FIGURE 9 illustrates the detailed sequences of words to be transmitted and received for the three individual messages.

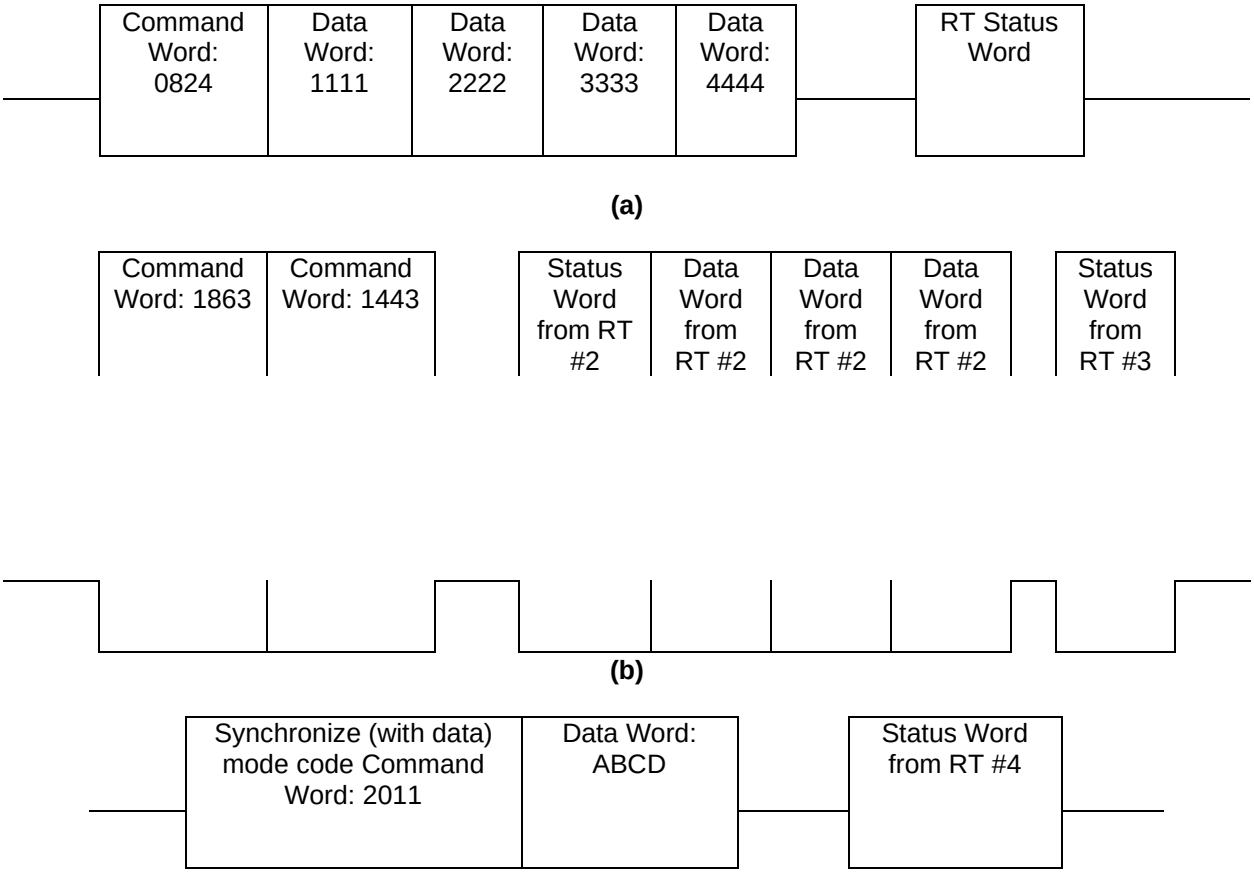


FIGURE 9. MESSAGES FOR BC PSEUDO CODE EXAMPLE

(a) FIRST MESSAGE;(b) SECOND MESSAGE; (c) THIRD MESSAGE

TABLE 70 illustrates the memory map to program the example sequence of messages.

TABLE 70. MEMORY MAP FOR BC EXAMPLE PSEUDO CODE

ADDRESS	DATA	DESCRIPTION	PORTION OF MEMORY, COMMENT
000	0000	Message #1 Block Status Word.	Message #1 Block Descriptor (in Stack Area). Note that the Block Status Word and Time Tag locations are initialized to 0000. These locations will be overwritten by the ACE/Mini-ACE when the Message is processed.
001	0000	Message #1 Time-Tag Word.	
002	0320	800 µs Message Gap-Time Word for Message #1.	
003	0108	Message Block Pointer for Message #1.	
004	0000	Message #2 Block Status Word.	Message #2 Block Descriptor (in Stack Area). Note that the Block Status Word and Time Tag locations are initialized to 0000. These locations will be overwritten by the ACE/Mini-ACE when the Message is processed.
005	0000	Message #2 Time-Tag Word.	
006	03E8	1000 µs Message Gap-Time Word for Message #2.	
007	0110	Message Block Pointer for Message #2.	
008	0000	Message #3 Block Status Word.	Message #3 Block Descriptor (in Stack Area). Note that the Block Status Word and Time Tag locations are initialized to 0000. These locations will be overwritten by the ACE/Mini-ACE when the Message is processed.
009	0000	Message #3 Time-Tag Word.	
00A	0000	0 µs Message Gap- Time Word for Message #3 (doesn't matter).	
00B	0119	Message Block Pointer for Message #3.	
100	0000	Active Area (Area A) Stack Pointer.	Fixed locations
101	FFFC	Active Area (Area A) Message Count Register. Note that 00FC is the ones complement of the number of messages to be processed (3).	
108	0180	BC Control Word for Message #1. Note that for this message, a "BC Control Word" interrupt is enabled. Also, the message will be transmitted on Channel A.	Message Block for Message #1.
109	0824	Command Word for Message #1.	
10A	1111	First Data Word to be transmitted for Message #1.	
10B	2222	Second Data Word to be transmitted for Message #1.	
10C	3333	Third Data Word to be transmitted for Message #1.	
10D	4444	Fourth Data Word to be transmitted for Message #1.	
10E	0000	Location for anticipated loopback of data word #4.	
10F	0000	Location for anticipated received Status Word for Message #1 programmed to 0000.	
110	0101	BC Control Word for Message #2. Note that for this message, retries are enabled, the message will be processed on Channel B, and the message format is an RT-to-RT transfer.	Message Block for Message #2
111	1863	Receive Command Word (to RT Address #3).	
112	1443	Transmit Command Word (to RT Address #2).	
113	0000	Location for anticipated loopback of transmit command.	
114	0000	Anticipated location for received Status Word from the transmitting RT (RT Address #2).	
115	0000	Anticipated location for the first received Data Word from RT #2.	
116	0000	Location for the second anticipated received Data Word from RT #2.	
117	0000	Location for the third anticipated received Data Word from RT #2.	
118	0000	Location for the anticipated received Status Word from the receiving RT (RT Address #3).	
119	0084	BC Control Word for Message #3. The message will be processed on Channel A, and is a mode-code message.	Message Block for message #3.
11A	2011	Synchronize with data mode-code Command Word to RT Address 4.	
11B	ABCD	Data Word associated for the Synchronize mode command.	
11C	0000	Location for anticipated loopback of data word.	
11D	0000	Location for anticipated received Status Word from the receiving RT (RT Address #4).	

5.7.1 Pseudo Code

The following pseudo code is the series of register and memory write transfers required to initiate the example message frame sequence. The notation "Rxy ⟵" represents a write access to ACE/Mini-ACE register address xy. The notation "Mwxyz ⟵" represents a write access to ACE/Mini-ACE shared RAM address wxyz.

R03 ⟵ 0001-Software reset via the Start/Reset Register

R07 ⟵ 8000-Set ENHANCED MODE bit in Config Register #3 to enable enhanced BC features (retries, Message gap times, etc.)

R00 ⟵ 0018-Interrupt Mask Register: Enable interrupts for BC Control Word (individual message(s)) and BC_END_OF_FRAME

R01 ⟵ 0030-Config Register #1: Configures for BC mode, enables variable Message gap times and message retries

R02 ⟵ 0408-Configuration Register #2: Enables 256-WORD BOUNDARIES DISABLED, LEVEL interrupt

R08 ⟵ 1060-Configuration Register #4: Enables EXPANDED BC CONTROL WORD, VALID BUSY/NO DATA, VALID MESSAGE ERROR/NO DATA

R09 ⟵ 0A00-Config Register #5: Enables EXPANDED ZERO CROSSING, programs BC Response Timeout to 22.5 µs

R05 ⟵ 0000-Initialize Time-Tag Counter Register to 0000

M0100 ⟵ 0000-Initialize Area A Stack Pointer to 0000

M0101 ⟵ FFFC-Initialize Area A Message Counter for three messages

M0000 ⟵ 0000-Initialize Message #1 Block Status Word

M0001 ⟵ 0000-Initialize Message #1 Time-Tag Word

M0002 ⟵ 0320-Message #1 Message Gap-Time Word

M0003 ⟵ 0108-Message #1 Message Block Pointer

M0004 ⟵ 0000-Initialize Message #2 Block Status Word

M0005 ⟵ 0000-Initialize Message #2 Time-Tag Word

M0006 ⟵ 03E8-Message #2 Message Gap-Time Word

M0007 ⟵ 0110-Message #2 Message Block Pointer

M0008 ⟵ 0000-Initialize Message #3 Block Status Word

M0009 ⟵ 0000-Initialize Message #3 Time-Tag Word

M000A ⟵ 0000-Message #3 Message Gap-Time Word

M000B ⟵ 0119-Message #3 Message Block Pointer

M0108 ⟵ 0180-BC Control Word for Message #1

M0109 ⟵ 0824-Command Word for Message #1

M010A ⟵ 1111-First Data Word for Message #1

M010B ⟵ 2222-Second Data Word for Message #1

M010C ⟵ 3333-Third Data Word for Message #1

M010D ⟵ 4444-Fourth Data Word for Message #1

M010F ⟵ 0000-Initialize Loopback word location

M010F ⟵ 0000-Initialize Message #1 anticipated Status Word location

M0110 ⟵ 0101-BC Control Word for Message #2

M0111 ⟵ 1863-First Command Word (receive command) for Message #2

M0112 ⟵ 1443-Second Command Word (transmit command) for Message #2

M0113 ⟵ 0000-Initialize Loopback word location

M0114 ⟵ 0000-Initialize location for anticipated transmitting RT Status Word

M0115 ⟵ 0000-Initialize location for first anticipated received Data Word

M0116 ⟵ 0000-Initialize location for second anticipated received Data Word

M0117 ⟵ 0000-Initialize location for third anticipated received Data Word

M0118 ⟵ 0000-Initialize location for anticipated receiving RT Status Word for Message #2

M0119 ⟵ 0084-BC Control Word for Message #3

M011A ⟵ 2011-Command Word for Message #3

M011B ⟵ ABCD-Data Word for Message #3

M011C ⟵ 0000-Initialize Loopback word location

M011D ⟵ 0000-Initialize location for anticipated received Status Word for Message #3

R03 ⟵ 0002-Start/Reset Register: BC START command, to initiate (single) message frame

5.7.2 Servicing In-Progress or Completed BC Frames

The end of BC messages and frames may be determined by means of either polling or interrupt techniques.

There are several polling techniques that may be used. These involve bits in either Configuration Register #1 and the Interrupt Status Register. In addition, the active area Stack Pointer and Message Count Register may be polled. The Stack Pointer increments by four at the end of each BC message. At the end of a BC frame, it will point to **4 locations beyond (modulo the stack size)** the first word of the message block descriptor (the location of the Block Status Word), for the last message of the BC frame. The Message Counter increments by one at the end of each BC message. When the frame has been completed, the Message Count location will have a value of FFFF (hex).

In the ENHANCED BC mode, the lower three bits of Configuration Register #1 may be polled as a means of determining BC status. BC ENABLED (bit 2) will return logic "1" after a BC frame has been initiated (by either a BC START command or from an external trigger) and up to the time that a single frame has completed or repeat frames have been halted. BC ENABLED will then transition to logic "0."

BC FRAME IN PROGRESS is similar to BC ENABLED, with the following exception: In the frame auto-repeat mode, BC FRAME IN PROGRESS will return logic "0" during the time following the End-of-Message (EOM) sequence for the last message of the frame, up to the

beginning of the Start-of-Message (SOM) sequence for the first message of the subsequent frame.

BC MESSAGE IN PROGRESS will return logic "1" between the time of the SOM sequence and the EOM sequence for each message processed.

If ENHANCED INTERRUPTS are enabled (bit 15 of Configuration Register #2 programmed to logic "1"), and the Interrupt Mask Register is programmed to logic "0" (disabling interrupt requests from the ACE), the Interrupt Status Register may still be polled for a number of conditions in BC mode. These include BC COMMAND STACK ROLLOVER (bit 11), BC RETRY (bit 8), TIME TAG ROLLOVER (bit 6), BC MESSAGE INTERRUPT (bit 4), BC END OF FRAME (bit 3), FORMAT ERROR (bit 2), STATUS SET (bit 1), and END OF MESSAGE (bit 0).

Note that any of the conditions listed in the previous paragraph may also be used to trigger an interrupt request to the host CPU. In most systems, an interrupt request will be enabled to signify a BC END OF FRAME condition. This indicates that a BC frame has been completed. In other systems, the BC RETRY interrupt request (for **selected** messages, as programmed in the BC Control Words) or the END-OF-MESSAGE interrupt request (for **all** messages) may be used.

The FORMAT ERROR and BC RETRY interrupt conditions may be used to inform the host of any bus error conditions. STATUS SET may be used to indicate to the CPU that one of the unmasked Status Word bits has been set in a responding RT's Status Word. A particular Status Word bit may be enabled to cause a Status Set condition by programming the respective Status Mask bit BC Control Word to logic "0."

The Status Mask bits may be used in conjunction with the STATUS SET STOP-ON-MESSAGE (bit 10) bits of Configuration Register #1. In this way (or via the ERROR-STOP-ON-MESSAGE bit), the host is able to interject asynchronous messages. An example of such an asynchronous message is for the BC to process a single-message frame consisting of a Transmit Vector Word mode command following reception of an RT Status Word with the Service Request bit set. After the host has processed this message and captured the RT's Vector Word, it may then resume processing of the in-line BC frame.

5.7.3 Terminating of BC Frames

Under most circumstances, a programmed BC frame will process all of the programmed messages in the frame. That is, the ACE/Mini-ACE BC will continue to process messages until the Message Count location has

incremented to FFFF. In the frame auto-repeat mode with INTERNAL TRIGGER ENABLED, the subsequent BC frame will automatically restart after one frame has been completed.

The ACE/Mini-ACE provides a number of mechanisms for aborting BC frames. Bits 12 through 9 of Configuration Register #1 provide mechanisms for automatically halting the ACE/Mini-ACE BC. If set to logic "1," ERROR STOP-ON-MESSAGE and STATUS SET STOP-ON-MESSAGE will cause the ACE/Mini-ACE BC to stop processing messages at the end of the **current message** if a Format Error or Status Set condition occurs. If the ACE BC is programmed for the frame auto-repeat mode, ERROR STOP-ON-FRAME and STATUS SET STOP-ON-FRAME will cause the ACE/Mini-ACE BC to stop processing messages at the end of the **current frame** if a Format Error or Status Set condition occurs.

Some of the bits in the Start/Reset Register provide a mechanism for the host CPU to terminate the processing of messages by the host BC. RESET will result in an **immediate** (that is, aborting the current message) termination of message processing. BC STOP ON MESSAGE and BC STOP-ON-FRAME will cause the ACE/Mini-ACE to terminate message processing at the **end** of the current message or frame.

5.7.4 BUS Controller Start-of-Message, End-of-Message, and Retry Transfer Sequences

At the start and end of each message, and prior to the processing of a message retry, the ACE/Mini-ACE performs the following sequences of transfers from/to the shared RAM:

BC Start-of-Message (SOM) Sequence

1) The Stack Pointer is read from the active area Stack Pointer location. This address is used for accessing the BC descriptor block in the active area Command Stack.

2) The Message Gap-Time word is read from the third location in the block descriptor.

3) The Message Block Pointer word is read from the fourth location in the block descriptor. This pointer provides the starting address of the BC message block (address of the BC Control Word).

4) The BC Control Word is read from the first location in the BC message block.

5) The (first) Command Word is read from the second location in the BC message block.

6) The Time-Tag word is written to the second location in the block descriptor.

7) The Block Status Word is written to the first location in the block descriptor.

BC End-of-Message (EOM) Sequence

1) The Message Count word is read from the active area Message Counter location. If the value of this word is less than FFFF (hex), the ACE/Mini-ACE (internally) increments the value by one. If the value of this word is equal to FFFF (hex), this denotes that the current message is the last message of the frame. The current frame is terminated following the end of the current EOM sequence.

2) The Time-Tag word is written to the second location in the block descriptor.

3) The Block Status Word is written to the first location in the block descriptor.

4) The Message Count Word is written to the active area Message Counter location.

5) The value of the Stack Pointer is incremented by four. The updated value is written to the active area Stack Pointer location.

BC Message Retry Sequence

1) The Message Count word is read from the active area Message Counter location.

2) The BC Control Word is read from the first location in the BC message block.

3) The (first) Command Word is read from the second location in the BC message block.

BC Exception Conditions

In response to various message errors and other exception conditions, the ACE/Mini-ACE bus controller takes actions and provides a number of indications. TABLE 71 indicates the respective Block Status Word bits that will be set, automatic retry activity, and interrupt requests that are

issued and Interrupt Status Register bits that become set as a result of these conditions.

TABLE 71. BC EXCEPTION CONDITIONS

	BLOCK STATUS WORD BITS	AUTOMATIC RETRIES (IF ENABLED)	INTERRUPTS, INTERRUPT STATUS WORD BITS	OTHER EFFECTS
No Response	ERROR FLAG, NO RESPONSE TIMEOUT, RETRY COUNT(1,0) (if enabled)	Yes	FORMAT ERROR, BC RETRY (if enabled)	
Received Word Count Error	ERROR FLAG, WORD COUNT ERROR, FORMAT ERROR, RETRY COUNT(1,0)(if enabled)	Yes	FORMAT ERROR, BC RETRY (if enabled)	
Incorrect Received Sync Type	ERROR FLAG, INCORRECT SYNC TYPE, FORMAT ERROR, RETRY COUNT (0,1)(if enabled)	Yes	FORMAT ERROR, BC RETRY (if enabled)	
Invalid Received Word (Manchester encoding, Bit Count, or Parity)	ERROR FLAG, FORMAT ERROR, INVALID WORD, RETRY COUNT(1,0)(if enabled)	Yes	FORMAT ERROR, BC RETRY (if enabled)	Note: If the ACE BC receives an invalid Data Word, it will continue to receive (but not store) all subsequent, contiguous Data Words. It will wait until it senses an idle bus before performing an EOM or retry transfer sequence, performing a message retry, or transmitting the next message.
Wrong RT Address in Received Status Word	ERROR FLAG, WRONG STATUS ADDRESS/NO GAP, FORMAT ERROR, RETRY COUNT(1,0)(if enabled)	Yes	STATUS SET, BC RETRY (if retry enabled for Status Set)	
Handshake Fail. Note that in BC mode, a Handshake Failure will not occur during a Start-of-Message (SOM), End-of-Message (EOM), or Retry transfer sequence. A Handshake Failure can occur during the transfer of a second Command Word (for an RT-to-RT transfer), Data Word, or RT Status Word. A Handshake Failure can occur in the Transparent Mode only) not in the buffered mode.	Block Status Word from Start-of-Message Sequence	No	HANDSHAKE FAIL	BC Frame is terminated.
Less than 2 µs gap before Status Word Response and	ERROR FLAG, FORMAT ERROR, WRONG STATUS ADDRESS/NO GAP,	Yes	FORMAT ERROR, BC RETRY (if enabled)	

TABLE 71. BC EXCEPTION CONDITIONS				
	BLOCK STATUS WORD BITS	**AUTOMATIC RETRIES (IF ENABLED)**	**INTERRUPTS, INTERRUPT STATUS WORD BITS**	**OTHER EFFECTS**
ENHANCED MODE and GAP CHECK ENABLED, bit 7 of Configuration Register #5 is logic "1"	RETRY COUNT(1,0)(if enabled)			
Loop Test Fail Transmitter Timeout: Transmitter attempts to transmit for longer than 668 µs	ERROR FLAG, LOOP TEST FAIL Block Status Word stored during Start-of-Message Sequence	No No	FORMAT ERROR BC/RT TRANSMITTER TIMEOUT	BC Frame is terminated
Non-ENHANCED mode or Expanded BC Control Word not enabled, and one or more bits set in RT Status Word	ERROR FLAG, STATUS SET, RETRY COUNT(1,0)(if RETRY IF STATUS SET, bit 9 of Configuration Register #4, is programmed to logic "1")	Yes, if RETRY IF STATUS SET, bit 9 of Configuration Register #4, is programmed to logic "1"	BC STATUS SET, BC RETRY(if retry enabled for Status Set)	
ENHANCED mode and Expanded BC Control Word enabled, and one or more bits set in RT Status Word with the corresponding STATUS SET bit(s) in the BC Control Word programmed to logic "0"	ERROR FLAG, STATUS SET, MASKED STATUS SET, RETRY COUNT(1,0)(if retry enabled for Status Set)	Yes, if RETRY IF STATUS SET, bit 9 of Configuration Register #4, is programmed to logic "1"	BC STATUS SET, BC RETRY(if retry enabled for Status Set)	
ENHANCED mode and Expanded BC Control Word enabled, and one or more bits set in RT Status Word with the corresponding STATUS SET bit(s) in the BC Control Word programmed to logic "1" and no bits set in the RT Status Word with the corresponding STATUS SET bit(s) in the BC Control Word programmed to logic "0"	ERROR FLAG, STATUS SET	No	None	
With VALID M.E./NO DATA = "0"; in Response to a Transmit Command, Message Error bit Set in Status Word, followed by no Data Words	ERROR FLAG, STATUS SET, MASKED STATUS SET (unless using Expanded BC Control Word and the M.E. MASK bit is logic "1"), FORMAT ERROR, WORD COUNT ERROR, RETRY COUNT(1,0) (if enabled)	Yes	FORMAT ERROR, BC STATUS SET (if Expanded BC Control Word is not enabled or if the M.E. MASK bit in the BC Control Word is logic "0"), BC RETRY (if enabled)	
With VALID M.E./NO DATA = "0"; in Response to a Transmit Command, Message Error bit Set in Status Word, Followed by the Correct Number of Data Words	ERROR FLAG, STATUS SET, MASKED STATUS SET (unless using Expanded BC Control Word and the M.E. MASK bit is logic "1"), RETRY COUNT(1,0) (if retry enabled for Status Set, unless using Expanded BC Control Word and the M.E. MASK bit is logic "1")	Yes, (if retry enabled for Status Set, unless using Expanded BC Control Word and the M.E. MASK bit is logic "1")	BC STATUS SET (if Expanded BC Control Word is not enabled or if the M.E. MASK bit is logic "0"), BC RETRY (if retry enabled for Status Set, unless using Expanded BC Control Word and the M.E. MASK bit is logic "1")	

5.7.5 BC Off-Line and On-Line Self-Tests

The BC mode of the ACE/Mini-ACE terminals provides a number of self-test features. The internal registers and shared RAM are accessible to the host processor at all times. In addition, the ACE/Mini-ACE BC includes wraparound test provisions for both an off-line self-test and an on-line self-test.

The internal registers and shared RAM can be tested by means of host processor software routines to implement checkerboard, walking zero, walking one and counting patterns and reading back and verifying the contents of the internal RAM.

The BC off-line self-test provides a means of exercising and verifying the parallel address and data paths, encoder, serial data path, decoder, and portions of the BC message format and word count logic, protocol state machine and memory management logic. In the off-line self test, the ACE/Mini-ACE does **not** transmit on the external 1553 bus. Instead, the Manchester II encoder output is routed directly to the decoder input. The off-line self-test can be run following power turn-on as part of system self-test or when the ACE/Mini-ACE hybrid has been functioning in RT mode, as part of a software controlled response to a Reset RT mode code command. A common element of the off-line and on-line BC self-tests is the method by which loopback words are checked. In each case, the received version of all transmitted words is checked for validity (sync, encoding, parity, bit count) and the received version of the last word transmitted by the BC is compared to the transmitted version of the word. The loopback test is considered to have failed if the validity and/or comparison tests do not verify.

Note: *For the BU-61580(1)X6, BU-61585(6)X6, BU-61590, BU-65620 versions of the ACE and the BU-65178/79, BU-61588, and BU-61688/89 of the Mini-ACE, it is important to note that the TX_INH_A and TX_INH_B inputs must be connected to logic "0" in order to pass the off-line self-test. The BC off-line self-test will <u>fail</u> if the respective transmitter inhibit input (TX_INH_A[B]) is connected to logic "1." Note that applying logic "1" to these inputs provides a mechanism for self-testing the transmit inhibit function.*

To run the off-line self-test for a particular message, bit 6 in the BC Control Word (OFF-LINE SELF-TEST) must be programmed to logic "1." As the result of a nonbroadcast self-test message, the RESPONSE TIMEOUT bit of the message's Block Status Word **should be set**. Following a broadcast self-test message, the RESPONSE TIMEOUT bit **should NOT be set.** If the self-test passes, the LOOP TEST FAIL bit of the Block Status Word will not be set. The other portion of determining the success of the BC self-test is to verify that the Loopback Word contents match those of the last transmitted word.

To make the off-line self-test as comprehensive as possible, a large number of self-test messages should be processed. To exercise the various portions of the BC protocol and memory management logic, the message block starting address, message format, data word count and contents of the last word to be transmitted should be varied for the individual test messages.

The off-line self-test may also exercise the ERROR, EOM, BC/RT MESSAGE, and BC_EOM interrupt request features. This may be done by setting the respective bit(s) in the Interrupt Mask register. If the ACE/Mini-ACE is configured for a multimessage frame of off-line self-test messages, an interrupt will occur after every message if the EOM interrupt is enabled. Similarly, an ERROR interrupt request will occur following every nonbroadcast off-line self-test message, due to the RESPONSE TIMEOUT condition. If the BC_EOM interrupt is enabled but the EOM interrupt is not, an interrupt request will only be issued after the **last** message of the frame is processed.

The BC STOP-ON-ERROR feature may be exercised by setting the respective bit in the Configuration Register, configuring the ACE for a multimessage BC frame of off-line self-test messages and verifying that the BC stops processing messages after the first nonbroadcast message of the frame has been processed.

The message gap-time and Time-Tag features may be self-tested by programming the Message gap time(s) for a multimessage frame and verifying the elapsed time of the frame by means of the Time-Tag Register. Automatic retries can be tested since a retry will occur, if programmed, as a result of the RESPONSE TIMEOUT condition resulting from a nonbroadcast off-line self-test message.

For the BC on-line self-test, the last word transmitted on the 1553 bus is monitored by the receiver and fed back to the decoder to formulate the Loopback Word. Similar to the off-line test, the LOOP TEST FAIL bit in the Block Status Word is either set (for fail) or cleared as a result of the Loopback test and the Loopback Word is stored in the Shared RAM. In addition to the digital circuitry exercised by the off-line self-test, the on-line test verifies the operation of the transmitter, receiver, and to a large extent, the external transformers, stub and bus cabling, coupling boxes and termination resistors. Open circuits or other faults in these external components will result in signal reflections; these reflections can result in failures of the loopback test.

6 RT OPERATION

6.1 INTRODUCTION

The ACE/Mini-ACE series RT incorporates all of the features of the previous generation BUS-61553 AIM-HY series and BUS-61559 AIM-HY'er series hybrids. In addition, there is a significant number of new RT features incorporated into the design of the ACE/Mini-ACE.

Some of the principal features of the ACE/Mini-ACE Remote Terminal include implementation of all MIL-STD-1553A/B formats and dual redundant mode codes, internal command illegalizing, implementation of the "Busy" function, an internally formulated BIT Word, and comprehensive error checking, including RT-to-RT transfer errors.

A major enhancement for the ACE RT is its multiprotocol functionality. This includes programmable options to provide support of MIL-STD-1553A, MIL-STD-1553B, and the McAir A3818, A5232 and A5690 protocols. The RT response time is approximately 4.8 µs dead time, providing compliance to MIL-STD-1553A/B and McAir. Additional multiprotocol features of the ACE series include fully programmable Built-In-Test (BIT) and RT Status Words.

The ACE/Mini-ACE provides a number of programmable options for RT memory management. The choice of memory management scheme is fully programmable on a transmit/receive/broadcast basis. The RT memory management options include a single message mode, a circular buffer mode to support bulk data transfers, and a double buffering mode for individual receive subaddresses to ensure data consistency. By making use of the double buffering feature, the host processor will easily be able to access the most recent, complete received block of valid Data Words for any given subaddress. In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from nonbroadcast received data.

For each transmit, receive or broadcast subaddress, either a single-message data block, a double buffered configuration (two alternating Data Word blocks), or a variable-sized (128 to 8192 words) circular buffer may be allocated for data storage. In addition to helping ensure data consistency, the circular buffer feature provides a means of greatly reducing host processor overhead for bulk data transfer applications. End-of-message interrupts may be enabled either globally, following error messages, on a Tx/Rx/Bcst-subaddress or mode code basis, or when any particular Tx/Rx/Bcst-subaddress circular buffer reaches its lower boundary. An interrupt status register allows the host processor to determine the cause of all interrupts by means of a single READ operation.

The ACE/Mini-ACE implements internal command illegalization for RT mode. The internal illegalization eliminates the need for an external

PROM, PLD or RAM device. The illegalization scheme allows for any subset of the 4096 possible combinations of broadcast/own address, $T/\overline{R}$ bit, subaddress and word count/mode code to be illegalized.

The ACE/Mini-ACE RT provides options for requesting interrupts following messages for individual mode codes as well as for storing Data Words for the various mode codes in separate RAM locations.

The ACE/Mini-ACE offers two different options for designating the Remote Terminal address. In one configuration (for BU-65170/61580/61585), the RT Address is pin programmable. Six input pins, RTAD4 through RTAD0 plus RTADP, need to be correctly strapped for RT address and odd address parity to enable RT operation. For the BU-65171, BU-61581, BU-61586, BU-61590, and BU-65620 versions of the ACE, the RT Address may be configured to be software programmable. The Mini-ACE series terminals (BU-65178/79, BU-61588, and BU-61688/89) provide the user the capability of configuring the RT address with either the pin programmable or software programmable methods.

The circular buffer feature of the ACE/Mini-ACE is enabled by setting the ENHANCED RT MEMORY MANAGEMENT bit (bit 1 of Configuration Register #2) to logic "1." If the ENHANCED RT MEMORY MANAGEMENT option is not chosen, each T/R-subaddress is mapped to a single data block by means of its

respective Lookup Table entry. In this mode, the data block for each T/R-subaddress is then repeatedly overwritten or overread.

As a programmable option, the ACE/Mini-ACE circular buffer pointers may be programmed to **not update** following the reception of invalid data blocks. This feature is enabled by setting the OVERWRITE INVALID DATA bit (bit 11) of Configuration Register #2. By so doing, retried data transmitted by the bus controller (or another RT) will automatically **overwrite** any invalid data blocks. This serves to facilitate bulk data transfers. The host processor needs only to initialize the Lookup Table Pointer, wait for a circular buffer rollover interrupt, and service the interrupt by accessing the multimessage block of valid data words. In this mode, the RT's host processor does **not** need to be concerned about servicing individual messages, retries, or errors.

Other RT options controlled by Configuration Register #2 include automatic clearing of the Service Request Status Word bit following a Transmit Vector Word mode command, and capabilities to clear and/or load the Time Tag Register following receipt of Synchronize mode commands. It should be noted that these three features, and the use of circular buffers can be used in the NON-ENHANCED mode (bit 15 of Configuration Register #3 programmed to logic "0"), as well as in the ENHANCED mode.

Many of the salient features of the ACE/Mini-ACE RT operate only in the ENHANCED mode (bit 15 in Configuration Register #3 programmed to logic "1"). In the ENHANCED mode, interrupts may be generated for individual mode commands, and separate fixed memory locations can be allocated for individual mode code Data Words (transmit and receive). The busy bit in the Status Word may set based on broadcast/valid RT address, transmit/receive bit, and subaddress. MIL-STD-1553B Notice 2 states that if the Busy bit is set it should be set for a particular subaddress only.

In the ENHANCED mode, the ACE provides RT subaddress double buffering. The RT subaddress double buffering mode allocates two 32-word data buffers to a selected subaddress. Received data is stored alternatively into each of these buffers. In many RT applications, the host processor needs to access only the data from the **latest** received message for a given subaddress. In this scenario, the use of the RT subaddress double buffer option serves to ensure data consistency by allowing the host processor to easily locate and read the most recent, consistent, valid data block received for the respective subaddress.

The ACE/Mini-ACE also provides a combined RT/Selective Monitor Mode. In this mode, all of the Advanced RT features are available, as well as a full selective message-based monitor. The selective message monitor mode allows the user to selectively monitor data based on RT address, T/R bit, and subaddress. The message monitor has separate command and data stacks.

6.2 RT MEMORY ORGANIZATION

Typical memory maps for the ACE/Mini-ACE in RT mode are illustrated in TABLE 72 and TABLE 73. As in BC mode, the two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. In addition to the Stack Pointer, for RT mode there are several other areas of the shared RAM address space that are designated as fixed locations. These are for the Area A and Area B Lookup Tables, the Illegalization lookup table, the Busy lookup table, and the mode code data tables.

The RT Lookup tables, which provide a mechanism for mapping data blocks for individual Tx/Rx/Bcst-subaddresses to areas in the RAM, are located in address range 0140 to 01BF for Area A and address range 01C0 to 023F for Area B. The RT lookup tables include Subaddress Control Words as well as the individual Data Block Pointers. If used, address range 0300-03FF is dedicated as the illegalizing section of RAM. The actual Stack RAM area, as well as the individual data blocks, may be located in any of the non-fixed areas in the shared RAM address space.

TABLE 72 illustrates the typical memory map for the case in which the enhanced mode RT features are **not** used. In this instance, address locations 0280-03FF (hex) may be used for storage of Stack Data or Message Data Blocks.

TABLE 73 illustrates the RT memory map for the case where the advanced RT features are used.

TABLE 72. TYPICAL RT MEMORY MAP (Without ENHANCED MODE features)

ADDRESS(HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0104	Stack Pointer B (fixed location)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-025F	Data Block 0
0260-027F	Data Block 1
0280-029F	Data Block 2
02A0-02BF	Data Block 3
02C0-02DF	Data Block 4
02E0-02FF	Data Table 5
0300-03FF	Command Illegalization Table
0400-041F	Data Block 6
• • •	• • •
0EE0-0EFF	Data Block 93
0F00-0FFF	Stack B

TABLE 73. TYPICAL RT MEMORY MAP (With ENHANCED MODE features)	
ADDRESS(HEX)	**DESCRIPTION**
0000-00FF	Stack A
0100	RT Command Stack Pointer A (fixed location)
0101-0103	RESERVED
0104	RT Command Stack Pointer B (fixed location)
0105-0107	RESERVED
0108-010F	Mode Code Selective Interrupt Table (fixed area)
0110-013F	Mode Code data (fixed area)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-0247	Busy Bit Lookup Table (fixed area)
0248-025F	(not used)
0260-027F	Data Block 0
0280-029F	Data Block 1
• •	• •
02E0-02FF	Data Block 4
0300-03FF	Command Illegalizing Table (fixed area)
0400-041F	Data Block 5
0420-043F	Data Block 6
• • •	• • •
0FE0-0FFF	Data Block 100

Note that in TABLE 73, the memory map shown for the RT ENHANCED mode (unlike the non-Enhanced mode), there is no area allocated for "Stack B." This is shown for purpose of illustration.

It should be noted that the global double buffering feature **may still be used** in conjunction with the Enhanced RT mode. However, in the Enhanced mode, it is strongly recommended that the Subaddress Double Buffering feature, rather than the "global" double buffering feature (Area A/Area B) be used as a more efficient means of ensuring data sample consistency.

Also, note that in TABLE 73, the allocated area for the RT command stack is 256 words. However, in the ENHANCED MODE, larger stack sizes are possible. In this mode, the RT Command Stack size is programmable for 256 words (64 messages), 512, 1024, or 2048 words (512 messages) by means of bits 14 and 13 of Configuration register #3. Refer to TABLE 74.

TABLE 74. RT COMMAND STACK SIZE		
BIT 14 BC/RT CMD STACK SIZE 1	**BIT 13 BC/RT CMD STACK SIZE 2**	**BC/RT STACK SIZE (WORDS)**
0	0	256 (64 messages)
0	1	512 (128 messages)
1	0	1024 (256 messages)
1	1	2048 (512 messages)

6.3 RT MEMORY MANAGEMENT

In order to comply with Notice 2 of MIL-STD-1553B and to better support bulk data transfers, the ACE/Mini-ACE provides enhanced RT memory management capabilities. These features allow broadcast message data to be separated from nonbroadcast receive data, help to ensure data consistency for transmitted and received data blocks, and generally serve to off-load the host processor for real-time applications.

Active Area Double Buffering. The ACE/Mini-ACE provides a global double buffering mechanism by means of bit 13, CURRENT AREA $\overline{A}$/B, of Configuration Register #1. At any point in time, this allows for one stack pointer, stack area, lookup table, and set of data blocks to be designated as \"active\" (used for the processing of 1553 messages) and the alternate set of respective data structures to be designated as \"nonactive.\"

Both the "active" and "nonactive" RAM areas are **always accessible** by the host processor.

TABLE 75 illustrates the RT Lookup tables. Within each lookup table, 32 locations provide optional separation of broadcast messages. The last 32 words of each table are Subaddress Control Words, one appropriated for each RT subaddress.

TABLE 75. RT LOOKUP TABLES			
AREA A	**AREA B**	**DESCRIPTION**	**COMMENT**
0140 • • • 015F	01C0 • • • 01DF	Rx(/Bcst) SA0 • • • Rx(/Bcst) SA31	Receive (/Broadcast) Lookup Pointer Table
0160 • • • 017F	01E0 • • • 01FF	Tx SA0 • • • Tx SA31	Transmit Lookup Pointer Table
0180 • • • 019F	0200 • • • 021F	Bcst SA0 • • • Bcst SA31	Broadcast Lookup Pointer Table (Optional)
01A0 • • • 01BF	0220 • • • 023F	SACW SA0 • • • SACW SA31	Subaddress Control Word Table (Optional)

6.3.1 Subaddress Control Word

In the Enhanced RT Memory Management mode, each of the 32 Subaddress Control Words specify the memory management and interrupt schemes for the respective subaddress. For each Subaddress Control Word, five bits control the memory management scheme and interrupts for each of transmit, receive, and broadcast messages. In addition, bit 15 (MSB) may be used to enable subaddress double buffering for receive (and/or broadcast receive) subaddresses. Refer to TABLE 76 and TABLE 77 for a summary of bit functions.

For each transmit (or receive or broadcast) subaddress, three bits are used to specify the memory management scheme. For each Rx(/Bcst) subaddress, the memory management scheme may be selected from among the single message mode (as in the nonenhanced mode), the circular buffer mode, or the double buffered mode. For each transmit subaddress, the memory management scheme may be selected from among the single message mode or the circular buffer mode. Note that the double buffered mode **is not applicable** for transmit subaddresses.

It should be noted that for mode code messages, the Subaddress Control Word is only applicable if ENHANCED MODE CODE HANDLING **is <u>disabled</u>.** ENHANCED MODE CODE HANDLING is disabled in the non-ENHANCED mode **or** if bit 0 of Configuration Register #3 is logic "0." ENHANCED MODE CODE HANDLING is enabled in the ENHANCED MODE by setting bit 0 of Configuration Register #3 to logic "1."

In the single buffer mode, a single data block is repeatedly overread (for transmit data) or overwritten (for receive or broadcast data). Alternatively, in the circular buffer mode, Data Words for successive messages to/from any particular Tx/Rx/Bcst subaddresses are read from or written to the **next** contiguous block of locations in the respective circular buffer.

The size of the circular buffer for each transmit, receive, or broadcast subaddress may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words. For each Tx/Rx/Bcst subaddress, two bits of the subaddress control word are used to enable interrupts. One of these bits will result in an interrupt following **every** message directed to the specific Tx/Rx/Bcst subaddress. The other of these two bits will result in an interrupt at the end of a message if the message resulted in the Lookup table pointer for the respective Tx/Rx/Bcst-subaddress crossing the lower boundary of the circular buffer, rolling over to the top of the buffer.

In the subaddress double buffered mode, a pair of 32-word data blocks are allocated for a particular receive (and/or broadcast receive) subaddress. In this mode, successive messages received to the subaddress are stored in alternating data blocks.

TABLE 76. SUBADDRESS CONTROL WORD BIT MAP (READ/WRITE 04h)

BIT	DESCRIPTION
15(MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

TABLE 77. SUBADDRESS CONTROL WORD Memory Management Subaddress Buffer Scheme					
RX DOUBLE BUFFERED ENABLED (SEE NOTES)	**MM2**	**MM1**	**MM0**	**DESCRIPTION**	**COMMENT**
0	0	0	0	Single Message	
1	0	0	0	For Receive or Broadcast: Double Buffered For Transmit: Single Message	
X	0	0	1	128-Word	Circular Buffer of Specified Size
X	0	1	0	256-Word	
X	0	1	1	512-Word	
X	1	0	0	1024-Word	
X	1	0	1	2048-Word	
X	1	1	0	4096-Word	
X	1	1	1	8192-Word	

Notes: To utilize subaddress double buffering, the ACE/Min-ACE must be programmed to ENHANCED MODE (bit 15 of Configuration Register #3 must be logic "1"). It is recommended that a value of 0 be used for X to ensure compatibility with future versions.

In order to select subaddress double buffering by means of the Subaddress Control Word, the RX SUBADDRESS DOUBLE BUFFERING ENABLE bit (bit 13) **and** the ENHANCED RT MEMORY MANAGEMENT bit (bit 1) of Configuration Register #2 must be programmed to logic "1."

If the ACE is in ENHANCED MODE **and** RX SUBADDRESS DOUBLE BUFFERING ENABLE is logic "1" **and** ENHANCED RT MEMORY MANAGEMENT is logic "0," the subaddress double buffering mode will be used for **ALL** receive (and broadcast) subaddresses.

6.3.2 Single Message Mode

If bit 1 of Configuration Register #2 is logic "0," the ACE/Mini-ACE memory management scheme assumes its default or non-enhanced mode. In the non-enhanced RT operation, the single message memory management mode is used for **all** receive, transmit, or broadcast subaddresses. It should be noted, that under the enhanced RT memory management scheme, the single message mode may still be used for individual receive, transmit and/or broadcast subaddresses. This is the case if the SUBADDRESS RX DOUBLE BUFFERING bit (bit 15) **and** the three applicable "memory management" bits in the respective Subaddress Control Word are logic "0."

The operation of the single message RT mode is illustrated in FIGURE 10. In the single message mode, the respective Lookup Table entry must be loaded by the host processor. At the start of each message, the lookup table entry is stored in the third address location of the respective

message block descriptor in the stack area of RAM. Received Data Words are written to or transmitted Data Words are read from the Data Word Block referenced by the lookup table pointer. In the single message mode, the current lookup table pointer **is not** written to by the ACE/Mini-ACE memory management logic at the end of a message. Therefore, if a subsequent message is received for the same subaddress, the **same** Data Word block will be overwritten or overread.

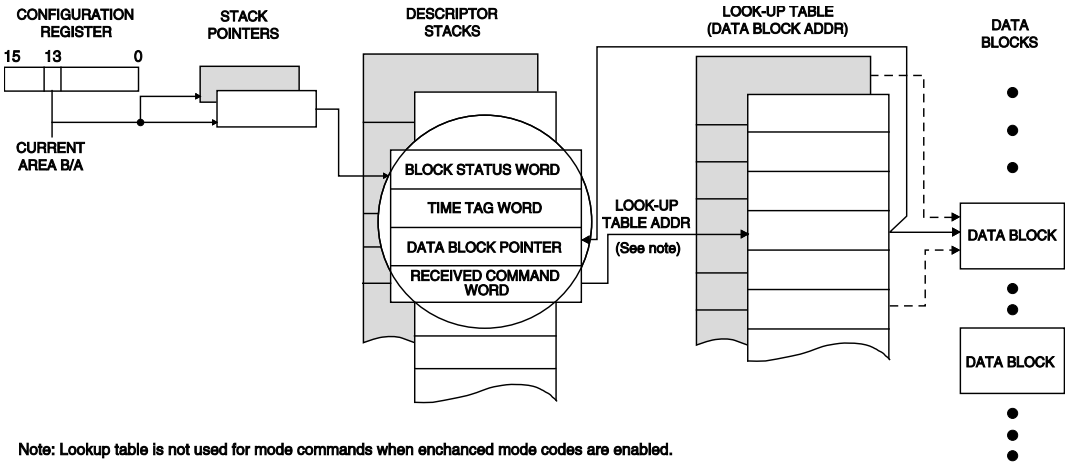


FIGURE 10. RT MEMORY MANAGEMENT, SINGLE-MESSAGE MODE

6.3.3 256-Word Boundaries

The programming of bit 10 of Configuration Register # 2, 256-WORD BOUNDARY DISABLE, must be considered for both the default memory management mode (bit 1 of Configuration Register # 2 = 0) or for any Tx/Rx/Bcst subaddresses in the enhanced mode (bit 1 of Configuration Register # 2 = logic "1"), using the single message mode. If 256-WORD BOUNDARY DISABLE is logic 0, the operation of the address counter for accessing RT Data Word Blocks for the single buffer mode will observe 256-word boundaries in the ACE/Mini-ACE shared RAM address space. That is, if 256-WORD BOUNDARY DISABLE is logic 0, the internal Data Word address pointer will roll over from XXFF to XX00 (hex), rather than increment to (XX+1)00.

If the 256-WORD BOUNDARY DISABLE bit is set to logic "1" however, the ACE/Mini-ACE address counter **will not** roll over at 256-word boundaries. In this instance, the Data Word addresses are generated from the output of a **16-bit** counter, rather than an 8-bit counter. That is, the address counter will increment from XXFF to (XX + 1)00, rather than roll back to XX00.

6.3.4 RT Subaddress Double Buffering Mode

The ACE/Mini-ACE provides a double buffering mechanism for **received** data, that is optionally selectable on a subaddress basis for all receive (and/or broadcast) subaddresses. It should be noted that the Subaddress Double Buffering mode is applicable for receive data only, **not for transmit data**. Double buffering of transmit messages may be easily implemented by software techniques.

The purpose of the double buffering mode is to provide the host processor with the highest possible degree of data consistency. This is accomplished by allocating **two** 32-word data word blocks for each individual receive (and/or broadcast receive) subaddress. One of the blocks will be designated as the active 1553 block while the other will be considered inactive. The data accompanying the next receive command to that subaddress will be stored in the active block. Upon completion of the message, provided that the message was valid and Receive Double Buffering is enabled, the ACE/Mini-ACE will automatically switch the active and inactive blocks for that subaddress. This means that the latest, valid, complete data block is always readily available to the host processor.

The subaddress double buffer mode is available only in the ENHANCED MODE (bit 15 in Configuration #3 set). If the ENHANCED RT MEMORY MANAGEMENT ENABLE bit (bit 1 in Configuration Register #2) is programmed to logic "0," then the selective double buffer mode is enabled by simply setting the DOUBLE BUFFER ENABLE bit (bit 12 in Configuration Register #2) to logic "1." In this case (global double

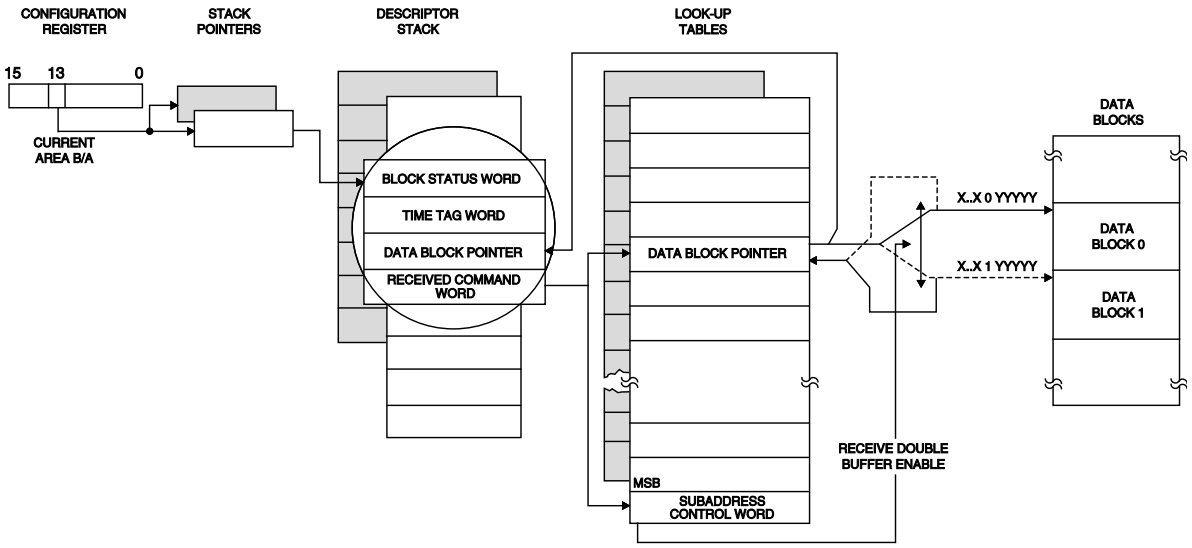
buffering), double buffering is enabled for **all** receive subaddresses (and all broadcast receive subaddresses if broadcast separation is enabled).

If ENHANCED RT MEMORY MANAGEMENT ENABLE bit is programmed to logic "1," then the double buffer mode is enabled **for selected subaddresses** by setting the DOUBLE BUFFER ENABLE bit (bit 12 in Configuration Register #2) to logic "1" **and** by the programming of the desired Subaddress Control Words. The Subaddress Control word must be programmed for receive single message mode (RX:MM2-0 (bits 7-5) set to logic "0") **and** the DOUBLE BUFFER ENABLE bit (bit 15) must be programmed to logic "1." If SEPARATE BROADCAST is enabled (bit 0 in Configuration Register #2 is set to logic "1"), then the broadcast memory management scheme should also be set to single message mode (RX:MM2-0 (bits 2-0) programmed to logic "0") if double buffering of broadcast receive commands is desired. Reference TABLE 78.

The software algorithm for reading the latest data block is to first disable double buffering for the desired subaddress. If ENHANCED RT MEMORY MANAGEMENT is not enabled (bit 1 of Configuration Register #2 programmed to logic "0"), double buffering must be disabled **FOR ALL SUBADDRESSES by setting RECEIVE SUBADDRESS DOUBLE BUFFERING ENABLE (bit 12 in Configuration Register #2) to logic "0."**

If ENHANCED RT MEMORY MANAGEMENT is enabled (the STRONGLY RECOMMENDED implementation), double buffering can be disabled on a subaddress basis by programming the DOUBLE BUFFER ENABLE bit (bit 15) of the appropriate Subaddress Control Word to logic "0." The host processor should then read the current value of the data block pointer in the lookup table. This pointer references the active Data Word block. The last consistent data block can be accessed in the **inactive** block by inverting bit 5 of the current data block pointer. The current lookup table entry should **not** be modified.

After reading the data block, the host processor should re-enable double buffering by setting the RX DOUBLE BUFFER ENABLE bit (if ENHANCED MEMORY MANAGEMENT is not enabled) or by setting the RX DOUBLE BUFFER ENABLE bit (bit 15) in the appropriate Subaddress Control Word to logic "1" (if ENHANCED MEMORY MANAGEMENT is enabled).



WARNING: Where user cannot guarantee to service a message before a second message to the same Subaddress is completed, it may be necessary to manually 'flip' the pointer before re-enabling Double Buffering after checking the Descriptor Stack for activity.

NOTE: Double Buffering is best suited to data types where messages are received at a high rate but only read occasionally, with un-read messages discarded (eg. Millisecond time update read only once per second). Otherwise Circular Buffering is more desirable.

FIGURE 11. RT MEMORY MANAGEMENT-SUBADDRESS DOUBLE BUFFERING MODE

6.3.5 Circular Buffer Mode

In the ENHANCED RT MEMORY MANAGEMENT mode, individual transmit, receive, and broadcast subaddresses may be programmed for either the single message or circular buffer modes.

The operation of the circular buffer RT memory management mode is illustrated in FIGURE 12. As in the single message mode, the individual Lookup Table entries are initially loaded by the host processor. At the start of each message, the Lookup Table entry is stored in the third position of the respective message block descriptor in the stack area of RAM. Receive or Transmit Data Words are transferred to/from the circular buffer, starting at the location referenced by the Lookup Table pointer. If the OVERWRITE INVALID DATA bit (bit 11) of Configuration Register #2 is logic "0," the location **after** the last word accessed for the message is stored into the respective Lookup Table location, **regardless of whether or not there were any errors in the just completed message.** By so doing, data for the **next** message for the respective Tx/Rx/Bcst subaddress will be accessed to/from the next lower contiguous block of locations in the circular buffer.

If the OVERWRITE INVALID DATA bit (bit 11) of Configuration Register #2 is logic "1," the location **after** the last word accessed for the message

is stored in the respective Lookup Table location **only following a valid received (or transmitted) message**. Assuming that the value of the Lookup Table pointer is updated, data for the **next** message for the respective Tx/Rx/Bcst subaddress will be accessed to/from the next contiguous block of locations in the circular buffer. Assuming the OVERWRITE INVALID DATA bit is logic "1," the Lookup Table pointer will **not** be updated at the end of the message if there was an error in the message. This allows failed messages in a bulk data transfer to be retried without disturbing the circular buffer data structure, and without intervention by the RT's host processor.

Note: *It is strongly recommended that OVERWRITE INVALID DATA be programmed to logic "1" when using the circular buffer mode.*

When the pointer reaches the lower boundary of the circular buffer (located at 128, 256, . . . 8192-word “modulo address” boundaries in the shared RAM address space), the pointer rolls back to the top boundary of the circular buffer, as shown in FIGURE 12. It should be noted that the pointer to the start of the RT Data Word block is stored in the third location of the message block descriptor (in the stack) for the single buffer mode as well as for the circular buffer mode.



Note : *Regarding “modulo address” boundaries in the shared RAM address space. If the circular buffer size is set to 1024 words it “Rolls-Over” at modulo 1024 increments. Whatever size selected for the circular buffer (128, 256, 512, 1024, 2048, 4096, 8192) will cause a “Roll-Over” at that respective modulo.*

To make best use of the circular buffer feature, the OVERWRITE INVALID DATA bit (bit 11 of Configuration Register #2) **and** RX: CIRCULAR BUFFER ROLLOVER bit (bit 8) in the Subaddress Control Word should be programmed to logic "1." The host processor need initialize the circular buffer lookup table pointer, and then wait for the circular buffer rollover interrupt. After this interrupt occurs, the CPU may then read the contiguous, multimessage block of valid, received Data Words from the shared RAM. Use of the RT circular buffer feature eliminates the need for the CPU to service individual messages, or be concerned with message errors or retries.

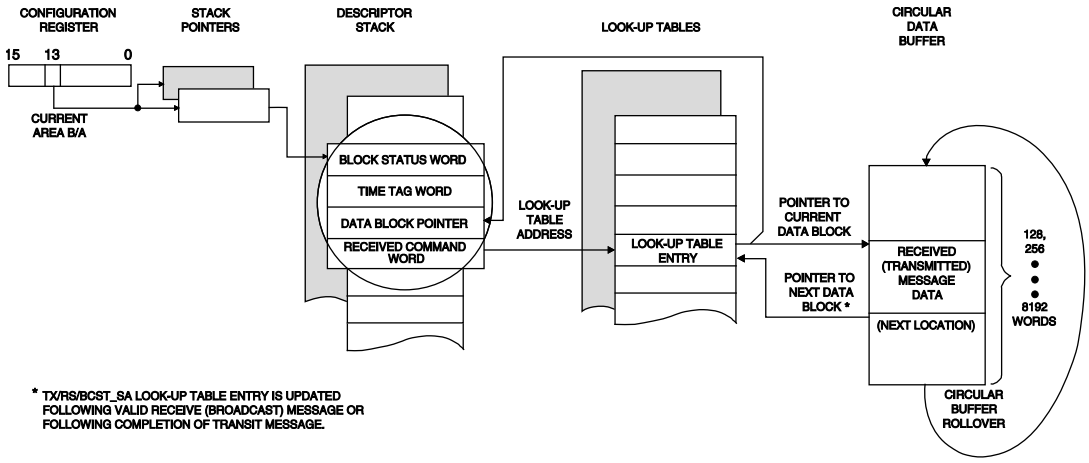


FIGURE 12. RT MEMORY MANAGEMENT - CIRCULAR BUFFER MODE

TABLE 78 summarizes the programming of configuration register bits required to enable the various ACE/Mini-ACE RT memory management features.

TABLE 78. BITS USED TO ENABLE RT MEMORY MANAGEMENT FEATURES

FEATURE	SUBADDRESS DOUBLE BUFFER ENABLE (BIT 12 OF CONFIGURATION REGISTER # 2)	OVERWRITE INVALID DATA (CONFIGURATION REGISTER # 2, BIT 11)	ENHANCED RT MEMORY MANAGEMENT (CONFIGURATION REGISTER #2, BIT 1)	SEPARATE BROADCAST (CONFIGURATION REGISTER #2, BIT 0)	ENHANCED MODE ENABLED (CONFIGURATION REGISTER #3, BIT 15)
Default (power turn-on) Mode: Single Message for ALL Tx/Rx/Bcst Subaddresses	0	0	0	0	0
Single Message mode for all transmit subaddresses; Double Buffering for ALL receive (and broadcast) subaddresses	1 (See Note)	0	0	X	1 (See Note)
Broadcast Separation	X	X	X	1	X
Enable circular buffers for individual subaddresses; NOT overwriting invalid data	X	0	1	X	X
Enable circular buffers for individual subaddresses; WITH overwriting invalid data	X	1	1	X	X
Enable subaddress double buffering for individual receive (and broadcast) subaddresses	1 (See Note)	X	1	X	1 (See Note)

Note: In order to enable the subaddress double buffering mode, ENHANCED MODE (bit 15 of Configuration Register #3) must be programmed to logic "1" **before** SUBADDRESS DOUBLE BUFFERING ENABLED (bit 12 of Configuration Register #2) is written as logic "1."

6.4 RT STACK AND INTERRUPTS

In RT mode, the Stack area of RAM contains a real-time chronology of all messages processed by the ACE/Mini-ACE. Similar to BC mode, there is a four word block descriptor in the Stack for each message processed. The four entries to each block descriptor are the Block Status Word, Time Tag Word, the pointer to the start of the data block, and the 16-bit received Command Word. Prior to the processing of messages, the host processor should initialize the Stack Pointer. In some applications, it may also prove helpful to "zero out" the Stack area prior to receiving messages.

In RT mode, the host processor may determine that a message has been processed either by means of interrupts or by polling the Interrupt Status Register or the active area Stack Pointer memory location. The RT Command Stack Pointer increments by four (modulo the stack size) at the start of each message processed. After a message is received, the host CPU should read the Block Status Word, Time Tag, data block starting address, and Command Word received from the Message Block Descriptor in the Stack. Assuming a valid message was received, it may then read the received Data Words from the referenced Data Word block.

RT Block Status Word. The bit map and bit definitions for the RT Block Status Word are indicated below.

TABLE 79. RT MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

END-OF-MESSAGE (EOM): Set at the completion of an RT message, regardless of whether or not there were any errors in the message.

START-OF-MESSAGE (SOM): Set approximately 3-4 µs following the receipt (mid-parity bit) of the Command Word and cleared at the end of the message.

CHANNEL B/$\overline{A}$: This bit will be low if the message was processed on Channel A or high if the message was processed on Channel B.

ERROR FLAG: If this bit is logic "1," and one or more of bits 10, 9, and/or 8 are logic "1," this indicates one or more of the following errors have occurred in the message: Format Error Response Timeout and/or Loop Test Fail.

If this bit is logic "1," the ACE/Mini-ACE is configured for its transparent mode of processor interface, and bits 11 through 8 are all logic "0," this indicates that a handshake failure has occurred. A handshake failure occurs when the input signal $\overline{\text{DTGRT}}$ is either not asserted low or is asserted low too late after the time that the output signal $\overline{\text{DTREQ}}$ is asserted low. A handshake failure also occurs if the CPU transfer control input $\overline{\text{STRBD}}$ is asserted for too long after the ACE/Mini-ACE's $\overline{\text{READYD}}$ output has been asserted (low). If a handshake failure occurs, a message should be considered invalid. The allotted time for the CPU providing the $\overline{\text{DTGRT}}$ signal or clearing the $\overline{\text{STRBD}}$ input is 4.0 µs when using a 16 MHz clock, or 3.5 µs when using a 12 MHz clock.

RT-to-RT FORMAT: Applicable for ENHANCED MODE only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1"). This bit will be set if the ACE is the **receiving** RT in an RT-to-RT transfer. Note that this bit will **not** be set if the ACE is the **transmitting** RT for an RT-to-RT transfer.

FORMAT ERROR: If set, indicates that the received portion of a message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.). This bit is a summation of bits 5, 4, 3, 2, 1, and 0.

RESPONSE TIMEOUT: If set, indicates that the ACE/Mini-ACE was the receiving RT for an RT-to-RT transfer **and** that the transmitting RT has either not responded or has responded later than the programmed value for the No Response Timeout time. The ACE/Mini-ACE's RT-to-RT No Response Timeout Time is defined as the time from the mid-bit crossing of the parity bit of the Transmit Command Word to the mid-sync crossing of the RT Status Word. In the nonenhanced mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "0"), the value of the BC Response Timeout is 17.5 to 19.5 µs. If ENHANCED MODE ENABLED is logic 1, the value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 µs (±1 µs) by means of bits 10 and 9 of Configuration Register #5.

LOOP TEST FAIL: A loopback test is performed on the transmitted portion of every nonbroadcast message in RT mode. A validity check is performed on the received version of every word transmitted by the ACE/Mini-ACE RT. In addition, a bit-by-bit comparison is performed on the last word transmitted by the RT for each message. If either the

received version of any transmitted word is determined to be invalid (sync, encoding, bit count, and/or parity error) and/or the received version of the last transmitted word does not match the transmitted version, the LOOP TEST FAIL bit will be set.

CIRCULAR BUFFER ROLLOVER: Applicable for ENHANCED MODE only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1") **and** if ENHANCED RT MEMORY MANAGEMENT is enabled (bit 1 of Configuration Register # 2 is set to logic "1") **and** the circular buffer option is enabled for the Bcst/Tx/Rx-subaddress for the current message, by means of the Subaddress Control Word. This bit will be set if the lookup table address pointer crossed the upper boundary of its circular buffer, resulting in a rollover. If OVERWRITE INVALID DATA is enabled (bit 11 of Configuration Register #2 set to logic "1"), this bit will only be set following completion of a transmit message or a **valid** receive message that resulted in a rollover. If OVERWRITE INVALID DATA is disabled (bit 11 of Configuration Register #2 set to logic "0"), this bit will be set when a rollover occurs, independent of message validity.



Note: *It should be noted that in the non-ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register # 3, is logic "0"), bits 7 through 0 will always be logic "0."*

ILLEGAL COMMAND WORD: Applicable for Enhanced Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, programmed to logic "1"). If this bit is set, it indicates that the message has been illegalized. A message is illegalized if (ENHANCE MODE ENABLE, bit 15 of Configuration Register #3 is logic "0" **or** ILLEGALIZATION DISABLE, bit 7 of Configuration Register #3 is logic "0") **and** the appropriate bit for the respective Broadcast-Tx/Rx-Subaddress-Word Count/Mode Code combination is set in the illegalization table, address locations 0300-03FF in the shared RAM.

WORD COUNT ERROR: Applicable for Enhanced Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, programmed to logic "1"). If set, indicates that the BC did not transmit the correct number of Data Words.

INCORRECT DATA SYNC: Applicable for Enhanced Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, programmed to logic "1"). If set, indicates that the BC transmitted a Command sync in a Data Word.

INVALID WORD: Applicable for Enhanced Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, programmed to logic "1"). Indicates the BC (or transmitting RT in an RT-to-RT transfer) transmitted with one or more words containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

RT-to-RT GAP/SYNC/ADDRESS ERROR: Applicable for Enhanced Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1"). This bit is set if the ACE RT is the receiving RT for an RT-to-RT transfer and one or more of the following occur: (1) If the GAP CHECK ENABLED bit (bit 8) of Configuration Register #5 is set to logic "1" and the transmitting RT responds with a response time of less than 4 µs, per MIL-STD-1553B (mid-parity bit to mid-sync); i.e., less than 2 µs dead time; and/or (2) There is an incorrect sync type or format error (encoding, bit count, and/or parity error) in the transmitting RT Status Word; and/or (3) The RT address field of the transmitting RT Status Word does not match the RT address in the transmit Command Word.

RT-to-RT SECOND COMMAND ERROR: Applicable for Enhanced Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, programmed to logic "1"). If the ACE/Mini-ACE is the receiving RT for an RT-to-RT transfer, this bit set indicates one or more of the following error conditions in the transmit Command Word: (1) $T/\overline{R}$ bit = logic "0"; (2) subaddress = 00000 or 11111; and/or (3) same RT Address field as the receive Command Word.

COMMAND WORD CONTENTS ERROR: Applicable for Enhanced Mode only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, programmed to logic "1"). Indicates a received command word is not defined in accordance with MIL-STD-1553B. This includes the following undefined Command Words: (1) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** the Command Word is a nonmode code, broadcast, transmit command; (2) The OVERRIDE MODE $T/\overline{R}$ ERROR bit, bit 6 of Configuration Register #3, is logic "0" **and** a message with a $T/\overline{R}$ bit of "0," a subaddress/mode field of 00000 or 11111 and a mode code field between 00000 and 01111; (3) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** a mode code command that is not permitted to be broadcast (e.g.. Transmit status) is sent to the broadcast address (11111).

6.4.1 Time Tag Word

The Time Tag Word, the second location of the message block descriptor in the RT Command Stack, is updated (written) during both the Start-of-Message (SOM) and End-of-Message (EOM) sequences. The SOM sequence occurs immediately after reception of a valid Command Word to the RT's address or the broadcast address. The EOM sequence occurs approximately 3 to 4 µs after the last word transmitted or received in a message.

During these sequences, the current value of the ACE/Mini-ACE's internal read/writable Time Tag Register (register address 05) is written to the respective RAM location. The resolution of the Time Tag counter is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB, or an externally provided clock, by means of bits 9, 8, and 7 of Configuration Register #2.

The value of the Time Tag Register will roll over from FFFF (hex) to 0000 after every 65,536 counts (LSB times). When the rollover occurs, a TIME TAG ROLLOVER interrupt request will occur, if enabled by means of the Interrupt Status Register. In addition, the TIME TAG ROLLOVER bit in the Interrupt Status Register will become set following the rollover if (1) the interrupt is enabled, or (2) ENHANCED INTERRUPTS are enabled (ENHANCED MODE **and** bit 15 of Configuration Register #2 is programmed to logic "1").

If CLEAR TIME TAG ON SYNCHRONIZE, bit 6 of Configuration Register #2, is programmed to logic "1," the value of the ACE RT Time Tag Register will be cleared to 0000 following receipt of a Synchronize (without data) mode command. If LOAD TIME TAG ON SYNCHRONIZE, bit 5 of Configuration Register #2, is programmed to logic "1," the value of the received Data Word will be loaded into the ACE/Mini-ACE RT Time Tag Register following receipt of a valid Synchronize with data mode command and the accompanying Data Word.

6.4.2 Data Block Pointer or Mode Data Word

The third word location within the RT message descriptor is used for two different purposes. For nonmode code messages, or for mode code messages with ENHANCED MODE CODE HANDLING disabled (bit 15 **or** bit 0 of Configuration Register #3 programmed to logic "0"), the value read from the RT lookup table is stored in this location. This value indicates the starting location of the Data Word block for the respective message.

For mode code messages with data **and** ENHANCED MODE CODE HANDLING enabled (bit 15 **and** bit 0 of Configuration Register #3 programmed to logic "1"), the Data Word that is transmitted or received for a mode code message with data is written to this location during the RT End-of-Message (EOM) sequence.

For mode code messages without data, **no word** is written to the third location of the message block descriptor.

6.4.3 Command Word Received

For all messages, the received Command Word is stored in the fourth location in the message block descriptor during the RT Start-of-Message (SOM) sequence.

6.4.4 Superseding Commands

A superseded message sequence occurs when a valid message begins on one bus, followed by a time gap, followed by a new command on the alternate bus. If both the old and the new command are to the same RT Address, the RT **must** stop processing the first command, and begin processing the new command. If the commands are to different RT

Addresses, the terminal responding to the first command **must** complete processing the message and ignore the activity on the alternate bus.

The ACE/Mini-ACE RT will abort processing the first message and begin processing the new message. The only exception to this is when the ACE/Mini-ACE is operating in the combined RT/Selective Message and the first command is to the ACE/Mini-ACE's RT Address **and** the second command is to different, nonbroadcast, RT Address. As an RT, the ACE/Mini-ACE must continue processing the first command (in compliance with MIL-STD-1553), and ignore the new command to a different terminal on the alternate bus.

The ACE/Mini-ACE selective message monitor will supersede a message on the same bus except when the superseding command may be interpreted as a status word. Hence, a RT status response with the wrong RT address in the status word will NOT appear to the ACE/Mini-ACE selective message monitor as a new command, but rather will appear to be a bad status word.

When a message is superseded, a normal Start Of Message (SOM) sequence is performed on the new (superseding) message. Note that an End Of Message (EOM) sequence is NOT executed on the original (superseded) message. This will result in a command stack entry with the Start Of Message (SOM) bit in the block status word set to logic "1" and the End Of Message (EOM) bit set to logic "0." The host processor can distinguish between a message in progress and a superseded message by the value of the monitor command stack pointer. If the monitor command stack pointer has incremented beyond the command stack entry in question and the block status word indicates an SOM state, then the message must have been superseded.

6.5 RT INTERRUPTS

The ACE/Mini-ACE offers a great deal of flexibility in terms of RT interrupt processing. In some systems, the transmission or reception of a message with a particular subaddress denotes the end of a complete set of consistent data. In this instance, the user should use the RT SUBADDRESS CONTROL WORD INTERRUPT in order to issue an interrupt request **only for a particular T/R-subaddress**, rather than following every message. One technique would then be for the host processor to switch the active area of shared RAM, by toggling bit 13 of Configuration Register #1 at this time.

An interrupt request for a circular buffer rollover condition (if enabled) will occur only **following the end** of a transmit message during which the last location in the circular buffer has been read **or** following the end of a **valid** receive or broadcast message in which the last location in the circular buffer has been written to.

If ENHANCED MODE CODES are enabled (ENHANCED MODE **and** bit 0 of Configuration Register #3 is logic "1"), interrupts may be enabled following receipt of specific mode code messages. These interrupts may be enabled by means of the Mode Code Selective Interrupt Table, address locations 0108-010F in the shared RAM.

6.6 IMPLEMENTING BULK DATA TRANSFERS

In systems involving bulk data transfers over the 1553 bus to/from the same subaddress, the host CPU should set the OVERWRITE INVALID DATA bit (bit 11) of Configuration Register #2 and enable the RT CIRCULAR BUFFER ROLLOVER interrupt request. By so doing, the routine transfer of multiple messages to the selected subaddress, **including errors and retries,** is transparent to the host processor. The ACE/Mini-ACE will issue an interrupt request only after it has received the anticipated number of valid data words to the particular subaddress. The anticipated number of words to be received (or transmitted) is programmable up to 8192 words.

6.7 RT COMMAND ILLEGALIZATION

The ACE/Mini-ACE provides an internal mechanism for RT Command Word illegalizing. The scheme utilizes a 256-word area in the ACE/Mini-ACE shared RAM space. A benefit of this feature is reduced P.C. board space requirements, by eliminating the need for an external PROM, PLD, or RAM device to perform the illegalizing function. The ACE/Mini-ACE illegalization scheme provides the maximum in flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, $T/\overline{R}$ bit, subaddress, and word count/mode code to be illegalized.

Another advantage of the RAM-based illegalizing technique is that it provides self-testability.

For the BU-65170/71/78/79, BU-61580/81/85/86/88, BU-61590, and BU-61688/89, the power turn-on default condition is for RT command illegalization to be **enabled.** For the BU-65620, the default for illegalization is "enabled" if the pin ILLENA is connected to logic "1." For the BU-65620, illegalization is **disabled** (cannot be enabled) if ILLENA is connected to logic "0." For any of the ACE products, command illegalization may be disabled by first setting bit 15 of Configuration Register #3, ENHANCED MODE, to logic "1" and then setting bit 7 of Configuration Register #3, ILLEGALIZATION DISABLED (while rewriting bit 15, ENHANCED MODE ENABLED, to logic "1"), to logic "1."

If command illegalization is used, address locations 0300 through 03FF are dedicated for the message illegalizing function and **must not** be used for Stack or Data Block storage. If RT command illegalization is disabled, the ACE/Mini-ACE assumes that all valid, defined, received Command Words are legal. If the illegalization option is disabled, address locations 0300 through 03FF may be used for the storage of the Descriptor Stack or Data Blocks.

It should be noted that the state of the ILLEGALIZATION DISABLED bit in Configuration Register #3 has **no effect** for Bus Controller (BC) or Monitor (MT) modes.

The ACE/Mini-ACE shared RAM allocates 256 words, address locations 0300 to 03FF (hex), for RT command illegalization. Broadcast commands are illegalized separately from nonbroadcast commands.

Commands may be illegalized down to the word count level. For example, a one-word receive command to subaddress 1 may be legal, while a two-word receive command to subaddress 1 may be illegalized.

6.7.1 Effects of Illegalization

If the ACE/Mini-ACE RT protocol logic determines that a nonbroadcast message has been illegalized, the ACE/Mini-ACE will respond with the Message Error bit set in the RT Status Word. If a transmit command has been illegalized, the ACE/Mini-ACE will respond with its Status Word with the Message Error bit set; **no** Data Words will be transmitted.

If a receive command has been illegalized and the ACE/Mini-ACE is in non-ENHANCED mode **or** bit 4 of Configuration Register #3, ILLEGAL RECEIVE TRANSFER DISABLE is programmed to logic "0," Data Words received in a BC-to-RT (or RT-to-RT) transfer will be stored to the shared RAM. However, if the ACE/Mini-ACE is in ENHANCED MODE **and**

ILLEGAL RECEIVE TRANSFER DISABLE is programmed TO logic "1," received data words **will not** be stored to RAM.

In the case of an illegalized broadcast command, the ACE/Mini-ACE will not respond, but will set the Message Error and Broadcast Command Received bits in its internal RT Status Register. If the next message is a Transmit status or Transmit last command mode code, the ACE/Mini-ACE RT will then respond with the Message Error bit set to logic "1." For a broadcast receive command, the storage or non-storage of Data Words is controlled by the ILLEGAL RECEIVE TRANSFER DISABLE bit, as described above.

If the ACE/Mini-ACE RT is programmed for the ENHANCED MODE (bit 15 of Configuration Register #3 programmed to logic "1"), ILLEGAL COMMAND WORD, bit 6 of the RT Block Status Word, will be set to logic "1" when the Block Status Word is written to the message block descriptor in the Command Stack during both the Start-of-Message (SOM) **and** End-of-Message (EOM) transfer sequences.

6.7.2 Illegalization RAM Memory Map

TABLE 80. ILLEGALIZING RAM ADDRESS DEFINITION	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	LOGIC “0”
9	LOGIC “1”
8	LOGIC “1”
7	$\overline{\text{BROADCAST}}$/ OWN ADDRESS
6	T/$\overline{\text{R}}$
5	SA4
4	SA3
3	SA2
2	SA1
1	SA0
0(LSB)	WC4/MC4

Notes:

(1) Address bit 7, $\overline{\text{BROADCAST}}$/ OWN ADDRESS, is logic "0" for broadcast commands, logic "1" for nonbroadcast commands.

(2) Address bit 6, T/$\overline{\text{R}}$, is high for transmit commands, low for receive commands.

(3) Bits 5 through 1, SA4 through SA0, define the command subaddress. SA4-SA0 are 00000 or 11111 for mode code commands. SA4-SA0 assume a value between 00001 and 11110 for non-mode code messages.

(4) Address bit 0, WC4/MC4, specifies the MSB of the command's Word Count/Mode Code field: Word Count for 00001 SA4-SA0 11110, Mode Code for SA4-SA0 = 00000 or SA4-SA0 = 11111. If WC4/MC4 is logic "0," the referenced word in the illegalization RAM is used to program command illegalization for Word Counts/Mode Codes 15 through 0. If WC4/MC4 is logic 1, the referenced word in the command illegalization RAM is used to program illegalization for Word Counts/Mode Codes 31 through 16.

(5) WC=00000 for a 32 word message as in the WC field of a command word.

The organization of the illegalization RAM table is illustrated in TABLE 81. As shown, the base address of the illegalization table is 0300 (hex). The index into the illegalizing RAM is formulated by means of BROADCAST/$\overline{\text{OWN ADDRESS}}$, T/$\overline{\text{R}}$ bit, Subaddress (4-0), and the MSB of the Word Count/Mode Code field (WC4/MC4), as defined by TABLE 80.

Commands may be illegalized down to the Word Count level. For example, a 1-word receive command to subaddress 1 can be legal, while a 2-word receive command can be illegalized.

The first 64 words of the ILLEGALIZATION table are used to illegalize Broadcast Receive Commands (two words per subaddress). The next 64 words refer to Broadcast Transmit Commands. Since nonmode code broadcast transmit commands are not defined by MIL-STD-1553B, the section of the illegalization table between (and including) address locations 0342 and 037D (hex) do **not** need to be programmed by the user. The next 64 words correspond to nonbroadcast receive commands. The final 64 words refer to nonbroadcast transmit commands. Reference TABLE 81.

For each broadcast/own address-T/$\overline{\text{R}}$-subaddress, **a pair** of words (32 bits) in the illegalization RAM table are allocated for the purpose of illegalizing any combination of the 32 possible word counts or mode codes.

The programming of the individual words in the illegalization table is defined by TABLE 82 and TABLE 83.

TABLE 81. ILLEGALIZATION RAM MAP	
ADDRESS	**DESCRIPTION**
0300	Brdcst/Rx, SA 0, MC15-0
0301	Brdcst/Rx, SA 0, MC31-16
0302	Brdcst/Rx, SA 1, WC15-0
0303	Brdcst/Rx, SA 1, WC31-16
• • •	• • •
033F	Brdcst/Rx, SA 31, MC31-16
0340	Brdcst/Tx, SA 0, MC15-0
0341	Brdcst/Tx, SA 0, MC31-16
0342	Brdcst/Tx, SA 1, WC 15-0
• •	• •
{Note: Non-Mode Code Broadcast/Transmit Commands (SA1-30) are not defined by MIL-STD-1553B. Therefore, addresses 0342-037D **do not need to be programmed**.}	
• •	• •
037D	Brdcst/Tx, SA 30, WC 31-16
037E	Brdcst/Tx, SA 31, MC 15-0
037F	Brdcst/Tx, SA 31, MC 31-16
0380	Own Addr/Rx, SA 0, MC 15-0
0381	Own Addr/Rx, SA 0, MC 31-16
0382	Own Addr/Rx, SA 1, WC 15-0
0383	Own Addr/Rx, SA 1, WC 31-15
• • •	• • •
03BE	Own Addr/RX, SA 31, MC 15-0
03BF	Own Addr/Rx, SA 31, MC 31-16
03C0	Own Addr/Tx, SA 0, MC 15-0
03C1	Own Addr/Tx, SA 0, MC 31-16
03C2	Own Addr/Tx, SA 1, WC 15-0
03C3	Own Addr/Tx, SA 1, WC 31-16
• • •	• • •
03FC	Own Addr/Tx, SA 30, WC 15-0
03FD	Own Addr/Tx, SA 30, WC 31-16
03DE	Own Addr/Tx, SA 31, MC 15-0
03FF	Own Addr/TX, SA 31. MC 31-16

6.7.3 Subaddress Illegalization Word 0

TABLE 82. ILLEGALIZATION RAM WORD BIT DEFINITIONS For even numbered addresses (WC/MC4=0)	
BIT	**DESCRIPTION**
15(MSB)	WC/MC = 15 Illegal
14	WC/MC = 14 Illegal
13	WC/MC = 13 Illegal
12	WC/MC = 12 Illegal
11	WC/MC = 11 Illegal
10	WC/MC = 10 Illegal
9	WC/MC = 9 Illegal
8	WC/MC = 8 Illegal
7	WC/MC = 7 Illegal
6	WC/MC = 6 Illegal
5	WC/MC = 5 Illegal
4	WC/MC = 4 Illegal
3	WC/MC = 3 Illegal
2	WC/MC = 2 Illegal
1	WC/MC = 1 Illegal
0(LSB)	WC = 32 illegal, MC = 0 Illegal

6.7.4 Subaddress Illegalization Word 1

TABLE 83. ILLEGALIZATION RAM WORD BIT DEFINITIONS : For odd numbered addresses (WC/MC4=1)	
BIT	**DESCRIPTION**
15(MSB)	WC/MC = 31 Illegal
14	WC/MC = 30 Illegal
13	WC/MC = 29 Illegal
12	WC/MC = 28 Illegal
11	WC/MC = 27 Illegal
10	WC/MC = 26 Illegal
9	WC/MC = 25 Illegal
8	WC/MC = 24 Illegal
7	WC/MC = 23 Illegal
6	WC/MC = 22 Illegal
5	WC/MC = 21 Illegal
4	WC/MC = 20 Illegal
3	WC/MC = 19 Illegal
2	WC/MC = 18 Illegal
1	WC/MC = 17 Illegal
0(LSB)	WC/MC = 16 Illegal

The following should be noted with regards to TABLE 82 and TABLE 83:

(1) To illegalize a particular word count for a given broadcast/own address-$T/\overline{R}$*-subaddress, the appropriate bit position in the respective illegalization word should be programmed to logic "1." A bit value of logic "0" designates the respective Command Word as a legal command.*

(2) For subaddresses 00001 through 11110, the "WC/MC" field specifies the Word Count field of the respective Command Word. For

subaddresses 00000 and 11111, the "WC/MC" field specifies the Mode Code field of the respective Command Word.

*(3) Since nonmode code broadcast transmit messages are not defined by MIL-STD-1553B, the sixty (60) words in the illegalization RAM, addresses 0342 through 037D, corresponding to these commands do not need to be initialized. The ACE will **not** respond to a nonmode code broadcast transmit command, but will **automatically** set the Message Error bit in its internal Status Word Register, regardless of whether or not corresponding bit in the illegalization RAM has been set. If the next message is a Transmit Status or Transmit Last Command mode code, the ACE will respond with its Message Error bit set.*

6.7.5 Accessing the Illegalization Table

In order to use the illegalizing feature, the host processor should write to the 256 words of illegalizing RAM as part of the ACE/Mini-ACE'S initialization procedure, following power turn-on. After the illegalization RAM has been loaded, the host processor then has the option of reading it back in order to verify. When the illegalization RAM initialization has been completed, the host processor should put the ACE/Mini-ACE on-line in RT mode by writing to Configuration Register #1.

If desired, the host processor may periodically reread the contents of the illegalization RAM, for continual verification. The ACE/Mini-ACE's 1553 protocol logic will perform a single read access during the RT Start-of-Message (SOM) sequence. As a result of the read access, the ACE/Mini-ACE will determine if the particular Command Word has been illegalized by the host CPU. Since the illegalization RAM should not be used for stack or message data (assuming illegalization is enabled), the ACE/Mini-ACE's 1553 logic will **never** write to this section of memory.

6.8 ENHANCED MODE CODE HANDLING

The ACE/Mini-ACE includes a mechanism for storing Data Words associated with specific mode code commands in individual locations in the shared RAM. In addition, the ACE/Mini-ACE has the ability to generate selective interrupts for specific mode commands based on a lookup table. These features are enabled in the ACE/Mini-ACE RT Enhanced mode, by setting ENHANCED MODE bit (bit 15 in Configuration Register #3) to logic "1," followed by setting ENHANCED MODE CODE HANDLING bit (bit 0 in Configuration Register #3) to logic "1."

ENHANCED MODE CODE HANDLING enables three aspects of handling mode code messages:

(1) For all nonmode code messages, and for mode code messages with ENHANCED MODE CODE HANDLING disabled, the third word of the message descriptor block in the stack is reserved for the DATA BLOCK POINTER. Reference FIGURES 8, 9, and 10. The DATA BLOCK POINTER references the starting location of the Data Word block for received or transmitted data. In the case of mode code messages, the Data Word block consists of a single Data Word.

However, for mode code commands with data, if ENHANCED MODE CODE HANDLING is enabled, the third word of the message descriptor in the RT stack will contain the actual **Data Word** transmitted or received, rather than a pointer to the (single word) data block. For mode commands without data, the third word of the descriptor is **not written to**.

(2) ENHANCED MODE CODE HANDLING affects the address mapping of Data Words transmitted or received for mode code messages. With ENHANCED MODE CODE HANDLING enabled, for mode commands with Data Words associated with them (transmit and receive commands 10 to 1F hex), the ACE/Mini-ACE will read the data from or store the data to **individual (for each mode code) fixed locations** in the RAM. The address locations associated with receive mode commands are 110-11F hex. These locations are accessed based on Mode Code bits 3-0. Transmit mode code data will be read from locations 120-12F based on Mode Code bits 3-0. If the SEPARATE BROADCAST option is selected (bit 0 of Configuration Register #2 is set to logic "1"), broadcast mode code receive Data Words will be stored in locations 130-13F hex . If the SEPARATE BROADCAST option is not selected (bit 0 of Configuration Register #2 is set to logic "0"), broadcast mode receive data will be stored along with the nonbroadcast receive Data Words in locations 110-11F hex. TABLE 84 illustrates the RAM locations for each of the mode commands with data.

(3) Mode code selective interrupts are enabled in the Enhanced ACE/Mini-ACE RT Mode by setting the ENHANCED MODE CODE HANDLING bit (bit 0 of Configuration Register #3) to logic "1" **and** by setting the RT SELECTED MODE CODE INTERRUPT bit (bit 1 in the Interrupt Mask Register) to logic "1" **and** initializing the MODE COMMAND SELECTIVE INTERRUPT TABLE (locations 108-10F hex in the RAM). Entries in the MODE COMMAND SELECTIVE INTERRUPT TABLE are addressed by appending the 3-bit value formed by broadcast, $T/\overline{R}$ bit, and MODE CODE bit 4 to the base address of 108 hex. The bit location within this 16-bit word that determines if the given mode command will generate an interrupt is specified by the 4-bit value formed by MODE CODE bits 3-0. If the appropriate bit has been programmed to logic "1," the ACE/Mini-ACE will generate an interrupt at the end of the current message. Note that some of the possible Command Word combinations are invalid. As long as the Command Word meets the 1553 criteria for word validation, the interrupt will be generated at the end of the message, even if the particular command is illegal or invalid. Refer to TABLE 85 and TABLE 86.

TABLE 84. ENHANCED MODE CODE DATA LOCATIONS

RAM LOCATION	MODE CODE
0110	UNDEFINED
0111	SYNCHRONIZE WITH DATA
0112	UNDEFINED
0113	UNDEFINED
0114	SELECTED TRANSMITTER SHUTDOWN
0115	OVERRIDE SELECTED TRANSMITTER SHUTDOWN
0116-011F	RESERVED (RECEIVE MODE CODES)
0120	TRANSMIT VECTOR WORD
0121	UNDEFINED
0122	UNDEFINED
0123	TRANSMIT BIT WORD
0124	UNDEFINED
0125	UNDEFINED
0126-012F	RESERVED (TRANSMIT MODE CODES)
0130	UNDEFINED BROADCAST
0131	BROADCAST SYNCHRONIZE WITH DATA
0132	UNDEFINED BROADCAST
0133	UNDEFINED BROADCAST
0134	BROADCAST SELECTED TRANSMITTER SHUTDOWN
0135	BROADCAST OVERRIDE SELECTED TRANSMITTER SHUTDOWN
0136-013F	RESERVED BROADCAST

TABLE 85. MODE CODE INTERRUPT LOOKUP TABLE RAM MAP	
ADDRESS	**DESCRIPTION**
0108	Receive Mode Commands 0-15 (Undefined)
0109	Receive Mode Commands 16-31 (With Data)
010A	Transmit Mode Commands 0-15 (Without Data)
010B	Transmit Mode Commands 16-31 (With Data)
010C	Broadcast Receive Mode Commands 0-15 (Undefined)
010D	Broadcast Receive Mode Commands 16-31 (With Data)
010E	Broadcast Transmit Mode Commands 0-15 (Without Data)
010F	Broadcast Transmit Mode Commands 16-31 (Undefined/Reserved)

TABLE 86. SAMPLE MODE COMMAND INTERRUPT LOOKUP TABLE ENTRY (Shown for location 010Ah)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED MODE CODE
14	RESERVED MODE CODE
13	RESERVED MODE CODE
12	RESERVED MODE CODE
11	RESERVED MODE CODE
10	RESERVED MODE CODE
9	RESERVED MODE CODE
8	RESET REMOTE TERMINAL
7	OVERRIDE INHIBIT TERMINAL FLAG
6	INHIBIT TERMINAL FLAG
5	OVERRIDE Tx SHUTDOWN
4	TRANSMITTER SHUTDOWN
3	INITIATE SELF TEST
2	TRANSMIT STATUS
1	SYNCHRONIZE
0(LSB)	DYNAMIC BUS CONTROL

6.9 BROADCAST OPTION

In RT mode, the ACE/Mini-ACE allows the use of broadcast messages as a software-programmable option. In the non-ENHANCED RT Mode, if the BROADCAST DISABLED bit (bit 7 in Configuration Register #5) is programmed to logic "0," the ACE/Mini-ACE will recognize RT Address 31 as the broadcast address. If the BROADCAST DISABLED bit is programmed to logic "1," then RT Address 31 will not be recognized as the broadcast address and may be used as a discrete terminal address. MIL-STD-1553B stipulates that RT address 31 shall **not** be assigned as a discrete terminal address.

With the BU-65620, broadcast may also be disabled by connecting the input pin BRO_ENA to logic "0."

If broadcast is enabled and the ACE/Mini-ACE RT receives a broadcast Command Word (RT address 31), followed **contiguously** by a Transmit Command Word to the ACE/Mini-ACE RT's own address, indicating an RT-to-RTs (broadcast) message, the broadcast Command Word will be superseded and the ACE/Mini-ACE RT will respond to the transmit command. Refer to page 152 for information of the effects of superseded commands.

6.10 BUSY BIT

If the host CPU asserts the $\overline{\text{BUSY}}$ bit low in Configuration Register #1, the ACE/Mini-ACE will respond to **any** command with the BUSY bit set in its RT Status Word. Similarly, if ALTERNATE RT STATUS WORD ENABLED (bit 5 of Configuration Register #3) is programmed to logic "1," then the BUSY Status Word Bit is directly controlled by means of bit 4 (S03) of Configuration Register #1. If the ACE/Mini-ACE is programmed for the non-ENHANCED mode (bit 15 of Configuration Register #3 is logic "0") **or** if BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3 is logic "0," for a receive command, Data Words **will be** written to the data block in the shared RAM referenced by the respective Lookup Table location. If the ACE/Mini-ACE is programmed for the ENHANCED mode (bit 15 of Configuration Register #3 is logic "1") **and** if BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3 is logic "1," for a nonmode code receive command, Data Words **will NOT be** written to the data block in the shared RAM referenced by the respective Lookup pointer.

For a nonmode code transmit command, the ACE/Mini-ACE will respond with Status/BUSY, but **no data words** will be transmitted.

If the Alternate RT Status Word option is **not selected**, the ACE may optionally set the busy bit based on broadcast/own RT address, T/$\overline{\text{R}}$ bit, and subaddress. ALTERNATE STATUS WORD ENABLE is nonselected in the non-ENHANCED mode (bit 15 of Configuration Register #3 set to logic "0") **or** if bit 5 of Configuration Register #3, ALTERNATE STATUS WORD ENABLE, is logic "0."

Assuming that ALTERNATE STATUS WORD is **not enabled**, the ACE/Mini-ACE's "Busy by Broadcast-T/$\overline{\text{R}}$-Subaddress" option is available in the Enhanced RT Mode (bit 15 of Configuration Register #3 set to logic "1") only. The Busy Bit Lookup Table is enabled by setting bit 13 of Configuration Register #2, BUSY LOOKUP TABLE ENABLE, to logic "1."

The Busy Bit Lookup Table occupies eight word locations, 0240 through 0247 (hex). As illustrated in TABLE 87, the offset into the lookup table is formulated for a specific command based on BROADCAST/$\overline{\text{OWN ADDRESS}}$, TRANSMIT/$\overline{\text{RECEIVE}}$, and the MSB of the Subaddress field (SA4).

For any given BROADCAST/$\overline{\text{OWN ADDRESS}}$, and TRANSMIT/$\overline{\text{RECEIVE}}$ combination, a pair of words (32 bits) are allocated in the Busy Bit Lookup Table for the purpose of setting the busy bit in response to a command to any of the 32 possible subaddresses. The MSB (SA4) of the subaddress is used to select which word is to be used, and Subaddress bits 3 through 0 (SA3-SA0) are used to determine which of the 16 bits in the selected word is to be used to program a particular subaddress as busy. A logic "0" in the respective bit location indicates

that the busy bit will not be set for that command, while a logic "1" indicates that the busy bit will be set in the next response to the next message to the selected subaddress.

If the ACE/Mini-ACE is Busy for a Transmit Vector Word mode command, a Data Word (Vector Word) will **not** be transmitted in the non-ENHANCED mode **or** if MODE COMMAND OVERRIDE BUSY, bit 13 of Configuration Register #3, is logic "0." Similarly, if the ACE is busy for a Synchronize with data mode command, the Data Word **will** be stored to shared RAM in the non-ENHANCED mode **or** if BUSY RX TRANSFER DISABLE, bit 3 of Configuration Register #3 is logic "0."

If the ACE/Mini-ACE is programmed for ENHANCED MODE **and** MODE COMMAND OVERRIDE BUSY is programmed to logic "1," then a Data Word **will** be transmitted for a Transmit Vector Word mode code. A Data Word **will** be stored for a Synchronize with data-mode code, even if the ACE/Mini-ACE is Busy **and** BUSY RECEIVE TRANSFER DISABLE is programmed to logic "1."

If the ACE/Mini-ACE is Busy for a Transmit BIT Word mode command, the Data Word (BIT Word) **will be transmitted** if the ACE/Mini-ACE is programmed for its non-ENHANCED MODE **or** if INHIBIT BIT WORD IF BUSY, bit 14 of Configuration Register #4, is logic "0." If the ACE/Mini-ACE is Busy for a Transmit BIT Word mode command, the Data Word (BIT Word) **will NOT be transmitted** if the ACE/Mini-ACE is programmed for its ENHANCED MODE **and** if INHIBIT BIT WORD IF BUSY, bit 14 of Configuration Register #4, is logic "1."

TABLE 87. BUSY BIT LOOKUP TABLE ADDRESS DEFINITION	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	LOGIC “0”
9	LOGIC “1”
8	LOGIC “0”
7	LOGIC “0”
6	LOGIC “1”
5	LOGIC “0”
4	LOGIC “0”
3	LOGIC “0”
2	BROADCAST/$\overline{\text{OWN ADDRESS}}$
1	T/$\overline{\text{R}}$
0(LSB)	SA4

Notes:

(1) Address bit 2, BROADCAST/$\overline{\text{OWN ADDRESS}}$, is logic "1" for broadcast commands, logic "0" for nonbroadcast commands.

(2) Address bit 1, T/$\overline{\text{R}}$, is high for transmit commands, low for receive commands.

(3) Address bit 0, SA4 specifies the MSB of the command's Subaddress field.

6.10.1 Subaddress Busy Word 0

TABLE 88. BUSY BIT LOOKUP TABLE FOR DEFINITION (For SA4 = 0)	
BIT	**DESCRIPTION**
15(MSB)	SUBADDRESS 15 BUSY
14	SUBADDRESS 14 BUSY
13	SUBADDRESS 13 BUSY
12	SUBADDRESS 12 BUSY
11	SUBADDRESS 11 BUSY
10	SUBADDRESS 10 BUSY
9	SUBADDRESS 9 BUSY
8	SUBADDRESS 8 BUSY
7	SUBADDRESS 7 BUSY
6	SUBADDRESS 6 BUSY
5	SUBADDRESS 5 BUSY
4	SUBADDRESS 4 BUSY
3	SUBADDRESS 3 BUSY
2	SUBADDRESS 2 BUSY
1	SUBADDRESS 1 BUSY
0(LSB)	SUBADDRESS 0 BUSY

6.10.2 Subaddress Busy Word 1

TABLE 89. BUSY BIT LOOKUP TABLE FOR DEFINITION (For SA4 = 1)

BIT	DESCRIPTION
15(MSB)	SUBADDRESS 31 BUSY
14	SUBADDRESS 30 BUSY
13	SUBADDRESS 29 BUSY
12	SUBADDRESS 28 BUSY
11	SUBADDRESS 27 BUSY
10	SUBADDRESS 26 BUSY
9	SUBADDRESS 25 BUSY
8	SUBADDRESS 24 BUSY
7	SUBADDRESS 23 BUSY
6	SUBADDRESS 22 BUSY
5	SUBADDRESS 21 BUSY
4	SUBADDRESS 20 BUSY
3	SUBADDRESS 19 BUSY
2	SUBADDRESS 18 BUSY
1	SUBADDRESS 17 BUSY
0(LSB)	SUBADDRESS 16 BUSY

6.11 RT ADDRESS INPUTS

In order for the ACE/Mini-ACE to respond as an RT to a discrete (nonbroadcast) RT address, the address of a received Command Word must match the value programmed for pins RTAD4-RTAD0, **and** RTADP must be programmed to create an **odd** parity sum with RTAD4-0. Unless broadcast is disabled (broadcast disabled bit 7 of Configuration Register #5 programmed to logic "1."), the ACE/Mini-ACE's capability to receive messages to the broadcast address, RT address 31 (11111), is not effected by the programming of RTAD4-0 and RTADP. In the ACE/Mini-ACE's RT mode, the programmed value of the RT Address is sampled approximately 2 µs after the mid-parity zero-crossing of a received Command Word.

Odd parity requires that there be **an odd number of logic "1"s in RTAD4 through RTAD0 and RTADP.** Therefore, RTADP should be programmed to logic "0" for RT addresses 1, 2, 4, 7, 8, 11, 13, 14, 16, 19, 21, 22, 25, 26, 28, and 31 (if broadcast is disabled). RTADP must be programmed to logic "1" for RT addresses 0, 3, 5, 6, 9, 10, 12, 15, 17, 18, 20, 23, 24, 27, 29, and 30.

The ACE/Mini-ACE provides options for either a hardwired RT Address or a latched RT Address. The BU-65170, BU-61580, and BU-61585 versions provide the "hardwired" option only. The BU-65171, BU-61581, and BU-61586 versions provide the "latchable" option only. With the BU-61578/79, BU-61588, BU-61590, BU-65620, BU-61688/89 both options are available, programmable by means of the RT_AD_LAT input pin.

There are internal pull-up resistors between the RT Address inputs, RTAD4-RTAD0 and RTADP, and +5V. The nominal value of these pull-up resistors is between 10K and 100K ohms. If there is a minimal P.C.

board trace length (e.g., 1 to 2 inches) from the input pins for these signals to on-board jumper points, the internal pull-up resistors may be used to establish a logic "1" signal level, without external pull-ups. **However, if the connection involves a longer signal trace, particularly to an external connector, it is strongly recommended that a direct connection to +5 volts be made to provide a logic "1" input signal.** If this is not possible, it is recommended that low level value pull-up resistors (less than 10K ohms) be used to increase the noise immunity for providing a logic "1" input.

With the BU-65178/79, BU-61588, BU-61590, BU-65620, and BU-61688/89, RT_AD_LAT should be connected to logic "0" to configure for the "hardwired" mode, and to logic "1" to configure for the "latchable" mode. For the other ACE products, RT_AD_LAT is hardwired internally.

For **all** versions of the ACE/Mini-ACE, the sense of the RT_AD_LAT signal is CPU readable in the ENHANCED MODE, by means of bit 6 of Configuration Register #5. In addition, for **all** versions of the ACE/Mini-ACE in the ENHANCED MODE, the value of the RT address and parity is readable by means of bits 5 through 0 of Configuration Register #5.

While in the hardwired RT Address mode, the internal RT Address continuously tracks the logic values presented on the RTAD4-RTAD0, and RTADP inputs.

There are two methods of updating the value held in the internal RT Address latch:

1) The first method is applicable only for the BU-55178/79, BU-61588, BU-61590, BU-65620, and BU-61688/89.. This method is to bring the RT_AD_LAT input signal low and then back high again. On the rising edge of RT_AD_LAT, the value presented on the RTAD4-RTAD0, and RTADP inputs will be stored in the internal RT Address latch.

2) The second method allows for a software programmable RT Address. With this method, the ACE/Mini-ACE needs to be programmed for the Enhanced Mode of operation (bit 15 of Configuration Register #3 programmed to logic "1"), and enabling the LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5 feature (bit 3 of Configuration Register #4 set to logic "1"), and then writing to Configuration Register #5. During the write access to Configuration Register #5, the logic values presented on the RTAD4-RTAD0, and RTADP inputs will be stored in the internal RT Address latch. Note that this method of programming may not be used in the zero-wait state mode since the RT Address latch is updated during the internal data word transfer, which is after the external transfer.

It should be noted that the only mechanism available for updating the RT Address latch in the BU-65171, BU-61581, and BU-61586 is through the use of the Latch RT Address with Configuration Register #5 feature. For these products, or with the BU-65178/79, BU-61588, BU-61590, BU-65620, BU-61688/89 with RT_AD_LAT connected to logic "1," a hardware reset ($\overline{\text{MSTCLR}}$ input of logic "0" for 100 ns minimum) will clear the internal latched RT Address value to 0 (including the address parity bit).

A software reset (writing a logic "1" to bit 0 of the Start/Reset Register) or a Mode Code Reset Command has no effect on the value of the internal RT Address latch.

The sequence to configure and program the ACE/Mini-ACE for a software programmable RT address is summarized as follows:

1) For a BU-65178/79, BU-61588, BU-61590, BU-65620, BU-61688/89, the input signal RT_AD_LAT must be connected to logic "1." For a BU-65171, BU-61581, or BU-61586, this connection is made by an internal wire bond. For a BU-65170, BU-61580, or BU-61585, the latchable RT Address option is not available.

2) Connect RTAD4 to D5, RTAD3 to D4, ... RTAD0 to D1, RTADP to D0.

3) Configure the ACE/Mini-ACE for enhanced mode operation by programming bit 15 of Configuration Register #3, ENHANCED MODE ENABLED, to logic "1."

4) Program LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5, bit 3 of Configuration Register #4, to logic "1."

5) Program the RT Address by writing to bits 5 through 1 (RTAD4-0) and bit 0 (RTADP) of Configuration Register #5. It should be noted that the value of the ACE/Mini-ACE's internal RT Address register is CPU readable by means of these 6 bits.

Another configuration to use the latchable RT Address function is to hardwire the RTAD4-RTAD0, and RTADP inputs using external jumpers (such as a MIL-STD-1760 umbilical). Now, when the latch mode is enabled and the host processor writes to Configuration Register #5, the hardwired RT Address provided by the jumpers will be latched internally. A common mode of operation is to latch the RT Address during the host processor's power-up initialization sequence.

6.12 RT STATUS WORD

The ACE/Mini-ACE supports two options for the host processor to program the bits of the RT Status Word:

1) The standard or "nonalternate" Status Word. For MIL-STD-1553B applications, this option is normally used. In this configuration, the ACE/Mini-ACE automatically updates the values of the Message Error, Broadcast Command Received, and Dynamic Bus Control bits in accordance with MIL-STD-1553B. The values of the Busy, Service Request, and Subsystem Flag bits are programmable by the host CPU. In addition, the values for the Instrumentation and Reserved bits are automatically set to logic "0" in the RT's Status Word response. There is also an option for the Terminal Flag bit to be automatically set for the response to the subsequent nonbroadcast message following a failure of the ACE/Mini-ACE RT's on-line self-test.

2) The "Alternate" status word mode. With this option, **all 11** RT Status Word bits are programmable by the host processor, by means of bits 11 through 1 of Configuration Register #1. This mode may be used to support MIL-STD-1553A, McAir, G.D. F16, or other "non-1553B" applications.

The default (power turn-on value) is for the standard (1553B) "non-Alternate" Status Word. The ACE/Mini-ACE configures to this mode in the non-enhanced mode (bit 15 of Configuration Register #3 programmed to logic "0" **or** ALTERNATE STATUS WORD ENABLED, bit 5 of Configuration Register #3 programmed to logic "0").

To configure the ACE/Mini-ACE RT for the Alternate RT Status Word mode, the ACE/Mini-ACE must be programmed for by programming bits 15, ENHANCED MODE ENABLED, **and** bit 5, ALTERNATE STATUS WORD ENABLED, of Configuration Register #3, to logic "1."

Both options support command illegalization.

In either of the two modes, the values programmed in Configuration Register #1 are sampled approximately 4 to 5 µs after the mid-parity bit crossing of the received Command Word.

In either of the two modes, the value of the RT Status Word that was transmitted in response to the **last** nonbroadcast message processed by the ACE/Mini-ACE RT may be read from the read-only RT Status Word Register (register address 01110).

The programming of the ACE/Mini-ACE RT Status Word bits is summarized in TABLE 90.

TABLE 90. RT STATUS WORD PROGRAMMING OPTIONS			
BIT NUMBER (PER MIL-STD-1553B)	**BIT FUNCTION (PER MIL-STD-1553B)**	**OPERATION IN STANDARD ("NON-ALTERNATE") STATUS MODE**	**OPERATION IN ALTERNATE STATUS MODE (SEE NOTES 8 AND 9)**
1-3	Sync Field	Sync Field	Sync Field
4-8	RT Address	RT Address	RT Address
9	Message Error	Set to logic "1" following an error in the Data Word portion of a received message, or for an illegalized Command Word, in accordance with MIL-STD-1553B. See Note 1.	Controlled by S10, bit 11 of Configuration Register #1. Also, set to logic "1" for illegalized Command Word, in accordance with MIL-STD-1553B. See Note 10.
10	Instrumentation	Logic "0"	Controlled by S9, bit 10 of Configuration Register #1.
11	Service Request	Controlled by means of $\overline{\text{SERVICE REQUEST}}$, bit 9 of Configuration Register #1. As an option, may be automatically cleared by a Transmit Vector mode command. See Note 2.	Controlled by S8, bit 9 of Configuration Register #1.
12	Reserved	Logic "0"	Controlled by S7, bit 8 of Configuration Register #1.
13	Reserved	Logic "0"	Controlled by S6, bit 7 of Configuration Register #1.
14	Reserved	Logic "0"	Controlled by S5, bit 6 of Configuration Register #1.
15	Broadcast Command Received	In compliance with MIL-STD-1553B. See Note 3.	Controlled by S4, bit 5 of Configuration Register #1.
16	Busy	Controlled by means of $\overline{\text{BUSY}}$, bit 10 of Configuration Register #1 and Busy Lookup Table. See Note 4.	Controlled by S3, bit 4 of Configuration Register #1. Can have an effect on received Data Words. See Note 11.
17	Subsystem Flag	Controlled by means of $\overline{\text{SUBSYSTEM FLAG}}$, bit 8 of Configuration Register #1, and $\overline{\text{SSFLAG}}$ input signal. See note 5.	Controlled by S2, bit 3 of Configuration Register #1.
18	Dynamic Bus Control Accepted	Controlled in accordance with MIL-STD-1553B by means of $\overline{\text{DYNAMIC BUS CONTROL ACCEPTANCE}}$, bit 11 of Configuration Register #1. See Note 6.	Controlled by S1, bit 2 of Configuration Register #1.
19	Terminal Flag	In ENHANCED MODE (bit 15 of Configuration Register #3 set to logic "1"), controlled by $\overline{\text{RTFLAG}}$, bit 7 of Configuration Register #1. Optionally, may be automatically set as the result of a self-test failure. See Note 7.	Controlled by S0, bit 1 of Configuration Register #1. See Note 12.
20	Parity	Odd parity, per MIL-STD-1553B.	Odd parity, per MIL-STD-1553B.

Notes:

(1) For an error in the Data Word portion of a received message (sync or Manchester encoding, bit count, word count, or parity error), the ACE/Mini-ACE RT will not respond to the current message. However, the internal Message Error bit will be set to logic "1." This value will be reflected in the read-only RT Status Word Register.

If the ACE/Mini-ACE receives a Command Word that has been illegalized by means of the illegalization table (see section on RT COMMAND ILLEGALIZATION), the ACE will respond with the Message Error bit set in its Status Word. An illegalized command will result in ILLEGAL COMMAND WORD, bit 6 of the RT Block Status Word, to be set to logic "1." For an illegalized transmit command, the ACE/Mini-ACE will transmit the Status Word only with the Message Error bit set; it will not transmit any Data Words. For a valid illegalized receive command, the ACE/Mini-ACE will store the received Data Words unless: the ACE/Mini-ACE is in ENHANCED MODE (bit 15 of Configuration Register #3 is logic "1") and ILLEGAL RECEIVE TRANSFER DISABLE, bit 4 of Configuration Register #3, is programmed to logic "1." In the latter case, received Data Words will not be stored to the ACE/Mini-ACE shared RAM.

In either case, if the next message is a Transmit Status or Transmit Last Command mode code, the ACE/Mini-ACE RT will respond to the next command with the Message Error bit set to logic "1." To all other subsequent commands, the ACE/Mini-ACE RT will respond with the Message Error bit set to logic "0."

Notes (continued):

(2) Note that programming $\overline{\text{SERVICE REQUEST}}$ to logic "0" in Configuration Register #1 results in a value of logic "1" for the Service Request bit transmitted in the RT Status Word. Also, note that this bit is effected by the value programmed for CLEAR SERVICE REQUEST, bit 2 of Configuration Register #2. If CLEAR SERVICE REQUEST is logic "1," the value of $\overline{\text{SERVICE REQUEST}}$ will automatically clear (to logic "1") after the ACE/Mini-ACE RT has responded to a Transmit Vector Word mode code command. That is, if CLEAR SERVICE REQUEST is logic "1" and SERVICE REQUEST is logic "0," the ACE/Mini-ACE RT will respond with the Service request bit set to logic "1" until the ACE/Mini-ACE responds to a Transmit Vector Word command. For this message, the ACE/Mini-ACE will respond with the Service Request bit still set to logic "1" in its Status Word. Following this message, the value of $\overline{\text{SERVICE REQUEST}}$ clears to logic "1" and stays cleared until re-asserted to logic "0" by the host processor.

(3) In accordance with MIL-STD-1553B, the value of the internal Broadcast Command Received bit will be set to logic "1" following reception of a valid Broadcast Command Word. This value will be reflected in the read-only RT Status Word Register. If the next message is a Transmit status or Transmit last command mode code, the ACE/Mini-ACE RT will respond with the Broadcast command received bit set to logic "1." To all other commands, the ACE/Mini-ACE will respond with the Broadcast command received bit set to logic "0."

(4) Note that programming $\overline{\text{BUSY}}$ to logic "0" in Configuration Register #1 results in a value of logic "1" for the Busy bit transmitted in the RT Status Word.

If $\overline{\text{BUSY}}$ is programmed to logic "0" or the ACE/Mini-ACE receives a Command Word (Bcst, $\text{T}/\overline{\text{R}}$ bit, Subaddress) that has been programmed for a BUSY response by means of the Busy lookup table (see BUSY BIT section), the ACE/Mini-ACE will respond with the Busy bit set in its Status Word.

For the response to a transmit command when Busy, the ACE/Mini-ACE will transmit the Status Word only with the Busy bit set; it will not transmit any Data Words. For a "Busy" receive command, the ACE/Mini-ACE will store the received Data Words unless: the ACE/Mini-ACE is in ENHANCED MODE (bit 15 of Configuration Register #3 is logic "1") and BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3, is logic "1." In the latter case, received Data Words will not be stored in the ACE/Mini-ACE shared RAM.

In either case, if the next message is a Transmit Status or Transmit last Command mode code, the ACE/Mini-ACE RT will respond with the Busy bit set to logic "1." To all other commands, the ACE/Mini-ACE will respond with the value of the Busy bit determined by the value of $\overline{\text{BUSY}}$ in Configuration Register #1 and the programming of the Busy lookup table for that command (not the previous command).

(5) Note that programming $\overline{\text{SUBSYSTEM FLAG}}$ to logic "0" in Configuration Register #1 results in a value of logic "1" for the Subsystem Flag bit transmitted in the RT Status Word.

The Subsystem Flag Status Word bit will also be set to logic "1" if the value of logic "0" is sampled on the $\overline{\text{SSFLAG}}$ input signal during the RT Start-of-Message (SOM) sequence, approximately 4 µs after the mid-parity bit of the received Command Word. A possible use of the $\overline{\text{SSFLAG}}$ input is to indicate failure of the host CPU, by connecting $\overline{\text{SSFLAG}}$ to the output of a processor watchdog timer. Note that the value presented on $\overline{\text{SSFLAG}}$ has no effect on the value of the $\overline{\text{SUBSYSTEM FLAG}}$ bit written or read in Configuration Register #1. Also, note that the value presented on the $\overline{\text{SSFLAG}}$ input has no effect in the Alternate RT Status mode.

(6) In accordance with MIL-STD-1553B, the Dynamic Bus Control Acceptance Status Word bit will only be set to logic "1" if $\overline{\text{DYNAMIC BUS CONTROL ACCETPANCE}}$ (bit 11 of Configuration Register #1) is programmed for a value of logic "0" and the ACE/Mini-ACE RT is responding to a Dynamic Bus Control mode command. For all other commands, the Dynamic Bus Control Acceptance Status Word bit will be logic "0." It should be noted that the ACE/Mini-ACE will not automatically switch from RT to BC mode following reception (and acceptance) of a Dynamic Bus Control mode command.

(7) In ENHANCED MODE (bit 15 of Configuration Register #3 programmed to logic "1"), the value of the transmitted RT flag Status Word bit can be set to logic "1" by programming $\overline{\text{RTFLAG}}$, bit 7 of Configuration Register #1, to logic "0."

Notes (continued):

Alternatively, in ENHANCED MODE, the ACE/Mini-ACE RT may be programmed to automatically transmit logic "1" for the RT Flag Status Word bit following a failure of the ACE RT's on-line self-test. In this case, if the on-line self-test for a particular message fails, the Terminal Flag Status Word bit will be set to logic "1" in the response to the subsequent nonbroadcast message. This is done by programming RTFAIL-RTFLAG AUTOWRAP ENABLE, bit 2 of Configuration Register #3, to logic "1."

In RT mode, the self-test is performed for every nonbroadcast message processed by the ACE/Mini-ACE. The self-test is considered to have failed under either (or both) of two circumstances:

(a) Loop Test Failure. A loopback test is performed on the transmitted portion of every nonbroadcast message. A validity check is performed on the received version of every word transmitted by the ACE/Mini-ACE. In addition, a bit-by-bit comparison is performed on the last word transmitted by the RT for each message. If either the received version of any transmitted word is determined to be invalid (sync, encoding, bit count, or parity error) and/or the received version of the last word does not match the transmitted version, the looptest is considered to have failed.

(b) Transmitter Timeout. A transmitter timeout condition occurs when the ACE/Mini-ACE's 668 µs Transmitter Watchdog Timer times out and aborts transmission on the 1553 bus. This indicates a fault in the Manchester II encoder, RT state machine, or word count logic.

(8) In the Alternate Status mode, Status Word bit positions 9 through 19 (per MIL-STD-1553B) are controlled directly by means of S10 through S0, bits 11 through 1 of Configuration Register #1. That is, the respective RT Status Word bit are set to logic "1" by programming the respective Configuration Register #1 bits to logic "1" (not logic "0").

(9) The following functions are not applicable in the Alternate Status Word mode:
- (a) Service Request Auto-Clear (Note 2).
- (b) Operation of the MIL-STD-1553B Broadcast Command Received bit (Note 3).
- (c) $\overline{\text{SSFLAG}}$ input signal (Note 5).
- (d) Operation of the MIL-STD-1553B Dynamic Bus Control Acceptance bit (Note 6).
- (e) Effect of the RT on-line self-test on bit 19 ("Terminal Flag," per MIL-STD-1553B) (Note 7).

(10) For an error in the Data Word portion of a received message following a valid Command Word (sync or Manchester encoding, bit count, word count, or parity error), the ACE/Mini-ACE RT will not respond to the current message. However, the internal Message Error bit will be set to logic "1." This value will be reflected in the read-only RT Status Word Register. It should be noted that the value of this bit has no effect on the Message Error bit in the Status Word response to the next message.

If the ACE/Mini-ACE receives a Command Word that has been illegalized by means of the illegalization table (see RT COMMAND ILLEGALIZATION section), the ACE/Mini-ACE will respond with the Message Error bit set in its Status Word. An illegalized command will result in ILLEGAL COMMAND WORD, bit 6 of the RT Block Status Word, to be set to logic "1." For an illegalized transmit command, the ACE/Mini-ACE will transmit the Status Word only with the Message Error bit set; it will not transmit any Data Words. For a valid illegalized receive command, the ACE/Mini-ACE will store the received Data Words unless: the ACE/Mini-ACE is in ENHANCED MODE (bit 15 of Configuration Register #3 is logic "1") and ILLEGAL RECEIVE TRANSFER DISABLE, bit 4 of Configuration Register #3, is logic "1." In the latter case, received Data Words will not be stored in the ACE/Mini-ACE shared RAM.

(11) If S3, bit 4 of Configuration Register #4, is set to logic "1," the ACE/Mini-ACE will respond to a transmit command with a Status Word (with bit 16, per MIL-STD-1553B, set to logic "1"), followed by the requested number of Data Words.

If S3 is logic "1," and BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3, is programmed to logic "0," received Data Words will be stored to the ACE/Mini-ACE shared RAM. If both S3 and BUSY RECEIVE TRANSFER DISABLE are programmed to logic "1," received Data Words will not be stored in the ACE/Mini-ACE shared RAM.

In the Alternate Status Word mode, the Busy lookup table will affect the value of bit 16 ("Busy," per MIL-STD-1553B) for transmitted RT Status Words. However, the Busy lookup table has no effect on the transmission or storage of Data Words.

Notes (continued):

(12) In the Alternate Status Word mode, an RTFAIL condition (wraparound test failure) will not affect the value of the RT Flag Status Word bit, regardless of the value of the RTFAIL-RTFLAG AUTOWRAP ENABLE bit, bit 2 of Configuration Register #3.

6.13 RT-TO-RT RESPONSE TIMEOUT

The ACE/Mini-ACE's response timeout time is applicable to RT mode. When the ACE/Mini-ACE RT is the receiving RT in an RT-to-RT transfer message, the timer is used to determine that the transmitting RT has not responded in time. The value of the RT-to-RT timeout timer corresponds to the time between the mid-parity bit zero crossing of the Transmit Command Word and the mid-sync zero crossing of the transmitting RT's Status Word. In the non-ENHANCED mode, the value of this timer defaults to a nominal value of 18 µs. In order to accommodate long buses, the value of this timeout is programmable by the host processor. In the ENHANCED MODE (bit 15 of Configuration Register #3 programmed to logic "1"), the value of the RT-to-RT timeout is programmable by means of Configuration Register #5, as illustrated in TABLE 47 and TABLE 91.

TABLE 91. RT-to-RT RESPONSE TIMEOUT SELECT

BIT 10 OF C.R. #5 RESPONSE TIMEOUT SELECT 1	BIT 9 OF C.R. #5 RESPONSE TIMEOUT SELECT 0	RESPONSE TIMEOUT TIME VALUE (S)
0	0	18.5
0	1	22.5
1	0	50.5
1	1	130

6.14 RT BUILT-IN-TEST (BIT) WORD

The ACE/Mini-ACE RT offers two options for implementing the RT Built-In-Test (BIT) Word: an Internal BIT Word and an External BIT Word.

Using the Internal BIT Word option, the ACE/Mini-ACE RT responds to a Transmit BIT Word mode command with the Status Word, followed by the contents of the ACE/Mini-ACE RT's internal BIT Word Register. The format and bit descriptions for this word are defined in TABLE 92. With the External BIT Word option, the ACE/Mini-ACE RT responds with a BIT Word that is stored in a location in the ACE/Mini-ACE shared RAM. The value of this word is fully software programmable by the host CPU.

In the ENHANCED MODE, it should be noted that the CPU may read the value of the internal BIT Word by means of the read-only BIT Word Register, register address 0F (hex). This register may be read,

regardless of whether the ACE/Mini-ACE RT is programmed to respond with the Internal or External BIT Word.

In the NON-ENHANCED mode, **or** if EXTERNAL BIT WORD ENABLE, bit 15 of Configuration Register #4, is programmed to logic "0," the BIT Word transmitted is accessed from the ACE/Mini-ACE's internal BIT Word register.

If the ACE/Mini-ACE is programmed for ENHANCED MODE (bit 15 of Configuration Register #15 is logic "1") **and** if EXTERNAL BIT WORD ENABLE is programmed to logic "1," the BIT Word transmitted will be read from a memory location. In this case, if ENHANCED MODE CODE HANDLING is disabled (ENHANCED MODE disabled **or** ENHANCED MODE CODE HANDLING disabled (bit 0 of Configuration Register #3 is programmed to logic "0")), the location accessed for the external BIT Word will be the address referenced by the RT lookup table pointer for subaddress 00000 or subaddress 11111. In this case, it should be noted that for a given subaddress (00000 or 11111), the **same** Data Word will be transmitted in response to either a Transmit BIT Word **or** a Transmit vector word mode command.

If ENHANCED MODE CODES are enabled (ENHANCED MODE **and** ENHANCED MODE HANDLING enabled (bit 0 of Configuration Register #3 is programmed to logic "1")), the external BIT Word will be accessed from address location 0123.

If the ACE/Mini-ACE is Busy (either globally, or for Transmit subaddress 00000 or 11111), for a Transmit BIT Word mode command, the Data Word (BIT Word) **will be transmitted** if the ACE/Mini-ACE is programmed for its non-ENHANCED MODE **or** if INHIBIT BIT WORD IF BUSY, bit 14 of Configuration Register #4, is logic "0." If the ACE/Mini-ACE is Busy for a Transmit BIT Word mode command, the Data Word (BIT Word) **will NOT be transmitted** if the ACE/Mini-ACE is programmed for its ENHANCED MODE **and** if INHIBIT BIT WORD IF BUSY, bit 14 of Configuration Register #4, is logic "1."

The bit map and bit descriptions for the internal RT Built-in-Test (BIT) Word are indicated below.

TABLE 92. RT BIT WORD (READ 0Fh)	
BIT	**DESCRIPTION**
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	CHANNEL B / $\overline{A}$
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

Notes : Bits 15 through 9 are cleared only following a $\overline{\text{MSTCLR}}$ input, a software reset via the Start/Reset Register, or reception of a Reset Remote Terminal mode command. Bits 8 through 0 are updated as a result of every message processed.

TRANSMITTER TIMEOUT: Set if the ACE/Mini-ACE's failsafe timer detected a fault condition. The transmitter timeout circuit will automatically shut down the CH. A or CH. B transmitter if it transmits for longer than 668 µs. In RT mode, the ACE/Mini-ACE will terminate the processing of the current message as the result of a transmitter timeout, however, it **will respond** to the next message received.

CH. B LOOP TEST FAILURE, CH. A LOOP TEST FAILURE: A loopback test is performed on the transmitted portion of every nonbroadcast message. A validity check is performed on the received version of every word transmitted by the ACE/Mini-ACE. In addition, a bit-by-bit comparison is performed on the last word transmitted by the RT for each message. If either the received version of any transmitted word is determined to be invalid (sync, encoding, bit count, or parity error) and/or the received version of the last transmitted word does not match the transmitted version, or a failsafe timeout occurs on the respective channel, the LOOP TEST FAILURE bit for the respective bus channel will be set.

HANDSHAKE FAILURE: A handshake can only occur in the ACE/Mini-ACE's transparent configuration for the processor interface. A handshake failure **cannot occur** in the buffered mode. If this bit is set, it indicates that the subsystem has failed to respond with the DMA handshake input $\overline{\text{DTGRT}}$ asserted within the allotted time in response to the ACE/Mini-ACE asserting $\overline{\text{DTREQ}}$. Alternatively, a handshake failure will occur if the host CPU fails to clear $\overline{\text{STRBD}}$ (high) within the allotted time after the ACE/Mini-ACE has asserted its $\overline{\text{READYD}}$ output (low). The allotted time is 4 µs for a 16 MHz clock, or 3.5 µs for a 12 MHz clock.

CH. B TRANSMITTER SHUTDOWN, CH. A TRANSMITTER SHUTDOWN: Indicates that the transmitter on the respective bus channel has been shut down by a Transmitter shutdown mode code command received on the alternate channel. If an Override transmitter shutdown mode code command is received on the alternate channel, this bit will revert back to logic "0."

TERMINAL FLAG INHIBITED: Set to logic "1" if the ACE/Mini-ACE's Terminal Flag RT Status bit has been disabled by an Inhibit terminal flag mode code command. Will revert to logic "0" if an Override inhibit terminal flag mode code command is received.

$\overline{\text{CH. A/CH. B:}}$ Logic "0" if the previous message was received on CH.A, logic "1" if the previous message was received on CH. B.

HIGH WORD COUNT: Set to logic "1" if the previous message had a high word count error.

LOW WORD COUNT: Set to logic "1" if the previous message had a low word count error.

INCORRECT SYNC TYPE RECEIVED: If set, indicates that the ACE/Mini-ACE detected a Command sync in a received Data Word.

INVALID WORD: Indicates that the ACE/Mini-ACE RT received a Data Word containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

RT-to-RT GAP/SYNC/ADDRESS ERROR: This bit is set if the ACE/Mini-ACE RT is the receiving RT for an RT-to-RT transfer and one or more of the following occur: (1) If the GAP CHECK ENABLED bit (bit 8) of Configuration Register #5 is set to logic "1" and the transmitting RT responds with a response time of less than 4 µs, per MIL-STD-1553B (mid-parity bit to mid-sync); i.e., less than 2 µs dead time; and/or (2) There is an incorrect sync type or format error (encoding, bit count, and/or parity error) in the transmitting RT Status Word; and/or (3) The RT address field of the transmitting RT Status Word does not match the RT address in the transmit Command Word.

RT-to-RT RESPONSE TIMEOUT: If set, indicates that, for the previous message, the ACE/Mini-ACE was the receiving RT for an RT-to-RT transfer **and** that the transmitting RT either did not respond or responded later than the ACE/Mini-ACE's RT-to-RT Timeout time. The ACE/Mini-ACE's RT-to-RT Response Timeout Time is defined as the time from the mid-bit crossing of the parity bit of the transmit Command Word to the mid-sync crossing of the transmitting RT Status Word. The value of the RT-to-RT Response Timeout is nominally 18.5 µs in the non-Enhanced mode, or programmable from among nominal values of 18.5, 22.5, 50.5, or 130 µs in the enhanced mode.

RT-to-RT SECOND COMMAND ERROR: If the ACE/Mini-ACE is the receiving RT for an RT-to-RT transfer, this bit set indicates one or more of the following error conditions in the transmit Command Word: (1) T/R bit = logic "0"; (2) subaddress = 00000 or 11111; (3) same RT Address field as the receive Command Word.

COMMAND WORD CONTENTS ERROR: Indicates a received command word is not defined in accordance with MIL-STD-1553B. This includes the following undefined Command Words: (1) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** the Command Word is a nonmode code, broadcast, transmit command; (2) The OVERRIDE MODE $T/\overline{R}$ ERROR bit, bit 6 of Configuration Register #3, is logic "0" **and** a message with a $T/\overline{R}$ bit of "0," a subaddress/mode field of 00000 or 11111 and a mode code field between 00000 and 01111; (3) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** a mode code command that is not permitted to be broadcast (e.g., Transmit status) is sent to the broadcast address (11111).

6.15 RT START-OF-MESSAGE AND END-OF-MESSAGE TRANSFER SEQUENCES

Approximately 1.25 µs following the mid-parity bit crossing of a received Command Word, the ACE/Mini-ACE performs the RT Start-of-Message (SOM) sequence. Approximately 6 µs after the end of the last word transmitted by the RT (or received, for a broadcast message), the ACE/Mini-ACE performs the RT End-of-Message (EOM) Sequence. The SOM and EOM sequences consist of sequences of words read from and written to the ACE/Mini-ACE's shared RAM. The SOM and EOM sequences are summarized below:

6.15.1 RT Start-of-Message (SOM) Sequence.

1) If command illegalization is used, the appropriate illegalization word is read from the Illegalization lookup table.

2) The Stack Pointer address is read from the active area Stack Pointer location. This address is used for accessing the RT descriptor block in the Command Stack.

3) If the selective Busy (by Bcst, $T/\overline{R}$ bit, subaddress) option is used, the appropriate "Busy" word is read from the Busy lookup table.

4) If ENHANCED RT MEMORY MANAGEMENT is enabled (bit 1 of Configuration Register #2 programmed to logic "1"), allowing

the use of circular buffers and/or double buffering, the Subaddress Control Word is read from the Subaddress Control Word portion of the RT lookup table.

5) With the exceptions of a mode command with no Data Word or ENHANCED MODE CODE HANDLING enabled, the Data Block Address is read from the appropriate RT lookup table location.

6) The Command Word is written to the fourth location in the block descriptor.

7) With the exceptions of a mode command with no Data Word or ENHANCED MODE CODE HANDLING enabled, the Data Block address is written to the third location in the block descriptor.

8) The Time Tag word is written to the second location in the block descriptor.

9) The Block Status Word is written to the first location in the block descriptor. The value of the block status word is 4000 (SOM and all status bits cleared).

10) The value of the Stack Pointer read in step 2 is incremented by four and written to the active area Stack Pointer location.

6.15.2 RT End-of-Message (EOM) Sequence.

1) If the current message is using circular buffering or double buffering, the Subaddress Control Word is read from the Subaddress Control Word section of the RT lookup table.

2) If the current message is using receive subaddress double buffering, the Data Block Address is read from the RT lookup table; **or,** if the message was a mode command with data **and** ENHANCED MODE CODE HANDLING is enabled, the Data Word transmitted or received for a mode code message with data is written to the third location in the block descriptor. If ENHANCED MODE CODE HANDLING is enabled, **no** word is stored to the third location in the RT descriptor for a mode code message without data.

3) If the current message is using circular buffering or double buffering and the pointer address needs to be updated, the updated value of the pointer is written to the RT lookup table.

4) The Time Tag word is written to the second location in the block descriptor.

5) The Block Status Word is written to the first location of the block descriptor.

6.16 SUMMARY OF RT EXCEPTION CONDITIONS

In response to various message errors and other exception conditions, the ACE/Mini-ACE remote terminal takes actions and provides a number of indications. TABLE 93 indicates the respective RT response and effect on the RT Status Word, Block Status Word bits that will be set, RT Built-in-Test (BIT) Word bits, and interrupt requests that are issued and Interrupt Status Register bits that become set as a result of these conditions.

It should be noted that the responses to error conditions for Mode code messages are delineated separately, in TABLE 93.

TABLE 93. RT EXCEPTION CONDITIONS

	RT RESPONSE, EFFECT ON RT STATUS WORD REGISTER BITS	RT BLOCK STATUS WORD BITS (ASSUMING ENHANCED MODE)	RT BUILT-IN-TEST (BIT) WORD BITS	INTERRUPT CONDITIONS, INTERRUPT STATUS REGISTER BITS (IF ENABLED)
Invalid Command Word	No response (message ignored)	None (No SOM or EOM sequence)	No effect	None
RT Address Parity Error	RT will not receive words or respond to messages sent to its own RT address. RT will receive words to the broadcast address (31), unless BROADCAST DISABLED, bit 7 of Configuration Register #5, is logic '1." For a broadcast message, the Broadcast Command Received bit is set to logic "1" in the internal Status Word Register.	No Block Status Word for a message to the RT's own address. Normal Block Status Word, including EOM bit, for a broadcast message (if enabled).	None	RT ADDRESS PARITY ERROR
Command Type Sync in Data Word Following Reception of Valid Command Word	No response. MESSAGE ERROR bit set in internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, FORMAT ERROR, INCORRECT DATA SYNC, INVALID WORD	INCORRECT SYNC RECEIVED	END OF MESSAGE; FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE
Valid Command Word Followed by Reception of Invalid Data Word(s) (Manchester encoding, bit count, parity)	No response. MESSAGE ERROR bit set in internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, FORMAT ERROR, INVALID WORD	PARITY/ MANCHESTER ERROR RECEIVED	END OF MESSAGE; FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected)
Valid Command Word Followed by Incorrect Number of Data Words	No response. MESSAGE ERROR bit set in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, FORMAT ERROR, WORD COUNT ERROR	HIGH WORD COUNT or LOW WORD COUNT	END OF MESSAGE; FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected)
ACE/Mini-ACE is receiving RT in a correct RT-to-RT transfer sequence	Normal Status Word response. If the message was received to the broadcast address, the Broadcast Command Received bit is set to logic "1" in the internal Status Word Register.	EOM, RT-to-RT FORMAT	None	END OF MESSAGE; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected) (CHECK IF SELECTED)
RT-to-RT Timeout: ACE/Mini-ACE is Receiving RT in an RT-to-RT Transfer and the transmitting RT Does Not Respond in Time	No response. MESSAGE ERROR bit set in internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, NO RESPONSE TIMEOUT	RT-to-RT, NO RESPONSE ERROR	FORMAT ERROR; END OF MESSAGE; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected) (AT SET)
ENHANCED MODE CODE disabled or ENHANCED MODE	If the message is a Transmit Status or Transmit Last Command mode code, the RT Status Word resulting	EOM; if illegal command: ILLEGAL COMMAND	Any of the following may be set or cleared, as	RT SUBADDRESS CONTROL WORD; EOM (if Selected)

TABLE 93. RT EXCEPTION CONDITIONS				
	RT RESPONSE, EFFECT ON RT STATUS WORD REGISTER BITS	**RT BLOCK STATUS WORD BITS (ASSUMING ENHANCED MODE)**	**RT BUILT-IN-TEST (BIT) WORD BITS**	**INTERRUPT CONDITIONS, INTERRUPT STATUS REGISTER BITS (IF ENABLED)**
CODE HANDLING disabled; Receive valid, defined mode code message (including RESERVED mode codes).	from the previous message is transmitted and the internal Status Word is not updated. Otherwise, may affect the following RT Status Word bits, as applicable: MESSAGE ERROR (if illegal), BUSY (per Configuration Register #1 and Busy lookup table), DYNAMIC BUS CONTROL ACCEPTANCE, and TERMINAL FLAG. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register. The lookup table pointer value for subaddress 0 or 31 is stored in the third location of the message block descriptor. For a Transmit Last Command or Transmit BIT Word mode command (unless EXTERNAL BIT WORD is enabled), the Data Word transmitted is read from an internal register. For other mode commands with data, the Data Word is accessed from/to the location referenced by the lookup table pointer for subaddress 0 or 31.		applicable: TERMINAL FLAG INHIBITED, TRANSMITTER SHUTDOWN A, TRANSMITTER SHUTDOWN B.	
ENHANCED MODE enabled and ENHANCED MODE CODE HANDLING enabled; Receive valid, defined mode code message (including RESERVED mode codes).	If the message is a Transmit Status or Transmit Last Command mode code, the RT Status Word resulting from the previous message is transmitted and the internal Status Word is not updated. Otherwise, affects the following RT Status Word bits, as applicable: MESSAGE ERROR (if illegal), BUSY (per Busy lookup table), DYNAMIC BUS CONTROL ACCEPTANCE, and TERMINAL FLAG. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register. For a Transmit Last Command or Transmit BIT Word (unless EXTERNAL BIT WORD is enabled) mode command, the Data Word transmitted is read from an internal register. For other mode codes with data, the Data Word is accessed from/to the mode code Data Word table, address locations 0110-013F, which is mapped by broadcast, $T/\overline{R}$, and MC3-MC0. In addition, the Data Word received or transmitted will be stored in the third location in the message block descriptor.	EOM; if illegal command: ILLEGAL COMMAND	Any of the following may be set or cleared, as applicable: TERMINAL FLAG INHIBITED, TRANSMITTER SHUTDOWN A, TRANSMITTER SHUTDOWN B.	RT MODE CODE (if selected for the particular mode command by means of the Mode Code Selective Interrupt Table, locations 0108-010F); EOM
Loop Test Failure: The received version of a	If ENHANCED MODE is enabled and RTFAIL-RTFLAG WRAP ENABLE, bit 2 of Configuration Register #3 is	EOM, ERROR FLAG, LOOP TEST FAIL	LOOP TEST FAILURE A or LOOP TEST	FORMAT ERROR; EOM; RT SUBADDRESS

TABLE 93. RT EXCEPTION CONDITIONS				
	RT RESPONSE, EFFECT ON RT STATUS WORD REGISTER BITS	**RT BLOCK STATUS WORD BITS (ASSUMING ENHANCED MODE)**	**RT BUILT-IN-TEST (BIT) WORD BITS**	**INTERRUPT CONDITIONS, INTERRUPT STATUS REGISTER BITS (IF ENABLED)**
transmitted word was determined to be invalid (encoding, bit count, parity) and/or the received version of the last word transmitted did not match the transmitted version.	logic "1," the Terminal Flag Status Word bit will be set to logic "1" in response to the next nonbroadcast message.		FAILURE B	CONTROL WORD or RT MODE CODE (if selected)
Transmitter Timeout: The transmitter failsafe timer timed out after the ACE/Mini-ACE RT attempted to transmit for longer than 668 µs.	Response is terminated as a result of the timeout. If ENHANCED MODE is enabled and RTFAIL-RTFLAG WRAP ENABLE, bit 2 of Configuration Register #3, is logic "1," the Terminal flag Status Word bit will be set to logic "1" in response to the next nonbroadcast message. A Transmitter Timeout has no effect on the RT responding to subsequent messages.	EOM	TRANSMITTER TIMEOUT	EOM, RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected)
Handshake Failure: For a Start-of-Message (SOM) or Data Word (read or write) transfer sequence. Note that a handshake failure will not occur during an RT End-of-Message (EOM) sequence. In DMA mode, the host processor did not assert $\overline{\text{DTGRT}}$ in time (4.4 µs for 20MHz clock, 4 µs for a 16 MHz clock, 3.5 µs for a 12 MHz clock, 3.2 µs for 10 MHz clock), after the ACE/Mini-ACE asserted its $\overline{\text{DTREQ}}$ output or In transparent mode, the CPU kept $\overline{\text{STRBD}}$ asserted too long after the ACE/Mini-ACE asserted its $\overline{\text{READYD}}$ handshake output.	If the Handshake Failure occurs during the RT Start-of-Message (SOM) transfer sequence, the ACE/Mini-ACE terminates processing of the message: the message will be ignored, and therefore will not result in a descriptor being written to the stack. Storage of received Command Word and/or Data Words, or response of transmit Data Words is terminated as a result of the handshake timeout.	If the Handshake Failure occurred during the Start-of-Message (SOM) transfer sequence: NO bits will be set: that is, the message will be completely ignored. If the Handshake Failure occurs during a Data Word transfer sequence: EOM, ERROR FLAG	HANDSHAKE FAILURE	HANDSHAKE FAILURE
ENHANCED MODE and Valid receive Command Word received that has been illegalized by means of the illegalization table	The RT responds with the Message Error bit set. The Message Error bit is set to logic "1" in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register. If ILLEGAL RECEIVE TRANSFER DISABLE, bit 4 of Configuration Register #3, is set to logic "0," received Data Words are stored to the shared RAM. If ILLEGAL RECEIVE TRANSFER DISABLE is programmed to logic "1," received Data Words are not stored to the shared RAM.	EOM, ILLEGAL COMMAND WORD, FORMAT ERROR	None	RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); FORMAT ERROR; END OF MESSAGE

TABLE 93. RT EXCEPTION CONDITIONS				
	RT RESPONSE, EFFECT ON RT STATUS WORD REGISTER BITS	**RT BLOCK STATUS WORD BITS (ASSUMING ENHANCED MODE)**	**RT BUILT-IN-TEST (BIT) WORD BITS**	**INTERRUPT CONDITIONS, INTERRUPT STATUS REGISTER BITS (IF ENABLED)**
ENHANCED MODE and Valid transmit Command Word received that has been illegalized by means of the illegalization table	The RT responds with the Message Error bit set. No Data Words are transmitted. The Message Error bit is set to logic "1" in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ILLEGAL COMMAND WORD	None	RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE
ENHANCED MODE and RT is Busy for a valid receive Command (either globally, or in response to a particular valid receive command)	The RT responds with the Busy bit set. The Busy bit is set to logic "1" in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register. If BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3, is set to logic "0," received Data Words are stored to the shared RAM. If BUSY RECEIVE TRANSFER DISABLE is programmed to logic "1," received Data Words are not stored to the shared RAM.	EOM, ERROR FLAG, FORMAT ERROR	None	RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); FORMAT ERROR; END OF MESSAGE
ENHANCED MODE and RT is Busy for a valid Transmit Command (either globally, or in Response to a Particular Valid Transmit Command)	The RT responds with the Busy bit set. No Data Words are transmitted. The Busy bit is set to logic "1" in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ILLEGAL COMMAND WORD	None	RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE
ENHANCED MODE and the ACE RT is the receiving RT in an RT-to-RT transfer and: GAP CHECK ENABLED, bit 8 of Configuration Register #5, is programmed to logic "1" and the transmitting RT's response time gap is less than 2 µs, or Incorrect Sync Type or Format Error (encoding, bit count and/or parity) in the transmitting RT's Status Word, or The RT Address in the Transmitting RT's Status Word does not match the RT address in the transmit Command Word.	No RT response. The Message Error bit is set to logic "1" in the internal RT Status Word. If the message was received at the broadcast address, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, FORMAT ERROR, RT-RT GAP/SYNC/ ADDRESS ERROR	RT-RT GAP/SYNC/ ADDRESS ERROR	FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE

TABLE 93. RT EXCEPTION CONDITIONS				
	RT RESPONSE, EFFECT ON RT STATUS WORD REGISTER BITS	**RT BLOCK STATUS WORD BITS (ASSUMING ENHANCED MODE)**	**RT BUILT-IN-TEST (BIT) WORD BITS**	**INTERRUPT CONDITIONS, INTERRUPT STATUS REGISTER BITS (IF ENABLED)**
ENHANCED MODE and the ACE RT is receiving RT in RT-to-RT Transfer and: Error in Command Word to Transmitting RT: $T/\overline{R}$ bit = 0, or subaddress = 00000, or 11111, or same RT address as receive Command Word.	No RT response. The Message Error bit is set to logic "1" in the internal RT Status Word. If the message was received at the broadcast address, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, FORMAT ERROR, RT-RT SECOND COMMAND ERROR	RT-RT SECOND COMMAND WORD ERROR	FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE
ENHANCED MODE and ACE is Receiving RT for RT-to-RT Transfer and there is an error in the Transmitting RT's Response: sync or Manchester encoding, bit count, parity, and word count. This includes a response by the transmitting RT with the Message Error and/or Busy bits set to logic "1," followed by no Data Words.	No RT response. The Message Error bit is set to logic "1" in the internal RT Status Word. If the message was received at the broadcast address, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, FORMAT ERROR, and one of the following: WORD COUNT ERROR or INCORRECT DATA SYNC or INVALID WORD	One of the following (as appropriate): HIGH WORD COUNT or LOW WORD COUNT or INCORRECT SYNC RECEIVED or PARITY/ MANCHESTER ERROR RECEIVED	FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected): END OF MESSAGE
ENHANCED MODE and Command Word Contents Error: BROADCAST DISABLED is programmed to logic "0" and Command is a non-mode code transmit broadcast command, or BROADCAST DISABLED is programmed to logic "0" and message is a broadcasted -1553B mode code that is not permitted to be broadcast, or OVERRIDE MODE $T/\overline{R}$ ERROR is logic "0" and a Command Word has a $T/\overline{R}$ bit of 0, a subaddress/mode field of 00000 or 11111, and a mode code field between 00000 and 01111.	No RT response. The Message Error bit is set to logic "1" in the internal RT Status Word. If the message was a broadcast command, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, FORMAT ERROR, COMMAND WORD CONTENTS ERROR	COMMAND WORD CONTENTS ERROR	FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected): END OF MESSAGE
Superseded Message: RT receives an	The ACE RT will abort processing of the first (superseded) message and respond in full to the second	The Block Status Word stored during the Start-of-Message (SOM) sequence	None	There will be no interrupts following the first message. For the

TABLE 93. RT EXCEPTION CONDITIONS				
	RT RESPONSE, EFFECT ON RT STATUS WORD REGISTER BITS	**RT BLOCK STATUS WORD BITS (ASSUMING ENHANCED MODE)**	**RT BUILT-IN-TEST (BIT) WORD BITS**	**INTERRUPT CONDITIONS, INTERRUPT STATUS REGISTER BITS (IF ENABLED)**
incomplete message on one bus, followed by a gap with a maximum time of between 6 and 10 µs, followed by a new valid message on the same bus or alternate bus, or RT is responding to a transmit message on one bus and receives the start of a valid message on the alternate bus.	(superseding) message. If either message was broadcast, the Broadcast Command Received bit is set to logic "1" in the internal Status Word Register. If the second message was not a broadcast message, or a Transmit Status or Transmit Last Command mode code, the Broadcast Command Received bit in the internal RT Status Word Register is cleared to logic "0." If broadcast is enabled and the ACE RT receives a broadcast Command Word (RT address 31), followed contiguously by a Transmit Command Word to the ACE RT's own address, indicating an RT-to-RTs (broadcast) message, the broadcast Command Word will be superseded and the ACE RT will respond to the transmit command.	for the first message remains stored in the block descriptor for that (superseded) message. This word will have an EOM bit of logic "0" and an SOM bit of logic "1." The Block Status Word for the second message will be stored at an address four locations above (modulo the stack size) that of the Block Status Word for the first message. Assuming that the second message is not itself superseded, its Block Status Word will have an EOM bit of logic "1," and an SOM bit of logic "0". All other bits will be valid for the second message.		second message: RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE

6.17 SUMMARY OF RESPONSES TO MODE CODE MESSAGES

In the "1553B" Mode Codes configuration, the ACE/Mini-ACE implements all MIL-STD-1553B mode codes applicable to dual redundant bus operation. The ACE's responses to mode codes, including responses to various error conditions, are summarized in TABLE 94.

TABLE 94. MODE CODE SUMMARY

T/R BIT	MODE CODE	FUNCTION	DATA WORD	BROADCAST ALLOWED
0	00000-01111	Undefined (see Note 1)	No	No
1	00000	Dynamic Bus Control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	No
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag	No	Yes
1	00111	Override Inhibit Terminal Flag	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	01001-01111	RESERVED	No	TBD
1	10000	Transmit Vector Word	From Memory	No
0	10001	Synchronize with Data	To Memory (and, possibly, to Time Tag Register, see Note 2)	Yes
1	10010	Transmit Last Command	From Internal Register	No
1	10011	Transmit BIT Word	From Internal Register or RAM location (see Note 3)	No
0	10100	Selected Transmitter Shutdown (see Note 4)	To Memory	Yes
0	10101	Override Selected Transmitter Shutdown (see Note 4)	To Memory	Yes
0	10110-11111	RESERVED	Yes	TBD
1	10110-11111	RESERVED	Yes	TBD

Notes :

1) Receive mode commands 00000 through 01111 are undefined per MIL-STD-1553B. If the ACE/Mini-ACE RT is not in ENHANCED MODE or if OVERRIDE MODE CODE $T/\overline{R}$ BIT ERROR, bit 6 of Configuration Register #3, is programmed to logic "0," the ACE/Mini-ACE RT will not respond and the Message Error bit will be set in the internal Status Word Register. If the ACE/Mini-ACE is in ENHANCED MODE and OVERRIDE MODE CODE $T/\overline{R}$ BIT ERROR is programmed to logic "1," the ACE/Mini-ACE RT will treat the message as a RESERVED mode command. That is, it will respond with Status, with a Message Error bit of logic "0" (unless the command has been illegalized).

2) If LOAD TIME TAG ON SYNCHRONIZE, bit 5 of Configuration Register #2, is programmed to logic "1," the received Data Word is stored to the Time Tag Register.

3) In the non-ENHANCED mode, or if EXTERNAL BIT WORD ENABLE, bit 15 of Configuration Register #4, is programmed to logic "0," the BIT Word defined by TABLE 92 and stored in the ACE/Mini-ACE's BIT Word Register is transmitted. If the ACE/Mini-ACE is programmed for ENHANCED MODE (bit 15 of Configuration Register #15 is logic "1") and if EXTERNAL BIT WORD ENABLE is programmed to logic "1," the BIT Word transmitted will be read from a memory location. Refer to the section on the Transmit BIT Word mode command.

4) Terminal responds with Clear Status but no action is taken.

6.17.1 Detailed Functional Description of Mode Codes ("1553B" IMPLEMENTATION)

6.17.1.1 DYNAMIC BUS CONTROL (T/$\overline{R}$ = 1; 00000)

MESSAGE SEQUENCE = DBC----STATUS

The ACE/Mini-ACE responds with Status. If the host processor has written a logic "0" to the $\overline{\text{DB ACCEPT}}$ bit in Configuration Register #1 (bit 11), the DYNAMIC BUS CONTROL ACCEPTANCE bit will be logic "1" in the RT Status Word. If the ACE/Mini-ACE responds with the DYNAMIC BUS CONTROL ACCEPTANCE bit set, the ACE/Mini-ACE **remains in RT mode** until directed to switch to BC mode by the CPU.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Command Followed by Data Word. No Status response. Set Message error bit (Status Word), High Word Count (BIT Word).

3) $T/\overline{R}$ bit set to zero. No Status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

4) Zero $T/\overline{R}$ bit and Broadcast Address. No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).

5) Broadcast Address. No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).

6.17.1.2 SYNCHRONIZE WITHOUT DATA WORD (T/$\overline{R}$ = 1; 00001)

MESSAGE SEQUENCE = SYNC----STATUS

The ACE/Mini-ACE responds with Status. If sent as a broadcast, the Broadcast Received bit will be set and Status response suppressed. If the CLEAR TIME TAG ON SYNCHRONIZE option is enabled (bit 6 in Configuration Register #2 programmed to logic "1") the ACE will clear its internal time tag register to zero upon receipt of this mode code.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

3) $T/\overline{R}$ bit set to zero. No Status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

4) Zero T/$\overline{R}$ bit and Broadcast Address. No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).

6.17.1.3 TRANSMIT STATUS WORD (T/$\overline{R}$ = 1; 00010)

MESSAGE SEQUENCE = TRANSMIT STATUS----STATUS

The Status register is **not** updated before it is transmitted and contains the resulting status from the previous command (assuming that it was not a Transmit status or Transmit last command mode command).

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Command Followed by Data Word. No Status response. Set Message Error bit (Status Word)

3) T/$\overline{R}$ bit set to zero. No Status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

4) Zero T/$\overline{R}$ bit and Broadcast Address. No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).

5) Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Contents Error (BIT Word).

6.17.1.4 INITIATE SELF-TEST (T/$\overline{R}$ = 1; 00011)

MESSAGE SEQUENCE = SELF-TEST----STATUS

The ACE/Mini-ACE responds with Status. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. If the message was nonbroadcast, the normal Loopback self-test is performed on the transmitted Status Word. If the test fails, the Terminal flag bit is automatically set in the RT's internal Status Word Register. This result will be reflected in the status response to the **next** nonbroadcast message (assuming that the RTFAIL-RT FLAG WRAP ENABLE bit, bit 2, in Configuration Register #3 is programmed to logic "1"). The loopback self-test is completed approximately 5 µs after the mid-parity bit crossing of the transmitted Status Word.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

3) 3. T/$\overline{R}$ bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

4) Zero T/$\overline{R}$ bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

5) Loopback Test Fails. Set Terminal Flag bit in internal Status register (Status Word for next nonbroadcast command), Current Channel (A or B) Loop Test Failure and CH A/B Loop Test Failure (BIT Word), assert Rt Fail output.

6.17.1.5 TRANSMITTER SHUTDOWN (T/$\overline{R}$ = 1; 00100)

MESSAGE SEQUENCE = SHUTDOWN----STATUS

This command is only used with dual redundant bus systems. The ACE/Mini-ACE responds with Status. Following the Status transmission, the ACE/Mini-ACE inhibits any further transmission from the alternate redundant channel. Once shutdown, the transmitter can only be reactivated by an Override Transmitter Shutdown or Reset RT mode command, a Software Reset (writing logic "1" to bit 0 in the Start/Reset Register), or Hardware Reset (MSTRCLR input). Note that the receivers on both channels are always active, even when the transmitters are inhibited.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

3) T/$\overline{R}$ bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

4) Zero T/$\overline{R}$ bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

6.17.1.6 OVERRIDE TRANSMITTER SHUTDOWN (T/$\overline{R}$ = 1; 00101)

MESSAGE SEQUENCE = OVERRIDE SHUTDOWN----STATUS

This command is only used with dual redundant bus systems. The ACE/Mini-ACE responds with Status. At the end of the Status transmission, the ACE/Mini-ACE reactivates the transmitter of the alternate redundant bus. If the command was broadcast, the Broadcast Command Received Status Word bit is set and status transmission is suppressed.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

3) T/$\overline{R}$ bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

4) Zero T/$\overline{R}$ bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

6.17.1.7 INHIBIT TERMINAL FLAG BIT (T/$\overline{R}$ = 1; 00110)

MESSAGE SEQUENCE = INHIBIT TERMINAL FLAG----STATUS

The ACE/Mini-ACE responds with Status and inhibits further setting of the Terminal Flag bit in its internal Status Word register. Once the Terminal Flag has been inhibited, it can only be reactivated by an Override Inhibit Terminal Flag or Reset RT mode code commands, or by Reset. If the command was broadcast, the Broadcast Received bit is set, the state of the Terminal Flag bit in the internal Status Word register remains unchanged and Status transmission is suppressed.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

3) T/$\overline{R}$ bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

4) Zero T/$\overline{R}$ bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

6.17.1.8 OVERRIDE INHIBIT TERMINAL FLAG BIT (T/$\overline{R}$ = 1; 00111)

MESSAGE SEQUENCE = OVERRIDE INHIBIT TERMINAL FLAG----STATUS

The ACE/Mini-ACE responds with Status and re-enables the Terminal Flag bit in its internal Status register. If the command was a broadcast, the Broadcast Command Received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

3) T/$\overline{R}$ bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

4) Zero T/$\overline{R}$ bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

6.17.1.9 RESET REMOTE TERMINAL (T/$\overline{R}$ = 1; 01000)

MESSAGE SEQUENCE = RESET REMOTE TERMINAL----STATUS

The ACE/Mini-ACE responds with Status and internally resets. The Message Error and Broadcast Command Received bits of the internal Status register are reset to 0. The internal BIT Word Register is reset to 0. If either of the 1553 transmitters has been shut down, the shutdown condition is overridden. If the Terminal Flag bit has been inhibited, the inhibit is overridden. The receipt of this command **does not** reset any of the ACE's host programmable registers.

If the command is received as a broadcast, the Broadcast Command Received bit is set and the Status Word is suppressed. Also, if the command is received as a broadcast and the Terminal Flag bit had been set as a result of the Loopback test of the previous message, the Terminal Flag bit is not reset to zero. The resulting operation is completed approximately 8 µs after the mid-parity bit crossing of the Reset mode code command.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

3) T/$\overline{R}$ bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

4) Zero T/$\overline{R}$ bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

6.17.1.10 RESERVED MODE CODES (T/$\overline{R}$=1; 01001 - 01111)

MESSAGE SEQUENCE = RESERVED MODE CODES----STATUS

The ACE/Mini-ACE responds with status. If the command has been illegalized by means of the illegalization table, the Message Error Status Word bit will be set.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

3) T/$\overline{R}$ bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

4) Zero T/$\overline{R}$ bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

*6.17.1.11 TRANSMIT VECTOR WORD (*T/$\overline{R}$ *= 1; 10000)*

MESSAGE SEQUENCE = TRANSMIT VECTOR WORD---- STATUS/VECTOR WORD

The ACE/Mini-ACE transmits a Status Word followed by a Vector Word. If the ENHANCED MODE CODES are enabled (bit 15 in Configuration Register #3 set to logic "1") the contents of the Vector Word are obtained from RAM location 120 (hex). If ENHANCED MODE CODES are not enabled, the single word data block in the shared RAM that is referenced by the lookup table pointer for transmit subaddress 00000 or 11111.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Correct Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

3) T/$\overline{R}$ bit set to zero, no Data Word. No Status response. Set Message Error bit (Status Word), and Low Word Count (BIT Word).

4) T/$\overline{R}$ bit set to zero plus one Data Word. The ACE will respond with Status. The Data Word will be stored in RAM location 0110 (or single-word data block for subaddress 0000 or 1111).

5) Zero T/$\overline{R}$ bit and Broadcast Address, no Data Word. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), and Low Word Count (BIT word).

6) Zero T/$\overline{R}$ bit and Broadcast Address, plus one Data Word. No Status response. Set Broadcast Command Received bits (Status Word).

7) Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Word Contents Error (BIT word).

6.17.1.12 SYNCHRONIZE WITH DATA WORD (T/$\overline{R}$ = 0; 10001)

MESSAGE SEQUENCE = SYNCHRONIZE COMMAND/DATA WORD----STATUS

If the ENHANCED MODE CODES are enabled (bit 15 in Configuration Register #3 set to logic "1") the received data word is stored in RAM location 0111 (hex). If ENHANCED MODE CODES are not enabled, the word is stored in the single-word data block in the shared RAM referenced by receive subaddress 00000 or 11111 in the lookup table. If the LOAD TIME TAG ON SYNCHRONIZE option is enabled (bit 5 in Configuration Register #2 set to logic "1"), the ACE/Mini-ACE will load the received 16 bit Data Word into its internal Time Tag Register upon receipt of this mode command.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Correct Command not followed by Data Word. No Status response. Set Message Error bit (Status Word), Low Word Count (BIT Word).

3) Command Followed by too many Data Words. No Status response. Set Message Error bit (Status Word), High Word Count (BIT word).

4) Command T/$\overline{R}$ bit set to one followed by Data Word. No Status response. Set Message Error bit (Status Word), and High Word Count (BIT Word).

5) Command T/$\overline{R}$ bit set to one not followed by Data Word. The ACE/Mini-ACE replies with Status plus one Data Word. The Data Word is read from RAM location 121 hex (or single-word data block for subaddress 0000 or 1111).

6) Command T/$\overline{R}$ Bit set to one and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word); Set Command Word Contents Error (BIT word).

6.17.1.13 TRANSMIT LAST COMMAND (T/$\overline{R}$ = 1; 10010)

MESSAGE SEQUENCE = TRANSMIT LAST COMMAND----STATUS/LAST COMMAND

The Status register is not updated before transmission. It contains the Status from the previous command. The Data Word transmitted contains

the previous valid command (providing it was not another TRANSMIT LAST COMMAND mode command).

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Correct Command followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count Error (Bit Word).

3) T/$\overline{R}$ Bit set to zero, no Data Word. No Status response. Set Message Error bit (Status Word), Low Word Count (BIT Word).

4) T/$\overline{R}$ bit set to zero plus one Data Word. The ACE/Mini-ACE will respond with Status. The Data Word is transferred to RAM location 0112 (or single-word data block for subaddress 0000 or 1111).

5) Zero T/$\overline{R}$ Bit and Broadcast Address, no Data Word. No Status response. Set Message Error and Broadcast Received bits (Status Word), Low Word Count Error(BIT Word).

6) Zero T/$\overline{R}$ bit and Broadcast Address, one Data Word. No Status response. Set Broadcast Received Bit (status word). The Data Word is transferred to RAM location 0132 (or single-word data block for subaddress 0000 or 1111).

7) Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Word Contents Error (BIT Word).

6.17.1.14 TRANSMIT BIT WORD (T/$\overline{R}$ = 1; 10011)

MESSAGE SEQUENCE = TRANSMIT BIT WORD----STATUS/BIT WORD

The ACE/Mini-ACE responds with Status followed by the Built-in Test (BIT) word. In the NON-ENHANCED mode, or if EXTERNAL BIT WORD ENABLE, bit 15 of Configuration Register #4, is programmed to logic "0," the BIT Word transmitted is accessed from the ACE's internal BIT Word register. This word is defined in TABLE 92.

If the ACE/Mini-ACE is programmed for ENHANCED MODE (bit 15 of Configuration Register #15 is logic "1") **and** if EXTERNAL BIT WORD ENABLE is programmed to logic "1," the BIT Word transmitted will be read from a memory location. In this case, if ENHANCED MODE CODES are disabled (ENHANCED MODE disabled **or** ENHANCED MODE HANDLING disabled [bit 0 of Configuration Register #3 is

programmed to logic "0"]), the location accessed for the external BIT Word will be the address referenced by the RT lookup table pointer for subaddress 00000 or subaddress 11111. In this case, it should be noted that for a given subaddress (00000 or 11111), the **same** Data Word will be transmitted in response to either a Transmit BIT Word **or** Transmit vector word mode command.

If ENHANCED MODE CODES are enabled (ENHANCED MODE **and** ENHANCED MODE HANDLING enabled (bits 15 and 0 of Configuration Register #3 are programmed to logic "1"), the external BIT Word will be accessed from address location 0123.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Correct Command followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count Error (Bit Word).

3) $T/\overline{R}$ Bit set to zero, no Data Word. No Status response. Set Message Error bit (Status Word), Low Word Count (BIT Word).

4) $T/\overline{R}$ bit set to zero plus one Data Word. The ACE will respond with Status. The Data Word is transferred to RAM address 0113 (or single-word data block for subaddress 0000 or 1111).

5) Zero $T/\overline{R}$ Bit and Broadcast Address, no Data Word. No Status response. Set Message Error and Broadcast Received bits (Status Word), Low Word Count Error(BIT Word).

6) Zero $T/\overline{R}$ bit and Broadcast Address, one Data Word. No Status response. Set Broadcast Received Bit (status word). The Data Word is transferred to RAM location 0133 (or single-word data block for subaddress 0000 or 1111).

7) Broadcast Address. No Status response. Set Message Error and Broadcast Command received bits (Status Word), Command Word contents Error (BIT Word).

6.17.1.15 SELECTED TRANSMITTER SHUTDOWN ($T/\overline{R}$ *= 0; 10100)*

MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN/DATA----STATUS

The Data Word received is transferred to the RAM and Status is transmitted. If ENHANCED MODE CODES are not enabled, the Data Word is written to the single-word data block referenced by the lookup table pointer for subaddress 00000 or 11111. If ENHANCED MODE

CODES are enabled, the Data Word is stored at hex location 0114. No other action is taken by the ACE. No transmitters are shut down as a result of this mode command. This command is intended for use with RTs with more than one dual redundant channel. If the command was a broadcast, the Broadcast Command Received bit is set and Status transmission is suppressed.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Correct Command not followed by Data Word. No Status response. Set Message Error bit (Status Word), and Low Word Count Bit (BIT Word).

3) Command followed by too many Data Words. No Status response. Set Message Error bit (Status Word), and High Word Count Bit (BIT Word).

4) Command $T/\overline{R}$ bit Set to one followed by one Data Word. No Status response. Set Message Error bit (Status Word), and High Word Count (BIT Word).

5) Command $T/\overline{R}$ bit set to one not followed by Data Word. The ACE replies with Status plus one Data Word. The Data Word is read from hex RAM location 0124 (or single-word data block for subaddress 0000 or 1111).

6) Command $T/\overline{R}$ Bit Set to One and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), and Command Contents Error (BIT Word).

6.17.1.16 OVERRIDE SELECTED TRANSMITTER SHUTDOWN (T/$\overline{R}$ = 0; 10101)

MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN/DATA----STATUS

The Data Word received is transferred to the RAM. If ENHANCED MODE CODES are disabled, the single-word data block is referenced by the lookup table pointer for subaddress 00000 or 11111. If ENHANCED MODE CODES are enabled, the Data Word is stored in hex RAM location 0115. No transmitters that have been previously shut down are reactivated as a result of this command. No other action is taken by the ACE/Mini-ACE. This command is intended for use with RTs with more than one dual redundant channel. If the command was a broadcast, the Broadcast Command Received bit is set and Status transmission is suppressed.

ERROR CONDITIONS

1) Invalid Command. No response, command ignored.

2) Command not followed by Data Word. No Status response. Set Message Error bit (Status Word), and Low Word Count (BIT Word).

3) Command followed by too many Data Words. No Status response. Set Message Error bit (Status Word), and High Word Count bit (BIT Word).

4) Command $T/\overline{R}$ bit Set to one followed by Data Word. No Status response. Set Message Error bit (Status Word), and High Word Count (BIT Word).

5) Command $T/\overline{R}$ bit Set to one not followed by Data Word. The ACE replies with Status plus one Data Word. The Data Word is read from hex RAM location 0125 (or single-word data block for subaddress 0000 or 1111).

6) Command $T/\overline{R}$ Bit Set to one and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Word Contents (BIT Word).

6.17.1.17 RESERVED MODE CODES (T/$\overline{R}$ = 0; 10110 - 11111)

(T/$\overline{R}$ = 1; 10110 - 11111)

MESSAGE SEQUENCE = RESERVED MODE CODE (T/R = 1)----STATUS/DATA = RESERVED MODE CODE (T/R = 0)/DATA----STATUS

For a RESERVED receive Command, the ACE/Mini-ACE stores the Data Word to the shared RAM. If the command was a broadcast, the Broadcast Command Received bit is set and Status transmission is suppressed. For a RESERVED transmit Command Word, the ACE responds with Status plus a single Data Word. The Data Word is read from the shared RAM. The shared RAM locations are referenced by the lookup table pointers for subaddresses 0 and 31 if ENHANCED MODE CODES are disabled. If ENHANCED MODE CODES are enabled, the RAM location accessed are 0116-001F for received mode codes, 0126-012F for transmit mode codes, or 0136-013F for broadcast mode codes.

ERROR CONDITIONS (T/R = 1)

1) Invalid Command. No response, command ignored.

2) Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

3) Broadcast Command. No Status response. Set Message Error bit (status word), and Command Word Contents Error (BIT Word).

ERROR CONDITIONS (T/R = 0)

1) Invalid Command. No response, command ignored.

2) Command not followed by contiguous Data Word. No Status response. Set Message Error bit (Status Word), and Low Word Count (BIT Word).

3) Command followed by too many Data Words. No Status response. Set Message Error bit (Status Word), and High Word Count (BIT word).

6.18 RT SOFTWARE INITIALIZATION PROCEDURE

The following software sequence is typical of the steps the host CPU should perform following power turn-on to configure the ACE/Mini-ACE for RT operation. For most applications, it is possible to skip many of the steps indicated.

1) Perform a software reset, by writing 0001 (hex) to the Start/Reset Register.

2) If any of the Enhanced mode functions (e.g., subaddress double buffering) are to be used, invoke the ACE/Mini-ACE RT's ENHANCED MODE by writing 8000 (hex) to Configuration Register #3.

3) Initialize the Interrupt Mask register. For many RT applications, the EOM interrupt will generally be enabled. In other instances, the RT SUBADDRESS CONTROL WORD, RT CIRCULAR BUFFER ROLLOVER, RT MODE CODE and/or FORMAT ERROR Interrupt Requests may also be enabled. The RT SUBADDRESS CONTROL WORD interrupt enables interrupt requests to be issued following messages to specified transmit, receive, or broadcast subaddresses. The RT MODE CODE interrupt enables interrupt requests to be programmed for individual mode code commands. The RT CIRCULAR BUFFER ROLLOVER interrupt may be used to provide an interrupt request following a multimessage reception or transmission of a specified number of Data Words to/from a given subaddress.

4) Load the starting location of the Stack into the Active Area Stack Pointer location in RAM.

5) As an option, initialize the Active Area Stack. If there is a desire to poll the Stack RAM while 1553 messages are being processed, the Block Status Word locations for the respective message block descriptors (relative address locations 0, 4, 8...[stack size -4] in the stack) should be cleared to 0000. A Block Status Word of 0000 (SOM = EOM = 0) indicates that a message has not yet been processed.

6) Initialize the Active Area Lookup Table. The Lookup Table address for each transmit, receive, and (optionally) broadcast subaddress should be initialized as the pointer value for each respective lookup table. If the RT is going to be used in the ENHANCED RT MEMORY MANAGEMENT mode, it will also be necessary to select the memory management and interrupt options for each subaddress by initializing the Subaddress Control Words for the Active Area.

   If there are several unused subaddresses for an RT, it is recommended that the Lookup Table pointers for these be initialized to the same value in order to conserve memory space.

7) If ENHANCED MODE CODE HANDLING (bit 0 of Configuration Register #4) is not used, the pointers for receive subaddresses 0 and 31 (for Synchronize with Data messages) generally get loaded with the same pointer value. Similarly, the Lookup Table addresses for transmit subaddresses 0 and 31 (for Transmit Vector Word messages) generally get loaded with the same pointer value.

   If ENHANCED MODE CODE HANDLING is enabled, Data Words for these mode codes are stored in locations 0111 (for Synchronize with data) and 0130 (for Transmit Vector Word).

8) Initialize Configuration Register #2. This involves selecting use of the of the following functions: ENHANCED RT MEMORY MANAGEMENT should be selected if it is desirable to select the circular buffer feature and/or subaddress double buffering features on an individual subaddress basis. SEPARATE BROADCAST should be set if it is necessary to comply to Notice 2 for broadcast messages. This enables **separate** lookup table pointers for nonbroadcast received and broadcast receive messages.

   For RT mode, 256-WORD BOUNDARY DISABLE should normally be programmed to logic "0." If this bit is programmed to logic "1," it should be noted that the size of **all** circular buffers becomes **64K** words.

   The three TIME TAG RESOLUTION bits should be programmed to select the desired resolution for the time tag register. The choices are 2, 4, 8, 16, 32, or 64 µs/LSB, or "EXTERNAL" (external clock). CLEAR TIME TAG ON SYNCHRONIZE should be programmed to logic "1" if it is desired to clear the time tag to 0000 following receipt of a synchronize (without data) mode code. Similarly, LOAD TIME TAG ON SYNCHRONIZE should be programmed to logic "1" if it is desired to load the time tag to the value of the received Data Word following receipt of a synchronize with data mode code.

   ENHANCED INTERRUPTS should be enabled if the CPU needs to poll using the Interrupt Status Register and/or it is desired that one or more of the following conditions cause an interrupt: TRANSMITTER TIMEOUT, RT COMMAND STACK ROLLOVER, or RT MODE CODE interrupt. INTERRUPT STATUS AUTO CLEAR should be programmed to logic "1" if it is desired to automatically clear the Interrupt Status Register and the ACE's $\overline{\text{INT}}$ output (for a "level" type interrupt output) after the Interrupt Status Register has been read. LEVEL/$\overline{\text{PULSE}}$ INTERRUPT REQUEST should be programmed to logic "0" for a pulse type interrupt (500 ns) or to logic "1" for a level type interrupt.

   CLEAR SERVICE REQUEST should be programmed to logic "1" if it is desired to automatically clear the Service Request Status Word bit

following reception of a Transmit vector word mode command.

OVERWRITE INVALID DATA should be set to logic "1" if the circular buffer mode is used with one or more subaddresses. SUBADDRESS DOUBLE BUFFERING should be enabled, if desired. BUSY LOOKUP TABLE ENABLE should be logic "1" if there is a need for the Busy bit in the RT Status Word to be set for particular T/$\overline{R}$/Bcst subaddresses.

9) Initialize Configuration Register #3. If one or more of the ENHANCED MODE features are to be used, **bit 15 must be maintained at logic "1."** The RT Stack size is programmable with choices of 256 words (default, 64 messages), 512, 1024, or 2048 words (512 messages) by bits 14 and 13. Other RT features that may be selected by this register include ILLEGALIZATION (default = "0" = enabled), ALTERNATE STATUS (allowing software programming of **all 11** Status Word bits), the choice of storing or not storing words for illegal or "BUSY" messages, and ENHANCED MODE CODE HANDLING.

   If enhanced mode code handling is selected, Data Words for mode codes are stored in address locations 0110-013F, and interrupt requests for individual mode codes may be enabled by means of a table in address locations 0108-010F. Other RT options selectable by Configuration Register #3 include 1553A MODE CODES ENABLED, and RTFAIL/$\overline{\text{RTFLAG}}$ WRAP ENABLED. 1553A MODE CODES ENABLED causes only subaddress 00000 to be treated as a mode code subaddress. RTFAIL/$\overline{\text{RTFLAG}}$ WRAP ENABLE causes the RT FLAG Status bit to be automatically set following a failure of the loop test. OVERRIDE MODE CODE T/R ERROR should only be programmed to logic "1" if receive Mode Codes 0000 through 01111 are to be treated as defined mode codes.

10) Initialize Configuration Registers #4. If EXTERNAL BIT WORD ENABLE is logic "1," the Data Word for a Transmit BIT Word mode command is accessed from a shared RAM location, rather than from an internal register. If ENHANCED MODE CODES are not enabled, the RAM location for the external BIT Word is the location pointed to by the lookup table pointer for subaddress 0 or 31. If ENHANCED MODE CODES are enabled, the external BIT Word is stored in location 0123.

    INHIBIT BIT WORD IF BUSY prevents the BIT Word from being transmitted if the RT is Busy. If MODE CODE OVERRIDE BUSY is logic "1," this enables the ACE/Mini-ACE RT to transmit a Data Word in response to a Transmit Vector Word or Reserved transmit mode command, even if the RT is busy.

    For the BU-65171, BU-61581, BU-61586, BU-65620, and BU-61590 versions of the ACE/Mini-ACE, LATCH RT ADDRESS WITH C.R. #5 allows the ACE's RT Address to be software programmable by means of

bits 5 through 0 of Configuration Register #5. If LATCH RT ADDRESS WITH C.R. #5 is logic "1," writing to Configuration #5 causes the RT Address to be read from pins RTAD4-0 and RTADP and latched internally. After the RT Address has been programmed, it is suggested that LATCH RT ADDRESS WITH C.R. #5 be cleared to logic "0" to prevent an erroneous overwrite.

11) Initialize Configuration Register #5. As explained in step (10), for some versions of the ACE/Mini-ACE, the RT Address may be programmable by means of bits 5 through 0.

    The default clock frequency for the ACE/Mini-ACE is 16 MHz (20 MHz for BU-61689). To select 12 MHz or 10 MHz operation, 12 MHZ CLOCK SELECT (10MHz CLOCK SELECT for BU-61689), Bit 15 of Configuration Register #5, must be programmed to logic "1." For the BU-65179, the clock selection must be pin selectable for either 10, 12, 16, or 20 MHz clock frequency by using address bit A15/A14 (refer to the programming of Configuration Register #5 in the Software Interface section of this manual for additional details on the setting of clock frequency operation).

    EXPANDED ZERO-CROSSING should be set to logic "1" to expand the Manchester decoders' tolerance for zero crossing distortion by enabling a sampling rate of 32 MHz (for 16 MHz clock) or 24 MHz (for 12 MHz clock). **Note** that for the Mini-ACE series terminals (BU-65178/79, BU-61588, and BU-61688/89), the EXPANDED ZERO-CROSSING is **always** internally enabled. RESPONSE TIMEOUT SELECT 1-0 selects the time value for the RT-to-RT response timeout from among 18.5 µs (default), 22.5, 50.5, or 130 µs. If GAP CHECK ENABLED is programmed to logic "1," the RT will verify for a minimum bus dead time of 2 µs prior to the transmitting RT's response in an RT-to-RT transfer, where the ACE/Mini-ACE RT is the receiving RT.

12) If RT Illegalization is used, the CPU should initialize the Illegalization Table, address locations 0300-03FF.

13) If the BUSY LOOKUP TABLE is enabled, select the desired subaddresses to be busy by programming the Busy table, address locations 0240 through 0247.

14) If ENHANCED INTERRUPTS are enabled **and** ENHANCED MODE CODE HANDLING is enabled, interrupts for selective mode code messages may be enabled by programming locations 0108 through 010F.

15) Data to be transmitted on the 1553 bus (in response to transmit commands) should be written into the appropriate data blocks. As an option, the locations for Data Words for anticipated receive Data Words

may be initialized to zero.

16) To configure the ACE/Mini-ACE as an on-line RT, write to Configuration Register #1, setting bit 15 (MSB) to logic "1" and bit 14 to logic "0." The current active area is selected by the setting of bit 13 (0 for A, 1 for B). If ALTERNATE RT STATUS is not enabled, bits 11 through 8 should be initialized to select the values for the RT Status Word bits Dynamic Bus Control Acceptance, Busy, Service Request, and Subsystem Flag. Also, in the ENHANCED mode, the RT flag Status Word bit is programmable by bit 7. These bits must be programmed for the **logical inverse** of their desired values in the RT Status Word.

    If ALTERNATE RT STATUS is enabled, bits 10 through 0 of the ACE/Mini-ACE's RT Status Word are programmable via bits 11 through 1 of Configuration Register #1. In this case, the **logical values** (non-inverted) of the intended Status Word bit values must be programmed.

6.19 RT PSEUDO CODE EXAMPLE

The following example illustrates the programming steps necessary to initialize the ACE/Mini-ACE Remote Terminal registers and memory, and place the RT in its on-line state.

The example illustrates the initialization of four subaddresses plus mode codes.

The four subaddresses are:

1) Subaddress 1, transmitting; single message mode, enabling TX:EOM interrupt

2) Subaddress 7, receiving (and broadcast); 1024-word circular buffer mode, enabling RX:CIRCULAR BUFFER ROLLOVER and BCST:CIRCULAR BUFFER ROLLOVER interrupts

3) Subaddress 19, receiving (and broadcast); double buffered mode, enabling RX:EOM and BCST:EOM interrupts

4) Subaddress 30, receiving, broadcast, and transmitting (wraparound subaddress); single message mode, no interrupts enabled

ENHANCED MODE will be enabled to allow use of the full ACE/Mini-ACE RT functionality.

ENHANCED INTERRUPTS are enabled. Interrupts for RT SUBADDRESS CONTROL WORD, RT CIRCULAR BUFFER ROLLOVER, RT MODE CODE, and FORMAT ERROR are enabled.

BROADCAST SEPARATION is implemented.

ENHANCED MEMORY MANAGEMENT and OVERWRITE INVALID DATA are enabled, and 256-WORD BOUNDARY DISABLED is disabled, allowing the proper use of circular buffers for subaddress 7.

Time Tag Resolution of 64 µs/LSB (default) is selected.

Busy by subaddress is enabled. However, all subaddresses are initially programmed as "not busy."

A loopback test failure will cause the RTFLAG bit to become set.

Received Data Words will not be stored for nonmode messages, but will be stored for mode code messages.

ENHANCED MODE CODE HANDLING will be enabled. As such, individual address locations are allocated for Data Words for Synchronize with data and Transmit vector word mode commands. In addition, interrupts are enabled for the Synchronize (with and without data), Reset, and Self-test mode commands. Interrupts are also enabled for those commands received to the broadcast address.

The example assumes that a version of the ACE/Mini-ACE allowing a software programmable RT Address is used (e.g., BU-65171/61581), and that the ACE/Mini-ACE's RT Address inputs are connected to the CPU data bus bits 5 through 0 to allow this. An RT Address of seven (7) is assigned.

The ACE/Mini-ACE is initialized for a 12 MHz clock input, with GAP CHECKING and EXPANDED ZERO CROSSING enabled.

All used subaddresses, as well as all MIL-STD-1553B mode codes except Selected transmitter shutdown and override, are programmed as legal. This includes the associated broadcast commands, where appropriate. All unused subaddresses and mode codes, and undefined and reserved mode codes are illegalized.

The (single) 32-word Data Word Block for transmit subaddress 1 is initially loaded with a pattern of 0000, 0001, ...001F.

The values of all RT Status Word bits are initialized to 0.

TABLE 95 illustrates the memory map to initialize for the subaddresses, mode codes, and other conditions described above.

TABLE 95. MEMORY MAP FOR RT EXAMPLE PSEUDO CODE			
ADDRESS	**DATA**	**DESCRIPTION**	**PORTION OF MEMORY, COMMENT**
0000 0004 • • • 00FC	0000 0000 • • • 0000	Block Status Word location for Message #0 • • • • Block Status Word location for Message #63	Stack Area. Note that the locations allocated for anticipated Block Status Words, stored by the ACE in every fourth location (0000, 0004, ...00FC) at the start and end of messages, are initialized to 0000.
0100	0000	Area A (active area) Stack Pointer	Fixed Location
0108	0000	No interrupts for receive mode codes 0-15	Mode code interrupts
0109	0002	Enable interrupts for receive mode code: Synchronize with data	
010A	010A	Enable interrupts for transmit mode codes: Synchronize (without data), Reset RT, Self-Test	
010B	0000	No interrupts for transmit mode codes 16-31	
010C	0000	No interrupts for broadcast receive mode codes 0-15	
010D	0000	Enable interrupts for broadcast receive mode code: Synchronize with data	
010E	010A	Enable interrupts for broadcast transmit mode codes: Synchronize without data, Reset RT, Self-test	
010F	0000	No interrupts for transmit broadcast mode codes 16-31	
0111	0000	Reserved for received Data Word for Synchronize with data mode command	Mode code Data Words (since ENHANCED MODE CODES are enabled)
0120	1234	Data Word for Transmit vector word mode code initialized to 1234	
0147	0800	Receive subaddress 7	RT lookup table. Note that for the wraparound subaddress, (30, in accordance with the recommendation in MIL-STD-1553B Notice 2), the same pointer value (0480) is used for transmit, receive, and broadcast receive messages. Also, note that a pointer value of 04E0 should be assigned for all unused subaddresses (not shown).
0153	0440	Receive subaddress 19	
0161	0400	Transmit subaddress 1	
015E	0480	Receive subaddress 30	
017E	0480	Transmit subaddress 30	
0187	0C00	Broadcast receive subaddress 7	
0193	04A0	Broadcast receive subaddress 19	
019E	0480	Broadcast receive subaddress 30	
01A1	4000	Subaddress 1. Programmed for single message transmit buffer. TX:EOM interrupt enabled.	RT Subaddress Control Words. Note that a value of 0000 should be assigned to the Subaddress Control Words for all unused subaddresses not shown).
01A7	018C	Subaddress 7. 1024-word circular buffer programmed for receive and broadcast receive. RX:CIRCULAR BUFFER ROLLOVER and BCST:CIRCULAR BUFFER ROLLOVER interrupts enabled.	
01B3	8210	Subaddress 19. Programmed for double buffered receive and broadcast receive operation. RX:EOM and BCST:EOM interrupts enabled.	
01BE	0000	Subaddress 30. Data wraparound subaddress. Programmed for single message operation for transmit, receive, and broadcast receive operation. No interrupts enabled.	
0240 • • 0247	0000 • • 0000	All subaddresses initialized as “not busy”	Subaddress Busy Table
0300	FFFF	Subaddress 0, broadcast receive mode codes. Only Synchronize (with data) is legal.	Command illegalization Table. Note that only used subaddress and mode codes are

TABLE 95. MEMORY MAP FOR RT EXAMPLE PSEUDO CODE			
ADDRESS	**DATA**	**DESCRIPTION**	**PORTION OF MEMORY, COMMENT**
0301	FFFD		legalized. All unused subaddresses and mode codes are illegalized.
0302-030D	FFFF	Broadcast receive subaddress 1-6 illegal	
030E-030F	0000	Broadcast receive subaddress 7 legal	
0310-0325	FFFF	Broadcast receive subaddress 8-18 illegal	
0326-0327	0000	Broadcast receive subaddress 19 legal	
0328-033B	FFFF	Broadcast receive subaddress 20-29 illegal	
033C-033D	0000	Broadcast receive subaddress 30 legal	
033E	FFFF	Subaddress 31, broadcast receive mode codes. Only Synchronize (without data) is legal.	
033F	FFFD		
0340	FE05	Subaddress 0, broadcast transmit mode codes. Synchronize (without data), Initiate self-test, Transmitter shutdown, Override transmitter shutdown, Inhibit terminal flag bit, Override inhibit terminal flag bit, and Reset remote terminal are legal.	
0341	FFFF		
0342-037D	Don't need to program (nonmode code broadcast transmit commands)		
037E	FE05	Subaddress 31, broadcast transmit mode codes. Synchronize (without data), Initiate self-test, Transmitter shutdown, Override transmitter shutdown, Inhibit terminal flag bit, Override inhibit terminal flag bit, and Reset remote terminal are legal.	Command illegalization Table. Note that only used subaddress and mode codes are legalized. All unused subaddresses and mode codes are illegalized.
037F	FFFF		
0381	FFFD		
0382-038D	FFFF	Nonbroadcast subaddresses 1-6 illegal.	
038E-038F	0000	Receive subaddress 7 legal	
0390-03A5	FFFF	Nonbroadcast receive subaddresses 8-18 illegal.	
03A6-03A7	0000	Nonbroadcast receive subaddress 19 legal	
03A8-03BB	FFFF	Nonbroadcast receive subaddresses 20-29 illegal	
03BC-03BD	0000	Receive subaddress 30 legal	
03BE	FFFF	Subaddress 31, nonbroadcast receive mode codes. Only Synchronize (with data) is legal.	
03BF	FFFD		
03C0	FE00	Subaddress 0, nonbroadcast transmit mode codes. Dynamic bus control, Synchronize (without data), Transmit status word, Initiate self-test, Transmitter shutdown, Override transmitter shutdown, Inhibit terminal flag bit, Override inhibit terminal flag bit, Reset remote terminal, Transmit vector word, Transmit last command, and Transmit BIT word are legal.	
03C1	FFF2		
03C2-03C3	0000	Nonbroadcast transmit subaddress 1 legal	
03C4-03FB	FFFF	Nonbroadcast transmit subaddresses 2-29 illegal	
03FC-03FD	0000	Transmit subaddress 30 legal	
03FE	FE00	Subaddress 31, nonbroadcast transmit mode codes. Dynamic bus control, Synchronize (without data), Transmit status word, Initiate self-test, Transmitter shutdown, Override transmitter shutdown, Inhibit terminal flag bit, Override inhibit terminal flag bit, Reset remote terminal, Transmit vector word, Transmit last command, and Transmit BIT word are legal.	
03FF	FFF2		

TABLE 95. MEMORY MAP FOR RT EXAMPLE PSEUDO CODE			
ADDRESS	**DATA**	**DESCRIPTION**	**PORTION OF MEMORY, COMMENT**
0400 0401 0402 • • 041F	0000 0001 0002 • • 001F	Data Words stored (“walking pattern” 0000 to 001F) to be transmitted for transmit subaddress 1.	RT Data Word tables.
0440-045F	----	Reserved for “Block 0” (double buffered) for receive subaddress 19	
0460-047F	----	Reserved for “Block 1” (double buffered) for receive subaddress 19	
0480-049F	----	Reserved for subaddress 30 (data wraparound subaddress) transmit, receive, and broadcast receive Data Words	
04A0-04BF	----	Reserved for “Block 0” (double buffered) for receive subaddress 19	
04C0-04DF	----	Reserved for “Block 1” (double buffered) for receive subaddress 19	
04E0-04FF	----	Reserved for all unused subaddresses.	
0800-0BFF	----	Reserved for 1024-word circular buffer for receive subaddress 7	
0C00-0FFF	----	Reserved for 1024-word circular buffer for receive subaddress 7	

6.19.1 Pseudo Code

The following pseudo code is the series of register and memory write transfers required to initiate the ACE/Mini-ACE RT as described above. The notation "Rxy ⟵" represents a write access to ACE/Mini-ACE register address xy. The notation "Mwxyz ⟵" represents a write access to ACE/Mini-ACE shared RAM address wxyz.

R03 ⟵ 0001 Software reset via the Start/Reset Register

R07 ⟵ 8000 Set ENHANCED MODE bit in Configuration Register #3 to enable enhanced RT features (busy by subaddress, enhanced mode code handling, enhanced interrupts, etc.)

R00 ⟵ 0036 Interrupt Mask Register: Enable interrupts for RT CIRCULAR BUFFER ROLLOVER, RT SUBADDRESS CONTROL WORD, FORMAT ERROR, and RT MODE CODE.

R02 ⟵ B803 Configuration Register #2: Enable ENHANCED INTERRUPTS, BUSY LOOKUP TABLE, RECEIVE SUBADDRESS DOUBLE BUFFERING, OVERWRITE INVALID DATA, ENHANCED RT MEMORY MANAGEMENT, and SEPARATE BROADCAST DATA.

R07 ⟵ 801D Configuration Register #3: Keep ENHANCED MODE enabled. Disable ILLEGAL RECEIVE DATA TRANSFERS and ILLEGAL BUSY DATA TRANSFERS (by programming the respective bits to logic

"1"). Enable RTFAIL-RTFLAG WRAP and ENHANCED MODE CODE HANDLING.

R08 ←— 2008 Configuration Register #4: Enable MODE CODE OVERRIDE BUSY and LATCH RT ADDRESS WITH CONFIGURATION REGISTER # 5.

R09 ←— 890E Configuration Register #5: Enable 12 MHZ CLOCK SELECT (10 MHZ CLOCK SELECT for the BU-61689), EXPANDED ZERO CROSSING, and GAP CHECK. Program RT Address to 7 (parity bit = 0)

M0000 ←— 0000 Initialize Block Status Word locations in stack to 0000.
• • •
• • •
• • •
M00FC ←— 0000 •

M0100 ←— 0000 Initialize Stack Pointer to top of stack

M0108 ←— 0000 Program mode code interrupts
M0109 ←— 0002 •
M010A ←— 010A •
M010B ←— 0000 •
M010C ←— 0000 Program mode code interrupts (continued)
M010D ←— 0000 •
M010E ←— 010A •

M010F ←— 0000 •

M0111 ←— 0000 Reserved for received Data Word for Synchronize (with data) mode code
M0120 ←— 1234 Programmed value for vector word (to be transmitted)

M0147 ←— 0800 RT Lookup table
M0153 ←— 0440 •
M0161 ←— 0400 •
M015E ←— 0480 •
M017E ←— 0480
M0187 ←— 0C00 •
M0193 ←— 04A0 •
M019E ←— 0480 •

M01A1 ←— 4000 RT Subaddress Control Words
M01A7 ←— 018C •
M01B3 ←— 8210 •
M01BE ←— 0000 •

M0240 ←— 0000 Subaddress Busy table
•
•
•
M0247 ←— 0000

M0300 ←— 0000 Command Illegalization Table
M0301 ←— FFFD •
M0302-030D ←— FFFF •
M030E-030F ←— 0000 •
M0310-0325 ←— FFFF •
M0326-0327 ←— 0000 •
M0328-033B ←— FFFF •
M033C-033D ←— 0000 •
M033E ←— FFFF •
M033F ←— FFFD •
M0340 ←— FE05 •
M0341 ←— FFFF •
M037E ←— FE05 •
M037F ←— FFFF •
M0380 ←— FFFF •
M0381 ←— FFFD •
M0382-038D ←— FFFF •
M038E-038F ←— 0000 •
M0390-03A5 ←— FFFF •
M03A6-03A7 ←— 0000 •
M03A8-03BB ←— FFFF •
M03BC-03BD ←— 0000 •
M03BE ←— FFFF •
M03BF ←— FFFD •
M03C0 ←— FE00 •
M03C1 ←— FFF2 •
M03C2-03C3 ←— 0000 •
M03C4-03FB ←— FFFF •
M03FC-03FD ←— 0000 •
M03FE ←— FE00 •
M03FF ←— FFF2 •

M0400 ←— 0000 Data Words for transmit subaddress 1
M0401 ←— 0001 •
• • •
• • •
• • •
M041F ←— 001F •

R01 ←— 8F80 Configuration Register #1: Configure ACE/Mini-ACE for RT mode. Clear DYNAMIC BUS CONTROL, BUSY, SERVICE REQUEST, SUBSYSTEM FLAG, and RTFLAG RT Status Word bits (by programming the respective bits to logic "1").

6.20 SERVICING COMPLETED RT MESSAGES

The ACE/Mini-ACE RT provides a number of techniques for determining when a message has been processed. These methods support both polling-driven and interrupt-driven software.

There are several polling methods that may be used. These include:

1) In the ENHANCED mode, the host may continuously poll RT MESSAGE IN PROGRESS, bit 0 of Configuration Register #1. This bit will return logic "0" while the ACE/Mini-ACE RT is not processing a message. During the time that the ACE/Mini-ACE RT is servicing a message (after the receipt of a Command Word), RT MESSAGE IN PROGRESS will return logic "1." When the message completes, RT MESSAGE IN PROGRESS will once again return logic "0."

2) The CPU can poll the contents of the Stack Pointer RAM location. The active area Stack Pointer increments by four **at the beginning** of each message being processed (after receipt of a Command Word).

3) If the host needs to determine the occurrence of a **particular** Command Word, it may do so by polling the RT Last Command Register. It should be noted that the contents of this register are updated at the **beginning** of a message being processed. The CPU may then poll the EOM (End-of-Message) bit of the Interrupt Status Register to determine when the message has been completed. See explanation below.

4) If the ACE is programmed for the ENHANCED mode **and** ENHANCED INTERRUPTS (bit 15 of Configuration Register #2) are enabled, the CPU may poll the Interrupt Status Register. In this mode, the various bits in the Interrupt Status Register will become set **regardless** of the programming of the corresponding bits in the Interrupt Mask register.

In this mode, the ACE/Mini-ACE may determine that a message has been **completed** by polling the Interrupt Status Register until the EOM (End-of-Message) bit returns logic "1."

In this mode, the host processor may also poll to determine when a message has been processed for a **particular** transmit, receive, or broadcast subaddress. To enable do this, ENHANCED RT MEMORY MANAGEMENT (bit 1 of Configuration Register #2) must be invoked. To cause the bit to be set for a particular Tx/RX/Bcst-subaddress, it is then necessary to set the appropriate bit ([TX:, RX:, or BCST:] INT on EOM) in the desired Subaddress Control Word to logic "1." All other Subaddress Control Word ([TX:, RX:, or BCST:] INT on EOM) bits should be programmed to logic "0." This will cause the RT SUBADDRESS CONTROL WORD EOM bit in the Interrupt Status Register to be set to logic "1" after completion of the desired message.

Similarly, the host may poll for receipt of a **particular** mode code message. This feature is enabled by invoking ENHANCED MODE CODE HANDLING (bit 0 of Configuration Register #3). The desired mode code may be selected by setting the appropriate bit in the Mode Code Selective Interrupt Table (address range 0108-010F). When the specific mode code message has been completed, the RT MODE CODE bit of the Interrupt Status Register will return logic "1."

Similarly, the Interrupt Status Register may be polled to determine the occurrence of FORMAT ERROR, CIRCULAR BUFFER ROLLOVER, and/or COMMAND STACK ROLLOVER conditions. FORMAT ERROR indicates any error in a received message, other than an invalid Command Word: sync or Manchester encoding, parity, bit count, word count, or RT-to-RT transfer errors. CIRCULAR BUFFER ROLLOVER may be used to signal completion of a multimessage bulk data transfer. COMMAND STACK ROLLOVER occurs when the Stack rolls over at an address boundary of 256, 512, 1024, or 2048 words, as programmed in Configuration Register #3.

If interrupts are used, the normal procedure would be to **not** invoke ENHANCED INTERRUPTS. This allows the Interrupt Mask Register to be used to enable interrupts and the corresponding Interrupt Status Register bits for only **selected** condition(s), as discussed above.

6.21 RT ERROR HANDLING

As discussed above, the preferred method for handling erroneous messages is to make use of the circular buffer and/or double buffering techniques. In the case of the circular buffer mode, the OVERWRITE INVALID DATA bit should be set to logic "1." With these techniques, Data Words received and stored from invalid messages will be automatically overwritten by the ACE/Mini-ACE RT. In most systems, the bus controller will retry failed messages. By so doing, the occurrence of errors and message retries is transparent to the RT's host processor.

If necessary, the RT's host processor may ascertain the occurrence of failed messages by several methods:

1) Determine, by polling or interrupt techniques, when a FORMAT ERROR condition occurs.

2) Read the Block Status Words for all messages processed. Bits 12-9 and 6-0 all indicate error conditions in received messages.

7 MONITOR OPERATION

The ACE/Mini-ACE terminals provide three different bus monitor modes: (1) a Word Monitor, (2) a Selective Message Monitor, (3) a combined RT/Selective Message Monitor mode. When the ACE/Mini-ACE is in Non-Enhanced Mode, the Monitor operates the same as the previous generation product, BUS-61559 Advanced Integrated Mux Hybrid with Enhanced RT features (AIM-HY'er). In ENHANCED MODE, both Selective Message Monitor and Combined RT/Selective Message Monitor modes may be activated. ENHANCED MODE also enables the Monitor triggering capability for the Word Monitor mode.

In Enhanced mode, the Word Monitor provides a programmable Trigger Word. The Trigger Word, which defines a specific Command Word, may be used to start and stop the Monitor or generate an interrupt. You may also start the Word Monitor by means of an external trigger.

The Selective Message Monitor supports message filtering, based on RT Address/T-$\overline{R}$ bit/Subaddress, and provides separate Command and Data Stacks. The Message Monitor also stores the contents of the 16-bit Time Tag Register (see Time Tag Register for resolution programming).

The RT/Selective Message Monitor mode provides full RT capability for the ACE/Mini-ACE terminal's own RT address **PLUS** selective monitoring for all other RT addresses. Similar to RT mode, the Selective Monitor's Command Stack stores all command words, Time Tag words, Block Status words, and Data block pointers for each monitored message. The Command and Data Stacks are programmable via bits 12-8 in Configuration Register 3.

7.1 WORD MONITOR MODE

In Word Monitor Terminal mode, the ACE/Mini-ACE monitors both 1553 buses. After the software initialization and MONITOR START sequences, the ACE stores all Command, Status, and Data Words received from both buses. For each word received from either bus, **a pair** of words are stored to the ACE's shared RAM. The first word is the 16 bits of data from the received word. The second word is the Monitor Identification (ID), or "Tag" word. The ID Word contains information relating to bus channel, word validity, and interword time gaps. The data and ID words are stored in a circular buffer in the shared RAM address space.

7.2 WORD MONITOR MEMORY MAP

A typical word monitor memory map is illustrated in TABLE 96. TABLE 96 assumes that the full 64K words of shared RAM address space is available for the ACE/Mini-ACE's monitor. The Active Area Stack pointer provides the address where the first monitored word is stored. In the

example, it is assumed that the Active Area Stack Pointer for Area A (location 0100) is initialized to 0000. The first received data word is stored in location 0000, the ID word for the first word is stored in location 0001, etc.

The current Monitor address is maintained by means of an internal counter register. This value may be read by the CPU by means of the Data Stack Address Register. It is important to note that when the counter reaches the Stack Pointer address of 0100 (for active area A) or 0104 (for active area B), the initial pointer value stored in this shared RAM location **will be overwritten** by the monitored data and ID Words. When the internal address counter reaches an address of FFFF (or 0FFF, if only the ACE/Mini-ACE's 4K of internal RAM is used), the counter rolls over to 0000.

TABLE 96. TYPICAL WORD MT MEMORY MAP

HEX ADDRESS	FUNCTION
0000	First Received 1553 Word
0001	First Identification Word
0002	Second Received 1553 Word
0003	Second Identification Word
0004	Third Received 1553 Word
0005	Third Identification Word
•	•
•	•
0100	Stack Pointer (Fixed Location)
•	•
•	•
FFFF	•

To initialize the ACE/Mini-ACE for Word Monitor mode, the host processor should program bits 15, 14, and 12 of Configuration Register #1 to logic "0," logic "1," and logic "0" respectively. Next, the Stack Pointer for the active area should be loaded with the starting location of the monitor stack in the ACE/Mini-ACE shared RAM address space. Finally, to start the monitor, a "Start" command should be issued by means of the Start/Reset Register.

Note: *In ENHANCED MODE, the Word Monitor may also be started via the external trigger (EXT_TRIG) input.*

The Monitor ID Word contains a Word Flag bit (always logic 1) plus information relating to bus channel, word validity, Command-Status/$\overline{\text{Data}}$ sync type, and inter-word gap time information. This latter field includes a "Contiguous Data" bit as well as an 8-bit gap time field, indicating 0 to 127 µs with a resolution of 0.5 µs per LSB.

In order to take the ACE/Mini-ACE monitor off-line, the host CPU must issue a RESET command to the Start/Reset Register.

The ACE/Mini-ACE Identification Word is defined in TABLE 97.

TABLE 97. WORD MONITOR IDENTIFICATION WORD

BIT	DESCRIPTION
15(MSB)	GAP TIME
•	•
•	•
•	•
8	GAP TIME
7	WORD FLAG
6	$\overline{\text{THIS_RT}}$
5	$\overline{\text{BROADCAST}}$
4	ERROR
3	COMMAND/ $\overline{\text{DATA}}$
2	CHANNEL B/ $\overline{\text{A}}$
1	CONTIGUOUS DATA/ $\overline{\text{GAP}}$
0(LSB)	$\overline{\text{MODE_CODE}}$

GAP TIME: If the CONTIGUOUS DATA bit is high, these 8 bits are not used. If CONTIGUOUS DATA is low, GAP TIME indicates the time gap between the end of the previous word to the start of the current word in 0.5 µs/LSB resolution, up to 127.5 µs. For inter-word time gaps greater than 127.5 us, the GAP time field will indicate FF (hex). It should be noted that if the current word was received on the **alternate** bus from the previous word, the GAP TIME field will indicate approximately **20 us greater** than the actual gap time from the word on the first bus. That is, if the current word is received on the alternate bus from the previous word and the current GAP TIME is a time of less than 20 µs, this indicates that the current word **overlapped** the previous word (received on the alternate bus).

WORD FLAG: Always set to logic "1" for every Identification Word. Each location in the shared RAM where an ID Word is anticipated being stored should be initialized by the CPU to logic "0."

$\overline{\text{THIS_RT}}$: If this bit is low, it indicates that the received word was valid, contained a Command/Status sync type, had an RT Address field matching the address on inputs RTAD4-RTAD0 and that correct odd parity was presented on RTADP. This bit will be high otherwise.

$\overline{\text{BROADCAST}}$: If this bit is low, it indicates that the received word was valid, contained a Command/Status sync type and an RT Address field of 31. This bit will be high otherwise.

Note: *If the ACE/Mini-ACE is programmed for ENHANCED MODE* ***and*** *Broadcast has been disabled by programming bit 7 of Configuration Register #5 to logic "1," Broadcast will* ***always*** *return logic "1."*

ERROR: If this bit is low, it indicates that the received word passed all of the MIL-STD-1553 validation criteria. If this bit is high, it indicates an error in the word: either Manchester II encoding, sync, bit count or parity.

COMMAND/$\overline{\text{DATA}}$ SYNC: If this bit is high, it indicates the word contained a Command/Status type sync. If this bit is low, it indicates that the word contained a Data type sync.

CHANNEL B/$\overline{\text{A}}$: If this bit is low, it indicates that the word was received on Channel A. If the bit is high, it indicates that the word was received on Channel B.

CONTIGUOUS DATA/$\overline{\text{GAP}}$: If this bit is high, it indicates either no gap or less than 2 µs of dead time on the bus from the end of the previous word to the start of the current word. In this case, the GAP TIME field is not used. If this bit is low, it indicates a gap time of more than 2 µs from the end of the previous word to the start of the current word. In this case, the GAP TIME field **does** contain valid bus dead time information.

$\overline{\text{MODE_CODE}}$: If this bit is low, it indicates that the received word was valid, had a Command/Status sync type and contained a subaddress field of either 0 or 31. This bit will be high otherwise. However, if the MONITOR TAG GAP OPTION bit , bit 4 of Configuration Register #4(01000h, Read/Write) is set to logic “1", the $\overline{\text{MODE_CODE}}$ bit indicates the occurrence of a handshake failure. A hand shake failure occurs in the transparent mode when an external arbitration circuit withholds the data transfer grant signal beyond the specified timeout period. When a timeout occurs, the monitored 1553 word and tag word will be lost and the ACE/Mini-ACE will assert the $\overline{\text{MODE_CODE}}$ bit in the tag word of the NEXT monitored word to indicate that a timeout occurred and a word was lost. Note that this feature is not implemented in some versions of the ACE family. However, this feature is implemented in all Mini-ACE series terminals.

7.3 WORD MONITOR INITIALIZATION

In Word MT mode, the active area stack pointer provides the address where the first monitored word is stored. This pointer must be written by the CPU prior to issuing a MT START command. The data for the first received word will be stored in the location pointed to by the Active Area Stack Pointer. It is important to note that both (Area A and B) Stack Pointers will be **overwritten** by received data or identification words. (See FIGURE 13 and FIGURE 14)

7.3.1 Word Monitor Start and Stop

To start the ACE/Mini-ACE Monitor, write the value 0002 to the Start/Reset Register (BC/MT START) . To stop the Monitor from storing further words from the 1553 bus, write the value 0001 to the Start/Reset Register (RESET).

7.3.2 Word Monitor Software Initialization Sequence

The software procedure for initializing the ACE/Mini-ACE in Monitor mode is outlined as follows:

1) Issue a software RESET by writing a value of 0001 to the Start/Reset Register.

2) Initialize the ACE/Mini-ACE to MT mode with Active Area A (the Active Area selection doesn't matter in MT mode) by writing a value of 5000 to Configuration Register #1.

3) Write the desired location to start storing received words to the Area A Stack Pointer location, 0100.

4) Optionally, clear the area of shared RAM where received data and ID words are anticipated to be received to values of 0000. This allows the host processor to easily determine the location of the last word received by means of the WORD FLAG bit in the ID Word.

5) To initiate the Monitor to start storing received words, write the value 0002 to the Start/Reset Register (BC/MT START).

6) To subsequently cause the Monitor to stop storing received words, write the value 0001 to the Start/Reset Register (RESET).

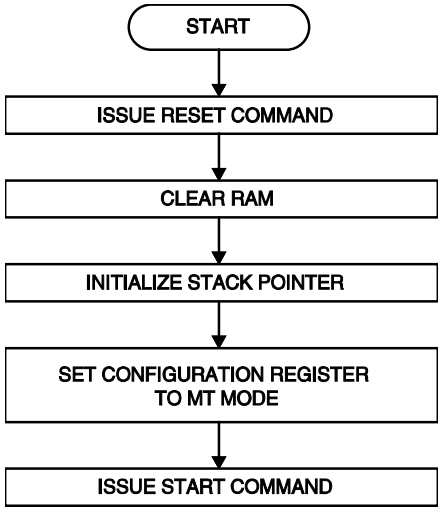


FIGURE 13. MT INITIALIZATION

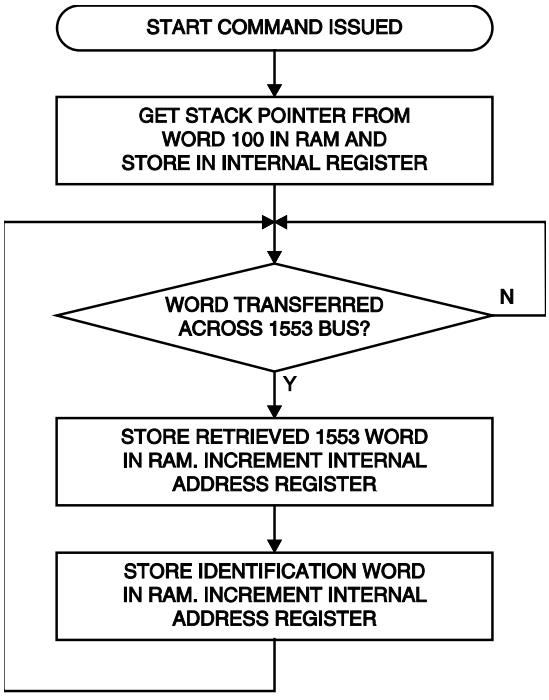


FIGURE 14. MT DATA STORAGE OPERATION

7.4 DISTINGUISHING COMMAND WORDS FROM STATUS WORDS: Message Reconstruction

In the Word Monitor mode, message reconstruction entails determining when individual messages received from the 1553 bus begin and end. A critical part of this process, which must be implemented in software (either in real time or off-line), is to distinguish between Command Words and Status Words.

There probably is no universal algorithm for making an absolute "100%" determination between Command and Status Words. This would have to take into account superseding and bus switching command sequences in addition to a multiplicity of message error conditions. However, the rules listed below will prove useful in making the command/status determination for the **vast majority (greater than 99.99%)** of all "real-world" MIL-STD-1553B applications.

1) A word containing a Command/Status sync and any sub-address field (bits 9 (MSB) through 5 (LSB)) **other than 0 or 8** is a Command Word.

2) A word with a Command/Status sync preceded by a gap time of longer than the "response timeout" time is a Command Word. For most applications, 14 µs is probably a good starting value for the "response timeout" parameter. For applications entailing very long lengths of bus cable (several hundred feet), a longer period for the "bus timeout" parameter may be required.

3) A word with a Command/Status type of sync received on the alternate bus from the last previous received word may be considered to be a Command Word.

4) Two contiguous (no intervening gap time) words with Command/Status sync types, with the first of the two words preceded by a gap, are the two Command Words for an RT-to-RT transfer or RT-to-Broadcast transfer.

5) A word with a Command/Status sync and a value of 31 (11111) for the RT Address field (bits 15 [MSB] through 11 [LSB]) is a Command Word to the Broadcast address.

6) The next **noncontiguous** word with a Command/Status sync following a Command Word to the Broadcast address is a Command Word.

7) The principal purpose of the CPU's Monitor software will be to reconstruct the 1553 messages. Once the parsing routine encounters a Command Word, marking the beginning of a new message, it should continue to search through the message,

verifying that it conforms to one of the MIL-STD-1553B message formats (reference FIGURE 3 of MIL-STD-1553B).

If the "message reconstructor" software is parsing through a received message that is **not** an RT-to-RT transfer, a word with a Command/Status sync, and a **different** RT address than the previous word with a command/status sync may be considered to be the Command Word for the next message.

8) If the message reconstructor software is parsing through a stream of Data Words and determines the end of a complete, valid message followed by a gap time (possibly less than the "response timeout" value), the **next** word with a command/status sync type will be a Command Word. This is regardless of whether the word contains the same RT address or a different RT address than the previous Command/Status word.

7.5 WORD MONITOR TRIGGER

In the Word Monitor mode, there is a pattern recognition trigger and a pattern recognition interrupt. The 16-bit compare word for both the trigger and the interrupt is stored in the MT TRIGGER WORD register. The pattern recognition interrupt is enabled by setting the MT PATT TRIG bit (bit 9) in the Interrupt Mask Register. The pattern recognition trigger is enabled by setting the TRIGGER ENABLE bit (bit 11) in Configuration Register #1 and selecting either the START-ON-TRIGGER (bit 10) or the STOP-ON-TRIGGER (bit 9) bit in Configuration Register #1.

TABLE 98. WORD MONITOR WITH TRIGGER TRUTH TABLE (Configuration Register # 1 bits)

START ON TRIGGER (BIT 10)	STOP ON TRIGGER (BIT 9)	EXTERNAL TRIGGER (BIT 7)	WORD MT START AND STORE OPERATION
0	0	0	Software Start, MT stores all data on the bus.
0	0	1	Software or External Trigger Start, MT stores all data on the BUS
0	1	0	Software Start, MT stores all data until the Command Word matches the word stored in the MT Trigger Register (MTR). This Command Word is the last word stored in the MT Stack.
0	1	1	Software or External Trigger Start stores all data until the Command Word matches the word stored in the MT Trigger Register (MTR). This Command Word is the last word stored in the MT Stack.
1	0	0	Software Start, stores all data after a valid Command Word matches the word stored in the MT Trigger Register (MTR). This Command Word is stored in the MT Stack.
1	0	1	Software or External Trigger Start, stores all data after a valid Command Word matches the word stored in the MT Trigger Register (MTR). This Command Word is stored in the MT Stack.
1	1	0	Software Start, stores ONLY the Command Word that matches the word stored in the MT Trigger Register.
1	1	1	Software or External Trigger Start, stores ONLY the Command Word that matches the word stored in the MT Trigger Register.

The Word Monitor with Trigger truth table (TABLE 98) assumes the following:

1) User is in the ENHANCED MODE.

2) Word Monitor is selected in Config Reg #1 (Bit 15=0 14=1 12=0).

3) User programs the "Trigger Word" in the MT Trigger Register.

4) Trig Enable Bit (bit 11 in Config Reg # 1) is set to a logic 1.

7.6 SELECTIVE MESSAGE MONITOR MODE

The ACE/Mini-ACE provides a flexible interface that allows selective monitoring of 1553 messages based on RT Address, T/R, and Subaddress with very little host processor intervention. The Message Monitor mode of the ACE/Mini-ACE recreates all command/response messages on the 1553 bus on channels A and B, and stores them into the shared RAM based on a user programmable filter (RT Address, T/R, and Subaddress). This monitor can be used as a monitor alone or in a combined RT/Monitor mode. The Message Monitor contains two stacks (a command stack and a data stack) that are independent from the BC/RT command stack. The pointers for these stacks are located in fixed locations in the RAM.

The Message Monitor is enabled in the RT/Monitor mode by setting the ENHANCED MODE bit (bit 15) in Configuration Register bit #3 to a logic "1," RT/BC_L (bit 15) to logic "0," and setting MT (bit 14) and MESSAGE MONITOR ENABLE (bit 12) bits in Configuration Register #1 to logic "1."

It should be noted that an MT START command (setting bit 1 of the START/RESET REGISTER) is **required** to start the Selective Message Monitor in the monitor only mode. However, in the combined RT/Selective Message Monitor mode, an MT START command is **not required**.

7.6.1 Monitor Selection Function

While operating in Selective Message Monitor mode, upon receipt of a valid command, the ACE/Mini-ACE will reference the selective monitor lookup table (a fixed block of RAM) to determine if this command is enabled. The address for this location is determined by using the RT Address, $T/\overline{R}$ bit, and Subaddress bit 4, of the current command, and adding it to the base address 0280(hex) (FIGURE 16). The bit location within this 16-bit word is determined by subaddress bits 3..0 of the current Command Word. If the specified bit in the lookup table is logic

"0" the command is not enabled and the ACE/Mini-ACE will abort processing this message and will begin looking for new command words. It should be noted that an RT status word may be interpreted by the ACE/Mini-ACE as a new command word. If the bit in the monitor look up table is logic "1," the command is enabled and the ACE/Mini-ACE will create an entry on the monitor command stack (based on the monitor command stack pointer) and store the data associated with this command into sequential locations in the monitor data stack.

The address definition for the Selective Monitor Lookup Table is illustrated below.

TABLE 99. MESSAGE MONITOR SELECTION TABLE ADDRESS

BIT	DESCRIPTION
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	LOGIC “0”
9	LOGIC “1”
8	LOGIC “0”
7	LOGIC “1”
6	RTAD_4
5	RTAD_3
4	RTAD_2
3	RTAD_1
2	RTAD_0
1	$T/\overline{R}$
0(LSB)	SUBADDRESS_4

For even-numbered addresses in the Selective Monitor Lookup Table (SUBADDRESS_4 = A0 = 0), bit 15 enables monitoring for subaddress 15, bit 14 enables monitoring for subaddress 14,.....bit 0 enables subaddress 0. For odd-numbered addresses in the Selective Monitor Lookup Table (SUBADDRESS_4 = A0 = 1), bit 15 enables monitoring for subaddress 31, bit 14 enables monitoring for subaddress 30,.....bit 0 enables subaddress 16. Programming a bit to logic "0" **disables** monitoring for the respective RT Address-$T/\overline{R}$ bit-subaddress; i.e., a message will be ignored. Programming a bit to logic "1" **enables** monitoring for the respective RT Address-$T/\overline{R}$ bit-subaddress; that is, the message will be stored.

7.6.2 Message Monitor Formats

The format of the information in the data stack depends on the type of message that was processed. A BC-to-RT command transfer (receive) will store the Command Word in the monitor Command Word stack, the N-Data Words followed by the receiving RT's status response in the monitor data stack.

Note: *If the ACE/Mini-ACE selects the* ***receive*** *command in a RT-to-RT transfer, the RT-RT TRANSFER FORMAT bit (bit 11) of the Block Status Word will be set regardless of whether the transmit command was selected. In the case where the ACE/Mini-ACE selects only the transmit Command Word in an RT-to-RT transfer, the first word stored in the monitor data stack entry will be the second (transmit) Command Word, followed by Tx status, data and Rx status, i.e., the ACE/Mini-ACE will ignore the receive command word and status word.*

Reading a monitored message from the ACE/Mini-ACE, requires the use of:

1) The Block Status Word to determine if the message was an RT-to-RT transfer.

2) The Command Word to determine the message format (transmit, receive, mode code, broadcast, etc) and word count.

3) The data pointer to the data block entry.

Refer to FIGURE 15 for a complete listing of all message monitor data stack message formats.

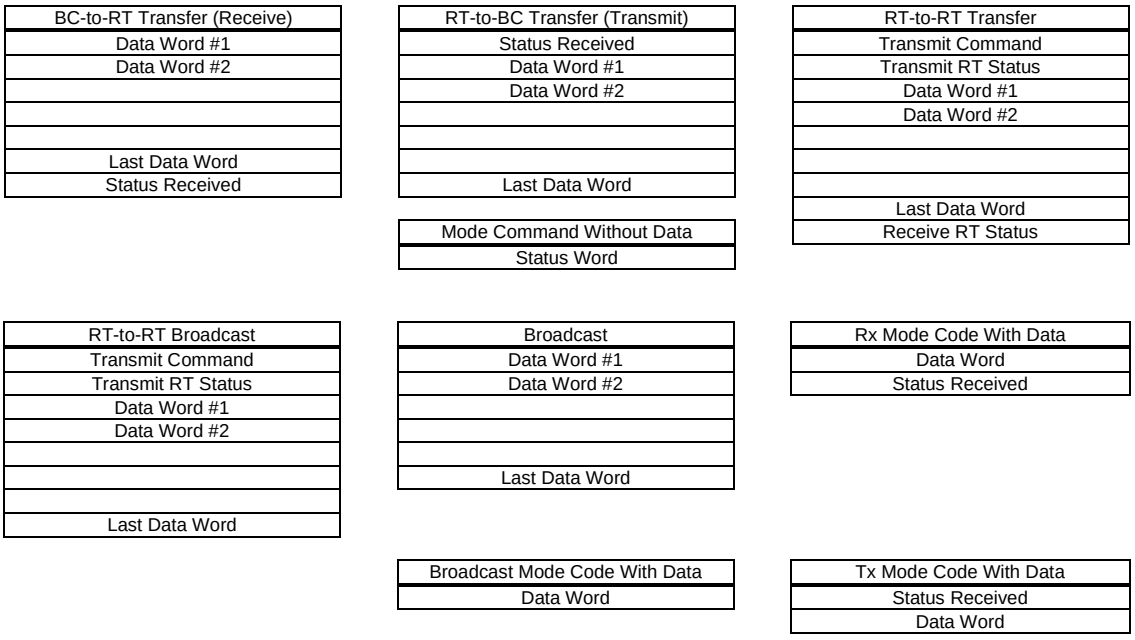


FIGURE 15. SELECTIVE MESSAGE MONITOR DATA BLOCK FORMATS

A typical memory map for the ACE/Mini-ACE in the Selective Message Monitor mode is illustrated in TABLE 100. This mode of operation defines several fixed locations in the RAM. These locations are allocated in a manner in which none of them overlap with the reserved RT locations. This allows for a combined RT/Selective Message Monitor mode. Refer to TABLE 101 for an example of a typical RT/Selective Message Monitor Memory Map.

The fixed memory map consists of two Monitor Command Stack Pointers (locations 102 and 106 hex), two Monitor Data Stack Pointers (locations 103 and 107 hex), and a Selective Message Monitor Lookup Table (locations 0280 through 02FF hex) based on RT Address, T/$\overline{R}$, and subaddress. The Monitor Command Stack size is assumed to be 1K words, and the Monitor Data Stack size is assumed to be 2K words.

TABLE 100. TYPICAL SELECTIVE MESSAGE MONITOR MEMORY MAP (shown for 4K RAM for "Monitor only" mode)

ADDRESS (HEX)	DESCRIPTION
0000-0101	Not Used
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack Pointer A (fixed location)
0104-105	Not Used
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-027F	Not Used
0280-02FF	Selective Monitor Lookup Table (fixed area)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0FFF	Monitor Data Stack A

Note: Stack B is not used in this example

TABLE 101. TYPICAL RT/SELECTIVE MESSAGE MONITOR MEMORY MAP (shown for 12K RAM for combined RT/MT mode)	
ADDRESS (HEX)	**DESCRIPTION**
0000-00FF	RT Command Stack A
0100	RT Command Stack Pointer A (fixed location)
0101	RESERVED
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack Pointer A (fixed location)
0104	Stack Pointer B (fixed location)
0105	RESERVED
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-010F	Mode Code Selective Interrupt Table (fixed area)
0110-013F	Mode Code data (fixed area)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-0247	Busy Bit Lookup Table (fixed area)
0248-025F	(not used)
0260-027F	RT Data Block 0 or Registers
0280-02FF	Selective Monitor Lookup Table (fixed area)
0300-03FF	Command Illegalizing Table (fixed area)
0400-07FF	Monitor Command Stack A
0800-0FFF	Monitor Data Stack
1000-101F	Data Block 0
1020-103F	Data Block 1
• • •	• • •
2FE0-2FFF	Data Block 255

The size of the monitor command stack is programmable to 256, 1K, 4K, or 16K by bits 11 and 12 of Configuration Register #3. The Monitor Data Stack size is programmable to 512, 1K, 2K, 4K, 8K, 16K, 32K or 64K by use of bits 8 through 10 in Configuration Register #3.

Interrupts can be generated for MONITOR COMMAND STACK OVERFLOW (bit 13 of interrupt status register), MONITOR DATA STACK OVERFLOW (bit 12 of interrupt status register), or END OF MESSAGE (bit 0 of interrupt status register).

Refer to FIGURE 16 for an illustration of the Selective Message Monitor operation. Upon receipt of a valid Command Word, the ACE/Mini-ACE will reference the Selective Monitor Lookup Table (a fixed block of addresses) to determine if the current command is enabled. If the current command is disabled, the ACE/Mini-ACE will ignore (and not store) the current message. If the command is enabled, the ACE/Mini-ACE will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer.

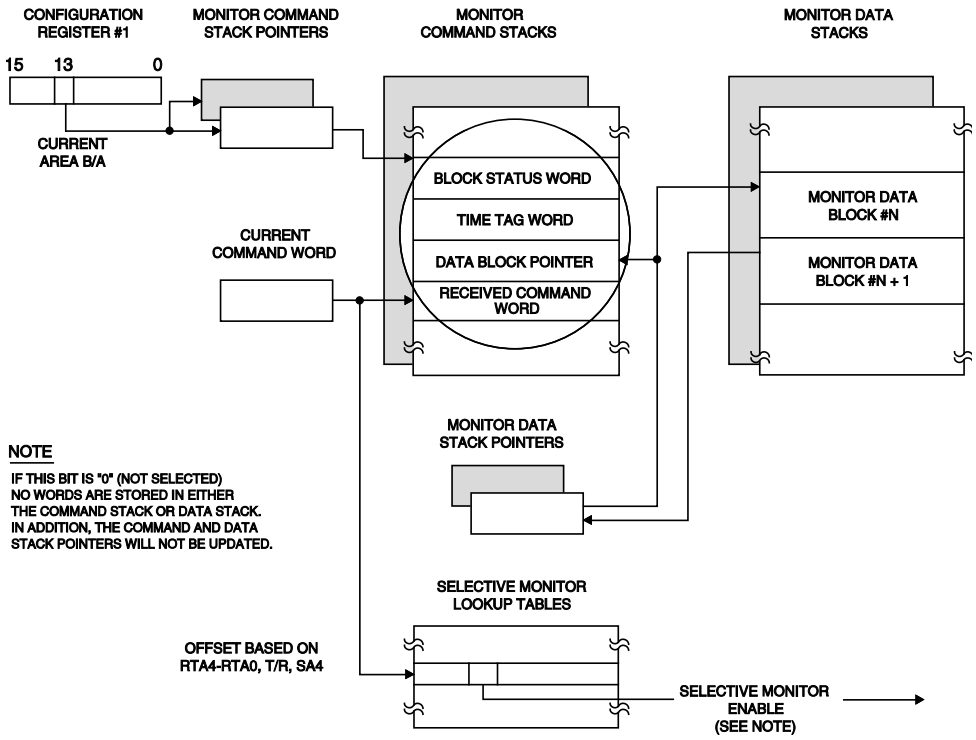


FIGURE 16. SELECTIVE MESSAGE MONITOR

7.6.3 Message Monitor Block Status Word

The bit map and bit descriptions for the Message Monitor Block Status Word are indicated in TABLE 58 on page 86.

END-OF-MESSAGE (EOM): Set at the completion of a monitored message, regardless of whether or not there were any errors in the message.

START-OF-MESSAGE (SOM): Set approximately 3-4 µs following the receipt (mid-parity bit) of the Command Word and cleared at the end of the message.

CHANNEL B/$\overline{A}$: This bit will be low if the message was monitored from Channel A or high if the message was monitored on Channel B.

ERROR FLAG: If this bit is high and bit 10 and/or bit 9 is high, this indicates that either a format error, no response error occurred in the message. If this bit is high, the ACE is configured for its transparent mode of processor interface, and bits 10 and 9 are both logic "0," this indicates that a handshake failure has occurred. A handshake failure occurs when the input signal $\overline{\text{DTGRT}}$ is either not asserted low or is asserted low too late (later than 4.4 µs in 20 MHz mode, 4 µs in 16 MHz mode, 3.5 µs in 12 MHz mode, or 3.2 µs in 10 MHz) after the time that the output signal $\overline{\text{DTGRT}}$ is asserted low. Alternatively, a handshake failure will occur if the host CPU fails to clear $\overline{\text{STRBD}}$ (high) within 4 µs after the ACE/Mini-ACE has asserted its $\overline{\text{READYD}}$ output (low). If a handshake failure occurs, a received message should be considered invalid.

RT-to-RT TRANSFER: This bit indicates that the message was an RT-to-RT transfer. The receive Command Word must be selected, and is stored in the Monitor Command Stack. The transmit Command Word is stored in the Monitor Data Stack in the location referenced by the Data Block Pointer Word in the Monitor Command Stack.

FORMAT ERROR: If set, indicates that a message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.).

RESPONSE TIMEOUT: If set, indicates that an RT has either not responded or has responded later than the programmed No Response Timeout time. The ACE/Mini-ACE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the nominal values (±1 µs) 18.5, 22.5, 50.5, and 130 µs by means of bits 10 and 9 of Configuration Register #5.

GOOD DATA BLOCK TRANSFER: Set to logic "1" following completion of a valid (error-free) message, set to logic "0" following completion of an erroneous (invalid) message.

DATA STACK ROLLOVER: If DATA STACK ROLLOVER is logic "1," indicates that the current message resulted in the value of the Monitor Data Stack Pointer rolling over, from the bottom to the top of its range. The size of the Monitor Data Stack is programmable from among 512, 1K, 2K, 4K, 8K, 16K, 32K, and 64K words by means of bits 10, 9, and 8 of Configuration Register #3.

WORD COUNT ERROR: If set, indicates that either a BC or a responding RT did not transmit with the correct number of Data Words.

INCORRECT SYNC TYPE: If set, indicates that a BC transmitted a Data sync with a Command Word or a Command/Status sync with a Data Word, or a responding RT responded with a Data sync in a Status Word and/or a Command/Status sync in a Data Word.

INVALID WORD: Indicates a BC transmitted, or an RT responded with one or more words containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

RT-to-RT GAP/SYNC/ADDRESS ERROR: This bit is set if one or more of the following occur: (1) If the GAP CHECK ENABLED bit (bit 8) of Configuration Register #5 is set to logic "1" **and** a the transmitting RT responds with a response time of less than 4 µs, per MIL-STD-1553B (mid-parity bit to mid-sync); i.e., less than 2 µs dead time; and/or (2) A responding RT for an RT-to-RT transfer responds with an invalid Status Word (encoding, bit count, and/or parity error) or a Data Word sync in its Status Word and/or; (3) The RT Address field of the command word does not match the RT address in the RT status response.

RT-to-RT SECOND COMMAND ERROR: For an RT-to-RT transfer, this bit set to logic "1" indicates one or more of the following error conditions in the second of two contiguous Command Words: (1) $T/\overline{R}$ bit = logic "0"; (2) subaddress = 00000 or 11111; (3) The RT Address in the transmit Command Word is the same as the RT Address in the receive Command Word.

COMMAND WORD CONTENTS ERROR: Indicates that a received Command Word is not defined in accordance with MIL-STD-1553B. This includes the following undefined Command Words: (1) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** the Command Word is a non-mode code, broadcast, transmit command; (2) The OVERRIDE MODE $T/\overline{R}$ ERROR bit, bit 6 of Configuration Register #3, is logic "0" **and** a message with a the Command Word had a $T/\overline{R}$ bit

of "0," a subaddress/mode field of 00000 or 11111 and a mode code field between 00000 and 01111; (3) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** the Command Word is a broadcast command of a mode code that is not permitted to be broadcast to the broadcast address (11111).

7.6.4 Superseding Commands

A superseded message sequence occurs when a valid message begins on one bus, followed by a time gap, followed by a new command on the alternate bus. If both the old and the new command are to the same RT Address, the RT **must** stop processing the first command, and begin processing the new command. If the commands are to different RT Addresses, the terminal responding to the first command **must** complete processing the message and ignore the activity on the alternate bus.

The ACE/Mini-ACE selective message monitor will abort processing the first message and begin processing the new message. The only exception to this is when the ACE is operating in the combined RT/Selective Message and the first command is to the ACE/Mini-ACE's RT Address **and** the second command is to different, nonbroadcast, RT Address. As an RT, the ACE/Mini-ACE must continue processing the first command (in compliance with MIL-STD-1553), and ignore the new command to a different terminal on the alternate bus.

The ACE/Mini-ACE selective message monitor will supersede a message on the same bus except when the superseding command may be interpreted as a status word. Hence, a RT status response with the wrong RT address in the status word will NOT appear to the ACE/Mini-ACE selective message monitor as a new command, but rather will appear to be a bad status word.

When a message is superseded, a normal Start Of Message (SOM) sequence is performed on the new (superseding) message. Note that an End Of Message (EOM) sequence is NOT executed on the original (superseded) message. This will result in a command stack entry with the Start Of Message (SOM) bit in the block status word set to logic "1" and the End Of Message (EOM) bit set to logic "0." The host processor can distinguish between a message in progress and a superseded message by the value of the monitor command stack pointer. If the monitor command stack pointer has incremented beyond the command stack entry in question and the block status word indicates an SOM state, then the message must have been superseded.

7.7 SELECTIVE MESSAGE MONITOR SOM AND EOM TRANSFER SEQUENCES

Approximately 1.25 µs following the mid-parity bit crossing of a received Command Word, the ACE/Mini-ACE performs the Selective Monitor Start-of-Message (SOM) sequence. After the first two steps of the SOM sequence, the ACE/Mini-ACE determines if the message is "selected" (to be stored); this is a function of the RT address, T/R bit, and Subaddress fields of the received Command Word. Approximately 6 µs after the end of the last word received for a selected message, the ACE/Mini-ACE performs the MT End-of-Message (EOM) Sequence. The MT SOM and EOM sequences consist of sequences of words read from and written to the ACE's shared RAM. The Monitor SOM and EOM sequences are summarized below:

MT Start-of-Message (SOM) Sequence.

1) Corresponding to the RT address, $T/\overline{R}$ bit, and subaddress of the received Command Word, the appropriate Monitor Selection word is read from the Monitor Selection table.

2) The Monitor Command Stack Pointer is read from the active area Monitor Command Stack Pointer location. This address is used to locate the first word of message's block descriptor in the Monitor Command Stack. If the result of step 1 indicated that the message is "selected" (to be stored), continue to step 3. If the message is not "selected," the SOM sequence is terminated.

3) The Monitor Data Stack Pointer is read from the active area Monitor Data Stack Pointer location (either memory location 103h or 107h, depending on what channel the message was received from).

4) The Command Word is written to the fourth location in the current descriptor block.

5) The Data Stack Pointer is written to the third word of the current descriptor block. This value is used for locating the first location for the current message in the Monitor Data Stack.

6) The Time Tag word is written to the second location in the current descriptor block.

7) The Block Status Word is written to the first location in the current descriptor block.

8) The value of the Command Stack Pointer read in step 2 is incremented by four and written to the active area Stack Pointer.

MT End-of-Message (EOM) Sequence.

1) The address of the last word stored in the Data Stack is incremented by one (modulo the Data Stack size) and written to the active area Data Stack Pointer location.

2) The Time Tag word is written to the second location in the block descriptor.

3) The Block Status Word is written to the first location in the block descriptor.

7.8 SELECTIVE MESSAGE MONITOR PROGRAMMING SEQUENCE (assuming 4K RAM using End-of-Message (EOM) interrupt)

7.8.1 Initialization

1) Write 0001h to START/RESET Register to reset the device.

2) Write 8000h to CONFIGURATION REGISTER #3 to enable ENHANCED MODE features.

3) Write 8D00h to CONFIGURATION REGISTER #3 to configure the device for ENHANCED MODE enabled, a 1K Monitor Command Stack size and a 2K Monitor Data Stack size.

4) Write 5000h to CONFIGURATION REGISTER #1 to place the device in the Selective Message Monitor mode.

5) Write 0400h to RAM location 0102h to initialize the Monitor Command Stack Pointer.

6) Write 0800h to RAM location 0103h to initialize the Monitor Data Stack Pointer.

7) Initialize the Selective Monitor Lookup Table in RAM locations 0280h to 02FFh. Note that programming FFFFh in all 128 locations will program the ACE to monitor ALL commands.

8) Write 0010h to CONFIGURATION REGISTER #2 to enable interrupt auto clear function.

9) Write 0001h to INTERRUPT MASK register to enable End Of Message (EOM interrupt.

10) Initialize the software variable stkptr to 0400h. This will act as an indicator of the next message that is to be serviced.

11) Write 0002h to START/RESET register to start the monitor.

Note: *The order in which steps 3-10 are executed does not matter.*

7.8.2 Servicing Technique

Note: *The initial value of the 'STKPTR' variable is set to the initial value of 'MTCMDPTR' at location 102/106h.*

Define an Interrupt Service Routine that will do the following:

a) Read and save value of INTERRUPT STATUS register.

b) Verify that Interrupt Status is 0001h (EOM occurred).

c) Read and store value of RAM location 0102h (Monitor Command Stack Pointer). This value will be referred to as MTCMDPTR.

d) Repeat the following sequence until (stkptr = MTCMDPTR) or [(((stkptr + 4) mod stack size) = MTCMDPTR) and (Block status word has som set)]:

i) Block Status Word = RAM location stkptr.

ii) Time Tag = RAM location stkptr + 1.

iii) Data pointer = RAM location stkptr + 2.

iv) Command Word = RAM location stkptr + 3.

v) Status and Data words are stored sequentially in RAM locations starting at the value of data pointer, the number of words and message format is determined by reading bit 11 of the Block Status Word and the contents of the Command Word. If bit 11 of the Block Status Word is logic "1," the message was an RT-to-RT transfer. In addition, you must check for a 2K data stack rollover when reading words from | the data stack.

vi) Store and/or use message information must be based on application requirements.

vii) stkptr = (stkptr + 4) modulo 1024. Increment to next message to be serviced, with a 1k rollover.

e) Exit Interrupt Service Routine.

8 EXTERNAL INTERFACES

8.1 INTERFACE TO A MIL-STD-1553 BUS

FIGURE 17 illustrates the interface between the various versions of the ACE/Mini-ACE series and a MIL-STD-1553 bus. Connections for both direct (short stub) and transformer (long stub) coupling, as well as the peak-to-peak voltage levels that appear at various points (when transmitting), are indicated in the Figure.

TABLE 102 lists the characteristics of the required isolation transformers for the various ACE/Mini-ACE terminals, and lists the DDC and the Beta Transformer Technology Corporation corresponding part numbers, as well as the MIL (DESC) drawing numbers (if applicable). Beta Transformer Technology is a direct subsidiary of DDC.

For both coupling configurations, the transformer that interfaces directly to the ACE/Mini-ACE component is called the isolation transformer. For the transformer (long stub) coupled configuration, the transformer that interfaces the stub to the bus is the coupling transformer. The turns ratio of the isolation transformer varies, depending upon the peak-to-peak output voltage of the specific ACE/Mini-ACE terminal.

The transmitter voltage of each model of the ACE varies directly as a function of the power supply voltage. The turns ratios of the respective transformers will yield a secondary voltage of approximately 28 volts peak-to-peak on the outer taps (used for direct coupling) and 20 volts peak-to-peak on the inner taps (used for stub coupling). For the Mini-ACE series terminals, transceiverless or +5V-only transceivers are available. The +5V-only transceiver terminals produce either a minimum of 18 Vp-p or 20 Vp-p differential output voltage on the stub based on whether standard testing or MIL-STD-1760 Amplitude testing has been ordered.

In accordance with MIL-STD-1553B, the turns ratio of the coupling transformer is required to be 1.0 to 1.4. For both coupling configurations, an isolation resistor is required to be in series with each leg connecting to the 1553 bus. This protects the bus against short circuit conditions in the transformers, stubs, or terminal components.

For most system applications, transformer (stub) coupling is preferred over direct coupling. Some of the advantages of transformer coupling are:

1) Looking from the 1553 bus towards the stub, the effect of the 1.4 to 1.0 stepdown of the coupling transformer will be to **double** the impedance of the stub/terminal combination, as seen by the bus. Since the stub impedance decreases as a

function of stub length due to distributed cable capacitance, this doubling effect serves to reduce the amount of impedance loading on the bus by individual terminals. For this reason, stub coupled terminals may be located up to 20 feet from the bus; the distance for direct coupled terminals is limited to 12 inches.

2) Looking from the isolation transformer down the stub (towards the bus), the impedance seen is Z_0. Therefore, the characteristic impedance of the stub cabling (78 ohms nominal) matches the stub's load impedance, minimizing reflections back toward the transmitter.

3) In a direct-coupled terminal, the main bus is not protected against a short circuit in the stub cabling. For the transformer coupled case, the bus is protected against such a fault.

4) A transformer coupled terminal provides improved DC and common mode isolation over a direct-coupled terminal.

TABLE 102. RECOMMENDED ISOLATION TRANSFORMERS

ACE PART NUMBER	TURNS RATIO		RECOMMENDED TRANSFORMER	
	DIRECT COUPLED	TRANSFORMER COUPLED	PLUG-IN	SURFACE MOUNT
BU-65170X1 BU-61580X1 BU-61582X1 BU-63825X1	1.41 : 1	2 : 1	BUS-25679, B-2203, DESC M21038/27-02	B-2387, B-2343, DESC M21038/27-12, DESC M21038/27-17, LPB-5002, LPB-5009, HLP-6002, HLP-6009
BU-65170X2 BU-61580X2 BU-61582X2 BU-63825X2	1 : 0:83 1.25 : 1 (See Note)	1 : 0.67	BUS-29854	LPB-5001, LPB-5008, HLP-6001 HLP-6008
BU-65170/71X3 BU-65170/71X6 BU-61580/81X3 BU-61580/81X6 BU-65178/79X3 BU-61588X3 BU-61688/89X3 BU-61585/86X3 BU-61585/86X6 BU-61582/83X3 BU-63825/925X3 BU-61582/83X6 BU-63825/925X6	1 : 2.5	1 : 1.79	Please see Transformer Considerations for +5V only (X3/X6) versions below.	
BU-61590X5	1 : 1	1.41 : 1	BUS-27765, B-2202, DESC M21038/27-01	B-2386, B-2342, DESC M21038/27-11, DESC M21038/27-16, LPB-5003, LPB-5010, HLP-6003, HLP-6010

NOTE: The B-2204, B-2388, and 2344 transformers have a slightly different turns ratio on the direct coupled taps than the turns ratio of the BUS-29854 direct-coupled taps. They do, however, have the same transformer coupled ratios. For transformer coupled applications, either transformer may be used. The transceiver in the BU-65170X2 and BU-61580X2 was designed to work with a 1:0.83 ratio for direct-coupled applications. For direct-coupled applications, the 1:0.83 turns ratio is recommended, but the 1.25:1 may be used. The 1.25:1 turns ratio will result in a slightly lower transmitter amplitude (approximately 3.6% lower) and a slight shift in the ACE's receiver threshold.

It is important to note that the transformer center tap on the "ACE/Mini-ACE" side, pin 2, must be grounded for all transceiver options except for the sinusoidal McAir/universal version of the ACE (i.e. BU-61590X5). The reason for this is that only one transformer leg is driven at any point in time when the ACE/Mini-ACE is transmitting. There is no instantaneous current in the alternate leg. The voltage on the alternate leg of the transformer will swing an equal amount in the opposite polarity due to autotransformer action. The sinusoidal transceiver, on the other hand, drives both legs of the transformer differentially. The sinusoidal transceiver will operate with the center tap (pin 2) grounded, but may exhibit problems such as an excessive dynamic offset.

Using the BU-61580X1 as an example, during the first half of a Command/Status sync pulse, no current flows from TX/RX while TX/RX* is driven to approximately -10 volts. Due to the autotransformer inductance, TX/RX will swing to about +10 volts. The resulting primary voltage is approximately 20 volts peak, or 40 (nominally 39) volts peak-to-peak.

8.1.1 Transformer Considerations for +5V Only (X3/X6) Versions

In selecting isolation transformers to be used with +5V only (X3/X6) versions, there is a limitation on the maximum amount of leakage inductance. If this limit is exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553. In addition, an excessive leakage imbalance may result in a transformer dynamic offset that exceeds 1553 specifications. The maximum allowable leakage inductance is 6 µH, and is measured as follows:

The side of the transformer that connects to the +5V only (X3/X6) version is defined as the “primary” winding. If one side of the primary is shorted to the primary enter tap, the inductance should be measured across the “secondary” (stub side) winding. This inductance must be less than 6 µH. Similarly, if the other side of the primary is shorted to the primary center tap, the inductance measured across the “secondary” (stub side) winding must also be less than 6 µH. the difference between these two measurements is the “differential” leakage inductance. This value must be less than 1.0 µH.

Beta Transformer Technology Corporation (BTTC), a subsidiary of DDC, manufactures transformers in a variety of mechanical configurations with the required turns ratios of 1:2.5 direct coupled, and 1:1.79 transformer coupled. TABLE 103 provides a listing of many of these transformers.

For further information, contact BTTC at 631-244-7393 or at www.bttc-beta.com.

TABLE 103. BTTC TRANSFORMERS FOR USE WITH +5 Volt versions only (X3, X6)	
TRANSFORMER CONFIGURATION	**BTTC PART NO.**
Single epoxy transformer, through-hole, 0.625 X 0.625, 0.250" max height	B-3067 B-3226
Single epoxy transformer, through-hole, 0.625 X 0.625, 0.220" max height	B-3818
Single epoxy transformer, flat pack, 0.625" X 0.625", 0.275" max height	B-3231
Single epoxy transformer, surface mount, 0.625" X 0.625", 0.275" max height	B-3227
Single epoxy transformer, surface mount, hi-temp solder, 0.625" X 0.625", 0.220" max height.	B-3819
Single epoxy transformer, flat pack, 0.625" X 0.625", 0.150" max height	LPB-5014
Single epoxy transformer, surface mount, 0.625" X 0.625", 0.150" max height	LPB-5015
Single epoxy transformer, through hole, transformer coupled only, 0.500” X 0.350”, 0.250” max height	B-3229
Dual epoxy transformer, twin stacked, 0.625" X 0.625", 0.280" max height	TST-9007
Dual epoxy transformer, twin stacked, surface mount, 0.625" X 0.625", 0.280" max height	TST-9017
Dual epoxy transformer, twin stacked, flat pack, 0.625" X 0.625", 0.280" max height	TST-9027
Dual epoxy transformer, side by side, through-hole, 0.930" X 0.630", 0.155" max height	TLP-1205
Dual epoxy transformer, side by side, flat pack, 0.930" X 0.630", 0.155" max height	TLP-1105
Dual epoxy transformer, side by side, surface mount, 0.930" X 0.630", 0.155" max height	TLP-1005
Dual epoxy transformer, side by side, surface mount, 1.410" X 0.750", 0.130" max height	DLP-7115 (see note)
Single metal transformer, hermetically sealed, flat pack, 0.630" X 0.630", 0.175" max height	HLP-6014
Single metal transformer, hermetically sealed, surface mount, 0.630" X 0.630", 0.175" max height	HLP-6015
NOT RECOMMENDED	DLP-7014 SLP-8007 SLP-8024

Notes:
1. DLP-7115 operates to +85°C max. All other transformers listed operate to +130°C max.

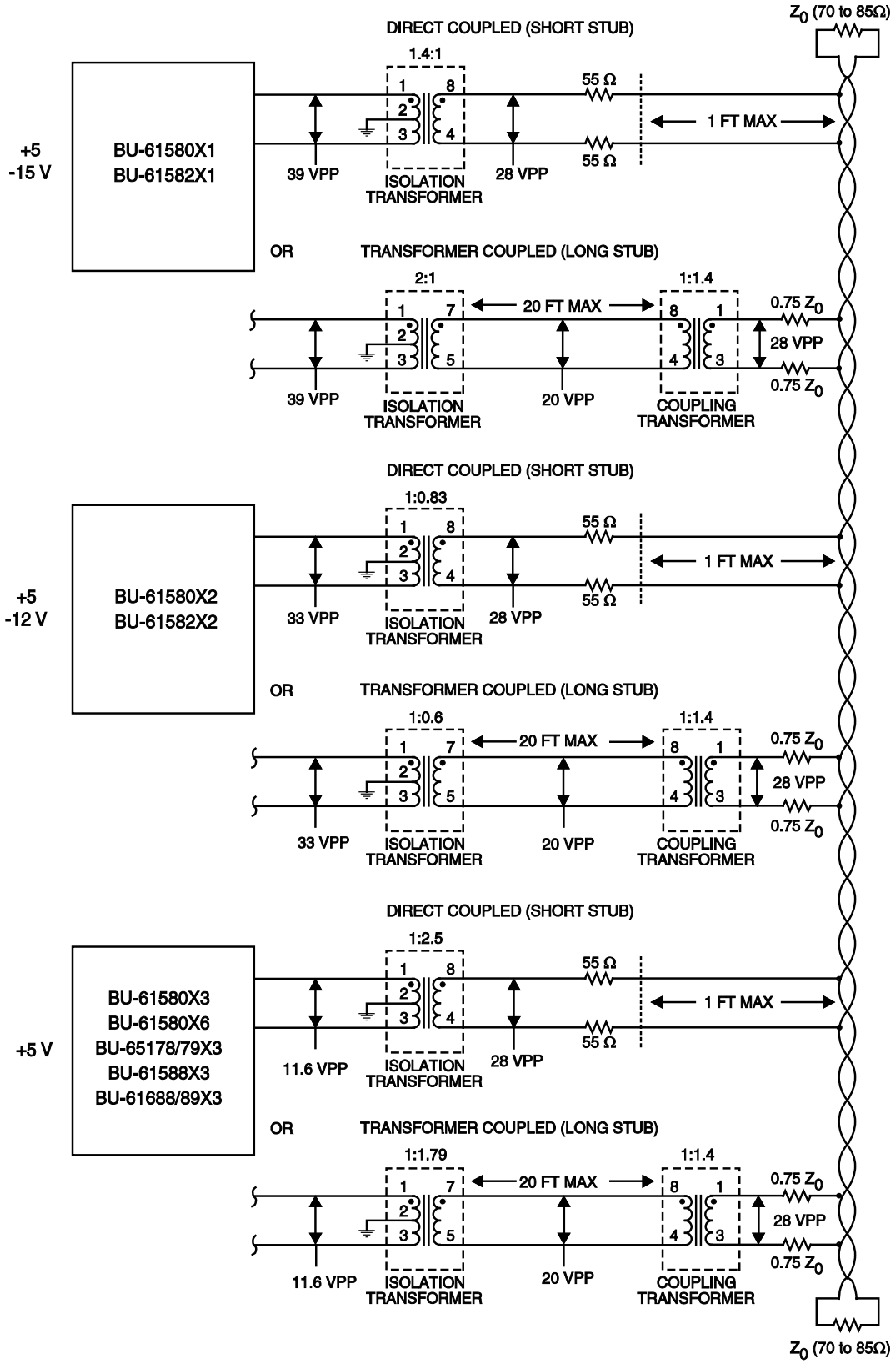
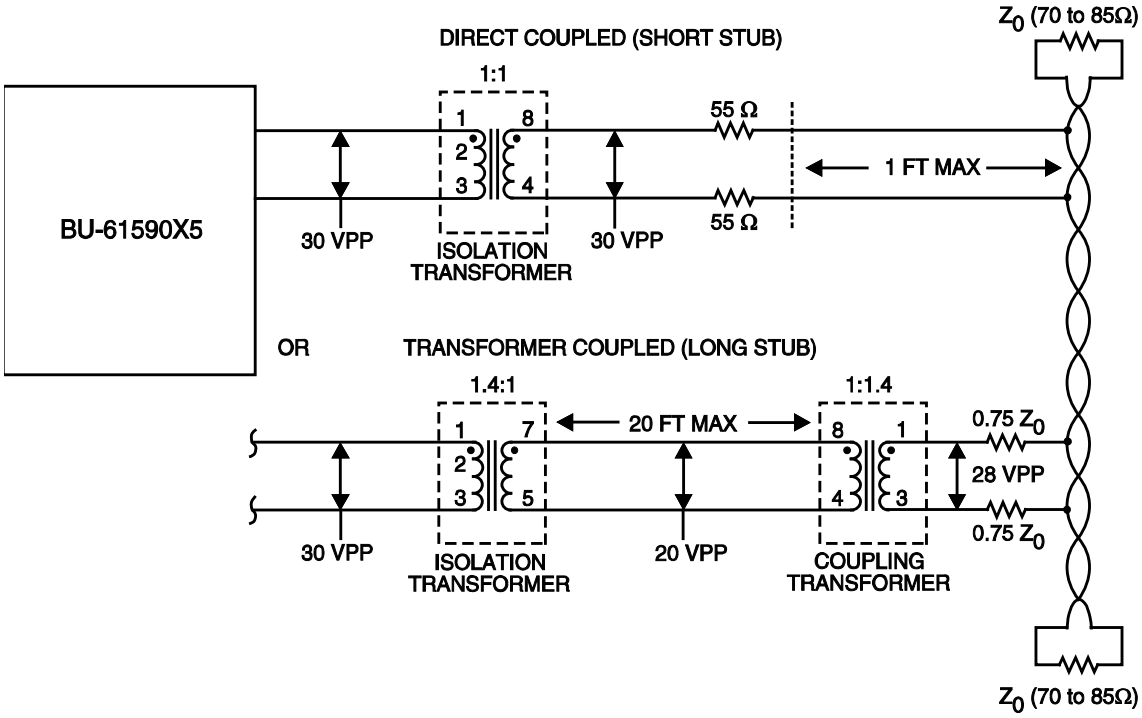


FIGURE 17. ACE/Mini-ACE INTERFACE TO 1553 BUS



Notes:
(1) Shown for one of two redundant buses that interface to the BU-65170, BU-65178/79, BU-61580, BU-61588, BU-61590, or BU-61688/89.
(2) Transmitted voltage level on 1553 bus is 6 Vp-p min, 7 Vp-p nominal, 9 Vp-p max.
(3) Required tolerance on isolation resistors is 2%. Instantaneous power dissipation (when transmitting) is approximately 0.5 W (typ), 0.8 W (max).
(4) Transformer pin numbering is correct for the DDC (e.g., BUS-25679) transformers. For the Beta transformers (e.g., B-2203) or the QPL-21038-31 transformers (e.g., M21038/27-02), the winding sense and turns ratio are mechanically the same, but the pin numbering is reversed. Therefore, it is necessary to reverse pins 8 and 4 or pins 7 and 5 for the Beta or QPL transformers (Note DDC transformer part numbers begin with a BUS-prefix, while Beta transformer part numbers begin with a B-prefix).

FIGURE 17. ACE/Mini-ACE INTERFACE TO 1553 BUS (continued)

8.2 POWER SUPPLY AND P.C. BOARD LAYOUT CONSIDERATIONS

With regard to the ACE/Mini-ACE terminal and the associated isolation transformers, there are a number of important factors to consider relating to component placement, circuit routing, and power distribution. Some of these factors include:

1) Isolation Transformers:
The isolation transformers should be placed **as physically close as possible** to the respective TX/RX pins on the hybrids. In addition to limiting the voltage drops in the analog signal traces when transmitting, reducing the hybrid-to-transformer spacing serves to minimize crosstalk from other signals on the board.

   Severe crosstalk can increase the ACE/Mini-ACE receiver's bit error rate beyond that allowed by MIL-STD-1553B. FIGURE 18 illustrates a typical P.C. board layout for the hybrid and isolation transformers.

2) Layout Considerations:
In addition to locating the transformers near the ACE/Mini-ACE, there are other additional practices, which minimize crosstalk. Avoid, if at all possible, running the 1553 analog signal traces in close proximity to other analog and digital signals on the board.

   Most importantly, avoid running another high-speed analog or digital signal in parallel with one of the 1553 bus traces on an adjacent layer of the P.C. board.

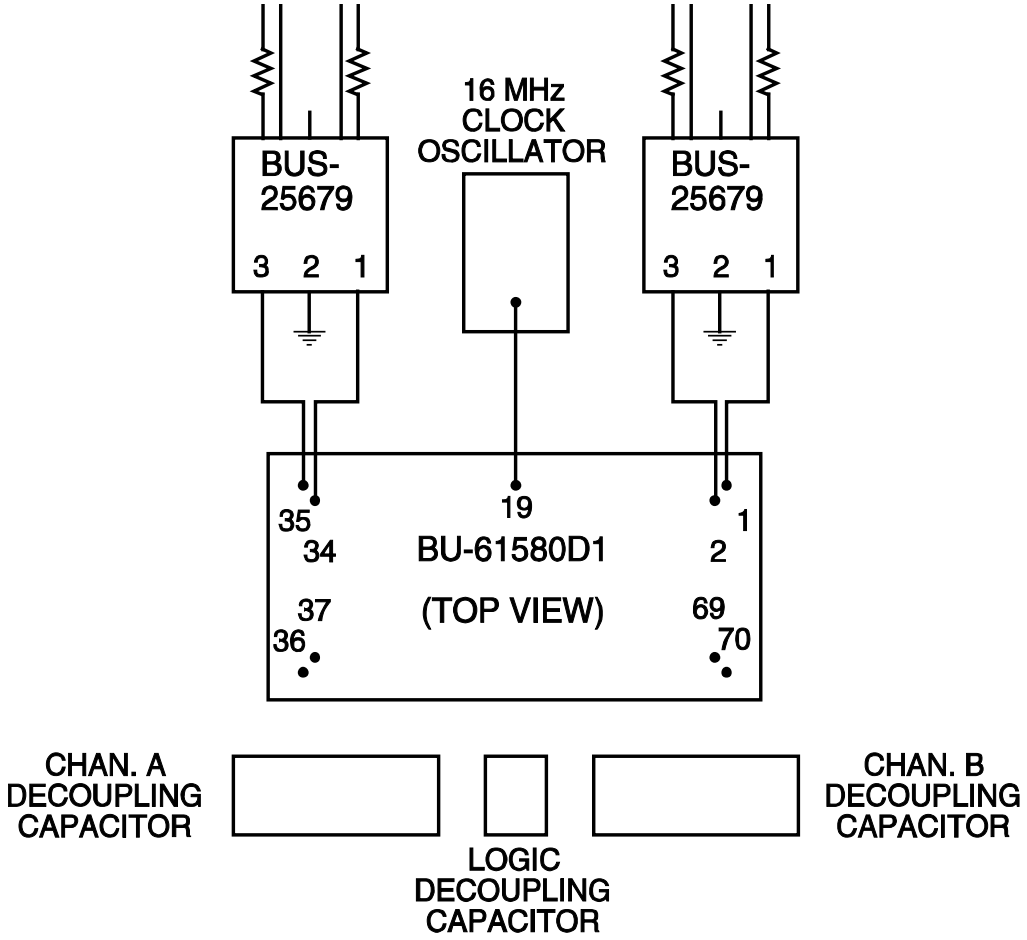
   The best layout practice is to avoid routing other parallel signals in any of the P.C. board layers in proximity to the 1553 signals.

3) Ground Planes:
As is the rule in all high speed digital circuits, it is good practice to use ground and power supply planes under the ACE as well as the host processor and associated buffers and glue logic.

Note: *It is very important that there be no ground and/or power supply planes underneath the Analog Bus Signal Traces, or the Transformers.*

This applies to the TX/RX Signals running from the ACE/Mini-ACE to the Transformers as well as from the Transformers to any connectors of cables leaving the board.

The reason for not using supply or ground planes under the analog signal traces is that the effect of the distributed capacitance will be to lower the input impedance of the terminal, as seen from the 1553 bus. MIL-STD-1553 requires a minimum input impedance of 2000 ohms for direct coupled terminals and 1000 ohms for transformer (stub) coupled terminals. If there are ground planes under the analog bus signal traces, it is likely that the terminal will not meet this requirement. It has been found that placing a ground plane under the body of the transformer only slightly effects the input impedance. A ground and/or power plane, therefore, may be placed under the transformer, if desired.



Notes:
1) Physical spacing between ACE/Mini-ACE and transformers must be kept to a minimum.
2) There must be **NO GROUND OR POWER SUPPLY PLANES** underneath the transformers or the signal traces running to or from the transformers.

FIGURE 18. P.C. BOARD LAYOUT EXAMPLE

4) Power and Ground Distribution:
Another important consideration is power and ground distribution. Refer to FIGURE 19. For the ACE/Mini-ACE hybrid/transformer combination, the high current path when the ACE/Mini-ACE is transmitting will be from the -15 volt (or -12 volt or +5 volt) power supply, through the ACE/Mini-ACE's transmitter output stage, through one leg of the isolation transformer to the transformer center tap. It is important to realize that the high current return path is **through the transformer center tap and not through the ACE/Mini-ACE's GNDA and GNDB pins.**

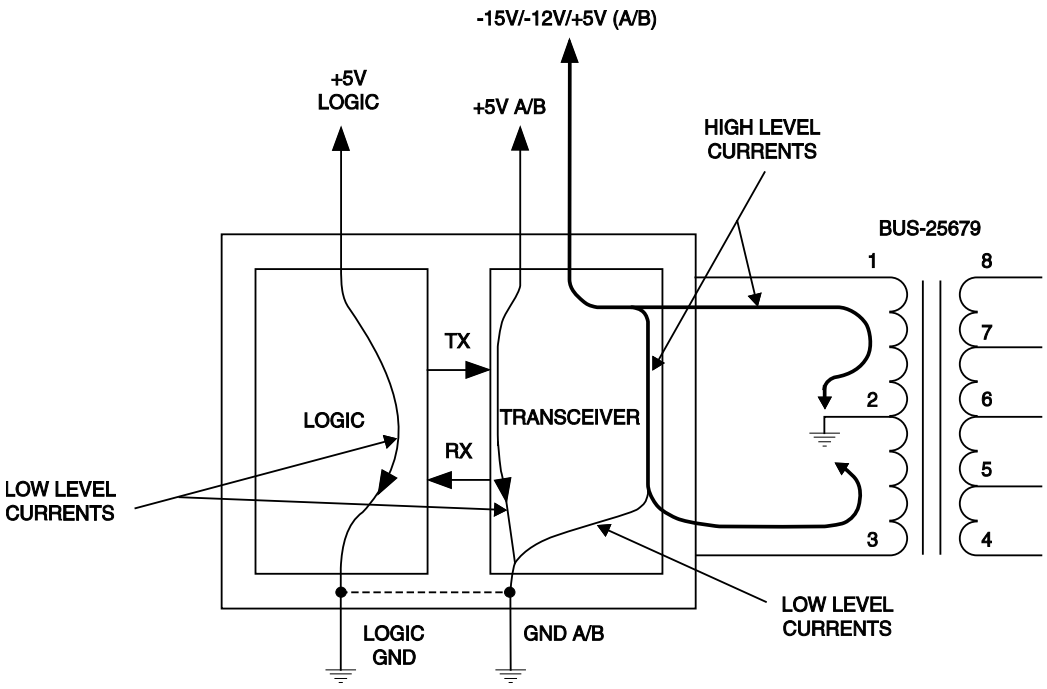
It is an important layout consideration to minimize the power supply distribution impedance along this path. Any resistance will result in voltage drops for the power supply input voltage, and can ultimately lower the transmitter output voltage, possibly below the minimum level required by MIL-STD-1553.

A worst-case analysis should ensure that with minimum supply voltage and calculated voltage drops, the transceiver voltage delivered between the ACE/Mini-ACE's transceiver supply pins and the center tap of the respective transformer will be no less than the specified minimum (-13.5, -10.5, or 4.5 volts).

In some cases, the voltage drop while transmitting may be reduced by means of large decoupling capacitors, but the best practice is to minimize the voltage drops in the power distribution.

5) Analog and Digital Grounds:
As far as the ACE/Mini-ACE and its associated transformers are concerned, the optimal circuit layout would entail a single ground plane for both the digital and analog (transceiver) circuits. While this is sometimes possible, in many applications there are system requirements for separate analog (-15V) and digital (+5V) power supply returns. In this case, the transformer center taps should be returned through the -15 V return.

In order to minimize the possibility of ground noise affecting the protocol/transceiver interface within the ACE, it is best that both the LOGIC GND pin as well as the GNDA and GNDB pins be connected to the +5V return, rather than the -15/-12V return. Note that the GNDA, GNDB, and Logic GND pins are tied common inside the ACE/Mini-ACE and **MUST** be connected to the same external ground.



NOTE: LOGIC GND and GNDA/B are internally tied together.

FIGURE 19. POWER/GROUND CURRENT DISTRIBUTION

6) Decoupling Capacitors: High-Frequency Ripple Reduction:

For the ACE/Mini-ACE terminal, two different size decoupling capacitor sizes are considered:

(a) A relatively small capacitor, with low effective series resistance (ESR) and effective series inductance (ESL) is usually needed to reduce high-frequency (1 MHz) power supply ripple. This is considered under this sub-heading.

(b) A relatively large capacitor **may** be needed to compensate for resistive voltage drops in the system power distribution. This is discussed under the next sub-heading.

For the +5 volt logic input and +5 VA/B inputs, 0.01 µ is generally sufficient.

For the transceiver power inputs, it is generally necessary to use small decoupling capacitors to eliminate the power supply ripple that may result from the 1 MHz and 2 MHz current pulses drawn by the ACE/Mini-ACE transceiver power inputs. A 2.2 µf low ESR/ESL capacitor should be sufficient.

For both cases, however, larger value decoupling capacitors may be needed in parallel if the voltage drops due to resistive distribution impedance are greater than the difference between the power supply's minimum output voltage and the ACE transceiver's minimum required input voltage. This is discussed under the next subheading.

7) Decoupling Capacitors: Power Distribution Voltage Drops:

For the -15VA/B transceiver power inputs, larger decoupling capacitors may be needed. If the minimum power supply voltage (as measured at the supply terminals) is greater than the ACE's required minimum, but not high enough to overcome the distribution voltage drops, it will generally be possible to achieve a satisfactory worst case minimum voltage by means of a decoupling capacitor. Particularly for the BUS-61555/65, this required value may be quite large; **to avoid the necessity of having to use such a large capacitor, it is important to minimize the voltage drops by means of low-impedance power distribution**.

Determination if Low Frequency Capacitor is Needed

Refer to the circuit illustrated in FIGURE 20. V_{in} is defined to be the rated minimum output voltage from the power supply. R_d is the series resistance of the power distribution path to the ACE's transceiver power inputs (-15 VA and VB). This includes resistance in the power supply return path, from the transformer center tap, as well as the power input path. R_i represents the effective resistance presented by the ACE's transceiver power inputs when the ACE is in its idle (nontransmitting) state. This may also take into account the currents drawn by other circuits in parallel with the ACE that draw current from the same power distribution path.

R_l represents the effective added parallel load resistance presented by the transceiver power inputs when the ACE is transmitting. If the "static" voltage drop results in a voltage of less than the transceiver's minimum supply voltage being presented between the ACE's transceiver supply pins and the transformer center tap, then either the power supply minimum output voltage V_{in} will have to be increased or the distribution resistance R_d will need to be reduced.

On the other hand, if the value of the voltage between the ACE's input and the center tap is greater than the minimum value when transmitting on the 1553 bus, then there is no

need for a large decoupling capacitor.

If, however, the voltage presented to the ACE's transceiver power inputs is greater than the required minimum when not transmitting, but less than the minimum when transmitting, a large decoupling capacitor may be necessary to sustain the power input voltage above the minimum level while the ACE is transmitting. If the power input voltage falls below the specified minimum during a transmission, the signal amplitude on the 1553 bus may fall below the MIL-STD-1553B minimum of 6 volts peak-to-peak (direct coupled).

The need for, and sizing of the decoupling capacitor is determined as a function of several variables. These include the power supply minimum output voltage, distribution resistance of the power and ground paths, the ACE's minimum transceiver input voltage, the length of the ACE's 1553 message transmission and the time between transmissions. The decoupling capacitor should be sized by a process of trial and error. As part of this process, the ACE should transmit message lengths and duty cycles representing the real system operation.

Note: *For Mini-ACE and Mini-ACE Plus terminals , it is recommended that the user locate external 10 µF Tantalum and 0.1 µF capacitors as close as possible to transceiver +5 V input pins 20 and 72 on the flat package (pins A9 and J3 on the PGA package). In addition, it is recommended that the user locate a 0.1 µF capacitor as close as possible to the logic +5 V input pin 37 on the flat package (pin D3 on the PGA package).*

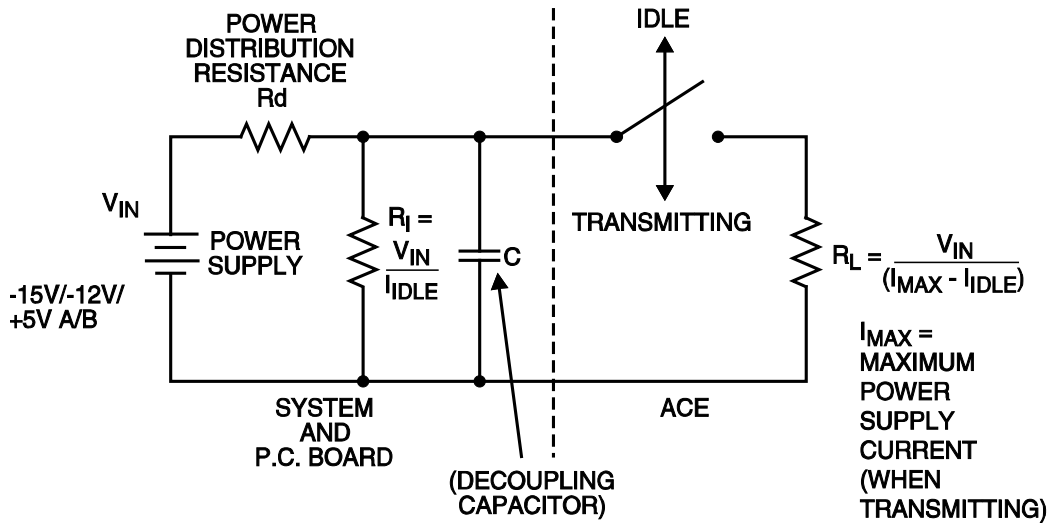


FIGURE 20. SIMPLIFIED EQUIVALENT CIRCUIT OF ACE TRANSMITTER

(All Versions Except BU-61590, BU-65620)

8) Avoid Switching Power Supplies and DC/DC Converters:

The use of switching power supplies or DC-to-DC converters on the same P.C. board as the ACE/Mini-ACE hybrid should be avoided. The switching noise may result in poor performance of the ACE/Mini-ACE's analog front end. Some of the possible problems include high output noise as well as degraded zero-crossing tolerance and bit error rate.

9) Location of Clock Oscillator:

As illustrated in FIGURE 18, the clock oscillator should be located as close as possible to the ACE/Mini-ACE's CLOCK IN input pin in order to minimize attenuation, distortion, and possible corrupting crosstalk from the clock signal.

8.3 ISOLATION TRANSFORMER INTERFACE TO SYSTEM CONNECTOR

The general practice in connecting the stub side of a transformer (or direct) coupled terminal to an external system connector is to make use of 78 ohm twisted-pair shielded cable. This minimizes impedance discontinuities. The decision of whether to isolate or make connections between the center tap of the isolation transformer's secondary, the stub shield, the bus shield, and/or chassis ground must be made on a system basis, as determined by an analysis of EMI/RFI and lightning considerations. In most systems, the secondary center tap is **not** grounded.

In some systems, it is specified that the 1553 terminal's input impedance must be measured at the system connector. This is despite the fact that the MIL-STD-1553B requirement is for it to be measured looking directly in from the bus side of the isolation transformer.

The effect of a relatively long stub cable will be to reduce the measured impedance. If this reduces the impedance below the required level of 1000 ohms (for transformer-coupled stubs), it is sometimes possible to increase the impedance somewhat by using a pair of coax wires (with the shields **ungrounded**), rather than a single twisted/shielded pair, for the stub connections.

The effect on the rest of the system performance of the bus signals coupled from the ungrounded shielded cables must be considered as a tradeoff against the increased terminal impedance.

8.4 “SIMULATED BUS” (LAB BENCH) INTERCONNECTIONS

For purposes of software development and system integration, it is generally not necessary to integrate the required couplers, terminators, etc., that comprise a complete MIL-STD-1553B bus. In most instances, a simplified electrical configuration will suffice. The interconnection methods illustrated in FIGURE 21 allow the ACE/Mini-ACE to be interfaced over a "simulated bus" to simulation and test equipment. The length of this simulated bus should not exceed 5 feet. It is important to note that the **termination resistors indicated are necessary** (if not already present within the test/simulation equipment) in order to ensure reliable communications between the ACE/Mini-ACE hybrid and the simulation/test equipment. As illustrated in FIGURE 21, the 78 ohm and 39 ohm termination resistors should be physically located as close as possible to the test/simulation equipment.

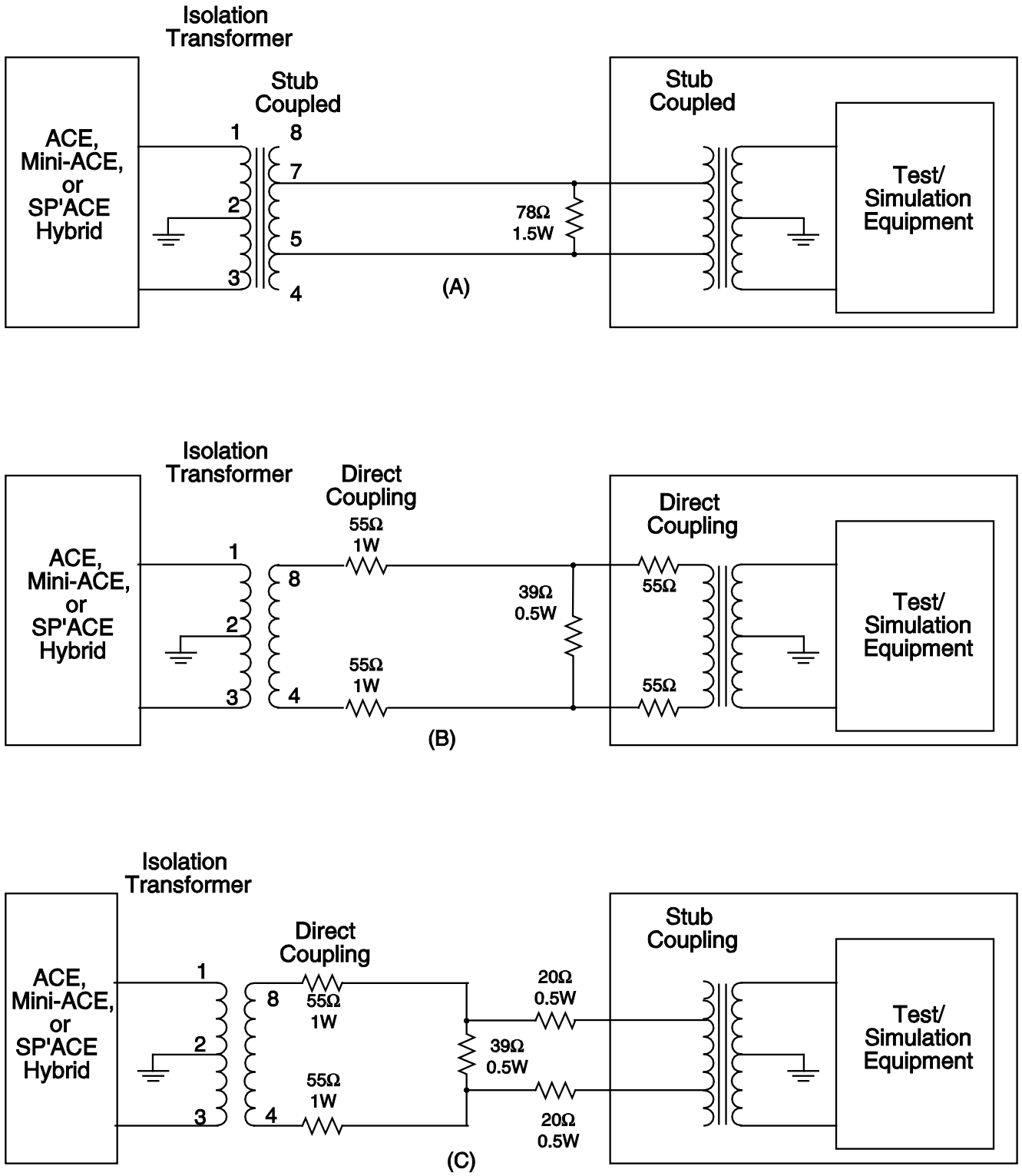
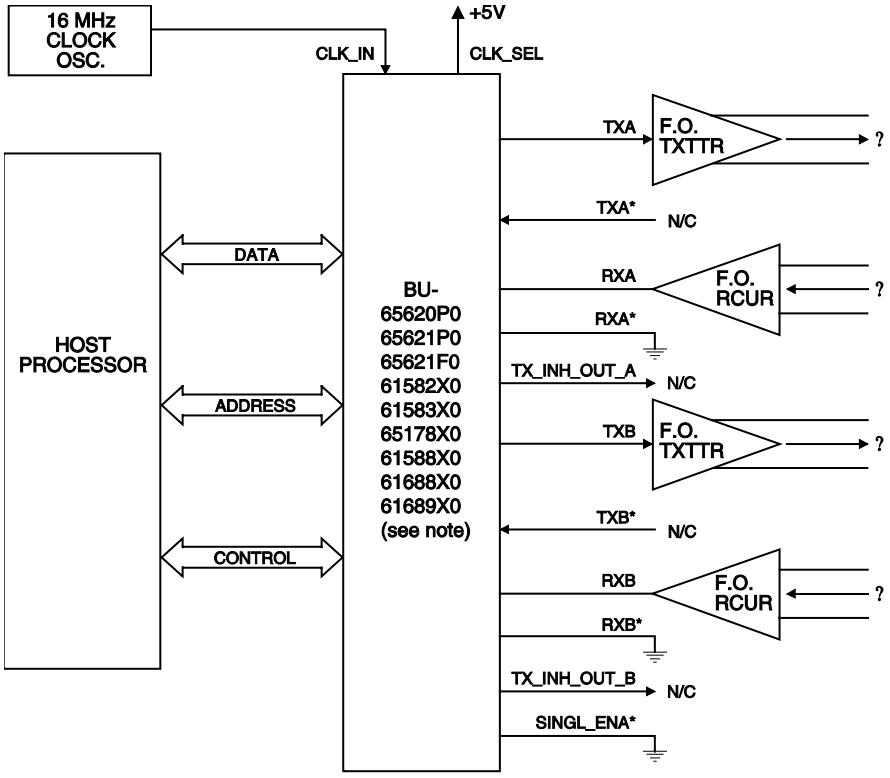


FIGURE 21. SIMULATED BUS INTERCONNECTIONS

(a) TRANSFORMER COUPLED ACE-TO-TRANSFORMER COUPLED EQUIPMENT;
(b) DIRECT COUPLED ACE-TO-TRANSFORMER COUPLED EQUIPMENT;
(c) DIRECT COUPLED ACE-TO-TRANSFORMER COUPLED EQUIPMENT.

8.5 BU-65620/21-, BU-61582/83- (BU-63825/925-), BU-65178-, BU-61588-, BU-61688/89-TO-FIBER OPTIC TRANSCEIVER INTERFACE

For MIL-STD-1773 applications involving a fiber optic transceiver, the BU-65620/21 digital monolithic version of the ACE, as well as the BU-61582/83 (BU-63825/925), 65178, 61588, and 61688/89 may be easily interfaced to a fiber optic transceiver. To facilitate this interface, the Manchester decoders provide a pin-programmable option allowing them to accept the single-ended input signals from a fiber-optic receiver. As shown in FIGURE 22, this option is activated by strapping the input signal $\overline{\text{SNGL_ENA}}$ to ground.



Note: For BU-65621X0, 61582X0 (63825X0), and 61583X0 (63925X0), the signal $\overline{\text{SNGL_ENA}}$ is **not** brought out. For these products, to enable operation with a single-ended receiver (e.g., fiber optic), bit 15 of Configuration Register #3, ENHANCED MODE ENABLED, **and** bit 14 of Configuration Register #5, SINGLE-ENDED SELECT, must be programmed to logic "1".

FIGURE 22. BU-65620/21-, BU-61582/83- (BU-63825/925-), BU-65178-, BU-61588-, BU-61688/89-TO-FIBER OPTIC TRANSCEIVER INTERFACE

8.6 LOGIC COMPATIBILITY

The ACE/Mini-ACE's logic signals provide compatibility with both TTL and CMOS type systems. The address and data bus I/O signals are capable of sourcing and sinking up to 6.4 mA. The other digital outputs are capable of sourcing and sinking up to 3.2 mA.

The ACE/Mini-ACE has **internal** (on-chip) pull-up resistors for all input and I/O signals. The value of the pull-up resistors is in the range from 10K to 100K ohms. Therefore, external pull-up signals **are not** generally required for any of the ACE/Mini-ACE's digital signals. One exception may involve the RT address inputs (RTAD4-0, RTADP). If these signals are not hardwired to +5V for logic "1," it is recommended that pull-up resistors (10K ohms or less) be used to provide improved noise immunity.

The SP'ACE's (BU-61582, BU-61583, and BU-65621) logic signals are CMOS compatible. The digital outputs are capable of sourcing and sinking up to 8 mA.

The majority of the SP'ACE II's (BU-63825, BU-63925) logic signals are TTL compatible (see datasheet for details). The digital outputs are capable of sourcing and sinking up to 8 mA.

The SP'ACE and SP'ACE II also have **internal** (on-chip) pull-up resistors on the address bus (A15-A0) data bus (D15-D0), RT address (RTAD4-RTAD0, RTADP), $\overline{\text{MEMWR}}/\overline{\text{ZERO_WAIT}}$, $\overline{\text{DTREQ}}/16/\overline{8}$, and $\overline{\text{DTACK}}/\text{POLARITY_SEL}$ inputs. All other SP'ACE and SP'ACE II inputs have no pull-ups.

8.7 HOST PROCESSOR AND MEMORY INTERFACE

The ACE/Mini-ACE provides a great deal of flexibility for interfacing to a host processor and optional external memory. As shown in FIGURE 1, there are 14 control signals (13 for the Mini-ACE series terminals), 6 of which are dual purpose, for the processor/memory interface. FIGURE 23 through FIGURE 28 illustrate six of the configurations that may be used for interfacing an ACE/Mini-ACE to a host processor bus. The various possible configurations serve to reduce to an absolute minimum the amount of "glue" logic required to interface to 8-, 16-, and 32-bit processor buses. In addition, features are included to facilitate interfacing to processors that do not have a "wait state" type of handshake acknowledgment. Finally, the ACE/Mini-ACE supports a reliable interface to an external dual port RAM. This type of interface minimizes the portion of the available processor bandwidth required to access its internal 1553 RAM.

8.8 ADDRESS MAPPING: WORDS VS. BYTES

It is important to note that with respect to the ACE/Mini-ACE's address bus, A15 through A0, all address mapping is **word oriented**, rather than byte oriented. Although there are a few exceptions (a significant one being the MIL-STD-1750A instruction set architecture), the inherent address mapping for most standard 8-, 16-, and 32-bit microprocessors is **byte oriented**. This difference in mapping convention must be taken into account when assigning pointer values and making CPU accesses to the ACE/Mini-ACE's internal data structures (stack, lookup tables, data tables, etc.) in the ACE/Mini-ACE's shared RAM address space. That is, in terms of the CPU's memory map, the address of these data structures, relative to the ACE/Mini-ACE's base memory address, will be **double** the value of the pointer that is stored in the ACE/Mini-ACE's shared RAM.

For interfacing to most 16-bit microprocessors, the processor's A1 signal connects to the ACE/Mini-ACE's A0 pin, processor A2 connects to the ACE/Mini-ACE's A1 pin, etc. For interfacing to an 8-bit microprocessor **(Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)**, the processor A0 output connects to the ACE/Mini-ACE's MSB/LSB input, the processor's A1 output connects to the ACE/Mini-ACE's A0 pin, processor A2 connects to the ACE/Mini-ACE's A1 pin, etc.

While the ACE/Mini-ACE's internal shared RAM is intended primarily for the buffering of 1553 messages and related pointer data, it is important to noted that there is **no restriction** prohibiting the use of this RAM for general purpose program memory or "scratchpad" data memory.

8.9 16-BIT BUFFERED MODE

The 16-bit buffered mode (FIGURE 23) is the most common interface configuration used. It provides a direct, shared RAM interface to a 16-bit or 32-bit microprocessor. In this mode, the ACE/Mini-ACE's internal address and data buffers provide the necessary isolation between the host processor's address and data buses and the corresponding internal memory buses. In the buffered mode, the 1553 shared RAM address space is limited to the BU-65170/61580's internal 4K words (or 12K for BU-61585) of internal RAM. For the Mini-ACE series terminals, the buffered mode provides 4K of internal RAM on the BU-65178/79 and BU-61588. For the BU-61688/89, 64K of internal RAM is available. The 16-bit buffered mode offers a pair of pin-programmable options.

In the shared RAM configuration, the processor **always** has access to its own buses. That is, the ACE/Mini-ACE will **never** request the use of the CPU buses. This provides the advantage of allowing the ACE/Mini-ACE to access its buffer RAM while the CPU is able to **simultaneously** use

its buses to access its memory or I/O. In this way, a shared RAM interface utilizes less of the CPU's bandwidth than does a DMA interface.

In the 16-bit buffered mode, note that TRANSPARENT/$\overline{\text{BUFFERED}}$ is strapped to logic "0," while 16/$\overline{8}$-BIT is connected to logic "1." The input signal ADDR_LAT may be used to demultiplex the address bus. For examples, for some Intel microprocessors (i.e., Intel 80186), the CPU's ALE output should be connected to ADDR_LAT. If not used, ADDR_LAT should be connected to logic "1."

The logic sense of the RD/$\overline{\text{WR}}$ control input is selectable by means of the POLARITY_SEL input. For example, POLARITY_SEL should be connected to logic "1" to write on RD/$\overline{\text{WR}}$ low for Motorola 680X0 processors; POLARITY_SEL should be connected to logic "0" to write on RD/$\overline{\text{WR}}$ high for Intel i960 series processors. By strapping the input signal $\overline{\text{ZERO_WAIT}}$ to logic "1," the ACE/Mini-ACE may be interfaced to processors that have an acknowledge type of handshake input to accommodate hardware controlled wait states; most current processor chips have such an input. For this type of processor, the ACE/Mini-ACE will assert its $\overline{\text{READYD}}$ output low only after it has latched data to be written or has presented data to be read on D15-D0. In the non-zero wait mode, the host processor terminates the transfer cycle by releasing $\overline{\text{STRBD}}$ high after the ACE/Mini-ACE has asserted $\overline{\text{READYD}}$ low.

By strapping $\overline{\text{ZERO_WAIT}}$ to logic "0," it is possible to easily interface the ACE/Mini-ACE to processors that **do not** have an acknowledge type of handshake input. An example of such a processor is Analog Device's ADSP2101 DSP chip. In this configuration, the processor can clear its strobe output (the ACE/Mini-ACE's $\overline{\text{STRBD}}$ input) before the access to the ACE/Mini-ACE has been completed (before $\overline{\text{READYD}}$ goes low).

In the buffered configuration, the host initiates an access to the ACE/Mini-ACE's internal RAM or registers by asserting the signals $\overline{\text{SELECT}}$, $\overline{\text{STRBD}}$, MEM/$\overline{\text{REG}}$, and RD/$\overline{\text{WR}}$. $\overline{\text{SELECT}}$ and MEM/$\overline{\text{REG}}$ are generally the outputs of an address decoder. $\overline{\text{SELECT}}$ must be asserted low to access the ACE/Mini-ACE's RAM or registers. MEM/$\overline{\text{REG}}$ must be presented high for memory access and low for register access. If POLARITY_SEL is logic "1," RD/$\overline{\text{WR}}$ must be presented high to read and low to write; if POLARITY_SEL is logic "0," RD/$\overline{\text{WR}}$ must be presented low to read and high to write. $\overline{\text{STRBD}}$ is the main processor control input to the ACE/Mini-ACE to control the length of an access cycle.

8.9.1 Zero Wait Configuration

Some microprocessors **do not** have a "strobe/acknowledge" type of handshake mechanism. In this case, the ACE/Mini-ACE's "zero wait" interface configuration may be used by strapping $\overline{\text{ZERO_WAIT}}$ to logic "0." In this mode, the CPU is able to release $\overline{\text{STRBD}}$ high **before** the ACE/Mini-ACE's $\overline{\text{READYD}}$ output transitions from high to low. The high-to-low transition of $\overline{\text{READYD}}$ indicates the end of the ACE/Mini-ACE's internal transfer cycle. This mode takes advantage of the ACE/Mini-ACE's internal address and data latches and added control logic and serves to minimize the amount of "glue" logic required.

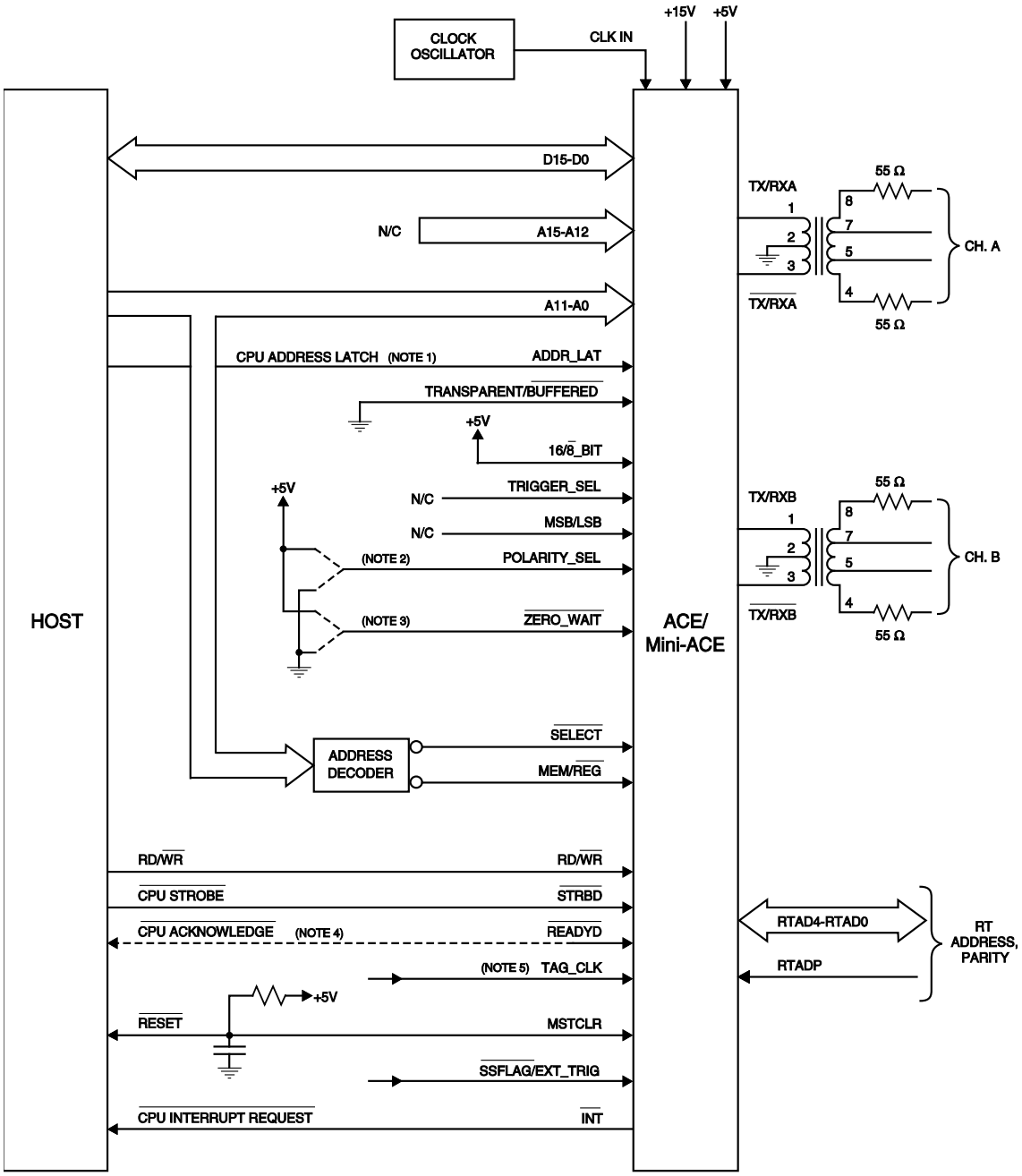
The following considerations are necessary when reading the Interrupt Status Register in 16-bit zero wait mode. This is to ensure that subsequent interrupt events after a triggering read of an ISR result in bit(s) being set in the respective ISR (i.e. to avoid interrupting events becoming “lost”).

- For 16-bit zero wait mode, all transfers are triggering. However, it is important that for the operation in which the ISR value is actually read – that is, the read transfer *after* the ISR address has been presented – that some register or memory address *other than* that of the ISR be presented. This can be register address 0x0000, or some other register or memory address.

In the 16-bit zero wait mode, the CPU writes a word by presenting the address and data for the word to be written on A15-A0 and D15-D0 respectively. To implement a single zero wait read operation, the host processor must perform **two** read accesses to the ACE/Mini-ACE. During the first access, the address and transfer type indication (memory or register) of the location to be read must be asserted on A15-A0 and MEM/$\overline{\text{REG}}$, respectively. The data read on D15-D0 during this cycle **should be ignored ("thrown away")**. During the **second** read access, the ACE/Mini-ACE presents the data corresponding to the address presented on the **first** access on D15-D0. If the CPU performs a multi-word read burst, the address for the **next** word should be presented on A15-A0 on the same cycle that data is read from D15-D0. That is, for a multi-word read transfer, the address presented should always be **one location ahead** of that of the data being read.

In the zero wait mode, $\overline{\text{STRBD}}$ must be asserted low for a minimum of 20 ns. Reference FIGURE 23 and FIGURE 28. If $\overline{\text{STRBD}}$ is not sampled low for two rising edges of the clock input CLK_IN, $\overline{\text{READYD}}$ will go high within 40 ns after the rising edge of $\overline{\text{STRBD}}$. If $\overline{\text{STRBD}}$ is sampled low for two rising edges of CLK_IN, $\overline{\text{READYD}}$ will go high within 40 ns after the second rising clock edge. In either case, the ACE/Mini-ACE's internal transfer cycle will not begin until after the second rising edge of CLK_IN

and $\overline{\text{STRBD}}$ is returned to logic "1." When the ACE/Mini-ACE initiates the internal transfer, it asserts the output signal $\overline{\text{IOEN}}$ low for four clock cycles. When the ACE/Mini-ACE completes the internal transfer cycle, $\overline{\text{IOEN}}$ clears high. One-half clock cycle after $\overline{\text{IOEN}}$ goes high, the ACE/Mini-ACE acknowledges completion of the transfer by asserting $\overline{\text{READYD}}$ low. In the zero wait mode, the CPU can determine if the ACE/Mini-ACE has completed its transfer cycle by polling the value of the $\overline{\text{READYD}}$ output.



NOTES:

1. CPU ADDRESS LATCH SIGNAL PROVIDED BY PROCESSORS WITH MULTIPLEXED ADDRESS/DATA BUSES.
2. IF POLARITY_SEL = "1", RD/$\overline{WR}$ IS HIGH TO READ, LOW TO WRITE.
   IF POLARITY_SEL = "0", RD/$\overline{WR}$ IS LOW TO READ, HIGH TO WRITE.
3. $\overline{ZERO_WAIT}$ SHOULD BE STRAPPED TO LOGIC "1" FOR NON-ZERO WAIT INTERFACE AND TO LOGIC "0" FOR ZERO WAIT INTERFACE.
4. CPU ACKNOWLEDGE PROCESSOR INPUT ONLY FOR NON-ZERO WAIT TYPE OF INTERFACE.
5. TAG_CLK NOT AVAILABLE ON MINI-ACE SERIES TERMINALS.

FIGURE 23. INTERCONNECTION DIAGRAM FOR 16-BIT BUFFERED MODE

8.10 16-TRANSPARENT MODE

Similar to the 16-bit buffered mode, the 16-bit transparent mode (FIGURE 24) supports a shared RAM interface to a host CPU. The transparent mode offers the advantage of allowing the buffer RAM size to be expanded to up to 64K words, using external RAM. For Mini-ACE Plus terminals BU-61688/89 that contain 64K of internal RAM, the user may operate in transparent mode, but the combination of internal and external RAM may not exceed 64K. A disadvantage of the transparent mode is that external address and data buffers are required to isolate the processor buses from the ACE/Mini-ACE buses.

In the transparent mode, the host is able to access up to 64K of external RAM. Like the buffered mode, the host is able to use its data/address buses while the ACE/Mini-ACE **simultaneously** accesses its internal or external shared RAM. Note that in the transparent configuration, external tri-state buffers are required to isolate the CPU's data/address buses from the ACE/Mini-ACE's RAM buses.

TABLE 104 summarizes the operation of the ACE/Mini-ACE's tri-state address and data bus buffers for the 16-bit buffered and transparent modes.

TABLE 104. OPERATION OF ADDRESS AND DATA BUFFERS FOR 16-BIT INTERFACES

TRANSPARENT/ BUFFERED MODE	CPU/1553 ACCESS	READ/WRITE	INT/EXT RAM (NOTE 1)	ADDRESS BUFFERS	DATA BUFFERS
Buffered	CPU	WRITE	INT	⟶	⟶
Buffered	CPU	READ	INT	⟶	
Buffered	1553	WRITE	INT	Hi-Z	Hi-Z
Buffered	1553	READ	INT	Hi-Z	Hi-Z
Transparent	CPU	WRITE	INT	⟶	⟶
Transparent	CPU	WRITE	EXT	⟶	Hi-Z
Transparent	CPU	READ	INT	⟶	⟵
Transparent	CPU	READ	EXT	⟶	Hi-Z
Transparent	1553	WRITE	INT	⟵	⟵
Transparent	1553	WRITE	EXT	⟵	⟵
Transparent	1553	READ	INT	⟵	⟵
Transparent	1553	READ	EXT	⟵	⟶

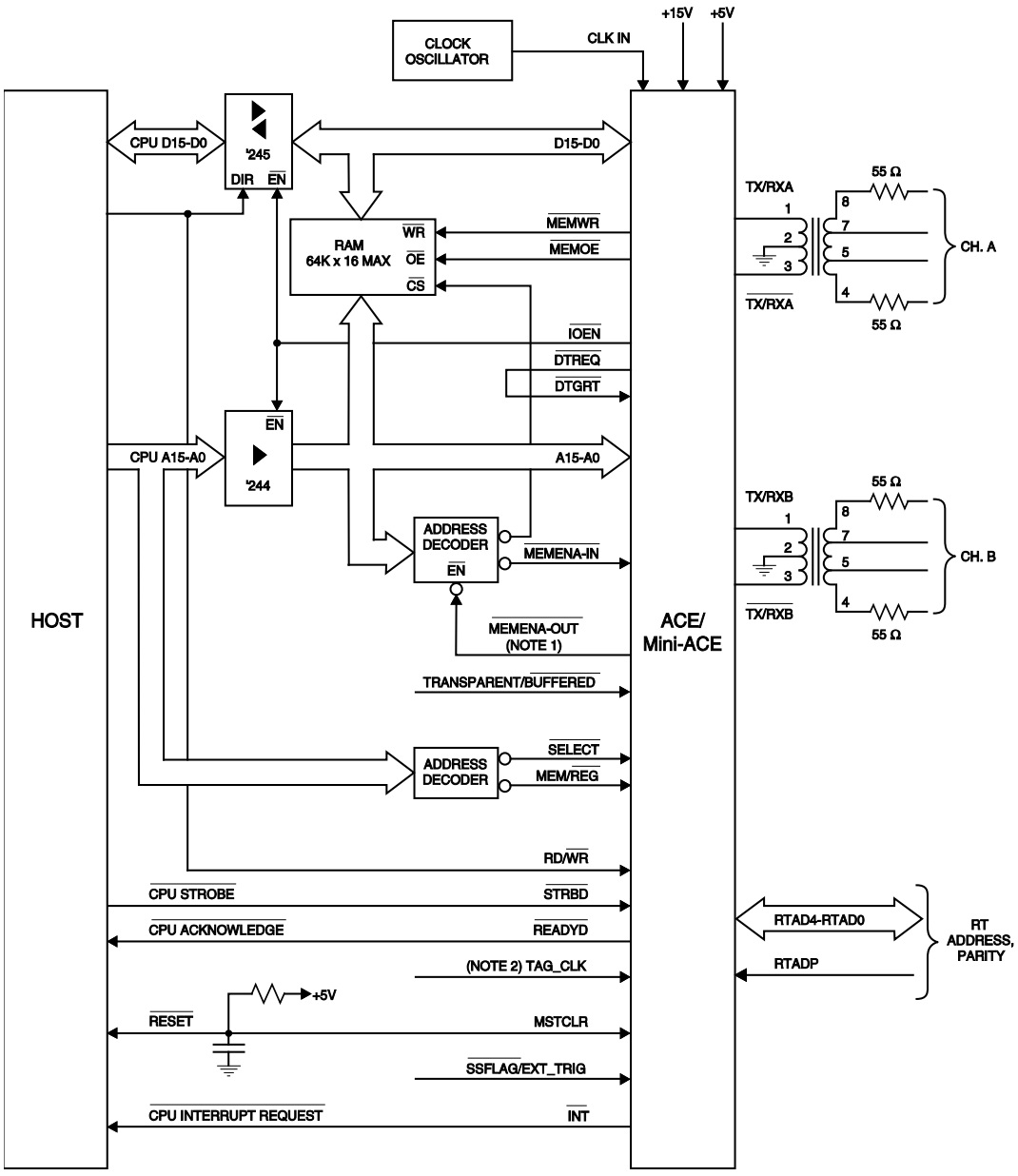
Notes:

(1) The ACE/Mini-ACE distinguishes between internal (INT) and external (EXT) RAM by means of the input signal $\overline{\text{MEMENA}-\text{IN}}$. $\overline{\text{MEMENA}-\text{IN}}$ is low for internal RAM access, high for external RAM access.

(2) "⟶" indicates buffers enabled in direction from external processor bus towards internal memory bus. "⟵" indicates buffers enabled in direction from internal memory bus towards external processor bus. " Hi-Z" indicates buffers are in high impedance (tri-state) condition.

In the transparent mode (reference FIGURE 24), the memory control signals $\overline{\text{MEMENA-OUT}}$, $\overline{\text{MEMWR}}$, and $\overline{\text{MEMENA-IN}}$ must be connected to the respective control inputs of external RAM. Note, for the Mini-ACE series terminals, the $\overline{\text{MEMENA-OUT}}$ signal is not available. The $\overline{\text{MEMENA-OUT}}$ signal may be generated by logically AND'ing $\overline{\text{DTACK}}$ and $\overline{\text{IOEN}}$. If the ACE/Mini-ACE's internal RAM is used, the address decoder output to select this RAM must be connected to the ACE/Mini-ACE's $\overline{\text{MEMENA-IN}}$ input. If the ACE/Mini-ACE's internal RAM is not used, $\overline{\text{MEMENA-IN}}$ must be connected to logic "1." As shown in the figure, the ACE/Mini-ACE's $\overline{\text{IOEN}}$ output should be connected to the tri-state enable inputs of the external address and data buffers.

In the transparent mode, there is an extra clock cycle (four, instead of the three in buffered mode) between the falling edge of $\overline{\text{IOEN}}$ and the falling edge of the acknowledge (handshake) output $\overline{\text{READYD}}$. This extra time is provided to accommodate the enable times and propagation delays associated with the external tri-state buffers.



NOTES:

1. MEMENA-OUT IS NOT AVAILABLE ON THE MINI-ACE SERIES TERMINALS BUT MAY BE REPLACED BY LOGICALLY OR'ING DTACK WITH IOEN.
2. TAG_CLK NOT AVAILABLE ON MINI-ACE SERIES TERMINALS.

FIGURE 24. INTERCONNECTION DIAGRAM FOR 16-BIT TRANSPARENT MODE

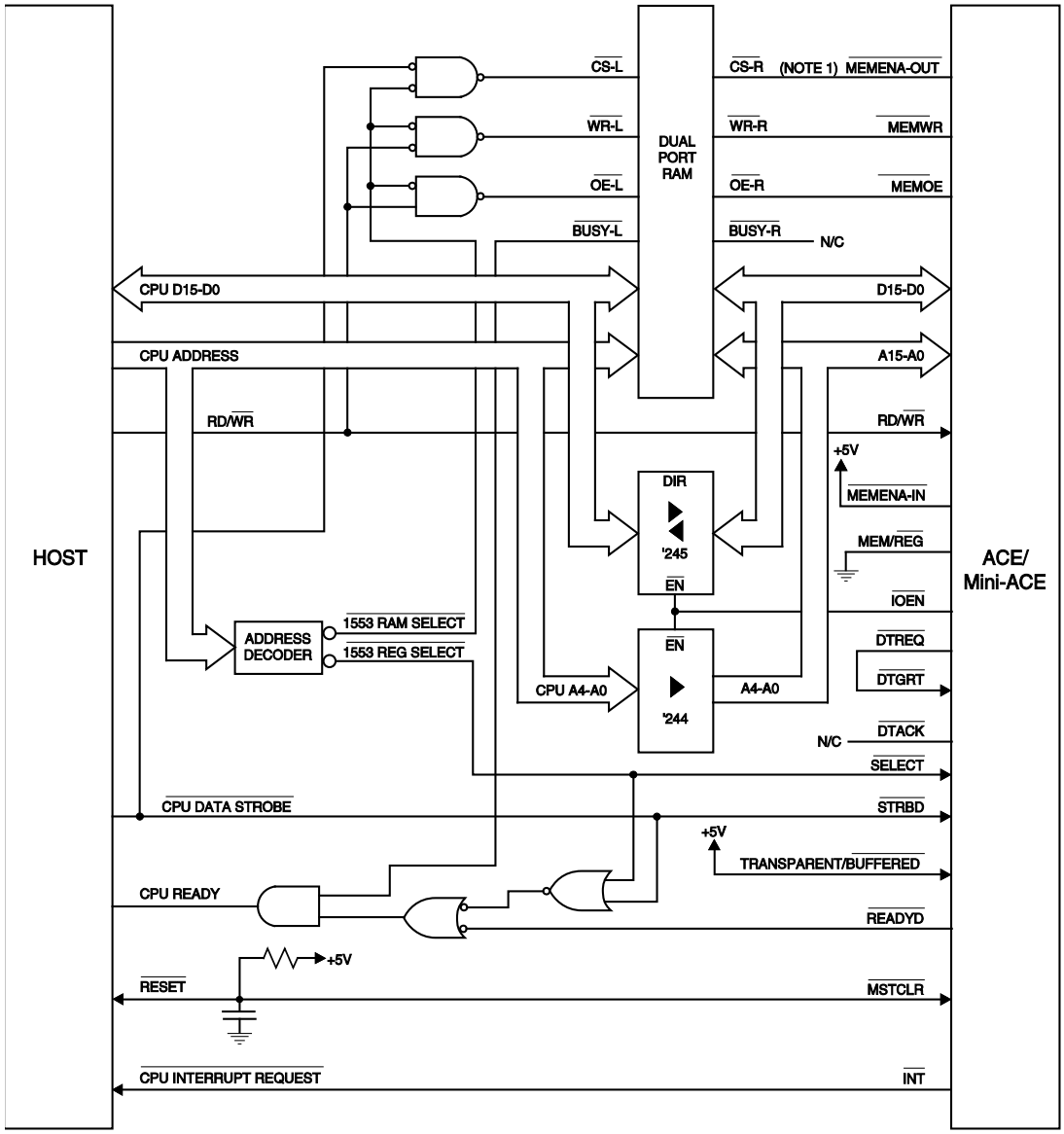
A modified version of the transparent mode involves the use of external dual port RAM, rather than conventional static RAM. Reference FIGURE 25. This allows the host to access RAM very quickly (the only limitation is essentially the RAM speed); the ACE/Mini-ACE arbitration delays are eliminated in this instance. The worst case delay time occurs only during simultaneous access by the host CPU and the ACE/Mini-ACE to the same memory address; in general, this will occur very rarely and the delay is limited to approximately 250 ns.

In the dual port RAM interface, one side of the RAM is accessed by the host CPU, while the other side is accessed by the ACE/Mini-ACE's "1553" logic, by means of the memory control signals. Note that tri-state buffers are required on the address and data buses in order for the CPU to be able to access the ACE/Mini-ACE's internal registers. Note that the ACE/Mini-ACE input signal MEM/$\overline{\text{REG}}$ is hardwired to logic "0," and $\overline{\text{SELECT}}$ is connected to the address decoder output $\overline{\text{1553REGSELECT}}$ to enable the register accesses. The signal CPU READY is asserted low (indicating "not ready") under either of two conditions:

1) When the dual port RAM's $\overline{\text{BUSY-L}}$ output is asserted, indicating that the host tried to access the same location currently being accessed by the 1553 logic. Note that with most dual port RAM chips, a "Busy" condition will only result when both sides are performing an access to the same address location.

2) CPU READY will be asserted low during the time of a register access, prior to the completion of the ACE/Mini-ACE's transfer cycle. That is, during the time that the $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ inputs are asserted low, but before $\overline{\text{READYD}}$ is asserted low.

Note: *in this configuration, the dual port RAM's* $\overline{\text{BUSY-R}}$ *output is not connected. As a result, it is important to note that the length of the pulse (low) presented on the dual port RAM's* $\overline{\text{CS-L}}$ *input (derived from the CPU's* $\overline{\text{CPU DATA STROBE}}$ *output) must be less than 100 ns. If* $\overline{\text{CS-L}}$ *is asserted low for too long, it may cause the ACE/Mini-ACE's "1553" logic to miss a transfer cycle. This could have the effect of corrupting a 1553 message (on an ACE/Mini-ACE read cycle) or causing the ACE/Mini-ACE to not store a word in the dual port RAM (on an ACE/Mini-ACE write cycle).*



NOTES:

1. MEMENA-OUT IS NOT AVAILABLE ON THE MINI-ACE SERIES TERMINALS BUT MAY BE REPLACED BY LOGICALLY OR'ING DTACK WITH IOEN.

FIGURE 25. INTERCONNECTION DIAGRAM FOR 16-BIT DUAL PORT RAM MODE

8.11 16-BIT DMA MODE

FIGURE 26 illustrates the connections for the 16-bit Direct Memory Access (DMA) mode. In this configuration, use of the address and data buses is arbitrated by the host processor, rather than by the ACE/Mini-ACE. The arbitration involves the three DMA control signals Request ($\overline{\text{DTREQ}}$), Grant ($\overline{\text{DTGRT}}$), and Acknowledge ($\overline{\text{DTACK}}$). The DMA interface allows the ACE/Mini-ACE to interface to large amounts of system RAM. For system address spaces greater than 64K words, it is necessary for the host processor to provide a page register for the upper address bits (above A15) when the ACE/Mini-ACE accesses the RAM ($\overline{\text{DTACK}}$ is asserted low).

The internal RAM is accessible through the standard ACE/Mini-ACE interface ($\overline{\text{SELECT}}$, $\overline{\text{STRBD}}$, $\overline{\text{READYD}}$, etc). The host CPU may access external RAM by means of the ACE/Mini-ACE's arbitration logic and output control signals, as illustrated in FIGURE 26. Alternatively, control of the RAM may be multiplexed between the host processor and the ACE/Mini-ACE, as shown in FIGURE 27. The latter requires the use of external logic, but allows the processor to access the RAM directly at the full access speed of the RAM, rather than waiting for the ACE/Mini-ACE handshake acknowledge output ($\overline{\text{READYD}}$).

In the DMA configuration, the host processor controls access to the address and data buses by means of a request/grant/acknowledge handshake. Refer to FIGURE 33 and FIGURE 34. When the 1553 terminal needs to transfer a word or block of words to RAM, it requests use of the buses from the host CPU by asserting its $\overline{\text{DTREQ}}$ (Data Transfer Request) output low. When the host CPU completes its current instruction cycle, it relinquishes use of the buses by asserting $\overline{\text{DTGRT}}$ (Data Transfer Grant) low. When the ACE/Mini-ACE samples $\overline{\text{DTGRT}}$ low on a rising edge of CLK_IN, it asserts $\overline{\text{DTACK}}$ (Data Transfer Acknowledge) low to indicate that the ACE/Mini-ACE has accepted control of the buses.

One clock cycle later, the ACE will assert the output signal $\overline{\text{MEMENA-OUT}}$ **(Note that the Mini-ACE series terminals do not make the** $\overline{\text{MEMENA-OUT}}$ **signal available, but the** $\overline{\text{MEMENA-OUT}}$ **signal may be replaced by logically AND'ing** $\overline{\text{DTACK}}$ **and** $\overline{\text{IOEN}}$**)**. This signal can be connected to an external address decoder to derive $\overline{\text{MEMENA-IN}}$ for internal RAM access, or $\overline{\text{CS}}$ input(s) to external RAM. $\overline{\text{MEMENA-OUT}}$ and $\overline{\text{DTACK}}$ stay asserted for four clock cycles (200 ns at 20 MHz, 250 ns at 16 MHz, 333 ns at 12 MHz, 400 ns at 10 MHz) to complete a single-word transfer cycle. For a read cycle, the ACE/Mini-ACE output $\overline{\text{MEMOE}}$

(Memory Output Enable) is asserted low; for a write cycle, $\overline{\text{MEMWR}}$ (Memory Write) is asserted low. For a multiword transfer cycle during a Start-of-Message (SOM), End-of-Message (EOM), or BC Retry sequences, $\overline{\text{DTACK}}$ and $\overline{\text{MEMENA-OUT}}$ will remain asserted for an additional [4•(number of words)] clock cycles; either $\overline{\text{MEMOE}}$ or $\overline{\text{MEMWR}}$ will be asserted for each word cycle.

In the DMA configuration, the host has two mechanisms for accessing external RAM. As shown in FIGURE 26, the host can access the RAM by means of the ACE/Mini-ACE's control signals $\overline{\text{SELECT}}$, $\overline{\text{STRBD}}$, MEM/$\overline{\text{REG}}$. RD/$\overline{\text{WR}}$, $\overline{\text{READYD}}$, $\overline{\text{MEMENA-OUT}}$, $\overline{\text{MEMWR}}$ and $\overline{\text{MEMOE}}$. While this requires no external control logic, it does entail about 250 ns of processor bandwidth to complete an access. This time allows the ACE/Mini-ACE to arbitrate between 1553 and CPU accesses, and between internal and external RAM access and to enable internal tri-state buffers. Alternatively, in the configuration of FIGURE 27, the host processor's access time to read or write the external RAM is reduced by means of the extra logic gates shown. The only limitations are the CPU's strobe width, the access time of the RAM, and the gate delays. Note that in this configuration, the host must still activate the signals $\overline{\text{SELECT}}$, $\overline{\text{STRBD}}$, etc. in order to access the ACE/Mini-ACE's internal registers.

8.11.1 Handshake Timeout

In the DMA or transparent modes, the host processor must allow the ACE/Mini-ACE's 1553 logic to gain access to the system address and data buses to read and write memory. In order to ensure that words are transferred to/from RAM when required during the processing of 1553 messages, the CPU must provide the ACE/Mini-ACE access to the system buses within the allotted time. The allotted time is 4.4 µs when using a 20 MHz clock input, 4 µs when using a 16 MHz clock input, 3.5 µs when using a 12 MHz clock, and 3.2 µs when using a 10 MHz clock input. If the CPU fails to provide access within the allotted time, the ACE/Mini-ACE will be unable to transfer a word or burst of words.

A Handshake Timeout can occur on Data Word Transfers in all modes, and during Start-of-Message (SOM) sequences in RT or Message Monitor modes.

Note that a Handshake Timeout condition **will not occur** during the following transfer sequences: BC Start-of-Message (SOM), End-of-Message (EOM), and Retry sequences; Word Monitor start sequence; RT End-of-Message (EOM) sequence; and Message Monitor End-of-Message (EOM) sequence.

The handshake timer will expire in either of two circumstances. For both conditions, the allotted time is 4.4 µs using a 20 MHz clock, 4.0 µs using

a 16 MHz clock, 3.5 µs using a 12 MHz clock, 3.2 µs using a 10 MHz clock.

1) In the DMA configuration, if the host processor did not assert $\overline{\text{DTGRT}}$ (low) within the allotted time after the ACE/Mini-ACE asserted its $\overline{\text{DTREG}}$ output (low); or

2) In transparent mode (includes the DMA configuration), if the processor kept $\overline{\text{STRBD}}$ asserted (low) for longer than the allotted time after the ACE/Mini-ACE asserted its $\overline{\text{READYD}}$ acknowledge output low.

The effects of a handshake timeout are as follows:

1) In BC, RT, or Selective Monitor modes, the processing of the current message is immediately terminated. In BC or RT modes, if the ACE/Mini-ACE is transmitting on the 1553 bus in BC or RT modes, the transmission is terminated. The current received Data Word and any subsequent Data Words **will not** be stored to the ACE/Mini-ACE shared RAM.

2) In RT mode, the ACE/Mini-ACE **will continue** to monitor received Data Words for error conditions (encoding, parity, etc.) after a Handshake Timeout condition has occurred. Any detected errors will be flagged in the Block Status Word, Interrupt Status Register, and RT BIT Word Register.

3) In BC mode, the processing of a frame of messages is terminated and not re-started.

4) In Word Monitor mode, the ACE/Mini-ACE will not store the current "Word/ID Word" pair, but will continue to store subsequent word pairs.

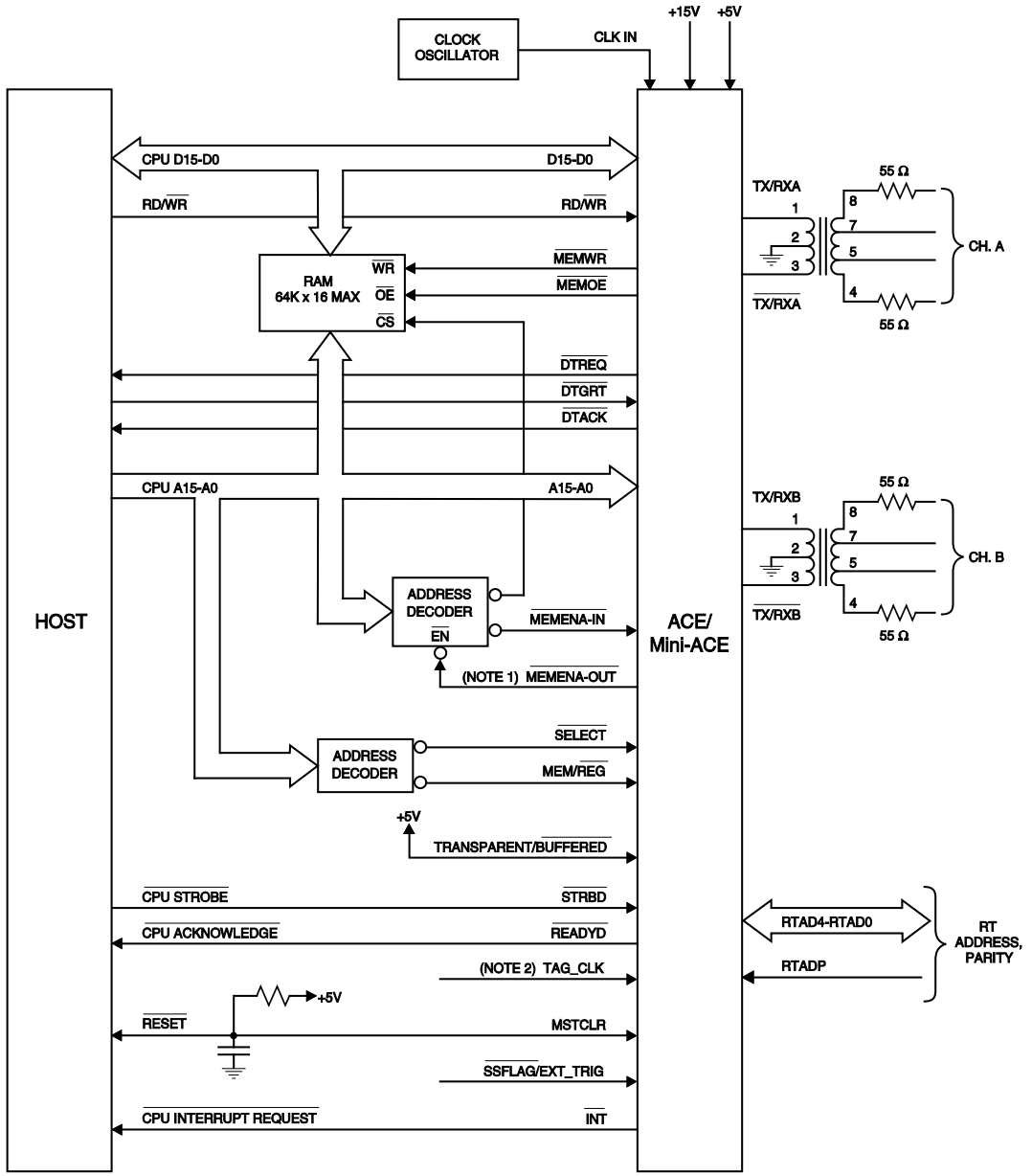
5) In BC, RT, or Selective Monitor modes, the EOM and ERROR FLAG bits will be set in the Block Status Word for the current message.

6) If enabled, a HANDSHAKE FAILURE interrupt request will be issued, and the HANDSHAKE FAILURE bit will be set to logic "1" in the Interrupt Status register.

7) In RT mode, the HANDSHAKE FAILURE bit will be set in the RT Built-In-Test (BIT) Word.

8) If a Handshake Failure occurs during an RT Start-of-Message (SOM) transfer sequence, **the entire message will be ignored.**

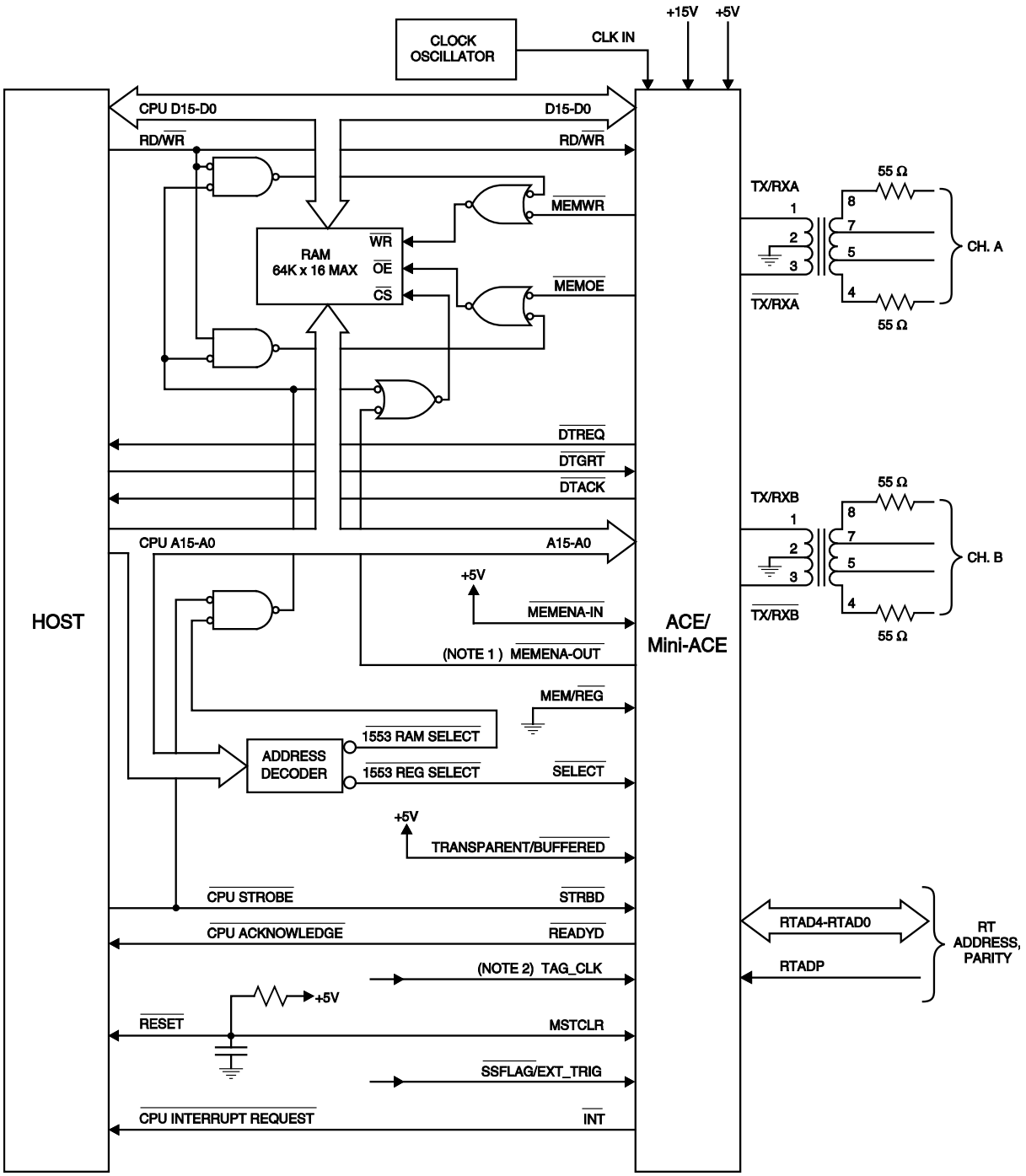
It should be noted that a handshake timeout **cannot** occur in the buffered mode configuration.



NOTES:

1. MEMENA-OUT IS NOT AVAILABLE ON THE MINI-ACE SERIES TERMINALS BUT MAY BE REPLACED BY LOGICALLY OR'ING DTACK WITH IOEN.
2. TAG_CLK NOT AVAILABLE ON MINI-ACE SERIES TERMINALS.

FIGURE 26. INTERCONNECTION DIAGRAM FOR 16-BIT DMA MODE



NOTES:

1. MEMENA-OUT IS NOT AVAILABLE ON THE MINI-ACE SERIES TERMINALS BUT MAY BE REPLACED BY LOGICALLY OR'ING DTACK WITH IOEN.
2. TAG_CLK NOT AVAILABLE ON MINI-ACE SERIES TERMINALS.

FIGURE 27. 16-BIT DMA WITH EXTERNAL LOGIC TO REDUCE CPU ACCESS TIME

8.12 8-BIT BUFFERED MODE

(Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)

FIGURE 28 illustrates the 8-bit buffered mode. This interface allows a direct connection to 8-bit microprocessors and 8-bit microcontrollers **(Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)**. As in the 16-bit buffered configuration, the buffered RAM is limited to the ACE/Mini-ACE's internal RAM (4K words on BU-65170/61580's, BU-65178/79, BU-61588 series terminals, 12K words on BU-61585/86, and 64K words on BU-61688/89 Mini-ACE Plus series terminals). In the 8-bit mode, the host CPU accesses the ACE/Mini-ACE's internal registers and RAM by means of a pair of 8-bit registers embedded in the ACE/Mini-ACE interface. The 8-bit interface may be further configured by means of three strappable inputs: $\overline{\text{ZERO_WAIT}}$, POLARITY_SEL, and TRIGGER_SEL.

In the 8-bit buffered mode, the input 16/$\overline{8}$-BIT must be strapped to logic "0" and the CPU's data bus must be connected to **both D15-D8 and D7-D0.** The LSB of the processor address bus (processor A0) must be connected to the input MSB/LSB for upper/lower byte selection. The processor's A1 output connects to the ACE/Mini-ACE's A0 input, processor A2 to ACE/Mini-ACE A1, etc.

The programmable inputs POLARITY_SEL and TRIGGER_SEL allow the ACE/Mini-ACE terminals to accommodate the different byte ordering conventions (Big/Little Endian) and "A0" logic sense implemented by different 8-bit processor families. For example, a Motorola 6809 writes upper data first to the lower (usually even) address location, followed by lower data to the next highest (usually odd numbered) location. By contrast, an Intel 8088 will first write lower data to the lower (usually even numbered) address location and then write the upper byte to the next highest (usually odd numbered) address.

If the POLARITY_SEL input signal is connected to logic "1" in the 8-bit non-zero wait mode **(Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)**, then the MSB/LSB input signal will select the most significant byte when low and the least significant byte when high. When the POLARITY_SEL input signal is connected to logic "0," the MSB/LSB input signal will select the least significant byte when low and the most significant byte when high. Therefore, a Motorola 6809 would require that the POLARITY_SEL input be connected to logic "1," while an Intel 8088 would require a logic "0" on POLARITY_SEL.

The TRIGGER_SEL input will control the order in which bytes are transferred to or from the ACE/Mini-ACE. This is important because the ACE/Mini-ACE performs 16-bit internal transfers. For the case of a write operation, the host processor will write 8 bits of a 16-bit word to the ACE/Mini-ACE. The ACE/Mini-ACE will store this byte in an internal data latch. The host processor will then present the other 8 bits of the word. At this point in time, the ACE/Mini-ACE will "trigger" an internal 16-bit transfer, with half of the data being presented from the CPU data bus, while the other half (written during the previous CPU cycle) is presented to the ACE/Mini-ACE's RAM or register from the internal latch.

When operating in the non-zero wait mode **(Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)**, a logic "0" on the TRIGGER_SEL input will configure the ACE/Mini-ACE to trigger an internal 16-bit transfer on the least significant byte transfer for a read access, and by the most significant byte transfer for a write access. A logic "1" on the TRIGGER_SEL input will configure the ACE/Mini-ACE to trigger an internal 16-bit transfer on the most significant byte transfer for a read access, and by the least significant byte transfer for a write access. Therefore, a 6809 interface would require that the TRIGGER_SEL input be connected to logic "1," while an 8088 interface requires a logic "0."

The following considerations are necessary when reading the Interrupt Status Register in 8-bit non-zero wait mode. This is to ensure that subsequent interrupt events after a triggering read of an ISR result in bit(s) being set in the respective ISR (i.e. to avoid interrupting events becoming "lost").

- For 8-bit non-zero wait mode, for reading an ISR, that ISR address must be presented on the triggering (first) transfer. The address presented on the subsequent non-triggering read is a "don't care". The only exception is for the case of SP'ACE II, where the address for the non-triggering read must be a *register* read, rather than a memory read, with a suggested register address of 0x0000.

The operation of the ACE's 8-bit non-zero wait buffered mode (**Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)** is essentially the same as the 16-bit mode, with the following exceptions:

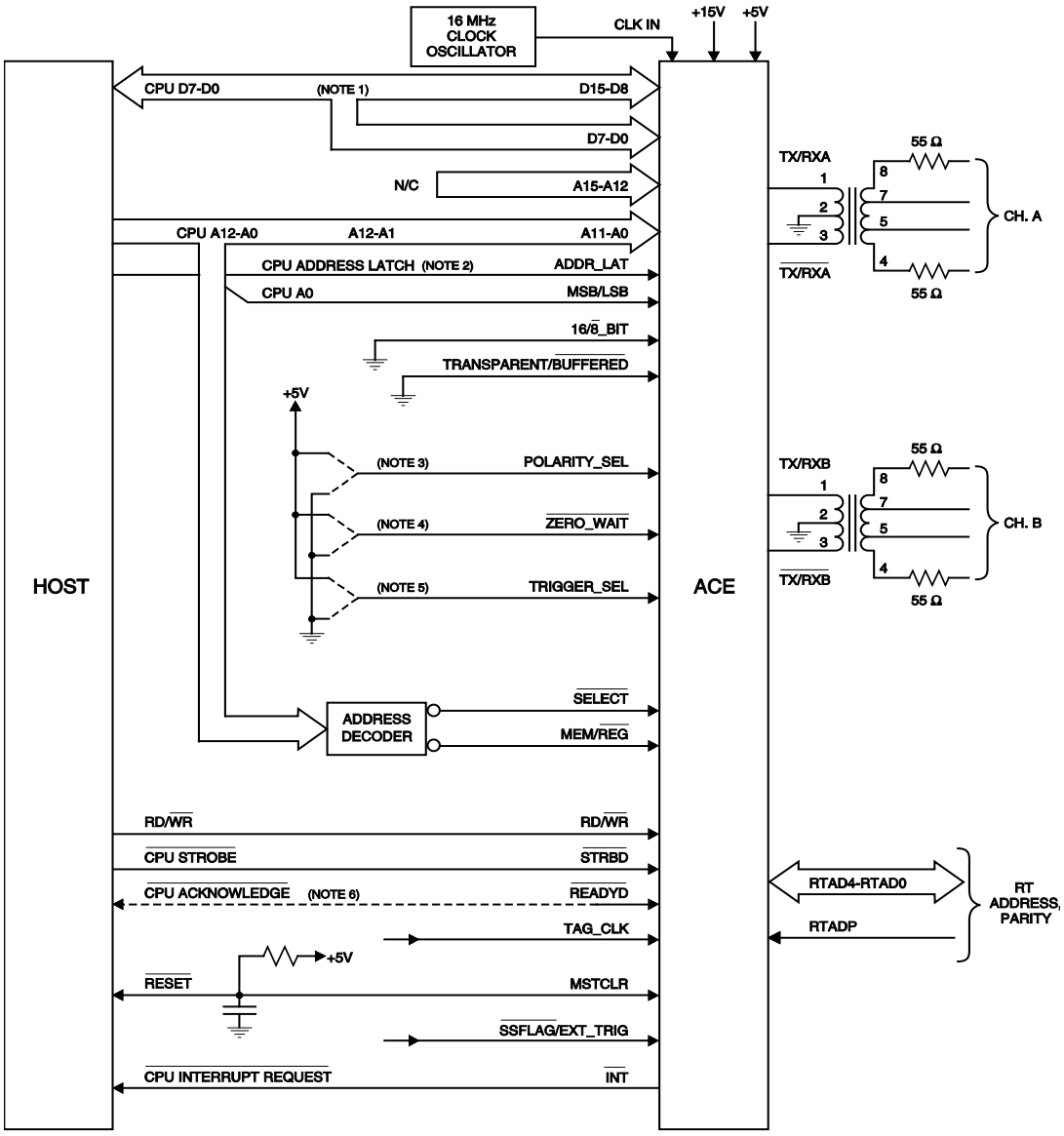
1) For SP'ACE (BU-61582, BU-61583), memory and registers must **not** be accessed when the SP'ACE is processing a 1553 message.

2) For SP'ACE II (BU-63825, BU-63925), during non-triggering register or memory transfers. MEM/REG* must be asserted to '0', and a register address of 0x0000, rather than the actual

memory or register address, must be used.

3) For a write cycle, the first byte is written to an internal latch; the second byte is written directly to a register or RAM location. When the second byte is written to register or RAM, the first byte is simultaneously transferred from the buffer register to register or RAM. The address (A15-A0 and MEM/$\overline{\text{REG}}$) is "don't care" during the first byte transfer, but must be valid during the second byte transfer. The handshake output $\overline{\text{READYD}}$ is asserted low after **both** byte transfers.

4) For a read cycle in the "non-zero wait" mode, the first byte is read directly from register or RAM. While the first byte is read by the CPU, the second byte is being stored in an internal latch. The processor may then read the second byte from the buffer. The address (A15-A0 and MEM/$\overline{\text{REG}}$) must be valid during the first byte read, but is "don't care" during the second byte read. The handshake output $\overline{\text{READYD}}$ is asserted low after **both** byte transfers.



NOTES:

1. CPU D7-D0 CONNECTS TO BOTH D15-D8 AND D7-D0.
2. CPU ADDRESS LATCH SIGNAL PROVIDED BY PROCESSORS WITH MULTIPLEXED ADDRESS/DATA BUFFERS.
3. IF POLARITY_SEL = "1", THEN MSB/LSB SELECTS THE MOST SIGNIFICANT BYTE WHEN LOW, AND THE LEAST SIGNIFICANT BYTE WHEN HIGH.
   IF POLARITY_SEL = "0", THEN MSB/LSB SELECTS THE LEAST SIGNIFICANT BYTE WHEN LOW, AND THE MOST SIGNIFICANT BYTE WHEN HIGH.
4. ZERO WAIT SHOULD BE STRAPPED TO LOGIC "1" FOR NON-ZERO WAIT INTERFACE AND TO LOGIC "0" FOR ZERO WAIT INTERFACE.
5. OPERATION OF TRIGGER_SELECT INPUT IS AS FOLLOWS:
   FOR NON-ZERO WAIT INTERFACE (ZERO WAIT = "1"):
   IF TRIGGER_SEL = "1", THEN INTERNAL 16-BIT TRANSFERS ARE TRIGGERED BY THE MOST SIGNIFICANT BYTE TRANSFER READ ACCESSES AND BY THE LEAST SIGNIFICANT BYTE TRANSFER FOR WRITE ACCESSES.
   IF TRIGGER_SEL = "0", THEN INTERNAL 16-BIT TRANSFERS ARE TRIGGERED BY THE LEAST SIGNIFICANT BYTE TRANSFER FOR READ ACESSES AND BY THE MOST SIGNIFICANT BYT TRANSFER FOR WRITE ACCESSES.
   FOR ZERO WAIT INTERFACE (ZERO WAIT = "0"):
   IF TRIGGER_SEL = "1", THEN INTERNAL 16-BIT TRANSFERS ARE TRIGGERED BY THE LEAST SIGNIFICANT BYTE TRANSFER, FOR BOTH READ AND WRITE ACCESSES.
   IF TRIGGER_SEL = "0", THEN INTERNAL 16-BIT TRANSFERS ARE TRIGGERED BY THE MOST SIGNIFICANT BYTE TRANSFER, FOR BOTH READ AND WRITE ACCESES.
6. CPU ACKNOWLEDGE PROCESSOR INPUT ONLY FOR NON-ZERO WAIT TYPE OF INTERFACE.

(Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)

FIGURE 28. INTERCONNECTION DIAGRAM FOR 8-BIT BUFFERED MODE

TABLE 105 provides a summary of the possible transfer sequences in the 8-bit non-zero wait mode. **(Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)**.

TABLE 105. SUMMARY OF 8-BIT OPERATION (NON-ZERO WAIT MODE)

$\overline{\text{ZERO_WAIT}}$	TRIGGER SELECT	POLARITY SELECT	RD/$\overline{\text{WR}}$	FIRST BYTE TRANSFER	SECOND BYTE TRANSFER
1	1	1	1	MSB/LSB = 0; Valid A15-A0, MEM/$\overline{\text{REG}}$; CPU ⟵ RAM 15-8; Buffer 7-0 ⟵ RAM 7-0	MSB/LSB = 1; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟵ Buffer 7-0
1	1	1	0	MSB/LSB = 0; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟶ Buffer 15-8	MSB/LSB = 1; Valid A15-A0, MEM/$\overline{\text{REG}}$; Buffer 15-8 ⟶ RAM 15-8; CPU ⟶ RAM 7-0
1	1	0	1	MSB/LSB = 1; Valid A15-A0, MEM/$\overline{\text{REG}}$; CPU ⟵ RAM 15-8; Buffer 7-0 ⟵ RAM 7-0	MSB/LSB = 0; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟵ Buffer 7-0
1	1	0	0	MSB/LSB = 1; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟶ Buffer 15-8	MSB/LSB = 0; Valid A15-A0, MEM/$\overline{\text{REG}}$; Buffer 15-8 ⟶ RAM 15-8; CPU ⟶ RAM 7-0
1	0	1	1	MSB/LSB = 1; Valid A15-A0, MEM/$\overline{\text{REG}}$; CPU ⟵ RAM 7-0; Buffer 15-8 ⟵ RAM 15-8	MSB/LSB = 0; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟵ Buffer 15-8
1	0	1	0	MSB/LSB = 1; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟶ Buffer 7-0	MSB/LSB = 0; Valid A15-A0, MEM/$\overline{\text{REG}}$; Buffer 7-0 ⟶ RAM 7-0; CPU ⟶ RAM 15-8
1	0	0	1	MSB/LSB = 0; Valid A15-A0, MEM/$\overline{\text{REG}}$; CPU ⟵ RAM 7-0; Buffer 15-8 ⟵ RAM 15-8	MSB/LSB = 1; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟵ Buffer 15-8
1	0	0	0	MSB/LSB = 0; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟶ Buffer 7-0	MSB/LSB = 1; Valid A15-A0, MEM/$\overline{\text{REG}}$; Buffer 7-0 ⟶ RAM 7-0; CPU ⟶ RAM 15-8

8.13 8-BIT ZERO WAIT MODE

By connecting $\overline{\text{ZERO_WAIT}}$ to logic "0" in the 8-bit buffered mode **(Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)**, the ACE/Mini-ACE may be interfaced with minimal "glue" logic to microcontrollers, such as the Intel 8051 series, that do not have an "acknowledge" type of handshake input. When performing a write transfer in the zero wait mode, the ACE/Mini-ACE will begin the cycle in the same manner as the non-zero wait mode. The difference is that the ACE/Mini-ACE will latch the data, address and control lines internally if the host processor terminates the transfer cycle (brings $\overline{\text{STRBD}}$ high)

before the ACE/Mini-ACE has responded with the handshake acknowledge output (high-to-low transition of $\overline{\text{READYD}}$). The only constraint is that the host processor must not begin a new transfer to the ACE/Mini-ACE until the ACE/Mini-ACE has completed the previous internal transfer.

The following considerations are necessary when reading the Interrupt Status Register in 8-bit zero wait mode. This is to ensure that subsequent interrupt events after a triggering read of an ISR result in bit(s) being set in the respective ISR (i.e. to avoid interrupting events becoming "lost").

- For 8-bit zero wait mode, the address of the Interrupt Status Register *must* be used for the triggering read transfer prior to the actual read of the data.
- For the first read, data is either "thrown away", or possibly used, (if data is used, then it is for a memory or register address presented on an *earlier* triggering transfer).
- For the second read (non-triggering), the register address presented does not matter (for the case of SP'ACE II, must be a *register*, rather than memory address).
- For the third read (triggering), the register address presented on *this* transfer must *not* be that of the ISR. This is to avoid an inadvertent clearing of the indication of a new interrupt, which would be "missed" by a subsequent read of the Interrupt Status Register.

Alternatively, this address can either be register address 0x0000 or that of some other register or memory address to be read *next*. Ideally, the host should be reading the values of Interrupt Status Register as an atomic instruction, meaning that interrupts should be disabled during this time, to avoid the possibility of the processor being interrupted in the middle of this read(s).

The operation of the $\overline{\text{READYD}}$ output signal in the non-zero wait mode is to indicate when a transfer is complete. In the zero wait mode, however, $\overline{\text{READYD}}$ indicates that a transfer is active. $\overline{\text{READYD}}$ is normally low and will go high upon the start of the internal transfer, and will remain high until the internal transfer is complete.

The operation of the TRIGGER_SEL input in the 8-bit zero wait mode is similar to its operation in the 8-bit non-zero wait mode **(Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)**. The ACE/Mini-ACE must be configured to trigger the internal transfer off of the proper byte transfer. A write operation is the same for both zero wait and non-zero wait, in that the ACE/Mini-ACE will trigger the internal write when the

second of two byte transfers is performed. An internal read transfer will be triggered after the host processor reads the second byte of a 2-byte read. This is in contrast to a non-zero wait read, in which the internal read is triggered on the first of a two byte access.

The write cycle for the 8-bit "zero wait" mode ($\overline{\text{ZERO_WAIT}}$ = logic "0") is identical to that for the 8-bit "non-zero wait" mode, except for the operation of the $\overline{\text{READYD}}$ output. In the "zero wait" mode, $\overline{\text{READYD}}$ stays low during the entire first byte (nontriggering) transfer cycle. During the second byte transfer time (triggering transfer), $\overline{\text{READYD}}$ stays low until $\overline{\text{STRBD}}$ is either cleared high (after a minimum pulse width of 20 ns), or has been sampled low for two rising edges of the CLK_IN input. $\overline{\text{READYD}}$ then goes high (indicating "not ready") and remains high until the internal 16-bit transfer of data between the ACE's internal latches and internal RAM or register has been completed.

When using the 8-bit (or 16-bit) "zero wait" mode, it is assumed there is no "acknowledge" input on the processor to connect the ACE/Mini-ACE's $\overline{\text{READYD}}$ output to. However, the CPU may still poll the $\overline{\text{READYD}}$ output. **It should not initiate another transfer cycle to the ACE while** $\overline{\text{READYD}}$ **is logic "1."** Alternatively, the CPU may insert software wait states between successive accesses to the ACE/Mini-ACE. The required wait time varies with the mode of operation and frequency of the clock input. Refer to TABLE 106 to determine the required minimum wait time.

TABLE 106. MINIMUM REQUIRED DELAY TIMES

MODE	@ 20 MHZ	@ 16 MHZ	@ 12 MHZ	@ 10 MHZ
Bus Controller (BC)	1.45 µs	1.81 µs	2.41 µs	2.90 µs
Remote Terminal (RT)	2.05 µs	2.56 µs	3.41 µs	4.10 µs
Word Monitor	450 ns	562 ns	750 ns	900 ns
Selective Message Monitor	1.85 µs	2.31 µs	3.08 µs	3.70 µs

For the read cycle for the 8-bit "zero wait" mode: It is important to realize that for a given read cycle, the internal RAM address (including the value of MEM/$\overline{\text{REG}}$) is the address that was presented on the ACE/Mini-ACE's address inputs (A15-A0) during the **SECOND byte read of the PREVIOUS (word) READ cycle.** Therefore, in order to read a word (two bytes) in this mode, the first byte read access is a "dummy cycle" as far as the data bus (D15-8, D7-D0) is concerned; however, the **address** (A15-A0 and MEM/$\overline{\text{REG}}$) for the first word to be read must be presented at this time.

That is, in order to initiate a series of word accesses, the CPU must **FIRST perform a "second byte transfer" read access (illustrated in** TABLE 107**)** with the valid address and value of MEM/$\overline{\text{REG}}$ for the first

word presented. The data read during this transfer should be ignored ("thrown away"). The CPU should then perform the "first byte" and "second byte" read cycles to acquire the data from the address (including MEM/$\overline{\text{REG}}$) that was previously presented. As far as the ACE/Mini-ACE is concerned, the address presented on A15-A0 and MEM/$\overline{\text{REG}}$ is "Don't Care" during the "first byte" transfer. On the second byte transfer, the valid address for the **next** word to be read may be presented on A15-A0 and MEM/$\overline{\text{REG}}$. The CPU may then read the subsequent word by performing a first byte read, followed by a second byte read, etc.

Note that the $\overline{\text{READYD}}$ output will remain low through the end of the first "zero wait" read cycle, but will transition to logic "1" during (or possibly after) the $\overline{\text{STRBD}}$ pulse for the second byte read cycle. During the time that $\overline{\text{READYD}}$ is logic "1," the RAM data for the address presented is transferred from the ACE/Mini-ACE's internal RAM or register to the two internal 8-bit latches. When $\overline{\text{READYD}}$ is re-asserted to logic "0" (2.6 µs max later with a 16 MHz clock), the CPU may then proceed to read the first byte, then the second byte.

TABLE 107 summarizes the possible transfer sequences for the 8-bit zero wait mode.

TABLE 107. SUMMARY OF 8-BIT OPERATION (ZERO WAIT MODE)					
$\overline{\text{ZERO_WAIT}}$	TRIGGER SELECT	POLARITY SELECT	RD/$\overline{\text{WR}}$	FIRST BYTE TRANSFER	SECOND BYTE TRANSFER
0	1	1	1	MSB/LSB = 0; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟵ Buffer 15-8 (**Last** A15-A0, MEM/$\overline{\text{REG}}$)	MSB/LSB = 1; A15-A0 and MEM/$\overline{\text{REG}}$ Valid for **Next Word**; CPU ⟵ Buffer 7-0 (**Last** A15-A0, MEM/$\overline{\text{REG}}$); then, Buffer 15-0 ⟵ RAM 15-0
0	1	1	0	MSB/LSB = 0; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟶ Buffer 15-8	MSB/LSB = 1; Valid A15-A0, MEM/$\overline{\text{REG}}$; CPU ⟶ Buffer 7-0; then, Buffer ⟶ RAM 15-0
0	1	0	1	MSB/LSB = 1; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟵ Buffer 15-8 (**Last** A15-A0, MEM/$\overline{\text{REG}}$)	MSB/LSB = 0; A15-A0 and MEM/$\overline{\text{REG}}$ Valid for **Next Word**; CPU ⟵ Buffer 7-0 (**Last** A15-A0, MEM/$\overline{\text{REG}}$); then, Buffer 15-0 ⟵ RAM 15-0
0	1	0	0	MSB/LSB = 1; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟶ Buffer 15-8	MSB/LSB = 0; Valid A15-A0, MEM/$\overline{\text{REG}}$; CPU ⟶ Buffer 7-0; then, Buffer ⟶ RAM 15-0
0	0	1	1	MSB/LSB = 1; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟵ Buffer 7-0 (**Last** A15-A0, MEM/$\overline{\text{REG}}$)	MSB/LSB = 0; A15-A0 and MEM/$\overline{\text{REG}}$ Valid for **Next Word**; CPU ⟵ Buffer 15-8 (**Last** A15-A0, MEM/$\overline{\text{REG}}$); then, Buffer 15-0 ⟵ RAM 15-0
0	0	1	0	MSB/LSB = 1; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟶ Buffer 7-0	MSB/LSB = 0; Valid A15-A0, MEM/$\overline{\text{REG}}$; CPU ⟶ Buffer 15-8; then, Buffer ⟶ RAM 15-0
0	0	0	1	MSB/LSB = 0; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟵ Buffer 7-0 (**Last** A15-A0, MEM/$\overline{\text{REG}}$)	MSB/LSB = 1; A15-A0 and MEM/$\overline{\text{REG}}$ Valid for **Next Word**; CPU ⟵ Buffer 15-8 (**Last** A15-A0, MEM/$\overline{\text{REG}}$); then, Buffer 15-0 ⟵ RAM 15-0
0	0	0	0	MSB/LSB = 0; A15-A0, MEM/$\overline{\text{REG}}$ = "Don't Care;" CPU ⟶ Buffer 7-0	MSB/LSB = 1; Valid A15-A0, MEM/$\overline{\text{REG}}$; CPU ⟶ Buffer 15-8; then, Buffer ⟶ RAM 15-0

8.14 CONTROL LOGIC

"Glue" control logic is generally required to provide conditioning between the processor's control signals and the ACE/Mini-ACE's control signals. In many systems, this circuitry may be implemented into a programmable logic device (PLD/PAL). It is often possible to combine the address decoding and control logic glue functions in the same PLD/PAL device. One typical function of the glue logic is to formulate the ACE/Mini-ACE's $\overline{\text{STRBD}}$ input. This is a simple OR'ing function for many processors that provides separate $\overline{\text{WRITE}}$ and $\overline{\text{READ}}$ strobe outputs. In addition, gating, inverting, and/or tri-state control logic is often needed between the ACE/Mini-ACE's $\overline{\text{READYD}}$ output and the processor's acknowledge input.

8.15 INTERRUPT LOGIC

In many cases, the interrupt request logic may be implemented in the same PLD/PAL with the address decoding and glue logic. The most common functions of this logic include providing tri-state or open collector INTERRUPT REQUEST outputs, clearing the request flip-flop, and providing interrupt vector responses.

8.16 RESET (MSTCLR*) INPUT

The ACE/Mini-ACE may be placed in its power turn-on, or initialization state, following either a hardware or software reset. A hardware reset, which generally occurs following power turn-on, is caused by asserting the MSTCLR* input to logic "0" for at least 100 ns.

The state of the ACE/Mini-ACE's internal logic following a hardware, software, or "Reset RT" reset is summarized in TABLE 2, in the "SOFTWARE INTERFACE" section of the User's Guide.

8.17 CHIP SELECT (SELECT*) INPUT

In all modes, a CPU transfer is initiated through the use of the input signals $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$. The ACE/Mini-ACE will begin a CPU transfer upon sampling both $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low on a rising clock edge. A CPU transfer, once started (as indicated by a logic 0 output on the $\overline{\text{IOEN}}$ output signal), will remain active until the $\overline{\text{STRBD}}$ input returns to a logic 1 state.

For the ACE/Mini-ACE series terminals, the order in which $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ are asserted low does not matter. The SP'ACE and SP'ACE II (BU-61582 (BU-63825)) series terminals, on the other hand, will latch the state of $\overline{\text{SELECT}}$ on the second rising clock edge in which $\overline{\text{STRBD}}$ is sampled low. This latching mechanism allows for address pipelining, which is becoming more popular in modern processors. Address pipelining allows the address for the next cycle to be asserted at the end of the current cycle. If the current transfer is not to the ACE/Mini-ACE

(i.e., $\overline{\text{SELECT}}$ is high and $\overline{\text{STRBD}}$ is low), but the next transfer is the ACE/Mini-ACE, there is a possibility that at the end of the current transfer (while $\overline{\text{STRBD}}$ is still low) $\overline{\text{SELECT}}$ may be asserted low for the next transfer. Under these conditions the ACE/Mini-ACE will begin an erroneous transfer at the end of the current. The SP'ACE and SP'ACE II, on the other hand will latch $\overline{\text{SELECT}}$ and maintain the value during the current transfer and will not release that value until $\overline{\text{STRBD}}$ returns to logic 1.

8.18 16-BIT BUFFERED, NON-ZERO WAIT MODE INTERFACE TIMING

FIGURE 29 and FIGURE 31 illustrate the timing for the host processor to access the ACE/Mini-ACE's internal RAM or registers in the 16-bit, non-zero wait buffered mode. FIGURE 29 illustrates the 16-bit buffered, non-zero wait state mode read cycle timing, while FIGURE 31 shows the 16-bit, buffered, non-zero wait state mode write cycle timing.

During a CPU transfer cycle, the signals $\overline{\text{STRBD}}$ and $\overline{\text{SELECT}}$ must be sampled low on the rising edge of the system clock to request access to the ACE/Mini-ACE internal shared RAM. The transfer will begin on the first rising system clock edge when ($\overline{\text{SELECT}}$ **and** $\overline{\text{STRBD}}$) is low **and** the 1553 protocol/memory management unit is not accessing the internal RAM. The start of the transfer is indicated by the falling edge of the output signal IOEN*. The signals MEM/REG* and RD/WR* are latched internally on the first falling clock edge after the start of the transfer cycle. The address inputs are latched internally on the first rising clock edge after the signal $\overline{\text{IOEN}}$ goes low. Note that the address lines may be latched at any time using the ADDR_LAT input signal.

The output signal READYD* will be asserted low on the third rising system clock edge after $\overline{\text{IOEN}}$ goes low for both read and write transfers when using the ACE/Mini-ACE or for write transfers when using the SP'ACE and SP'ACE II (61582 (63825)). $\overline{\text{READYD}}$ signal will be asserted low on the seventh rising system clock edge after $\overline{\text{IOEN}}$ goes low when reading from the SP'ACE and SP'ACE II (61582 (63825)). The assertion of $\overline{\text{READYD}}$ low indicates to the host processor that read data is available on the parallel data bus (D15-D0), or that write data has been stored. At this time, the CPU should bring the signal $\overline{\text{STRBD}}$ high, completing the transfer cycle.

TABLE 108. CPU READING RAM/REGISTERS (16-BIT, BUFFERED, NON-ZERO WAIT)

CPU READING RAM OR REGISTERS (SHOWN FOR 16-BIT, BUFFERED, NON-ZERO WAIT MODE)

REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	SELECT* and STRBD* low setup time prior to clock rising edge (Note 2,10)	10			15			ns
t2	SELECT* and STRBD* low to IOEN* low (uncontended access @20 MHz) (Notes 2,6)			95.0				ns
	SELECT* and STRBD* low to IOEN* low (contended access @20 MHz) (Notes 2,6)			2.2				µs
	SELECT* and STRBD* low to IOEN* low (uncontended access @16 MHz) (Notes 2,6)			107.5			107.5	ns
	SELECT* and STRBD* low to IOEN* low (contended access @16 MHz) (Notes 2,6)			2.8			5.5	µs
	SELECT* and STRBD* low to IOEN* low (uncontended access @12 MHz) (Notes 2,6)			128.3			128.3	ns
	SELECT* and STRBD* low to IOEN* low (contended access @12 MHz) (Notes 2,6)			3.7			7.4	µs
	SELECT* and STRBD* low to IOEN* low (uncontended access @10 MHz) (Notes 2,6)			145.0				ns
	SELECT* and STRBD* low to IOEN* low (contended access @10 MHz) (Notes 2,6)			4.4				µs
t3	MEM/REG* and RD/WR* setup time following SELECT* and STRBD* low (@20 MHz) (Notes 3,4,5,7)			10				ns
	MEM/REG* and RD/WR* setup time following SELECT* and STRBD* low (@16 MHz) (Notes 3,4,5,7)			10			10	ns
	MEM/REG* and RD/WR* setup time following SELECT* and STRBD* low (@12 MHz) (Notes 3,4,5,7)			20			20	ns
	MEM/REG* and RD/WR* setup time following SELECT* and STRBD* low (@10 MHz) (Notes 3,4,5,7)			20				ns
t4	Address valid setup time following SELECT* and STRBD* low (@20 MHz).			17				ns
	Address valid setup time following SELECT* and STRBD* low (@16 MHz).			30			50	ns
	Address valid setup time following SELECT* and STRBD* low (@12 MHz).			50			70	ns
	Address valid setup time following SELECT* and STRBD* low (@10 MHz).			67				ns
t5	CLOCK IN rising edge delay to IOEN* falling edge (Note 6)			35			30	ns
t6	SELECT* hold time following IOEN* falling (Note 2)	0			0			ns
t7	MEM/REG*, RD/WR* setup time prior to CLOCK IN falling edge (Notes 3,4,5,7)	10			10			ns
t8	MEM/REG*, RD/WR* hold time following CLOCK IN falling edge (Notes 3,4,5,7)	30			25			ns
t9	Address valid setup time prior to CLOCK IN rising edge (Notes 7,8,9)	30			10			ns
t10	Address hold time following CLOCK IN rising edge (Notes 7,8,9,10)	30			25			ns
t11	IOEN* falling delay to READYD* falling (reading RAM @20 MHz) (Notes 6,10)	135	150	165				ns
	IOEN* falling delay to READYD* falling (reading registers @20 MHz) (Notes 6,10)	135	150	165				ns
	IOEN* falling delay to READYD* falling (reading RAM @16 MHz) (Notes 6,10)	170	187.5	205	420	437.5	455	ns
	IOEN* falling delay to READYD* falling (reading registers @16 MHz) (Notes 6,10)	170	187.5	205	170	187.5	205	ns
	IOEN* falling delay to READYD* falling (reading RAM @12 MHz) (Notes 6,10)	235	250	265	565	583.3	600	ns
	IOEN* falling delay to READYD* falling (reading registers @12 MHz) (Notes 6,10)	235	250	265	235	250	265	ns
	IOEN* falling delay to READYD* falling (reading RAM @10 MHz) (Notes 6,10)	270	300	315				ns
	IOEN* falling delay to READYD* falling (reading registers @10 MHz) (Notes 6,10)	270	300	315				ns
t12	Output Data valid prior to READYD* falling (@20 MHz) (Note 6)	21						ns
	Output Data valid prior to READYD* falling (@16 MHz) (Note 6)	33			33			ns
	Output Data valid prior to READYD* falling (@12 MHz) (Note 6)	54			54			ns
	Output Data valid prior to READYD* falling (@10 MHz) (Note 6)	71						ns
t13	CLOCK IN rising edge delay to READYD* falling (Note 6)			35			30	ns
t14	READYD* falling to STRBD* rising release time.							ns
t15	STRBD* rising edge delay to IOEN* rising edge and READYD* rising edge (Note 6)			30			30	ns
t16	Output Data hold time following STRBD* rising edge.	0			0			ns
t17	STRBD* rising delay to output Data tri-state			40			40	ns
t18	STRBD* high hold time from READYD* rising	0			0			ns
t19	CLOCK IN rising edge delay to Output data valid			60			50	ns

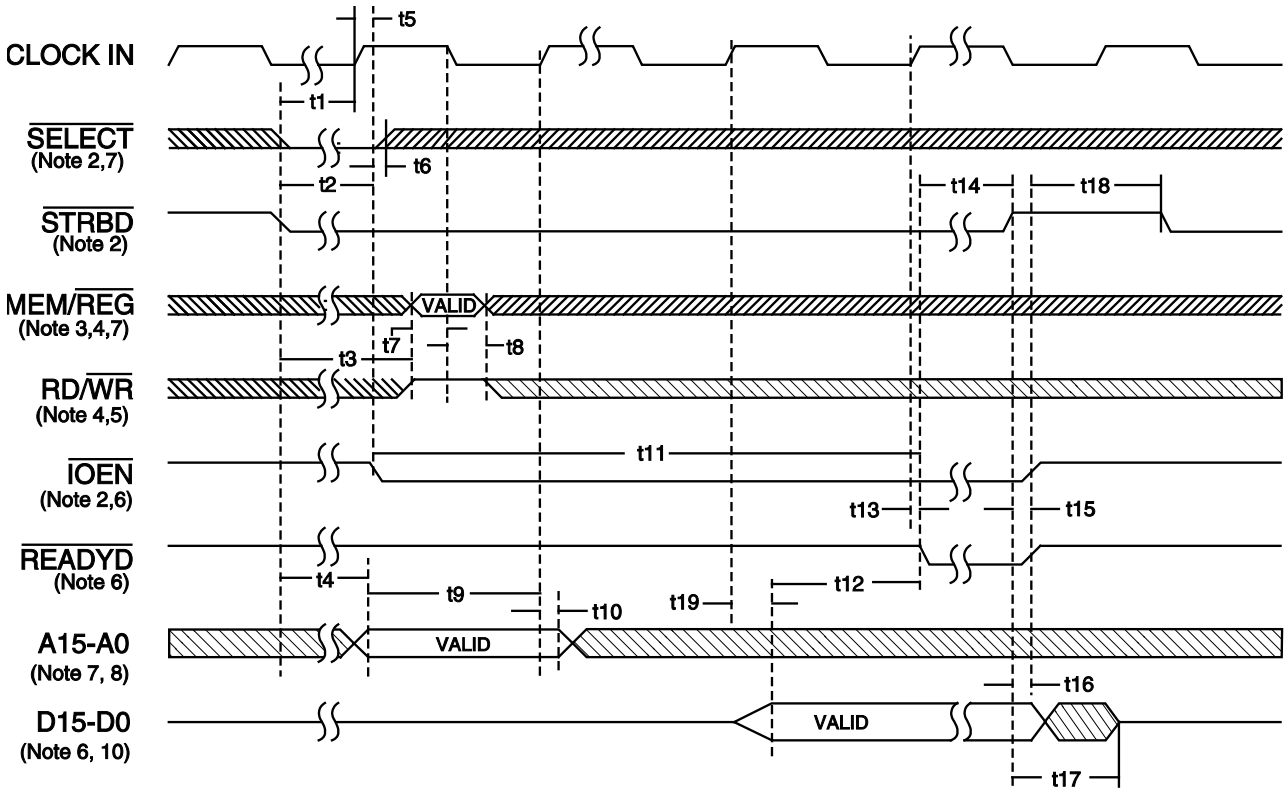


FIGURE 29. CPU READING RAM/REGISTERS (16-BIT, BUFFERED, NON-ZERO WAIT)

Notes for TABLE 108 and FIGURE 29:

1. For the 16-bit buffered non-zero wait configuration, TRANSPARENT/BUFFERED* must be connected to logic "0". ZERO_WAIT* and DTREQ*/16/8* must be connected to logic "1". The inputs TRIGGER_SEL and MSB/LSB may be connected to either +5V or ground.
2. SELECT* and STRBD* may be tied together. IOEN* goes low on the first rising CLK edge when SELECT*•STRBD* is sampled low (satisfying t_1) and the ACE/Mini-ACE's protocol/memory management logic is not accessing the internal RAM. When this occurs, IOEN* goes low, starting the transfer cycle. After IOEN* goes low, SELECT* may be released high. For SP'ACE and SP'ACE II application, SELECT* is latched on the second rising CLOCK edge after STRBD* goes low. Therefore, for a transfer to occur, SELECT* must go low within 1 clock cycle of STRBD* falling.
3. MEM/REG* must be presented high for memory access, low for register access.
4. MEM/REG* and RD/WR* are buffered transparently until the first falling edge of CLK after IOEN* goes low. After this CLK edge, MEM/REG* and RD/WR* become latched internally.
5. The logic sense for RD/WR* in the diagram assumes that POLARITY_SEL is connected to logic "1." If POLARITY_SEL is connected to logic "0," RD/WR* must be asserted low to read.
6. The timing for IOEN*, READYD* and D15-D0 assumes a 50 pf load. For loading above 50 pf, the validity of IOEN*, READYD*, and D15-D0 is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/REG* and SELECT* assumes ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A11 through A0 (A13 through A0 for 61585, 61586, 61582 (63825) and 61583 (63925), A15 through A0 for 61688 and 61689). Registers are accessed by A4 through A0.
9. The address bus A15-A0 is internally buffered transparently until the first rising edge of CLK after IOEN* goes low. After this CLK edge, A15-A0 becomes latched internally.
10. Setup time given for use in worst case timing calculations. None of the ACE/Mini-ACE input signals are required to be synchronized to the system clock. For ACE applications only, where SELECT* and STRBD* do not meet the setup time of t1, but occur during the setup window of an internal flip-flop, an additional clock cycle will be inserted between the falling clock edge that latches MEM/REG* and RD/WR* and the rising clock edge that latches the Address (A15-A0). When this occurs, the pulse width of IOEN* falling to READYD* falling (t11) increases by one clock cycle and the address hold time (t10) must be increased be one clock cycle.
11. For SP'ACE and SP'ACE II application only, the Data Bus (D15-D0) will remain in tri-state during register reads from hex address 18 through 1F.

8.18.1.1 For SP'ACE II (BU-63825/925) only

TABLE 109. CPU READing ram/registers (16-BIT, BUFFERED, NON-ZERO WAIT)						
CPU READING RAM OR REGISTERS (SHOWN FOR 16-BIT, BUFFERED, NON-ZERO WAIT MODE)						
REF	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTE REFERENCE**
t1	SELECT* and STRBD* low setup time prior to clock rising edge	15			ns	Note 2
t2	STRBD* low delay to IOEN* low (uncontended access @16 MHz)			170	ns	Notes 2,6
	STRBD* low delay to IOEN* low (contended access @16 MHz)			5.3	µs	Notes 2, 6
	STRBD* low delay to IOEN* low (uncontended access @12 MHz)			211.6	ns	Notes 2, 6
	STRBD* low delay to IOEN* low (contended access @12 MHz)			7.05	µs	Notes 2, 6
t3	MEM/REG* and RD/WR* setup time following STRBD* low (@16 MHz)			70	ns	
	MEM/REG* and RD/WR* setup time following STRBD* low (@12 MHz)			100	ns	
t4	Address valid setup time following STRBD* low (@16 MHz).			110	ns	
	Address valid setup time following STRBD* low (@12 MHz).			150	ns	
t5	CLOCK IN rising edge delay to IOEN* falling edge			30	ns	
t6	SELECT* hold time following IOEN* falling	0			ns	Note 2
t7	MEM/REG*, RD/WR* setup time prior to CLOCK IN falling edge	10			ns	Notes 3, 4, 5
t8	MEM/REG*, RD/WR* hold time prior to CLOCK IN falling edge	25			ns	Notes 3, 4, 5
t9	Address valid setup time prior to CLOCK IN rising edge	10			ns	
t10	Address hold time following CLOCK IN rising edge	25			ns	Note 9
t11	IOEN* falling delay to READYD* falling (reading RAM @16 MHz)	420	437.5	455	ns	Note 6
	IOEN* falling delay to READYD* falling (reading RAM @ 12 MHz)	565	583.3	600	ns	Note 6
	IOEN* falling delay to READYD* falling (read registers @ 16 MHz)	170	187.5	205	ns	Note 6
	IOEN* falling delay to READYD* falling (reading registers @ 12 MHz)	230	250	265	ns	Note 6
t12	Output Data valid prior to READYD* falling (@ 16 MHz)	33			ns	Note 6
	Output Data valid prior to READYD* falling (@12 MHz)	54			ns	Note 6
t13	CLOCK IN rising edge delay to READYD* falling			30	ns	Note 6
t14	READYD* falling to STRBD* rising release time			∞	ns	
t15	STRBD* rising edge delay to IOEN* rising edge and READYD* rising edge			40	ns	Note 6
t16	Output Data hold time following STRBD* rising edge	0			ns	
t17	STRBD* rising delay to output Data tri-state			40	ns	
t18	STRBD* high hold time from READYD* rising	0			ns	
t19	CLOCK_IN rising edge delay to output data valid			50	ns	

8.18.1.2 For SP'ACE II (BU-63825/925) only

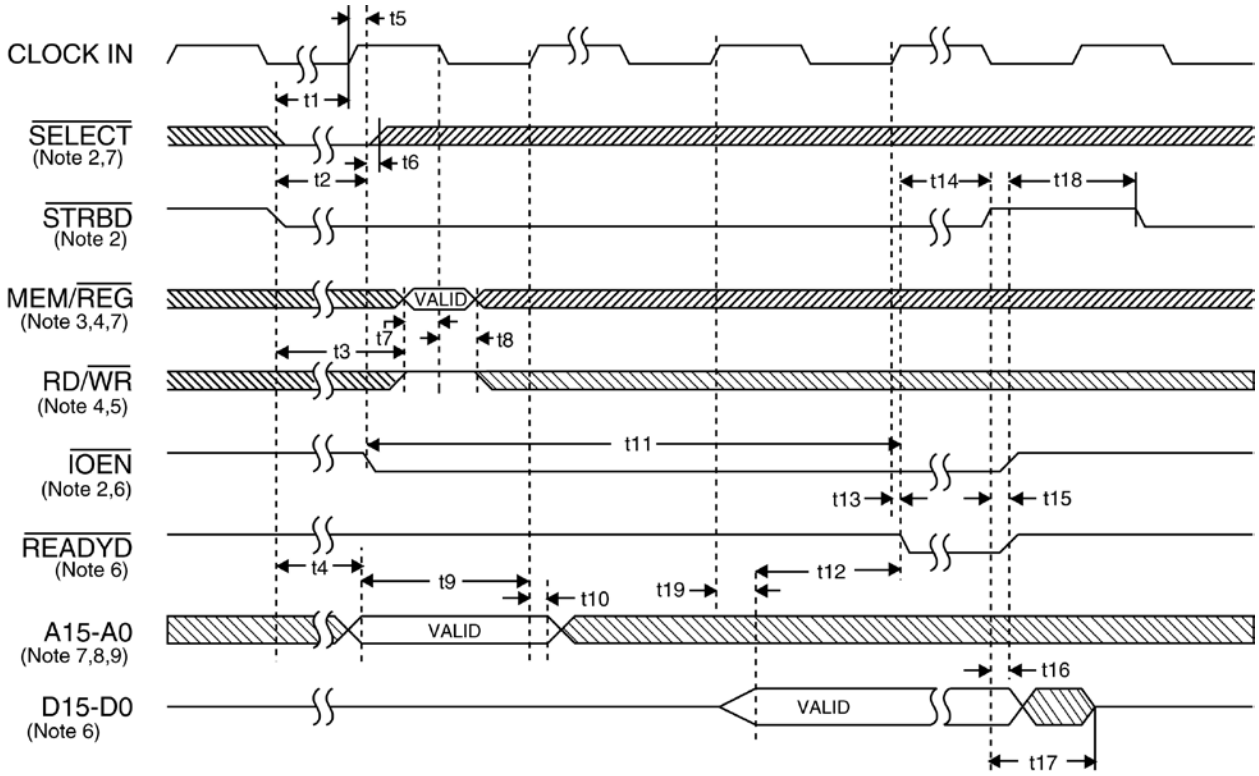


FIGURE 30. CPU READING RAM (SHOWN FOR 16-BIT, BUFFERED, NON-ZERO WAIT MODE, UNCONTENDED ACCESS)

Notes for TABLE 109 and FIGURE 30

1. For the 16-bit buffered configuration, the inputs TRIGGER_SEL and MSB/LSB may be connected to +5V or GND. For the non-zero wait interface ZEROWAIT*, must be connected to logic "1".
2. SELECT* and STRBD* may be tied together. IOEN* goes low on the second rising CLK edge when STRBD* is sampled low, provided SELECT* is also sampled low on that CLK edge and the BU-63825/925's protocol/memory management logic is not accessing internal RAM. If the protocol/memory management logic is accessing internal RAM, SELECT* is latched on the second rising CLK edge and transfer will begin once protocol/memory management access is complete. If SELECT* is sampled high on the second rising CLK edge, no transfer will take place. IOEN* will not drop.
3. MEM/REG* must be presented high for memory access, low for register access.
4. MEM/REG* and RD/WR* are buffered transparently until the first falling edge of CLK after IOEN* goes low. After this CLK edge, MEM/REG* and RD/WR* become latched internally.
5. The logic sense for RD/WR* in the diagram assumes that POLARITY_SEL is connected to logic "1". If POLARITY_SEL is connected to logic "0", RD/WR* must be asserted low to read.
6. The timing for IOEN*, READYD* and D15-D0 assumes a 50 pf load. For loading above 50 pf, the validity of IOEN*, READYD* and D15-D0 is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0 assume ADDR-LAT is connected to logic "1". Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A13 through A0. Registers are accessed by A4 through A0.
9. The address bus A15-A0 is internally buffered transparently until the first rising edge of CLK after IOEN* goes low. After this CLK edge, A15-A0 becomes latched internally.

TABLE 110. CPU WRITING RAM/REGISTERS (16-BIT, BUFFERED, NON-ZERO WAIT)									
CPU WRITING RAM OR REGISTERS (SHOWN FOR 16-BIT, BUFFERED, NON-ZERO WAIT MODE)									
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
t1	SELECT* and STRBD* low setup time prior to clock rising edge (Note 2,10)	10			15			ns	
t2	SELECT* and STRBD* low delay to IOEN* low (uncontended access @20 MHz) (Notes 2,6)			95.0				ns	
	SELECT* and STRBD* low delay to IOEN* low (contended access @20 MHz) (Notes 2,6)			2.2				µs	
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @16 MHz) (Notes 2,6)			107.5			107.5	ns	
	SELECT* and STRBD* low delay to IOEN* low (contended access @16 MHz) (Notes 2,6)			2.8			5.5	µs	
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @12 MHz) (Notes 2,6)			128.3			128.3	ns	
	SELECT* and STRBD* low delay to IOEN* low (contended access @12 MHz) (Notes 2,6)			3.7			7.4	µs	
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @10 MHz) (Notes 2,6)			145.0				ns	
	SELECT* and STRBD* low delay to IOEN* low (contended access @10 MHz) (Notes 2,6)			4.4				µs	
t3	MEM/REG* and RD/WR* setup time following SELECT* and STRBD* low (@20 MHz) (Notes 3,4,5,7)			10				ns	
	MEM/REG* and RD/WR* setup time following SELECT* and STRBD* low (@16 MHz) (Notes 3,4,5,7)			10			10	ns	
	MEM/REG* and RD/WR* setup time following SELECT* and STRBD* low (@12 MHz) (Notes 3,4,5,7)			20			20	ns	
	MEM/REG* and RD/WR* setup time following SELECT* and STRBD* low (@10 MHz) (Notes 3,4,5,7)			20				ns	
t4	Address valid setup time following SELECT* and STRBD* low (@20 MHz).			17				ns	
	Address valid setup time following SELECT* and STRBD* low (@16 MHz).			30			50	ns	
	Address valid setup time following SELECT* and STRBD* low (@12 MHz).			50			70	ns	
	Address valid setup time following SELECT* and STRBD* low (@10 MHz).			67				ns	
t5	Input Data Valid setup time following SELECT* and STRBD* low (@ 20MHz)			37				ns	
	Input Data Valid setup time following SELECT* and STRBD* low (@ 16MHz)			50			50	ns	
	Input Data Valid setup time following SELECT* and STRBD* low (@ 12MHz)			70			70	ns	
	Input Data Valid setup time following SELECT* and STRBD* low (@ 10MHz)			87				ns	
t6	CLOCK IN rising edge delay to IOEN* falling edge (Note 6)			35			30	ns	
t7	SELECT* hold time following IOEN* falling (Note 2)	0			0			ns	
t8	MEM/REG*, RD/WR* setup time prior to CLOCK IN falling edge (Notes 3,4,5,7)	10			10			ns	
t9	MEM/REG*, RD/WR* hold time following CLOCK IN falling edge (Notes 3,4,5,7)	30			25			ns	
t10	Address valid setup time prior to CLOCK IN rising edge (Notes 7,8,9)	30			10			ns	
t11	Input Data valid setup time prior to CLOCK IN rising edge	10			10			ns	
t12	Address valid hold time following CLOCK IN rising edge (Notes 7,8,9,10)	30			25			ns	
t13	Input Data valid hold time following CLOCK IN rising edge (Notes 9,10)	30			25			ns	
t14	IOEN* falling delay to READYD* falling (@20 MHz) (Notes 6,10)	135	150	165				ns	
	IOEN* falling delay to READYD* falling (@16 MHz) (Notes 6,10)	170	187.5	205	170	187.5	205	ns	
	IOEN* falling delay to READYD* falling (@12 MHz) (Notes 6,10)	235	250	265	235	250	265	ns	
	IOEN* falling delay to READYD* falling (@10 MHz) (Notes 6,10)	270	300	315				ns	
t15	CLOCK IN rising edge delay to READYD* falling (Note 6)			35			30	ns	
t16	READYD* falling to STRBD* rising release time.							ns	
t17	STRBD* rising edge delay to IOEN* rising edge and READYD* rising edge (Note 6)			30			30	ns	
t18	STRBD* valid high hold time from READYD rising edge	0			0			ns	

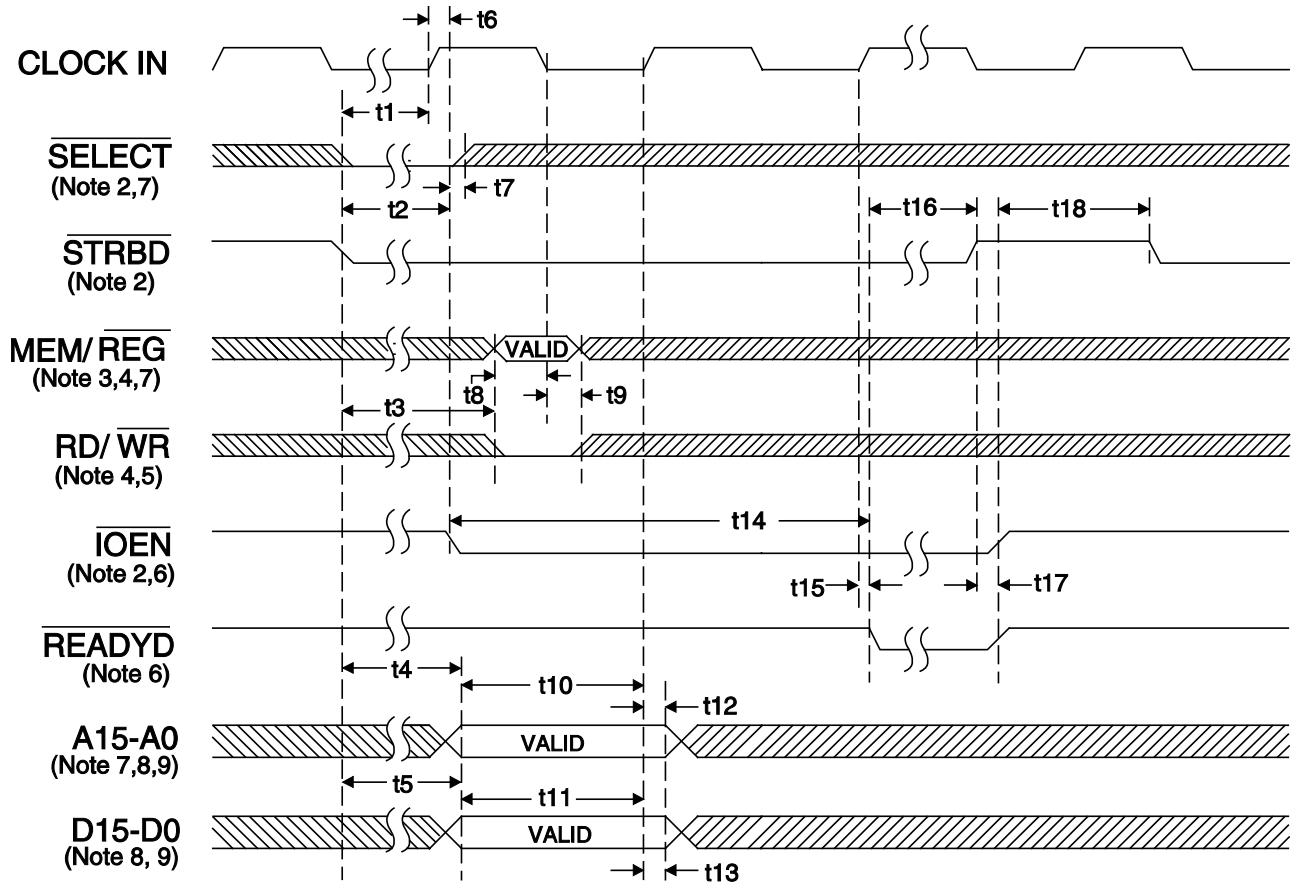


FIGURE 31. CPU WRITING RAM/REGISTERS (16-BIT, BUFFERED, NON-ZERO WAIT)

Notes for TABLE 110 and FIGURE 31:

1. For the 16-bit buffered non-zero wait configuration TRANSPARENT/BUFFERED* must be connected to logic "0". ZERO_WAIT* and DTREQ*/16/8* must be connected to logic "1". The inputs TRIGGER_SEL and MSB/LSB may be connected to either +5V or ground.
2. SELECT* and STRBD* may be tied together. IOEN* goes low on the first rising CLK edge when SELECT*•STRBD* is sampled low (satisfying t_i) and the ACE/Mini-ACE's protocol/memory management logic is not accessing the internal RAM. When this occurs, IOEN* goes low, starting the transfer cycle. After IOEN* goes low, SELECT* may be released high. For SP'ACE and SP'ACE II applications SELECT* is latched on the second rising CLK edge after STRBD* goes low. Therefore, for a transfer to occur, SELECT* must go low within 1 clock cycle of STRBD* falling.
3. MEM/REG* must be presented high for memory access, low for register access.
4. MEM/REG* and RD/WR* are buffered transparently until the first falling edge of CLK after IOEN* goes low. After this CLK edge, MEM/REG* and RD/WR* become latched internally.
5. The logic sense for RD/WR* in the diagram assumes that POLARITY_SEL is connected to logic "1." If POLARITY_SEL is connected to logic "0," RD/WR* must be asserted high to write.
6. The timing for IOEN* and READYD* outputs assumes a 50 pf load. For loading above 50 pf, the validity of IOEN* and READYD* is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/REG*, and SELECT* assumes ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A11 through A0 (A13 through A0 for 61585, 61586, 61582 (63825), and 61583 (63925) and A15 through A0 for 61688 and 61689). Registers are accessed by A4 through A0.
9. The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until the first rising edge of CLK after IOEN* goes low. After this CLK edge, A15-A0 and D15-D0 become latched internally.
10. Setup time given for use in worst case timing calculations. None of the ACE input signals are required to be synchronized to the system clock. For ACE applications only, where SELECT* and STRBD* do not meet the setup time of t1, but occur during the setup time of an internal flip-flop, an additional clock cycle will be inserted between the falling clock edge that latches MEM/REG* and RD/WR* and the rising clock edge that latches the address (A15-A0) and data (D15-D0). When this occurs, the pulse width of IOEN* falling to READYD* falling (t14) increases by one clock cycle and the address and data hold time (t12+t13) must be increased by one clock cycle.

8.18.1.3 For SP'ACE II (BU-63825/925) only

TABLE 111. CPU Writing ram/registers (16-BIT, BUFFERED, NON-ZERO WAIT)						
CPU WRITING RAM OR REGISTERS (SHOWN FOR 16-BIT, BUFFERED, NON-ZERO WAIT MODE)						
REF	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTE REFERENCE**
t1	SELECT* and STRBD* low setup time prior to CLOCK IN rising edge	15			ns	Note 2
t2	STRBD* low delay to IOEN* low (uncontended access @16 MHz)			170	ns	Notes 2,6
	STRBD* low delay to IOEN* low (contended access @16 MHz)			5.3	µs	Notes 2, 6
	STRBD* low delay to IOEN* low (uncontended access @12 MHz)			211.6	ns	
	STRBD* low delay to IOEN* low (contended access @12 MHz)			7.05	µs	
t3	MEM/REG* and RD/WR* setup time following STRBD* low (@16 MHz)			70	ns	
	MEM/REG* and RD/WR* setup time following STRBD* low (@12 MHz)			100	ns	
t4	Address valid setup time following STRBD* low (@16 MHz).			110	ns	
	Address valid setup time following STRBD* low (@12 MHz).			150	ns	
t5	Input Data valid setup following STRBD* low (@ 16 MHz)			110	ns	
	Input Data valid setup following STRBD* low (@ 12 MHz)			150		
t6	CLOCK IN rising edge delay to IOEN* falling edge			30	ns	
t7	SELECT* hold time following IOEN* falling edge	0			ns	Note 2
t8	MEM/REG*, RD/WR* setup time prior to CLOCK IN falling edge	10			ns	Notes 3, 4, 5
t9	MEM/REG*, RD/WR* hold time following CLOCK IN falling edge	25			ns	Notes 3, 4, 5
t10	Address valid setup prior to CLOCK IN rising edge	10			ns	
t11	Input Data valid setup prior to CLOCK IN falling edge	10			ns	
t12	Address hold time following CLOCK IN rising edge	25			ns	Note 9
t13	Input Data valid hold time following CLOCK IN rising edge	25			ns	Note 9
t14	IOEN* falling delay to READYD* falling (@ 16 MHz)	170	187.5	205	ns	Note 6
	IOEN* falling delay to READYD* falling (@ 12 MHz)	230	250	265	ns	Note 6
t15	CLOCK IN rising edge delay to READYD* falling edge			30	ns	
t16	READYD* falling to STRBD* rising release time			∞	ns	
t17	STRBD* rising delay to IOEN* rising, READYD* rising			40	ns	
t18	STRBD* high hold following READYD* rising	0			ns	

8.18.1.4 For SP'ACE II (BU-63825/925) only

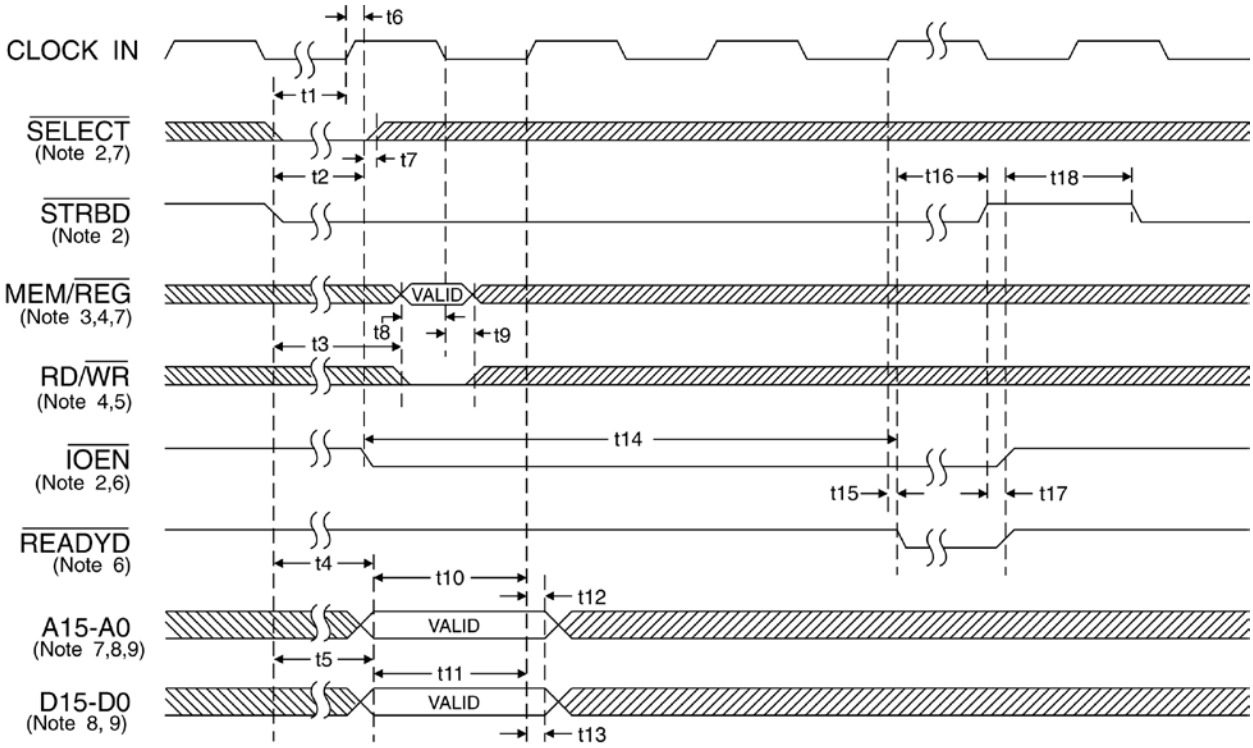


FIGURE 32. CPU WRITING RAM (SHOWN FOR 16-BIT, BUFFERED, NON-ZERO WAIT MODE, UNCONTENDED ACCESS)

Notes for TABLE 111 and FIGURE 32

1. For the 16-bit buffered configuration, the inputs TRIGGER_SEL and MSB/LSB may be connected to +5 V or GND. For the non-zero wait interface, ZEROWAIT* must be connected to logic "1".
2. SELECT* and STRBD* may be tied together. IOEN* goes low on the second rising CLK edge when STRBD* is sampled low, provided SELECT* is also sampled low on that CLK edge and the BU-63825/925's protocol/memory management logic is not accessing internal RAM, SELECT* is latched on the second rising CLK edge and transfer will begin once protocol/memory management access is complete. If SELECT* is sampled high on the second rising CLK edge, no transfer will take place. IOEN* will not drop.
3. MEM/REG* must be presented high for memory access, low for register access.
4. MEM/REG* and RD/WR* are buffered transparently until the first falling edge of CLK after IOEN* goes low. After this CLK edge, MEM/REG* and RE/WR* become latched internally.
5. The logic sense for RD/WR* in the diagram assumes that POLARITY_SEL is connected to logic "1". If POLARITY_SEL is connected to logic "0", RD/WR* must be asserted high to read.
6. The timing for the IOEN* and READYD* outputs assumes a 50 pf load. For loading above 50 pt, the validity of IOEN* and READYD* is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0 assumes ADDR-LAT is connected to logic "1". Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A13 through A0. Registers are accessed by A4 through A0.
9. The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until the first rising edge of CLK after IOEN* goes low. After this CLK edge, A15-A0 and D15-D0 become latched internally.

TABLE 112. CPU READING RAM/REGISTERS (16-BIT, BUFFERED, ZERO WAIT)

CPU READING RAM OR REGISTER (SHOWN FOR 16-BIT, BUFFERED, ZERO WAIT MODE)

REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	SELECT* and STRBD* low setup time prior to CLOCK IN rising (Note 10)	10			15			ns
t2	SELECT* and STRBD* low minimum pulse width	20			20			ns
t3	SELECT* and STRBD* low delay to Data valid (Note 13)			35			30	ns
t4	RD/WR* setup time prior to SELECT* and STRBD* low	10			10			ns
t5	RD/WR* high delay to Data valid (Note 13)			35			30	ns
t6A	Address setup time prior to STRBD* rising (Note 11)	10			10			ns
t6B	Address setup time prior to CLOCK IN rising (Note 12)	10			10			ns
t7A	MEM/REG* setup time prior to STRBD* rising (Note 11)	10			10			ns
t7B	MEM/REG* setup time prior to CLOCK IN rising (Note 12)	10			10			ns
t8A	SELECT* low hold time following STRBD* rising (Note 11)	0			0			ns
t8B	SELECT* low hold time following CLOCK IN rising (Note 12)	25			25			ns
t9A t9B	STRBD* rising setup time prior to CLOCK IN rising (Note 10)	15			20			ns
t10A	MEM/REG* and RD/WR* hold time following STRBD* rising (Note 11)	20			20			ns
t10B	MEM/REG* and RD/WR* hold time following CLOCK IN rising (Note 12)	25			25			ns
t11A	STRBD* rising delay to READYD* high (Note 11)			30			30	ns
t11B	CLOCK IN rising delay to READYD* high (Note 12)			35			30	ns
t12A	Address hold time following STRBD* rising (Note 11)	20			20			ns
t12B	Address hold time following CLOCK IN rising (Note 12)	25			25			ns
t13	Output Data hold time following STRBD* rising	0			0			ns
t14	STRBD* rising delay to Data tri-state			35			30	ns
t15	STRBD* rising delay to start of next transfer (uncontended access @20 MHz)	320						ns
	STRBD* rising delay to start of next transfer (contended access @20 MHz)	2.5						µs
	STRBD* rising delay to start of next transfer (uncontended access @16 MHz)	395			650			ns
	STRBD* rising delay to start of next transfer (contended access @16 MHz)	3.1			5.9			µs
	STRBD* rising delay to start of next transfer un(contended access @12 MHz)	520			850			ns
	STRBD* rising delay to start of next transfer (contended access @12 MHz)	4.1			7.8			µs
	STRBD* rising delay to start of next transfer (uncontended access @10 MHz)	620						ns
	STRBD* rising delay to start of next transfer (contended access @10 MHz)	4.9						µs
t16	STRBD* rising delay to IOEN* falling (uncontended access @20 MHz)			105				ns
	STRBD* rising delay to IOEN* falling (contended access @20 MHz)			2.2				µs
	STRBD* rising delay to IOEN* falling (uncontended access @16 MHz)			120			115	ns
	STRBD* rising delay to IOEN* falling (contended access @16 MHz)			2.8			5.5	µs
	STRBD* rising delay to IOEN* falling (uncontended access @12 MHz)			140			135	ns
	STRBD* rising delay to IOEN* falling (contended access @12 MHz)			3.7			7.4	µs
	STRBD* rising delay to IOEN* falling (uncontended access @10 MHz)			160				ns
	STRBD* rising delay to IOEN* falling (contended access @10 MHz)			4.4				µs
t17	CLOCK IN rising to IOEN* low (Note 2)			40			30	ns
t18	IOEN* low pulse width for RAM read (@20 MHz)	185	200	215				ns
	IOEN* low pulse width for REGISTER read (@20 MHz)	185	200	215				ns
	IOEN* low pulse width for RAM read (@16 MHz)	235	250	265	485	500	515	ns
	IOEN* low pulse width for REGISTER read (@16 MHz)	235	250	265	235	250	265	ns
	IOEN* low pulse width for RAM read (@12 MHz)	315	333	350	650	666	685	ns
	IOEN* low pulse width for REGISTER read (@12 MHz)	315	333	350	315	333	350	ns
	IOEN* low pulse width for RAM read (@16 MHz)	385	400	415				ns
	IOEN* low pulse width for REGISTER read (@16 MHz)	385	400	415				ns
t19	CLOCK IN rising delay to IOEN* rising			35			30	ns
t20	CLOCK IN falling delay to READYD* falling			35			30	ns
t21	READYD* low delay to start of next transfer (STRBD* falling)	0			0			ns

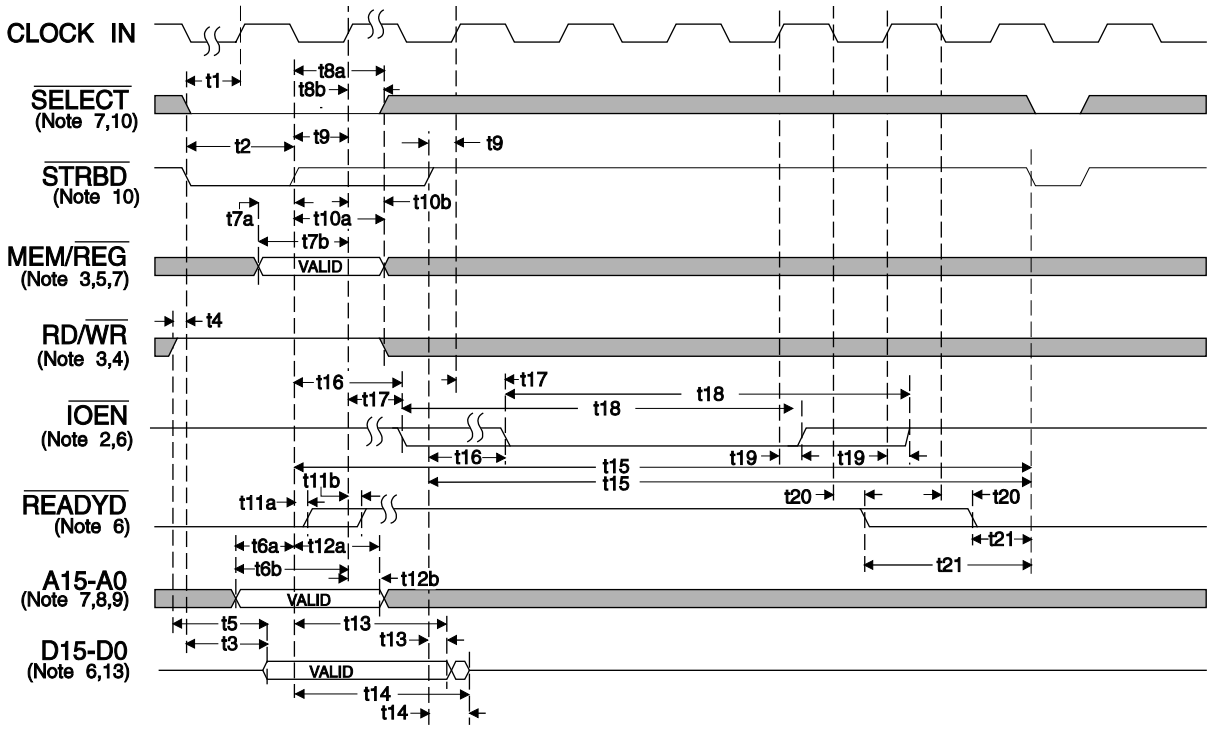


FIGURE 33. CPU READING RAM/REGISTERS (16-BIT, BUFFERED,ZERO WAIT)

Notes for TABLE 112 and FIGURE 33:

1. For the 16-bit buffered configuration, the inputs TRIGGER_SEL and MSB/LSB may be connected to +5V or GND. For the zero wait interface, ZERO_WAIT* must be connected to logic "0."
2. IOEN* goes low on the first rising CLK edge when READYD* is high and STRBD* is sampled high (satisfying t9 setup time) and the ACE's protocol/memory management logic is not accessing the internal RAM. When this occurs, IOEN* goes low, starting the internal transfer.
3. MEM/REG* and RD/WR* are buffered transparently until latched by STRBD* rising or second rising clock edge.
4. The logic sense for RD/WR* in the diagram assumes that POLARITY_SEL is connected to logic "1." If POLARITY_SEL is connected to logic "0," RD/WR* must be asserted low to read.
5. Data output is ready from register/RAM address referenced by the value of MEM/REG* and A15-A0 from the previous read cycle.
6. The timing for IOEN*, READYD* and D15-D0 assumes a 50 pf load. For loading above 50 pf, the validity of IOEN*, READYD*, and D15-D0 is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/REG*, and SELECT* assumes ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A11 through A0 (A13-A0 for BU-61585, 61586, 61582 (63825) and 61583 (63925) and A15 through A0 for 61688 and 61689)). Registers are accessed by A4 through A0.
9. The address bus A15-A0 is internally buffered transparently until latched by STRBD* rising or second rising clock edge.
10. Setup time given for use in worst case timing calculations. These signals do not have to be synchronized to the system clock. Removal of SELECT* prior to being latched on the second rising clock edge will have the same effect as STRBD* rising. For ACE applications, transfer will not start until SELECT* and STRBD* are both low. For SP'ACE and SP'ACE II, setup time applies only to STRBD*. SELECT* must go low prior to the second rising clock edge after STRBD* goes low or transfer will be blocked.
11. For the case in which STRBD* goes high before second rising clock edge in which SELECT* is low and STRBD* is low.
12. For the case in which STRBD* is low and SELECT* is low for a minimum of two rising clock edges for the ACE or low on the second edge for SP'ACE and SP'ACE II.
13. Valid data will be present on D15-D0 only after SELECT*, STRBD* and RD/WR* propagation delays (T3 and T5) are met.
14. For SP'ACE and SP'ACE II, in order to avoid data transfer errors, the "AND'd" combination of STRBD* and SELECT* must be kept at logic "1" for a minimum of 5.9 µS before both of these two signals are re-asserted to logic "0" to start the next transfer cycle. This means that at any time during this 5.9 µS, or at least until the SP'ACE(II) READYD* output transitions from low to high and back to low, at least one of the STRBD* or SELECT* inputs must be high.

TABLE 113 CPU WRITING RAM/REGISTERS (16-BIT, BUFFERED, ZERO WAIT)

CPU READING RAM OR REGISTER (SHOWN FOR 16-BIT, BUFFERED, ZERO WAIT MODE)

REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	SELECT* and STRBD* low setup time prior to CLOCK IN rising (Note 10)	10			15			ns
t2	SELECT* and STRBD* low minimum pulse width	20			20			ns
t3	RD/WR* setup time prior to SELECT* and STRBD* low	10			10			ns
t4A	Address setup time prior to STRBD* rising (Note 12)	10			10			ns
t4B	Address setup time prior to CLOCK IN rising (Note 13)	10			10			ns
t5A	Data setup time prior to STRBD* rising (Note 12)	10			15			ns
t5B	Data setup time prior to CLOCK IN rising (Note 13)	10			10			ns
t6A	MEM/REG* setup time prior to STRBD* rising (Note 12)	10			10			ns
t6B	MEM/REG* setup time prior to CLOCK IN rising (Note 13)	10			10			ns
t7A	SELECT* low hold time following STRBD* rising (Note 12)	0			0			ns
t7B	SELECT* low hold time following CLOCK IN rising (Note 13)	25			25			ns
t8	STRBD* rising setup time prior to CLOCK IN rising (Note 10)	15			20			ns
t9A	MEM/REG* and RD/WR* hold time following STRBD* rising (Note 12)	20			20			ns
t9B	MEM/REG* and RD/WR* hold time following CLOCK IN rising (Note 13)	25			25			ns
t10A	STRBD* rising delay to READYD* high (Note 12)			30			30	ns
t10B	CLOCK IN rising delay to READYD* high (Note 13)			35			30	ns
t11A	Address hold time following STRBD* rising (Note 12)	20			20			ns
t11B	Address hold time following CLOCK IN rising (Note 13)	25			25			ns
t12A	Input Data hold time following STRBD* rising (Note 12)	20			20			ns
t12B	Input Data hold time following CLOCK IN rising (Note 13)	25			25			ns
t13	STRBD* rising delay to IOEN* falling (uncontended access @20 MHz)			105				ns
	STRBD* rising delay to IOEN* falling (contended access @20 MHz)			2.2				µs
	STRBD* rising delay to IOEN* falling (uncontended access @16 MHz)			120			115	ns
	STRBD* rising delay to IOEN* falling (contended access @16 MHz)			2.8			5.5	µs
	STRBD* rising delay to IOEN* falling (uncontended access @12 MHz)			140			135	ns
	STRBD* rising delay to IOEN* falling (contended access @12 MHz)			3.7			7.4	µs
	STRBD* rising delay to IOEN* falling (uncontended access @10 MHz)			160				ns
	STRBD* rising delay to IOEN* falling (contended access @10 MHz)			4.4				µs
t14	STRBD* rising delay to start of next transfer (uncontended access @20 MHz)	320						ns
	STRBD* rising delay to start of next transfer (contended access @20 MHz)	2.5						µs
	STRBD* rising delay to start of next transfer (uncontended access @16 MHz)	395			650			ns
	STRBD* rising delay to start of next transfer (contended access @16 MHz)	3.1			5.9			µs
	STRBD* rising delay to start of next transfer un(contended access @12 MHz)	520			850			ns
	STRBD* rising delay to start of next transfer (contended access @12 MHz)	4.1			7.8			µs
	STRBD* rising delay to start of next transfer (uncontended access @10 MHz)	620						ns
	STRBD* rising delay to start of next transfer (contended access @10 MHz)	4.9						µs
t15	CLOCK IN rising to IOEN* low (Note 2)			40			30	ns
t16	IOEN* low pulse width for RAM read (@20 MHz)	185	200	215				ns
	IOEN* low pulse width for REGISTER read (@20 MHz)	185	200	215				ns
	IOEN* low pulse width for RAM read (@16 MHz)	235	250	265	485	500	515	ns
	IOEN* low pulse width for REGISTER read (@16 MHz)	235	250	265	235	250	265	ns
	IOEN* low pulse width for RAM read (@12 MHz)	315	333	350	650	666	685	ns
	IOEN* low pulse width for REGISTER read (@12 MHz)	315	333	350	315	333	350	ns
	IOEN* low pulse width for RAM read (@16 MHz)	385	400	415				ns
	IOEN* low pulse width for REGISTER read (@16 MHz)	385	400	415				ns
t17	CLOCK IN rising delay to IOEN* rising			35			30	ns
t18	CLOCK IN falling delay to READYD* falling			35			30	ns
t19	READYD* low delay to start of next transfer (STRBD* falling)	0			0			ns

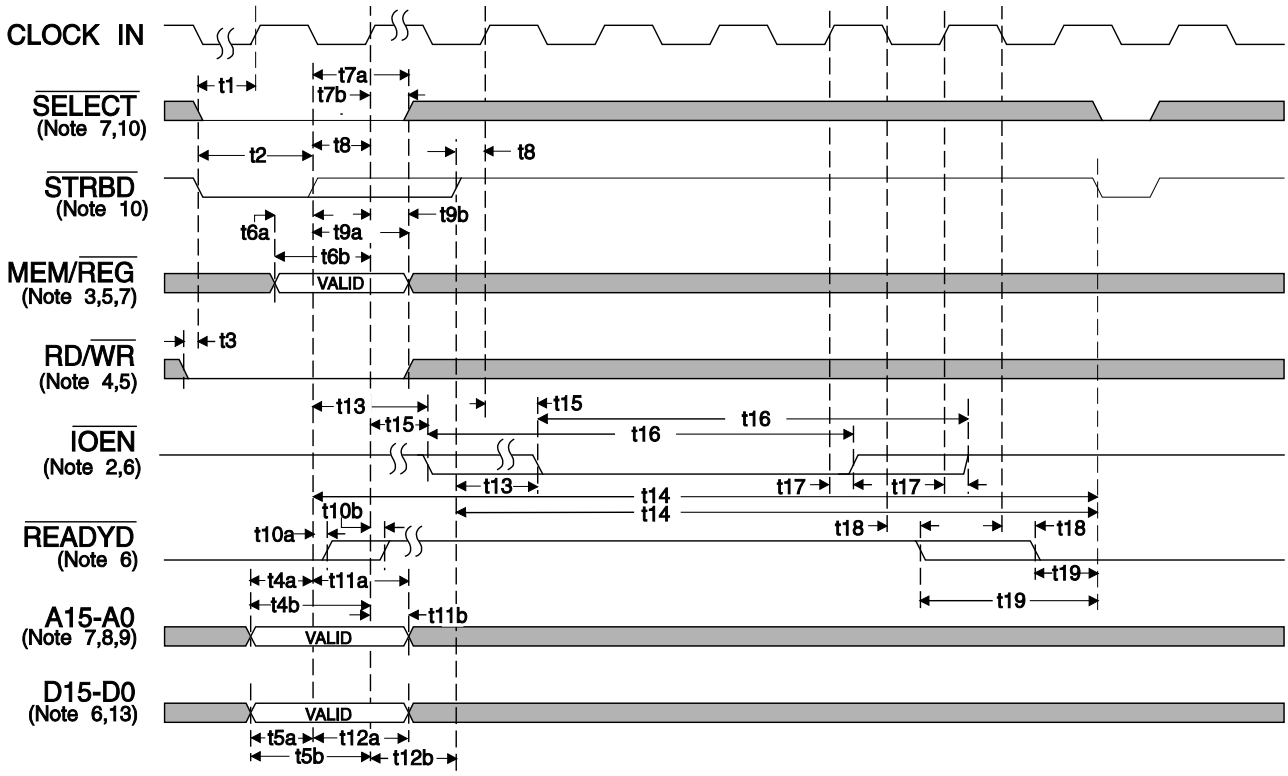


FIGURE 34. CPU WRITING RAM/REGISTERS (16-BIT,BUFFERED,ZERO WAIT)

Notes for TABLE 113 and FIGURE 34.

1. For the 16-bit buffered configuration, the inputs TRIGGER_SEL and MSB/LSB may be connected to +5V or GND. For the zero wait interface, ZERO_WAIT* must be connected to logic "0."
2. IOEN* goes low on the first rising CLK edge when READYD* is high and STRBD* is sampled high (satisfying t9 setup time) and the ACE's protocol/memory management logic is not accessing the internal RAM. When this occurs, IOEN* goes low, starting the internal transfer.
3. MEM/REG* must be presented high for memory access, low for register access.
4. MEM/REG* and RD/WR* are buffered transparently until latched by STRBD* rising or second CLK edge.
5. The logic sense for RD/WR* in the diagram assumes that POLARITY_SEL is connected to logic "1." If POLARITY_SEL is connected to logic "0," RD/WR* must be asserted high to write.
6. The timing for IOEN* and READYD* outputs assumes a 50 pf load. For loading above 50 pf, the validity of IOEN* and READYD* is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/REG*, and SELECT* assumes ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A11 through A0 (A13-A0 for BU-61585,61586,61582 (63825) and 61583 (63925) and A15 through A0 for 61688 and 61689). Registers are accessed by A4 through A0.
9. The address bus A15-A0 is internally buffered transparently until latched by STRBD* rising or second rising clock edge. The data bus starts to track when SELECT* and STRBD* are low until STRBD* rises or second rising clock edge.
10. Setup time given for use in worst case timing calculations. These signals do not have to be synchronized to the system clock. Removal of SELECT* prior to being latched on the second rising clock edge will have the same effect as STRBD* rising. For ACE applications, transfer will not start until SELECT* and STRBD* are both low. For SP'ACE and SP'ACE II, setup time applies only to STRBD*. SELECT* must go low prior to the second rising clock edge after STRBD* goes low or transfer will be blocked.
11. Data Bus will be actively driven when SELECT* is low, STRBD* is low and RD/WR* is high. To prevent a bus crash between the host driving the Data Bus and the ACE driving the Data Bus, RD/WR* must be setup prior to SELECT* low and STRBD* low
12. For the case in which STRBD* goes high before second rising clock edge in which SELECT* is low and STRBD* is low.
13. For case in which STRBD* is low and SELECT* is low for a minimum of two rising clock edges.
14. For SP'ACE and SP'ACE II, in order to avoid data transfer errors, the "AND'd" combination of STRBD* and SELECT* must be kept at logic "1" for a minimum of 5.9 µS before both of these two signals are re-asserted to logic "0" to start the next transfer cycle. This means that at any time during this 5.9 µS, or at least until the SP'ACE(II) READYD*output transitions from low to high and back to low, at least one of the STRBD* or SELECT* inputs must be high.

TABLE 114. CPU READING RAM/REGISTERS (TRANSPARENT MODE)

CPU READING RAM OR REGISTERS (SHOWN FOR TRANSPARENT MODE)

REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			SP'ACE II			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t1	SELECT* and STRBD* low setup time prior to CLOCK IN rising (Note 1)	10			10			10			ns
t2	SELECT* and STRBD* low delay to IOEN* low (uncontended access @20 MHz)			95.0							ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @20 MHz)			2.3							µs
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @16 MHz)			107.5			97.5			165	ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @16 MHz)			2.8			5.5			5.5	µs
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @12 MHz)			128.3			118.3			210	ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @12 MHz)			3.7			7.4			7.4	µs
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @10 MHz)			145.0							ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @10 MHz)			4.4							µs
t3	CLOCK IN rising edge delay to IOEN* falling			35			25			25	ns
t4	SELECT* low hold time following IOEN* falling	0			0			0			ns
t5	MEM/REG* and RD/WR* setup time prior to CLOCK IN falling	10			10			10			ns
t6	MEM/REG* and RD/WR* hold time following CLOCK IN falling	30			25			25			ns
t7	IOEN* falling delay to READYD* falling reading INT. RAM (@20 MHz)	185	200	215							ns
	IOEN* falling delay to READYD* falling reading REG. or EXT. RAM (@20 MHz)	185	200	215							ns
	IOEN* falling delay to READYD* falling reading INT. RAM (@16 MHz)	235	250	265	485	500	520	485	500	520	ns
	IOEN* falling delay to READYD* falling reading REG. or EXT. RAM (@16 MHz)	235	250	265	235	250	265	235	250	265	ns
	IOEN* falling delay to READYD* falling reading INT. RAM (@12 MHz)	315	333	350	650	666	685	650	666	685	ns
	IOEN* falling delay to READYD* falling reading REG. or EXT. RAM (@12 MHz)	315	333	350	315	333	350	315	333	350	ns
	IOEN* falling delay to READYD* falling reading INT. RAM (@10 MHz)	385	400	415							ns
	IOEN* falling delay to READYD* falling reading REG. or EXT. RAM (@10 MHz)	385	400	415							ns
t8	CLOCK IN rising delay to MEMENA-OUT* low			35			30			30	ns
t9	MEMENA-IN setup time prior to CLOCK IN rising	5			10			10			ns
t10	MEMENA-IN hold time following CLOCK IN rising	30			25			25			ns
t11	CLOCK IN rising delay to MEMOE* falling			40			30			30	ns
t12	Address setup time prior to CLOCK IN rising	30			10			10			ns
t13	Address hold time following CLOCK IN rising	30			25			25			ns

TABLE 114. CPU READING RAM/REGISTERS (TRANSPARENT MODE)											
CPU READING RAM OR REGISTERS (SHOWN FOR TRANSPARENT MODE)											
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			SP'ACE II			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t14	CLOCK IN rising to Output Data valid			60			50			50	ns
t15	CLOCK IN rising delay to READYD* falling			35			30			30	ns
t16	STRBD* release time following READYD* falling (Internal RAM @20 MHz)			4.2							µs
	STRBD* release time following READYD* falling (External RAM @20 MHz)			4.2							µs
	STRBD* release time following READYD* falling (Internal RAM @16 MHz)			3.6			3.3			3.3	µs
	STRBD* release time following READYD* falling (External RAM @16 MHz)			3.6			3.6			3.6	µs
	STRBD* release time following READYD* falling (Internal RAM @12 MHz)			3.0			2.7			2.7	µs
	STRBD* release time following READYD* falling (External RAM @12 MHz)			3.0			3.0			3.0	µs
	STRBD* release time following READYD* falling (Internal RAM @10 MHz)			2.7							µs
	STRBD* release time following READYD* falling (External RAM @10 MHz)			2.7							µs
t17	STRBD* rising delay to IOEN* rising, READYD* rising, MEMENA-OUT rising, and MEMOE* rising			30			35			35	ns
t18	Output Data hold time following STRBD* rising	0			0			0			ns
t19	STRBD* rising delay to Output Data tri-state			40			40			40	ns
t20	READYD* rising delay to STRBD* falling (delay to start of next transfer cycle)	0			0			0			ns

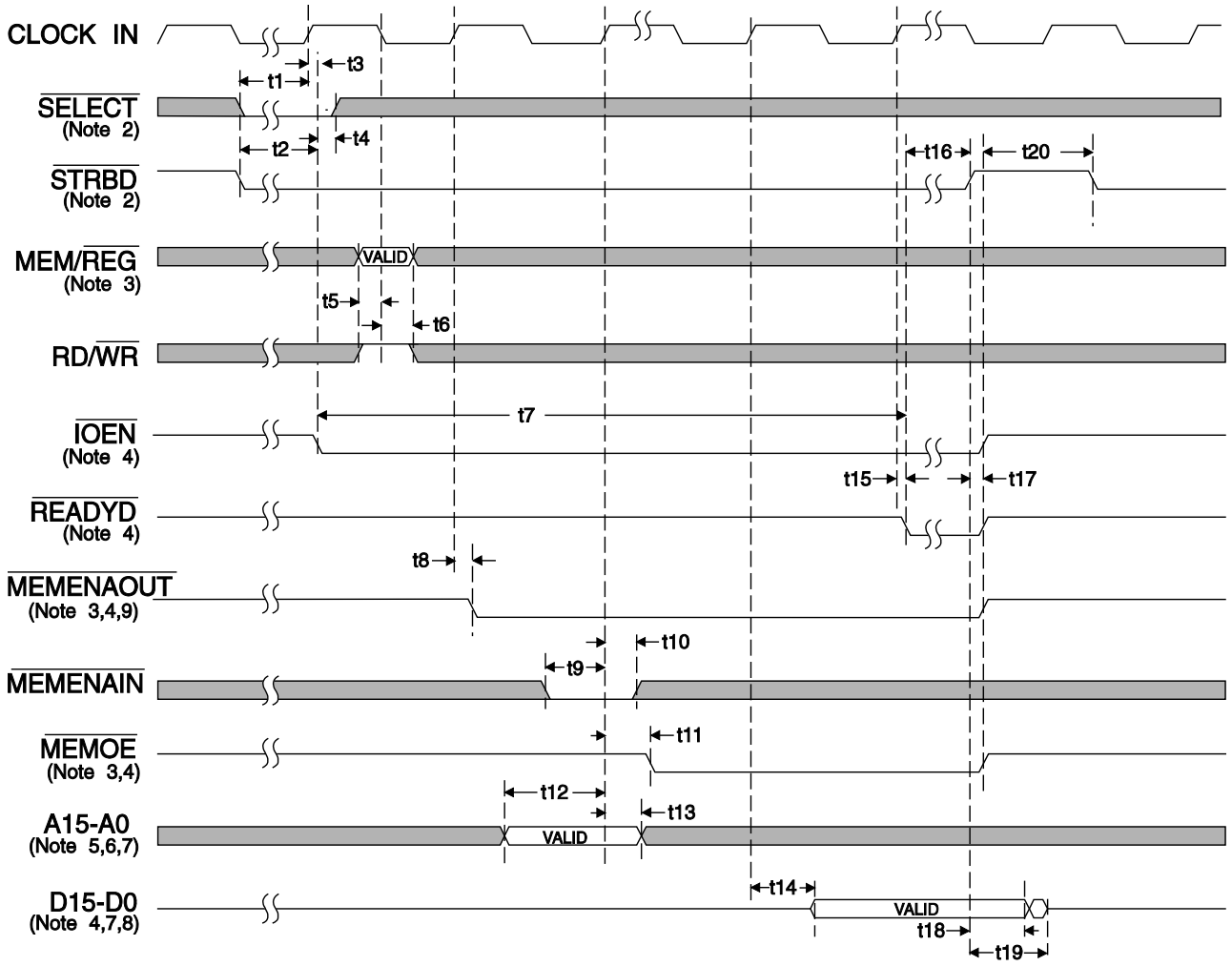


FIGURE 35. CPU READING RAM/REGISTERS (TRANSPARENT MODE)

Notes for TABLE 114 and FIGURE 35:

1. Setup time given for use in worst case timing calculations. These signals do not have to be synchronized to the system clock.
2. SELECT* and STRBD* may be tied together. IOEN* goes low on the first rising CLK edge when SELECT* STRBD* is sampled low (satisfying t_1) and the ACE/Mini-ACE's protocol/memory management logic is not actively performing a DMA transfer (i.e.,., DTACK* is logic 1). When this occurs, IOEN* goes low, starting the transfer cycle. After IOEN* goes low, SELECT* may be released high. For SP'ACE and SP'ACE II applications, SELECT* is latched on the second rising CLK edge after STRBD* goes low. Therefore, for a transfer to occur, SELECT* must go low within 1 clock cycle of STRBD* falling. For Sp'ACE II IOEN* goes LOW on the 2nd rising clock edge following STRBD* provided that SELECT* is LOW and there is no contention.
3. The timing diagram (FIGURE 351) illustrates the CPU reading RAM. For register reads from the ACE (MEM/REG* input = logic 0) the MEMENA-OUT* and MEMOE* output signals are not asserted, and therefore maintain a logic "1" level.
4. The timing for IOEN*, READYD*, MEMENA_OUT*, MEMOE*, and D15-D0 assumes a 50 pf load. For loading above 50 pf, the validity of IOEN*, READYD*, MEMENA_OUT*, MEMOE*, and D15-D0 is delayed by an additional 0.14 ns/pf typical, 0.28 ns/pf max.
5. Internal RAM is accessed by A11 through A0 (A13 through A0 for BU-61585,61586,61582 (63825) and 61583 (63925) and A15 through A0 for 61688 and 61689)). Registers are accessed by A4 through A0.
6. The address bus A15-A0 is internally buffered transparently until the second rising edge of CLOCK_IN after IOEN* goes low. After this CLOCK_IN edge, A15-A0 becomes latched internally.
7. For read operations from external memory, the address (A15-A0) must be held longer to meet the hold time requirements of the external memory used. The data bus (D15-D0) will remain in tri-state. D15-D0 will only be driven by the external RAM. All data bus timing will now be dependent on the external RAM used.
8. For SP'ACE and SP'ACE II applications only, the data bus (D15-D0) will remain in tri-state during register reads from address $18 thru $1F.
9. For Mini-ACE series applications, MEMENA-OUT* is not available to the user. This signal may be replaced by logically AND'ing DTACK* and IOEN*. However, it should be noted that DTACK* and IOEN* assert low one clock period earlier than the corresponding MEMENA-OUT* providing longer address decode and memory enable times.

TABLE 115. CPU WRITING RAM/REGISTERS (TRANSPARENT MODE)

CPU WRITING RAM OR REGISTERS (SHOWN FOR TRANSPARENT MODE)											
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			SP'ACE II			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t1	SELECT* and STRBD* low setup time prior to CLOCK IN rising (Note 1)	10			10			10			ns
t2	SELECT* and STRBD* low delay to IOEN* low (uncontended access @20 MHz)			95.0							ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @20 MHz)			2.2							µs
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @16 MHz)			107.5			97.5			165	ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @16 MHz)			2.8			5.5			5.5	µs
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @12 MHz)			128.3			118.3			210	ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @12 MHz)			3.7			7.4			7.4	µs
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @10 MHz)			145.0							ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @10 MHz)			4.4							µs
t3	CLOCK IN rising edge delay to IOEN* falling			35			25			25	ns
t4	SELECT* low hold time following IOEN* falling	0			0			0			ns
t5	MEM/REG* and RD/WR* setup time prior to CLOCK IN falling	10			10			10			ns
t6	MEM/REG* and RD/WR* hold time following CLOCK IN falling	30			25			25			ns
t7	IOEN* falling delay to READYD* falling (@ 20 MHz)	185	200	215							ns
	IOEN* falling delay to READYD* falling (@ 16 MHz)	235	250	265	235	250	270	235	250	270	ns
	IOEN* falling delay to READYD* falling (@ 12 MHz)	315	333	350	315	333	355	315	333	355	ns
	IOEN* falling delay to READYD* falling (@ 10 MHz)	385	400	415							ns
t8	CLOCK IN rising delay to MEMENA-OUT* low			35			30			30	ns
t9	MEMENA-IN setup time prior to CLOCK IN rising	5			10			10			ns
t10	MEMENA-IN hold time following CLOCK IN rising	30			25			25			ns
t11	CLOCK IN rising delay to MEMWR* falling			40			30			30	ns
t12	Address setup time prior to CLOCK IN rising	30			10			10			ns
t13	Address hold time following CLOCK IN rising	30			25			25			ns
t14	Input Data setup time prior to CLOCK IN rising	10			10			10			ns
t15	Input Data hold time following CLOCK IN rising	30			25			25			ns
t16	MEMWR* low pulse width (@20 MHz)	37		62							ns
	MEMWR* low pulse width (@16 MHz)	50		75	55		70	55		70	ns
	MEMWR* low pulse width (@12 MHz)	70		95	75		90	75		90	ns
	MEMWR* low pulse width (@10 MHz)	87		112							ns
t17	CLOCK IN rising delay to MEMWR* rising			30			30			30	ns
t18	CLOCK IN rising delay to READYD* falling			35			30			30	ns
t19	STRBD* release time following READYD* falling (@20 MHz)			4.2							µs
	STRBD* release time following READYD* falling (@16 MHz)			3.6			3.6			3.6	µs
	STRBD* release time following READYD* falling (@12 MHz)			3.0			3.0			3.0	µs
	STRBD* release time following READYD* falling (@10 MHz)			2.7							µs
t20	STRBD* rising delay to IOEN* rising, READYD* rising, and MEMENA-OUT rising			30			35			35	ns
t21	READYD* rising delay to STRBD* falling (delay to start of next transfer cycle)	0			0			0			ns

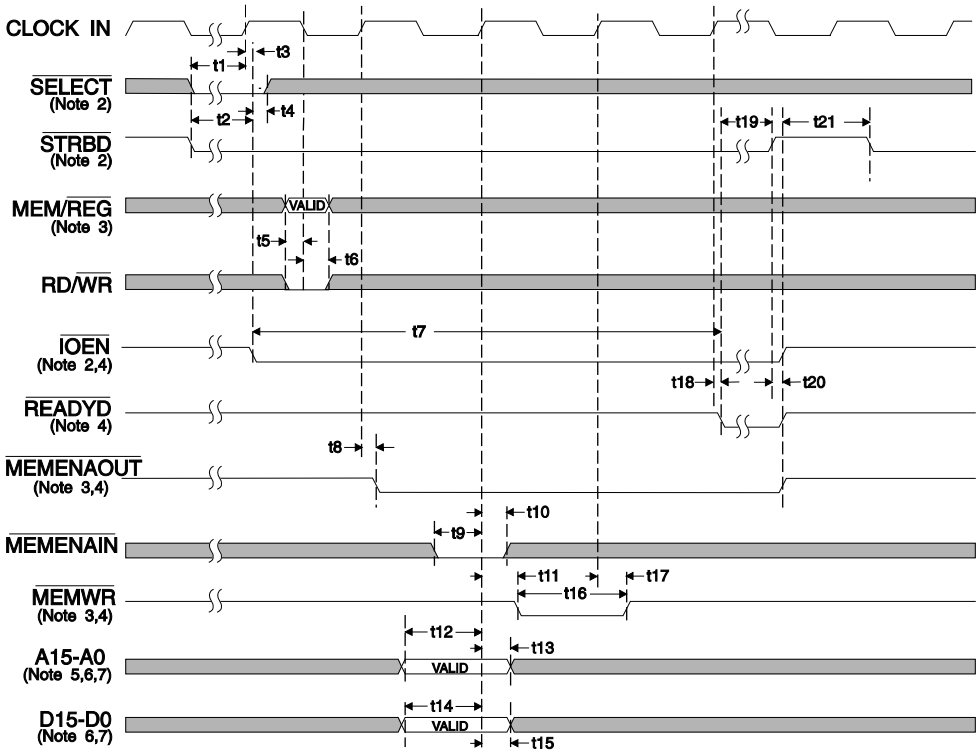


FIGURE 36. CPU WRITING RAM/REGISTERS (TRANSPARENT MODE)

Notes for TABLE 115 and FIGURE 36:

1. Setup time given for use in worst case timing calculations. These signals do not have to be synchronized to the system clock.
2. SELECT* and STRBD* may be tied together. IOEN* goes low on the first rising CLK edge when SELECT* STRBD* is sampled low (satisfying t_1) and the ACE/Mini-ACE's protocol/memory management logic is not active performing a DMA transfer (i.e.,., DTACK* is logic 1). When this occurs, IOEN* goes low, starting the transfer cycle. After IOEN* goes low, SELECT* may be released high. For SP'ACE and SP'ACE II application, SELECT* is latched on the second rising CLK edge after STRBD* goes low. Therefore, for a transfer to occur, SELECT* must go low within 1 clock cycle of STRBD* falling. For Sp'ACE II IOEN* goes LOW on the 2nd rising clock edge following STRBD* provided that SELECT* is LOW and there is no contention.
3. The timing diagram (FIGURE 36) illustrates the CPU writing to RAM. For register writes, the ACE (MEM/REG* input = logic 0) the MEMENA-OUT* and MEMWR* output signals are not asserted, and therefore maintain a logic "1" level.
4. The timing for IOEN*, READYD*, MEMENA_OUT*, and MEMWR* assumes a 50 pf load. For loading above 50 pf, the validity of IOEN*, READYD*, MEMENA_OUT*, and MEMWR* is delayed by an additional 0.14 ns/pf typical, 0.28 ns/pf max.
5. Internal RAM is accessed by A11 through A0 (A13-A0 for BU-61585,61586,61582 (63825) and 61583 (63925) and A15 through A0 for 61688 and 61689). Registers are accessed by A4 through A0.
6. The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until the second rising edge of CLOCK_IN after IOEN* goes low. After this CLOCK_IN edge, A15-A0 and D15-D0 become latched internally.
7. For write operation to external memory, the address (A15-A0) and data (D15-D0) must be held longer to meet the hold time requirements of the external memory used.
8. For Mini-ACE series applications, MEMENA-OUT* is not available to the user. This signal may be replaced by logically AND'ing DTACK* and IOEN*. However, it should be noted that DTACK* and IOEN* assert low one clock period earlier than the corresponding MEMENA-OUT* providing longer address decode and memory enable times.

TABLE 116. CPU READING RAM/REGISTERS USING ACE/Mini-ACE (8-BIT, NON-ZERO WAIT)

CPU READING RAM OR REGISTERS (SHOWN FOR 8-BIT NON-ZERO WAIT STATE MODE)					
REF	**DESCRIPTION**	**ACE/MINI-ACE**			**UNITS**
		MIN	**TYP**	**MAX**	
t1	SELECT* and STRBD* low setup time prior to clock rising edge (Note 2,12)	10			ns
t2	SELECT* and STRBD* low delay to IOEN* low (uncontended access @20 MHz) (Notes 2,6)			95.0	ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @20 MHz) (Notes 2,6)			2.2	µs
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @16 MHz) (Notes 2,6)			107.5	ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @16 MHz) (Notes 2,6)			2.8	µs
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @12 MHz) (Notes 2,6)			128.3	ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @12 MHz) (Notes 2,6)			3.7	µs
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @10 MHz) (Notes 2,6)			145.0	ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @10 MHz) (Notes 2,6)			4.4	µs
t3	Address setup time prior to CLOCK IN rising	30			ns
t4	SELECT* hold time following IOEN* falling (Note 2)	0			ns
t5	MEM/REG*, RD/WR*, MSB/LSB setup time prior to clock falling edge (Notes 3,4,5,10,11)	10			ns
t6	MEM/REG*, RD/WR*, MSB/LSB hold time following clock falling edge (Notes 3,4,5,10,11)	30			ns
t7	Address hold time following clock rising edge (Note 9)	30			ns
t8	IOEN* falling delay to READYD* falling (@20 MHz) (Note 6)	185	200	215	ns
	IOEN* falling delay to READYD* falling (@16 MHz) (Note 6)	235	250	265	ns
	IOEN* falling delay to READYD* falling (@12 MHz) (Note 6)	315	333	350	ns
	IOEN* falling delay to READYD* falling (@10 MHz) (Note 6)	385	400	415	ns
t9	Output Data valid prior to READYD* falling (@20 MHz) (Note 6, 10, 11)	20			ns
	Output Data valid prior to READYD* falling (@16 MHz) (Note 6, 10, 11)	33			ns
	Output Data valid prior to READYD* falling (@12 MHz) (Note 6, 10, 11)	54			ns
	Output Data valid prior to READYD* falling (@10 MHz) (Note 6, 10, 11)	70			ns
t10	Clock rising delay to READYD* falling (Note 6)			35	ns
t11	READYD* falling to STRBD* rising release time (Note 6)				ns
t12	STRBD* rising delay to IOEN* rising and READYD* rising (Note 6)			30	ns
t13	Output Data hold time following STRBD* rising	0			ns
t14	STRBD* rising delay to output Data tri-state			40	ns
t15	STRBD* high hold time from READYD* rising	0			ns
t16	CLK rising edge delay to IOEN* falling			35	ns
t17	CLK rising edge delay to Output data valid			60	ns

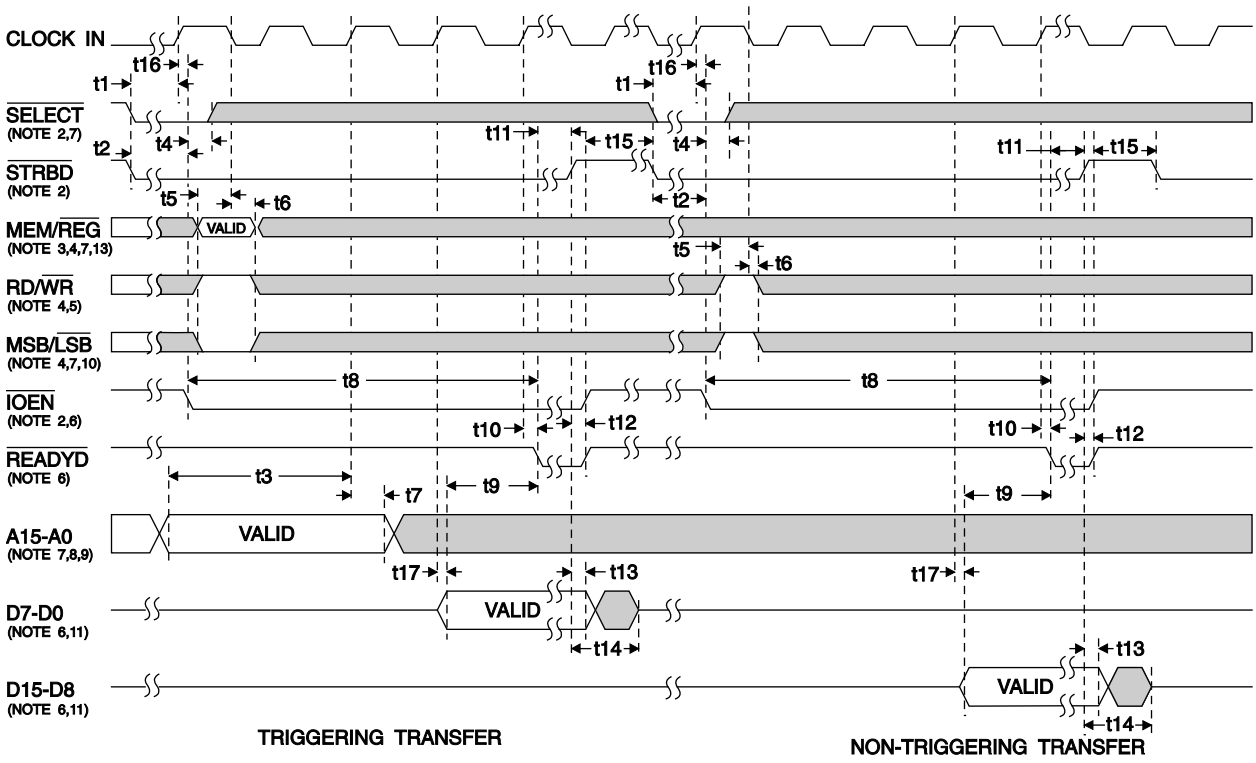


FIGURE 37. CPU READING RAM/REGISTERS USING ACE/Mini-ACE (8-BIT,NON-ZERO WAIT)

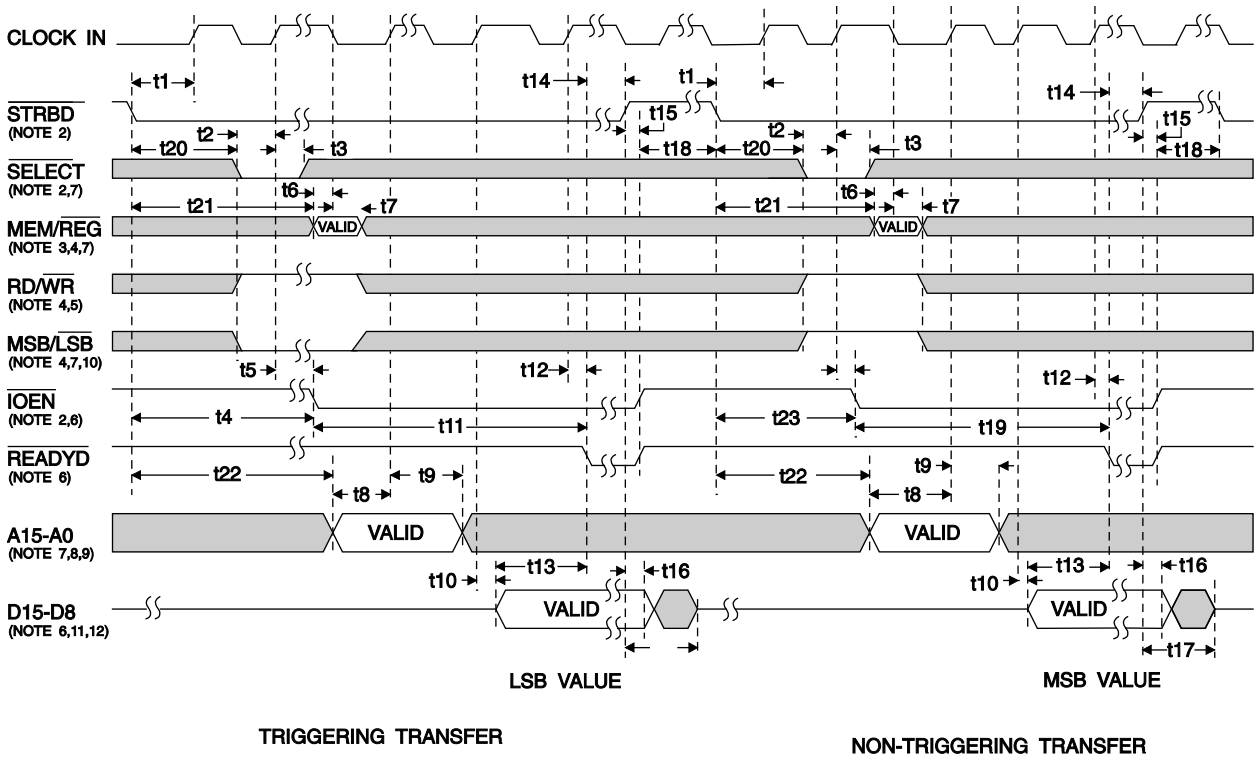
Notes for TABLE 116 and FIGURE 37:

1. For 8 bit non-zero wait interface, TRANSPARENT/BUFFERED* and DTREQ*/16/8* must be connected to logic "0". ZERO_WAIT* must be connected to logic "1".
2. SELECT* and STRBD* may be tied together. IOEN* goes low on the first rising CLK edge when SELECT* and STRBD* are both sampled low (satisfying t_1) and the ACE/Mini-ACE's protocol/memory management logic is not accessing the internal RAM. When this occurs, IOEN* goes low, starting the transfer cycle. After IOEN* goes low, SELECT* may be released high.
3. MEM/REG* must be presented high for memory access, low for register access. MEM/REG* is a "don't care" for nontriggering transfers.
4. MEM/REG*, MSB/LSB* and RD/WR* are buffered transparently until the first falling edge of CLK after IOEN* goes low. After this CLK edge, MEM/REG*, MSB/LSB* and RD/WR* become latched internally.
5. RD/WR* must be presented high for read accesses and low for write accesses. The logic sense for RD/WR* does not depend on the state of the POLARITY_SEL input in the 8-bit mode.
6. The timing for IOEN*, READYD* and D15-D0 assumes a 50 pf load. For loading above 50 pf, the validity of IOEN*, READYD*, and D15-D0 is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/REG*, SELECT* and MSB/LSB* assumes ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A11 through A0 (A13-A0 for BU-61585 and 61586 and A15-A0 for 61688 and 61689). Registers are accessed by A4 through A0.
9. The address bus A15-A0 is internally buffered transparently until the first rising edge of CLK after IOEN* goes low. After this CLK edge, A15-A0 becomes latched internally.
10. The polarity of the MSB/LSB* input signal assumes that the POLARITY_SEL input signal is connected to logic "0." If POLARITY_SEL is connected to logic "1," MSB/LSB* will be high for LSB transfers and low for MSB transfers.
11. The order of the consecutive byte transfers assumes that the TRIGGER_SEL input signal is connected to logic "0." The actual transfer from the internal RAM or Register takes place during the "triggering transfer" (LSB in this case). If TRIGGER_SEL is connected to logic "1," the order of the byte transfers would be MSB followed by LSB and the triggering transfer would be the MSB.
12. Setup time given for use in worst case timing calculations. None of the ACE input signals are required to be synchronized to the system clock.
13. For early ACE applications, to maintain valid data longer than 1 clock after READYD* falling edge, MSB/LSB* must be in the appropriate state. Therefore, the hold time for MSB/LSB* should be until STRBD* rises. Not applicable for Mini-ACE series terminals.

TABLE 117. CPU READING RAM/REGISTERS USING SP'ACE and SP'ACE II (8-BIT,NON-ZERO WAIT)

CPU READING RAM OR REGISTERS
(SHOWN FOR 8-BIT NON-ZERO WAIT STATE MODE)
(PLEASE SEE APPENDIX G FOR PRODUCT ADVISORY REGARDING SP'ACE AND SP'ACE II OPERATING IN 8-BIT BUFFERED NON-ZERO WAIT MODE)

REF	DESCRIPTION	SP'ACE			UNITS
		MIN	TYP	MAX	
t1	STRBD* low setup time prior to clock rising edge (Note 2)	15			ns
t2	SELECT*, RD/WR*, and MSB/LSB* setup time prior to clock rising edge	30			ns
t3	SELECT* hold time following clock rising edge	25			ns
t4	STRBD* low delay to IOEN* low (uncontended access @16 MHz)			170	ns
	STRBD* low delay to IOEN* low (uncontended access @12 MHz)			211.6	ns
	STRBD* low delay to IOEN* low (contended access @16 MHz)			5.6	µs
	STRBD* low delay to IOEN* low (contended access @12 MHz)			7.5	µs
t5	CLOCK IN delay to IOEN* falling (uncontended)			30	ns
t6	MEM/REG* setup time prior to clock falling	10			ns
t7	MEM/REG*, RD/WR*, and MSB/LSB* hold time after clock falling	25			ns
t8	Address setup time prior to clock rising	10			ns
t9	Address hold time following clock rising	25			ns
t10	CLOCK IN delay to Output data valid			50	ns
t11	IOEN* falling edge delay to READYD* falling (reading RAM @16 MHz)	420	437.5	455	ns
	IOEN* falling edge delay to READYD* falling (reading RAM @12 MHz)	565	583.3	600	ns
	IOEN* falling edge delay to READYD* falling (reading REGISTER @16 MHz)	170	187.5	205	ns
	IOEN* falling edge delay to READYD* falling (reading REGISTER @12 MHz)	235	250.0	265	ns
t12	CLOCK IN delay to READYD* falling			30	ns
t13	Output data valid prior to READYD* falling (@16 MHz)	33			ns
t13	Output data valid prior to READYD* falling (@12 MHz)	54			ns
t14	READYD* falling delay to STRBD* rising				ns
t15	STRBD* rising delay to IOEN* and READYD* rising			30	ns
t16	Output data hold time following STRBD* rising	0			ns
t17	STRBD* rising to Output Data tri-state			40	ns
t18	STRBD* high hold time following READYD rising	0			ns
t19	IOEN* falling edge delay to READYD* falling (@16 MHz)	170	187.5	205	ns
t19	IOEN* falling edge delay to READYD* falling (@12 MHz)	235	250	265	ns
t20	SELECT*, RD/WR* and MSB/LSB* setup time following STRBD* low (@16 MHz)			32	ns
t20	SELECT*, RD/WR* and MSB/LSB* setup time following STRBD* low (@12 MHz)			53	ns
t21	MEM/REG* setup time following STRBD* low (@16 MHz)			72	ns
t21	MEM/REG* setup time following STRBD* low (@12 MHz)			103	ns
t22	Address setup time following STRBD* low (@16 MHz)			115	ns
t22	Address setup time following STRBD* low (@12 MHz)			156	ns
t23	STRBD* low delay to IOEN* (@16 MHz)			170	ns
t23	STRBD* low delay to IOEN* (@12 MHz)			212	ns



(Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)

FIGURE 38. CPU READING RAM/REGISTERS USING SP'ACE and SP'ACE II (8-BIT, NON-ZERO WAIT)

Notes for TABLE 117 and FIGURE 38:

1. For 8 bit non-zero wait interface, ZERO_WAIT* must be connected to logic "1". TRANSPARENT/BUFFERED* and DTREQ*/16/8* must be connected to logic "0".
2. Setup time given for use in worst case timing calculations. STRBD* does not have to be synchronized to the system clock. On the second rising clock edge after STRBD* has gone low, the SELECT* input will be sampled. If low, IOEN* will go low providing this is a non-triggering transfer or if a triggering transfer, providing the protocol/memory management is not accessing the internal RAM. If it is, IOEN* will go low on the first available rising clock edge signifying the start of the transfer cycle.
3. MEM/REG* must be presented high for memory access, low for register access.
4. MEM/REG*, MSB/LSB*, and RD/WR* are buffered transparently until the first falling edge of CLK after IOEN* goes low. After this CLK edge, MEM/REG*, MSB/LSB* and RD/WR* become latched internally.
5. RD/WR* must be presented high for read accesses and low for write accesses. The logic sense for RD/WR* does not depend on the state of the POLARITY_SEL input in the 8-bit mode.
6. The timing for IOEN*, READYD* and D15-D8 assumes a 50 pf load. For loading above 50 pf, the validity of IOEN*, READYD*, and D15-D8 is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/REG*, SELECT*, and MSB/LSB* assumes ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A13 through A0. Registers are accessed by A4 through A0.
9. The address bus A15-A0 is internally buffered transparently until the first rising edge of CLK after IOEN* goes low. After this CLK edge, A15-A0 becomes latched internally.
10. The polarity of the MSB/LSB* input signal assumes that the POLARITY_SEL input signal is connected to logic "0." If POLARITY_SEL is connected to logic "1," MSB/LSB* will be high for LSB transfers and low for MSB transfers.
11. The order of the consecutive byte transfers assumes that the TRIGGER_SEL input signal is connected to logic "0." The actual transfer from the internal RAM or Register takes place during the "triggering transfer" (LSB in this case). If TRIGGER_SEL is connected to logic "1," the order of the byte transfers would be MSB followed by LSB and the triggering transfer would be the MSB.
12. The data bus D15-D8 will remain tri-stated during register reads from hex address 18 thru 1F regardless of whether it is a triggering or non-triggering transfer. Therefore MEM/REG* and/or address will be required on the non-triggering transfer.

TABLE 118. CPU WRITING RAM/REGISTERS USING ACE/Mini-ACE (8-BIT,NON-ZERO WAIT)

CPU WRITING RAM OR REGISTERS (SHOWN FOR 8-BIT, BUFFERED, NON-ZERO WAIT STATE MODE)

REF	DESCRIPTION	ACE/MINI-ACE			UNITS
		MIN	TYP	MAX	
t1	SELECT* and STRBD* low setup time prior to clock rising edge (Note 2,12)	10			ns
t2	SELECT* and STRBD* low delay to IOEN* low (uncontended access @20 MHz) (Notes 2,6)			95.0	ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @20 MHz) (Notes 2,6)			2.2	µs
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @16 MHz) (Notes 2,6)			107.5	ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @16 MHz) (Notes 2,6)			2.8	µs
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @12 MHz) (Notes 2,6)			128.3	ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @12 MHz) (Notes 2,6)			3.7	µs
	SELECT* and STRBD* low delay to IOEN* low (uncontended access @10 MHz) (Notes 2,6)			145.0	ns
	SELECT* and STRBD* low delay to IOEN* low (contended access @10 MHz) (Notes 2,6)			4.4	µs
t3	Address setup time prior to CLOCK IN rising	30			ns
t4	SELECT* hold time following IOEN* falling (Note 2)	0			ns
t5	MEM/REG*, RD/WR*, MSB/LSB setup time prior to clock falling edge (Notes 3,4,5,10,11)	10			ns
t6	MEM/REG*, RD/WR*, MSB/LSB hold time following clock falling edge (Notes 3,4,5,10,11)	30			ns
t7	Address and Data hold time following clock rising (Note 9)	30			ns
t8	IOEN* falling delay to READYD* falling (@20 MHz) (Note 6)	185	200	215	ns
	IOEN* falling delay to READYD* falling (@16 MHz) (Note 6)	235	250	265	ns
	IOEN* falling delay to READYD* falling (@12 MHz) (Note 6)	315	333	350	ns
	IOEN* falling delay to READYD* falling (@10 MHz) (Note 6)	385	400	415	ns
t9	Clock rising delay to READYD* falling			35	ns
t10	READYD* falling to STRBD* rising release time				ns
t11	STRBD* rising delay to IOEN* rising and READYD rising			30	ns
t12	STRBD* high hold time from READYD* rising	0			ns
t13	Input Data setup time prior to clock rising edge	10			ns
t14	Clock rising delay to IOEN* falling			35	ns

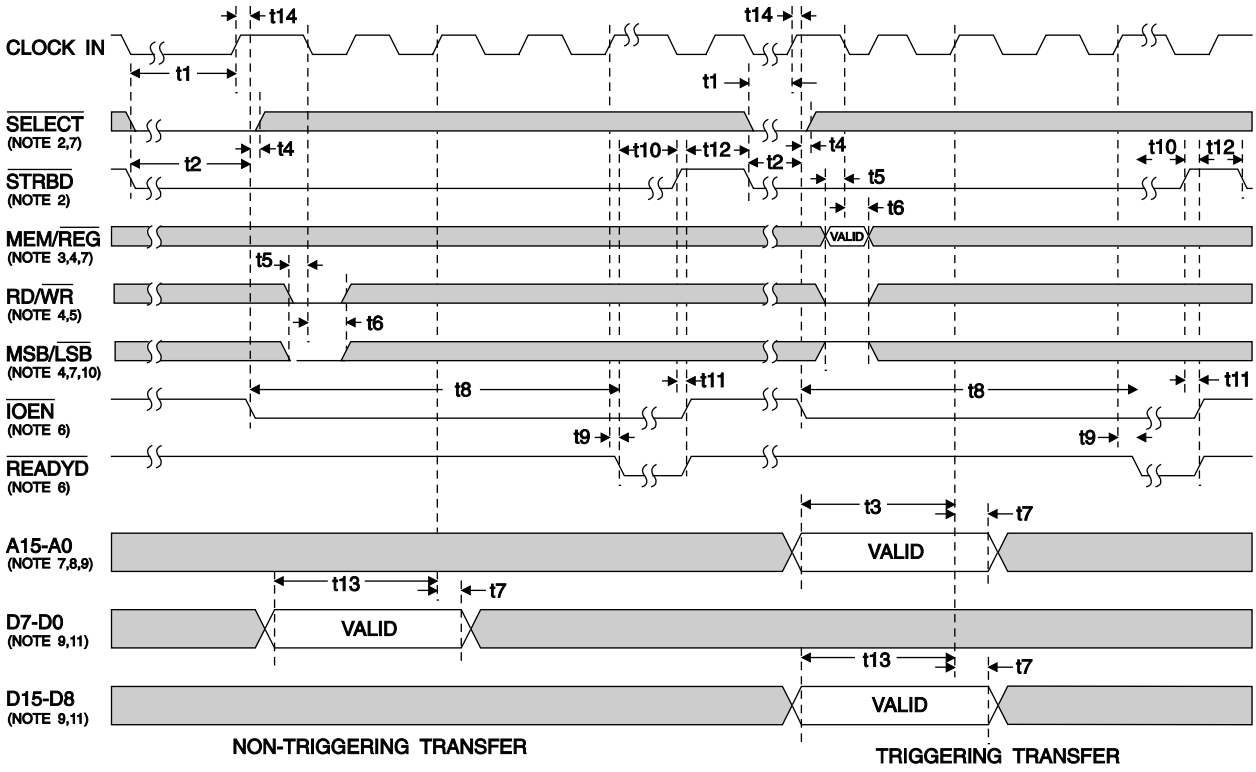


FIGURE 39. CPU WRITING RAM/REGISTERS USING ACE/Mini-ACE (8-BIT, NON-ZERO WAIT)

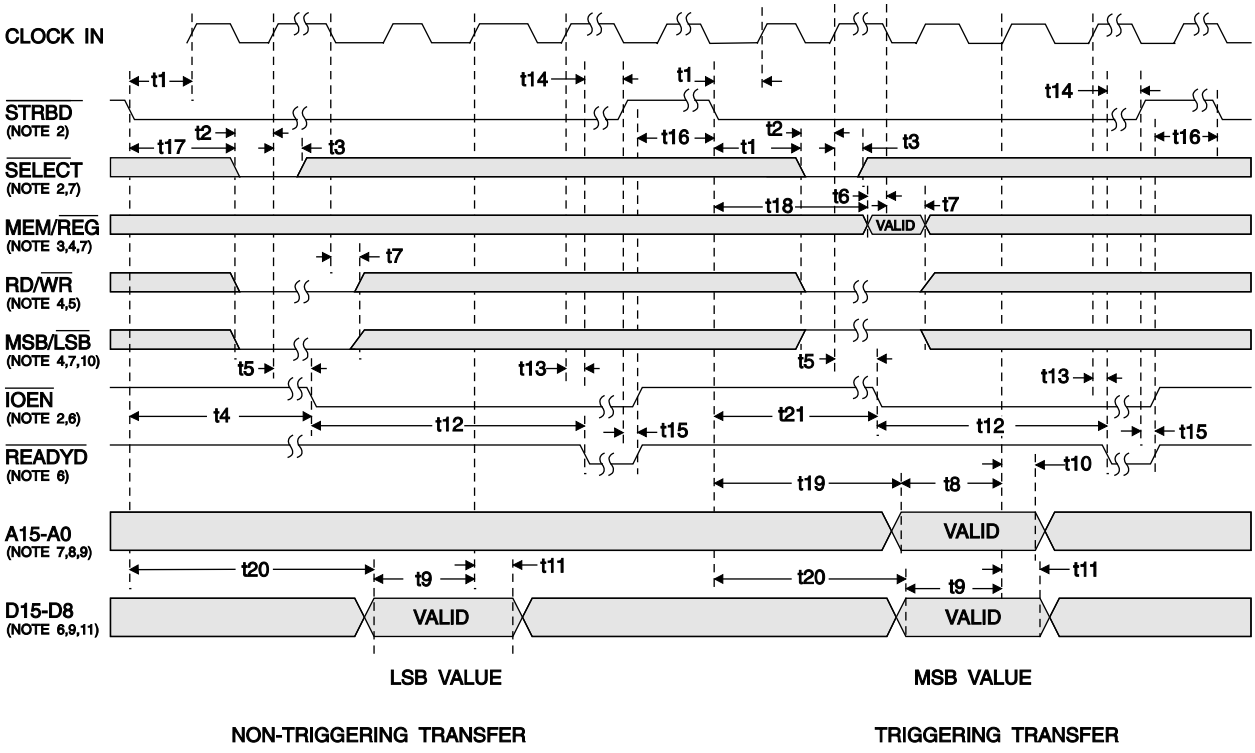
Notes for TABLE 118 and FIGURE 39:

1. For 8 bit non-zero wait interface, TRANSPARENT/BUFFERED* and DTREQ*/16/8* must be connected to logic "0". ZERO_WAIT* must be connected to logic "1".
2. SELECT* and STRBD* may be tied together. IOEN* goes low on the first rising CLK edge when SELECT* and STRBD* are both sampled low (satisfying t_2) and the ACE/Mini-ACE's protocol/memory management logic is not accessing the internal RAM. When this occurs, IOEN* goes low, starting the transfer cycle. After IOEN* goes low, SELECT* may be released high.
3. MEM/REG* must be presented high for memory access, low for register access. MEM/REG* is a "don't care" for nontriggering transfers.
4. MEM/REG*, MSB/LSB*, and RD/WR* are buffered transparently until the first falling edge of CLK after IOEN* goes low. After this CLK edge, MEM/REG*, MSB/LSB*, and RD/WR* become latched internally.
5. RD/WR* must be presented high for read accesses and low for write accesses. The logic sense for RD/WR* does not depend on the state of the POLARITY_SEL input in the 8-bit mode.
6. The timing for IOEN* and READYD* outputs assumes a 50 pf load. For loading above 50 pf, the validity of IOEN* and READYD* is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/REG*, SELECT* and MSB/LSB* assumes ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A11 through A0 (A13 through A0 for BU-61585 and 61586 and A15 through A0 for 61688 and 61689). Registers are accessed by A4 through A0.
9. The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until the first rising edge of CLK after IOEN* goes low. After this CLK edge, A15-A0 and D15-D0 become latched internally.
10. The polarity of the MSB/LSB* input signal assumes that the POLARITY_SEL input signal is connected to logic "0." If POLARITY_SEL is connected to logic "1," MSB/LSB* will be high for LSB transfers and low for MSB transfers.
11. The order of the consecutive byte transfers assumes that the TRIGGER_SEL input signal is connected to logic "0." The actual transfer to the internal RAM or Register takes place during the "triggering transfer" (MSB in this case). If TRIGGER_SEL is connected to logic "1," the order of the byte transfers would be MSB followed by LSB and the triggering transfer would be the LSB.
12. Setup time given for use in worst case timing calculations. None of the ACE input signals are required to be synchronized to the system clock.

TABLE 119. CPU WRITING RAM/REGISTERS USING SP'ACE and SP'ACE II (8-BIT,NON-ZERO WAIT)

CPU WRITING RAM OR REGISTERS
(SHOWN FOR 8-BIT, BUFFERED, NON-ZERO WAIT STATE MODE)
(PLEASE SEE APPENDIX G FOR PRODUCT ADVISORY REGARDING SP'ACE AND SP'ACE II OPERATING IN 8-BIT BUFFERED NON-ZERO WAIT MODE)

REF	DESCRIPTION	SP'ACE			UNITS
		MIN	TYP	MAX	
t1	STRBD* low setup time prior to clock rising edge (Note 2)	15			ns
t2	SELECT*, RD/WR*, and MSB/LSB* setup time prior to clock rising edge	30			ns
t3	SELECT* hold time following clock rising edge	25			ns
t4	STRBD* low delay to IOEN* low (contended access @16 MHz)			405	ns
	STRBD* low delay to IOEN* low (contended access @12 MHz)			530	ns
	STRBD* low delay to IOEN* low (uncontended access @16 MHz)			170	ns
	STRBD* low delay to IOEN* low (uncontended access @12 MHz)			211.6	ns
t5	CLOCK IN delay to IOEN* falling (uncontended)			30	ns
t6	MEM/REG* setup time prior to clock falling edge	10			ns
t7	MEM/REG*, RD/WR*, and MSB/LSB* hold time after clock falling edge	25			ns
t8	Address setup time prior to clock rising edge	10			ns
t9	Input data setup time prior to clock rising edge	10			ns
t10	Address hold time following clock rising edge	25			ns
t11	Input data hold time following clock rising edge	25			ns
t12	IOEN* falling edge delay to READYD* falling (@16 MHz)	170	187.5	205	ns
	IOEN* falling edge delay to READYD* falling (@12 MHz)	235	250	265	ns
t13	CLOCK IN delay to READYD* falling			30	ns
t14	READYD* falling delay to STRBD rising				ns
t15	STRBD* rising delay to IOEN* and READYD* rising			30	ns
t16	STRBD* high hold time following READYD* rising	0			ns
t17	SELECT*, RD/WR*, and MSB/LSB* setup time following STRBD* low (@16 MHz)			32	ns
	SELECT*, RD/WR*, and MSB/LSB* setup time following STRBD* low (@12 MHz)			53	ns
t18	MEM/REG* setup time following STRBD* low (@16 MHz)			72	ns
	MEM/REG* setup time following STRBD* low (@12 MHz)			103	ns
t19	Address setup time following STRBD* low (@16 MHz)			115	ns
	Address setup time following STRBD* low (@12 MHz)			156	ns
t20	Input data setup time following STRBD* low (@16 MHz)			115	ns
	Input data setup time following STRBD* low (@12 MHz)			156	ns
t21	STRBD* low delay to IOEN* low (uncontended @16 MHz)			170	ns
	STRBD* low delay to IOEN* low (contended @16 MHz)			5.6	µs
	STRBD* low delay to IOEN* low (uncontended @12 MHz)			211.6	ns
	STRBD* low delay to IOEN* low (contended @12 MHz)			7.5	µs



(Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)

FIGURE 40. CPU WRITING RAM/REGISTERS USING SP'ACE and SP'ACE II (8-BIT, NON-ZERO WAIT)

Notes for TABLE 119 and FIGURE 40:

1. For 8 bit non-zero wait interface, ZER0_WAIT* must be connected to logic "1". TRANSPARENT/BUFFERED* and DTREQ*/16/8* must be connected to logic "0".
2. Setup time given for use in worst case timing calculations. STRBD* does not have to be synchronized to the system clock. On the second rising clock edge after STRBD* has gone low, the SELECT* input will be sampled. If low, IOEN* will go low providing the protocol/memory management is not accessing the internal RAM (for a triggering transfer) or completing a prior write transfer (for a non-triggering transfer). If it is, IOEN* will go low on the first available rising clock edge signifying the start of the transfer cycle.
3. MEM/REG* must be presented high for memory access, low for register access. MEM/REG* is a "don't care" for nontriggering transfers unless REG_WR* is being used (BU-65621 configuration only). If so, timing requirements are the same as the triggering transfer.
4. MEM/REG*, MSB/LSB*, and RD/WR* are buffered transparently until the first falling edge of CLK after IOEN* goes low. After this CLK edge, MEM/REG*, MSB/LSB*, and RD/WR* become latched internally.
5. RD/WR* must be presented high for read accesses and low for write accesses. The logic sense for RD/WR* does not depend on the state of the POLARITY_SEL input in the 8-bit mode.
6. The timing for IOEN* and READYD* outputs assumes a 50 pf load. For loading above 50 pf, the validity of IOEN* and READYD* is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/REG*, SELECT* and MSB/LSB* assumes ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A13 through A0. Registers are accessed by A4 through A0. Address is a "don't care" for non-triggering transfers unless REG_WR* is being used(BU-65621 configuration only). If so, timing requirements are the same as the triggering transfer.
9. The address bus A15-A0 and data bus D15-D8 are internally buffered transparently until the first rising edge of CLK after IOEN* goes low. After this CLK edge, A15-A0 and D15-D8 become latched internally.
10. The polarity of the MSB/LSB* input signal assumes that the POLARITY_SEL input signal is connected to logic "0." If POLARITY_SEL is connected to logic "1," MSB/LSB* will be high for LSB transfers and low for MSB transfers.
11. The order of the consecutive byte transfers assumes that the TRIGGER_SEL input signal is connected to logic "0." The actual transfer to the internal RAM or Register takes place during the "triggering transfer" (MSB in this case). If TRIGGER_SEL is connected to logic "1," the order of the byte transfers would be MSB followed by LSB and the triggering transfer would be the LSB.

TABLE 120. CPU READING RAM/REGISTERS (8-BIT,ZERO WAIT)

CPU READING RAM OR REGISTER (SHOWN FOR 8-BIT, ZERO WAIT MODE)

REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	RD/WR* and MSB/LSB* setup time prior to STRBD* and SELECT* falling (Note 11)	10			10			ns
t2	SELECT* and STRBD* low setup time prior to CLOCK IN rising (Note 10)	10			15			ns
t3	SELECT* and STRBD* low minimum pulse width	20			20			ns
t4	SELECT* and STRBD* low delay to Data valid (Note 13)			35			30	ns
t5	RD/WR* and MSB/LSB delay to Data valid (Note 13)			45			40	ns
t6A	MEM/REG* setup time prior to STRBD* rising (Note 11)	10			10			ns
t6B	MEM/REG* setup time prior to CLOCK IN rising (Note 12)	10			10			ns
t7A	MEM/REG*, RD/WR*, MSB/LSB* hold time following STRBD* rising (Note 11)	20			20			ns
t7B	MEM/REG*, RD/WR*, MSB/LSB* hold time following CLOCK IN rising (Note 12)	25			25			ns
t8A	Address setup time prior to STRBD* rising (Note 11)	10			10			ns
t8B	Address setup time prior to CLOCK IN rising (Note 12)	10			10			ns
t9A	Address hold time following STRBD* rising (Note 11)	20			20			ns
t9B	Address hold time following CLOCK IN rising (Note 12)	25			25			ns
t10	Output Data hold time following STRBD* rising	0			0			ns
t11	STRBD* rising delay to Data tri-state			35			30	ns
t12	STRBD* rising delay to IOEN* low (uncontended access @20 MHz)			107				ns
	STRBD* rising delay to IOEN* low (contended access @20 MHz)			2.2				µs
	STRBD* rising delay to IOEN* low (uncontended access @16 MHz)			120			115	ns
	STRBD* rising delay to IOEN* low (contended access @16 MHz)			2.8			5.5	µs
	STRBD* rising delay to IOEN* low (uncontended access @12 MHz)			140			135	ns
	STRBD* rising delay to IOEN* low (contended access @12 MHz)			3.7			7.4	µs
	STRBD* rising delay to IOEN* low (uncontended access @10 MHz)			157				ns
	STRBD* rising delay to IOEN* low (contended access @10 MHz)			4.4				µs
t13A	STRBD* rising delay to READYD* high (Note 11)			30			30	ns
t13B	CLOCK IN rising delay to READYD* high (Note 12)			35			30	ns
t14	CLOCK IN rising to IOEN* low			40			30	ns
t15A	SELECT* low hold time following STRBD* rising (Note 11)	0			0			ns
t15B	SELECT* low hold time following CLOCK IN rising (Note 12)	25			25			ns
t16	STRBD* rising setup time prior to CLOCK IN rising (Note 10)	15			20			ns
t17	IOEN* low pulse width for RAM read (@20 MHz)	185	200	215				ns
	IOEN* low pulse width for REGISTER read (@20 MHz)	185	200	215				ns
	IOEN* low pulse width for RAM read (@16 MHz)	235	250	265	485	500	515	ns
	IOEN* low pulse width for REGISTER read (@16 MHz)	235	250	265	235	250	265	ns
	IOEN* low pulse width for RAM read (@12 MHz)	315	333	350	650	666	685	ns
	IOEN* low pulse width for REGISTER read (@12 MHz)	315	333	350	315	333	350	ns
	IOEN* low pulse width for RAM read (@10 MHz)	385	400	415				ns
	IOEN* low pulse width for REGISTER read (@10 MHz)	385	400	415				ns
t18	STRBD* rising delay to start of next transfer (uncontended access @20 MHz)	320						ns
	STRBD* rising delay to start of next transfer (contended access @20 MHz)	2.5						µs
	STRBD* rising delay to start of next transfer (uncontended access @16 MHz)	395			650			ns
	STRBD* rising delay to start of next transfer (contended access @16 MHz)	3.1			5.9			µs
	STRBD* rising delay to start of next transfer (uncontended access @12 MHz)	520			850			ns
	STRBD* rising delay to start of next transfer (contended access @12 MHz)	4.1			7.8			µs
	STRBD* rising delay to start of next transfer (uncontended access @10 MHz)	620						ns
	STRBD* rising delay to start of next transfer (contended access @10 MHz)	4.9						µs
t19	CLOCK IN rising delay to IOEN* rising			35			30	ns
t20	CLOCK IN falling delay to READYD* falling			35			30	ns
t21	STRBD* rising delay to start of next transfer (SELECT* and STRBD* low) trigger	20			20			ns

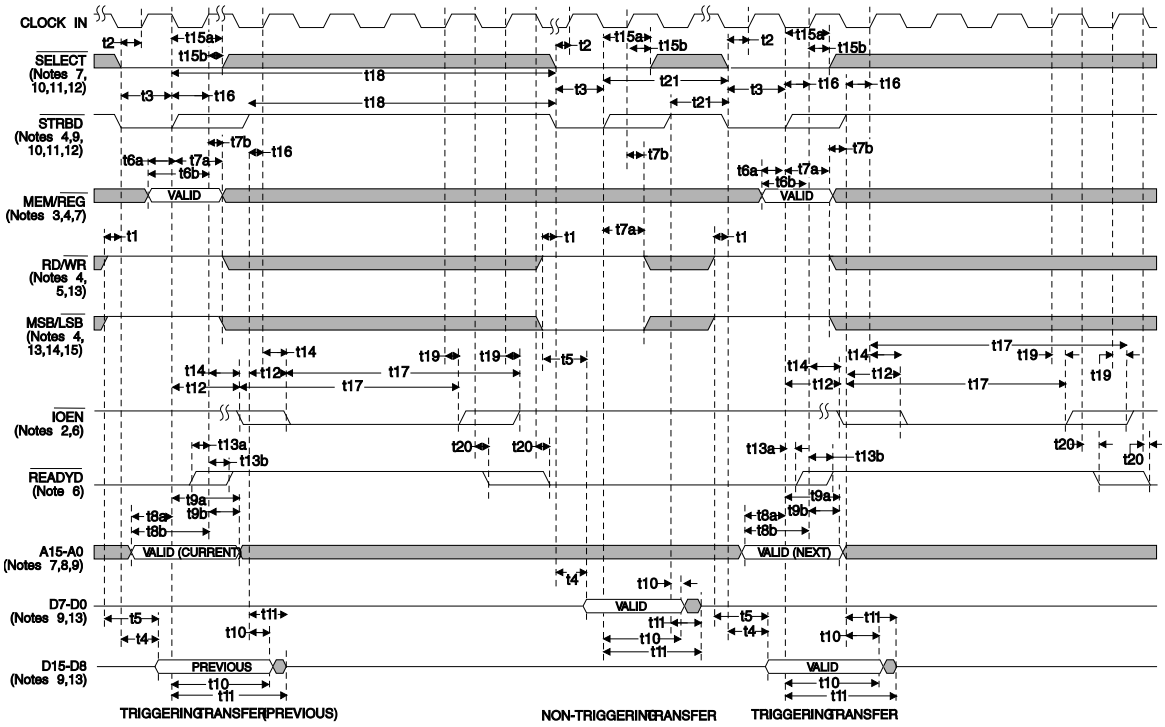


FIGURE 41. CPU READING RAM/REGISTERS (8-BIT,ZERO WAIT)

Notes for TABLE 120 and FIGURE 41:

1. For 8 bit non-zero wait interface, TRANSPARENT/BUFFERED*, ZERO_WAIT* and DTREQ*/16/8* must be connected to logic "0".
2. IOEN* goes low on the first rising CLK edge when READYD* is high and STRBD* is sampled high (satisfying t16 setup time) and the ACE's protocol/memory management logic is not accessing the internal RAM. When this occurs, IOEN* goes low, starting the internal transfer.
3. MEM/REG* must be presented high for memory access, low for register access.
4. MEM/REG*, MSB/LSB*, and RD/WR* are buffered transparently until latched by STRBD* rising or second rising CLK edge.
5. RD/WR* must be presented high for read accesses and low for write accesses. The logic sense for RD/WR* does not depend on the state of the POLARITY_SEL input in the 8-bit mode.
6. The timing for IOEN* and READYD* outputs assumes a 50 pf load. For loading above 50 pf, the validity of IOEN* and READYD* is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.1
7. Timing for A15-A0, MEM/REG*, MSB/LSB*, and SELECT* assumes ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A11 through A0 (A13-A0 for BU-61585,61586,61582 (63825), and 61583 (63925) and A15-A0 for 61688 and 61689). Registers are accessed by A4 through A0.
9. The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until latched be STRBD* rising or second CLK edge.
10. Setup time given for use in worst case timing calculations. These signals do not have to be synchronized to the system clock. Removal of SELECT* prior to being latched on the second rising clock edge will have the same effect as STRBD* rising. For ACE applications, transfer will not start until SELECT* and STRBD* are both low. For SP'ACE and SPACE II, setup time applies only to STRBD*. SELECT* must go low prior to the second rising clock edge after STRBD* goes low or transfer will be blocked.
11. For the case in which STRBD* goes high before the second rising clock edge in which SELECT* is low and STRBD* is low.
12. For the case in which STRBD* is low and SELECT* is low for a minimum of two rising clock edges.
13. Valid data will be present on the data bus only after SELECT*, STRBD*, MSB/LSB* and RD_WR* propagation delays (t3-t5) are met. For SP'ACE and SPACE II, all data will be presented on D15-D8. D7-D0 will remain in tri-state.
14. The polarity of the MSB/LSB* input signal assumes that the POLARITY_SEL input signal is connected to logic "0". If POLARITY_SEL is connected to logic "1", MSB/LSB* will be high for LSB transfers and low for MSB transfers.
15. The order of the consecutive byte transfers assumes that the TRIGGER_SEL input signal is connected to logic "0." The actual transfer to the internal RAM or Register takes place during the "triggering transfer" (MSB in this case). If TRIGGER_SEL is connected to logic "1," the order of the byte transfers would be MSB followed by LSB and the triggering transfer would be the LSB.
16. For early ACE applications, to maintain proper operation, the RD/WR* and MSB/LSB* signals must be held valid on the non-triggering transfer until STRBD* rises meeting the hold time requirements of t7A (20 ns). Not applicable for Mini-ACE series terminals.
17. For SP'ACE and SP'ACE II, in order to avoid data transfer errors for a "triggering" transfer, the "AND'd" combination of STRBD* and SELECT* must be kept at logic "1" for a minimum of 5.9 µS before both of these two signals are re-asserted to logic "0" to start the next transfer cycle. This means that at any time during this, 5.9 µS, or at least until the SP'ACE(II) READYD* output transitions from low to high and back to low, at least one of the STRBD* or SELECT* inputs must be high.

TABLE 121. CPU WRITING RAM/REGISTERS (8-BIT,ZERO WAIT)

CPU WRITING RAM OR REGISTER (SHOWN FOR 8-BIT, ZERO WAIT MODE)

REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	RD/WR* setup prior to SELECT* low and STRBD* low (Note 11)	10			10			
t2	SELECT* and STRBD* low setup time prior to CLOCK IN rising (Note 10)	10			15			ns
t3	SELECT* and STRBD* low minimum pulse width	20			20			ns
t4A	MSB/LSB* setup prior to STRBD* rising (Note 12)	20			20			ns
t4B	MSB/LSB* setup prior to CLOCK IN rising (Note 13)	20			20			ns
t5A	MSB/LSB*, RD/WR* hold timing following STRBD* rising (Note 12)	20			20			ns
t5B	MSB/LSB*, RD/WR* hold time following CLOCK IN rising (Note 13)	25			25			ns
t6A	Input Data setup prior to STRBD* rising (Note 12)	10			15			ns
t6B	Input Data setup prior to CLOCK IN rising (Note 13)	10			10			ns
t7A	Input Data hold time following STRBD* rising (Note 12)	20			20			ns
t7B	Input Data hold time following CLOCK IN rising (Note 13)	25			25			ns
t8A	SELECT* low hold time following STRBD* rising (Note 12)	0			0			ns
t8B	SELECT* low hold time following CLOCK IN rising (Note 13)	25			25			ns
t9	STRBD* rising delay to start of next transfer (SELECT* low and STRBD* low)	20			20			ns
t10	MSB/LSB* high setup prior to SELECT* low and STRBD* low (Note 16)	10			10			ns
t11A	MEM/REG* setup prior to STRBD* rising (Note 12)	10			10			ns
t11B	MEM/REG* setup prior to CLOCK IN rising (Note 13)	10			10			ns
t12A	MEM/REG*, RD/WR*, MSB/LSB* hold time following STRBD* rising (Note 12)	20			20			ns
t12B	MEM/REG*, RD/WR*, MSB/LSB* hold time following CLOCK IN rising (Note 13)	25			25			ns
t13A	Address setup prior to STRBD* rising (Note 12)	10			10			ns
t13B	Address setup prior to CLOCK IN rising (Note 13)	10			10			ns
t14A	Address hold time following STRBD* rising (Note 12)	20			20			ns
t14B	Address hold time following CLOCK IN rising (Note 13)	25			25			ns
t15	STRBD* rising delay to IOEN* falling (uncontended access @20 MHz)			107				ns
	STRBD* rising delay to IOEN* falling (contended access @20 MHz)			2.2				µs
	STRBD* rising delay to IOEN* falling (uncontended access @16 MHz)			120			115	ns
	STRBD* rising delay to IOEN* falling (contended access @16 MHz)			2.8			5.5	µs
	STRBD* rising delay to IOEN* falling (uncontended access @12 MHz)			140			135	ns
	STRBD* rising delay to IOEN* falling (contended access @12 MHz)			3.7			7.4	µs
	STRBD* rising delay to IOEN* falling (uncontended access @10 MHz)			157				ns
	STRBD* rising delay to IOEN* falling (contended access @10 MHz)			4.4				µs
t16A	STRBD* rising delay to READYD rising			30			30	ns
t16B	CLOCK IN rising delay to READYD rising			35			30	ns
t17	CLOCK IN rising delay to IOEN* falling			40			30	ns
t18	STRBD* high setup prior to CLOCK IN rising	15			20			ns
t19	IOEN* low pulse width for RAM write (@20 MHz)	185	200	215				ns
	IOEN* low pulse width for REGISTER write (@20 MHz)	185	200	215				ns
	IOEN* low pulse width for RAM write (@16 MHz)	235	250	265	485	500	515	ns
	IOEN* low pulse width for REGISTER write (@16 MHz)	235	250	265	235	250	265	ns
	IOEN* low pulse width for RAM write (@12 MHz)	315	333	350	650	666	685	ns
	IOEN* low pulse width for REGISTER write (@12 MHz)	315	333	350	315	333	350	ns
	IOEN* low pulse width for RAM write (@10 MHz)	385	400	415				ns
	IOEN* low pulse width for REGISTER write (@10 MHz)	385	400	415				ns
t21	CLOCK IN rising delay to IOEN* rising			35			30	ns
t22	CLOCK IN falling delay to READYD* falling			35			30	ns
t23	READYD* low to STRBD* and SELECT* low (Next access)	0			0			ns

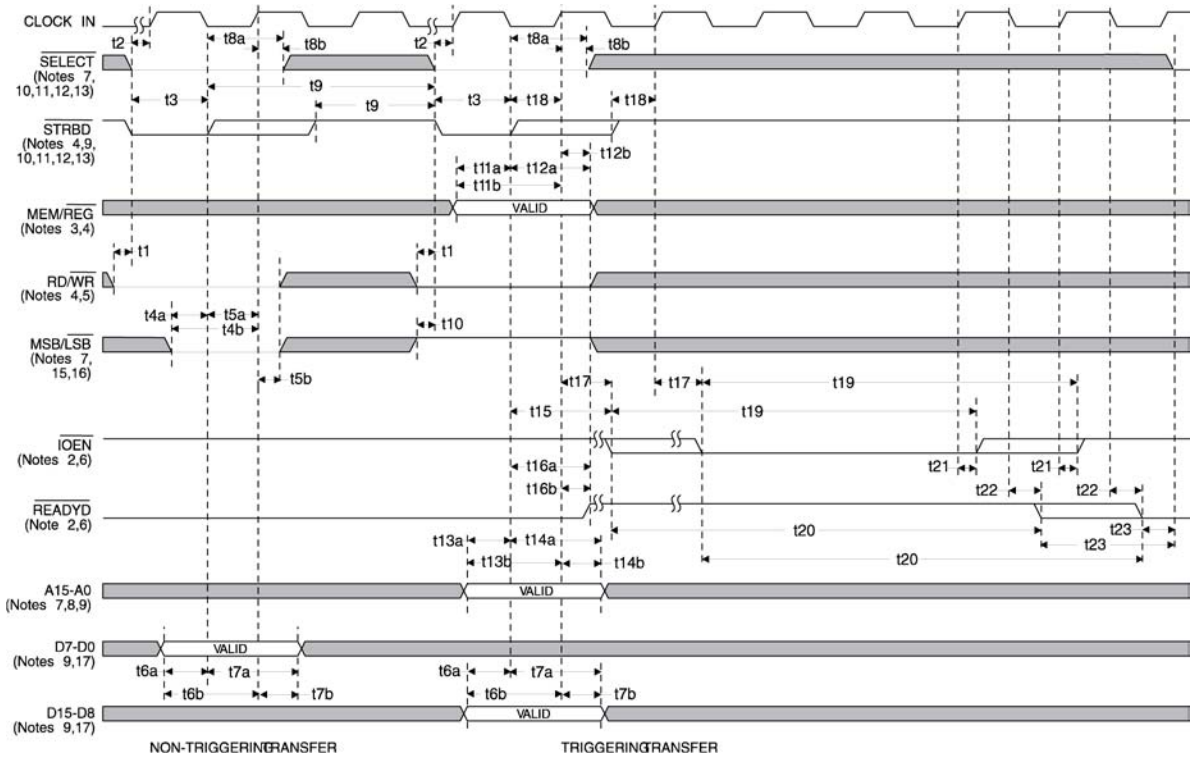


FIGURE 42. CPU WRITING RAM/REGISTERS (8-BIT,ZERO WAIT)

Notes for TABLE 121 and FIGURE 42:

1. For 8 bit zero-wait interface, TRANSPARENT/BUFFERED*, ZERO_WAIT* and DTREQ*/16/8* must be connected to logic "0".
2. IOEN* goes low on the first rising CLK edge when READYD* is high and STRBD* is sampled high (satisfying t18 setup time) and the ACE's protocol/memory management logic is not accessing the internal RAM. When this occurs, IOEN* goes low, starting the internal transfer.
3. MEM/REG* must be presented high for memory access, low for register access.
4. MEM/REG*, MSB/LSB*, and RD/WR* are buffered transparently until latched by STRBD* rising or second rising CLK edge.
5. RD/WR* must be presented high for read accesses and low for write accesses. The logic sense for RD/WR* does not depend on the state of the POLARITY_SEL input in the 8-bit mode.
6. The timing for IOEN* and READYD* outputs assumes a 50 pf load. For loading above 50 pf, the validity of IOEN* and READYD* is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/REG*, MSB/LSB* and SELECT* assumes ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A11 through A0 (A13-A0 for BU-61585,61586,61582 (63825) and 61583 (63925) and A15-A0 for 61688 and 61689). Registers are accessed by A4 through A0.
9. The address A15-A0 and data D15-D0 are internally buffered transparently until latched by STRBD* rising or the second rising clock edge.
10. Setup time given for use in worst case timing calculations. These signals do not have to be synchronized to the system clock. Removal of SELECT* effect as STRBD* are both low. For SP'ACE and SP'ACE II, setup time applies only to STRBD*. SELECT* must go low prior to the second clock rising edge after STRBD* goes low or transfer will be blocked.
11. Data Bus will be actively driven when SELECT* is low, STRBD* is low and RD/WR* is high. To prevent a bus crash between the host driving the Data Bus and the ACE driving the Data Bus, RD/WR* must be setup prior to SELECT* low and STRBD* low.
12. For the case in which STRBD* goes high before second rising clock edge in which SELECT* is low and STRBD* is low.
13. For the case in which STRBD* is low and SELECT* is low for a minimum of two rising clock edges.
14. IOEN* will be asserted low following the first rising clock edge in which STRBD* is high and the internal data bus is available.
15. The polarity of the MSB/LSB* input signal assumes that the POLARITY_SEL input signal is connected to logic "0". If POLARITY_SEL is connected to logic "1", MSB/LSB* will be high for LSB transfers and low for MSB transfers.
16. MSB/LSB* must be setup prior to SELECT* low and STRBD* low to prevent an accidental write to the internal nontriggering byte data latch.
17. For SP'ACE and SP'ACE II applications, all data must be present on D15-D8 input signals.
18. The order of the consecutive byte transfers assumes that the TRIGGER_SEL input signal is connected to logic "0". The actual transfer to internal RAM or register takes place during the "triggering transfer" (MSB in this case). If TRIGGER_SEL is connected to logic "1", the order of the byte transfers would be MSB followed by LSB and the triggering transfer would be the LSB.
19. For early ACE applications, to maintain proper operation, the RD/WR* and MSB/LSB* signals must be held valid on the non-triggering transfer until STRBD* rises meeting the hold time requirements of t7A (20 ns). Not applicable for Mini-ACE series terminals.
20. For SP'ACE and SP'ACE II, in order to avoid data transfer errors for a "triggering" transfer, the "AND'd" combination of STRBD* and SELECT* must be kept at logic "1" for a minimum of 5.9 µS before both of these two signals are re-asserted to logic "0" to start the next transfer cycle. This means that at any time during this 5.9 µS, or at least until the SP'ACE(II) READYD* output transitions from low to high and back to low, at least one of the STRBD* or SELECT* inputs must be high.

8.19 ADDRESS LATCH TIMING

FIGURE 43 and TABLE 122 illustrate the operation and timing of the address input latches for the buffered interface mode. In the transparent mode, the address buffers, and SELECT*, MEM/REG* inputs are always transparent (MSB/LSB* not applicable). Since the transparent mode requires the use of external buffers, external address latches would be required to demultiplex a multiplexed address bus. In the buffered mode however, the ACE/Mini-ACE's internal address may be used to perform the demultiplexing function.

The operation of the address latches is controlled by means of the ADDR_LAT input. When ADDR_LAT is high, the latch outputs, which drive the ACE/Mini-ACE's internal memory and control bus, transparently track the state of the address inputs A15 through A00, and the input signals SELECT*, MSB/LSB*, and MEM/REG*. When ADDR_LAT is low, the internal memory and control bus remain latched at the state of A15-A00, SELECT*, MSB/LSB*, and MEM/REG* just prior to the falling edge of ADDR_LAT.

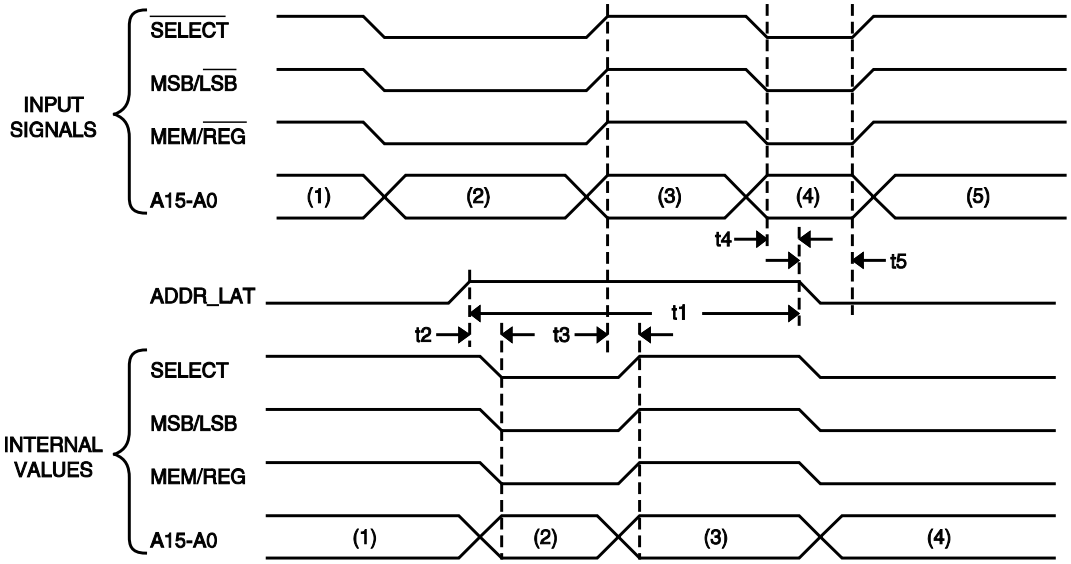


FIGURE 43. ADDRESS LATCH TIMING

TABLE 122. ADDRESS LATCH TIMING								
ADDRESS LATCH TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE AND SP'ACE II			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	ADDR_LAT pulse width	20			20			ns
t2	ADDR_LAT high delay to internal signals valid			10			10	ns
t3	Propagation delay from external input signals to internal signals valid			10			10	ns
t4	Input setup time prior to falling edge of ADDR_LAT	10			10			ns
t5	Input hold time following falling edge of ADDR_LAT	20			20			ns

Notes:
1.Applicable to buffered mode only. Address, SELECT*, and MEM/REG* latches are always transparent in the transparent mode of operation.
2.Latches are transparent when ADDR_LAT is high. Internal values do not update when ADDR_LAT is low.
3.MSB/LSB* input signal is applicable to 8-bit mode only (16/8* input = logic "0"). MSB/LSB* input is a "don't care" for 16-bit operation.

8.20 BUFFERED MEMORY INTERFACE (BU-65620)

The BU-65620 digital monolithic ACE contains two independent address/data/control buses. One of these buses, called the processor interface bus, provides a direct interface to a processor that is buffered from the internal RAM bus. This is the bus that is accessible on the BU-65170, 61580, 61585, and 61590 versions of the ACE. There is a second bus that allows more buffered RAM to be added to the system. This second bus is on the 1553 protocol side of the buffers and is isolated from the processor interface bus. This internal bus is called the Buffered RAM Interface Bus.

The buffered RAM interface bus is accessible on the BU-65620 monolithic. If no additional buffered RAM is to be added to the system, the INT_RAM_ENA* input signal should be connected to logic "0." This will cause the BU-65620 to select the internal 4K x 16 for all RAM accesses. If off-chip buffered RAM is to be used exclusively (disabling internal RAM), the INT_RAM_ENA* input signal should be connected to logic "1." Utilizing both the internal 4K x 16 and off-chip expansion RAM will require external decoding logic to operate the INT_RAM_ENA* input.

During a memory access in which the INT_RAM_ENA* input signal is connected to logic "0" (internal RAM selected), the BR_OE* signal (buffered RAM output enable) will be asserted on every read access to RAM. The BU-65620, however, will not enable the read data presented on the buffered interface bus onto its internal highway. For a write cycle, the BR_WR* signal (buffered RAM write pulse) will not be asserted unless the access is to off-chip buffered RAM access (INT_RAM_ENA* is logic "1").

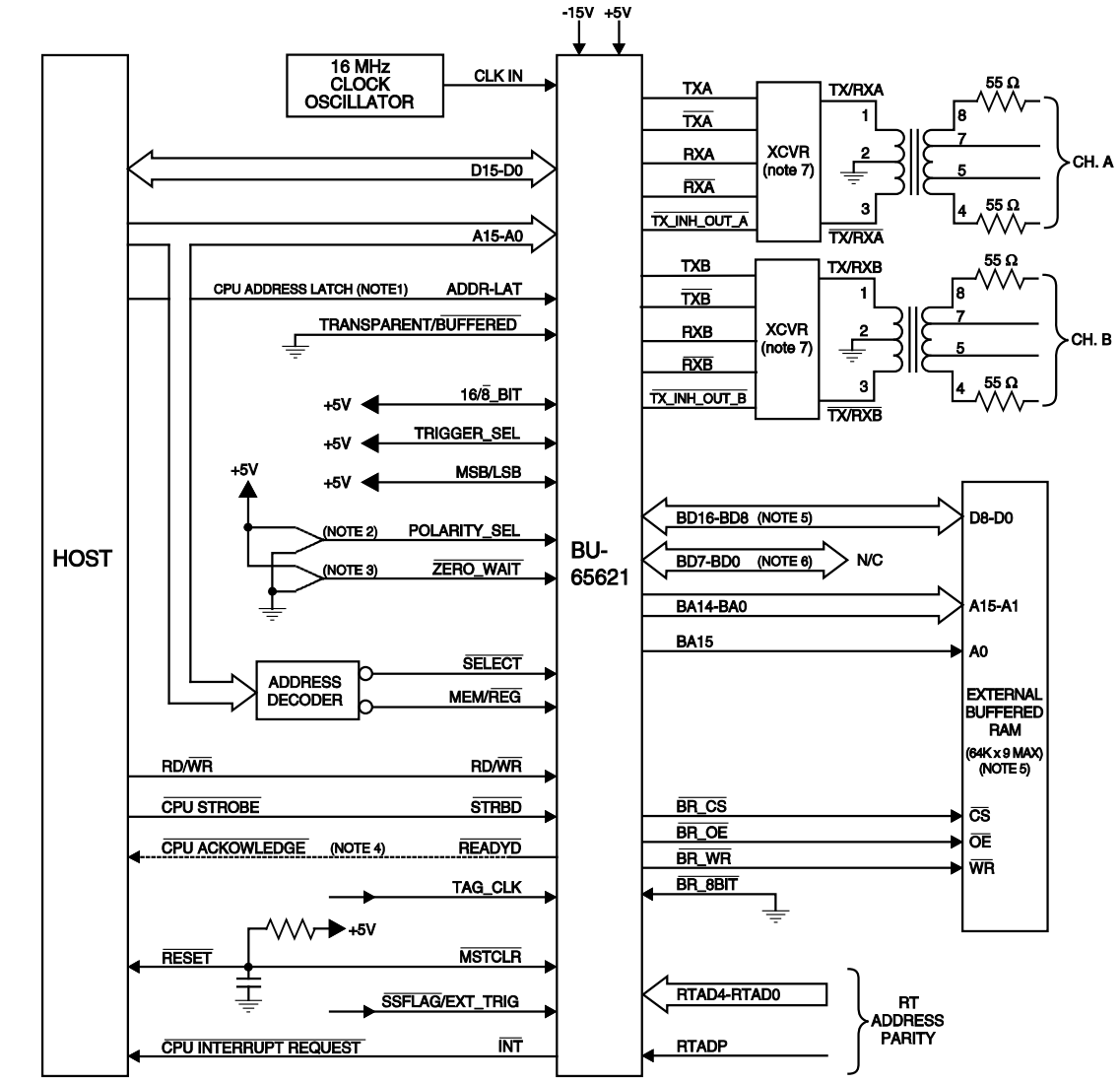
There are two possible sources/destinations for RAM data in the buffered mode and three possible sources/destinations in the transparent mode. The RAM sources are selected through the use of the MEMENA_IN* (transparent mode only) and the INT_RAM_ENA* signals. An access to an external nonbuffered (host processor bus side) RAM chip will occur, in the transparent mode, when the signal MEMENA_IN* input signal is

driven to logic "1" in response to the MEMENA_OUT* output signal. During this access cycle the state of the INT_RAM_ENA* input signal is "don't care."

An access to the buffered RAM occurs on every RAM access in the buffered mode. An access to the buffered RAM will also occur in the transparent mode during an access in which the MEMENA_IN* input signal is driven to logic "0" in response to the MEMENA_OUT* output signal being driven to logic "0." In either case, the RAM that is selected will be based on the state of the INT_RAM_ENA* input signal. If INT_RAM_ENA* is logic "0" the BU-65620's on-chip buffered RAM will be selected, while a logic "1" on the INT_RAM_ENA* signal will cause the off-chip buffered RAM to be selected.

For example, the 4K x 16 of on-chip buffered RAM may be used in conjunction with 4K x 16 of off-chip RAM to provide 8K x 16 of addressable buffered RAM. The buffered address bus (BA15-BA0) should be connected to the RAM address inputs, the buffered data bus (BD15-BD0) should be connected to the buffered RAM data bus, and the buffered RAM control outputs (BR_OE*, BR_WR*, and BR_CS*) should be connected directly to the RAM control inputs OE*, WR*, and CS*. If 17-bit wide external RAM is used to allow for parity generation and checking, BD16 should also be connected.

The selection between on-chip and off-chip RAM may be accomplished, in this configuration, with the use of the BA12 address output. Connecting BA12 directly to the INT_RAM_ENA* input signal will select the on-chip RAM for the lower 4K x 16 of the address map (locations 0000-0FFF hex), and will select (active high to select) the off-chip RAM for the upper 4K x 16 of the address map (locations 1000-1FFF hex). FIGURE 44 illustrates the interface between a host CPU, a BU-65620, and external buffered RAM. FIGURE 45 and FIGURE 46 illustrate the timing for access (both CPU and ACE) to the Buffered RAM Interface Bus.



NOTES

1. CPU ADDRESS LATCH SIGNAL PROVIDED BY PROCESSORS WITH MULTIPLEXED ADDRESS/DATA BUSES.
2. IF POLARITY_SEL = "1", RD/$\overline{WR}$ IS HIGH TO READ, LOW TO WRITE.
   IF POLARITY_SEL = "0", RD/$\overline{WR}$ IS LOW TO READ. HIGH TO WRITE.
3. $\overline{ZERO_WAIT}$ SHOULD BE STRAPPED TO LOGIC "1" FOR NON-ZERO WAIT INTERFACE AND TO LOGIC "0" FOR ZERO WAIT INTERFACE.
4. $\overline{CPU\ ACKNOWLEDGE}$ PROCESSOR INPUT ONLY FOR NON-ZERO WAIT TYPE OF INTERFACE.
5. BD16 IS ONLY REQUIRED TO BE CONNECTED IF 17-BIT WIDE EXTERNAL RAM IS USED IN 16-BIT SHARED RAM MODE ($\overline{BR_8BIT}$ CONNECTED TO LOGIC "1") OR 9-BIT WIDE RAM IS USED IN 8-BIT SHARED RAM MOD• E ($\overline{BR_8BIT}$ CONNECTED TO LOGIC "0"). ALLOWING USE OF PARITY GENERATION AND CHECKING FOR THE EXTERNAL RAM.
6. BD7-BD0 ARE ONLY USED IN 16-BIT SHARED RAM MODE ($\overline{BR_8BIT}$ CONNECTED TO LOGIC "1")
7. XCVR CAN BE ANY MIL-STD-1553 TRANSCEIVER, SUCH AS THE BUS-63125.

FIGURE 44. CPU/BU-65620/BUFFERED RAM INTERCONNECT

TABLE 123. CPU OR ACE READING BUFFERED RAM					
READ ACCESS FROM BUFFERED RAM					
REF	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1	CLOCK IN rising delay to BR_CS* falling (Note 2)			45	ns
t1A	CLOCK IN falling delay to BR_CS* falling (Note 3)			25	ns
t2	CLOCK IN rising delay to Address valid (Note 5)			65	ns
t2A	CLOCK IN rising delay to Address valid (Note 6)			5	ns
t3	BR_CS* low pulse width (@16 MHz)	188	250	265	ns
	BR_CS* low pulse width (@12 MHz)	250	333	350	ns
t4	CLOCK IN rising delay to BR_OE* low			40	ns
t5	BR_OE* low pulse width (@16 MHz)	170	187.5	205	ns
	BR_OE* low pulse width (@12 MHz)	235	250	265	ns
t6	INT_RAM_ENA* setup time prior to CLOCK IN rising	30			ns
t7	Input Data setup time prior to CLOCK IN rising	55			ns
t8	Input Data hold time following CLOCK IN rising	30			ns
t9	CLOCK IN rising to BR_CS* rising and BR_OE* rising			40	ns
t10	INT_RAM_ENA* hold time following BR_OE* rising	0			ns

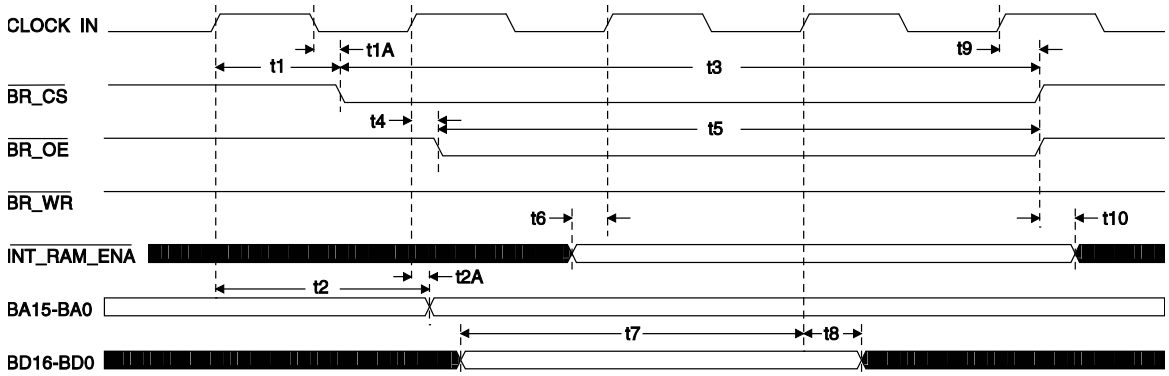


FIGURE 45. CPU OR ACE READING BUFFERED RAM

Notes for TABLE 123 and FIGURE 45:
1. Valid for CPU and 1553 accesses to RAM. Valid for all buffered mode and transparent mode transfers.
2. Applicable to all ACE transfers in 16 bit Transparent mode or ZERO WAIT Buffered Mode. Also applicable in NON-ZERO WAIT Buffered Mode where MEM/REG* is valid 10 ns after rising clock edge.
3. Applicable in NON-ZERO WAIT Buffered Mode where MEM/REG* meets the 10 ns set-up time prior to the falling edge of clock.
4. In transparent mode, transfer starts on the first rising clock-edge after DTACK* or IOEN* goes low. In buffered mode, transfer will start from the same clock edge which causes IOEN* to go low.
5. Applicable to all ACE transfers. Also applicable to all CPU transfers in which the address is setup 30 ns after the rising clock edge.
6. Applicable to CPU transfers in Transparent Mode or NON-ZERO WAIT Buffered Mode where the address meets the 30 ns set-up time prior to the rising clock edge.

TABLE 124. CPU OR ACE WRITING BUFFERED RAM					
WRITE ACCESS TO BUFFERED RAM					
REF	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1	CLOCK IN rising delay to BR_CS* falling (Note 2)			45	ns
t1A	CLOCK IN falling delay to BR_CS* falling (Note 3)			25	ns
t2	CLOCK IN rising delay to Address valid (Note 5)			65	ns
t2A	CLOCK IN rising delay to Address valid (Note 6)			5	ns
t3	BR_CS* low pulse width (@ 16 MHz)	188	250	265	ns
	BR_CS* low pulse width (@ 12 MHz)	250	333	350	ns
t4	CLOCK IN rising delay to Output Data valid			60	ns
t5	INT_RAM_ENA* setup time prior to clock rising	30			ns
t6	CLOCK IN rising to BR_WR* falling			40	ns
t7	BR_WR* low pulse width (@ 16 MHz)	50	62.5	80	ns
	BR_WR* low pulse width (@ 12 MHz)	70	83.3	95	ns
t8	INT_RAM_ENA* hold time following BR_WR* rising	20			ns
t9	CLOCK IN rising to BR_CS* rising			40	ns
t10	Output Data hold time following CLOCK IN rising	0			ns
t11	CLOCK IN rising to Output Data tri-state			45	ns

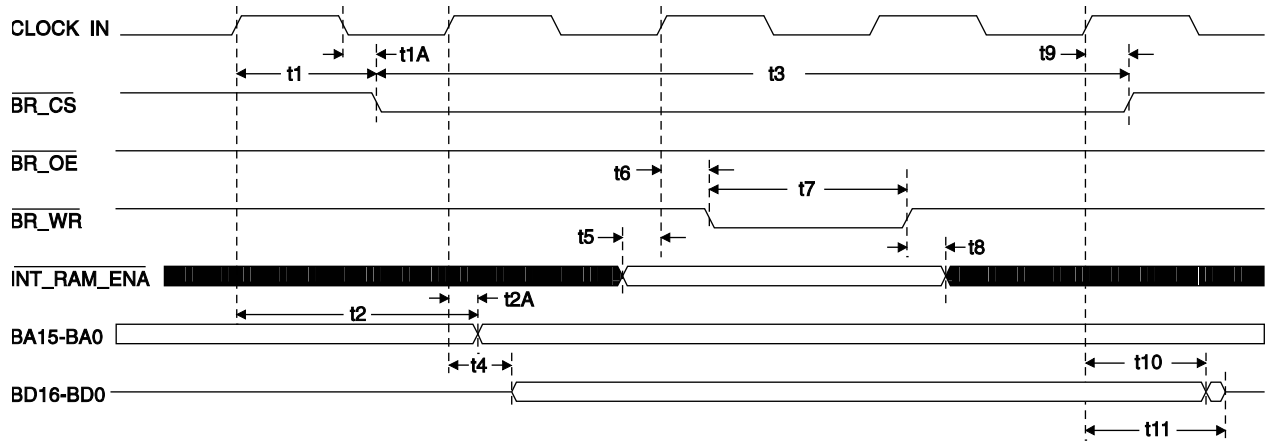


FIGURE 46. CPU OR ACE WRITING BUFFERED RAM

Notes for TABLE 124 and FIGURE 46:
1. Valid for CPU and 1553 accesses to RAM. Valid for all buffered mode and transparent mode transfers.
2. Applicable to all ACE transfers in 16 bit Transparent mode or ZERO WAIT Buffered Mode. Also applicable in NON-ZERO WAIT Buffered Mode where MEM/REG* is valid 10 ns after rising clock edge.
3. Applicable in NON-ZERO WAIT Buffered Mode where MEM/REG* meets the 10 ns set-up time prior to the falling edge of clock.
4. In transparent mode, transfer starts on the first rising clock-edge after DTACK* or IOEN* goes low. In buffered mode, transfer will start from the same clock edge which causes IOEN* to go low.
5. Applicable to all ACE transfers. Also applicable to all CPU transfers in which the address is setup 30 ns after the rising clock edge.
6. Applicable to CPU transfers in Transparent Mode or NON-ZERO WAIT Buffered Mode where the address meets the 30 ns set-up time prior to the rising clock edge.

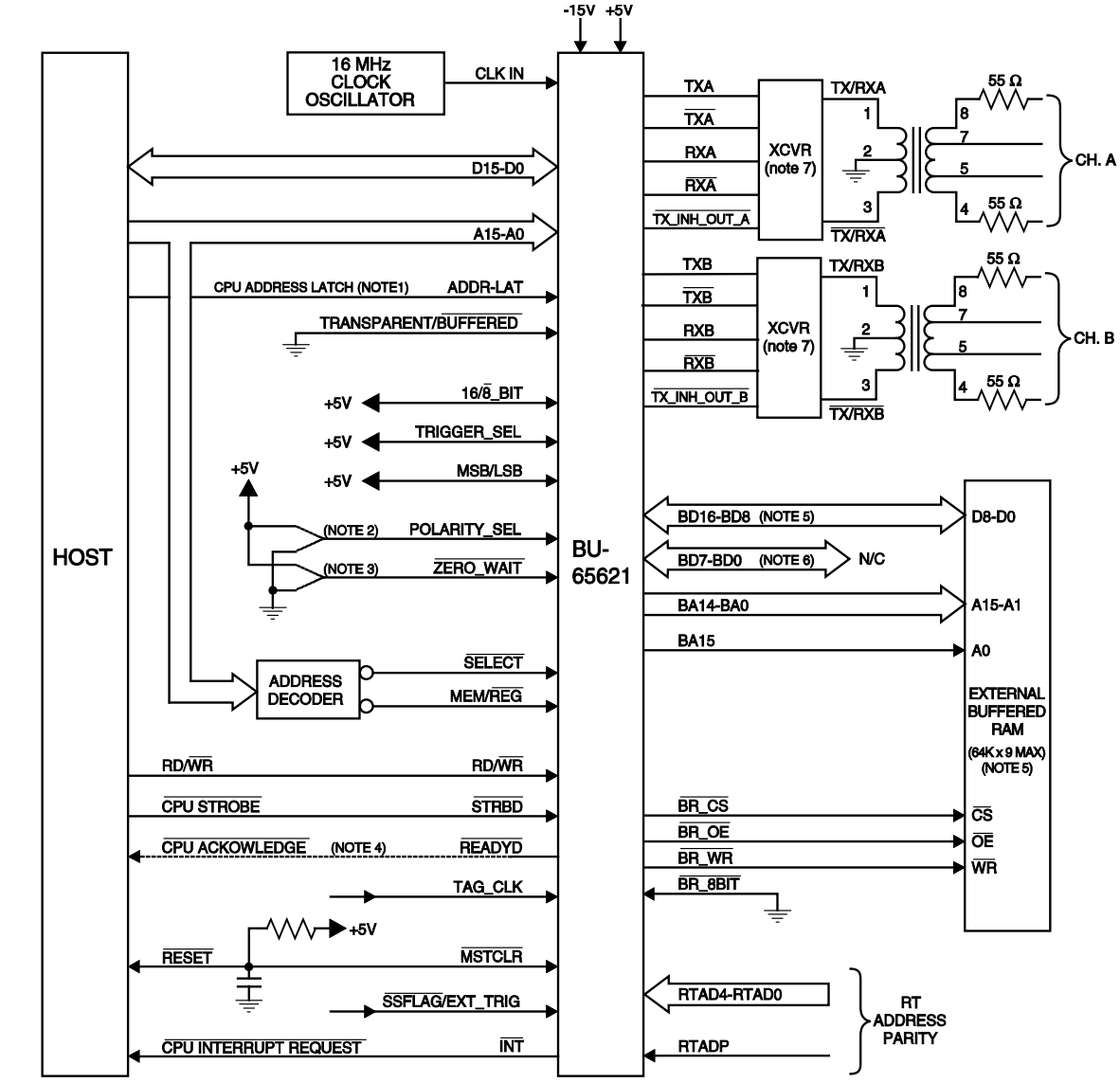
8.21 BUFFERED MEMORY INTERFACE (BU-65621)

The BU-65621 digital monolithic SP’ACE contains two independent address/data/control buses. One of these buses, called the processor interface bus, provides a direct interface to a processor that is buffered from the RAM bus. The processor interface bus is what is accessible on the BU-61582 (BU-63825), and 61583 (63925) versions of the SP'ACE and SP’ACE II. There is a second bus, which provides the interface to the buffered RAM. This second bus is on the 1553 protocol side of the buffers and is isolated from the processor interface bus. This internal bus is called the Buffered RAM Interface Bus.

An access to the buffered RAM occurs on every RAM access in the buffered mode. An access to the buffered RAM will also occur in the transparent mode during an access in which the MEMENA_IN* input signal is driven to logic "0" in response to the MEMENA_OUT* output signal being driven to logic "0."

The BU-65621 provides the option of interfacing to either a 16-bit or an 8-bit wide buffered RAM. The internal architecture of the BU-65621 is based on a 16-bit interface. When the 8-bit shared RAM option is enabled (BR_8BIT* connected to logic 0) all RAM accesses (both CPU transfers and internal 1553 transfers) will consist of two 8 bit accesses to the buffered RAM. In the 8-bit shared RAM mode buffered RAM address bit 15 (BR15) becomes an MSB/LSB address line. Hence, the maximum addressable RAM available to a CPU in the 8-bit shared RAM mode is 32K x 16. Buffered RAM Data bits 7 through 0 (BD7-BD0) are not used. Both upper and lower byte transfers are multiplexed through data lines BD15 through BD8.

FIGURE 47 illustrates the interface between a host CPU, a BU-65621, and external buffered RAM. FIGURE 48 and FIGURE 49 illustrate the timing for access (both CPU and ACE) to the Buffered RAM Interface Bus.



NOTES

1. CPU ADDRESS LATCH SIGNAL PROVIDED BY PROCESSORS WITH MULTIPLEXED ADDRESS/DATA BUSES.
2. IF POLARITY_SEL = "1", RD/$\overline{WR}$ IS HIGH TO READ, LOW TO WRITE.
   IF POLARITY_SEL = "0", RD/$\overline{WR}$ IS LOW TO READ. HIGH TO WRITE.
3. $\overline{ZERO_WAIT}$ SHOULD BE STRAPPED TO LOGIC "1" FOR NON-ZERO WAIT INTERFACE AND TO LOGIC "0" FOR ZERO WAIT INTERFACE.
4. $\overline{CPU\ ACKNOWLEDGE}$ PROCESSOR INPUT ONLY FOR NON-ZERO WAIT TYPE OF INTERFACE.
5. BD16 IS ONLY REQUIRED TO BE CONNECTED IF 17-BIT WIDE EXTERNAL RAM IS USED IN 16-BIT SHARED RAM MODE ($\overline{BR_8BIT}$ CONNECTED TO LOGIC "1") OR 9-BIT WIDE RAM IS USED IN 8-BIT SHARED RAM MOD• E ($\overline{BR_8BIT}$ CONNECTED TO LOGIC "0"). ALLOWING USE OF PARITY GENERATION AND CHECKING FOR THE EXTERNAL RAM.
6. BD7-BD0 ARE ONLY USED IN 16-BIT SHARED RAM MODE ($\overline{BR_8BIT}$ CONNECTED TO LOGIC "1")
7. XCVR CAN BE ANY MIL-STD-1553 TRANSCEIVER, SUCH AS THE BUS-63125.

FIGURE 47. CPU/BU-65621/BUFFERED RAM INTERCONNECT

TABLE 125. CPU OR SP'ACE and SP'ACE II READING BUFFERED RAM					
READ ACCESS FROM BUFFERED RAM					
REF	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	CLOCK IN rising delay to BR_CS* falling (Note 2)			30	ns
t1A	CLOCK IN falling delay to BR_CS* falling (Note 3)			15	ns
t2	CLOCK IN rising delay to Address valid (Note 6)			35	ns
t2A	CLOCK IN rising delay to Address valid (Note 7)			10	ns
t3	BR_CS* low pulse width (@16 MHz) (Note 5)	440	500	515	ns
t3	BR_CS* low pulse width (@12 MHz) (Note 5)	590	666	680	ns
t4	CLOCK IN rising delay to BR_OE* low			30	ns
t5	BR_OE* low pulse width (@ 16 MHz)	175	187.5	205	ns
t5	BR_OE* low pulse width (@ 12 MHz)	235	250	265	ns
t7	Input Data setup time prior to CLOCK IN rising	40			ns
t8	Input Data hold time following CLOCK IN rising	25			ns
t9	CLOCK IN rising to BR_CS* rising and BR_OE* rising			30	ns

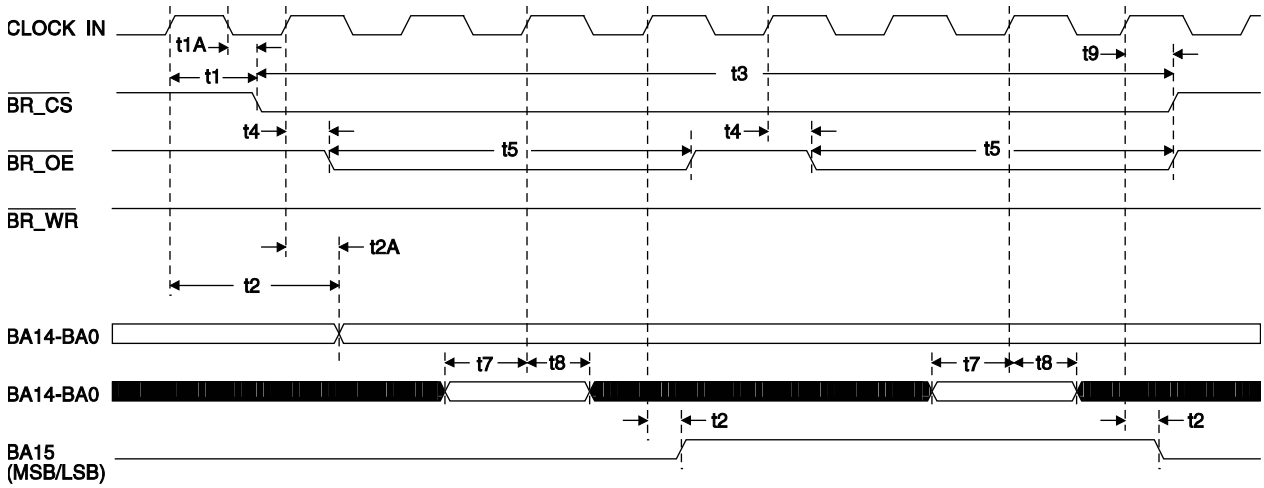


FIGURE 48. CPU OR SP'ACE/ SP'ACE II READING BUFFERED RAM

Notes for TABLE 125 and FIGURE 48:

1. Valid for CPU and 1553 accesses to RAM. Valid for all buffered mode and transparent mode transfers.
2. Applicable to all SP'ACE and SP'ACE II transfers and CPU transfers in 16 bit Transparent mode or ZERO WAIT Buffered Mode. Also applicable in NON-ZERO WAIT Buffered Mode. Also applicable in NON-ZERO WAIT Buffered Mode where MEM/REG* is valid 10 ns. after the rising clock edge.
3. Applicable in NON-ZERO WAIT Buffered Mode where MEM/REG* meets the 10 ns set-up time prior to the falling edge of clock.
4. In transparent mode, transfer starts on the first rising clock-edge after DTACK* or IOEN* goes low. In buffered mode, transfer will start from the same clock edge which causes IOEN* to go low.
5. Figure shows access to 8 bit buffered RAM. If operating in Transparent mode and external memory was selected (MEMIN* = 1) or configured with 16 bit buffered RAM (BU-65621) then second half of transfer would not occur. That is, BR_CS* would be 4 clock cycles instead of 8 and there would only be one BR_OE* pulse.
6. Applicable to all SP'ACE and SP'ACE II transfers. Also applicable to all CPU transfers in which the address is setup 15 ns after the rising clock edge.
7. Applicable to CPU transfers in Transparent Mode or NON-ZERO WAIT Buffered Mode where the address meets the 10 ns setup time prior to the rising clock edge.
8. If 8 bit buffered RAM was selected, all data would be entered on BD16 thru BD08. BD07-BD00 is a don't care.

TABLE 126. CPU OR SP'ACE and SP'ACE II WRITING BUFFERED RAM					
WRITE ACCESS TO BUFFERED RAM					
REF	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1	CLOCK IN rising delay to BR_CS* falling (Note 2)			30	ns
t1A	CLOCK IN falling delay to BR_CS* falling (Note 3)			15	ns
t2	CLOCK IN rising delay to Address valid (Note 6)			35	ns
t2A	CLOCK IN rising delay to Address valid (Note 7)			10	ns
t3	BR_CS* low pulse width (@16 MHz) (Note 5)	440	500	515	ns
t3	BR_CS* low pulse width (@12 MHz) (Note 5)	590	666	680	ns
t4	CLOCK IN rising delay to Output Data valid			40	ns
t6	CLOCK IN rising to BR_WR* falling			30	ns
t7	BR_WR* low pulse width (@16 MHz)	55	62.5	70	ns
t7	BR_WR* low pulse width (@12 MHz)	75	83.3	90	ns
t8	CLOCK IN rising delay to BR_WR* rising			30	ns
t9	CLOCK IN rising to BR_CS* rising			30	ns
t10	Output Data hold time following CLOCK IN rising	0			ns
t11	CLOCK IN rising to Output Data tri-state			35	ns

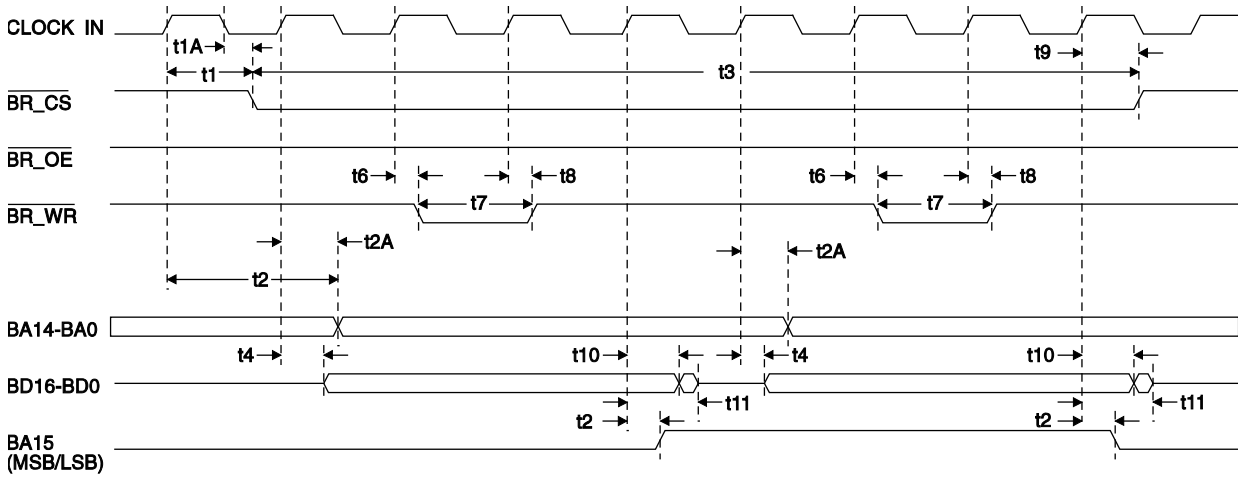


FIGURE 49. CPU OR SP'ACE/ SP'ACE II WRITING BUFFERED RAM

Notes for TABLE 126 and FIGURE 49:

1. Valid for CPU and 1553 accesses to RAM. Valid for all buffered mode and transparent mode transfers.
2. Applicable to all SP'ACE and SP'ACE II transfers and CPU transfers in 16 bit Transparent mode or ZERO WAIT Buffered Mode. Also applicable in NON-ZERO WAIT Buffered Mode where MEM/REG* is valid 10 ns after the rising clock edge.
3. Applicable in NON-ZERO WAIT Buffered Mode where MEM/REG* meets the 10 ns setup time prior to the falling edge of clock.
4. In transparent mode, transfer starts on the first rising clock-edge after DTACK* or IOEN* goes low. In buffered mode, transfer will start from the same clock edge which causes IOEN* to go low.
5. FIGURE shows access to 8 bit buffered RAM. If operating in Transparent mode and external memory was selected (MEMIN* = 1) or configured with 16 bit buffered RAM (BU-65621) then second half of transfer would not occur. That is, BR_CS* would be 4 clock cycles instead of 8 and there would only be one BR_WR* pulse if operating in 16 bit RAM mode and no pulse if external RAM was selected.
6. Applicable to all SP'ACE and SP'ACE II transfers. Also applicable to all CPU transfers in which the address is setup 15 ns after the rising clock edge.
7. Applicable to CPU transfers in Transparent Mode or NON-ZERO WAIT Buffered mode where the address meets the 10 ns setup time prior to the rising clock edge.
8. If 8 bit buffered RAM was selected, all data would be on BD16 thru BD08. BD07-BD00 would remain tri-state.

8.22 CLOCK INPUT CONSIDERATIONS

8.22.1 Input Frequency

The ACE may be operated from either a 12 MHz or 16 MHz clock input. In the default (power turn-on) state, the ACE assumes a 16 MHz clock input. In order to operate the ACE with a 12 MHz clock input, the ACE must be programmed for ENHANCED MODE (bit 15 of Configuration Register #1 programmed to logic "1") and 12 MHZ CLOCK SELECT (10 MHZ CLOCK SELECT for BU-61689), bit 15 of Configuration Register #5, must be programmed to logic "1." In addition, for the BU-65620 digital monolithic ACE, the input signals ENHANCED_MODE_ENABLE* (pin A08) and CLK_SEL* (pin B08) must be hardwired to logic "0" to enable operation from a 12 MHz clock.

The Mini-ACE Series additionally adds 10 MHz and 20 MHz operation capability based on the specific model purchased. The BU-61688 Mini-ACE Plus operates at either 12MHz or 16MHz as described above for the ACE series terminals. The BU-61689 Mini-ACE Plus operates at either 10 MHz or 20 MHz. In the default (power turn-on) state, the BU-61689 Mini-ACE Plus assumes a 20 MHz clock input. In order to operate the BU-61689 Mini-ACE Plus with a 10 MHz clock input, the BU-61689 must be programmed for ENHANCED MODE (bit 15 of Configuration Register #1 programmed to logic "1") and 12 MHZ CLOCK SELECT, bit 15 of Configuration Register #5, must be programmed to logic "1."

8.22.2 Single Edge or Double Edge Sampling

The ACE/Mini-ACE Manchester decoders operate by oversampling the digital input signal(s) from the 1553 (double-ended) or fiberoptic (single-ended) receivers. The decoders may be programmed to sample either on every rising edge of the CLK_IN input clock, or on every edge (both rising and falling) of CLK_IN. For the Mini-ACE series, the decoders always sample on both the rising and falling clock edges. In the default (power turn-on) state, the ACE samples off the rising edges only. In order for the ACE decoders to sample off both edges of CLK_IN, ACE must be programmed for ENHANCED MODE (bit 15 of Configuration Register #1 programmed to logic "1") and EXPANDED CROSSING ENABLED, bit 11 of Configuration Register #5, must be programmed to logic "1" (Note: For the Mini-ACE series, this register bit is obsolete). In addition, for the BU-65620 digital monolithic ACE, the input signal ENHANCED_MODE_ENABLE* (pin A08) must be hardwired to logic "0" in order to enable decoder sampling on both edges of CLK_IN.

If EXPANDED ZERO CROSSING is not enabled for an ACE series hybrid or monolithic, the decoders sample using a single rising edge rising of the CLOCK input. That is, the decoder sampling frequency is

either 16 or 12 MHz. If EXPANDED ZERO CROSSING is programmed to logic "1," the decoders sample using both edges of the clock-in input. In this case, the decoder sampling frequency doubles to either 24 or 32 MHz. The higher sampling frequency provides improved tolerance (about 30 to 40 ns) for input zero crossing distortion. It should be noted, however, that if the expanded zero-crossing option is used, a tighter tolerance is required for the ACE's CLK_IN input. The required duty cycle range for the CLK_IN input is approximately 33% to 67% if the expanded zero-crossing option is not used. If EXPANDED ZERO CROSSING IS USED, the requirement for clock duty cycle tightens to approximately 40% to 60%.

Note: It is strongly recommended that Expanded Crossing be enabled for 16 and 12 MHz operation when using an ACE series hybrid.

8.23 SAMPLE INTERFACES

8.23.1 Intel 8051

FIGURE 50 illustrates a simplified interface drawing between an Intel 8051 and an ACE/Mini-ACE. This interface is based on the ACE/Mini-ACE's 8-bit buffered, zero wait interface. The 4K words (8K bytes) of ACE/Mini-ACE internal RAM, map to Address range BMA (0000-1FFF), where BMA = Base Memory Address. The 16 register locations (32 bytes) of the BU-65170/61580 map to address range BRA (0000-001F), where BRA = Base Register Address. SELECT* must be asserted low to access either RAM or register. MEM/REG* must be asserted high to access RAM, low to access registers.

Write accesses are performed as follows:

1) Write lower data byte, with P0.0 (MSB/LSB*) = 0.

2) Write upper data byte, with P0.0 (MSB/LSB*) = 1.

3) If additional write cycles are to be performed, wait the minimum time, then return to step 1. The minimum times are listed in TABLE 127.

Read accesses are performed as follows:

1) Perform a "dummy" read access to the upper data byte address (P0.0 (MSB/LSB*) = 1). Do not use the data byte accessed from this operation.

2) After waiting the minimum time (see TABLE 127), read the lower data byte, with P0.0 (MSB/LSB*) = 0.

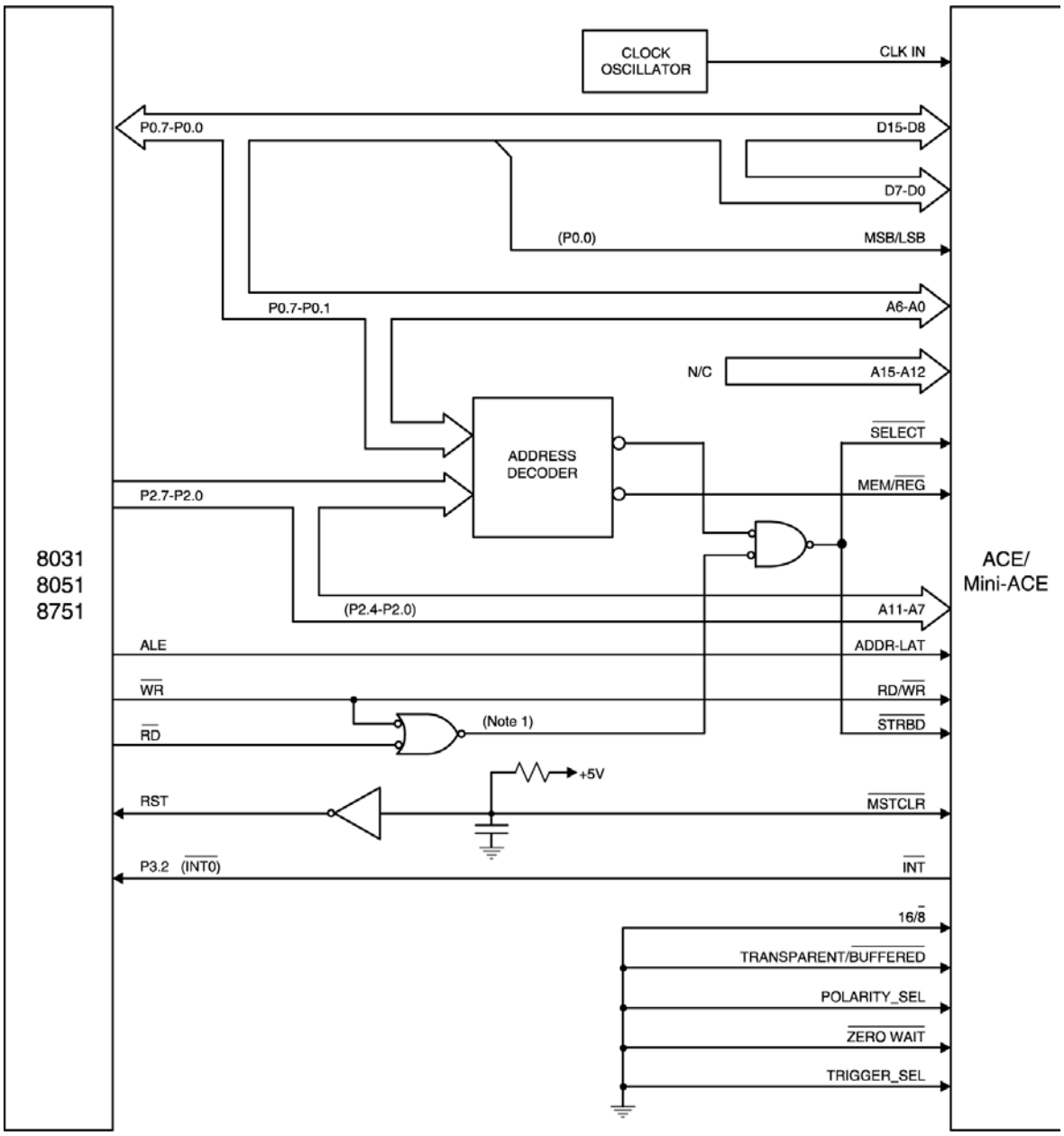
3) While presenting the Address for the next word to be accessed (if any), read the upper byte, with P0.0 (MSB/LSB*) = 1.

4) If there is a subsequent word to be read, repeat steps 2 and 3.

TABLE 127. MINIMUM REQUIRED DELAY TIMES

MODE	ACE/MINI-ACE				SP'ACE							
	@ 20MHZ	@ 16MHZ	@ 12MHZ	@ 10MHZ	16-BIT SHARED RAM MODE (NOTE)				8-BIT SHARED RAM MODE (NOTE)			
					@ 20MHZ	@ 16MHZ	@ 12MHZ	@ 10MHZ	@ 20MHZ	@ 16MHZ	@ 12MHZ	@ 10MHZ
Bus Controller (BC)	1.9 µs	2.4 µs	3.1 µs	3.8 µs	1.9 µs	2.4 µs	3.1 µs	3.8 µs	3.5 µs	4.4 µs	5.8 µs	7.0 µs
Remote Terminal (RT)	2.5 µs	3.1 µs	4.1 µs	4.9 µs	2.5 µs	3.1 µs	4.1 µs	4.9 µs	4.7 µs	5.9 µs	7.8 µs	9.4 µs
Word Monitor	0.9 µs	1.1 µs	1.5 µs	1.8 µs	0.9 µs	1.1 µs	1.5 µs	1.8 µs	1.5 µs	1.9 µs	2.5 µs	3.0 µs
Selective Message Monitor	2.1 µs	2.6 µs	3.5 µs	4.2 µs	2.1 µs	2.6 µs	3.5 µs	4.2 µs	3.9 µs	4.9 µs	6.5 µs	7.8 µs

Note: 8 and 16 BIT Shared RAM mode is an option available on the SP'ACE and SP'ACE II series of components. The mode is selected through the use of the BR_8BIT input signal. This input signal is hardwired for 8-bit mode for the BU-61582 (BU-63825) and BU-61583 (BU-63925).

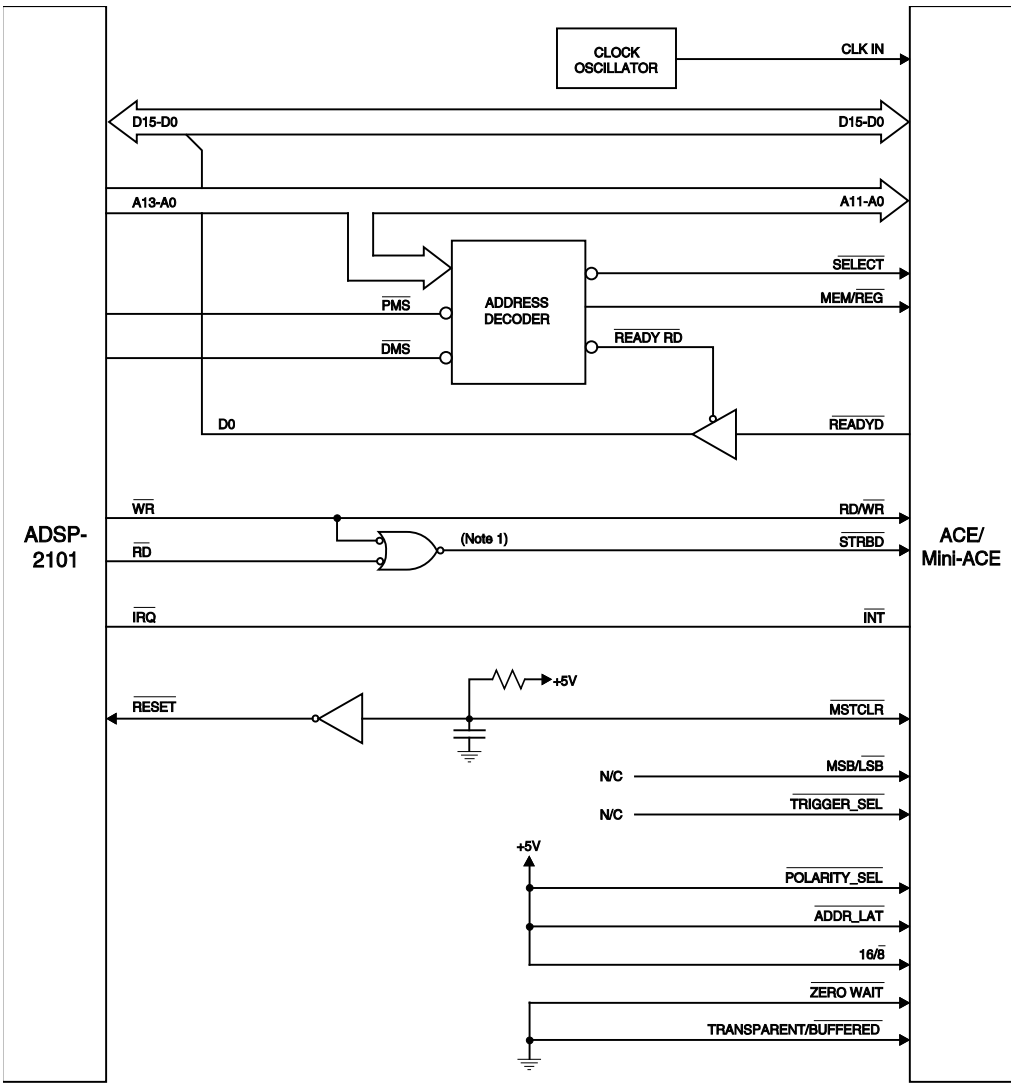


Note:
1. Select a gate such that the RD/WR* setup time prior to SELECT* and STRBD* low is satisfied.

FIGURE 50. INTEL 8051-TO-ACE INTERFACE

8.23.2 ADSP-2101

FIGURE 51 illustrates a simplified interface drawing between an Analog Devices ADSP-2101 and an ACE/Mini-ACE. This interface takes advantage of the ACE/Mini-ACE's 16-bit zero wait mode since the 2101 does not have an acknowledge handshake input. A restriction of the zero wait mode is that the processor may not begin a new transfer until the previous is complete. Therefore, the READYD* output may optionally be read by the processor on the LSB of the data bus as a method of polling the ACE to determine when the transfer is complete.



Notes:
1. Select a gate such that the RD/WR* setup time prior to SELECT* and STRBD* low is satisfied.

FIGURE 51. ADSP-2101-TO-ACE INTERFACE

8.23.3 Motorola 68040

FIGURE 52 illustrates a simplified interface drawing between a 68040 and an ACE/Mini-ACE.

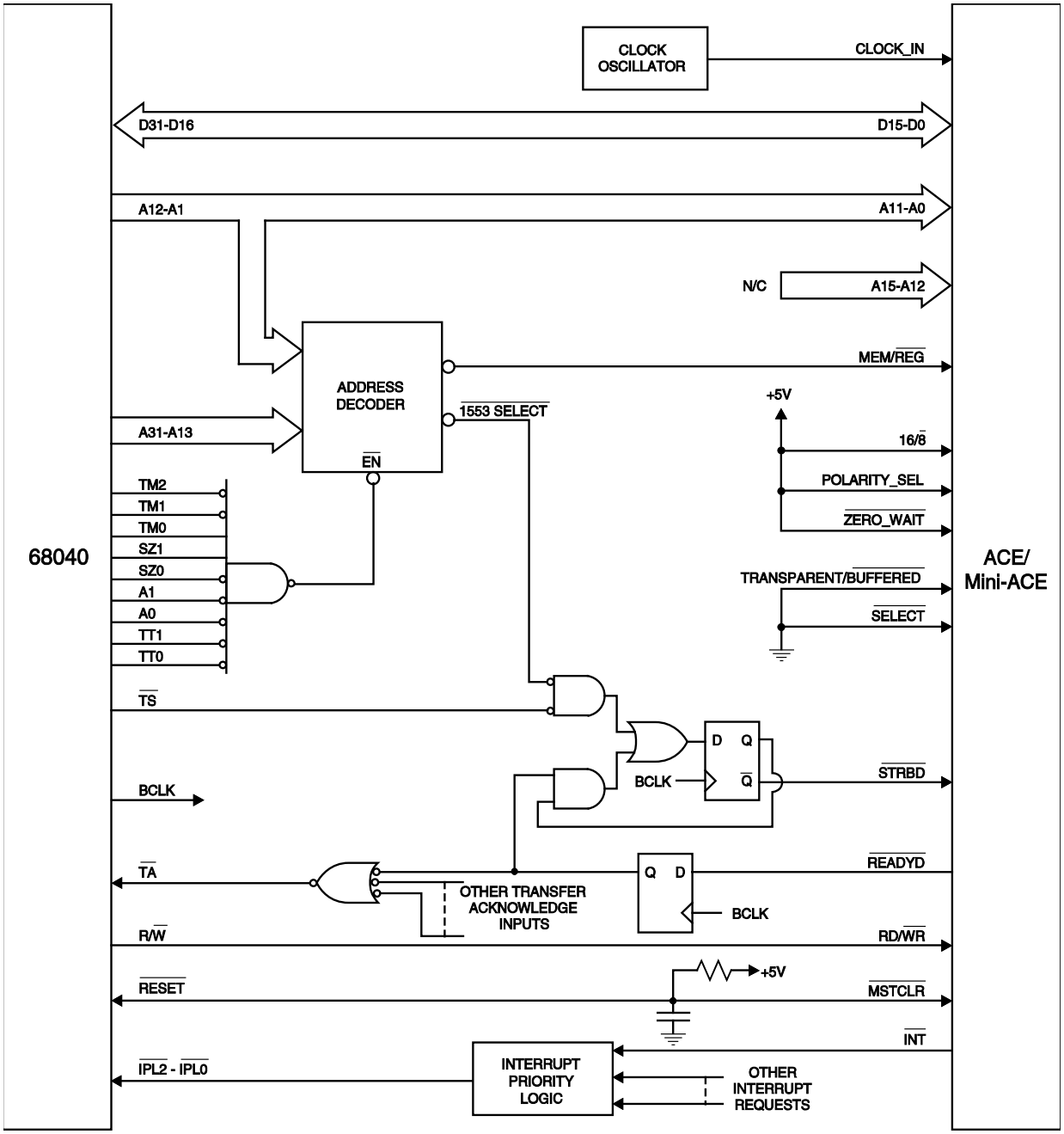


FIGURE 52. 68040-TO-ACE INTERFACE

8.23.4 Motorola 68020

FIGURE 53 illustrates a simplified interface drawing between a 68020 and an ACE/Mini-ACE.

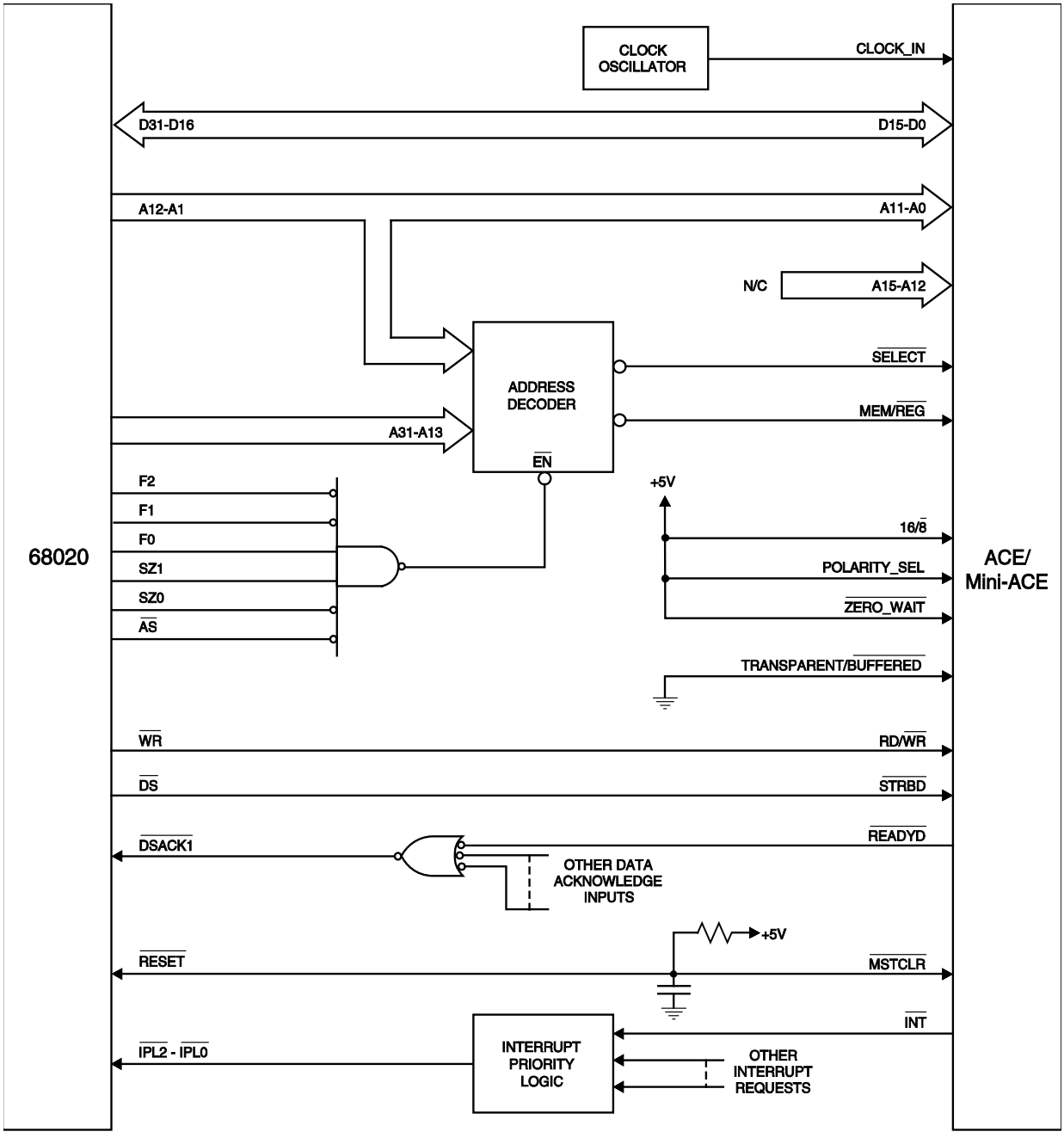


FIGURE 53. 68020-TO-ACE INTERFACE

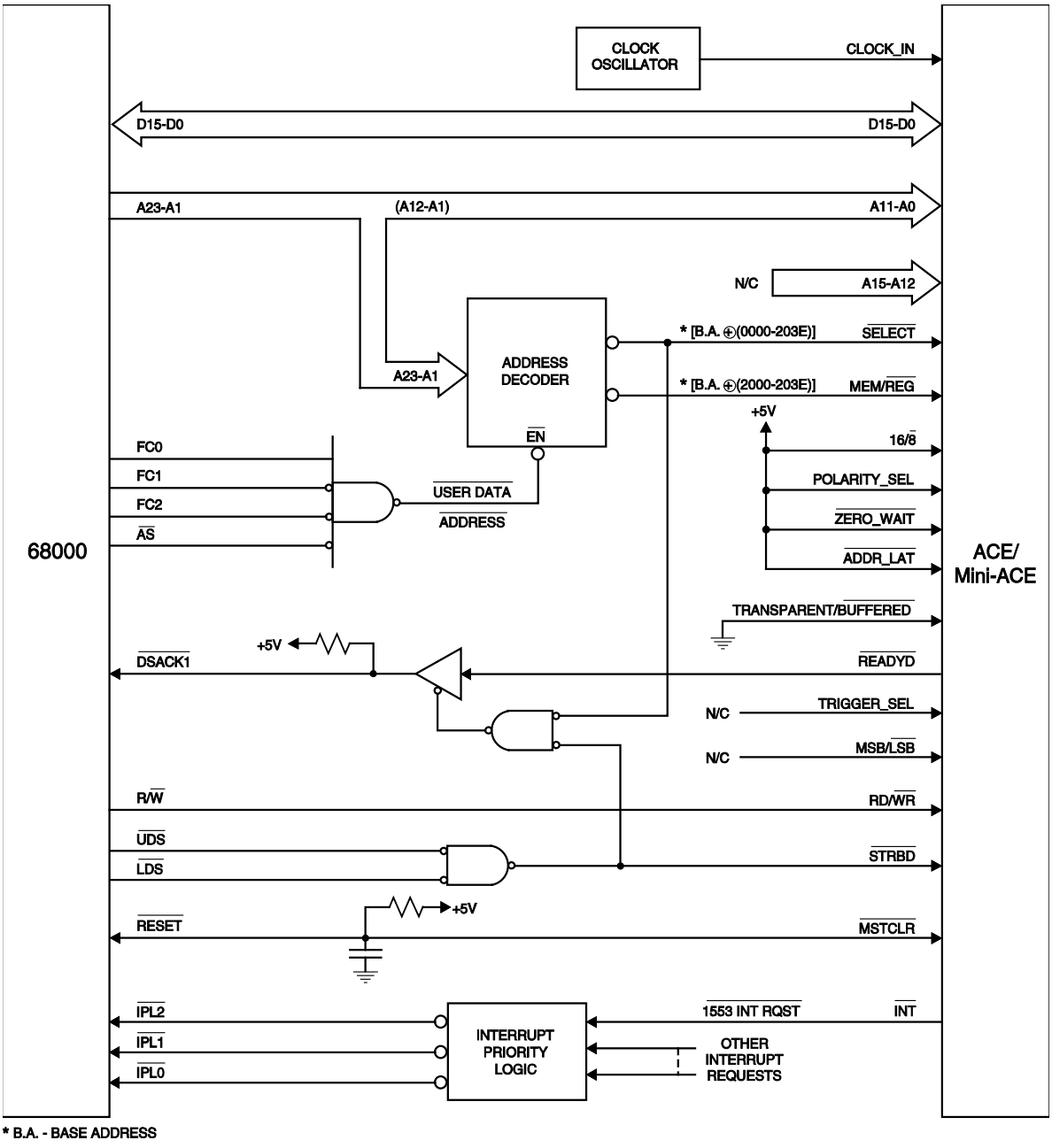


FIGURE 54. MOTOROLA 68000-TO-ACE INTERFACE

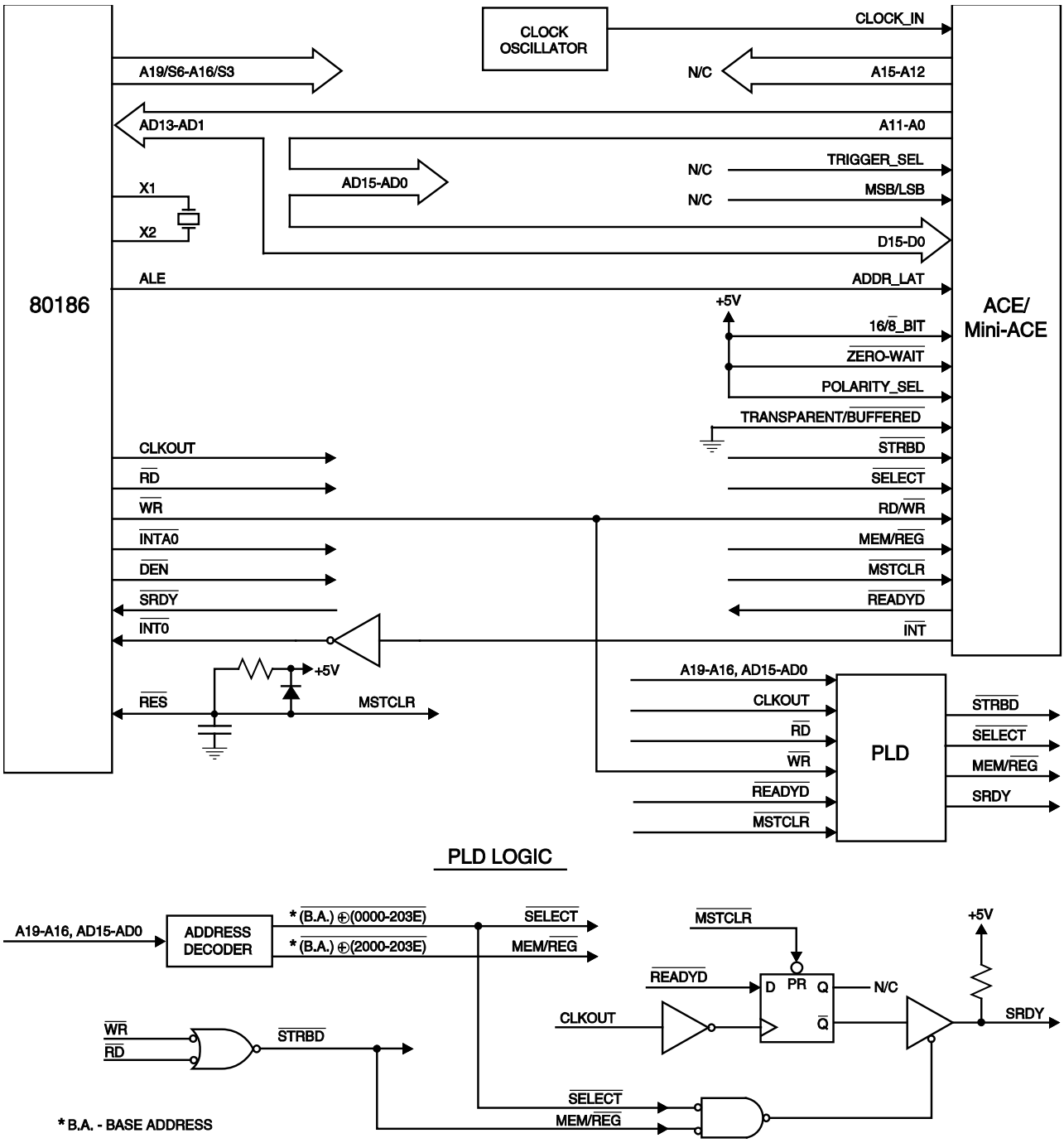


FIGURE 55. INTEL 80186-TO-ACE INTERFACE

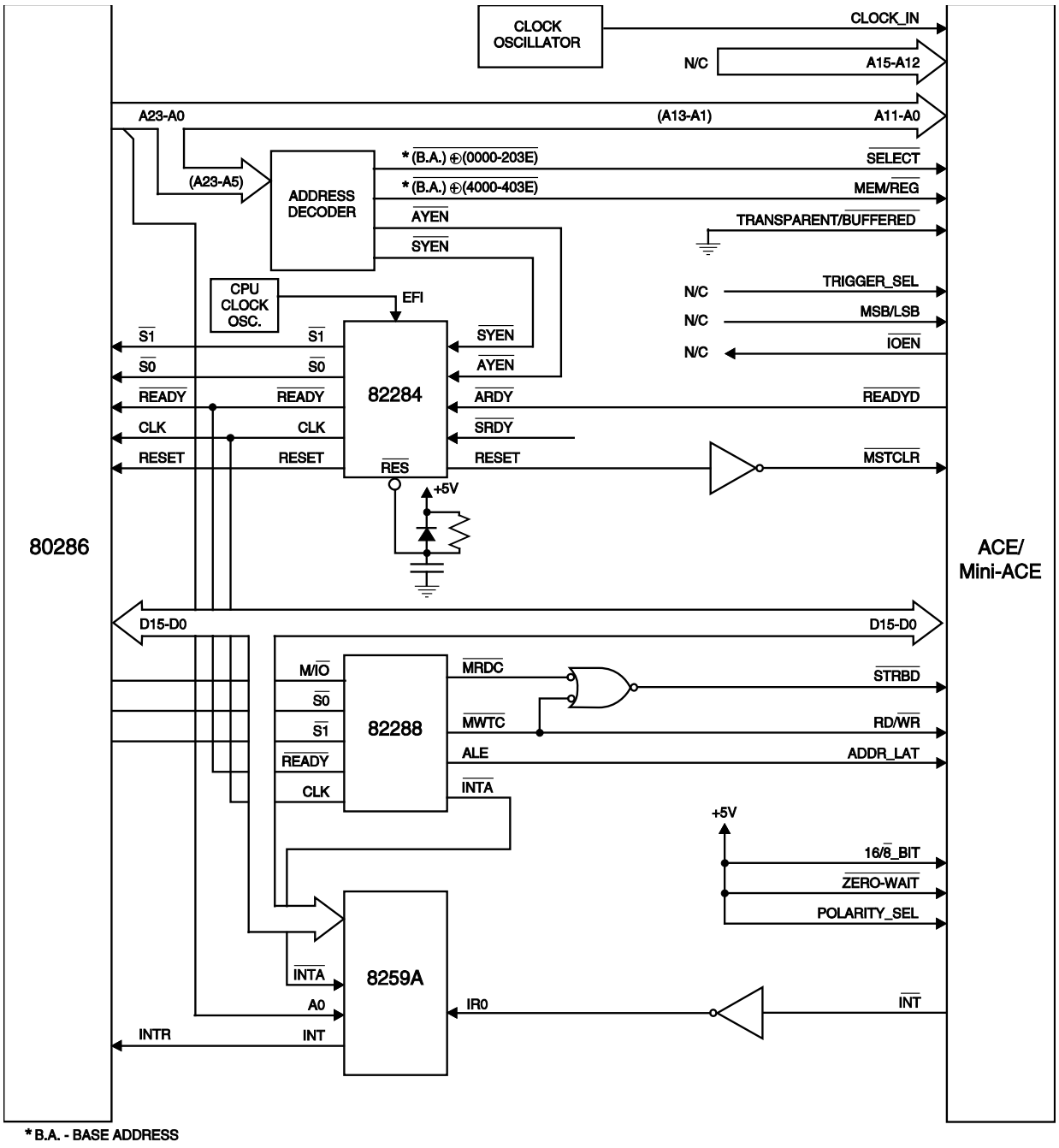


FIGURE 56. INTEL 80286-TO-ACE INTERFACE

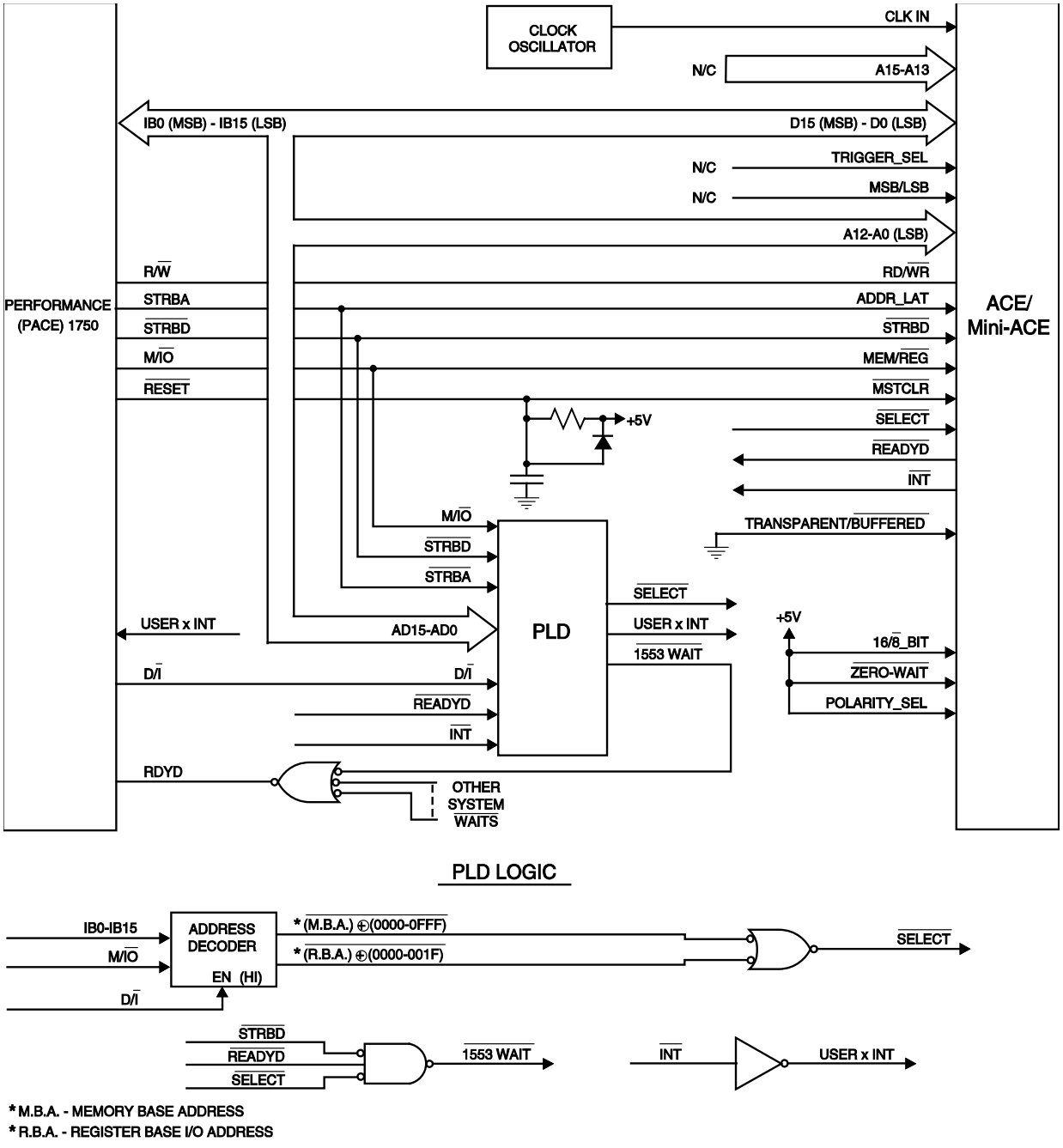


FIGURE 57. PERFORMANCE (PACE) 1750-TO-ACE INTERFACE

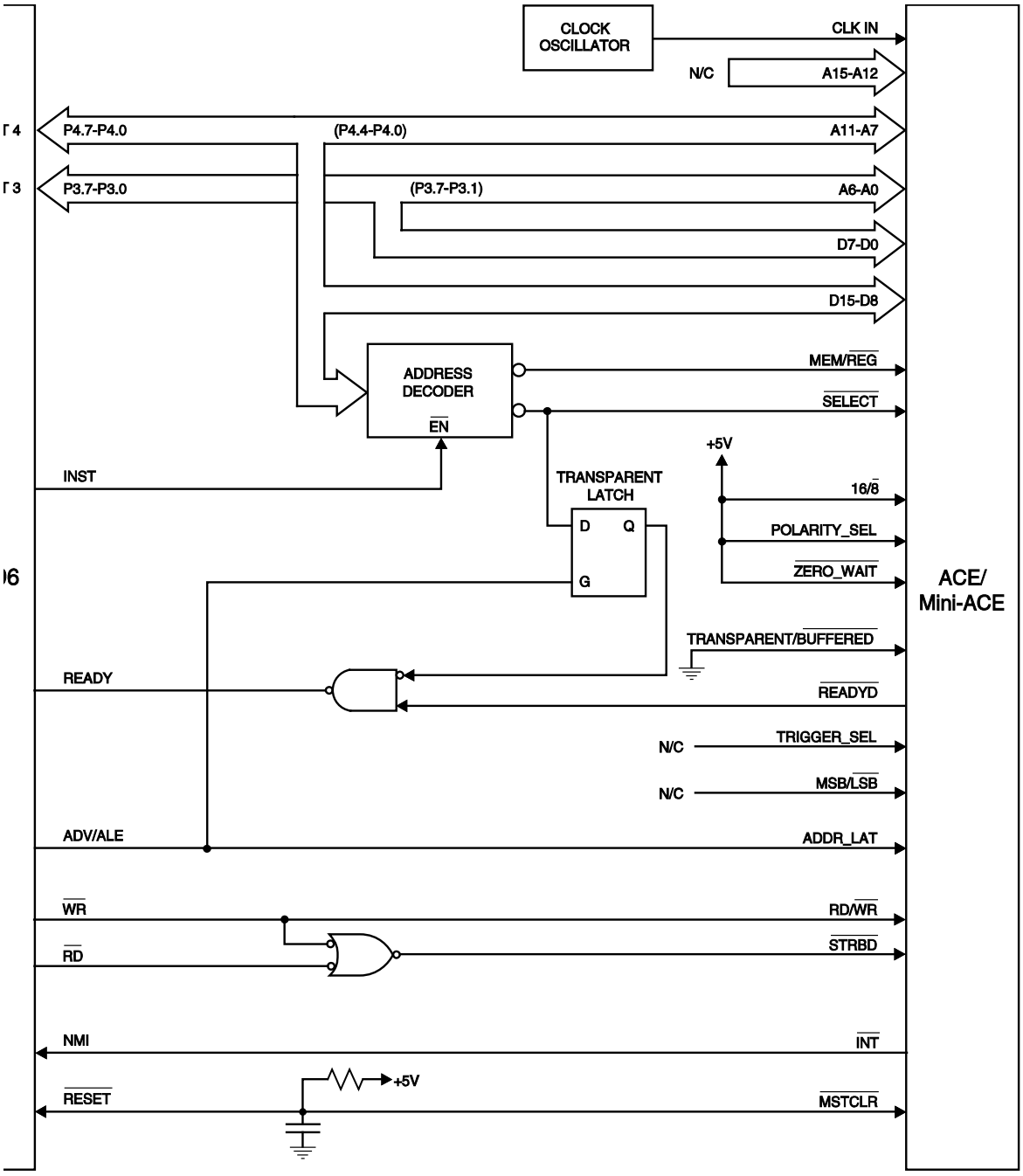


FIGURE 58. INTEL 80C196-TO-ACE INTERFACE

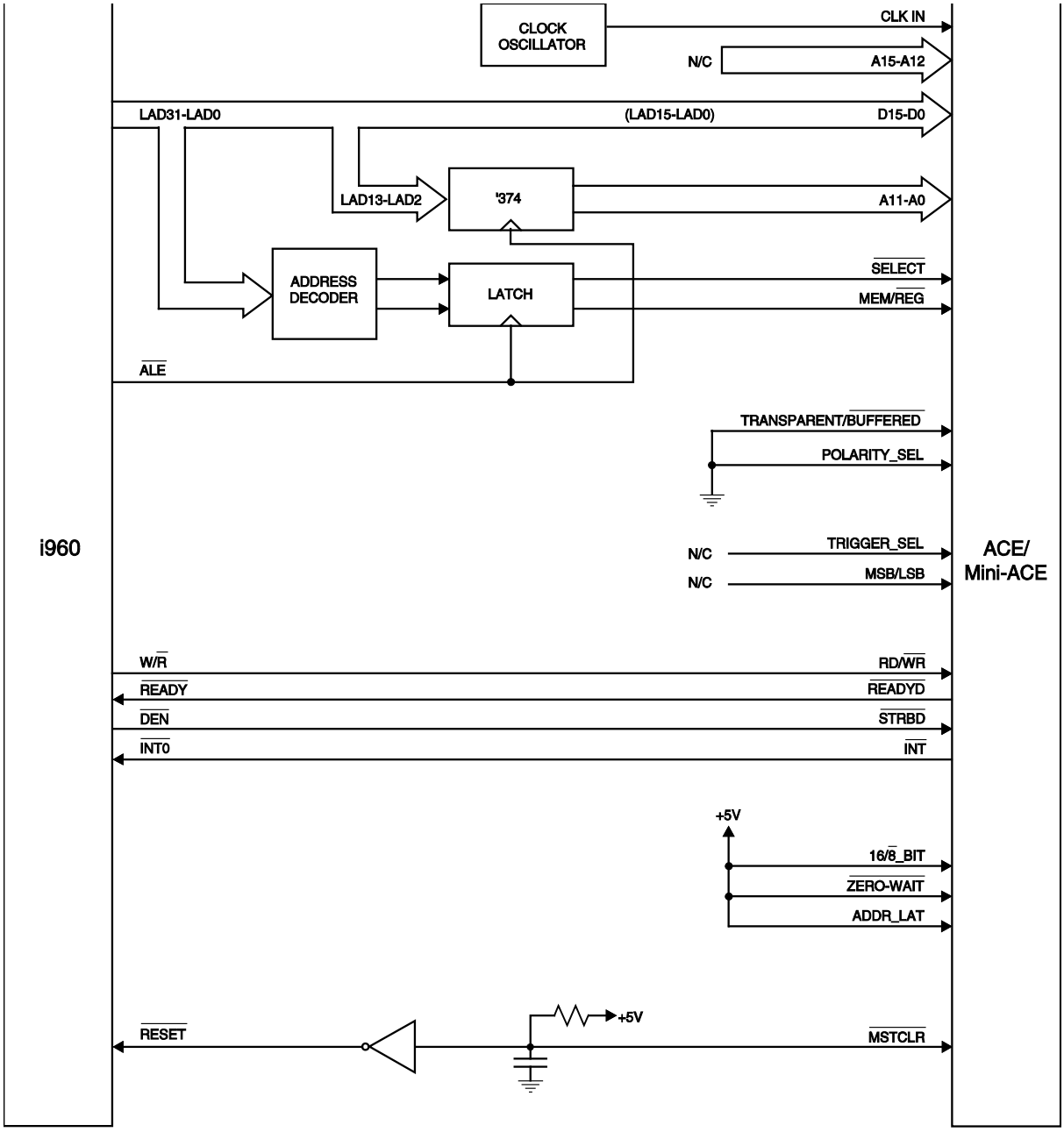


FIGURE 59. INTEL i960 TO ACE INTERFACE

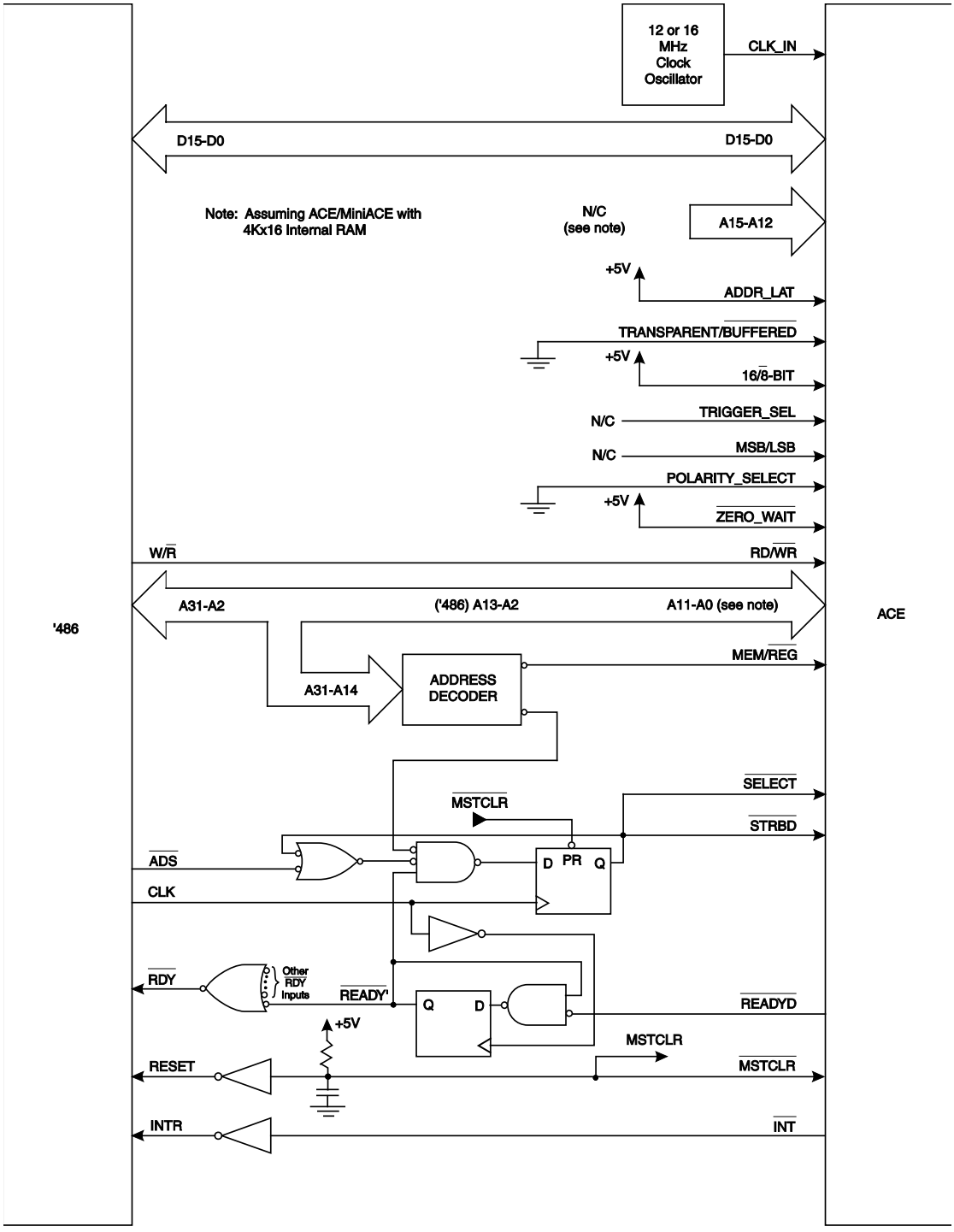


FIGURE 60. INTEL 80486 TO ACE INTERFACE

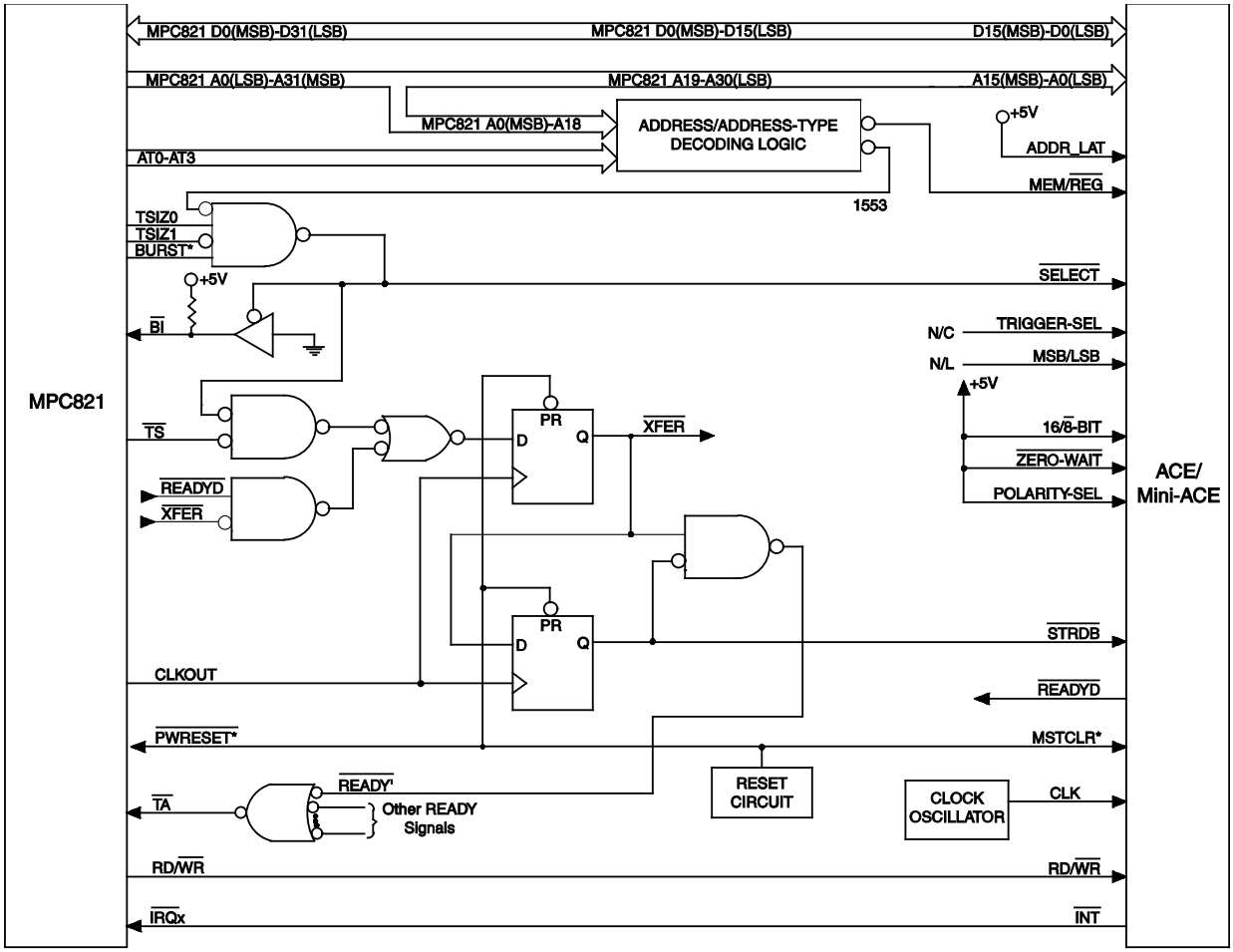


FIGURE 61. MOTOROLA MPC821 TO ACE INTERFACE

9 DETAILED DESCRIPTION OF 1553 MESSAGE SEQUENCES

9.1 GENERAL RAM TRANSFER TIMING

This section provides a comprehensive description of the 1553 protocol timing sequences for BC, RT, Message Monitor (MMT), and Word Monitor modes (WMT). This includes RAM transfer timing, and Message Sequence timing. All RAM transfer timing is shown for the transparent mode of operation (transfers are all internal for the buffered mode of operation and hence are not visible). The 1553 message sequence diagrams are shown as a top level summary of timing. These diagrams cross-reference detailed timing diagrams (such as Start Of Message sequence).

9.2 SINGLE WORD READ AND WRITE CYCLES

These transfer cycles are applicable to BC, RT, and MMT modes for the transfer of Command Words, Status Words, Data words, and Loopback words to the RAM and Data Words from the RAM.

The DMA control signal DTREQ* is asserted by the ACE/Mini-ACE (or SP'ACE and SP'ACE II) to request access to the host CPU RAM bus. The CPU responds with DTGRT* indicating that the interface bus is available for the ACE/Mini-ACE to read from RAM. The ACE/Mini-ACE in turn responds with a DMA acknowledge (DTACK*) and proceeds with the transfer cycle. The MEMENA_OUT* along with the Address lines are used to decode between external RAM (if applicable) and internal RAM through the use of the MEMENA-IN* input signal. (Note that for Mini-ACE series terminals, the MEMENA-OUT* signal is not available but be replaced by logically AND'ing DTACK* and IOEN*).

9.3 SOM/EOM BURST READ/WRITE TIMING

The Start Of Message (SOM) and End Of Message (EOM) timing sequences for BC, RT, and MMT modes consist of a multi-word read/modify/write cycle. FIGURE 64 illustrates a general multiword burst showing two read transfers followed by 2 write transfers. Note that the actual SOM and EOM transfers may consist of more than 2 read transfers and 2 write transfers. The timing for additional transfers remains the same. Each transfer (both read and write) consists of four clock cycles, with the exception being the first transfer, which takes five clock cycles. Note that the SP'ACE and SP'ACE II series components, when operating with an internal 8-bit shared RAM (i.e., BR_8BIT* connected to logic 0) will use 8 clock cycles per transfer (both read and write) when accessing internal RAM (i.e., MEMENA-IN* asserted to logic 0 in response to MEMENA-OUT* asserted to logic 0).

TABLE 128. ACE/Mini-ACE SINGLE WORD DMA READ (TRANSPARENT MODE)

ACE/MINI-ACE SINGLE WORD DMA READ (TRANSPARENT MODE)											
		ACE/MINI-ACE			SP'ACE			SP'ACE II			UNITS
REF	DESCRIPTION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t1	CLOCK IN rising delay to DTREQ* low			40			30			30	ns
t2	DTREQ* falling to DTGRT* low (@20 MHz - 8 Bit Buffered Memory)		N/A								µs
	DTREQ* falling to DTGRT* low (@20 MHz - 16 Bit Buffered Memory)			4.5							µs
	DTREQ* falling to DTGRT* low (@16 MHz - 8 Bit Buffered Memory)		N/A				4			4	µs
	DTREQ* falling to DTGRT* low (@16 MHz - 16 Bit Buffered Memory)			4			5			4	µs
	DTREQ* falling to DTGRT* low (@12 MHz - 8 Bit Buffered Memory)		N/A				3.5			3.5	µs
	DTREQ* falling to DTGRT* low (@12 MHz - 16 Bit Buffered Memory)			3.5			4.5			3.5	µs
	DTREQ* falling to DTGRT* low (@10 MHz - 8 Bit Buffered Memory)		N/A								µs
	DTREQ* falling to DTGRT* low (@10 MHz - 16 Bit Buffered Memory)			3.1							µs
t3	DTGRT* low setup prior to CLOCK IN rising	10			10			10			ns
t4	DTGRT* falling to DTACK* low (@20 MHz)			103							ns
	DTGRT* falling to DTACK* low (@16 MHz)			115			105			165	ns
	DTGRT* falling to DTACK* low (@12 MHz)			135			125			210	ns
	DTGRT* falling to DTACK* low (@10 MHz)			153							ns
t5	CLOCK IN rising to DTACK* low			40			30			30	ns
t6	DTGRT* hold time following DTACK* falling	0			0			0			ns
t7	CLOCK IN rising to MEMENA-OUT* low			40			35			35	ns
t8	CLOCK IN rising to Address outputs valid			40			30			30	ns
t9	CLOCK IN rising to MEMOE* low			40			30			30	ns
t10	MEMENA-IN* setup delay following CLOCK IN rising (@20 MHz)			20							
	MEMENA-IN* setup delay following CLOCK IN rising (@16 MHz)			30			40			40	ns
	MEMENA-IN* setup delay following CLOCK IN rising (@12 MHz)			50			60			60	ns
	MEMENA-IN* setup delay following CLOCK IN rising (@10 MHz)			70							
t11	DTACK* low pulse width (@20 MHz - 8 Bit Memory Access)		N/A								ns
	DTACK* low pulse width (@20 MHz - 16 Bit Memory Access)		250								ns
	DTACK* low pulse width (@16 MHz - 8 Bit Memory Access)		N/A		550	562.5	580	550	562.5	580	ns
	DTACK* low pulse width (@16 MHz - 16 Bit Memory Access)	300	312.5	330	300	312.5	330	300	312.5	330	ns
	DTACK* low pulse width (@12 MHz - 8 Bit Memory Access)		N/A		735	750	765	735	750	765	ns
	DTACK* low pulse width (@12 MHz - 16 Bit Memory Access)	400	416.6	430	400	416.6	430	400	416.6	430	ns
	DTACK* low pulse width (@10 MHz - 8 Bit Memory Access)		N/A								ns
	DTACK* low pulse width (@10 MHz - 16 Bit Memory Access)		500								ns
t12	CLOCK IN rising to Output Data valid (Note: Asserted for reads from internal RAM only)			60			60			60	ns
t13	Input Data setup time prior to CLOCK IN rising (Note: Valid for reads from external RAM only)	30			20			20			ns

TABLE 128. ACE/Mini-ACE SINGLE WORD DMA READ (TRANSPARENT MODE)											
ACE/MINI-ACE SINGLE WORD DMA READ (TRANSPARENT MODE)											
		ACE/MINI-ACE			SP'ACE			SP'ACE II			UNITS
REF	DESCRIPTION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t14	MEMOE* low pulse width (@20 MHz - 8 Bit Memory)		N/A								ns
	MEMOE* low pulse width (@20 MHz - 16 Bit Memory)	135	150	165							ns
	MEMOE* low pulse width (@16 MHz - 8 Bit Memory)		N/A		425	437.5	455	425	437.5	455	ns
	MEMOE* low pulse width (@16 MHz - 16 Bit Memory)	170	187.5	200	170	187.5	200	170	187.5	200	ns
	MEMOE* low pulse width (@12 MHz - 8 Bit Memory)		N/A		570	583.3	600	570	583.3	600	ns
	MEMOE* low pulse width (@12 MHz - 16 Bit Memory)	235	250	265	235	250	265	235	250	265	ns
	MEMOE* low pulse width (@10 MHz - 8 Bit Memory)		N/A								ns
	MEMOE* low pulse width (@10 MHz - 16 Bit Memory)	285	300	315							ns
t15	Input Data hold time following CLOCK IN rising	30			25			25			ns
t16	CLOCK IN rising to DTREQ* high, DTACK* high, MEMENA-OUT* high, MEMOE* high			40			35			35	ns
t17	Output Address and Output Data hold time following CLOCK IN rising	0			0			0			ns
t18	CLOCK IN rising to Output Address and Output Data tri-state			45			35			35	ns
t19	MEMENA_IN* low hold time following CLOCK IN rising edge	0			0			0			ns

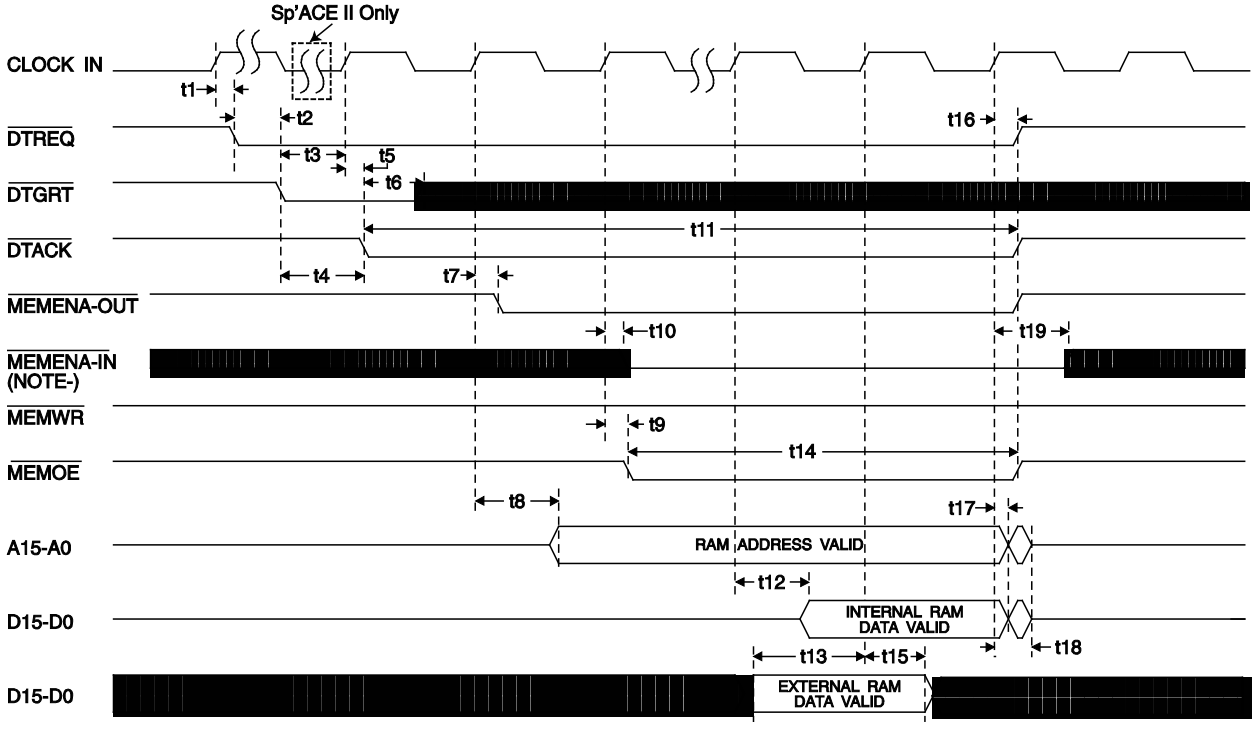


FIGURE 62. ACE/Mini-ACE SINGLE WORD DMA READ (TRANSPARENT MODE)

TABLE 129. ACE/Mini-ACE SINGLE WORD DMA WRITE (TRANSPARENT MODE)

ACE/MINI-ACE SINGLE WORD DMA WRITE (TRANSPARENT MODE)											
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			SP'ACE II			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t1	CLOCK IN rising delay to DTREQ* low			40			30			30	ns
t2	DTREQ* falling to DTGRT* low (@20 MHz - 8 Bit buffered Memory)		N/A								µs
	DTREQ* falling to DTGRT* low (@20 MHz - 16 Bit buffered Memory)			4.5							µs
	DTREQ* falling to DTGRT* low (@16 MHz - 8 Bit buffered Memory)		N/A				4			4	µs
	DTREQ* falling to DTGRT* low (@16 MHz - 16 Bit buffered Memory)			4			5			4	µs
	DTREQ* falling to DTGRT* low (@12 MHz - 8 Bit buffered Memory)		N/A				3.5			3.5	µs
	DTREQ* falling to DTGRT* low (@12 MHz - 16 Bit buffered Memory)			3.5			4.5			3.5	µs
	DTREQ* falling to DTGRT* low (@10 MHz - 8 Bit buffered Memory)		N/A								µs
	DTREQ* falling to DTGRT* low (@10 MHz - 16 Bit buffered Memory)			3.1							µs
t3	DTGRT* low setup prior to CLOCK IN rising	10			10			10			ns
t4	DTGRT* falling to DTACK* low (@16 MHz)			115			105			165	ns
t4	DTGRT* falling to DTACK* low (@12 MHz)			135			125			210	ns
t5	CLOCK IN rising to DTACK* low			40			30			30	ns
t6	DTGRT* hold time following DTACK* falling	0			0			0			ns
t7	CLOCK IN rising to MEMENA-OUT* low			40			35			35	ns
t8	CLOCK IN rising to Address outputs valid			40			30			30	ns
t9	CLOCK IN rising to Output Data valid			40			35			35	ns
	DTACK* low pulse width (@20 MHz - 8 Bit Memory Access)		N/A								ns
	DTACK* low pulse width (@20 MHz - 16 Bit Memory Access)	235	250	265							ns
	DTACK* low pulse width (@16 MHz - 8 Bit Memory Access)		N/A		550	562.5	580	550	562.5	580	ns
	DTACK* low pulse width (@16 MHz - 16 Bit Memory Access)	300	312.5	330	300	312.5	330	300	312.5	330	ns
	DTACK* low pulse width (@12 MHz - 8 Bit Memory Access)		N/A		735	750	765	735	750	765	ns
	DTACK* low pulse width (@12 MHz - 16 Bit Memory Access)	400	416.6	430	400	416.6	430	400	416.6	430	ns
	DTACK* low pulse width (@10 MHz - 8 Bit Memory Access)		N/A								ns
	DTACK* low pulse width (@10 MHz - 16 Bit Memory Access)	485	500	515							ns
t11	MEMENA-IN* setup delay following CLOCK IN rising (@16 MHz)			40			40			40	ns
t11	MEMENA-IN* setup delay following CLOCK IN rising (@12 MHz)			60			60			60	ns
t12	CLOCK IN rising to MEMWR* low			40			30			30	ns
t13	MEMWR* low pulse width (@20 MHz)	35	50	65							ns
	MEMWR* low pulse width (@16 MHz)	50	62.5	80	55	62.5	70	55	62.5	70	ns
	MEMWR* low pulse width (@12 MHz)	70	83.3	100	75	83.3	90	75	83.3	90	ns
	MEMWR* low pulse width (@10 MHz)	85	100	115							ns
t14	CLOCK IN rising to MEMWR* high			40			30			30	ns
t15	MEMENA-IN* hold time following CLOCK IN rising	0			0			0			ns
t16	CLOCK IN rising to DTREQ* high, DTACK* high, MEMENA-OUT* high			40			35			35	ns
t17	Output Address and Output Data hold time following CLOCK IN rising	0			0			0			ns
t18	CLOCK IN rising to Output Address and Output Data tri-state			45			35			35	ns

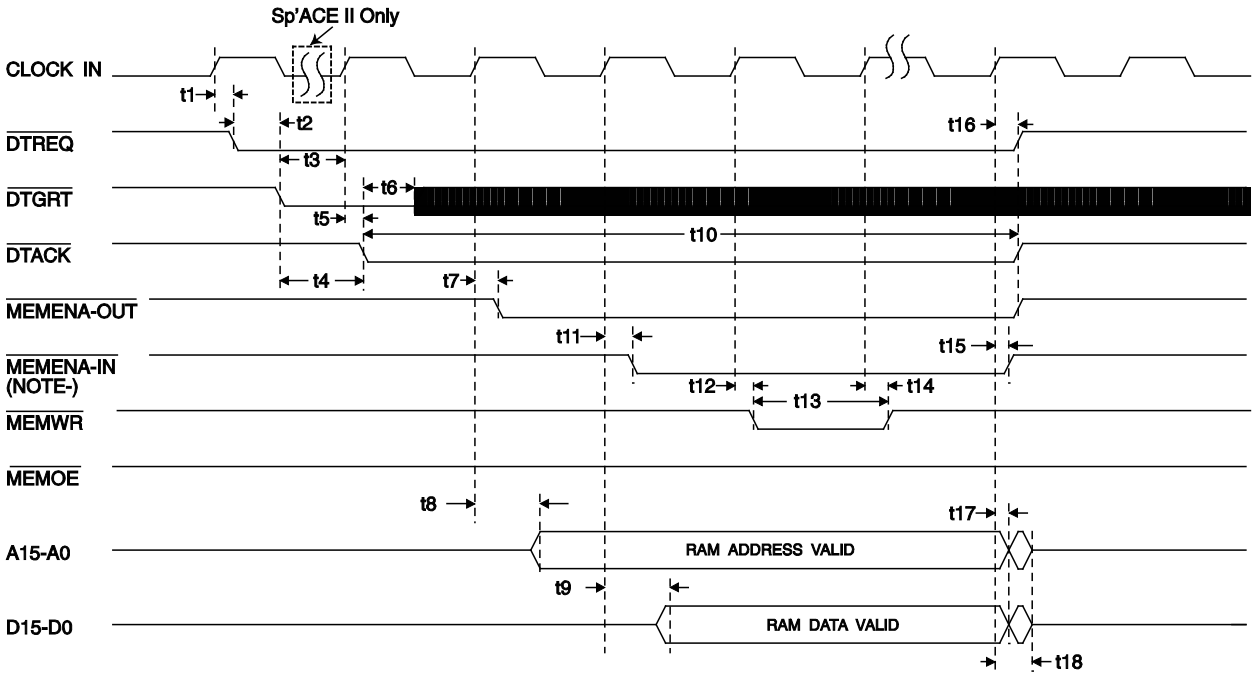


FIGURE 63. ACE/Mini-ACE SINGLE WORD DMA WRITE (TRANSPARENT MODE)

TABLE 130. BC/RT/MT SOM/EOM BURST READ/WRITE TIMING

BC/RT/MT SOM/EOM BURST READ/WRITE TIMING											
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			SP'ACE II			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t1	CLOCK IN rising delay to DTREQ* low			40			30			30	ns
t2	DTREQ* falling to DTGRT* low (@20 MHz - 8 Bit Buffered Memory)		N/A								µs
	DTREQ* falling to DTGRT* low (@20 MHz - 16 Bit Buffered Memory)			4.5							µs
	DTREQ* falling to DTGRT* low (@16 MHz - 8 Bit Buffered Memory)		N/A				4			4	µs
	DTREQ* falling to DTGRT* low (@16 MHz - 16 Bit Buffered Memory)			4			5			4	µs
	DTREQ* falling to DTGRT* low (@12 MHz - 8 Bit Buffered Memory)		N/A				3.5			3.5	µs
	DTREQ* falling to DTGRT* low (@12 MHz - 16 Bit Buffered Memory)			3.5			4.5			3.5	µs
	DTREQ* falling to DTGRT* low (@10 MHz - 8 Bit Buffered Memory)		N/A								µs
	DTREQ* falling to DTGRT* low (@10 MHz - 16 Bit Buffered Memory)			3.1							µs
t3	DTGRT* falling edge delay to DTACK* falling edge (@20 MHz)			107							
	DTGRT* falling edge delay to DTACK* falling edge (@16 MHz)			115			105			165	ns
	DTGRT* falling edge delay to DTACK* falling edge (@12 MHz)			135			125			210	ns
	DTGRT* falling edge delay to DTACK* falling edge (@10 MHz)			158							
t4	DTGRT* low hold time following DTACK* falling edge.	0			0			0			ns
t5	CLOCK IN rising to DTACK* low			40			30			30	ns
t6	CLOCK IN rising to MEMENA-OUT* low			40			35			35	ns
t7	CLOCK IN rising to Address outputs valid			40			30			30	ns
t8	CLOCK IN rising to MEMOE* low			40			30			30	ns
t9	MEMENA-IN* setup delay following to CLOCK IN rising			30			40			40	ns
t10	CLOCK IN rising to Output Data valid (Note: asserted for reads from internal RAM only)			60			60			60	ns
t11	Input Data setup time prior to CLOCK IN rising (Note: valid for reads from external RAM only)	30			20			20			ns
t12	Input Data hold time following CLOCK IN rising	30			25			25			ns
t13	MEMENAIN* valid hold time following CLOCK IN rising edge.	0			0			0			ns
t14	CLOCK IN rising edge delay to MEMOE* rising edge.			40			30			30	ns
t15	Output Address and Output Data valid hold time following CLOCK IN rising edge.	0			0			0			ns
t16	CLOCK IN rising edge delay to Output Address valid for next address.			50			30			30	ns
t17	CLOCK IN rising edge delay to Output Data tri-state.			45			35			35	ns
t18	CLOCK IN rising edge delay to Output Data valid.			40			35			35	ns
t19	CLOCK IN rising edge delay to MEMWR* falling edge.			40			30			30	ns
t20	CLOCK IN rising edge delay to MEMWR* rising edge.			40			30			30	ns
t22	CLOCK IN rising edge delay to DTREQ* rising edge.			35			30			30	ns
t23	CLOCK IN rising edge delay to DTACK* rising edge.			35			30			30	ns
t24	CLOCK IN rising edge delay to MEMENAOUT* rising edge.			40			35			35	ns
t25	CLOCK IN rising edge delay to Output Address tri-state.			45			35			35	ns

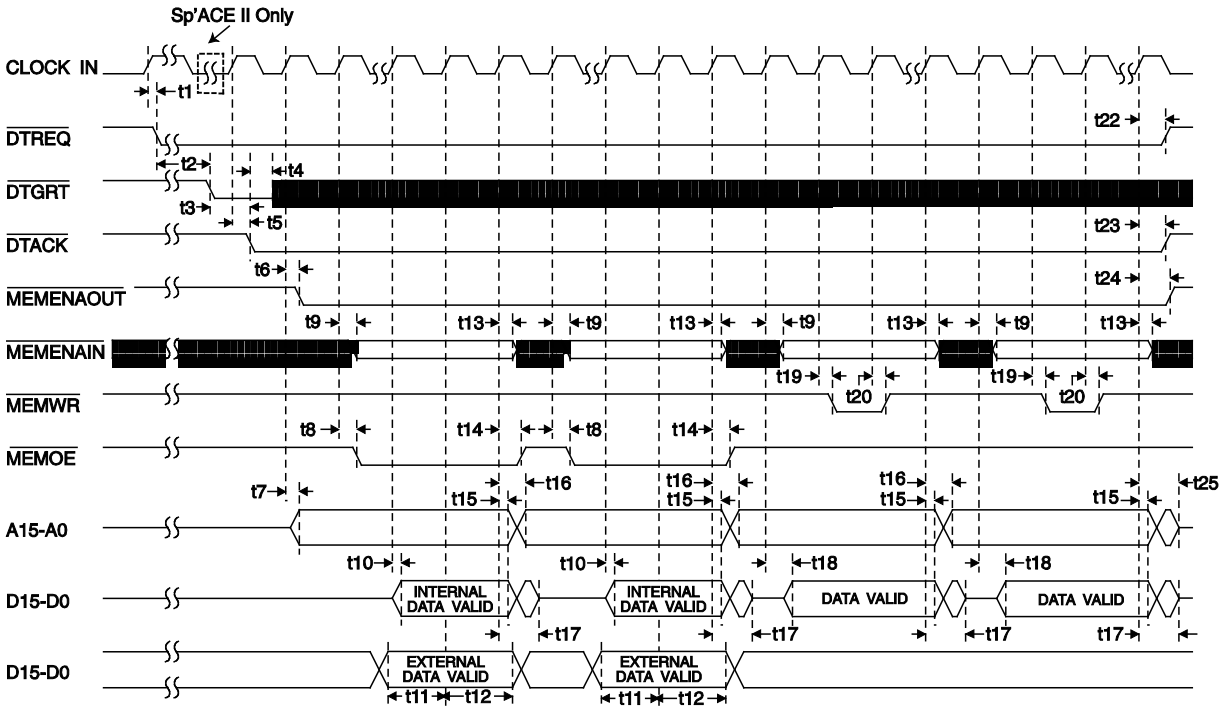


FIGURE 64. MT BC/RT/MT SOM/EOM BURST READ/WRITE TIMING

9.4 BC OPERATION

FIGURE 65 through FIGURE 71 illustrate the overall BC message sequence timing for receive, transmit, and broadcast message formats. Each message sequence shows an SOM and EOM sequence as well as single word DMA read cycles and/or DMA write cycles. One of the DMA write cycles shown in the sequence is a command word or data word "looped back". Each word transmitted by the ACE/Mini-ACE is also decoded by the ACE/Mini-ACE's receiver section. The transmitter and receiver sections are independent within the ACE/Mini-ACE and operate independently. Upon completion of the last word transmitted by the ACE/Mini-ACE (Command word in a transmit message or a data word in a receive message), assuming that there are no errors detected by the receiver, the received copy of the word is written into the ACE/Mini-ACE's RAM in a location referred to as the loopback word. The loopback word is stored in RAM to provide a simple mechanism for self testing the ACE/Mini-ACE.

FIGURE 68 illustrates BC start timing for messages in a frame. The first message in a frame may be started by either an external trigger input, an internal trigger (internal frame timer), or a software start (start bit in start/reset register). Subsequent message in a frame will start based on the minimum intermessage gap time, as illustrated in FIGURE 68, unless

the Message Gap time feature is used to increase this time. FIGURE 69 and FIGURE 70 illustrate the BC Start Of Message (SOM) and End Of Message (EOM) sequences. FIGURE 71 illustrates the timing of automatic retries.

TABLE 131. BC MODE RECEIVE MESSAGE TIMING SEQUENCE

BC MODE RECEIVE MESSAGE TIMING SEQUENCE								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Mid-sync crossing of current word delay to DTREQ* falling (requesting next data word read access) (@20 MHz)	1.0	1.12	1.2				µs
	Mid-sync crossing of current word delay to DTREQ* falling (requesting next data word read access) (@16 MHz)	1.2	1.35	1.45	1.2	1.35	1.45	µs
	Mid-sync crossing of current word delay to DTREQ* falling (requesting next data word read access) (@12 MHz)	1.36	1.52	1.6	1.36	1.52	1.6	µs
	Mid-sync crossing of current word delay to DTREQ* falling (requesting next data word read access) (@10 MHz)	1.5	1.65	1.8				µs
t2	RT Response timeout (note 1).			17.5			17.5	µs
t3	Mid-parity crossing of status word to DTREQ* falling (requesting status word write access) (@20 MHz)	1.04	1.32	1.60				µs
	Mid-parity crossing of status word to DTREQ* falling (requesting status word write access) (@16 MHz)	1.2	1.41	1.77	1.2	1.41	1.77	µs
	Mid-parity crossing of status word to DTREQ* falling (requesting status word write access) (@12 MHz)	1.36	1.6	1.98	1.36	1.6	1.98	µs
	Mid-parity crossing of status word to DTREQ* falling (requesting status word write access) (@10 MHz)	1.45	1.75	2.1				µs
t4	Mid-parity crossing of status word to DTREQ* falling (requesting BC end of message access) (@20 MHz)	6.58	6.8	7.16				µs
	Mid-parity crossing of status word to DTREQ* falling (requesting BC end of message access) (@16 MHz)	6.70	6.91	7.27	7.70	7.91	8.27	µs
	Mid-parity crossing of status word to DTREQ* falling (requesting BC end of message access) (@12 MHz)	6.78	7.02	7.39	7.78	8.02	8.39	µs
	Mid-parity crossing of status word to DTREQ* falling (requesting BC end of message access) (@10 MHz)	6.85	7.1	7.47				µs
t5	Mid-parity crossing of last transmitted word to DTREQ* falling (requesting loopback word write access) (@20 MHz)	2.92	3.15	3.25				µs
	Mid-parity crossing of last transmitted word to DTREQ* falling (requesting loopback word write access) (@16 MHz)	3.06	3.29	3.37	3.06	3.29	3.37	µs
	Mid-parity crossing of last transmitted word to DTREQ* falling (requesting loopback word write access) (@12 MHz)	3.20	3.43	3.51	3.20	3.43	3.51	µs
	Mid-parity crossing of last transmitted word to DTREQ* falling (requesting loopback word write access) (@10 MHz)	3.50	3.75	3.83				µs

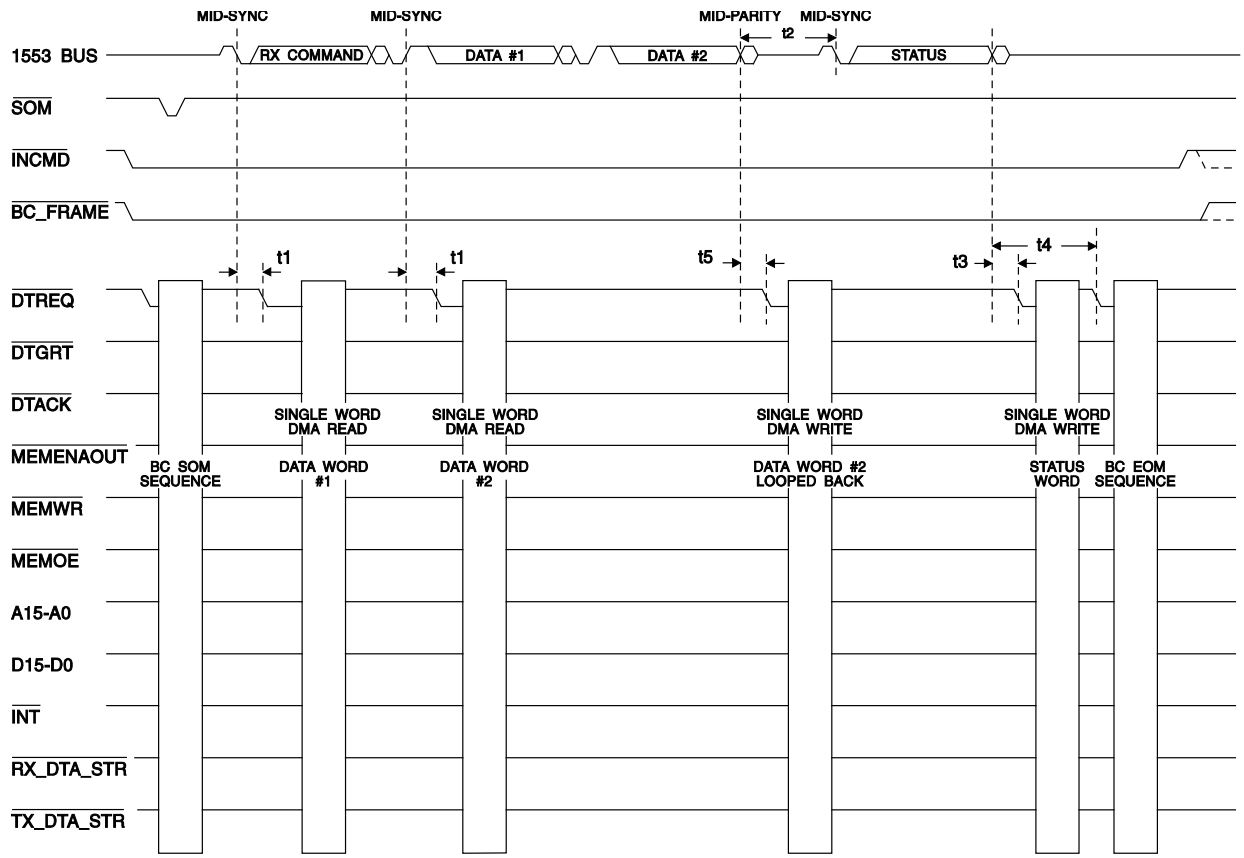


FIGURE 65. BC MODE RECEIVE MESSAGE TIMING SEQUENCE

NOTES for TABLE 131 and FIGURE 65.
1. RT response timeout is software programmable. 18.5 µs represents the default value.

TABLE 132. BC MODE TRANSMIT MESSAGE TIMING SEQUENCE

BC MODE TRANSMIT MESSAGE TIMING SEQUENCE								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	RT Response timeout (note 1).			17.5			17.5	µs
t2	Mid-parity crossing delay to DTREQ* falling (requesting loopback write access) (@20 MHz)	2.92	3.15	3.25				µs
	Mid-parity crossing delay to DTREQ* falling (requesting loopback write access) (@16 MHz)	3.06	3.29	3.37	3.06	3.29	3.37	µs
	Mid-parity crossing delay to DTREQ* falling (requesting loopback write access) (@12 MHz)	3.20	3.43	3.51	3.20	3.43	3.51	µs
	Mid-parity crossing delay to DTREQ* falling (requesting loopback write access) (@10 MHz)	3.50	3.75	3.83				µs
t3	Mid-parity crossing delay to DTREQ* falling (requesting BC end of message access) (@20 MHz)	6.58	6.8	7.16				µs
	Mid-parity crossing delay to DTREQ* falling (requesting BC end of message access) (@16 MHz)	6.70	6.91	7.27	7.70	7.91	8.27	µs
	Mid-parity crossing delay to DTREQ* falling (requesting BC end of access) (@12 MHz)message	6.78	7.02	7.39	7.78	8.02	8.39	µs
	Mid-parity crossing delay to DTREQ* falling (requesting BC end of message access) (@10 MHz)	6.85	7.1	7.47				µs
t4	Mid-parity crossing delay to DTREQ* falling (requesting Status and Data Word write access) (@20 MHz)	1.04	1.32	1.60				µs
	Mid-parity crossing delay to DTREQ* falling (requesting Status and Data Word write access) (@16 MHz)	1.20	1.41	1.77	1.20	1.41	1.77	µs
	Mid-parity crossing delay to DTREQ* falling (requesting Status and Data Word write access) (@12 MHz)	1.36	1.60	1.98	1.36	1.60	1.98	µs
	Mid-parity crossing delay to DTREQ* falling (requesting Status and Data Word write access) (@10 MHz)	1.45	1.75	2.1				µs

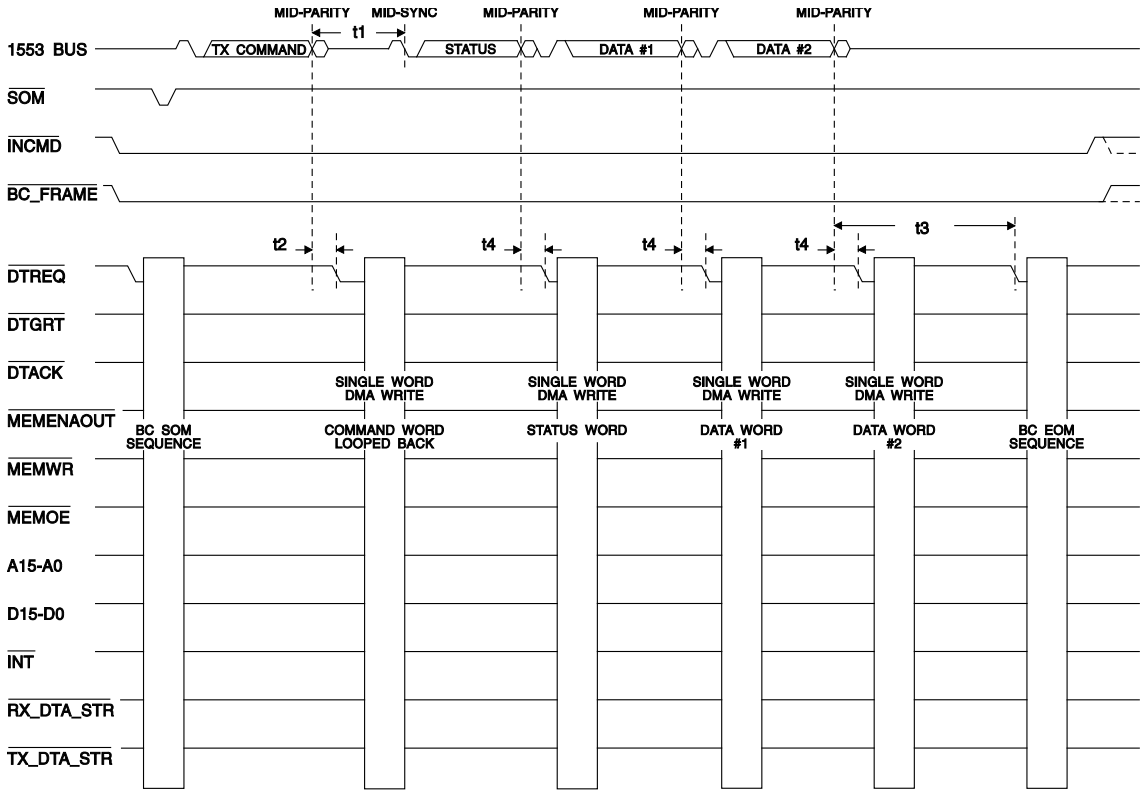


FIGURE 66. BC MODE TRANSMIT MESSAGE TIMING SEQUENCE

NOTES for TABLE 132 and FIGURE 66.
1. RT response timeout is software programmable. 18.5 µs represents the default timeout value.

TABLE 133. BC MODE BROADCAST MESSAGE TIMING SEQUENCE.

BC MODE BROADCAST MESSAGE TIMING SEQUENCE								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Mid-sync crossing of current word delay to DTREQ* falling (requesting next data word read access) (@20 MHz)	1.0	1.12	1.2				µs
	Mid-sync crossing of current word delay to DTREQ* falling (requesting next data word read access) (@16 MHz)	1.20	1.35	1.45	1.20	1.35	1.45	µs
	Mid-sync crossing of current word delay to DTREQ* falling (requesting next data word read access) (@12 MHz)	1.36	1.52	1.60	1.36	1.52	1.60	µs
	Mid-sync crossing of current word delay to DTREQ* falling (requesting next data word read access) (@10 MHz)	1.5	1.65	1.8				µs
t2	Mid-parity crossing of last data word to DTREQ* falling (loopback word write access request) (@20 MHz)	2.92	3.15	3.25				µs
	Mid-parity crossing of last data word to DTREQ* falling (loopback word write access request) (@16 MHz)	3.06	3.29	3.37	3.06	3.29	3.37	µs
	Mid-parity crossing of last data word to DTREQ* falling (loopback word write access request) (@12 MHz)	3.20	3.43	3.51	3.20	3.43	3.51	µs
	Mid-parity crossing of last data word to DTREQ* falling (loopback word write access request) (@10 MHz)	3.50	3.75	3.83				µs
t3	DTREQ* rising to DTREQ* falling (@20 MHz)	75	100	125				ns
	DTREQ* rising to DTREQ* falling (@16 MHz)	100	125	150	100	125	150	ns
	DTREQ* rising to DTREQ* falling (@12 MHz)	140	166	190	140	166	190	ns
	DTREQ* rising to DTREQ* falling (@10 MHz)	175	200	225				ns

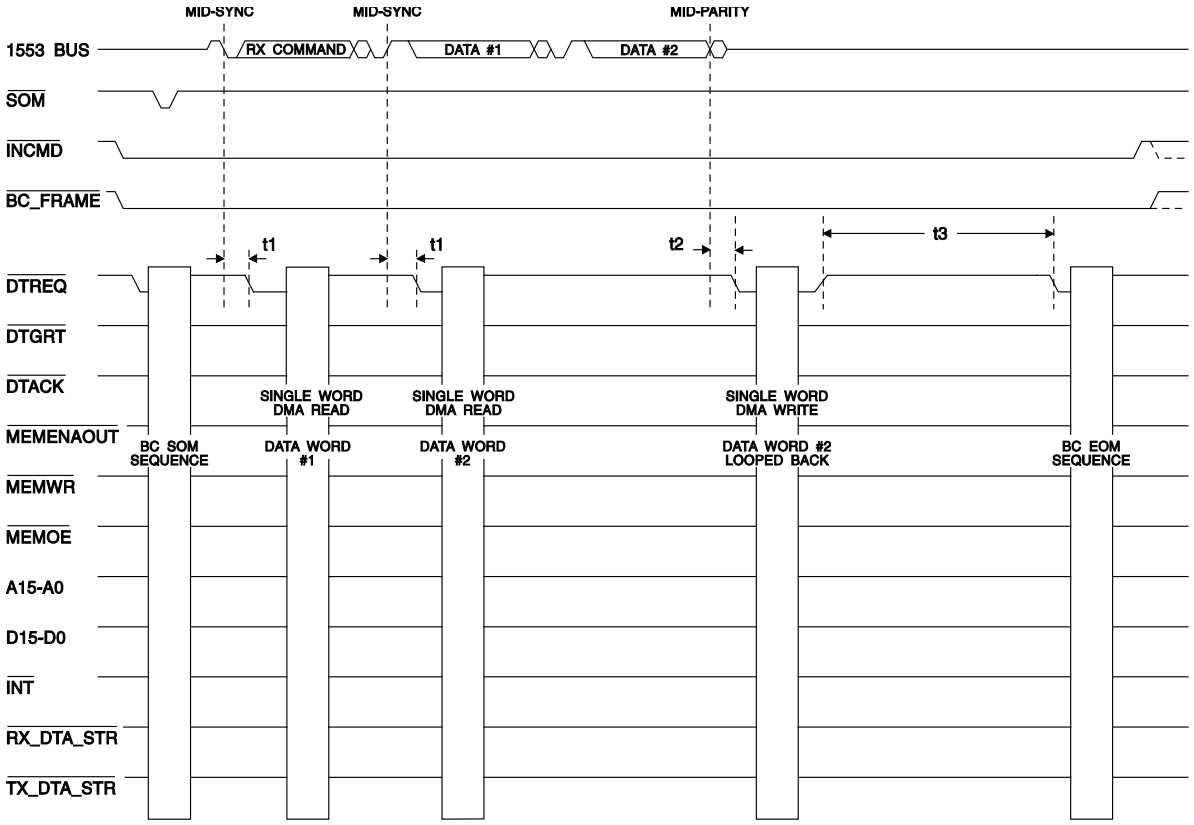


FIGURE 67. BC MODE BROADCAST MESSAGE TIMING SEQUENCE

NOTES for TABLE 133 and FIGURE 67.
1. RT response timeout is software programmable. 18.5 µs represents the default value.

TABLE 134. BC MODE START TIMING.

BC MODE START TIMING									
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	READYD* falling (write access to start register bit) delay to DTREQ* falling (BC SOM) (@20 MHz)	120	150	180				ns
	READYD* falling (write access to start register bit) delay to DTREQ* falling (BC SOM) (@16 MHz)	160	188	220	160	188	220	ns
	READYD* falling (write access to start register bit) delay to DTREQ* falling (BC SOM) (@12 MHz)	220	250	280	220	250	280	ns
	READYD* falling (write access to start register bit) delay to DTREQ* falling (BC SOM) (@10 MHz)	270	300	330				ns
t2	EXT_TRIG* rising delay to DTREQ* falling (BC SOM) (@20 MHz)	145	175	225				ns
	EXT_TRIG* rising delay to DTREQ* falling (BC SOM) (@16 MHz)	160	220	280	160	220	280	ns
	EXT_TRIG* rising delay to DTREQ* falling (BC SOM) (@12 MHz)	220	290	360	220	290	360	ns
	EXT_TRIG* rising delay to DTREQ* falling (BC SOM) (@10 MHz)	287	350	445				ns
t3	BC Intermessage GAP (Note 1,2) (@20 MHz - first Broadcast message)	8.4	8.5	8.7				µs
	BC Intermessage GAP (Note 1,2) (@20 MHz - non-Broadcast message)	10.7	10.8	11.0				µs
	BC Intermessage GAP (Note 1,2) (@16 MHz - first Broadcast message)	9.0	9.1	9.2	12.3	12.4	12.5	µs
	BC Intermessage GAP (Note 1,2) (@16 MHz - non-Broadcast message)	11.9	12.2	12.7	15.9	16.2	16.7	µs
	BC Intermessage GAP (Note 1,2) (@12 MHz - first Broadcast message)	10.6	10.7	10.8	14.9	15.0	15.1	µs
	BC Intermessage GAP (Note 1,2) (@12 MHz - non-Broadcast message)	13.2	13.6	14.1	18.2	18.6	19.1	µs
	BC Intermessage GAP (Note 1,2) (@10 MHz - first Broadcast message)	14.6	14.8	15.1				µs
	BC Intermessage GAP (Note 1,2) (@10 MHz - non-Broadcast message)	15.8	16.0	16.3				µs
t4	INCMD* rising delay to INCMD* falling (Note 1) (@20 MHz)	35	50	65				ns
	INCMD* rising delay to INCMD* falling (Note 1) (@16 MHz)	40	62.5	85	40	62.5	85	ns
	INCMD* rising delay to INCMD* falling (Note 1) (@12 MHz)	60	83.3	105	60	83.3	105	ns
	INCMD* rising delay to INCMD* falling (Note 1) (@10 MHz)	85	100	115				ns
t5	INCMD* falling delay to DTREQ* falling (BC SOM) (@20 MHz)	35	50	65				ns
	INCMD* falling delay to DTREQ* falling (BC SOM) (@16 MHz)	40	62.5	85	40	62.2	85	ns
	INCMD* falling delay to DTREQ* falling (BC SOM) (@12 MHz)	60	83.3	105	60	83.3	105	ns
	INCMD* falling delay to DTREQ* falling (BC SOM) (@10 MHz)	85	100	115				ns
t6	DTACK* falling delay to DTACK* rising (@20 MHz)	1.15	1.20	1.25				µs
	DTACK* falling delay to DTACK* rising (@16 MHz)	1.77	1.81	1.85	3.54	3.56	3.58	µs
	DTACK* falling delay to DTACK* rising (@12 MHz)	2.37	2.42	2.46	4.73	4.75	4.77	µs
	DTACK* falling delay to DTACK* rising (@10 MHz)	2.75	2.85	2.95				µs
t7	DTACK* rising delay to mid-sync crossing of command word (@20 MHz)	1.70	1.80	2.0				µs
	DTACK* rising delay to mid-sync crossing of command word (@16 MHz)	1.82	1.90	2.05	1.82	1.90	2.05	µs
	DTACK* rising delay to mid-sync crossing of command word (@12 MHz)	1.90	1.98	2.14	1.90	1.98	2.14	µs
	DTACK* rising delay to mid-sync crossing of command word (@10 MHz)	1.95	2.05	2.25				µs

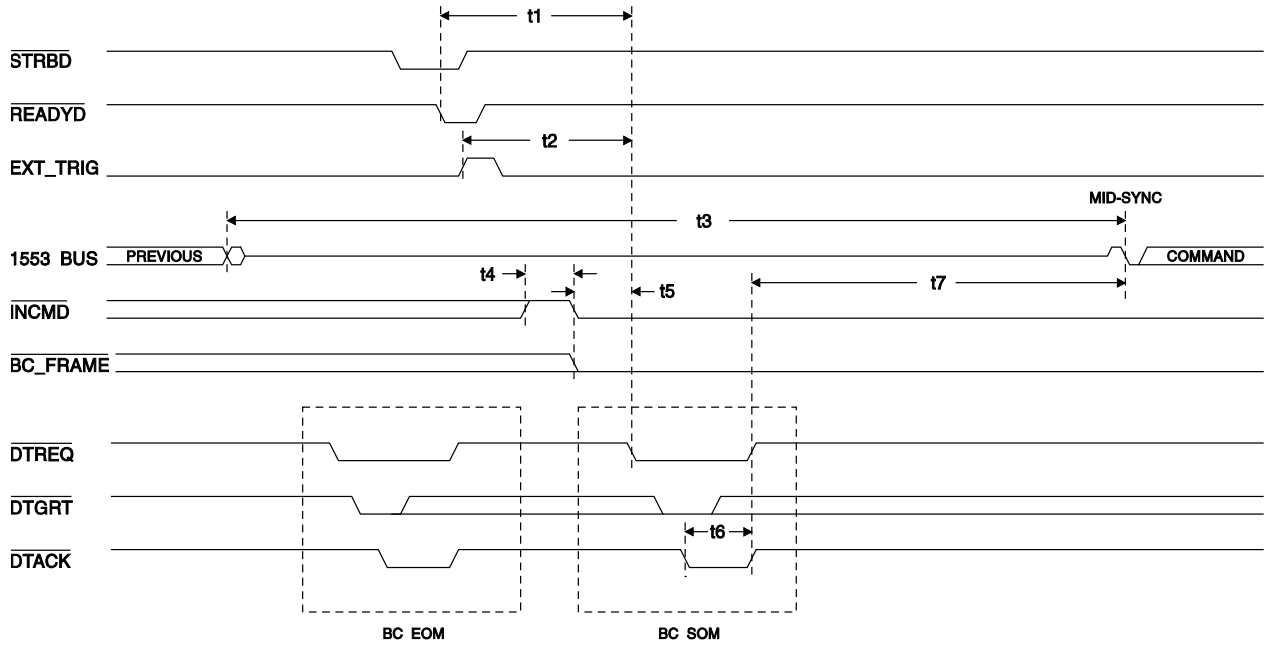


FIGURE 68. BC MODE START TIMING

NOTES for TABLE 134 and FIGURE 68.
1. Intermessage gap may be extended under software control. The message gap timer is assumed to be disabled.
2. Assumed DTREQ* is connected to DTGRT*, there is no CPU contention, and all transfers are to internal memory. For SP'ACE and SP'ACE II applications, subtract 4 clock cycles per transfer to external memory.

TABLE 135. BC START OF MESSAGE (SOM) SEQUENCE TIMING.								
BC START OF MESSAGE (SOM) SEQUENCE TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	DTREQ* falling delay DTGRT* low.			∞			∞	µs
t2	DTGRT* falling delay to DTACK* falling (@20 MHz).			102				ns
	DTGRT* falling delay to DTACK* falling (@16 MHz).			115			105	ns
	DTGRT* falling delay to DTACK* falling (@12 MHz).			135			125	ns
	DTGRT* falling delay to DTACK* falling (@10 MHz).			152				ns
t3	DTGRT* low hold time following DTACK* falling.	0			0			ns
t4	DTACK* falling delay to DTREQ* rising, DTACK* rising, and MEMENAOUT* rising (@20 MHz).		1.45					µs
	DTACK* falling delay to DTREQ* rising, DTACK* rising, and MEMENAOUT* rising (@16 MHz).		1.82			3.56		µs
	DTACK* falling delay to DTREQ* rising, DTACK* rising, and MEMENAOUT* rising (@12 MHz).		2.42			4.75		µs
	DTACK* falling delay to DTREQ* rising, DTACK* rising, and MEMENAOUT* rising (@10 MHz).		2.90					µs
t5	SOM* active low pulse width (@20 MHz).		50					ns
	SOM* active low pulse width (@16 MHz).		62.5			62.5		ns
	SOM* active low pulse width (@12 MHz).		83.3			83.3		ns
	SOM* active low pulse width (@10 MHz).		100					ns
t6	Data Bus (D15-D0) valid setup prior to SOM* rising.	60			20			ns
t7	Data Bus (D15-D0) valid hold time following SOM* rising.	60			30			ns
t8	DTACK* rising delay to mid-sync crossing of command word (@20 MHz)	1.70	1.80	2.0				µs
	DTACK* rising delay to mid-sync crossing of command word (@16 MHz)	1.82	1.9	2.05	1.82	1.9	2.05	µs
	DTACK* rising delay to mid-sync crossing of command word (@12 MHz)	1.90	1.98	2.14	1.90	1.98	2.14	µs
	DTACK* rising delay to mid-sync crossing of command word (@10 MHz)	1.95	2.05	2.25				µs

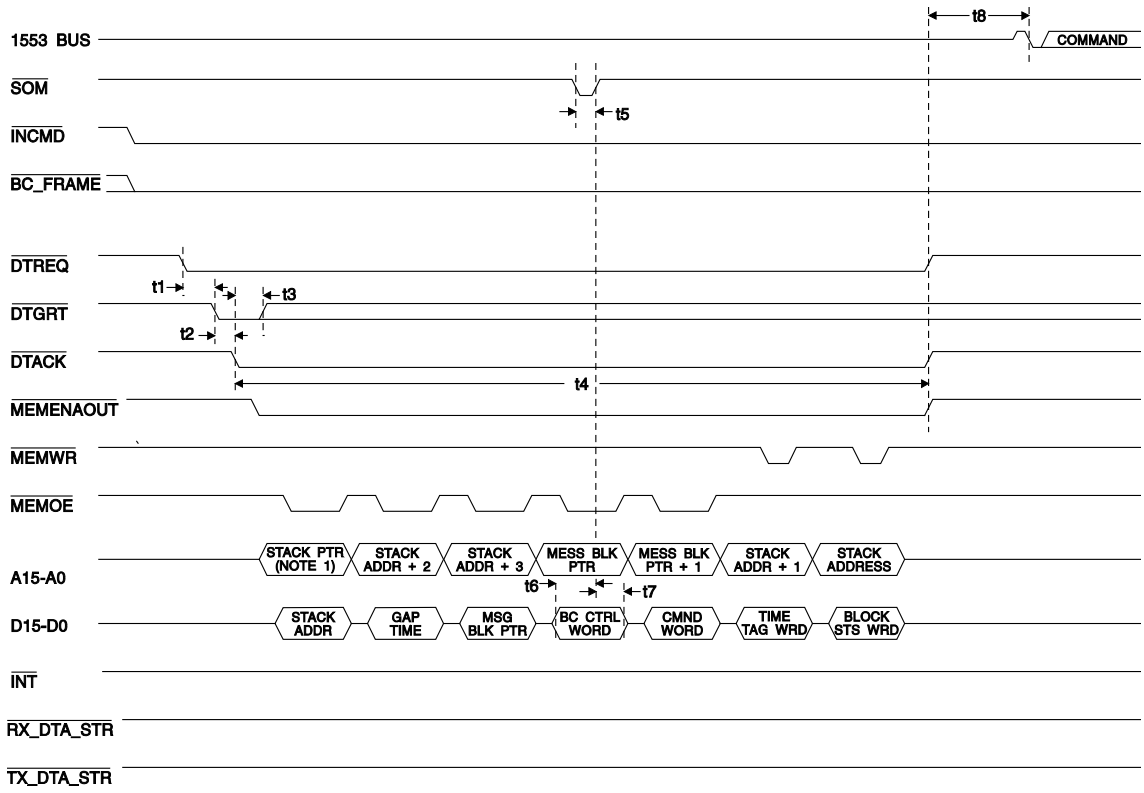


FIGURE 69. BC START OF MESSAGE (SOM) SEQUENCE TIMING

TABLE 136. BC END OF MESSAGE (EOM) SEQUENCE TIMING

BC END OF MESSAGE (EOM) SEQUENCE TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Mid-parity crossing of last word delay to DTREQ* falling (@20 MHz)	6.58	6.8	7.16				µs
	Mid-parity crossing of last word delay to DTREQ* falling (@16 MHz)	6.70	6.91	7.27	7.70	7.91	8.27	µs
	Mid-parity crossing of last word delay to DTREQ* falling (@12 MHz)	6.78	7.02	7.39	7.78	8.02	8.39	µs
	Mid-parity crossing of last word delay to DTREQ* falling (@10 MHz)	6.85	7.1	7.47				µs
t2	DTREQ* falling delay to DTGRT* falling							µs
t3	DTGRT* falling delay to DTACK* falling (@20 MHz)			102				ns
	DTGRT* falling delay to DTACK* falling (@16 MHz)			115			105	ns
	DTGRT* falling delay to DTACK* falling (@12 MHz)			135			125	ns
	DTGRT* falling delay to DTACK* falling (@10 MHz)			152				ns
t4	DTGRT* low hold time following DTACK* falling.	0			0			ns
t5	DTACK* falling delay to DTREQ* rising, DTACK* rising, and MEMENAOUT* rising (@20 MHz)		1.05					µs
	DTACK* falling delay to DTREQ* rising, DTACK* rising, and MEMENAOUT* rising (@16 MHz)		1.3125			2.563		µs
	DTACK* falling delay to DTREQ* rising, DTACK* rising, and MEMENAOUT* rising (@12 MHz)		1.75			3.417		µs
	DTACK* falling delay to DTREQ* rising, DTACK* rising, and MEMENAOUT* rising (@10 MHz)		2.10					µs
t6	DTACK* falling delay to INT* falling (@20 MHz) (Note 1)		1.00					µs
	DTACK* falling delay to INT* falling (@16 MHz) (Note 1)		1.25			2.5		µs
	DTACK* falling delay to INT* falling (@12 MHz) (Note 1)		1.66			3.33		µs
	DTACK* falling delay to INT* falling (@10 MHz) (Note 1)		2.00					µs
t7	INT* active low pulse width (Notes 1,2).		500			500		ns
t8	DTACK* rising delay to INCMD* rising (@20 MHz)		50.0					ns
	DTACK* rising delay to INCMD* rising (@16 MHz)		62.5			62.5		ns
	DTACK* rising delay to INCMD* rising (@12 MHz)		83.3			83.3		ns
	DTACK* rising delay to INCMD* rising (@10 MHz)		100.0					ns
t9	DTACK* rising delay to BC_FRAME* rising (@20 MHz)		100					ns
	DTACK* rising delay to BC_FRAME* rising (@16 MHz)		125			125		ns
	DTACK* rising delay to BC_FRAME* rising (@12 MHz)		166			166		ns
	DTACK* rising delay to BC_FRAME* rising (@10 MHz)		200					ns

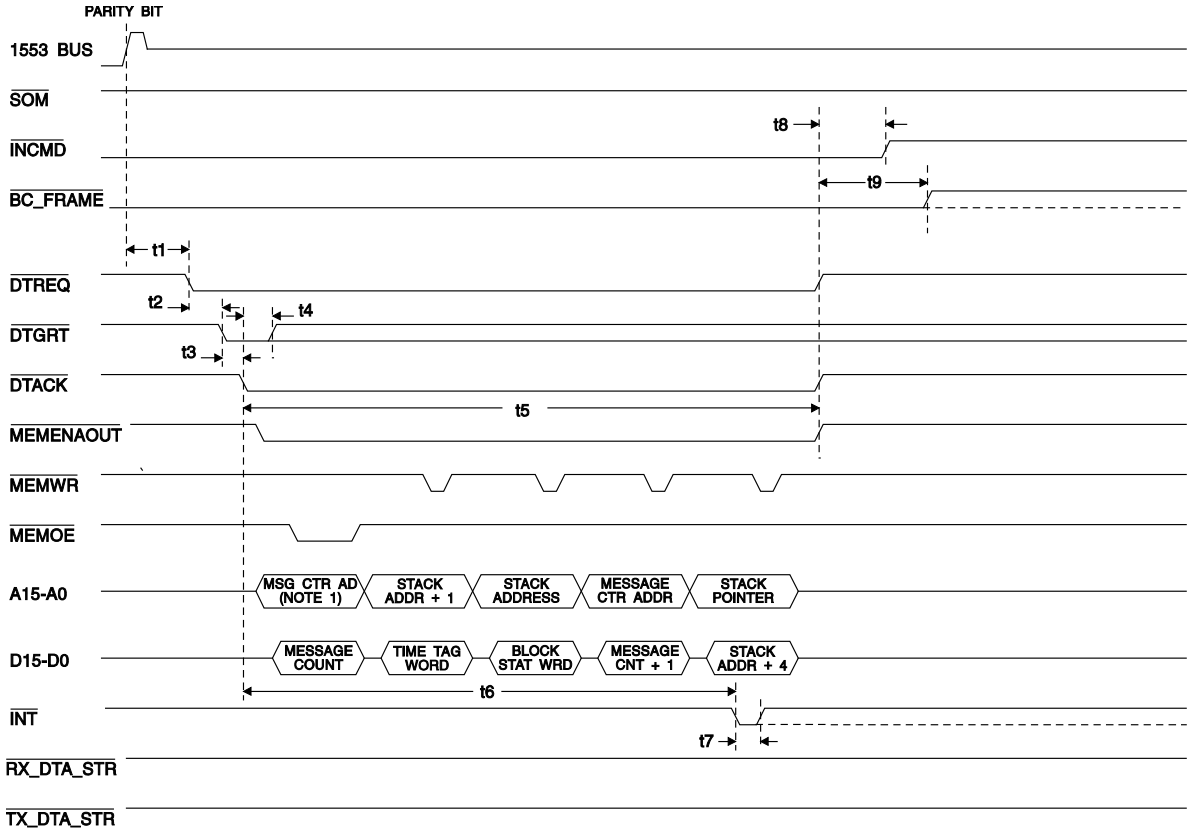


FIGURE 70. BC END OF MESSAGE (EOM) SEQUENCE TIMING

NOTES for TABLE 136 and FIGURE 70.
1. Assumes that the interrupt is enabled. Applies to all interrupts, which occur with the end of a message.
2. Interrupt output is software programmable for a pulse or level output. Pulse mode of operation is assumed.

TABLE 137. BC RETRY TIMING.								
BC RETRY TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1a	Mid-parity crossing delay to DTREQ* falling (Retry due to invalid word, incorrect sync, high word count or status address mismatch)	6.7	6.9	7.5	7.7	7.9	8.5	µs
t1b	Mid-parity crossing delay to DTREQ* falling (Retry due to no response or low word count) (programmable)	23		23.7	24		24.7	µs
t1c	DTREQ* rising to DTREQ* falling (Retry due to loop test fail on broadcast command)		2			2		clk
t2	DTREQ* falling delay to DTGRT* falling.			∞			∞	ns
t3	DTGRT* falling delay to DTACK* falling (@20 MHz)			102				ns
	DTGRT* falling delay to DTACK* falling (@16 MHz)			115			105	ns
	DTGRT* falling delay to DTACK* falling (@12 MHz)			135			125	ns
	DTGRT* falling delay to DTACK* falling (@10 MHz)			152				ns
t4	DTGRT* low hold time following DTACK* falling.	0			0			ns
t5	DTACK* falling delay to DTREQ* rising, DTACK* rising, and MEMENAOUT* rising (@20 MHz)		0.650					µs
	DTACK* falling delay to DTREQ* rising, DTACK* rising, and MEMENAOUT* rising (@16 MHz)		0.812			1.562		µs
	DTACK* falling delay to DTREQ* rising, DTACK* rising, and MEMENAOUT* rising (@12 MHz)		1.083			2.083		µs
	DTACK* falling delay to DTREQ* rising, DTACK* rising, and MEMENAOUT* rising (@10 MHz)		1.300					µs
t6	DTACK* rising delay to mid-sync crossing of command word (@20 MHz)	1.70	1.80	2.0				µs
	DTACK* rising delay to mid-sync crossing of command word (@16 MHz)	1.82	1.9	2.05	1.82	1.9	2.05	µs
	DTACK* rising delay to mid-sync crossing of command word (@12 MHz)	1.90	1.98	2.14	1.90	1.98	2.14	µs
	DTACK* rising delay to mid-sync crossing of command word (@10 MHz)	1.95	2.05	2.25				µs

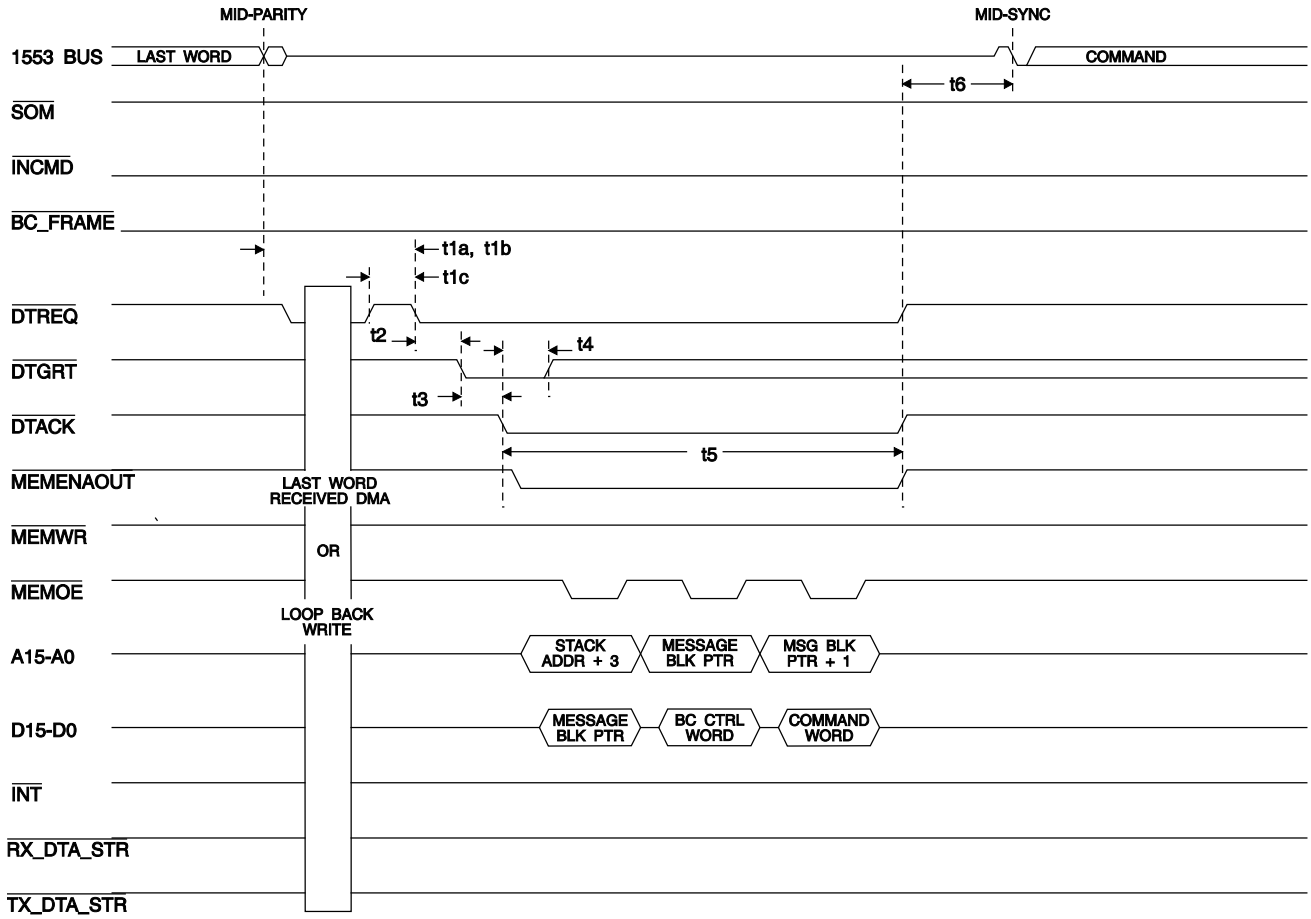


FIGURE 71. BC RETRY TIMING

NOTES For TABLE 137 and FIGURE 71.
1. Time based on default no response timeout program (18.5 µs typ.). For ACE/Mini-ACE products, add 5.3 µs to typical value, for SP'ACE and SP'ACE II add 6.3 µs.
2. Last word received applicable to t1A timings and loop back write applicable to t1B and t1C timings.

9.5 RT OPERATION

FIGURE 72 through FIGURE 76 illustrate the overall RT message sequence timing for receive, transmit, and broadcast message formats. FIGURE 75 and FIGURE 76 illustrate the RT Start Of Message Sequence and the End Of Message Sequence. The Start Of Message output signal (SOM*) is driven low during the SOM sequence at the time when the received command word is driven onto the data bus (D15-D0). The timing of the SOM* signal matches the timing of the write strobe (MEMWR*) and such can be used to externally latch the command word. Note also the that 1553 status bits are latched internally on the rising edge of the SOM* pulse (SSFLAG* is the only status bit which is driven from an external source).

During the RT SOM sequence several optional transfers are shown as dashed lines. The illegalization table is only accessed if command illegalization is enabled (bit 7 in configuration register #3 set to logic 0). A read of the busy bit table (transfer #3 in the SOM) only occurs if the busy bit lookup feature is enabled (bit 13 in configuration register #2 set to logic 1). The subaddress control word (SOM transfer #4) will only occur if enhanced RT memory management is enabled (bit 1 in configuration register #2 is set to logic 1) and the command is not a mode code or enhanced mode code handling is not enabled (bit 0 of configuration register #3 set to logic 0). The data block pointer is read (SOM transfer #5) for all commands except any mode code if enhanced mode code handling is enabled (bit 0 of configuration register #3 set to logic 1). If such is the case, the mode code interrupt look-up table will be read.

The RT EOM sequence also contains several optional transfers. The subaddress control word is re-read if enhanced RT memory management is enabled (bit 1 in configuration register #2 is set to logic 1) and the command is to receive data to a block address and the double buffering feature is enabled (bit 12 of configuration register #2 is set to logic 1). The data block address is re-read from the lookup table (EOM transfer #2) if subaddress double buffering is enabled and the command is to receive data to a block address. A write of a single data word to the third location on the descriptor stack (EOM transfer #2) will occur if the current message is a mode code with data and enhanced mode code handling is enabled (bit 0 of configuration register #3 set to logic 1). A write to the subaddress data pointer will occur if the data pointer has to be updated either because double-buffering was enabled or the stack address must be updated.

TABLE 138. RT RECEIVE MESSAGE TIMING

RT RECEIVE MESSAGE TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Mid-parity crossing of received command word to RT Address and RT Address Parity sampled.	500	800	1100	500	800	1100	ns
t2	RT Address and RT Address Parity setup prior to sampling.	500			500			ns
t3	RT Address and RT Address Parity hold time following sampling.	500			500			ns
t4	Mid-parity crossing of received command word to DTREQ* falling edge (requesting RT Start Of Message transfer) (@20 MHz) (Note 1)	1.10	1.39	1.75				µs
	Mid-parity crossing of received command word to DTREQ* falling edge (requesting RT Start Of Message transfer) (@16 MHz) (Note 1)	1.26	1.49	1.83	1.26	1.49	1.83	µs
	Mid-parity crossing of received command word to DTREQ* falling edge (requesting RT Start Of Message transfer) (@12 MHz) (Note 1)	1.44	1.60	2.06	1.44	1.60	2.06	µs
	Mid-parity crossing of received command word to DTREQ* falling edge (requesting RT Start Of Message transfer) (@10 MHz) (Note 1)	1.49	1.69	2.15				µs
t5	Mid-parity crossing of received data word to DTREQ* falling edge (requesting data word write transfer) (@20 MHz)	1.12	1.35	1.68				µs
	Mid-parity crossing of received data word to DTREQ* falling edge (requesting data word write transfer) (@16 MHz)	1.20	1.43	1.77	1.20	1.43	1.77	µs
	Mid-parity crossing of received data word to DTREQ* falling edge (requesting data word write transfer) (@12 MHz)	1.36	1.52	1.98	1.36	1.52	1.98	µs
	Mid-parity crossing of received data word to DTREQ* falling edge (requesting data word write transfer) (@10 MHz)	1.42	1.60	2.05				µs
t6	RT response time (6.9 s max if buffered or DTGRT* applied with 1 sec for SP'ACE or 2 sec for ACE)	5.9	6.3	9.4	5.9	6.3	10.4	µs
t7	Mid-parity crossing of RT status word to DTREQ* falling edge (requesting RT End Of Message transfer).	2.8		3.2	2.8		3.2	µs

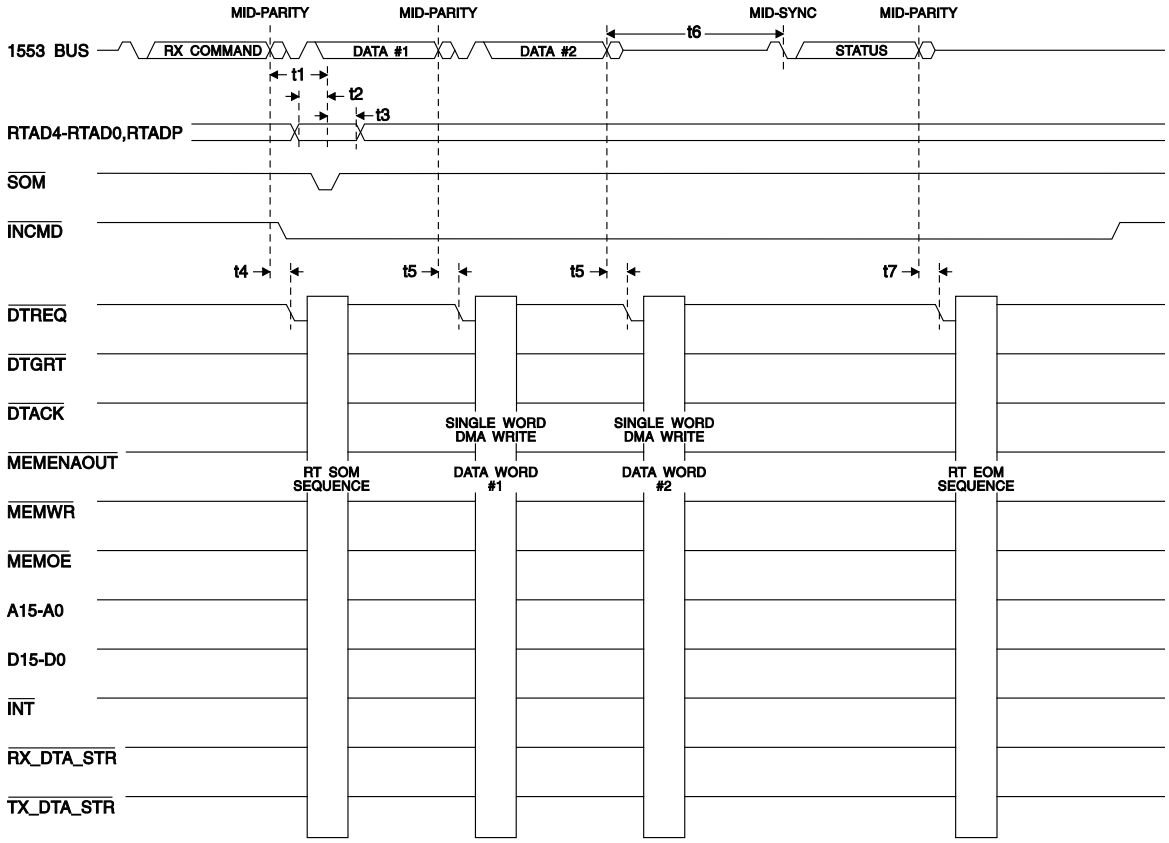


FIGURE 72. RT RECEIVE MESSAGE TIMING

NOTES for TABLE 138 and FIGURE 72.

1. If superseding command, max time can increase by 5 clk cycles for ACE/Mini-ACE and 9 clk cycles for SP'ACE and SP'ACE II.

TABLE 139. RT TRANSMIT MESSAGE TIMING								
RT TRANSMIT MESSAGE TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	RT Response time (6.9 µs max if buffered or DTGRT* applied within 1 µsec for SP'ACE or 2 µsec for ACE)	5.9	6.3	9.4	5.9	6.3	10.4	µs
t2	Mid-parity crossing of received command word to RT Address and RT Address Parity sampled.	500	800	1100	500	800	1100	ns
t3	RT Address and RT Address Parity setup prior to sampling.	500			500			ns
t4	RT Address and RT Address Parity hold time following sampling.	500			500			ns
t5	Mid-parity crossing of received command word to DTREQ* falling edge (requesting RT Start Of Message transfer).	1.25		2.1	1.25		2.1	µs
t6	Mid-sync crossing of current transmitting word to DTREQ* falling edge (requesting data word read transfer of next word to be transmitted).	1.2		1.6	1.2		1.6	µs
t7	Mid-parity crossing of last transmitted word to DTREQ* falling edge (requesting RT End Of Message transfer).	2.8		3.2	2.8		3.2	µs

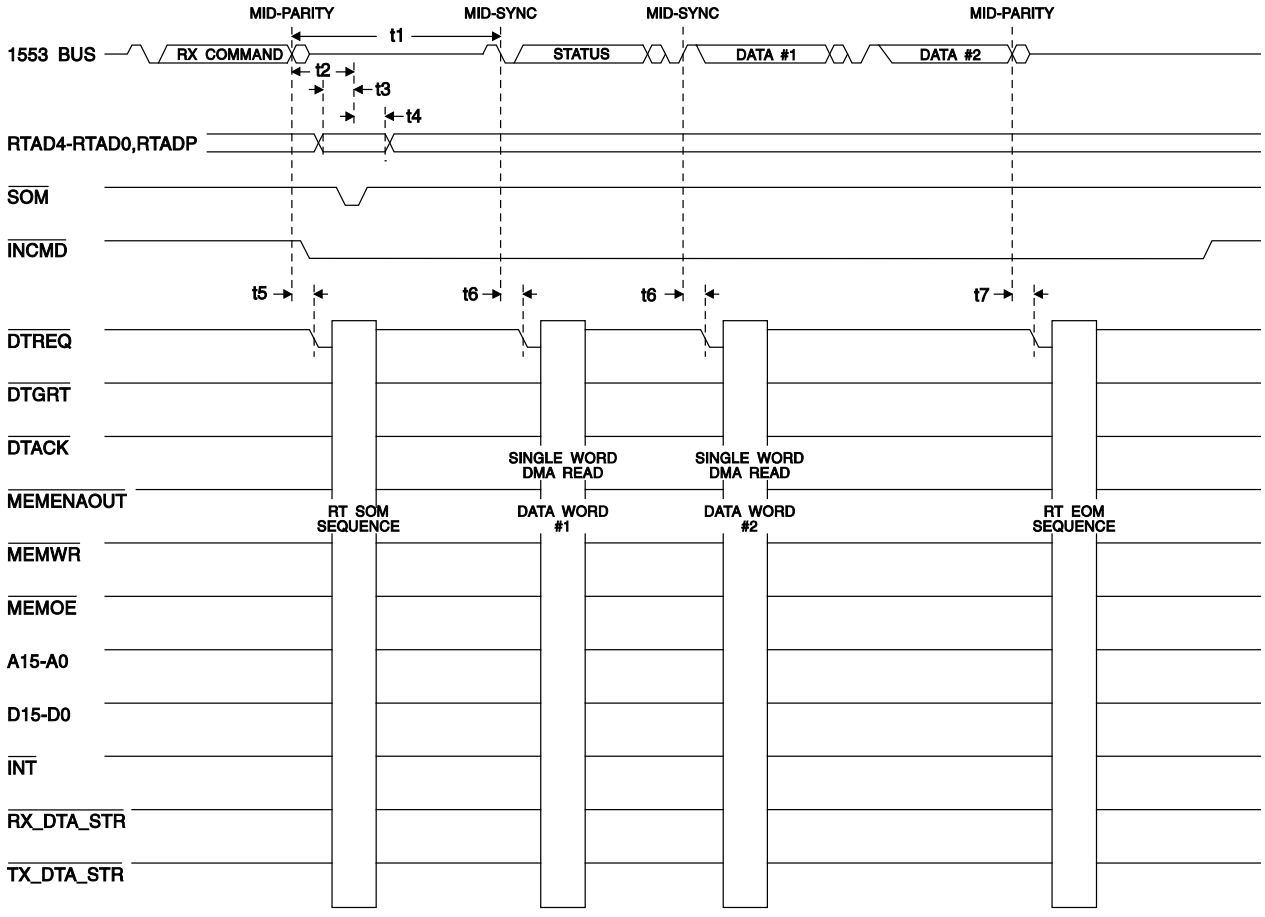


FIGURE 73. RT TRANSMIT MESSAGE TIMING

NOTES For TABLE 139 and FIGURE 73.
1. In the event SOM sequence stretches into first DMA read cycle, DTREQ* will fall 1 clk cycle after DTREQ* rises.

TABLE 140. RT BROADCAST RECEIVE MESSAGE TIMING.								
RT BROADCAST RECEIVE MESSAGE TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Mid-parity crossing of received command word to RT Address and RT Address Parity sampled.	500	800	1100	500	800	1100	ns
t2	RT Address and RT Address Parity setup prior to sampling.	500			500			ns
t3	RT Address and RT Address Parity hold time following sampling.	500			500			ns
t4	Mid-parity crossing of received command word to DTREQ* falling edge (requesting RT Start Of Message transfer).	1.25		2.1	1.25		2.1	µs
t5	Mid-parity crossing of received data word to DTREQ* falling edge (requesting data word write transfer).	1.2		2.0	1.2		2.0	µs
t6	Mid-parity crossing of last received data word to DTREQ* falling edge (requesting RT End Of Message transfer).	6.7		7.4	7.7		8.4	µs

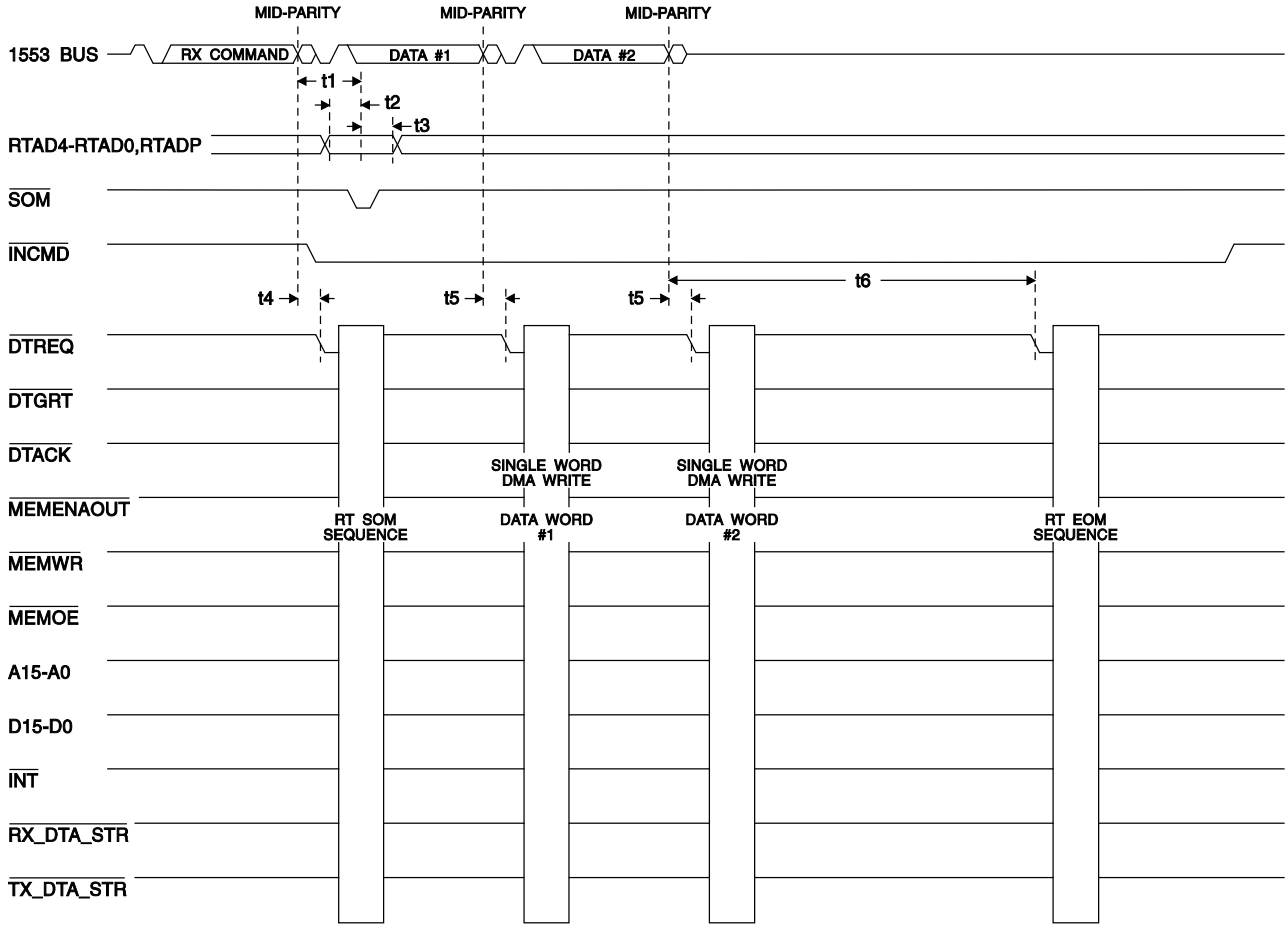


FIGURE 74. RT BROADCAST RECEIVE MESSAGE TIMING

TABLE 141. RT START OF MESSAGE TIMING.								
RT START OF MESSAGE TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Mid-parity crossing of received command word delay to INCMD* falling edge.	1.2		2.0	1.2		2.0	µs
t2	Mid-parity crossing of received command word delay to DTREQ* falling edge (requesting RT Start Of Message transfer sequence).	1.25		2.1	1.25		2.1	µs
t3	DTREQ* falling edge delay to DTGRT* falling edge (@20 MHz) (Note 1)			4.5				µs
	DTREQ* falling edge delay to DTGRT* falling edge (@16 MHz) (Note 1)			4.0			4.0	µs
	DTREQ* falling edge delay to DTGRT* falling edge (@12 MHz) (Note 1)			3.5			3.5	µs
	DTREQ* falling edge delay to DTGRT* falling edge (@10 MHz) (Note 1)			3.1				µs
t4	DTGRT* falling edge delay to DTACK* falling edge (@20 MHz)			102				ns
	DTGRT* falling edge delay to DTACK* falling edge (@16 MHz)			115			105	ns
	DTGRT* falling edge delay to DTACK* falling edge (@12 MHz)			135			125	ns
	DTGRT* falling edge delay to DTACK* falling edge (@10 MHz)			152				ns
t5	DTGRT* low hold time following DTACK* falling edge.	0			0			ns
t6	DTACK* falling edge delay to MEMENAOUT* rising edge, DTREQ* rising edge, and DTACK* rising edge (@20 MHz)	1.42		2.08				µs
	DTACK* falling edge delay to MEMENAOUT* rising edge, DTREQ* rising edge, and DTACK* rising edge (@16 MHz)	1.78		2.59	3.53		5.09	µs
	DTACK* falling edge delay to MEMENAOUT* rising edge, DTREQ* rising edge, and DTACK* rising edge (@12 MHz)	2.38		3.45	4.72		6.78	µs
	DTACK* falling edge delay to MEMENAOUT* rising edge, DTREQ* rising edge, and DTACK* rising edge (@10 MHz)	2.85		4.15				µs
t7	Status word inputs (SSFLAG*) valid setup time prior to SOM* rising edge.	40			40			ns
t8	Status word inputs (SSFLAG*) valid hold time following SOM* rising edge.	10			10			ns

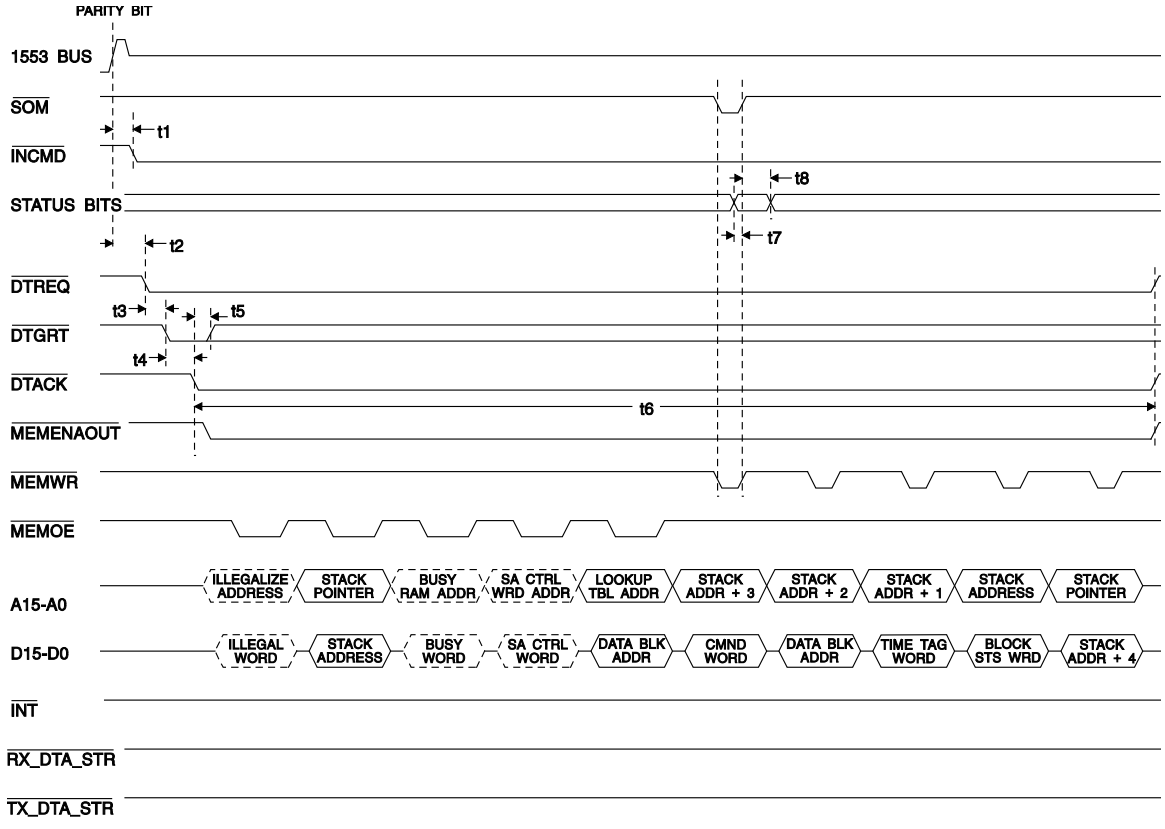


FIGURE 75. RT START OF MESSAGE TIMING

NOTES For TABLE 141 and FIGURE 75.
1. If maximum allowable request to grant time is exceeded, a handshake fail condition will occur. A handshake fail on the RT Start of Message sequence will cause the ACE/Mini-ACE to not respond to the current command.

TABLE 142. RT END OF MESSAGE TIMING.								
RT END OF MESSAGE TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Mid-parity crossing of last transmitted word delay to DTREQ* falling edge (requesting RT End Of Message transfer sequence).	2.8		3.2	2.8		3.2	µs
t2	DTREQ* falling edge delay to DTGRT* falling edge (Note 1).							ns
t3	DTGRT* falling edge delay to DTACK* falling edge (@20 MHz)			102				ns
	DTGRT* falling edge delay to DTACK* falling edge (@16 MHz)			115			105	ns
	DTGRT* falling edge delay to DTACK* falling edge (@12 MHz)			135			125	ns
	DTGRT* falling edge delay to DTACK* falling edge (@10 MHz)			152				ns
t4	DTGRT* low hold time following DTACK* falling edge.	0			0			ns
t5	DTACK* falling edge delay to MEMENAOUT* rising edge, DTREQ* rising edge, and DTACK* rising edge (@20 MHz)	0.43		1.07				µs
	DTACK* falling edge delay to MEMENAOUT* rising edge, DTREQ* rising edge, and DTACK* rising edge (@16 MHz)	0.53		1.34	1.03		2.59	µs
	DTACK* falling edge delay to MEMENAOUT* rising edge, DTREQ* rising edge, and DTACK* rising edge (@12 MHz)	0.72		1.78	1.39		3.45	µs
	DTACK* falling edge delay to MEMENAOUT* rising edge, DTREQ* rising edge, and DTACK* rising edge (@10 MHz)	0.96		2.03				µs
t6	INT* falling prior to DTACK* rising		1			5		clk
t7	INT* low pulse width (note 2).		500			500		ns
t8	MEMENAOUT* rising edge, DTREQ* rising edge, and DTACK* rising edge delay to INCMD rising edge.		2			2		clk

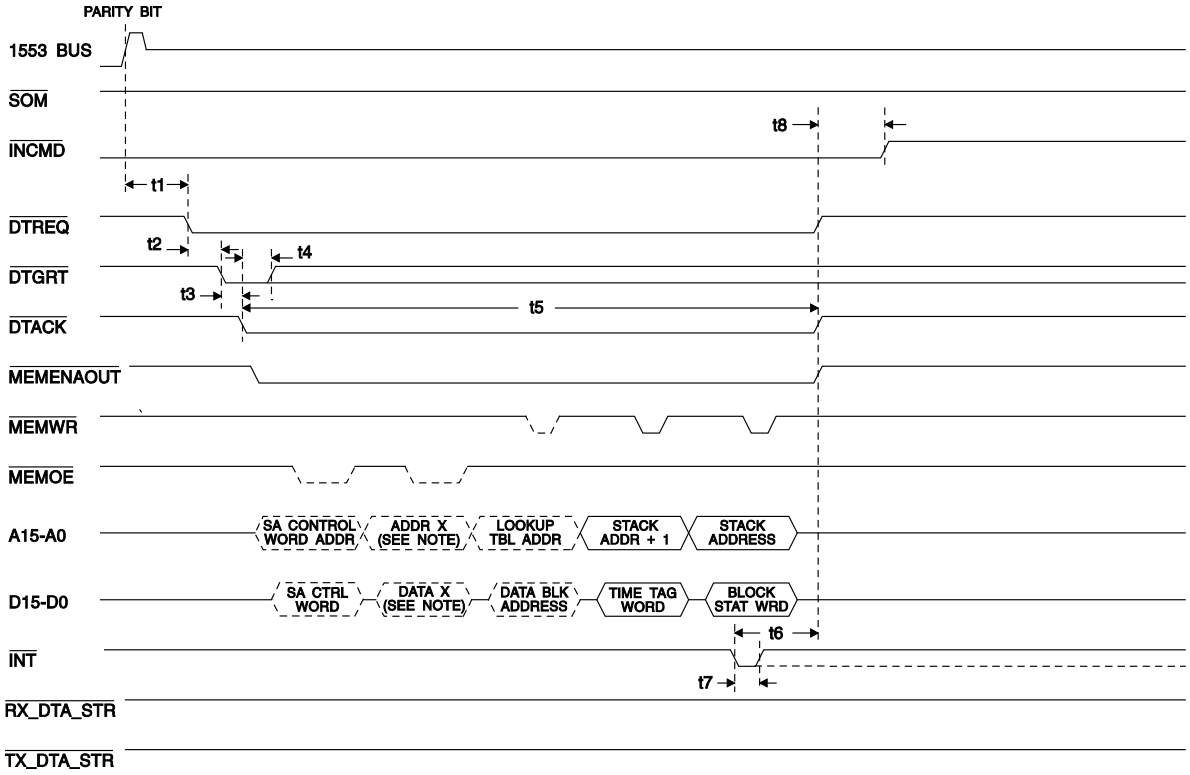


FIGURE 76. RT END OF MESSAGE TIMING

NOTES For TABLE 142 and FIGURE 76.
1. If maximum allowable request to grant time is exceeded, a handshake fail condition will occur. A handshake fail on the RT End of Message sequence will have no effect on 1553 message transfers.
2. Assumes that the interrupt request mode is set to pulse mode (bit 3 of configuration register #2 is set to logic "1").

9.6 MESSAGE MT OPERATION

FIGURE 77 through FIGURE 82 illustrate the overall MT message sequence timing for receive, transmit, and broadcast message formats. FIGURE 80 illustrates the timing sequence for a message in which the command word is not enabled in the ACE/Mini-ACE's monitor selection lookup table. The ACE/Mini-ACE will begin a normal Start Of Message, beginning with a read of the monitor lookup table, if the command is not selected in the lookup table, the ACE/Mini-ACE will abort the SOM sequence. By the time the ACE/Mini-ACE aborts the sequence, a read of the monitor command stack pointer has begun, so the ACE/Mini-ACE will finish the read cycle and abort immediately there after.

FIGURE 81 illustrates the Message Monitor Start Of Message (SOM) sequence. FIGURE 82 illustrates the Message Monitor End Of Message (EOM) sequence.

TABLE 143. MESSAGE MT RECEIVE MESSAGE TIMING

MESSAGE MT RECEIVE MESSAGE TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Mid-parity crossing of received command word to DTREQ* falling edge (requesting Message MT Start Of Message transfer).	1.25		2.10	1.25		2.10	µs
t2	Mid-parity crossing of received data word to DTREQ* falling edge (requesting data word write transfer).	1.2		2.0	1.2		2.0	µs
t3	RT no response timeout (note 1).			17.5			17.5	µs
t4	Mid-parity crossing of received status word to DTREQ* falling edge (requesting status word write transfer).	1.2		2.0	1.2		2.0	µs
t5	Mid-parity crossing of RT status word to DTREQ* falling edge (requesting Message MT End Of Message transfer).	6.7		7.4	7.7		8.4	µs

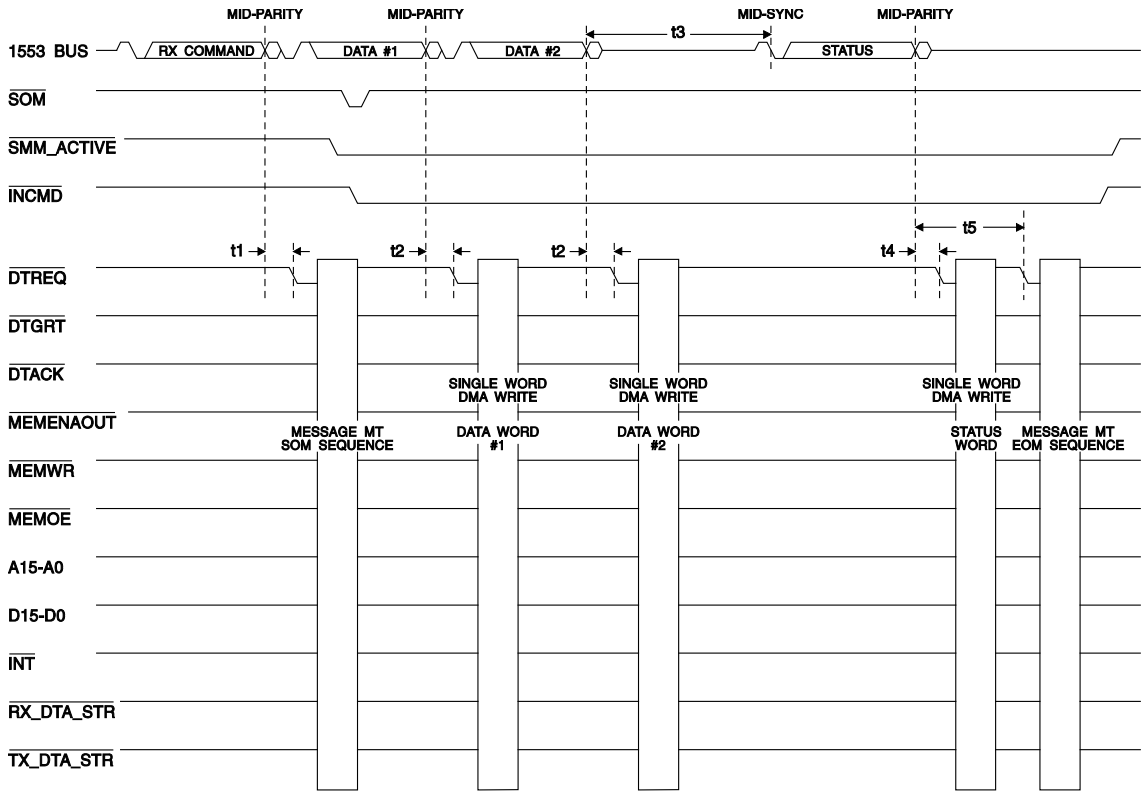


FIGURE 77. MESSAGE MT RECEIVE MESSAGE TIMING

NOTES for TABLE 143 and FIGURE 77.

1. Response timeout is programmable. Assumes default response timeout value is programmed. If a status response is not received with the response time period, a response timeout condition will be flagged and the ACE/Mini-ACE will begin looking for new command words.

TABLE 144. MESSAGE MT TRANSMIT MESSAGE TIMING								
MESSAGE MT TRANSMIT MESSAGE TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	RT no response timeout (Note 1).			17.5			17.5	µs
t2	Mid-parity crossing of transmit command word to DTREQ* falling edge (requesting Message MT Start Of Message transfer).	1.25		2.10	1.25		2.10	µs
t3	Mid-parity crossing of received status word to DTREQ* falling edge (requesting status word write transfer).	1.2		2.0	1.2		2.0	µs
t4	Mid-parity crossing of received data word to DTREQ* falling edge (requesting data word write transfer).	1.2		2.0	1.2		2.0	µs
t5	Mid-parity crossing of last transmitted data word to DTREQ* falling edge (requesting Message MT End Of Message transfer).	6.7		7.4	7.7		8.4	µs

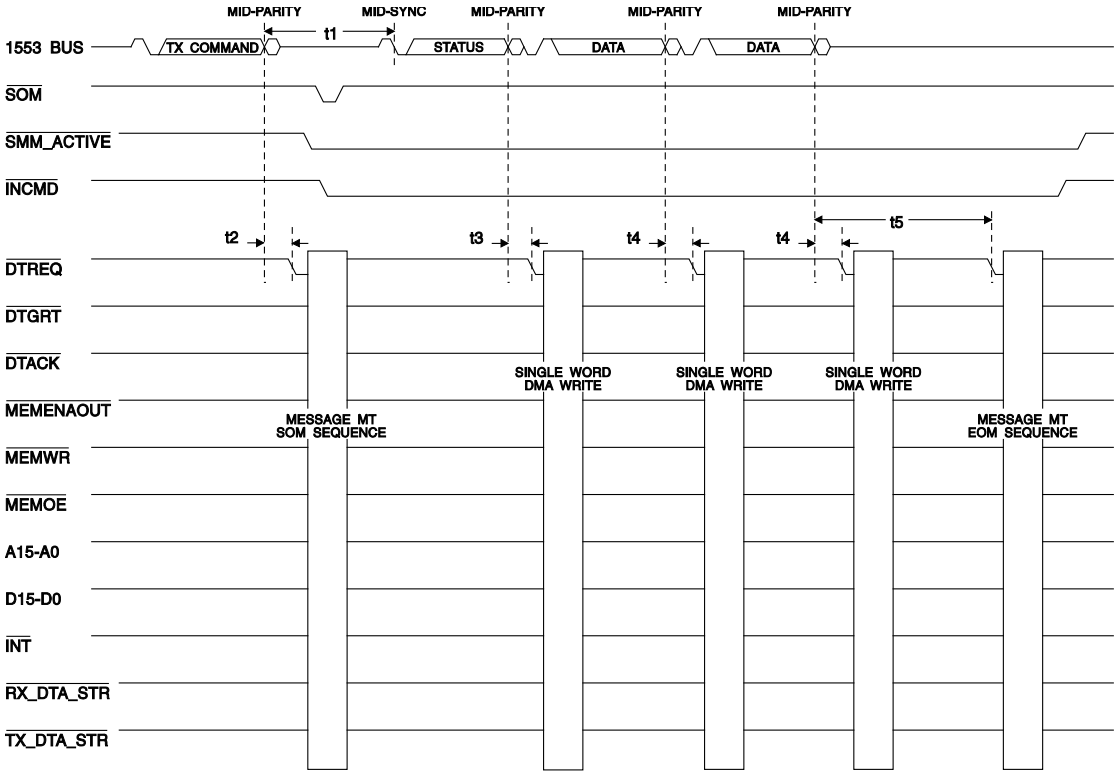


FIGURE 78. MESSAGE MT TRANSMIT MESSAGE TIMING

NOTES for TABLE 144. and FIGURE 78.
1. Response timeout is programmable. Assumes default response timeout value is programmed. If a status response is not received with the response time period, a response timeout condition will be flagged and the ACE/Mini-ACE will begin looking for new command words.

TABLE 145. MESSAGE MT BROADCAST RECEIVE MESSAGE TIMING								
MESSAGE MT BROADCAST RECEIVE MESSAGE TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Mid-parity crossing of received command word to DTREQ* falling edge (requesting Message MT Start Of Message transfer).	1.25		2.10	1.25		2.10	µs
t2	Mid-parity crossing of received data word to DTREQ* falling edge (requesting data word write transfer).	1.2		2.0	1.2		2.0	µs
t3	Mid-parity crossing of last data word to DTREQ* falling edge (requesting Message MT End Of Message transfer).	6.7		7.4	7.7		8.4	µs

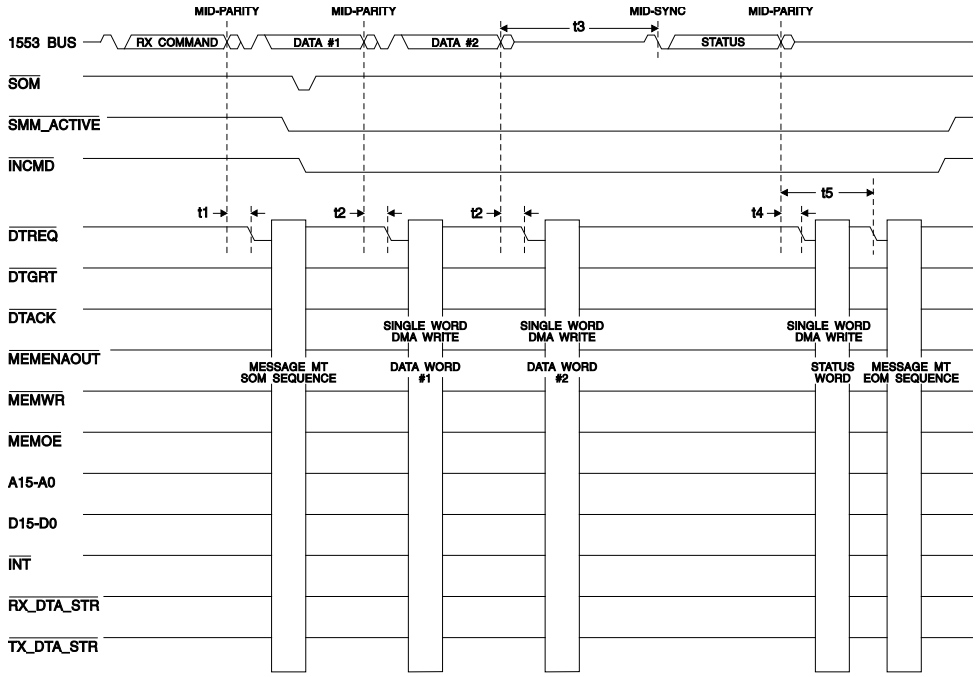


FIGURE 79. MESSAGE MT BROADCAST RECEIVE MESSAGE TIMING

TABLE 146. MESSAGE MT COMMAND NOT SELECTED TIMING

MESSAGE MT COMMAND NOT SELECTED TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Mid-parity crossing of received command word delay to DTREQ* falling edge (requesting Message MT Start Of Message transfer sequence).	1.25		2.10	1.25		2.10	µs
t2	DTREQ* falling edge delay to DTGRT* falling edge (@20 MHz) (Note 1)			4.5				µs
	DTREQ* falling edge delay to DTGRT* falling edge (@16 MHz) (Note 1)			4.0			4.0	µs
	DTREQ* falling edge delay to DTGRT* falling edge (@12 MHz) (Note 1)			3.5			3.5	µs
	DTREQ* falling edge delay to DTGRT* falling edge (@10 MHz) (Note 1)			3.1				µs
t3	DTGRT* falling edge delay to DTACK* falling edge (@20 MHz)			102				ns
	DTGRT* falling edge delay to DTACK* falling edge (@16 MHz)			115			105	ns
	DTGRT* falling edge delay to DTACK* falling edge (@12 MHz)			135			125	ns
	DTGRT* falling edge delay to DTACK* falling edge (@10 MHz)			152				ns
t4	DTGRT* low hold time following DTACK* falling edge.	0			0			ns
t5	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@20 MHz)	0.42	0.45	0.48				µs
	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@16 MHz)	0.53	0.56	0.59	1.03	1.06	1.09	µs
	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@12 MHz)	0.72	0.75	0.78	1.39	1.42	1.45	µs
	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@10 MHz)	0.87	0.90	0.93				µs
t6	Mid-parity crossing of receive command word to SMM_ACTIVE* falling edge (@20 MHz)	0.82	1.000	1.450				µs
	Mid-parity crossing of receive command word to SMM_ACTIVE* falling edge (@16 MHz)	1.01	1.140	1.580	1.01	1.140	1.580	µs
	Mid-parity crossing of receive command word to SMM_ACTIVE* falling edge (@12 MHz)	1.11	1.370	1.720	1.11	1.370	1.720	µs
	Mid-parity crossing of receive command word to SMM_ACTIVE* falling edge (@10 MHz)	1.27	1.550	1.830				µs
t7	DTACK* rising edge delay to SMM_ACTIVE* rising edge		2			2		clk

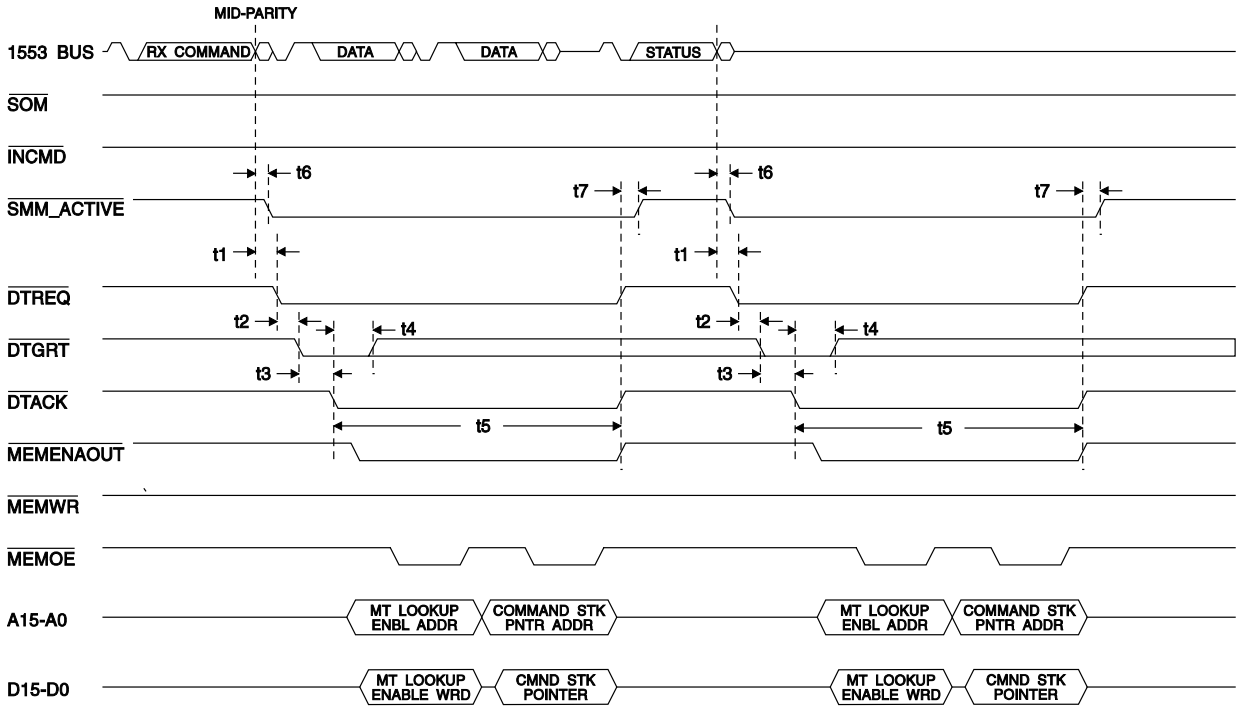


FIGURE 80. MESSAGE MT COMMAND NOT SELECTED TIMING

NOTES for TABLE 146 and FIGURE 80.
1. If maximum allowable request to grant time is exceeded, a handshake fail condition will occur. A handshake fail on the MT Start of Message sequence will cause the ACE/Mini-ACE to ignore the current command.

TABLE 147. MESSAGE MT START OF MESSAGE TIMING

MESSAGE MT START OF MESSAGE TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Mid-parity crossing of received command word delay to DTREQ* falling edge (requesting Message MT Start Of Message transfer sequence).	1.25		2.10	1.25		2.10	µs
t2	DTREQ* falling edge delay to DTGRT* falling edge (@20 MHz) (Note 1)			4.5				µs
	DTREQ* falling edge delay to DTGRT* falling edge (@16 MHz) (Note 1)			4.0			4.0	µs
	DTREQ* falling edge delay to DTGRT* falling edge (@12 MHz) (Note 1)			3.5			3.5	µs
	DTREQ* falling edge delay to DTGRT* falling edge (@10 MHz) (Note 1)			3.1				µs
t3	DTGRT* falling edge delay to DTACK* falling edge (@20 MHz)			102				ns
	DTGRT* falling edge delay to DTACK* falling edge (@16 MHz)			115			105	ns
	DTGRT* falling edge delay to DTACK* falling edge (@12 MHz)			135			125	ns
	DTGRT* falling edge delay to DTACK* falling edge (@10 MHz)			152				ns
t4	DTGRT* low hold time following DTACK* falling edge.	0			0			ns
t5	DTACK* falling edge delay to SOM* falling edge (@20 MHz)	720	750	780				ns
	DTACK* falling edge delay to SOM* falling edge (@16 MHz)	910	940	970	1660	1690	1720	ns
	DTACK* falling edge delay to SOM* falling edge (@12 MHz)	1220	1250	1280	2220	2250	2280	ns
	DTACK* falling edge delay to SOM* falling edge (@10 MHz)	1470	1500	1530				ns
t6	SOM* low pulse width (@20 MHz)	35	50	65				ns
	SOM* low pulse width (@16 MHz)	45	62.5	80	45	62.5	80	ns
	SOM* low pulse width (@12 MHz)	65	83.3	100	65	83.3	100	ns
	SOM* low pulse width (@10 MHz)	80	100	120				ns
t7	Mid-parity crossing of receive command word to SMM_ACTIVE* falling edge (@20 MHz)	0.82	1.000	1.450				µs
	Mid-parity crossing of receive command word to SMM_ACTIVE* falling edge (@16 MHz)	1.01	1.140	1.580	1.01	1.140	1.580	µs
	Mid-parity crossing of receive command word to SMM_ACTIVE* falling edge (@12 MHz)	1.11	1.370	1.720	1.11	1.370	1.720	µs
	Mid-parity crossing of receive command word to SMM_ACTIVE* falling edge (@10 MHz)	1.270	1.550	1.830				µs
t8	DTACK* falling edge delay to INCMD* falling edge (@20 MHz)	370	400	430				ns
	DTACK* falling edge delay to INCMD* falling edge (@16 MHz)	470	500	530	970	1000	1030	ns
	DTACK* falling edge delay to INCMD* falling edge (@12 MHz)	635	666	695	1300	1333	1360	ns
	DTACK* falling edge delay to INCMD* falling edge (@10 MHz)	770	800	830				ns
t9	DTACK* falling edge delay to DTREQ* rising edge and DTACK* rising edge (@20 MHz)	1.62	1.65	1.68				µs
	DTACK* falling edge delay to DTREQ* rising edge and DTACK* rising edge (@16 MHz)	2.03	2.06	2.09	4.03	4.06	4.09	µs
	DTACK* falling edge delay to DTREQ* rising edge and DTACK* rising edge (@12 MHz)	2.72	2.75	2.78	5.39	5.42	5.45	µs
	DTACK* falling edge delay to DTREQ* rising edge and DTACK* rising edge (@10 MHz)	3.27	3.30	3.33				µs

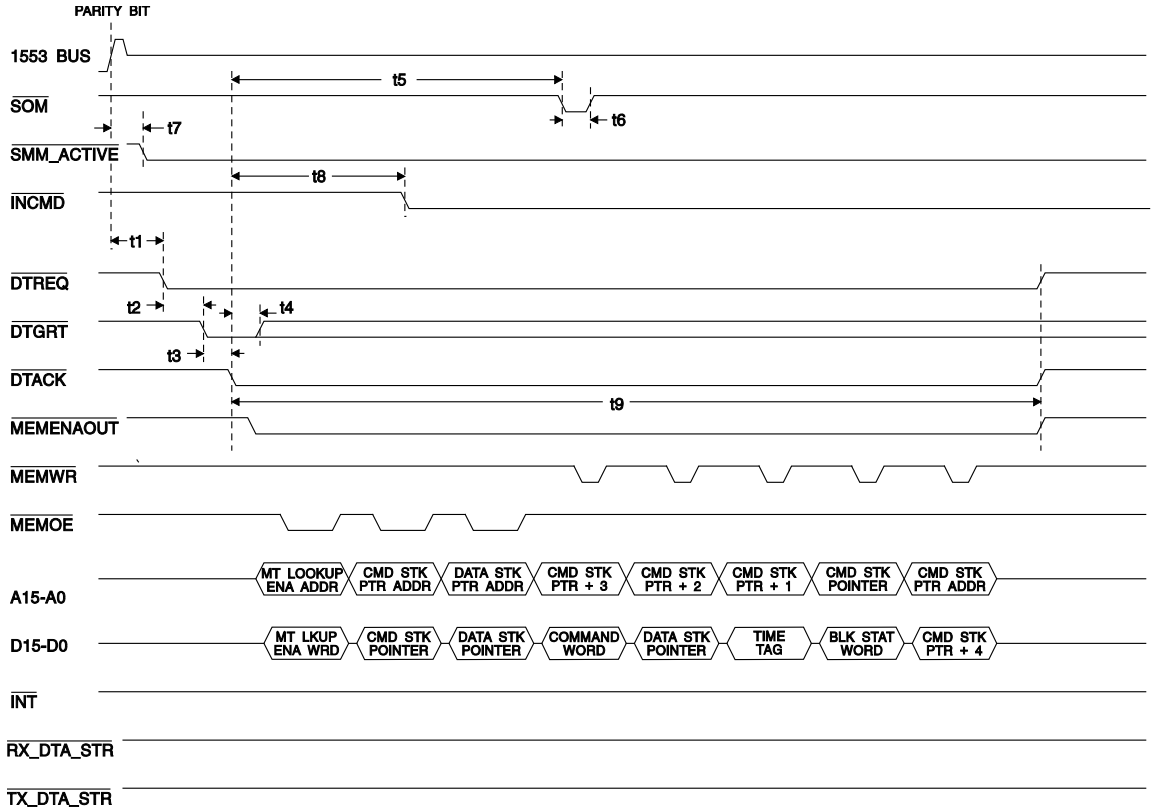


FIGURE 81. MESSAGE MT START OF MESSAGE TIMING

NOTES For TABLE 147 and FIGURE 81.

1. If maximum allowable request to grant time is exceeded, a handshake fail condition will occur. A handshake fail on the MT Start of Message sequence will cause the ACE/Mini-ACE to ignore the current command.

TABLE 148. MESSAGE MT END OF MESSAGE TIMING

MESSAGE MT END OF MESSAGE TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Mid-parity crossing of last word in message delay to DTREQ* falling edge (requesting Message MT End Of Message transfer sequence).	6.7		7.4	7.7		8.4	µs
t2	DTREQ* falling edge delay to DTGRT* falling edge (Note 1).							ns
t3	DTGRT* falling edge delay to DTACK* falling edge (@20 MHz)			102				ns
	DTGRT* falling edge delay to DTACK* falling edge (@16 MHz)			115			105	ns
	DTGRT* falling edge delay to DTACK* falling edge (@12 MHz)			135			125	ns
	DTGRT* falling edge delay to DTACK* falling edge (@10 MHz)			152				ns
t4	DTGRT* low hold time following DTACK* falling edge.	0			0			ns
t5	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@20 MHz)	0.62	0.650	0.68				µs
	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@16 MHz)	0.78	0.812	0.84	1.53	1.562	1.59	µs
	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@12 MHz)	1.05	1.083	1.11	2.05	2.083	2.11	µs
	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@10 MHz)	1.27	1.300	1.33				µs
t6	DTACK* falling edge delay to INT* falling edge (@20 MHz)	0.57	0.60	0.63				µs
	DTACK* falling edge delay to INT* falling edge (@16 MHz)	0.72	0.75	0.78	1.22	1.25	1.28	µs
	DTACK* falling edge delay to INT* falling edge (@12 MHz)	0.97	1.00	1.03	1.63	1.66	1.70	µs
	DTACK* falling edge delay to INT* falling edge (@10 MHz)	1.17	1.20	1.23				µs
t7	INT* active low pulse width (note 2).		500			500		ns
t8	DTACK* rising edge delay to SMM_ACTIVE* rising edge.		3			3		clk
t9	DTACK* rising edge delay to INCMD* rising edge.		2			2		clk

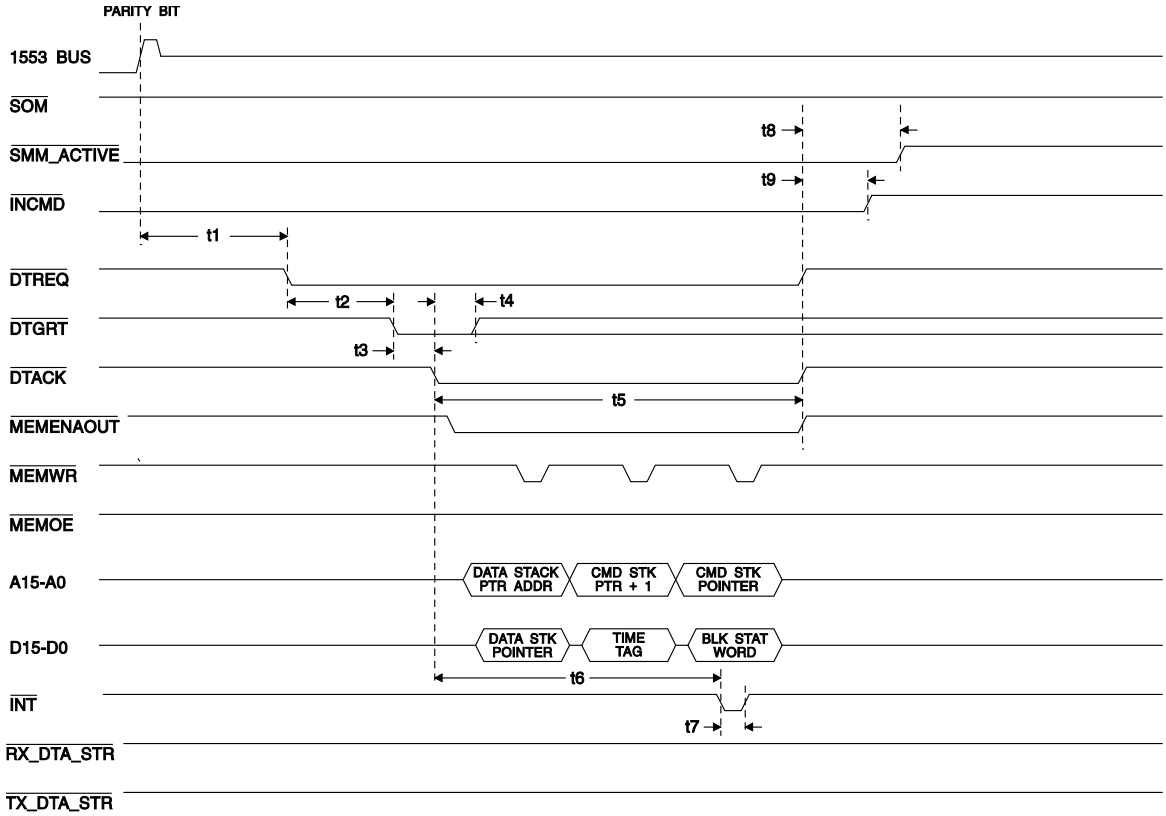


FIGURE 82. MESSAGE MT END OF MESSAGE TIMING

NOTES for TABLE 148 and FIGURE 82.

1. If maximum allowable request to grant time is exceeded, a handshake fail condition will occur. A handshake fail on the MT End of Message sequence will cause the ACE/Mini-ACE to abort processing the message. This message will appear on the communication stack as a message with the SOM bit set in the block status word.
2. Assumes that the interrupt request mode is set to pulse mode (bit 3 of configuration register #2 is set to logic "1").

9.7 WORD MT OPERATION

FIGURE 83 illustrates the start timing for the Word Monitor mode. The word monitor may be started by either a software command (writing a start command to the start/reset register) or by an external trigger input (EXT_TRIG) if the external trigger is enabled (bit 7 of configuration register #1 set to logic 1). Upon either of the start conditions, the ACE will perform a read operation from the stack pointer memory location (100 or 104). Once read, the stack pointer memory location (100 or 104) is not used by the ACE/Mini-ACE monitor and may be overwritten by either the monitor stack without effecting the operation of the ACE/Mini-ACE.

FIGURE 84 illustrates a word monitor received word write cycle. Once started, the ACE/Mini-ACE Word Monitor will store all 1553 words (command, status, and data) into the RAM. Each 1553 word will be stored with a corresponding tag word.

TABLE 149. WORD MT START TIMING

WORD MT START TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	READYD* falling edge (end of CPU MT start write cycle) delay to DTREQ* falling edge (requesting MT start sequence) (@20 MHz)	120	150	180				ns
	READYD* falling edge (end of CPU MT start write cycle) delay to DTREQ* falling edge (requesting MT start sequence) (@16 MHz)	160	188	220	160	188	220	ns
	READYD* falling edge (end of CPU MT start write cycle) delay to DTREQ* falling edge (requesting MT start sequence) (@12 MHz)	220	250	280	220	250	280	ns
	READYD* falling edge (end of CPU MT start write cycle) delay to DTREQ* falling edge (requesting MT start sequence) (@10 MHz)	270	300	330				ns
t2	EXT_TRIG* rising edge delay to DTREQ* falling edge (requesting MT start sequence) (@20 MHz) (Note 1)	100	170	240				ns
	EXT_TRIG* rising edge delay to DTREQ* falling edge (requesting MT start sequence) (@16 MHz) (Note 1)	160	210	280	160	210	280	ns
	EXT_TRIG* rising edge delay to DTREQ* falling edge (requesting MT start sequence) (@12 MHz) (Note 1)	220	290	360	220	290	360	ns
	EXT_TRIG* rising edge delay to DTREQ* falling edge (requesting MT start sequence) (@10 MHz) (Note 1)	300	370	440				ns
t3	DTREQ* falling edge delay to DTGRT* falling edge (Note 2)							ns
t4	DTGRT* falling edge delay to DTACK* falling edge (@20 MHz)			102				ns
	DTGRT* falling edge delay to DTACK* falling edge (@16 MHz)			115			105	ns
	DTGRT* falling edge delay to DTACK* falling edge (@12 MHz)			135			125	ns
	DTGRT* falling edge delay to DTACK* falling edge (@10 MHz)			152				ns
t5	DTGRT* low hold time following DTACK* falling edge.	0			0			ns
t6	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@20 MHz)	220	250	280				ns
	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@16 MHz)	280	312	340	530	562	590	ns
	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@12 MHz)	390	417	450	720	750	780	ns
	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@10 MHz)	470	500	530				ns

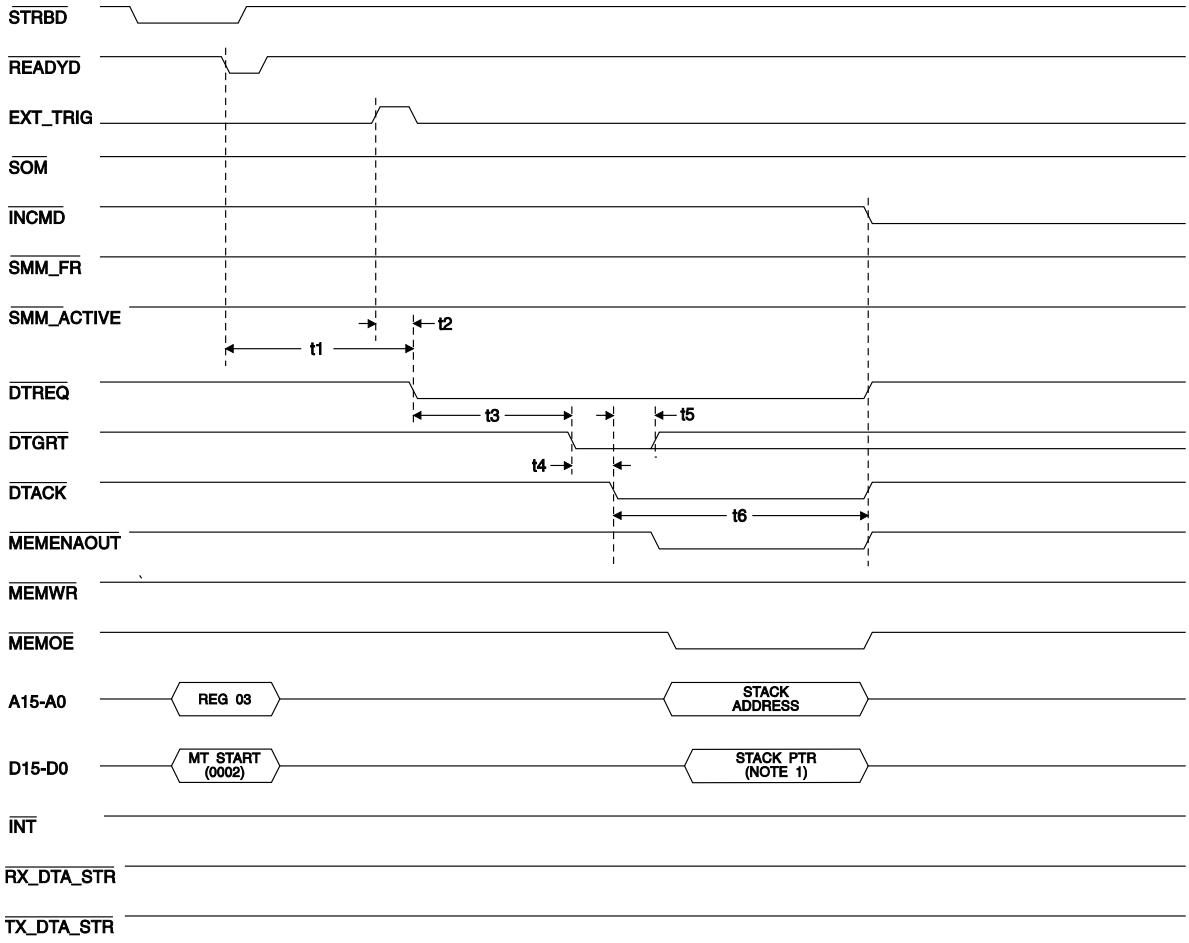


FIGURE 83. WORD MT START TIMING

NOTES for TABLE 149 and FIGURE 83.
1. Assumes that the external trigger is enabled in Configuration Register #1.
2. If maximum allowable request to grant time is exceeded, a handshake fail condition will occur. A handshake fail on the MT start sequence will cause the ACE/Mini-ACE monitor to not start (i.e., the ACE/Mini-ACE will remain in the Idle mode).

TABLE 150. WORD MT RECEIVED WORD WRITE CYCLE TIMING								
WORD MT RECEIVED WORD WRITE CYCLE TIMING								
REF	DESCRIPTION	ACE/MINI-ACE			SP'ACE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Mid-parity crossing of last word in message delay to DTREQ* falling edge (requesting received word write cycle) (@ 20 MHz)	1.04	1.32	1.60				µs
	Mid-parity crossing of last word in message delay to DTREQ* falling edge (requesting received word write cycle) (@16 MHz)	1.2	1.41	1.73	1.2	1.41	1.73	µs
	Mid-parity crossing of last word in message delay to DTREQ* falling edge (requesting received word write cycle) (@12 MHz)	1.36	1.6	1.94	1.36	1.6	1.94	µs
	Mid-parity crossing of last word in message delay to DTREQ* falling edge (requesting received word write cycle) (@10 MHz)	1.45	1.75	2.1				µs
t2	DTREQ* falling edge delay to DTGRT* falling edge (@20 MHz) (Note 1)			4.5				µs
	DTREQ* falling edge delay to DTGRT* falling edge (@16 MHz) (Note 1)			4.0			4.0	µs
	DTREQ* falling edge delay to DTGRT* falling edge (@12 MHz) (Note 1)			3.5			3.5	µs
	DTREQ* falling edge delay to DTGRT* falling edge (@10 MHz) (Note 1)			3.1				µs
t3	DTGRT* falling edge delay to DTACK* falling edge (@20 MHz)			102				ns
	DTGRT* falling edge delay to DTACK* falling edge (@16 MHz)			115			105	ns
	DTGRT* falling edge delay to DTACK* falling edge (@12 MHz)			135			125	ns
	DTGRT* falling edge delay to DTACK* falling edge (@10 MHz)			152				ns
t4	DTGRT* low hold time following DTACK* falling edge.	0			0			ns
t5	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@20 MHz)	0.42	0.450	0.48				µs
	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@16 MHz)	0.53	0.560	0.59	1.03	1.06	1.09	µs
	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@12 MHz)	0.72	0.750	0.78	1.39	1.42	1.45	µs
	DTACK* falling edge delay to DTREQ* rising edge, DTACK* rising edge, and MEMENAOUT* rising edge (@10 MHz)	0.87	0.900	0.93				µs

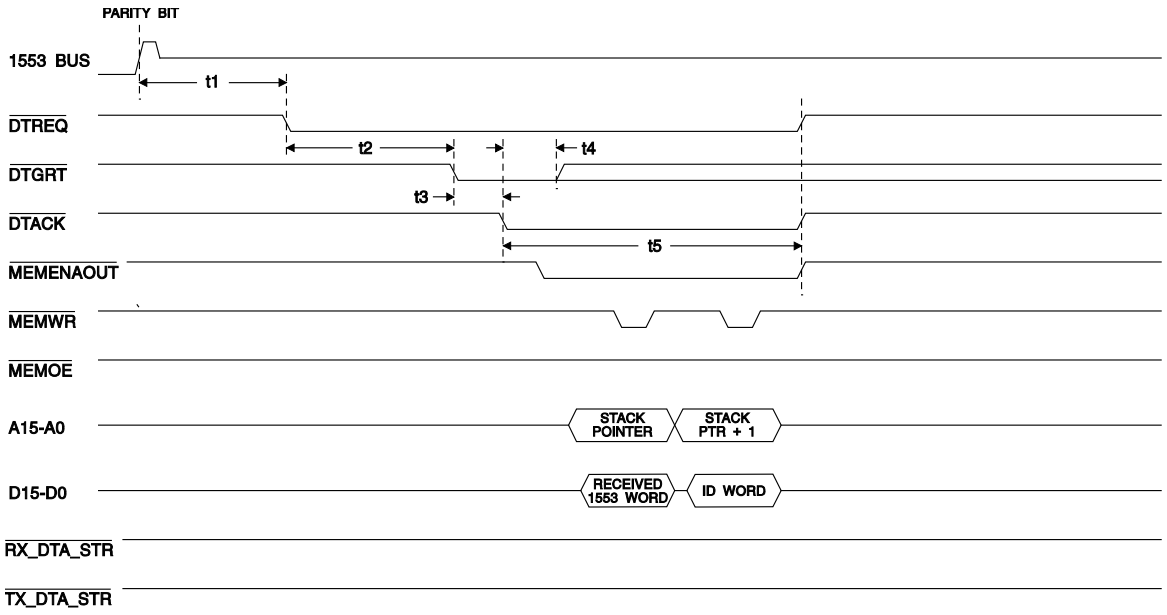


FIGURE 84. WORD MT RECEIVED WORD WRITE CYCLE TIMING

NOTES For TABLE 150 and FIGURE 84.
1. If maximum allowable request to grant time is exceeded, a handshake fail condition will occur. A handshake fail on an MT received word write sequence will cause the ACE/Mini-ACE monitor to ignore the received word (i.e., the word will be lost).

10 APPENDIX A

10.1 MTBF CURVES

The following Reliability Predictions apply to these products:

- BU-61580D1, BU-61580D2,
- BU-61581D1, BU-61581D2,
- BU-65170D1, BU-65170D2,
- BU-65171D1, BU-65171D2.

- BU-61580F1, BU-61580F2,
- BU-61581F1, BU-61581F2,
- BU-65170F1, BU-65170F2,
- BU-65171F1, BU-65171F2.

- BU-61580J1, BU-61580J2,
- BU-61581J1, BU-61581J2,
- BU-65170J1, BU-65170J2,
- BU-65171J1, BU-65171J2.

- BU-61580S1, BU-61580S2,
- BU-61581S1, BU-61581S2,
- BU-65170S1, BU-65170S2,
- BU-65171S1, BU-65171S2.

- BU-61580V1, BU-61580V2,
- BU-61581V1, BU-61581V2,
- BU-65170V1, BU-65170V2,
- BU-65171V1, BU-65171V2.

APPLICATION		REVISIONS			
NEXT ASSY.	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A	Initial Release	12/22/92	

RELIABILTY PREDICTION REPORT

DDC PART NUMBER: BU61580X1
REPORT NUMBER: 53512

Prepared by: _____ 12/22/92
J. McHugh — Date
Quality Assurance Engineer

Approved by: _____ 12/22/92
J. Saber, Supervisor — Date
Quality Assurance Engineering

Approved by: _____ 12/22/92
M. Green — Date
Vice President
Product Assurance

REV		A	A	A	A	A	A
SHEET		1	2	3	4	5	6

REV. STATUS OF SHEETS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON FRAC. DEC. ANGLES

MATERIAL:

FINISH:

PREPARED	McHugh	12/92
CHECKED		12/92
ENGINEER		

DDC
ILC DATA DEVICE CORPORATION
BOHEMIA N.Y.

RELIABILITY PREDICTION REPORT
DDC PART NUMBER: BU61580X1

SIZE	CODE IDENT. NO.	
A	19645	53512

SCALE | REV. A | SHEET 1 OF 6

n:lgrr.db
#5

DDC PART NUMBER: BU61580X1
QUALITY LEVEL: B
PACKAGE CONFIGURATION: 70 PIN CERAMIC BATHTUB
ENGINEER: T. HOFFMAN

DOCUMENT DATA FILE (DDF): TBD REV

MAIN BILL OF MATERIALS (BM): TBD REV MAIN ASSEMBLY DRAWING: TBD REV

SUBASSEMBLY (BM): SUBASSEMBLY DRAWING(S):

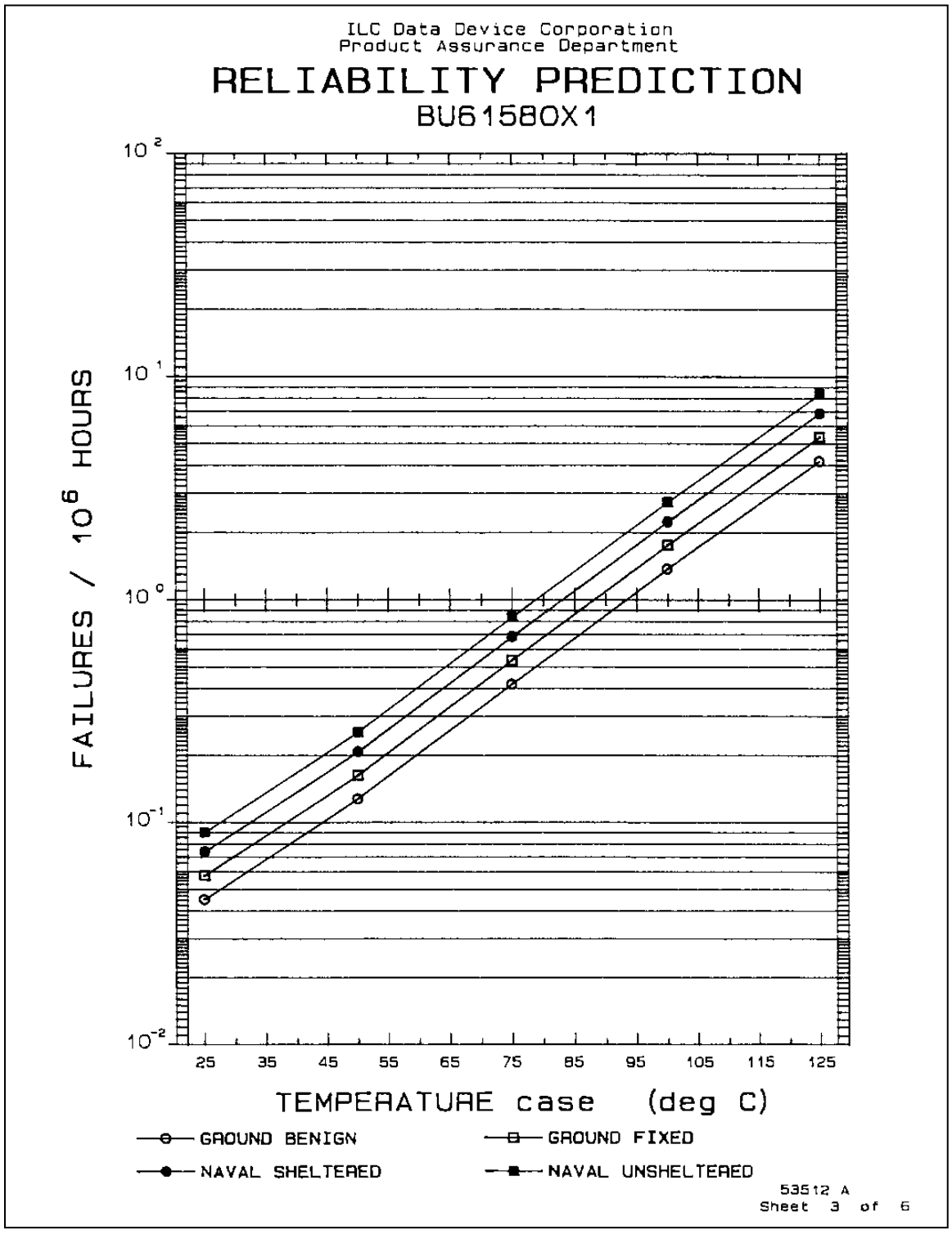
PREDICTION(S) ARE IN ACCORDANCE WITH THE METHODOLOGY AND MATH MODELS OF MIL-HDBK-217F.
CALCULATIONS WERE PERFORMED USING A CUSTOM MADE SPREADSHEET IN LOTUS 1-2-3 RELEASE 2.01.
APPLICATION DATA AND COMPONENT FAILURE RATE DATA REQUIRED TO PERFORM THESE CALCULATIONS SHALL BE FURNISHED UPON REQUEST.

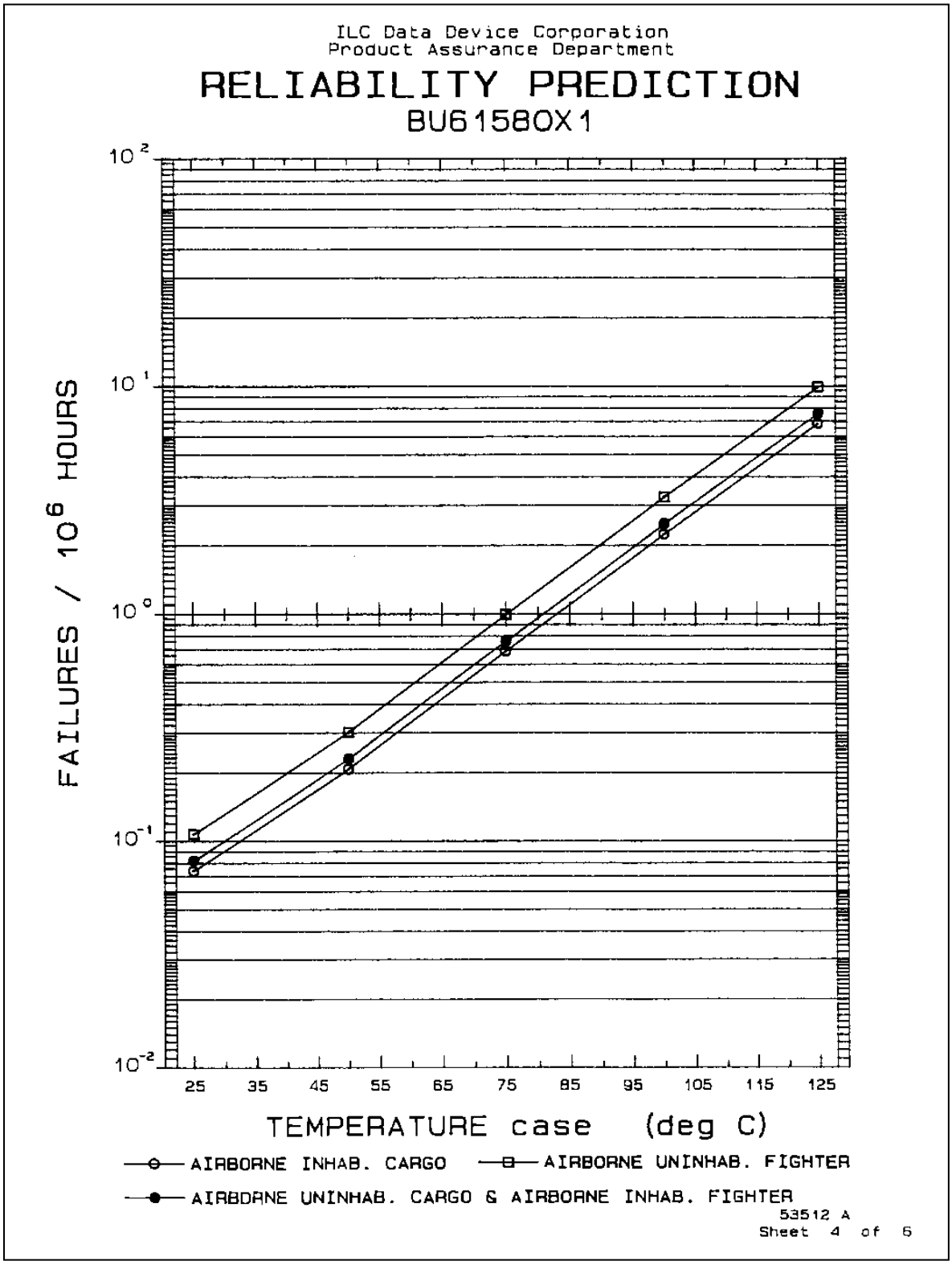
FAILURE RATE(S) AND MEAN TIME BETWEEN FAILURES FOR SPECIFIED ENVIRONMENT(S) AT SPECIFIED TEMPERATURE(S) ARE SHOWN BELOW.[1] GRAPHICAL REPRESENTATION SHOWING A RANGE FROM T_C = +25°C TO T_C = +125°C IS INCLUDED IN THIS REPORT.

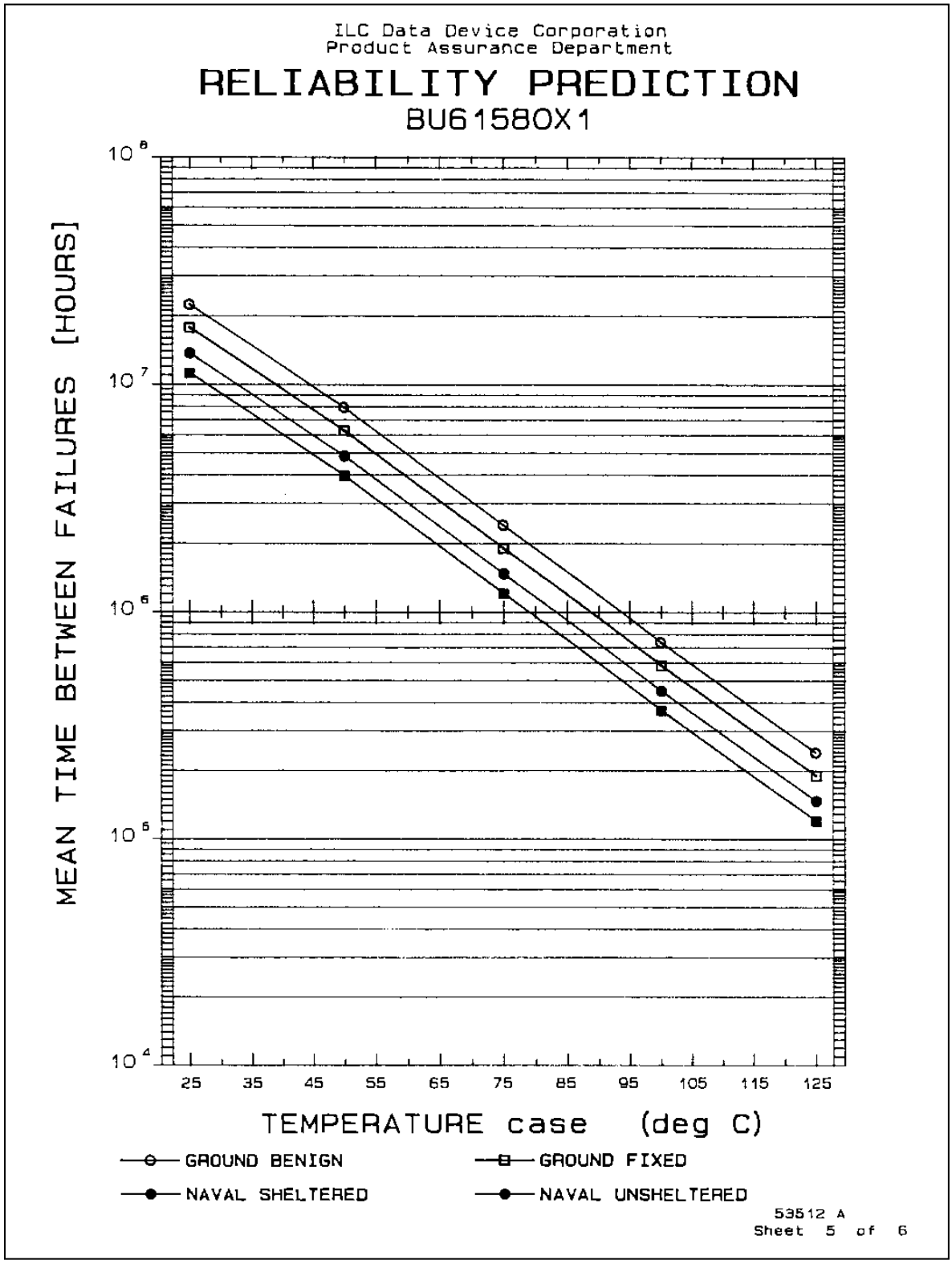
ENVIRONMENT(S)	TEMP(S).	FAILURE RATE(S) [FAILURES/1M HOURS]	MTBF
GROUND BENIGN	T_C = + 35°C	0.0658	15,200,000 HOURS
GROUND FIXED	T_C = + 45°C	0.129	7,780,000 HOURS
NAVAL SHELTERED	T_C = + 45°C	0.165	6,050,000 HOURS
NAVAL UNSHELTERED	T_C = + 50°C	0.253	3,950,000 HOURS
AIR INHABITED CARGO	T_C = + 60°C	0.331	3,020,000 HOURS
AIR UNINHABITED CARGO	T_C = + 75°C	0.757	1,320,000 HOURS
AIR INHABITED FIGHTER	T_C = + 60°C	0.368	2,720,000 HOURS
AIR UNINHABITED FIGHTER	T_C = + 75°C	0.984	1,020,000 HOURS

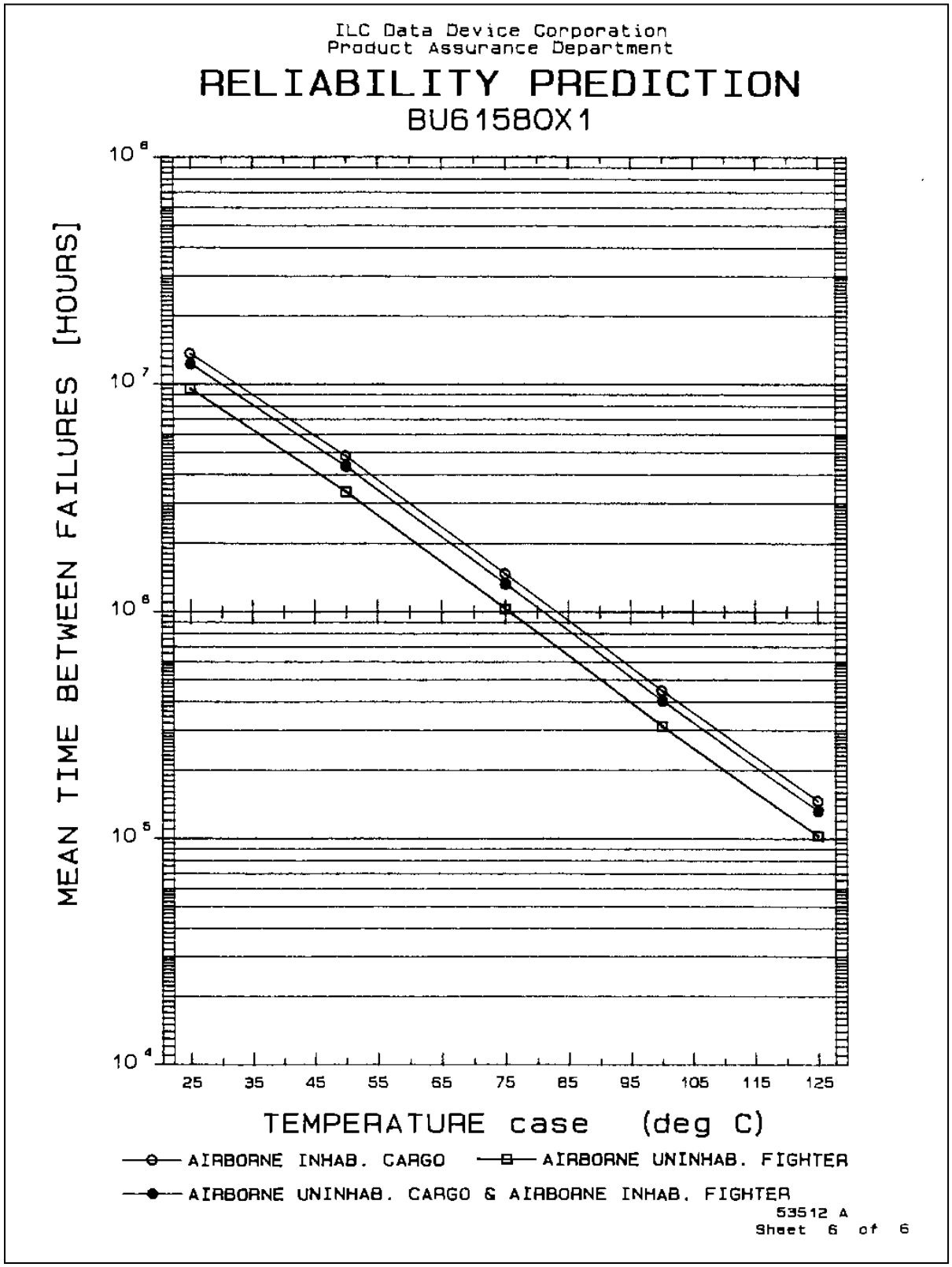
[1] WHEN ENVIRONMENT(S) AND TEMPERATURE(S) ARE NOT SPECIFIED (N/S), REFER DIRECTLY TO GRAPH(S).

	SIZE	FSCM NO.	
DDC ILC DATA DEVICE CORPORATION BOHEMIA, N.Y.	A	19645	53512
	SCALE	REV A	SHEET 2 OF 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU61580X1
FAILURES / 10^6 HOURS
10^2
10^1
10^0
10^-1
10^-2
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
GROUND BENIGN
GROUND FIXED
NAVAL SHELTERED
NAVAL UNSHELTERED
53512 A
Sheet 3 of 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU61580X1
FAILURES / 10^6 HOURS
10^2
10^1
10^0
10^-1
10^-2
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
AIRBORNE INHAB. CARGO
AIRBORNE UNINHAB. FIGHTER
AIRBDRNE UNINHAB. CARGO & AIRBORNE INHAB. FIGHTER
53512 A
Sheet 4 of 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU61580X1
MEAN TIME BETWEEN FAILURES [HOURS]
10 8
10 7
10 6
10 5
10 4
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
GROUND BENIGN
GROUND FIXED
NAVAL SHELTERED
NAVAL UNSHELTERED
53512 A
Sheet 5 of 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU61580X1
MEAN TIME BETWEEN FAILURES [HOURS]
10^8
10^7
10^6
10^5
10^4
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
AIRBORNE INHAB. CARGO
AIRBORNE UNINHAB. FIGHTER
AIRBORNE UNINHAB. CARGO & AIRBORNE INHAB. FIGHTER
53512 A
Sheet 6 of 6

The following Reliability Predictions apply to these products:

- BU-61580D3, BU-61581D3,
- BU-61580D6, BU-61581D6,
- BU-65170D3, BU-65171D3,
- BU-65170D3, BU-65171D6.

- BU-61580F3, BU-61581F3,
- BU-61580F6, BU-61581F6,
- BU-65170F3, BU-65171F3,
- BU-65170F3, BU-65171F6.

- BU-61580J3, BU-61581J3,
- BU-61580J6, BU-61581J6,
- BU-65170J3, BU-65171J3,
- BU-65170J3, BU-65171J6.

- BU-61580S3, BU-61581S3,
- BU-61580S6, BU-61581S6,
- BU-65170S3, BU-65171S3,
- BU-65170S3, BU-65171S6.

- BU-61580V3, BU-61581V3,
- BU-61580V6, BU-61581V6,
- BU-65170V3, BU-65171V3,
- BU-65170V3, BU-65171V6.

APPLICATION		REVISIONS			
NEXT ASSY.	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A	Initial Release	03/26/92	
		B	Change to MIL-HDBK-217F	10/12/92	

RELIABILTY PREDICTION REPORT - HYBRID

DDC PART NUMBER: BU61580X3
REPORT NUMBER: 52369

Prepared by: J. McHugh 3/26/92
J. McHugh — Date
Quality Assurance Engineer

Approved by: 3/26/92
J. Saber, Supervisor — Date
Quality Assurance Engineering

Approved by: 3/30/92
M. Green — Date
Vice President
Product Assurance

REV. STATUS OF SHEETS								
REV		B	B	B	B	B	B	
SHEET	1	2	3	4	5	6		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON FRAC DEC ANGLES

MATERIAL

FINISH

PREPARED	McHugh	03/92
CHECKED		3/92
ENGINEER		

DDC
ILC DATA DEVICE CORPORATION
BOHEMIA, N.Y.

RELIABILITY PREDICTION REPORT-HYBRID
DDC PART NUMBER: BU61580X3

SIZE	CODE IDENT NO	
A	19645	52369

SCALE | REV B | SHEET 1 OF 6

n:1grr.db
#5

DDC PART NUMBER: BU61580X3
QUALITY LEVEL: B
PACKAGE CONFIGURATION: 70 PIN CERAMIC BATHTUB
ENGINEER: T. HOFFMAN

DOCUMENT DATA FILE (DDF): TBD REV

MAIN BILL OF MATERIALS (BM): TBD REV MAIN ASSEMBLY DRAWING: TBD REV

SUBASSEMBLY (BM): SUBASSEMBLY DRAWING(S):

PREDICTION(S) ARE IN ACCORDANCE WITH THE METHODOLOGY AND MATH MODELS OF MIL-HDBK-217F.

CALCULATIONS WERE PERFORMED USING A CUSTOM MADE SPREADSHEET IN LOTUS 1-2-3 RELEASE 2.01.

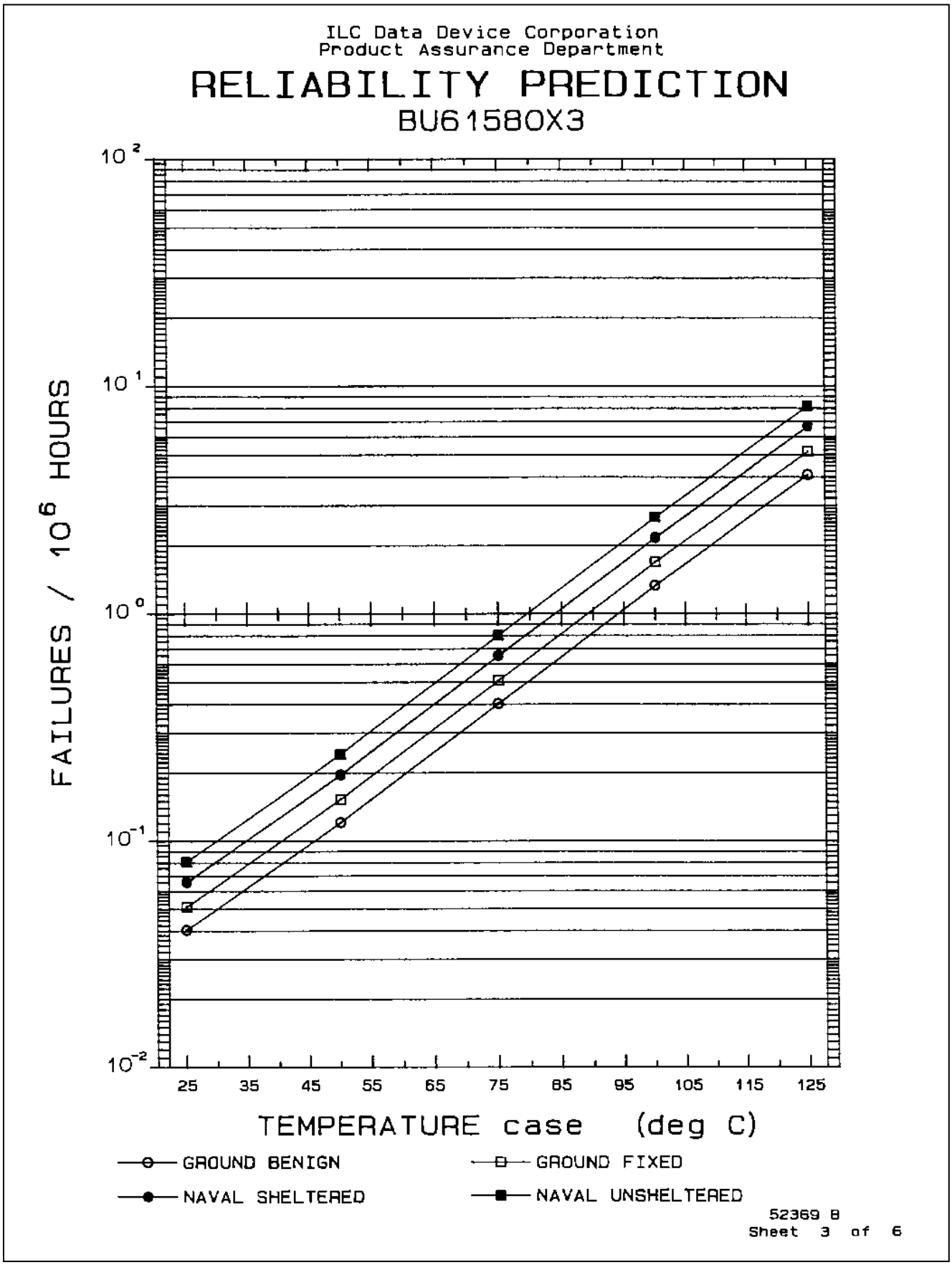
APPLICATION DATA AND COMPONENT FAILURE RATE DATA REQUIRED TO PERFORM THESE CALCULATIONS SHALL BE FURNISHED UPON REQUEST.

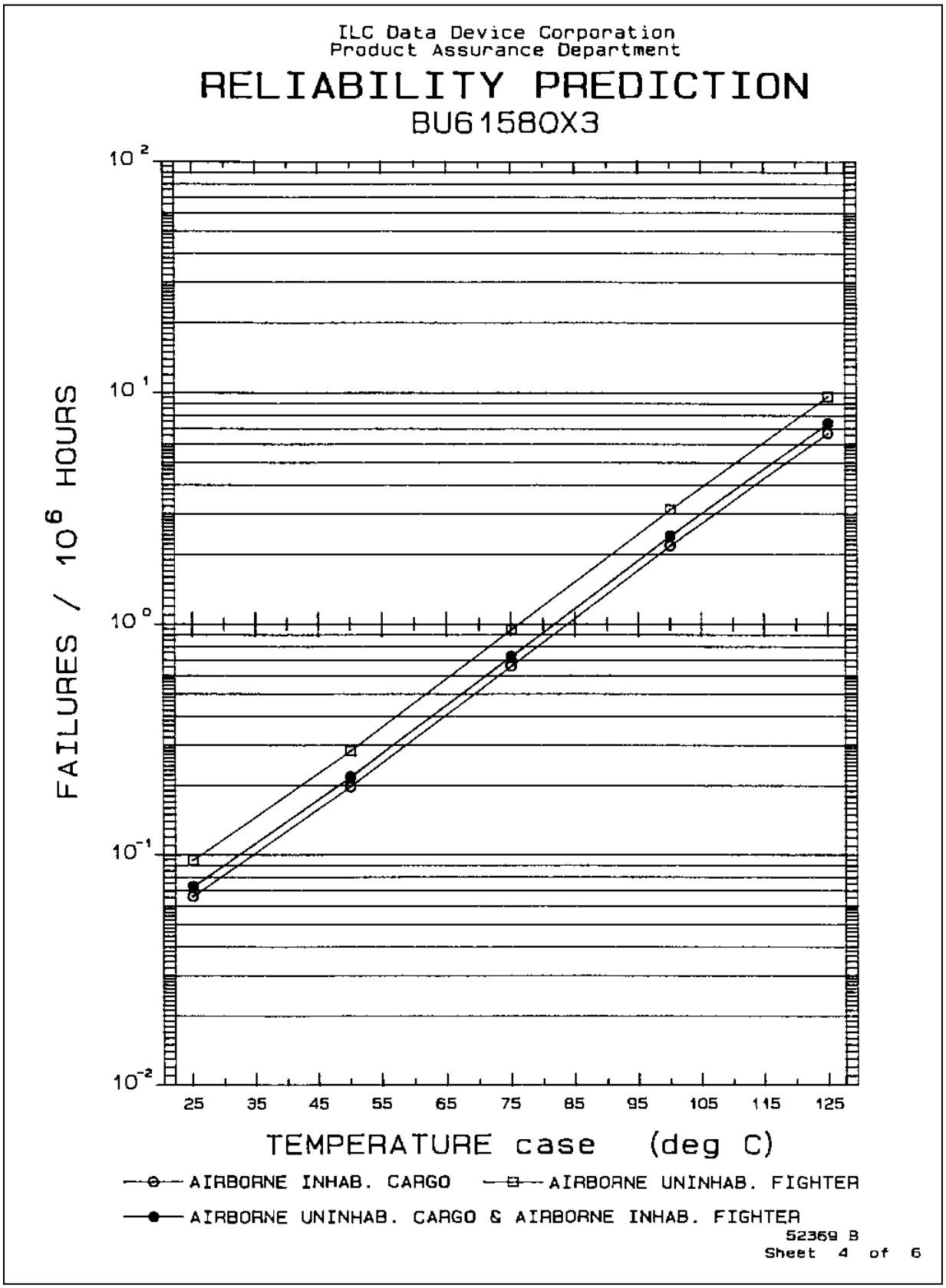
FAILURE RATE(S) AND MEAN TIME BETWEEN FAILURES FOR SPECIFIED ENVIRONMENT(S) AT SPECIFIED TEMPERATURE(S) ARE SHOWN BELOW.[1] GRAPHICAL REPRESENTATION SHOWING A RANGE FROM T_C = +25°C TO T_C = +125°C IS INCLUDED IN THIS REPORT.

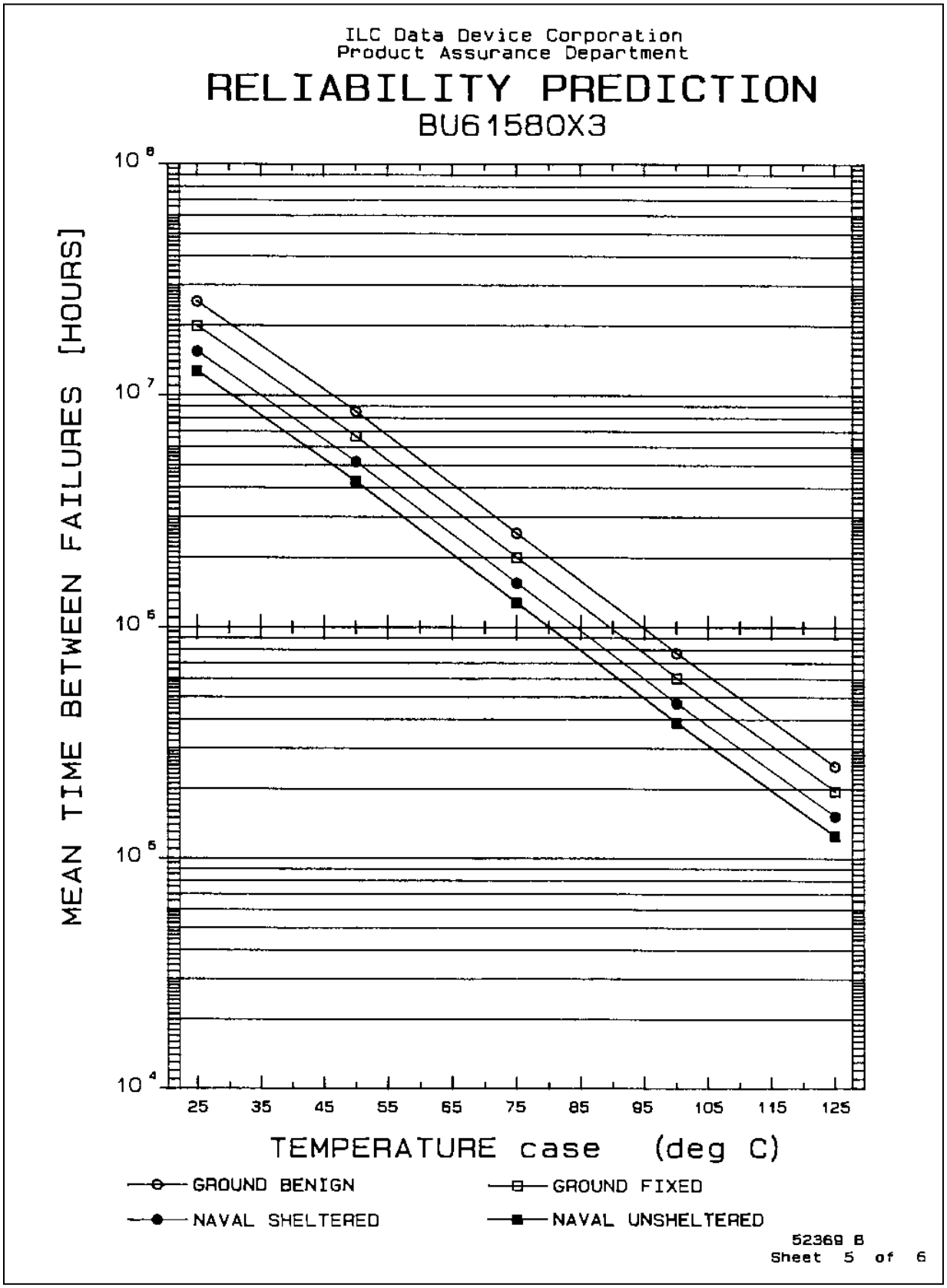
ENVIRONMENT(S)	TEMP(S).	FAILURE RATE(S) [FAILURES/1M HOURS]	MTBF
GROUND BENIGN	T_C = + 35°C	0.0601	16,600,000 HOURS
GROUND FIXED	T_C = + 45°C	0.120	8,350,000 HOURS
NAVAL SHELTERED	T_C = + 45°C	0.154	6,490,000 HOURS
NAVAL UNSHELTERED	T_C = + 50°C	0.238	4,210,000 HOURS
AIR INHABITED CARGO	T_C = + 60°C	0.314	3,190,000 HOURS
AIR UNINHABITED CARGO	T_C = + 75°C	0.723	1,380,000 HOURS
AIR INHABITED FIGHTER	T_C = + 60°C	0.349	2,87D,000 HOURS
AIR UNINHABITED FIGHTER	T_C = + 75°C	0.940	1,060,000 HOURS

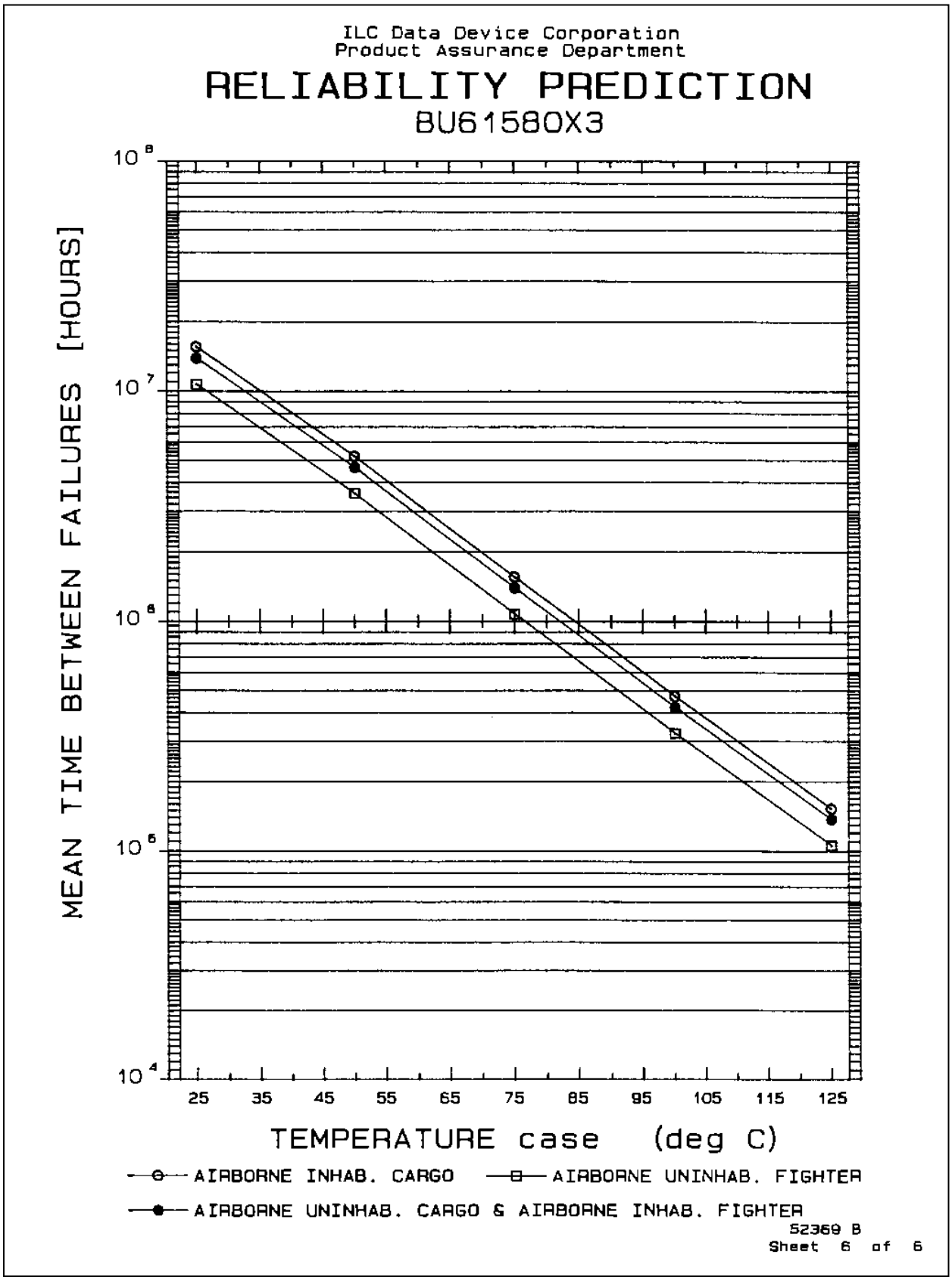
1 WHEN ENVIRONMENT(S) AND TEMPERATURE(S) ARE NOT SPECIFIED (N/S), REFER DIRECTLY TO GRAPH(S).

	SIZE	FSCM NO.	
DDC ILC DATA DEVICE CORPORATION BOHEMIA, N.Y.	A	19645	52369
	SCALE	REV B	SHEET 2 OF 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU61580X3
FAILURES / 10^6 HOURS
10^2
10^1
10^0
10^-1
10^-2
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
GROUND BENIGN
GROUND FIXED
NAVAL SHELTERED
NAVAL UNSHELTERED
52369 B
Sheet 3 of 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU61580X3
FAILURES / 10^6 HOURS
10^2
10^1
10^0
10^-1
10^-2
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
AIRBORNE INHAB. CARGO
AIRBORNE UNINHAB. FIGHTER
AIRBORNE UNINHAB. CARGO & AIRBORNE INHAB. FIGHTER
52369 B
Sheet 4 of 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU61580X3
MEAN TIME BETWEEN FAILURES [HOURS]
10 8
10 7
10 6
10 5
10 4
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
GROUND BENIGN
GROUND FIXED
NAVAL SHELTERED
NAVAL UNSHELTERED
52369 B
Sheet 5 of 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
8U61580X3
MEAN TIME BETWEEN FAILURES [HOURS]
10 8
10 7
10 6
10 5
10 4
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
AIRBORNE INHAB. CARGO
AIRBORNE UNINHAB. FIGHTER
AIRBORNE UNINHAB. CARGO & AIRBORNE INHAB. FIGHTER
52369 B
Sheet 6 of 6

APPENDIX A

The following Reliability Predictions apply to these products:

- BU-61585S1, BU-61586S1,
- BU-61585S2, BU-61586S2.

- BU-61585V1, BU-61586V1,
- BU-61585V2, BU-61586V2.

APPLICATION		REVISIONS			
NEXT ASSY.	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A	Initial Release	12/19/94	

RELIABILITY PREDICTION REPORT

DDC PART NUMBER: BU-61585S1
REPORT NUMBER: 57289

Prepared By: 12/19/94
J. McHugh — Date
Quality Assurance Engineer

Approved By: 12/20/94
J. Saber, Supervisor — Date
Quality Assurance Engineering

Approved By: 12/21/94
M. Green — Date
Vice President
Product Assurance

REV																					
SHEET																					
REV STATUS OF SHEETS	REV	A	A	A	A	A	A														
	SHEET	1	2	3	4	5	6														

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON FRAC. DEC. ANGLES

MATERIAL

FINISH

PREPARED	MCHUGH	12/94
CHECKED	J. McHugh	12/94
ENGINEER		

DDC
ILC DATA DEVICE CORPORATION
BOHEMIA, NY

RELIABILITY PREDICTION REPORT

DDC P/N: BU-61585S1

SIZE	CODE IDENT NO.	
A	19645	57289

SCALE | REV. A | SHEET 1 OF 6

H:\QA\MCHUGH\RELRPT\57289.JM

DDC PART NUMBER: **BU-61586B1**
QUALITY LEVEL: **B**
PACKAGE CONFIGURATION: **78 PIN DIP**
ENGINEER: **T. HOFFMAN**

DOCUMENT DATA FILE (DDF): **55398 REV B**

BILL OF MATERIALS (BM): **55329-13 REV A** ASSEMBLY DRAWING: **55329 REV A**

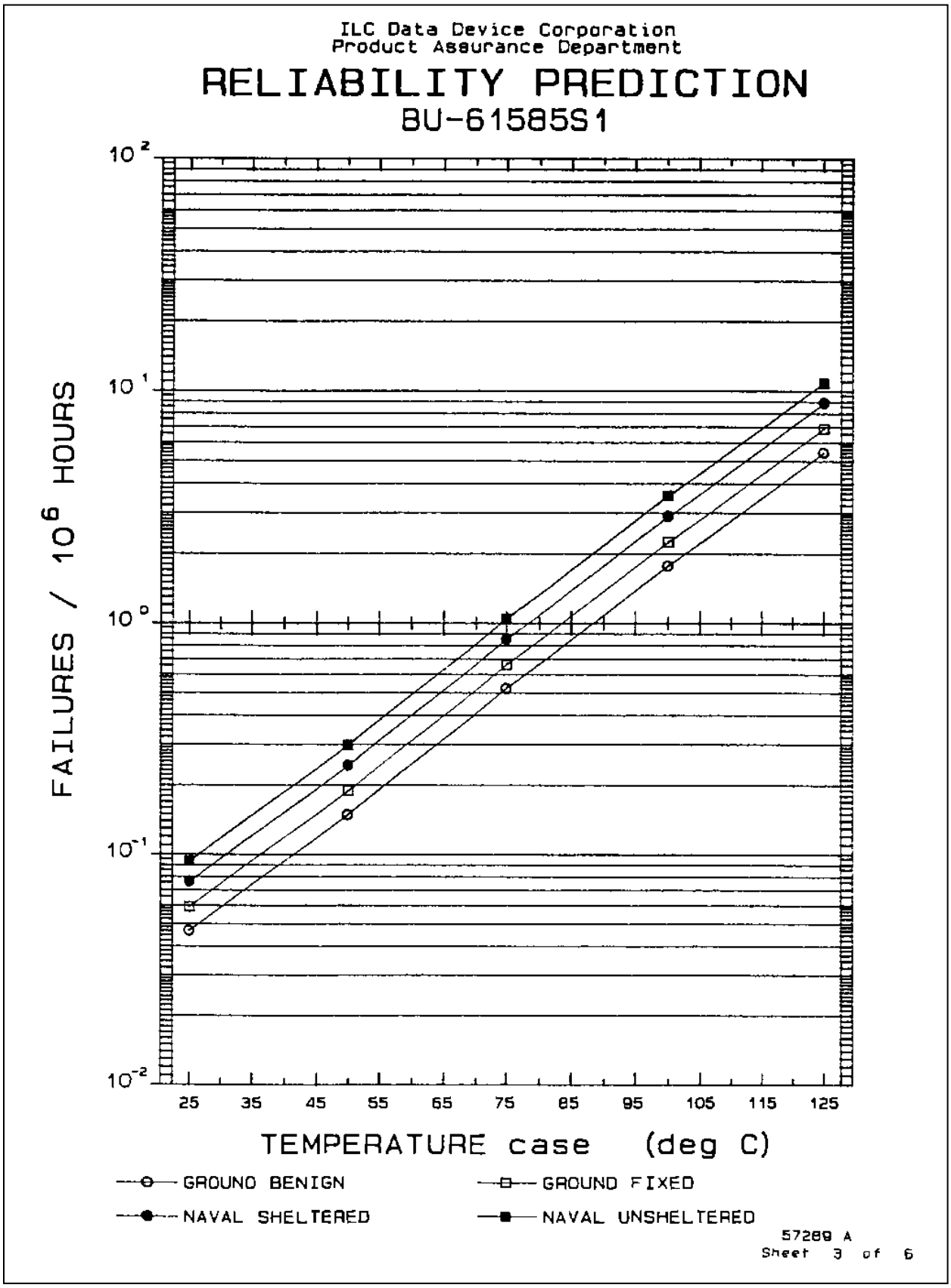
PREDICTIONS ARE IN ACCORDANCE WITH THE METHODOLOGY AND MATH MODELS OF MIL-HDBK-217F, NOTICE 1.

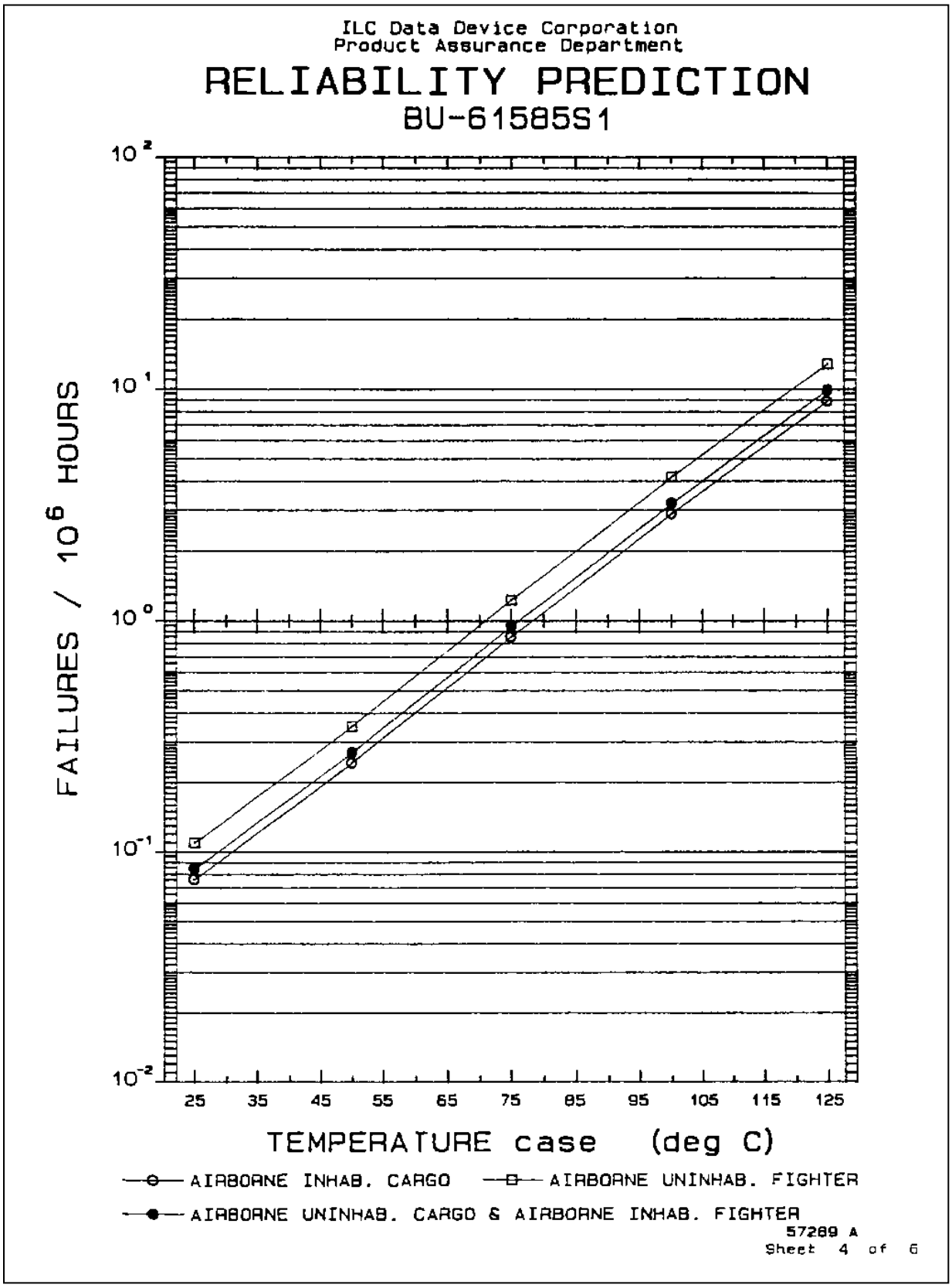
CALCULATIONS WERE PERFORMED USING A CUSTOM MADE SPREADSHEET IN LOTUS 1-2-3 RELEASE 2.01.

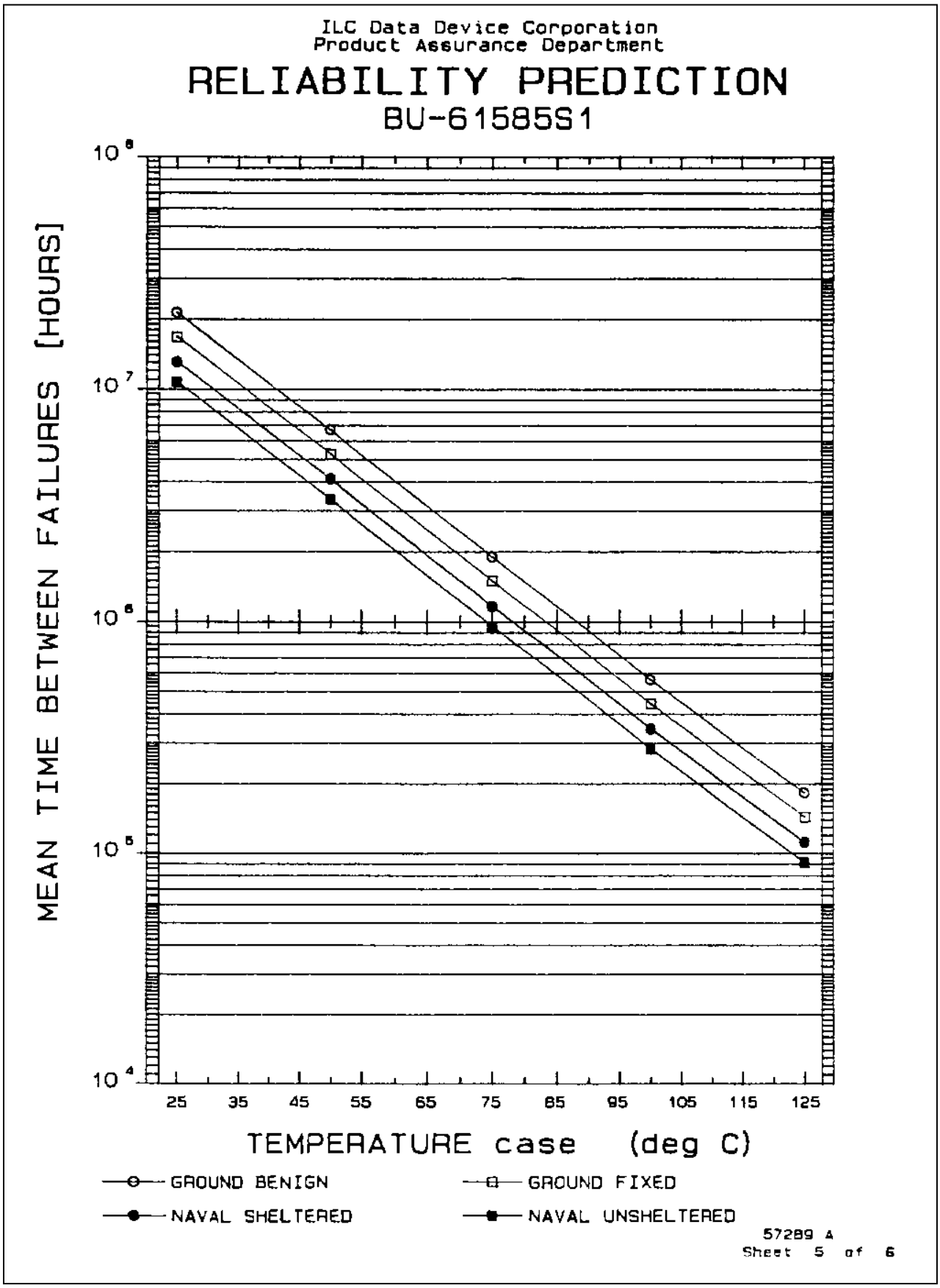
APPLICATION DATA AND COMPONENT FAILURE RATE DATA REQUIRED TO PERFORM THESE CALCULATIONS SHALL BE FURNISHED UPON REQUEST.

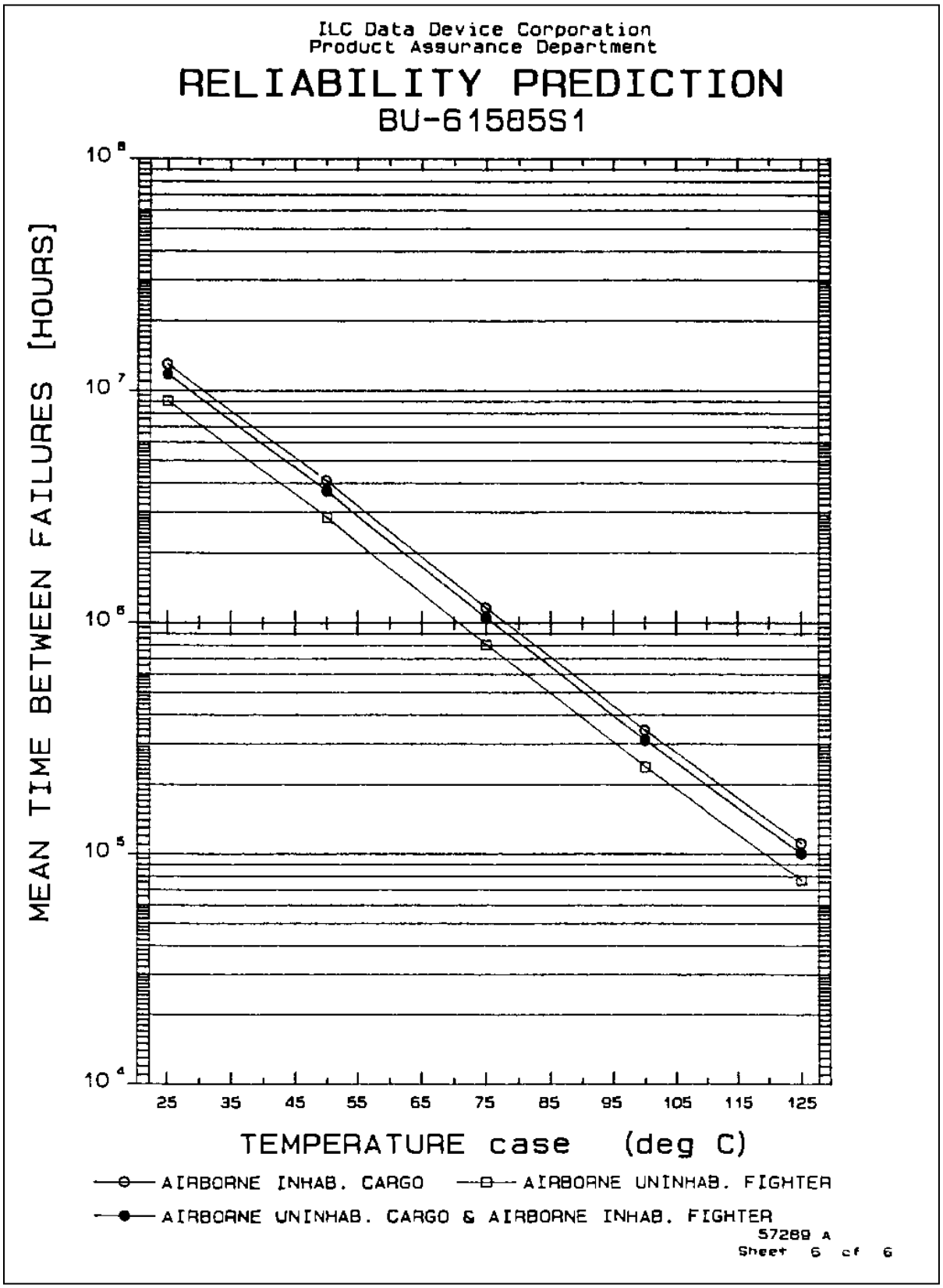
FAILURE RATES AND MEAN TIME BETWEEN FAILURES FOR SPECIFIED ENVIRONMENTS AT SPECIFIED TEMPERATURES ARE SHOWN BELOW. GRAPHICAL REPRESENTATION SHOWING A RANGE FROM T_C = +25 DEG C TO T_C = +125 DEG C IS INCLUDED IN THIS REPORT.

ENVIRONMENT	TEMPERATURE (CASE, DEG C)	FAILURE RATE (FAILURES/1M HOURS)	M.T.B.F. (HOURS)
GROUND BENIGN	+ 35	0.0723	13,800,000
GROUND FIXED	+ 45	0.148	6,760,000
NAVAL SHELTERED	+ 45	0.190	5,260,000
NAVAL UNSHELTERED	+ 50	0.297	3,360,000
AIR INHABITED CARGO	+ 60	0.402	2,490,000
AIR UNINHABITED CARGO	+ 75	0.952	1,050,000
AIR INHABITED FIGHTER	+ 60	0.447	2,240,000
AIR UNINHABITED FIGHTER	+ 75	1.24	808,000


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU-61585S1
FAILURES / 10^6 HOURS
10^2
10^1
10^0
10^-1
10^-2
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
GROUND BENIGN
GROUND FIXED
NAVAL SHELTERED
NAVAL UNSHELTERED
57289 A
Sheet 3 of 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU-61585S1
FAILURES / 10^6 HOURS
10^2
10^1
10^0
10^-1
10^-2
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
AIRBORNE INHAB. CARGO
AIRBORNE UNINHAB. FIGHTER
AIRBORNE UNINHAB. CARGO & AIRBORNE INHAB. FIGHTER
57289 A
Sheet 4 of 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU-61585S1
MEAN TIME BETWEEN FAILURES [HOURS]
10⁸
10⁷
10⁶
10⁵
10⁴
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
GROUND BENIGN
GROUND FIXED
NAVAL SHELTERED
NAVAL UNSHELTERED
57289 A
Sheet 5 of 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU-61585S1
MEAN TIME BETWEEN FAILURES [HOURS]
10 8
10 7
10 6
10 5
10 4
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
AIRBORNE INHAB. CARGO
AIRBORNE UNINHAB. FIGHTER
AIRBORNE UNINHAB. CARGO & AIRBORNE INHAB. FIGHTER
57289 A
Sheet 6 of 6

The following Reliability Predictions apply to these products:

- BU-61585S3, BU-61586S3,
- BU-61585S6, BU-61586S6.

- BU-61585V3, BU-61586V3,
- BU-61585V6, BU-61586V6.

APPLICATION		REVISIONS			
NEXT ASSY.	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A	Initial Release	12/19/94	

RELIABILITY PREDICTION REPORT

DDC PART NUMBER: BU-61585S3

REPORT NUMBER: 57290

Prepared By: J. McHugh 12/19/94

J. McHugh — Date

Quality Assurance Engineer

Approved By: J. Saber 12/20/94

J. Saber, Supervisor — Date

Quality Assurance Engineering

Approved By: M. Green 12/21/94

M. Green — Date

Vice President

Product Assurance

REV																						
SHEET																						
REV STATUS OF SHEETS	REV	A	A	A	A	A	A															
	SHEET	1	2	3	4	5	6															

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON FRAC. DEC. ANGLES

MATERIAL

FINISH

PREPARED	MCHUGH	12/94
CHECKED	J. McHugh	12/94
ENGINEER		

DDC
ILC DATA DEVICE CORPORATION
BOHEMIA, NY

RELIABILITY PREDICTION REPORT

DDC P/N: BU-61585S3

SIZE	CODE IDENT NO.	
A	19645	57290

SCALE | REV. A | SHEET 1 OF 6

H:\QA\MCHUGH\RELRPT\57290.JM

DDC PART NUMBER: BU-61585S3
QUALITY LEVEL: B
PACKAGE CONFIGURATION: 78 PIN DIP
ENGINEER: T. HOFFMAN

DOCUMENT DATA FILE (DDF): 56059 REV A

BILL OF MATERIALS (BM): 55329 REV A ASSEMBLY DRAWING: 55329 REV A

PREDICTIONS ARE IN ACCORDANCE WITH THE METHODOLOGY AND MATH MODELS OF MIL-HDBK-217F, NOTICE 1.

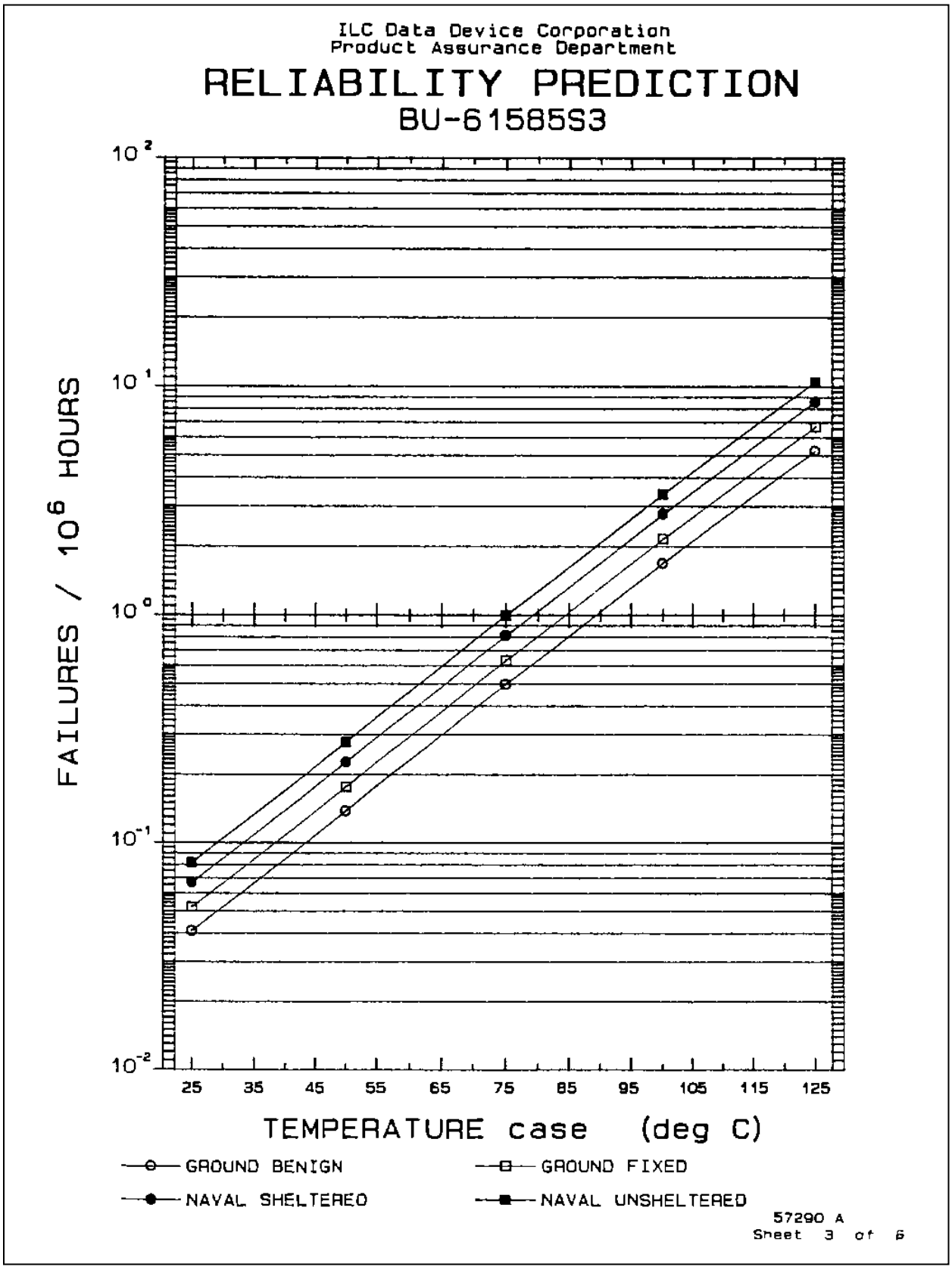
CALCULATIONS WERE PERFORMED USING A CUSTOM MADE SPREADSHEET IN LOTUS 1-2-3 RELEASE 2.01.

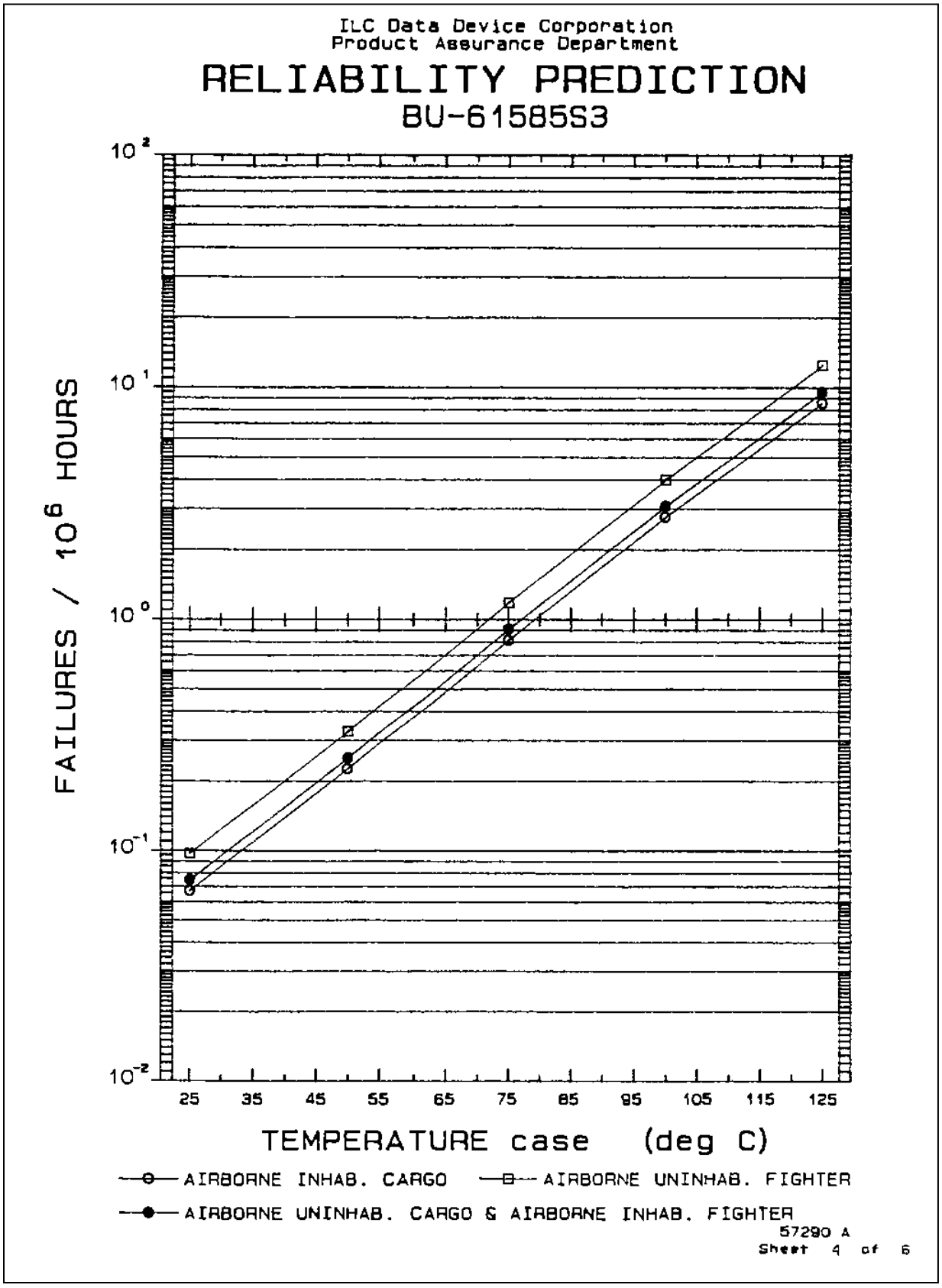
APPLICATION DATA AND COMPONENT FAILURE RATE DATA REQUIRED TO PERFORM THESE CALCULATIONS SHALL BE FURNISHED UPON REQUEST.

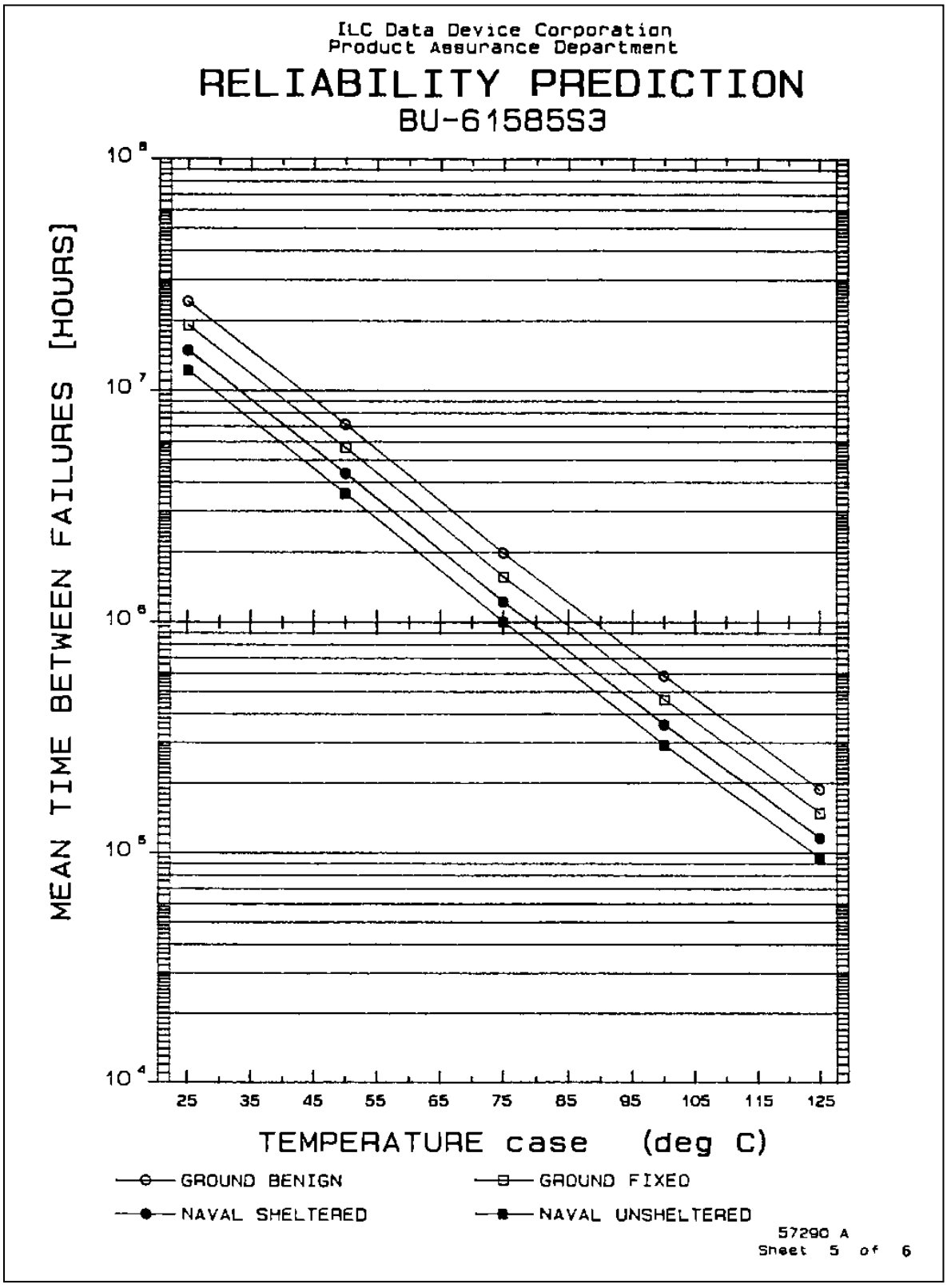
FAILURE RATES AND MEAN TIME BETWEEN FAILURES FOR SPECIFIED ENVIRONMENTS AT SPECIFIED TEMPERATURES ARE SHOWN BELOW. GRAPHICAL REPRESENTATION SHOWING A RANGE FROM T_C = +25 DEG C TO T_C = +125 DEG C IS INCLUDED IN THIS REPORT.

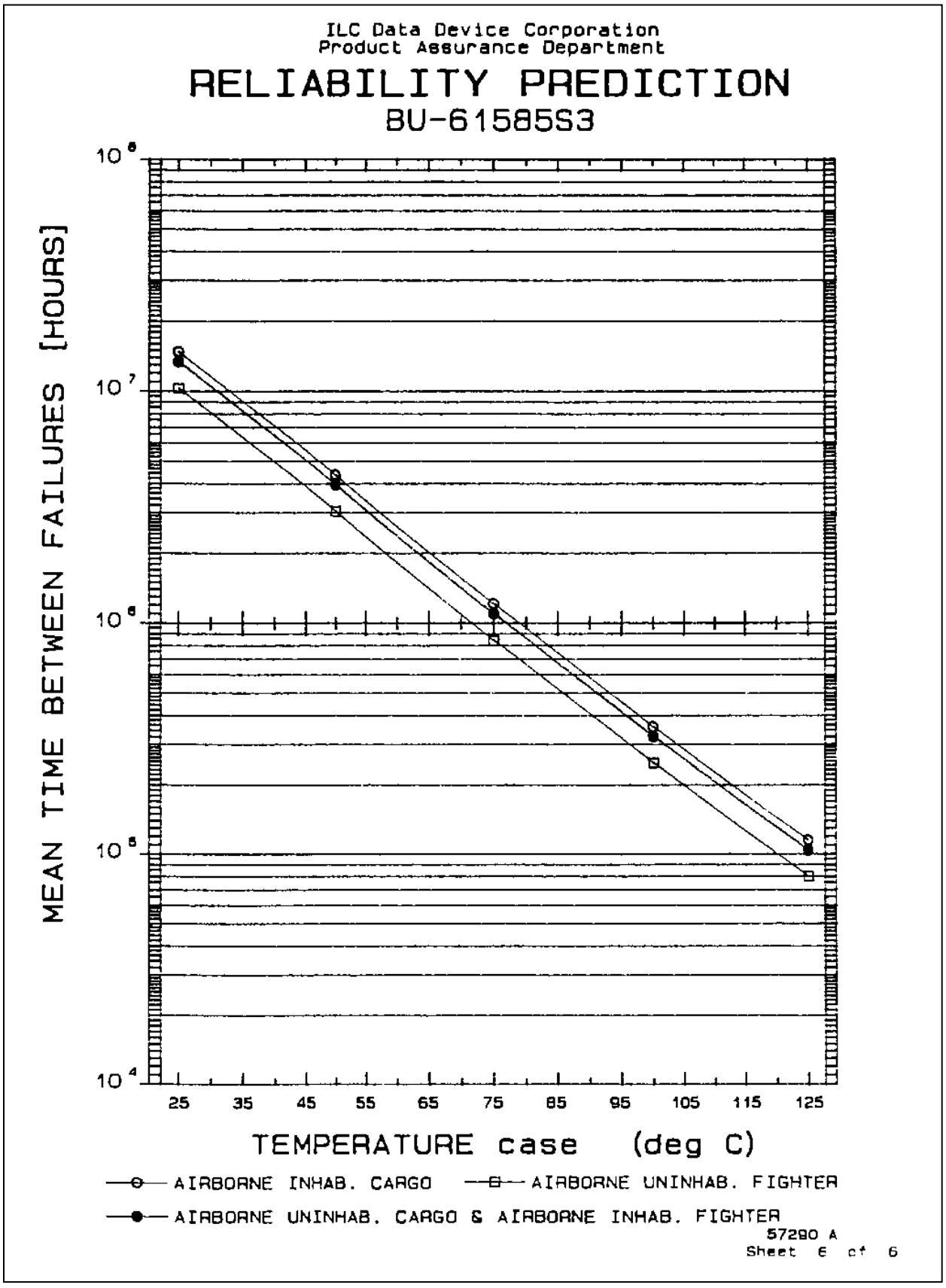
ENVIRONMENT	TEMPERATURE (CASE, DEG C)	FAILURE RATE (FAILURES/1M HOURS)	M.T.B.F. (HOURS)
GROUND BENIGN	+ 35	0.0657	15,200,000
GROUND FIXED	+ 45	0.137	7,280,000
NAVAL SHELTERED	+ 45	0.177	5,660,000
NAVAL UNSHELTERED	+ 50	0.278	3,590,000
AIR INHABITED CARGO	+ 60	0.380	2,630,000
AIR UNINHABITED CARGO	+ 75	0.908	1,100,000
AIR INHABITED FIGHTER	+ 60	0.422	2,370,000
AIR UNINHABITED FIGHTER	+ 75	1.18	846,000

	SIZE	FSCM NO.	
DDC® ILC DATA DEVICE CORPORATION BOHEMIA, N.Y.	A	19645	57290
	SCALE	REV A	SHEET 2 OF 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU-61585S3
FAILURES / 10^6 HOURS
10^2
10^1
10^0
10^-1
10^-2
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
GROUND BENIGN
GROUND FIXED
NAVAL SHELTERED
NAVAL UNSHELTERED
57290 A
Sheet 3 of 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU-61585S3
FAILURES / 10^6 HOURS
10^2
10^1
10^0
10^-1
10^-2
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
AIRBORNE INHAB. CARGO
AIRBORNE UNINHAB. FIGHTER
AIRBORNE UNINHAB. CARGO & AIRBORNE INHAB. FIGHTER
57290 A
Sheet 4 of 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU-61585S3
MEAN TIME BETWEEN FAILURES [HOURS]
10 8
10 7
10 6
10 5
10 4
25 35 45 55 65 75 85 95 105 115 125
TEMPERATURE case (deg C)
GROUND BENIGN
GROUND FIXED
NAVAL SHELTERED
NAVAL UNSHELTERED
57290 A
Sheet 5 of 6


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU-61585S3
MEAN TIME BETWEEN FAILURES (HOURS)
10⁸
10⁷
10⁶
10⁵
10⁴
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
AIRBORNE INHAB. CARGO
AIRBORNE UNINHAB. FIGHTER
AIRBORNE UNINHAB. CARGO & AIRBORNE INHAB. FIGHTER
57290 A
Sheet 6 of 6

APPENDIX A

The following Reliability Predictions applies to these products:

- BU-61590D5, BU-61590F5.

APPLICATION		REVISIONS			
NEXT ASSY.	USED ON	LETR	DESCRIPTION	DATE	APPROVED
		A	Initial Release	12/01/94	

RELIABILITY PREDICTION REPORT

DDC PART NUMBER: BU-61590
REPORT NUMBER: 57205

Prepared By: _____ 12/1/94
J. McHugh — Date
Quality Assurnace Engineer

Approved By: _____ 12/1/94
J. Sabet, Supervisor — Date
Quality Assurance Engineering

Approved By: _____ 12/1/94
M. Green — Date
Vice President
Product Assurance

REV STATUS OF SHEETS																							
REV																							
SHEET																							
REV STATUS OF SHEETS	REV	A	A	A	A																		
	SHEET	1	2	3	4																		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON FRAC. DEC. ANGLES

MATERIAL

FINISH

PREPARED	MCHUGH	12/94	
CHECKED			
ENGINEER			

DDC
ILC DATA DEVICE CORPORATION
BOHEMIA, NY

RELIABILTY PREDICTION REPORT
DDC PART NUMBER: BU-61590

SIZE	CODE IDENT NO.	
A	19645	57205

SCALE | REV. A | SHEET 1 OF 4

H:\QA\MCHUGH\RELRPT\57205.JM

DDC PART NUMBER: BU-61590
QUALITY LEVEL: B
PACKAGE CONFIGURATION: 78 PIN DIP
ENGINEER: T. HOFFMAN

DOCUMENT DATA FILE (DDF): 53963 REV 4

BILL OF MATERIALS (BM): 53960 REV A ASSEMBLY DRAWING: E53960 REV A

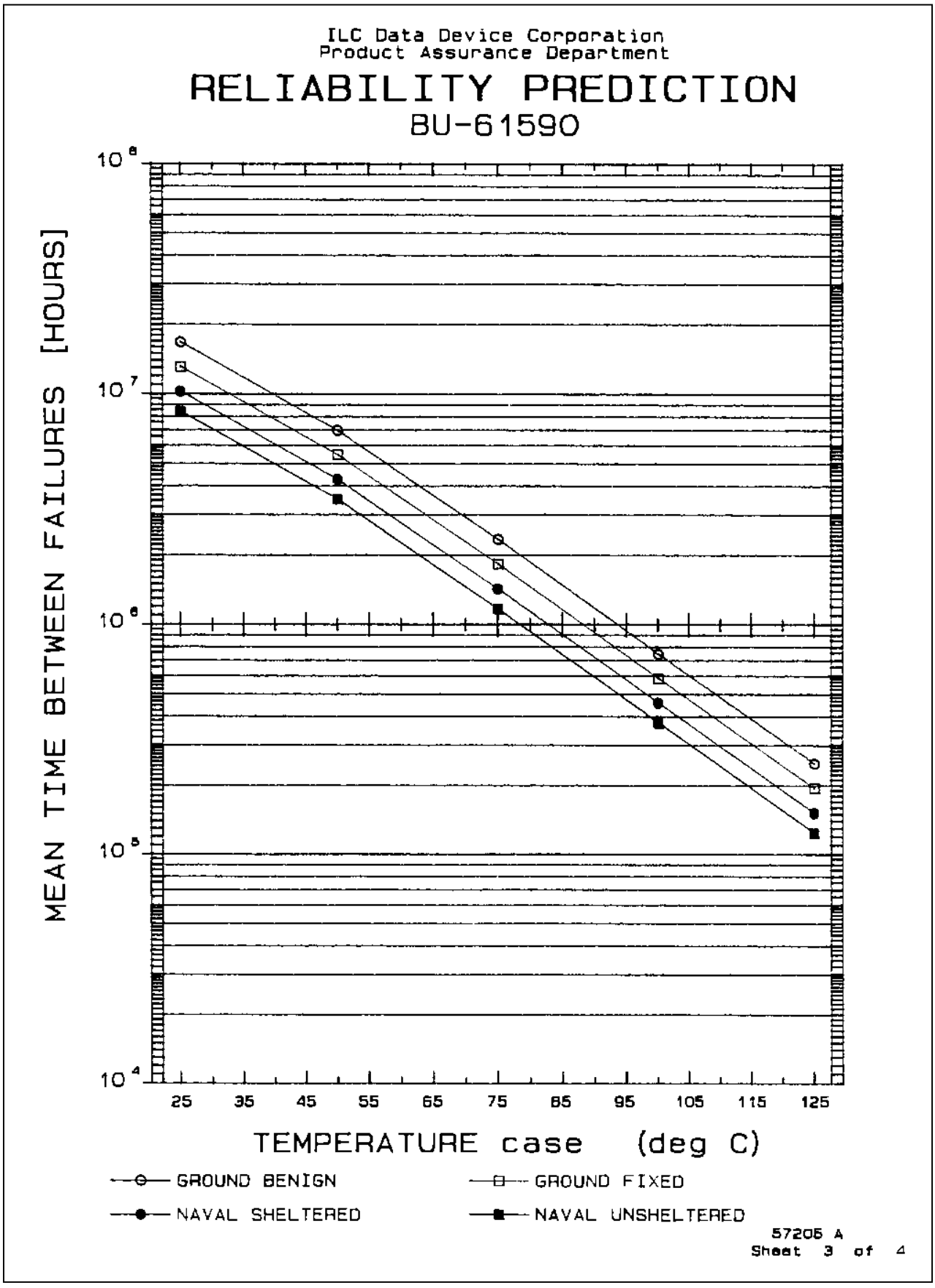
PREDICTIONS ARE IN ACCORDANCE WITH THE METHODOLOGY AND MATH MODELS OF MIL-HDBK-217F, NOTICE 1.

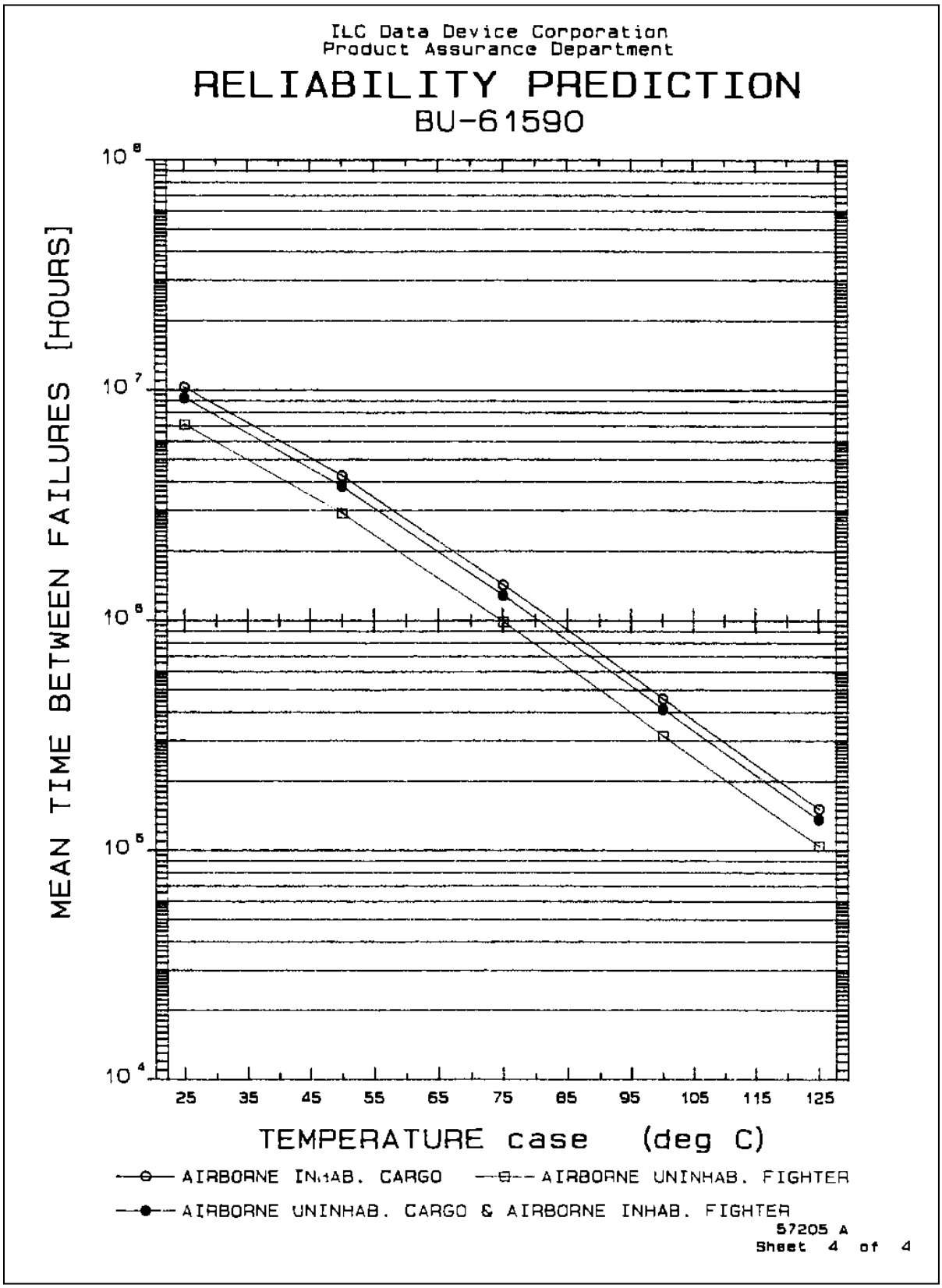
CALCULATIONS WERE PERFORMED USING A CUSTOM MADE SPREADSHEET IN LOTUS 1-2-3 RELEASE 2.01.

APPLICATION DATA AND COMPONENT FAILURE RATE DATA REQUIRED TO PERFORM THESE CALCULATIONS SHALL BE FURNISHED UPON REQUEST.

FAILURE RATES AND MEAN TIME BETWEEN FAILURES FOR SPECIFIED ENVIRONMENTS AT SPECIFIED TEMPERATURES ARE SHOWN BELOW. GRAPHICAL REPRESENTATION SHOWING A RANGE FROM T_C = +25 DEG C TO T_C = +125 DEG C IS INCLUDED IN THIS REPORT.

ENVIRONMENT	TEMPERATURE [CASE, DEG C]	FAILURE RATE [FAILURES/1M HOURS]	M.T.B.F. [HOURS]
GROUND BENIGN	+ 35	0.0821	12,200,000
GROUND FIXED	+ 45	0.151	6,640,000
NAVAL SHELTERED	+ 45	0.194	5,160,000
NAVAL UNSHELTERED	+ 50	0.289	3,470,000
AIR INHABITED CARGO	+ 60	0.359	2,780,000
AIR UNINHABITED CARGO	+ 75	0.780	1,280,000
AIR INHABITED FIGHTER	+ 60	0.399	2,500,000
AIR UNINHABITED FIGHTER	+ 75	1.01	986,000

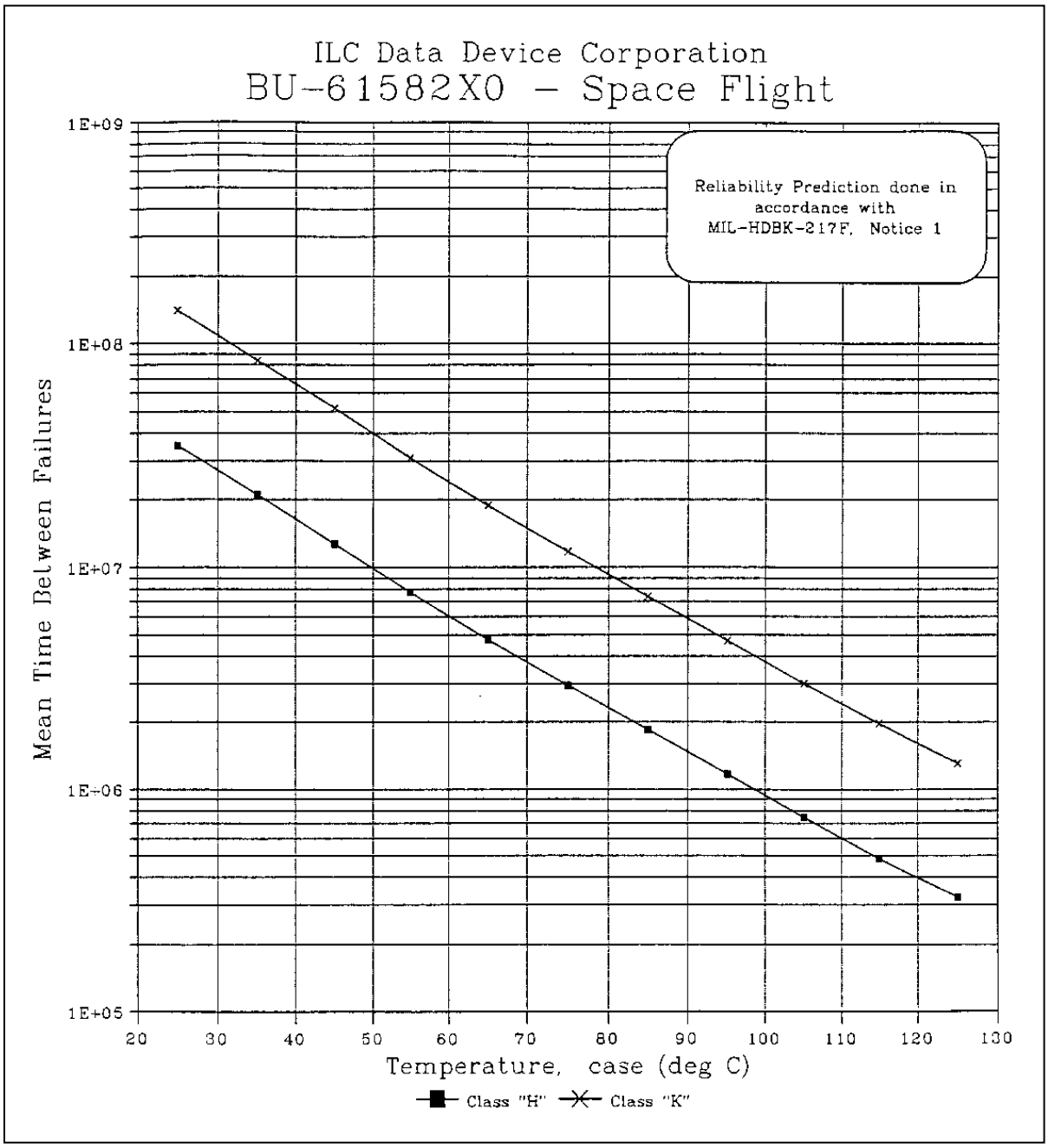

ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU-61590
MEAN TIME BETWEEN FAILURES [HOURS]
10 8
10 7
10 6
10 5
10 4
25 35 45 55 65 75 85 95 105 115 125
TEMPERATURE case (deg C)
GROUND BENIGN
GROUND FIXED
NAVAL SHELTERED
NAVAL UNSHELTERED
57205 A
Sheet 3 of 4


ILC Data Device Corporation
Product Assurance Department
RELIABILITY PREDICTION
BU-61590
MEAN TIME BETWEEN FAILURES [HOURS]
10^8
10^7
10^6
10^5
10^4
25
35
45
55
65
75
85
95
105
115
125
TEMPERATURE case (deg C)
AIRBORNE INHAB. CARGO
AIRBORNE UNINHAB. FIGHTER
AIRBORNE UNINHAB. CARGO & AIRBORNE INHAB. FIGHTER
57205 A
Sheet 4 of 4

APPENDIX A

The following Reliability Predictions applies to these products:

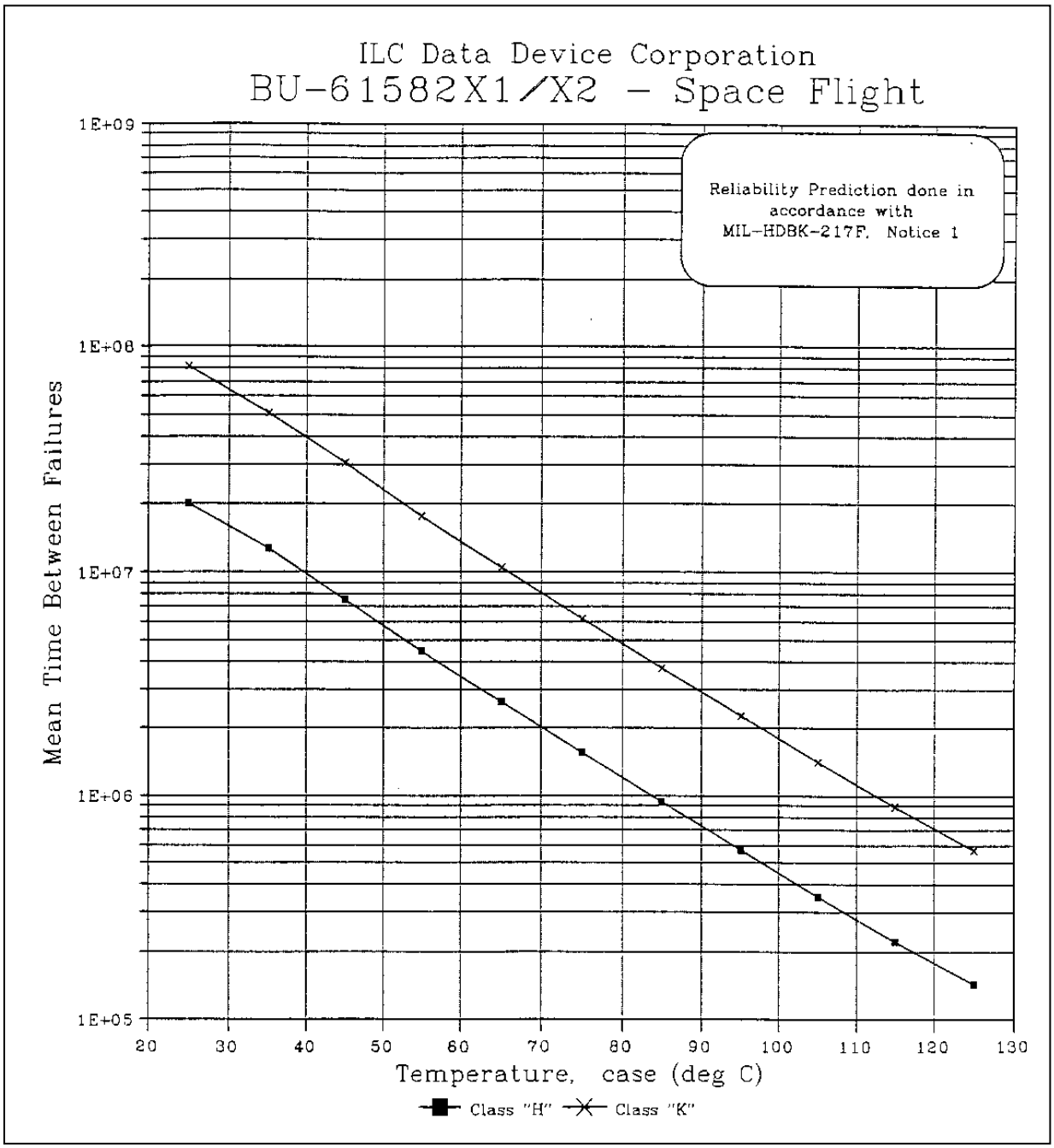
- BU-61582D0, BU-61582F0.


ILC Data Device Corporation
BU-61582X0 – Space Flight
Reliability Prediction done in accordance with MIL-HDBK-217F, Notice 1
Mean Time Between Failures
1E+09
1E+08
1E+07
1E+06
1E+05
20
30
40
50
60
70
80
90
100
110
120
130
Temperature, case (deg C)
Class "H"
Class "K"

APPENDIX A

The following Reliability Predictions applies to these products:

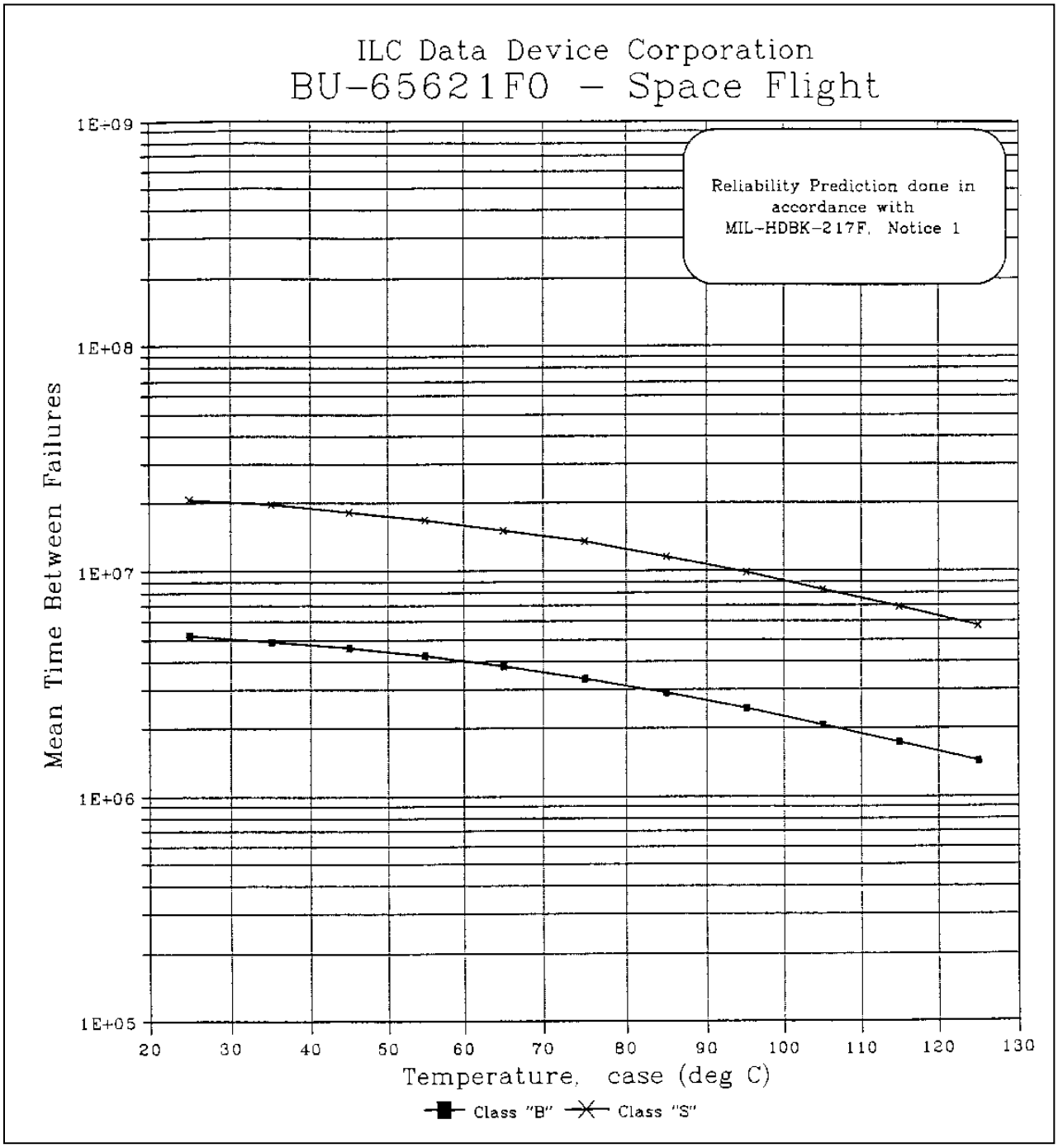
- BU-61582D1, BU-61582D2,
- BU-61582F1, BU-61582F2.


ILC Data Device Corporation
BU-61582X1/X2 – Space Flight
Reliability Prediction done in accordance with MIL-HDBK-217F, Notice 1
Mean Time Between Failures
1E+09
1E+08
1E+07
1E+06
1E+05
20
30
40
50
60
70
80
90
100
110
120
130
Temperature, case (deg C)
Class "H"
Class "K"

APPENDIX A

The following Reliability Predictions applies to these products:

- BU-65621F0.


ILC Data Device Corporation
BU-65621F0 - Space Flight
Reliability Prediction done in accordance with MIL-HDBK-217F, Notice 1
Mean Time Between Failures
1E+09
1E+08
1E+07
1E+06
1E+05
20
30
40
50
60
70
80
90
100
110
120
130
Temperature, case (deg C)
Class "B"
Class "S"

Note: Contact factory to obtain additional reliability data available for the

- BU-65178, BU-61588,
- BU-65179, BU-61688, BU-61689

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A	RELEASE	11/05/96	J.BIVONA

PREPARED BY: _____ DATE 11/5/96
JOHN BIVONA
ENGINEER
DESIGN ENGINEERING

APPROVED BY: _____ DATE 11/6/96
BARRY BECKER
DIRECTOR
DESIGN ENGINEERING

APPROVED BY: _____ DATE 1/9/97
J.SABER
MANAGER
QUALITY ASSURANCE

APPROVED BY: _____ DATE 1/9/97
M.GREEN
VICE PRESIDENT
PRODUCT ASSURANCE

REV STATUS OF SHEETS													
REV	A	A	A	A									
SHEET	1	2	3	4									

DDC
ILC DATA DEVICE CORPORATION
BOHEMIA,N.Y

RELIABILITY PREDICTION REPORT
DDC P/N:BU-61588P3

SIZE	CODE IDENT NO.	59078
A	19645	

SCALE	REV A	SHEET 1 OF 4

DDC PART NUMBER:	BU-61588P3	
QUALITY LEVEL:	B	
PACKAGE CONFIGURATION:	HERMETIC DIP	
ENGINEER:	J.BIVONA	
DOCUMENT DATA FILE (DDF):	A 58562	REV. 1
BILL OF MATERIALS (BM):	BM 58565-1	REV. 2
ASSEMBLY DRAWING:	E 58565	REV. 1

Predictions are in accordance with the methodology and math models of Mil-Hdbk-217F, Notice 2.

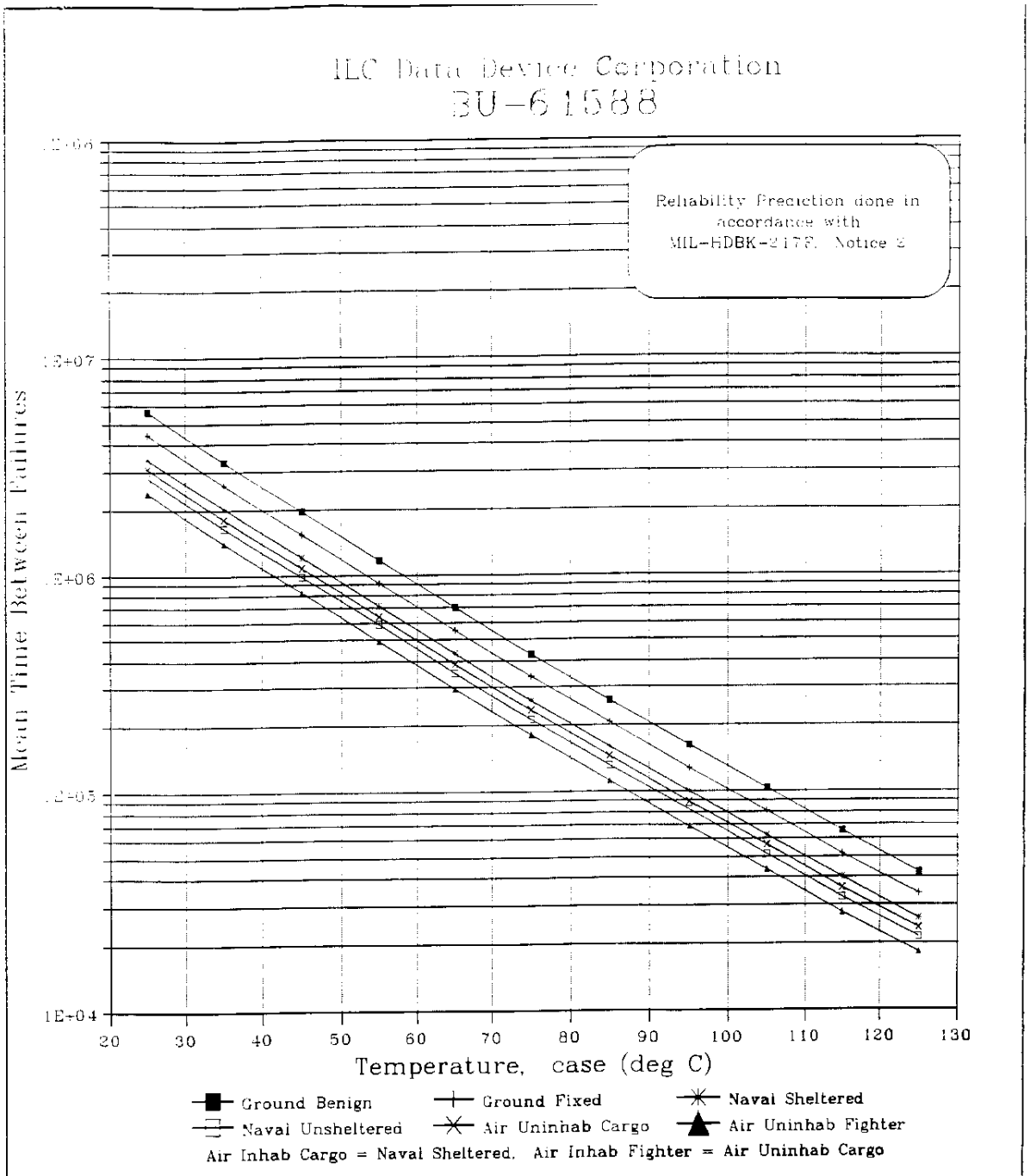
Calculations were performed using a custom made spreadsheet in Quattro Pro release 5.0.

Application data and component failure rate data required to perform these calculations shall be furnished upon request.

Failure Rates and Mean Time Between Failures for specified environments at specified temperatures are shown below. Graphical representation showing range from T_c = +25 deg. C to T_c = +125 deg. C is included in this report.

ENVIRONMENT	TEMPERATURE T_{case} °C	FAILURE RATE Failures/1Mhrs.	M.T.B.F. (Hrs.)
GROUND BENIGN	+35	0.30272	3,300,000
GROUND FIXED	+45	0.64979	1,540,000
NAVAL SHELTERED	+45	0.83545	1,200,000
NAVAL UNSHELTERED	+50	1.3223	756,000
AIR INHABITED CARGO	+60	1.8038	554,000
AIR UNINHABITED CARGO	+75	4.2464	235,000
AIR INHABITED FIGHTER	+60	2.0042	499,000
AIR UNINHABITED FIGHTER	+75	5.5203	181,000

DDC ILC DATA DEVICE CORPORATION BOHEMIA, N.Y.	SIZE A	FSCM NO. 19645	59078 COMPUTER CONTROLLED DOCUMENT
	SCALE	REV. A	SHEET 2


ILC Data Device Corporation
BU-61588
Reliability Prediction done in accordance with MIL-HDBK-217F, Notice 2
Mean Time Between Failures
1E+04
20
30
40
50
60
70
80
90
100
110
120
130
Temperature, case (deg C)
Ground Benign
Ground Fixed
Naval Sheltered
Naval Unsheltered
Air Uninhab Cargo
Air Uninhab Fighter
Air Inhab Cargo = Naval Sheltered, Air Inhab Fighter = Air Uninhab Cargo
DDC
ILC DATA DEVICE CORPORATION
BOHEMIA, N.Y.
SIZE
A
FSCM NO.
19645
59078
COMPUTER CONTROLLED DOCUMENT
SCALE
REV. A
SHEET 3

MIL-HDBK-217F, Notice 1

RELIABILITY PREDICTION- BU-61588 07-Jan-97

	25	45	65	85	105	125
GB	0.1779	0.5106	1.4190	3.8046	9.7322	23.5418
GF	0.2265	0.6498	1.8060	4.8422	12.3864	29.9623
NS	0.2912	0.8355	2.3220	6.2257	15.9254	38.5229
NU	0.3559	1.0211	2.8380	7.6091	19.4644	47.0835
AUC	0.3235	0.9283	2.5800	6.9174	17.6949	42.8032
AUF	0.4206	1.2068	3.3540	8.9926	23.0034	55.6442

		F/R	MTBF
GB	35	0.30272	3,300,000
GF	45	0.64979	1,540,000
NS	45	0.83545	1,200,000
NU	50	1.3223	756,000
AIC	60	1.8038	554,000
AUC	75	4.2464	235,000
AIF	60	2.0042	499,000
AUF	75	5.5203	181,000

DDC ILC DATA DEVICE CORPORATION
BOHEMIA, N.Y.

SIZE	FSCM NO.	59078
A	19645	COMPUTER CONTROLLED DOCUMENT
SCALE	REV. A	SHEET 4

11 APPENDIX B

11.1 TRANSFORMER SUMMARY

11.1.1 ISOLATION TRANSFORMERS FOR USE WITH DDC +5.0 VOLT MIL-STD-1553 TERMINALS

11.1.1.1 Introduction

Voltage source transmitters, such as those used in DDC's +5.0 volt terminals, are sensitive to transformer parasitic leakage inductance. Transformers with large leakage inductants (in effect, large series inductances) may result in excessively long transmitter rise and fall times which can result in a reduction in output amplitude if the slowdown becomes excessive. The higher the leakage inductance, the greater the problem.

11.1.1.2 Design Considerations

Our voltage source design provides superior line driving capability, especially when driving a healthily loaded bus (i.e., high capacitance). This transceiver has been exhaustively tested and characterized for compliance to our published data sheets as well as to MIL-STD-1553, and has successfully passed the RT Validation Test Plan per MIL-HDBK-1553A, Section 100. In addition, for specific products, DDC has verified that it meets the transmitter amplitude requirement for MIL-STD-1760.

As mentioned, reflected leakage inductance is a parameter that must be considered when selecting isolation transformers to be used with any of these products. For transformer-coupled (stub-coupled) terminals of transceivers, the maximum allowable reflected leakage inductance is 6.0µH and a maximum reflected leakage inductance imbalance must be less than 1.0µH. For direct-coupled (stub-coupled) terminals of transceivers, the maximum allowable reflected leakage inductance is 12.0µH and the maximum reflected leakage inductance imbalance must be less than 2.0µH.

If these limits are exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553. In addition, an excessive leakage imbalance may result in a dynamic offset (output symmetry) that exceeds 1553 specifications.

11.1.1.3 Test Method

Reflected leakage inductance should be measured as follows: the side of the transformer that connect to the terminal or transceiver hybrid is defined as the "primary" winding. If on side of the primary is shorted to the primary center-tap, the primary-to-secondary reflected inductance should be measured across the "secondary" (stub-side) winding. This

inductance must be less than 6.0 µH for stub-coupled and 12.0 µH for direct coupled. Similarly, if the other side of the primary is shorted to the primary center-tap, the reflected inductance measured across the "secondary" (stub-side) winding must also be less than 6.0 µH for stub-coupled and 12.0 µH for direct coupled. The difference between these two measurements is the "differential" leakage inductance. This value must be less than 1.0 µH for stub-coupled terminals and 2.0 µH for direct-coupled terminals.

11.1.1.4 Suitable Transformer from Beta Transformer Technology Corporation

Beta Transformer Technology Corporation (BTTC) manufactures transformers in a variety of mechanical configurations with the required turns ratios of 1.0:2.5 direct coupled, and 1.0:1.79 transformer coupled. The table below provides a listing of many of these transformers. Except where noted, all transformers in this table meet the leakage inductance requirements described in this section and therefore may be used with DDC +5.0 Volt terminal products. For further information, contact BTTC at 631-244-7393 or at www.bttcbeta.com.

TABLE 151. BTTC +5.0 Volt Transformers for use with Integrated Terminals

Transformer Configuration	BTTC Part Number
Single epoxy transformer, through-hole, 0.625" x 0.625", 0.250" max height	**B-3067** **B-3226**
Single epoxy transformer, through-hole with stand-offs, 0.625" x 0.625", 0.275" max height	**B-3225**
Single epoxy transformer, surface mount, 0.625" x 0.625", 0.275" max height	**B-3227**
Single epoxy transformer, through-hole, 0.350" x 0.500", 0.275" max height	**B-3229** **B-3230**
Single epoxy transformer, flat pack, 0.625" x 0.625", 0.275" max height	**B-3231**
Single epoxy transformer, through-hole, 0.625" x 0.625", 0.220" max height	**B-3818 (see note 1)**
Single epoxy transformer, surface mount, 0.625" x 0.625", 0.220" max height	**B-3819 (see note 1)**
Single epoxy transformer, flat pack, 0.625" x 0.625", 0.220" max height	**B-38920 (see note 1)**
Single epoxy transformer, flat pack, 0.625" x 0.625", 0.150" max height	**LPB-5014**
Single epoxy transformer, surface mount, 0.625" x 0.625", 0.150" max height	**LPB-5015**
Dual epoxy transformer, twin stacked, through hole, 0.625" x 0.625", 0.320" max height	**TST-9107**
Dual epoxy transformer, twin stacked, surface mount, 0.625" x 0.625", 0.320" max height	**TST-9117**
Dual epoxy transformer, twin stacked, flat pack, 0.625" x 0.625", 0.320" max height	**TST-9127**
Dual epoxy transformer, twin stacked, through hole, 0.625" x 0.625", 0.290" max height	**TST-9007**
Dual epoxy transformer, twin stacked, surface mount, 0.625" x 0.625", 0.290" max height	**TST-9017**
Dual epoxy transformer, twin stacked, flat pack, 0.625" x 0.625", 0.290" max height	**TST-9027**
Dual epoxy transformer, side-by-side, through-hole, 0.990" x 0.690", 0.155" max height	**TLP-1205/B-3300**
Dual epoxy transformer, side-by-side, flat pack, 0.930" x 0.630", 0.155" max height	**TLP-1105/B-3261**
Dual epoxy transformer, side-by-side, surface mount, 0.990" x 0.630", 0.155" max height	**TLP-1005/B-3310**

TABLE 151. BTTC +5.0 Volt Transformers for use with Integrated Terminals	
Transformer Configuration	**BTTC Part Number**
Single epoxy transformer, flat pack, 0.750” x 0.750”, 0.130” max height	**SLP-8124 (see note 2)**
Single epoxy transformer, surface mount, 0.750” x 0.750”, 0.190” max height	**SLP-8107 (see note 2)**
Dual epoxy transformer, side-by-side, flat pack, 1.410” x 0.750”, 0.130” max height	**DLP-7114 (see note 2)**
Dual epoxy transformer, side-by-side, surface mount, 1.410” x 0.750”, 0.130” max height	**DLP-7115 (see note 2)**
Single nickel-plated kovar transformer, flat pack, 0.690” x 0.690”, 0.175” max height	**HLP-6014**
Single nickel-plated kovar transformer, surface mount, 0.630” x 0.630”, 0.175” max height	**HLP-6015**
Single epoxy transformer, surface mount, 0.400” x 0.400”, 0.185” max height	**MLP-2005 (see note 2)**
Single epoxy transformer, surface mount, 0.400” x 0.400”, 0.185” max height	**MLP-2205 (see note 2)**
Single epoxy transformer, surface mount, 0.400” x 0.400”, 0.280” max height	**MMT-3005**
Single epoxy transformer, surface mount, 0.400” x 0.400”, 0.260” max height	**MMT-3205**
NOT RECOMMENDED	**DLP-7014** **DLP-7015** **SLP-8007** **SLP-8024**

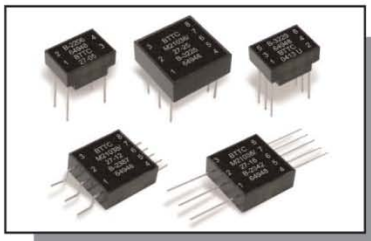
Notes:

1. Only the B-3819 and B-3820 can be used with McAir-compatible transceivers (i.e. products with a last digit suffix o “4” rather than “3”). All others, except for the 4 non-recommended transformers (DLP-7014, DLP-7015, SLP-8007, and SLP-8024(can be used with +5.0 Volt MIL-STD-1553 transceivers (i.e., products with a last digit suffix of “3”)

2. Operates to +105°C max. All other transformers operate to +125°C max.

BETA TRANSFORMER TECHNOLOGY CORPORATION
A Subsidiary of Data Device Corporation
40 Orville Drive, Bohemia, NY 11716-2529
Phone: (631) 244-7393; Fax: (631) 244-8893
Web site: www.bttc-beta.com

B-2200/2300/3200 SERIES



MIL-STD-1553 TRANSFORMERS FULLY QUALIFIED TO DESC SPECIFICATION MIL-PRF-21038/27

DESCRIPTION AND APPLICATIONS

The military data bus specification, MIL-STD-1553, has brought about the need for versatile pulse transformers that meet all the electrical requirements of Manchester II serial bi-phase data transmission. The B-2200/2300/3200 series of transformers provide the turns ratio configurations, component isolation, and common mode rejection ratio characteristics necessary for MIL-STD-1553A and B compliance.

The step-up and step-down ratios that are available with the B-2200/2300/3200 series complement DDC's entire MIL-STD-1553 product line. These transformers are low-profile, modular units that are multi-tapped to accommodate existing system configurations. Encapsulated in accordance with MIL-PRF-21038, their SN63 solder-dipped copper-clad steel leads conveniently accommodate printed circuit board mounting. Sinusoidal or trapezoidal waveforms are accurately processed, making the B-2200/2300/3200 series of transformers an excellent choice for any MIL-STD-1553A or B application.

FEATURES

- ***Fully Qualified to DESC Specification No. 21038/27***
- ***For use with MIL-STD-1553A and B, MacAir A-5690, A-5232, and A-4905***
- ***Low-Profile***
- ***-55°C to +130°C Operating Temperature Range***
- ***Built and Tested to MIL-PRF-21038 Level M, Level T available***
- ***Listed On QPL-21038-31***
- ***Qualification Validated Annually***

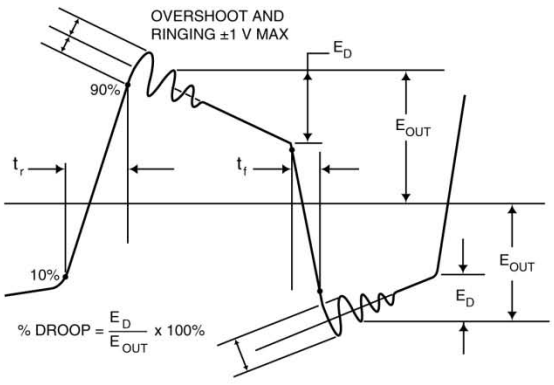


FIGURE 1. WAVEFORM INTEGRITY

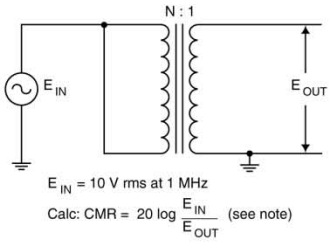


FIGURE 2. CIRCUIT FOR COMMON MODE REJECTION

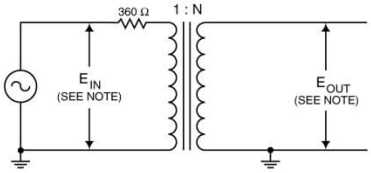


FIGURE 3. CIRCUIT FOR WAVEFORM INTEGRITY

Note: Input to be applied and output to be measured for all dash numbers are as shown. N represents highest turns winding in each test.

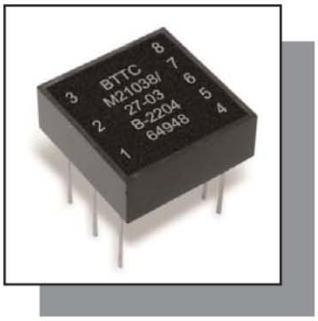
© 1989, 1999 Data Device Corporation

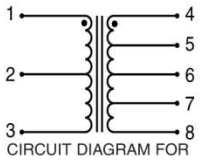
BETA TRANSFORMER TECHNOLOGY CORP • 40 ORVILLE DRIVE • BOHEMIA NY 11716-2529 • 631-244-7393 • FAX 631-244-8893

TABLE 1. B-2200/2300/3200 SERIES SPECIFICATIONS

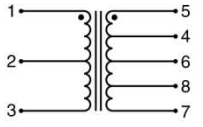
PARAMETER	UNIT	VALUE	REMARK
Case			Flame Resistant, DIALLYL PHTHALATE
Terminals			SN63 Solder-Dipped Copper-Clad Steel
Weight	oz (gm)	0.175 (5) max	
Terminal Strength	lbs	2	2 pounds applied force, Method 211, MIL-STD-202, Test condition A
Dielectric Withstanding Voltage	Vrms	100	Method 301, MIL-STD-202
Life (expectancy "X")	Hrs	10,000 min	In accordance with MIL-PRF-21038
Insulation Resistance	M Ohm	1,000 min	At 250 Vdc using method 302, test condition B, MIL-STD-202
Pulse Width (of Output Pulse)	µs	2	Tested using FIGURE 3 with resulting FIGURE 1 waveform.
Overshoot	V	<1	Tested using FIGURE 3 with resulting FIGURE 1 waveform.
Rise Time (of Output Pulse)	ns		Tested using FIGURE 3 with resulting FIGURE 1 waveform. See Respective ELECTRICAL CHARACTERISTICS TABLE
Common Mode Rejection	db	45 min	Tested using FIGURE 2.
Operating Temperature Range	°C	-55 to +130	
Droop	%	20 max	Tested using FIGURE 3 with resulting FIGURE 1 waveform.
DC Resistance	Ohm		See respective ELECTRICAL CHARACTERISTICS TABLE
Input Impedance	Ohm		See respective ELECTRICAL CHARACTERISTICS TABLE

CONFIGURATION A

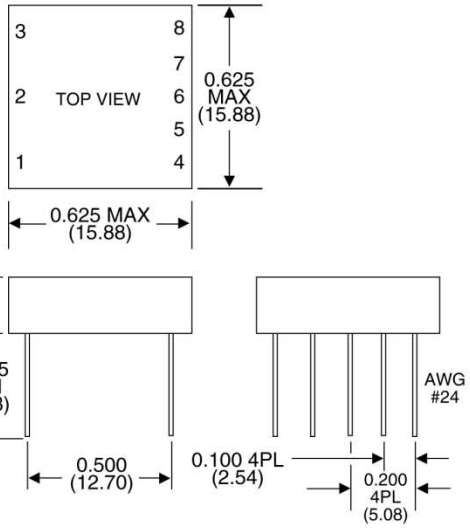




CIRCUIT DIAGRAM FOR DASH NUMBERS -01, -02, -03, -10 AND -26



CIRCUIT DIAGRAM FOR DASH NUMBER -04



Notes:
(1) Dimensions are in inches (mm).
(2) Unless otherwise specified, tolerance is ±0.010 inches (0.25mm)

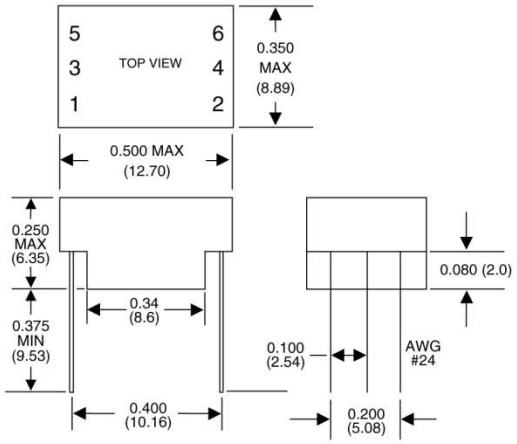
TABLE 2. ELECTRICAL CHARACTERISTICS - CONFIGURATION A

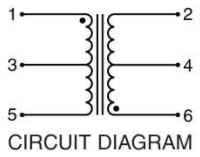
BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	"A" (max)	DC RESISTANCE Ω (MAX)	OUTPUT RISETIME (MAX)	IMPEDANCE Ω (MIN)
B-2202	M-21038/27-01	1:1 ±3% 1:0.707 ±3%	1-3 1-3	4-8 5-7	0.300	1-3 3.0 4-8 3.0	150 ns	(1-3) 4,000
B-2203	M-21038/27-02	1.4:1 ±3% 2:1 ±3%	1-3 1-3	4-8 5-7	0.250	1-3 3.5 4-8 3.0	150 ns	(1-3) 7,200
B-2204	M-21038/27-03	1.25:1 ±3% 1.66:1 ±3%	1-3 1-3	4-8 5-7	0.250	1-3 3.2 4-8 3.0	150 ns	(1-3) 4,000
B-2205	M-21038/27-04	2.3:1 ±3% 3.2:1 ±3%	1-3 1-3	4-8 5-7	0.300	1-3 1.2 4-8 3.0	150 ns	(5-7) 3,000
B-2385	M-21038/27-10	2.12:1 ±3% 1.5:1 ±3%	4-8 5-7	1-3 1-3	0.250	1-3 1.0 4-8 3.0	200 ns	(4-8) 4,000
B-3226	M-21038/27-26	1:2.5 ±3% 1:1.79 ±3%	1-3 1-3	4-8 5-7	0.250	1-3 1.0 4-8 3.5	250 ns	(4-8) 4,000

Note:
Wave soldering method shall preheat leads to a temperature of 100° C minimum and 140° C maximum at a rate of 2° C per second. Solder wave temperature to be 245° C nominal, 265° C maximum, with a nominal dwell time of 3 seconds and a maximum dwell time of 5 seconds.

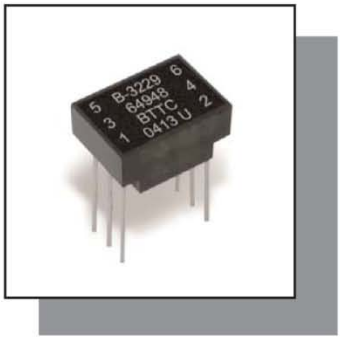
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CONFIGURATION B





CIRCUIT DIAGRAM



Notes:
(1) Dimensions are in inches (mm).
(2) Unless otherwise specified, tolerance is ±0.010 inches (0.25mm)

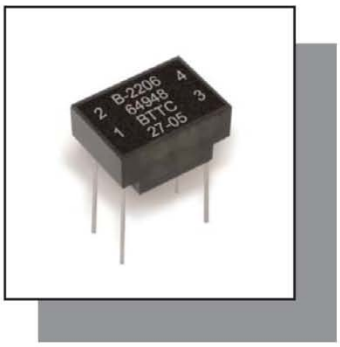
TABLE 3. ELECTRICAL CHARACTERISTICS - CONFIGURATION B

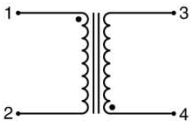
BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE Ω (MAX)	OUTPUT RISETIME (MAX)	IMPEDANCE Ω (MIN)
B-2207	M-21038/27-06	1:1 ±3%	1-5	2-6	1-5 2.5 2-6 2.8	150 ns	(1-5) 3,000
B-2208	M-21038/27-07	1:1.41 ±3%	1-5	2-6	1-5 2.2 2-6 2.7	150 ns	(2-6) 3,000
B-2209	M-21038/27-08	1:1.66 ±3%	1-5	2-6	1-5 1.5 2-6 2.4	150 ns	(2-6) 3,000
B-2210	M-21038/27-09	1:2 ±3%	1-5	2-6	1-5 1.3 2-6 2.6	200 ns	(2-6) 3,000
B-3228	M-21038/27-28	1:1.5 ±3%	1-5	2-6	1-5 0.90 2-6 2.5	150 ns	(2-6) 3,000
B-3229	M-21038/27-29	1:1.79 ±3%	1-5	2-6	1-5 0.90 2-6 2.5	150 ns	(2-6) 3,000
B-3230	M-21038/27-30	1:2.5 ±3%	1-5	2-6	1-5 1.0 2-6 2.8	250 ns	(2-6) 3,000

Note:
Wave soldering method shall preheat leads to a temperature of 100° C minimum and 140° C maximum at a rate of 2° C per second. Solder wave temperature to be 245° C nominal, 265° C maximum, with a nominal dwell time of 3 seconds and a maximum dwell time of 5 seconds.

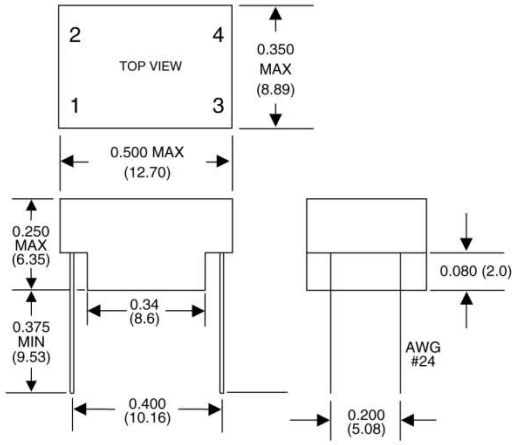
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CONFIGURATION C





CIRCUIT DIAGRAM



Notes:
(1) Dimensions are in inches (mm).
(2) Unless otherwise specified, tolerance is ±0.010 inches (0.25mm)

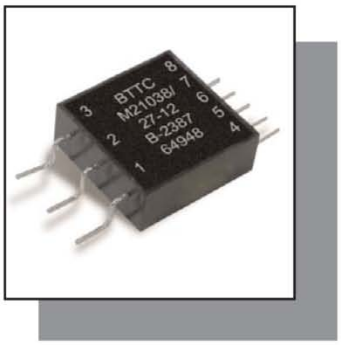
TABLE 4. ELECTRICAL CHARACTERISTICS - CONFIGURATION C

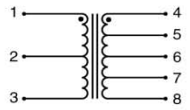
BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE Ω (MAX)	OUTPUT RISETIME (MAX)	IMPEDANCE Ω (MIN)
B-2206	M-21038/27-05	1:1.41 ±3%	1-2	3-4	1-2 2.2 3-4 2.7	150 ns	(3-4) 3,000

Note:
Wave soldering method shall preheat leads to a temperature of 100° C minimum and 140° C maximum at a rate of 2° C per second. Solder wave temperature to be 245° C nominal, 265° C maximum, with a nominal dwell time of 3 seconds and a maximum dwell time of 5 seconds.

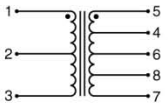
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CONFIGURATION D

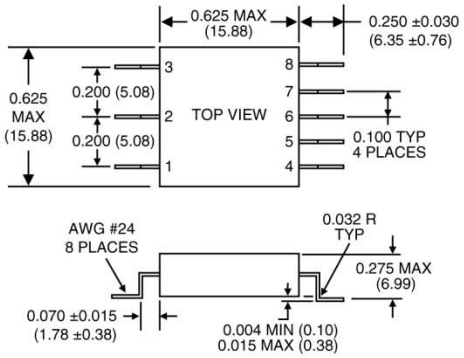




CIRCUIT DIAGRAM FOR
DASH NUMBERS -11,
-12, -13, -15, AND -27



CIRCUIT DIAGRAM FOR
DASH NUMBER -14



Notes:
(1) Dimensions are in inches (mm).
(2) Unless otherwise specified, tolerance is ±0.010 inches (0.25mm)

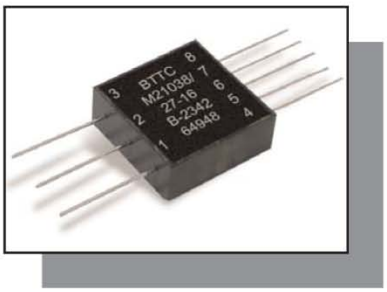
TABLE 5. ELECTRICAL CHARACTERISTICS - CONFIGURATION D

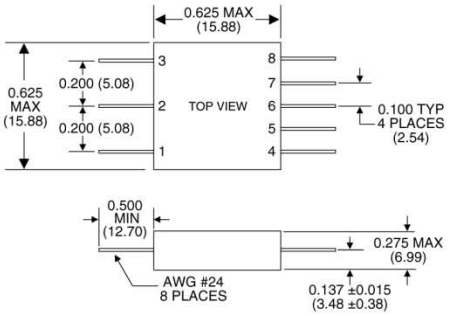
BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE Ω (MAX)	OUTPUT RISETIME (MAX)	IMPEDANCE Ω (MIN)
B-2386	M-21038/27-11	1:1 ±3% 1:0.707 ±3%	1-3 1-3	4-8 5-7	1-3 3.0 4-8 3.0	150 ns	(1-3) 4,000
B-2387	M-21038/27-12	1.4:1 ±3% 2:1 ±3%	1-3 1-3	4-8 5-7	1-3 3.5 4-8 3.0	150 ns	(1-3) 7,200
B-2388	M-21038/27-13	1.25:1 ±3% 1.66:1 ±3%	1-3 1-3	4-8 5-7	1-3 3.2 4-8 3.0	150 ns	(1-3) 4,000
B-2389	M-21038/27-14	2.3:1 ±3% 3.2:1 ±3%	4-8 5-7	1-3 1-3	1-3 1.2 4-8 3.0	150 ns	(5-7) 3,000
B-2390	M-21038/27-15	2.12:1 ±3% 1.5:1 ±3%	4-8 5-7	1-3 1-3	1-3 1.0 4-8 3.0	200 ns	(4-8) 4,000
B-3227	M-21038/27-27	1:2.5 ±3% 1:1.79 ±3%	1-3 1-3	4-8 5-7	1-3 1.0 4-8 3.5	250 ns	(4-8) 4,000

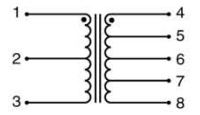
Note:
1) These transformers have been classified as Level 5A per IPC-9503 and must be processed accordingly. To ensure product integrity and maintain the product warranty, these transformers require a 24 hour bake at +125° C prior to any solder reflow processing. Dried transformers must be reflowed within 24 hours. J-STD-033 preconditioning (dry-pack) can be provided by Beta upon request. Reflow process must not cause the peak body temperature of the device to exceed 225° C and must not expose the device to temperatures above 183° C for more than 90 seconds.
2) By providing surface mount parts that have been dried per IPC-9503 (Moisture Sensitivity Classification for Non-IC components) and Dry-Packed in accordance with J-STD-033 (Standard for handling, packing, shipping and use of Moisture /Reflow sensitive surface mount devices), Beta has significantly reduced the possibility of moisture sensitivity/reflow induced "Pop-corning" or Bulging during customer's reflow soldering process. Experiments performed by Beta and data provided by manufacturers of similar devices indicate that post reflow visual/mechanical anomolies can be reduced by more than 90%. Since customer reflow profiles and CCA Density can vary, Beta recommends that the customer verify solder process compatibility and yield assessment of these devices.

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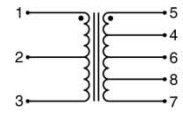
CONFIGURATION E







CIRCUIT DIAGRAM FOR
DASH NUMBERS -16, -17,
-18, -20 AND -31



CIRCUIT DIAGRAM FOR
DASH NUMBER -19

Notes:
(1) Dimensions are in inches (mm).
(2) Unless otherwise specified, tolerance is ±0.010 inches (0.25mm)

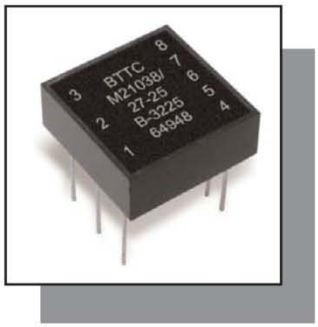
TABLE 6. ELECTRICAL CHARACTERISTICS - CONFIGURATION E

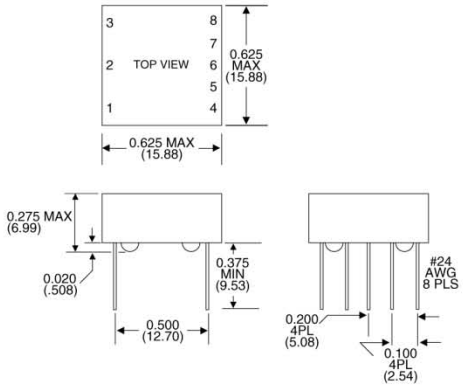
BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE Ω (MAX)	OUTPUT RISETIME (MAX)	IMPEDANCE Ω (MIN)
B-2342	M-21038/27-16	1:1 ±3% 1:0.707 ±3%	1-3 1-3	4-8 5-7	1-3 3.0 4-8 3.0	150 ns	(1-3) 4,000
B-2343	M-21038/27-17	1.4:1 ±3% 2:1 ±3%	1-3 1-3	4-8 5-7	1-3 3.5 4-8 3.0	150 ns	(1-3) 7,200
B-2344	M-21038/27-18	1.25:1 ±3% 1.66:1 ±3%	1-3 1-3	4-8 5-7	1-3 3.2 4-8 3.0	150 ns	(1-3) 4,000
B-2345	M-21038/27-19	2.3:1 ±3% 3.2:1 ±3%	4-8 5-7	1-3 1-3	1-3 1.2 4-8 3.0	150 ns	(5-7) 3,000
B-2391	M-21038/27-20	2.12:1 ±3% 1.5:1 ±3%	4-8 5-7	1-3 1-3	1-3 1.0 4-8 3.0	200 ns	(4-8) 4,000
B-3231	M-21038/27-31	1:2.5 ±3% 1:1.79 ±3%	1-3 1-3	4-8 5-7	1-3 1.0 4-8 3.5	250 ns	(4-8) 4,000

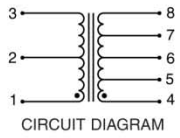
Note:
1) These transformers have been classified as Level 5A per IPC-9503 and must be processed accordingly. To ensure product integrity and maintain the product warranty, these transformers require a 24 hour bake at +125° C prior to any solder reflow processing. Dried transformers must be reflowed within 24 hours. J-STD-033 preconditioning (dry-pack) can be provided by Beta upon request. Reflow process must not cause the peak body temperature of the device to exceed 225° C and must not expose the device to temperatures above 183° C for more than 90 seconds.
2) By providing surface mount parts that have been dried per IPC-9503 (Moisture Sensitivity Classification for Non-IC components) and Dry-Packed in accordance with J-STD-033 (Standard for handling, packing, shipping and use of Moisture /Reflow sensitive surface mount devices), Beta has significantly reduced the possibility of moisture sensitivity/reflow induced "Pop-corning" or Bulging during customer's reflow soldering process. Experiments performed by Beta and data provided by manufacturers of similar devices indicate that post reflow visual/mechanical anomolies can be reduced by more than 90%. Since customer reflow profiles and CCA Density can vary, Beta recommends that the customer verify solder process compatibility and yield assessment of these devices.

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CONFIGURATION F







Notes:
(1) Dimensions are in inches (mm).
(2) Unless otherwise specified, tolerance is ±0.010 inches (0.25mm)

TABLE 7. ELECTRICAL CHARACTERISTICS - CONFIGURATION F

BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE Ω (MAX)	OUTPUT RISETIME (MAX)	IMPEDANCE Ω (MIN)
B-3221	M-21038/27-21	1:1 ±3% 1:0.707 ±3%	1-3 1-3	4-8 5-7	1-3 3.0 4-8 3.0	150 ns	(1-3) 4,000
B-3222	M-21038/27-22	1.4:1 ±3% 2:1 ±3%	1-3 1-3	4-8 5-7	1-3 3.5 4-8 3.0	150 ns	(1-3) 7,200
B-3223	M-21038/27-23	1.25:1 ±3% 1.66:1 ±3%	1-3 1-3	4-8 5-7	1-3 3.2 4-8 3.0	150 ns	(1-3) 4,000
B-3224	M-21038/27-24	1:2.12 ±3% 1:1.50 ±3%	1-3 1-3	4-8 5-7	1-3 1.2 4-8 3.0	200 ns	(4-8) 4,000
B-3225	M-21038/27-25	1:2.5 ±3% 1:1.79 ±3%	1-3 1-3	4-8 5-7	1-3 1.0 4-8 3.5	250 ns	(4-8) 4,000

Note:
Wave soldering method shall preheat leads to a temperature of 100° C minimum and 140° C maximum at a rate of 2° C per second. Solder wave temperature to be 245° C nominal, 265° C maximum, with a nominal dwell time of 3 seconds and a maximum dwell time of 5 seconds.

The information in this data sheet is believed to be accurate; however, no responsibility is assumed by Beta Transformer Technology Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.

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Phone: (631) 244-7393; Fax: (631) 244-8893
Web site: www.bttc-beta.com

L-04/08-0

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12 APPENDIX C

12.1 BREADBOARDING SOCKET

Note: *DDC does not supply the* ***QIP70 or QGSO78 sockets****. This information is provided for reference purposes only. Please contact* Ironwood Electronics or Advanced Interconnections *for more information on the breadboarding sockets shown.*

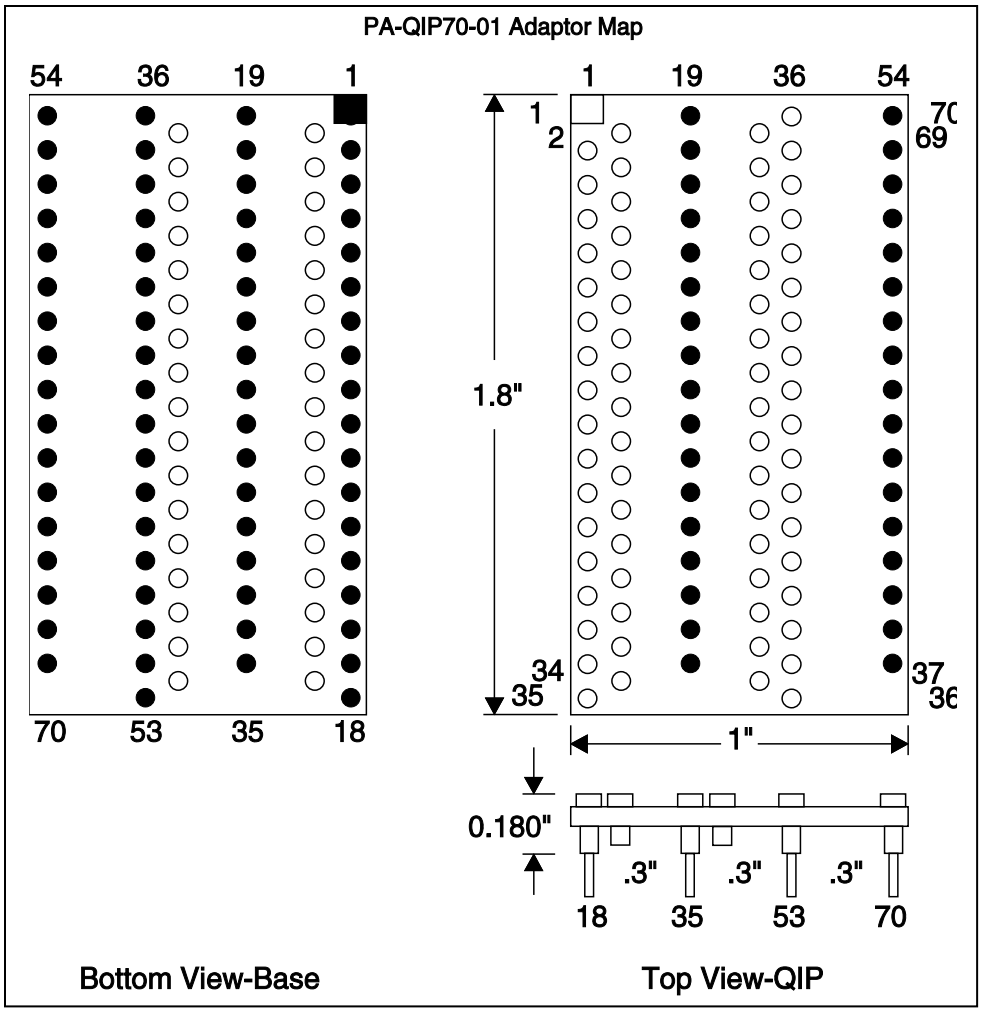
DDC does not supply the ***72-Lead CQFP Test Socket****. This information is provided for reference purposes only. Please contact Azimuth Electronics, Inc. for more information on the breadboarding sockets shown.*

Ironwood Electronics, Inc.
P.O. Box 21151
St. Paul, MN 55121
Tel: (651) 452-8100
Tel: (800) 404-0204
Fax: (651) 452-8400
Web site: www.ironwoodelectronics.com

Advanced Interconnections
5 Energy Way
West Warwick, RI 02893
Tel: (401) 823-5200
Tel: (800) 424-9850
Fax: (401) 823-8723
Web site: www.advintcorp.com

Azimuth Electronics, Inc.
2605 South El Camino Real
San Clemente, CA 92672 USA
Tel: (949) 492-6481
http://www.azimuth-electronics.com

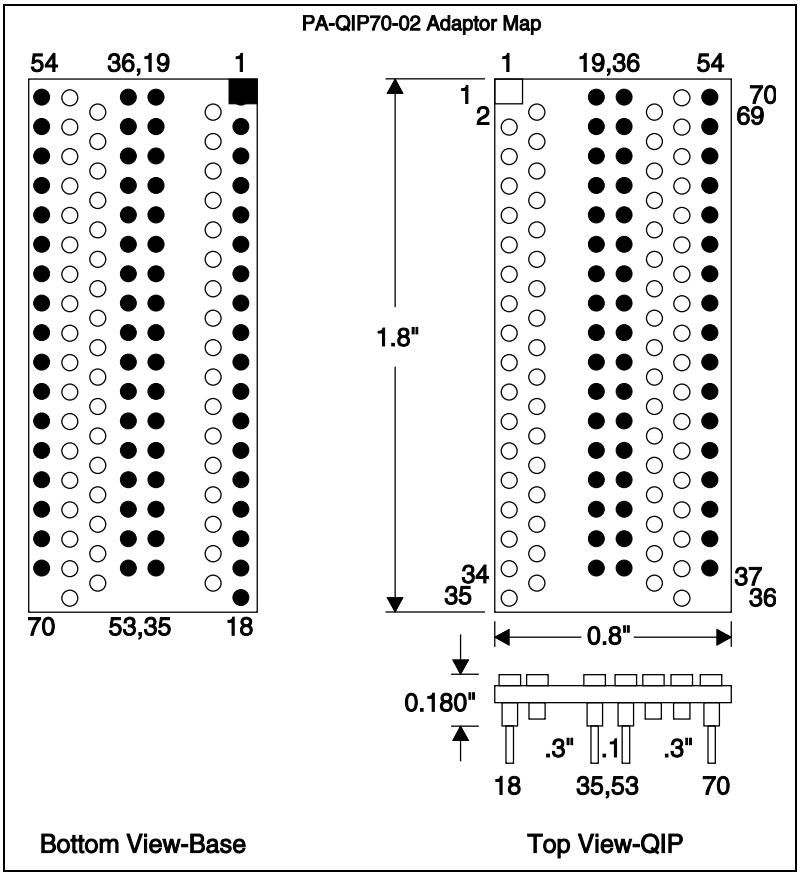
Ironwood Electronics, Inc., P.O. Box 21151, St. Paul, MN 55121, Tel: (800) 404-0204
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QIP	Base	QIP	Base	QIP	Base	QIP	Base	QIP	Base	QIP	Base	QIP	Base	QIP	Base
1	1	10	23	19	10	28	32	37	70	46	48	55	61	64	39
2	19	11	6	20	28	29	15	38	52	47	65	56	43	65	56
3	2	12	24	21	11	30	33	39	69	48	47	57	60	66	38
4	20	13	7	22	29	31	16	40	51	49	64	58	42	67	55
5	3	14	25	23	12	32	34	41	68	50	46	59	59	68	37
6	21	15	8	24	30	33	17	42	50	51	63	60	41	69	54
7	4	16	26	25	13	34	35	43	67	52	45	61	58	70	36
8	22	17	9	26	31	35	18	44	49	53	62	62	40		
9	5	18	27	27	14	36	53	45	66	54	44	63	57		

NOTE: QIP sockets are numerically mapped to base pins.

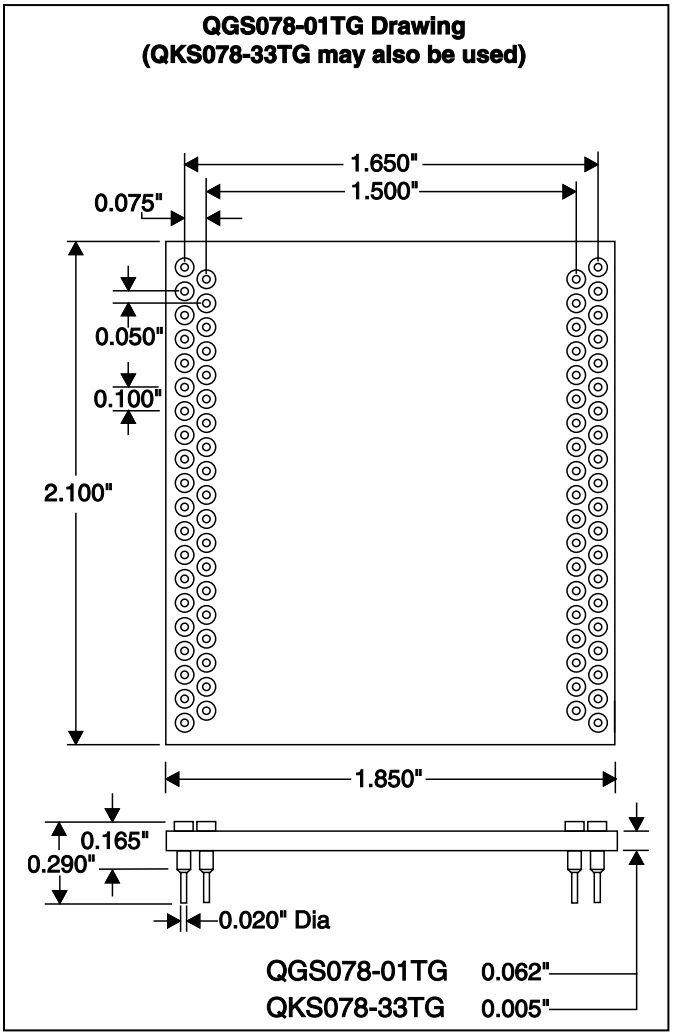
Ironwood Electronics, Inc., P.O. Box 21151, St. Paul, MN 55121, Tel: (800) 404-0204
© Ironwood Electronics, Inc.



QIP	Base	QIP	Base	QIP	Base	QIP	Base	QIP	Base
1	1	15	8	29	15	43	67	57	60
2	19	16	26	30	33	44	49	58	42
3	2	17	9	31	16	45	66	59	59
4	20	18	27	32	34	46	48	60	41
5	3	19	10	33	17	47	65	61	58
6	21	20	28	34	35	48	47	62	40
7	4	21	11	35	18	49	64	63	57
8	22	22	29	36	53	50	46	64	39
9	5	23	12	37	70	51	63	65	56
10	23	24	30	38	52	52	45	66	38
11	6	25	13	39	69	53	62	67	55
12	24	26	31	40	51	54	44	68	37
13	7	27	14	41	68	55	61	69	54
14	25	28	32	42	50	56	43	70	36

NOTE: QIP sockets are numerically mapped to base pins.

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Substrate: FR4/G10, 0.0625"±0.007" thick.

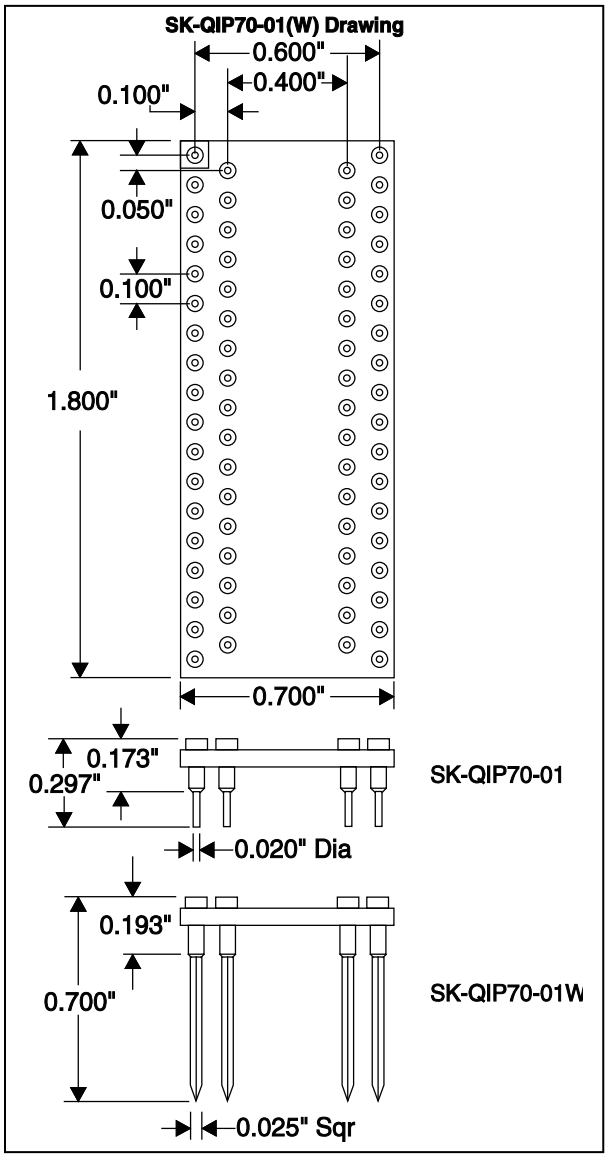
Pins: Socket/Terminal, LIF contact

Shell: Material; Brass Alloy 360, 1/2 Hard, plating; 10μ" Gold over 50μ" Nickel

Contact: Material; Beryllium Copper Alloy 172, HT, Plating; 10⌠" Gold over 50⌠" Nickel, Insertion force; 2.3 Oz w/0.018" round pin.

Drawing By: M. Tully	Date: 11/10/93	File Name: SK-QIP70-01(W) Dwg		
Modified By: P Jasmin	Date: 6/30/94	ECO#:	View: V1	Scale: 2:1

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Substrate: FR-4, 0.0625"±0.007" thick for the QGS; Polymide Film, 0.005" thick for the QKS.

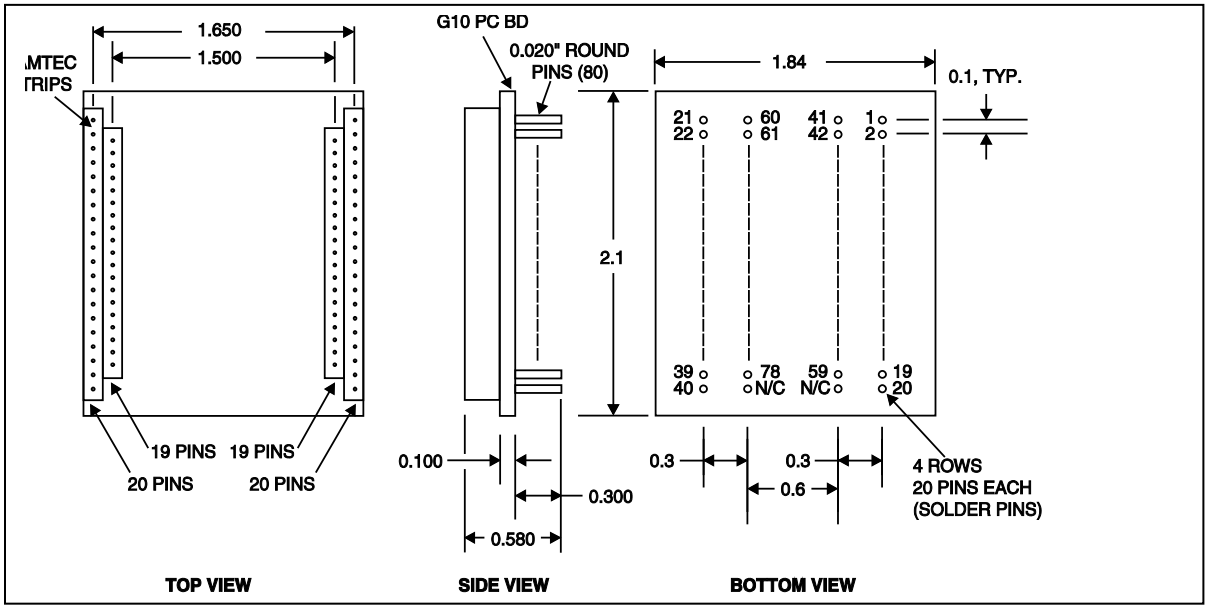
Pins: Socket/Terminal, LIF contact

Shell: Material: Brass Alloy 360, 1/2 Hard; Plating: 10⌠" Gold or Tin over 50⌠" Nickel

Contact: Material: Beryllium Copper Alloy 172, HT; Plating: 10⌠" Gold or Tin over 50⌠" Nickel, Insertion force; 2.3 Oz w/0.018" round pin.

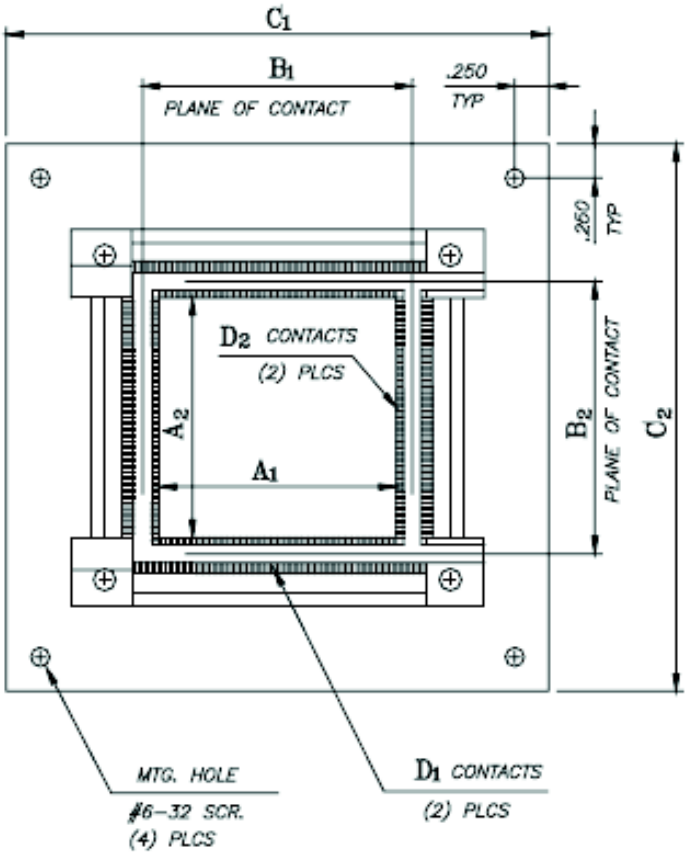
SKT-90101 SOCKET

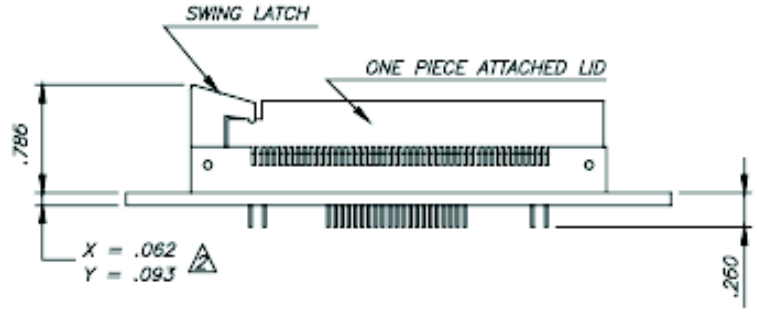
Converts staggered pins to 100 mil centers.



Description: SKT-90101 socket supports DDC ACE products and all other 78 pin SUPER HYBRID Packages. This socket is especially designed to support breadboarding efforts where 0.100" hole alignment is necessary. The socket retains the staggered pin configuration.

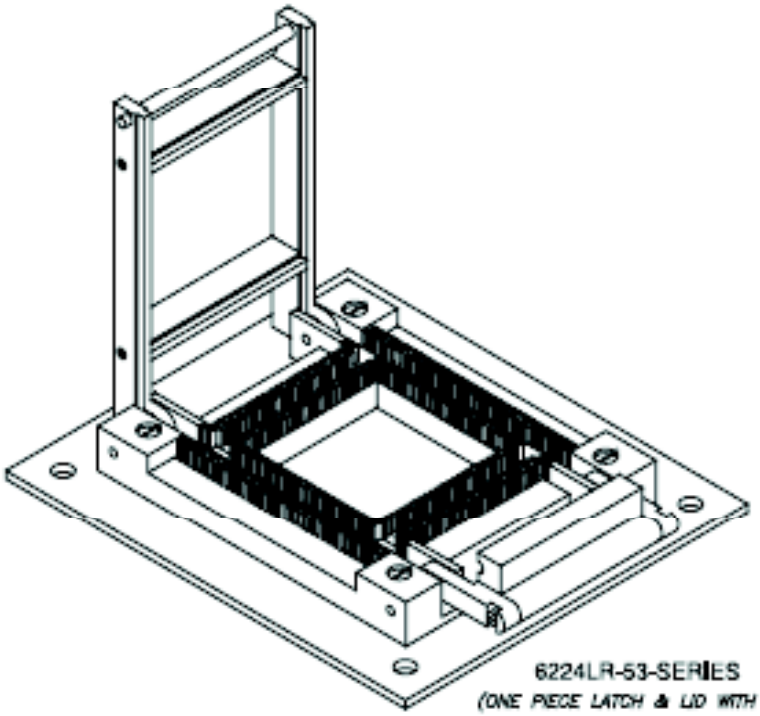
Bread Boarding Sockets
Azimuth Electronics, Inc.
2605 South El Camino Real
San Clemente, CA 92672 USA (949) 492-6481
http://www.azimuth-electronics.com



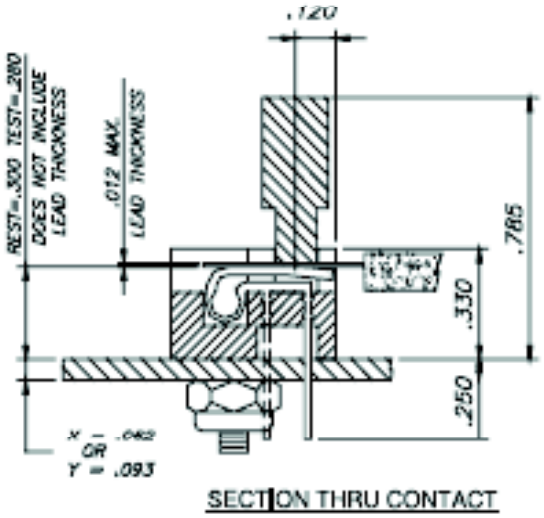


Azimuth 72-Lead CQFP Socket Test, Flat Pack, 6224-53-21X

Azimuth Electronics, Inc.
2605 South El Camino Real
San Clemente, CA 92672 USA (949) 492-6481
http://www.azimuth-electronics.com



6224LR-53-SERIES
(ONE PIECE LATCH & LID WITH ROLLER)



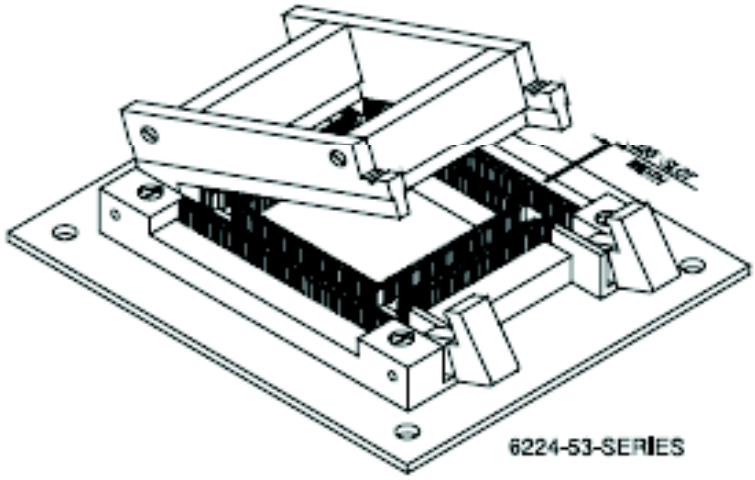
SECTION THRU CONTACT

SPECIFICATIONS:

INSULATOR: PPS (POLYPHENYLENE SULFIDE).
CONTACTS: BeCu. SPRING TEMPERED
30u GOLD OVER 30u NICKEL.
LID & LATCH: PEI (POLYETHERIMIDE)
MTG. BRAKET: GLASS EPOXY G-10.
X = .062 THICK
Y = .093 THICK
THERMAL RANGE: -65°C/+155°C.

FEATURES:

ACCOMMODATES MAX LEAD CROSS SECTION
OF .024 WIDE X .012 THICK.
FLEXIBLE DESIGN TO ACCOMMODATE DIFFERENT
SIZE Q.F.P.'s (QUAD FLAT PACKS).



6224-53-SERIES

13 APPENDIX D

13.1 DESC DRAWING CROSS-REFERENCE

Data Device Corporation
BU-65170 AND BU-61580 SERIES (ACE) DESC DRAWING PART NUMBERS

	SMD P/N	SMD SUFFIX		
		HXX [DIP]	HYX [FLAT-PACK]	HZX [J-LEAD]
-15V -12V	5962-9306501	BU-65170D1/S1	BU-65170F1/V1	BU-65170J1
	5962-9306502	BU-65170D2/S2	BU-65170F2/V2	BU-65170J2
	5962-9306503	BU-61580D1/S1	BU-61580F1/V1	BU-61580J1
	5962-9306504	BU-61580D2/S2	BU-61580F2/V2	BU-61580J2
	5962-9306505	BU-65171D1/S1	BU-65171F1/V1	BU-65171J1
	5962-9306506	BU-65171D2/S2	BU-65171F2/V2	BU-65171J2
	5962-9306507	BU-61581D1/S1	BU-61581F1/V1	BU-61581J1
	5962-9306508	BU-61581D2/S2	BU-61581F2/V2	BU-61581J2
+5V	5962-9306509	BU-65170S3	BU-65170V3	
	5962-9306510	BU-65170S6	BU-65170V6	
	5962-9306511	BU-61580S3	BU-61580V3	
	5962-9306512	BU-61580S6	BU-61580V6	
	5962-9306513	BU-65171S3	BU-65171V3	
	5962-9306514	BU-65171S6	BU-65171V6	
	5962-9306515	BU-61581S3	BU-61581V3	
	5962-9306516	BU-61581S6	BU-61581V6	
-15V -12V & XTRA RAM	5962-9306517	BU-61585S1	BU-61585V1	
	5962-9306518	BU-61585S2	BU-61585V2	
	5962-9306519	BU-61586S1	BU-61586V1	
	5962-9306520	BU-61586S2	BU-61586V2	
+5V & XTRA RAM	5962-9306521	BU-61585S3	BU-61585V3	
	5962-9306522	BU-61585S6	BU-61585V6	
	5962-9306523	BU-61586S3	BU-61586V3	
	5962-9306524	BU-61586S6	BU-61586V6	

14 APPENDIX E:

14.1 RT VALIDATION TEST REPORT

BU-61580 ACE SERIES
MIL-STD-1553
RT VALIDATION
TEST REPORT

105 Wilbur Place
Bohemia, N.Y. 11716
Telephone: 800-DDC-1772, 631-567-5600
FAX: 631-567-7358, 631-563-5218

June 16, 1994

The RT Validation Test Plan was run at Data Device Corporation using DDC's BUS-65520 RT validation tester. The test was performed on a BU-61580D2-110 ACE Series BC/RT/MT 1553 terminal. The following test equipment was used:

TEST EQUIPMENT	P/N	CALIBRATION
TEKTRONIX 2465 SCOPE	T# 2939	CAL DUE 7-31-94
FLUKE 8921A TRUE RMS VOLTMETER	T# 3005	CAL DUE 5-31-94
BECKMAN RMS 3060 DMM	T# 2877	CAL DUE 10-31-94
HP 4192A LF IMPEDANCE ANALYZER	T# 2958	CAL DUE 4-30-94
HP 3325B FUNCTION GENERATOR	T# 4485	CAL DUE 4-30-94
POWER SUPPLY MODEL TP340	T# 2889	
POWER SUPPLY MODEL TP340	DDC# 990048	
BUS 68015 NOISE TESTER	S/N 015-8618	
BUS 65517II S/N 1010 RUNNING VALIDATION SOFTWARE REV 1.67		

THE FOLLOWING D.U.T. WAS USED: **BU-61580D2-110 S/N 1091**

Electrical Tests Results JAN-13-1994 16:15

TEST EQUIPMENT	P/N	CALIBRATION
ACE TEST FIXTURE		
TEKTRONIX 2465 SCOPE	T# 2939	CAL DUE 7-31-94
FLUKE 8921A TRUE RMS VOLTMETER	T# 3005	CAL DUE 5-31-94
BECKMAN RMS 3060 DMM	T# 2877	CAL DUE 10-31-94
POWER SUPPLY MODEL TP340	T# 2889	

Configuration: **TRANSFORMER COUPLED**

```
5.1.1.1     Amplitude                                                    Pass

      Vpp value [V]     - Expected: 18.0-27.0
                        - Measured: 21.8

5.1.1.2     Risetime/falltime                                            Pass

    Sync waveform     - Tr value [nsec] - Expected: 100-300
                                        - Measured: 160
                      - Tf value [nsec] - Expected: 100-300
                                        - Measured: 160
    Data bit waveform - Tr value [nsec] - Expected: 100-300
                                        - Measured: 160
                      - Tf value [nsec] - Expected: 100-300
                                        - Measured: 160

5.1.1.3     Zero crossing stability                                      Pass

    500 nsec  - Tzcp value [nsec] - Expected: 475-525
                                  - Measured: 500
              - Tzcn value [nsec] - Expected: 475-525
                                  - Measured: 500
    1000 nsec - Tzcp value [nsec] - Expected: 975-1025
                                  - Measured: 1000
              - Tzcn value [nsec] - Expected: 975-1025
                                  - Measured: 1000
    1500 nsec - Tzcp value [nsec] - Expected: 1475-1525
                                  - Measured: 1500
              - Tzcn value [nsec] - Expected: 1475-1525
                                  - Measured: 1500
    2000 nsec - Tzcp value [nsec] - Expected: 1975-2025
                                  - Measured: 2000
              - Tzcn value [nsec] - Expected: 1975-2025
                                  - Measured: 2000

5.1.1.4     Distortion, overshoot and ringing                            Pass

    Absolute Vd value [mV] - Expected: 0-900
                           - Measured: 500

5.1.1.5     Output symmetry                                              Pass

    Absolute Vr value [mV] - Data 8000H - Expected: 0-250
                                        - Measured: 30
                           - Data 7FFFH - Expected: 0-250
                                        - Measured: 40
                           - Data 0000H - Expected: 0-250
                                        - Measured: 0
                           - Data FFFFH - Expected: 0-250
```

```
                                - Measured: 30
                    - Data 5555H - Expected: 0-250
                                - Measured: 100
                    - Data AAAAH - Expected: 0-250
                                - Measured: 100

5.1.1.6     Output noise                                                Pass

    Vrms value [mV] - OFF state - Expected: 0-14.0
                                - Measured: 1
                    - ON  state - Expected: 0-14.0
                                - Measured: 2

5.1.1.7     Output isolation                                            Pass

    Absolute value [dB] - Expected  :  45
                        - Calculated: 62.7

5.1.1.8.1   Power on/off noise                                          Pass

    Absolute Peak value [mV] - Expected: 0-250
```

OFF state		On state	
peak [mV]	width [nsec]	peak [mV]	width [nsec]
60	17	82	17
60	17	82	17
60	17	82	17
60	17	82	17
60	17	82	17
60	17	82	17
60	17	82	17
60	17	82	17
60	17	82	17
60	17	82	17

```
5.1.1.8.2   Power on response                                           Pass

5.1.1.9     Terminal response time                                      Pass

    Response Time [usec] - TX command    - Expected: 4.0-12.0
                                         - Measured: 6.4
                         - RX command    - Expected: 4.0-12.0
                                         - Measured: 6.4
                         - RT_RT command - Expected: 4.0-12.0
                                         - Measured: 6.4
                         - MODE command  - Expected: 4.0-12.0
                                         - Measured: 6.4

5.1.1.10    Frequency stability

    *** VERIFIED BY DESIGN ANALYSIS (see Appendix A) ***

5.1.2.1.1   Zero crossing distortion                                    Pass

    Response within ±150 [nsec]        - Expected: CS
                                       - Measured: CS
    Positive - value for first NR [ns] - Expected: >150
                                       - Measured: 189
    Negative - value for first NR [ns] - Expected: >150
                                       - Measured: 227

5.1.2.1.2   Amplitude variations                                       Pass

    Vpp at which response <> CS [V]   - Expected: <0.86
                                      - Measured: 0.63
    Vpp at which NR first occurred [V] - Expected:  0.2
                                      - Measured: 0.63
```

```
    Response for Vpp = 0.20 V         - Expected: NR
                                      - Measured: NR

5.1.2.1.3.1 Trapezoidal                                                  Pass

    Response - Expected: CS for each message
             - Measured: CS for each message

5.1.2.1.3.2 Sinusoidal                                                   Pass

    Response - Expected: CS for each message
             - Measured: CS for each message
```

Electrical Tests Results JAN-14-1994 9:19

TEST EQUIPMENT	P/N	CALIBRATION
ACE TEST FIXTURE		
TEKTRONIX 2465 SCOPE	T# 2939	CAL DUE 7-31-94
BECKMAN RMS 3060 DMM	T# 2877	CAL DUE 10-31-94
HP 3325B FUNCTION GENERATOR	T# 4485	CAL DUE 4-30-94
POWER SUPPLY MODEL TP340	T# 2889	
POWER SUPPLY MODEL TP340	DDC# 990048	

Configuration: **TRANSFORMER COUPLED**

5.1.2.2 Common mode rejection Pass

Response while applied +10.0 VDC -Expected:CS for each message
-Measured:CS for each message
Response while applied -10.0 VDC -Expected:CS for each message
-Measured:CS for each message
Response while applied ±10 Vp sinu -Expected:CS for each message
-Measured:CS for each message

Electrical Tests Results JAN-14-1994 9:46

TEST EQUIPMENT	P/N	CALIBRATION
ACE FIXTURE		
HP 4192A LF IMPEDANCE ANALYZER	T# 2958	CAL DUE 4-30-94
POWER SUPPLY MODEL TP340	T# 2889	

Configuration: **TRANSFORMER COUPLED**

```
5.1.2.3     Input impedance                                          Pass

    Zin at 75.0  KHz [ohms] - Expected:  1000
                - OFF state - Measured: 4173
                - ON  state - Measured: 4149
    Zin at 100.0 KHz [ohms] - Expected:  1000
                - OFF state - Measured: 5018
                - ON  state - Measured: 5012
    Zin at 250.0 KHz [ohms] - Expected:  1000
                - OFF state - Measured: 5743
                - ON  state - Measured: 6106
    Zin at 500.0 KHz [ohms] - Expected:  1000
                - OFF state - Measured: 4057
                - ON  state - Measured: 4437
    Zin at 1.0   MHz [ohms] - Expected:  1000
                - OFF state - Measured: 2266
                - ON  state - Measured: 2454
```

Protocol Tests Result DEC-18-1993 9:48

TEST EQUIPMENT	P/N	CALIBRATION
BUS 65529 S/N:1219 w/ACE ADAPTOR		
TEKTRONIX 2465 SCOPE	T# 2939	CAL DUE 7-31-94

Bus A	Bus B	Test	
Pass	Pass	5.2.1.1.1	RT response to command words
Pass	Pass	5.2.1.1.2	RT-RT response to command words
Pass	Pass	5.2.1.2.1	Minimum time
Pass	Pass	5.2.1.2.2	Transmission rate
Pass	Pass	5.2.1.3.1.1	Transmit command word
Pass	Pass	5.2.1.3.1.2	Receive command word
Pass	Pass	5.2.1.3.1.3	Receive data words
Pass	Pass	5.2.1.3.2.1	Transmit command word
Pass	Pass	5.2.1.3.2.2	Receive command word
Pass	Pass	5.2.1.3.2.3	Receive data words
Pass	Pass	5.2.1.3.3.1	Transmit command word
Pass	Pass	5.2.1.3.3.2	Receive command word
Pass	Pass	5.2.1.3.3.3	Receive data words
Pass	Pass	5.2.1.3.4.1	Transmit command word
Pass	Pass	5.2.1.3.4.2	Receive command word
Pass	Pass	5.2.1.3.4.3	Data word
Pass	Pass	5.2.1.3.5.1	Transmit command
Pass	Pass	5.2.1.3.5.2	Receive command
Pass	Pass	5.2.1.3.5.3	Mode command word count error
Pass	Pass	5.2.1.3.5.4	RT to RT word count error
Pass	Pass	5.2.1.3.6	Contiguous data
Pass	Pass	5.2.1.3.7	Terminal fail-safe
Pass	Pass	5.2.1.4	Superseding commands
Pass	Pass	5.2.1.4.1	RT to RT superseding command
Pass	Pass	5.2.1.5.1	Transmit status
Pass	Pass	5.2.1.5.2	Transmitter shutdown and override
Pass	Pass	5.2.1.5.3	Reset remote terminal
Pass	Pass	5.2.1.6	Data wrap-around
Pass	Pass	5.2.1.7.1	RT to RT timeout
Pass	Pass	5.2.1.7.2	RT to RT message format errors
Pass	Pass	5.2.1.7.3	Transmitting RT errors
Pass	Pass	5.2.1.8	Bus switching
Pass	Pass	5.2.1.9	Unique address
Pass	Pass	5.2.2.1.1	Dynamic bus control
Pass	Pass	5.2.2.1.2.1	Synchronize without data word
Pass	Pass	5.2.2.1.2.2	Synchronize with data word
Pass	Pass	5.2.2.1.3	Initiate self-test
Pass	Pass	5.2.2.1.4	Transmit BIT word
Pass	Pass	5.2.2.1.6	Terminal flag bit inhibit and override
Pass	Pass	5.2.2.1.7	Transmit vector word
Pass	Pass	5.2.2.1.8	Transmit last command
Pass	Pass	5.2.2.2.1	Service request
Pass	Pass	5.2.2.2.2	Broadcast command received
Pass	Pass	5.2.2.2.3	Busy
Pass	Pass	5.2.2.2.4	Subsystem flag
Pass	Pass	5.2.2.2.5	Terminal flag

Pass	Pass	5.2.2.3	Illegal command
Pass	Pass	5.2.2.4.1	Bcst synchronize without data word
Pass	Pass	5.2.2.4.2	Bcst synchronize with data word
Pass	Pass	5.2.2.4.3	Bcst initiate self-test
Pass	Pass	5.2.2.4.4	Bcst transmitter shutdown and override
Pass	Pass	5.2.2.4.6	Bcst terminal flag bit inhibit and override
Pass	Pass	5.2.2.4.7	Bcst reset remote terminal
Pass	Pass	5.2.2.4.8	Bcst dynamic bus control
Pass	Pass	5.2.2.5.1.1	Command word error
Pass	Pass	5.2.2.5.1.2	Data word error
Pass	Pass	5.2.2.5.2	Message length, BC to RT broadcast

Noise Rejection Test results JAN-12-1994 16:22

TEST EQUIPMENT	P/N	CALIBRATION
BUS 65529 S/N:1738 w/ACE ADAPTOR		
TEKTRONIX 2465 SCOPE	T# 2939	CAL DUE 7-31-94
FLUKE 8921A TRUE RMS VOLTMETER	T# 3005	CAL DUE 5-31-94
BUS 68015 NOISE TESTER	S/N 015-8618	

NOISE LEVEL = 145 mv CHANNEL A

Configuration: **TRANSFORMER COUPLED**

```
5.3         Noise rejection test                                        Pass

    Result - Expected: See table III - criteria for noise rejection
                       tests
           - Measured: 44,000,055 words - 0 errors
```

Noise Rejection Test results JAN-12-1994 16:22

TEST EQUIPMENT	P/N	CALIBRATION
BUS 65529 S/N:1738 w/ACE ADAPTOR		
TEKTRONIX 2465 SCOPE	T# 2939	CAL DUE 7-31-94
FLUKE 8921A TRUE RMS VOLTMETER	T# 3005	CAL DUE 5-31-94
BUS 68015 NOISE TESTER	S/N 015-8618	

NOISE LEVEL = 145 mv CHANNEL B

Configuration: **TRANSFORMER COUPLED**

```
5.3         Noise rejection test                                        Pass

    Result - Expected: See table III - criteria for noise rejection tests
           - Measured: 44,000,187 words - 0 errors
```

Analysis for 5.1.1.10 Frequency stability test.

MIL-STD-1553 paragraph 4.3.3.3 Transmission bit rate requires that "the transmission bit rate on the bus shall be 1.0 megabit per second with a combined accuracy and long-term stability of ±0.1 percent". The transmission bit rate of the ACE is derived directly from the clock input signal. The ACE requires a 16 MHz clock input, which is divided down to form an internal 2 MHz encoder clock. Providing a 16 MHz clock input with a combined accuracy and long-term frequency stability of ±0.1 percent or better will guarantee that the combined accuracy and long-term frequency stability of the 2 MHz encoder clock, and in turn the transmission bit rate will be ±0.1 percent or better.

15 APPENDIX F

15.1 DIFFERENCES BETWEEN 61580 SERIES AND 61582 SERIES

6-Feb-1995
Revised 1-May-08

1) Configuration Register 3 Bit 15 (Enhanced Mode Enable) has no effect. Enhanced is always enabled. This bit may be set or cleared without affecting any operation of the device.

2) Configuration Register 5 Bit 14 Single Ended Select has been modified to be a Read Write Bit. Single Ended Select, for the BU-61580, is a read only bit reflecting the state of a wire bond option to enable the single ended receiver input. The BU-61582 uses this bit for the purpose of selecting single ended operation. Writing a logic 0 (default) to this bit will configure the 61582 for standard Double Ended receivers. Writing a logic 1 to this bit will configure the 61582 for singled ended receivers (compatible with fiber optic receivers).

3) Internal RAM is "off-chip" for the BU-61582.

4) CPU Transfers
   a) SELECT_L is now latched on the second rising clock edge after STROBED_L is asserted low. Asserting SELECT_L low after the second rising clock edge after STROBED_L is asserted low will NOT begin an ACE transfer. This allows for address pipelining where SELECT_L may change states before STROBED_L is released from the previous transfer.
   b) 8 Bit transfer mode
      i) All 8 bit transfers are performed using D15 to D8 data bits (Muxed internally).
      ii) IOENA_L signal has been delayed one clock cycle in 8 bit mode. Hold time on MSB/LSB, R/W, and MEM/REG delayed one clock cycle. Transfer cycle is now 5 clocks.
      iii) For SP'ACE, memory and registers must **not** be accessed when the SP'ACE is processing a 1553 message when used in 8-bit Buffered Non-Zero Wait Mode **(Please see Appendix G for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)**
   c) Option for 8 or 16 Bit Internal RAM. When the 8 bit option is enabled the ACE will still operate internally as a 16 bit device and will perform two byte transfers to the internal RAM. This extends the internal RAM transfer by 4 clock cycles.

      i) Register transfer timing remains unchanged (i.e., 3 clock cycles from IOEN_L to READYD_L).
      ii) Memory write transfers remain unchanged (i.e., 3 clock cycles from IOEN_L to READYD_L) with one exception being that the next transfer may be extended if previous write transfer has not completed. CPU transfer will end normally but internal transfer will continue and may extend next transfer. READYD_L will handle extending transfer.
      iii) Memory read transfers extended by 4 clock cycles.
      iv) In Zero Wait mode the READYD_L signal is always extended by 4 clock cycles.
      v) When the 8 bit internal RAM option is enabled BA15 is used as MSB/LSB on the buffered RAM address bus.
      vi) The BR_OE* output signal will pulse twice on an internal memory transfer (one for each byte transfer). BR_OE* will pulse low only once for an external RAM transfer.

vii) The BR_WR* output signal will pulse twice on all internal memory write transfers. No pulse will occur during external write transfers.

d) During read operations from reserved register address locations 18 to 1F (hex) (registers 24 thru 31) the data bus will be tri-stated. The BU-61580 would drive the data bus with the data value from the previous CPU transfer.

e) Transparent mode DMA timeouts have been extended.
16 MHz, 16 bit buffered RAM = 5.0 µsec (61580 = 4 µsec)
16 MHz, 8 bit buffered RAM = 4.0 µsec " "
12 MHz, 16 bit buffered RAM = 4.5 µsec (61580 = 3.5 µsec)
12 MHz, 8 bit buffered RAM = 3.5 µsec " "

5) Internal No Data signal delayed 1 µsec
   a) RT Response time increased from 5.5 µsec to 6.5 µsec. Note the 61582 will extend the response time to 10 µsec if Data Transfer Grant is delayed (Transparent/DMA mode only). BU-61580 response time is fixed at 5.5 µsec.
   b) BC minimum Intermessage gap time extended from 9.5 µsec to 10.5 µsec nominal.

6) The following chip signals have been removed
CLK_SEL*, ENHANCED_MODE_ENA*, INT_RAM_ENA*, SNGL_END*, BRO_ENA, ILLENA, LATCH_BRO*, ME*, RT_FAIL*, HS_FAIL*, TX_DTA_STR*, RX_DTA_STR*, RT_FLAG.

7) The following chip signals have been added to the BU-65621P/F0:
MC_RST* (mode code reset pulse asserted following a mode reset command).
RM8_SEL* (8 bit selection for internal buffered RAM)
REG_WR* (Register Write pulse asserted during a write access to registers 24 thru 31)
REG_OE* (Register Read pulse asserted during a read access from registers 24 thru 31)

8) DC Parametric changes
   a) All inputs are now CMOS logic levels (BU-61580 has TTL input logic levels).
   b) All outputs are now 9 mA drive (BU-61580 had 3.2 mA drive on outputs and 6.4 mA drive on bi-directionals).
   c) Pull-up resistors are present only on bi-directionals, RT address inputs, transceiver RX inputs, and the IP_TST* input (BU-61580 has pull-ups on all inputs and bi-directionals).

15.2 DIFFERENCES BETWEEN 61580 SERIES and 63825/925 SERIES

1-May-08

1) Configuration Register 3 Bit 15 (Enhanced Mode Enable) has no effect. Enhanced is always enabled. This bit may be set or cleared without affecting any operation of the device.

2) Configuration Register 5 Bit 14 Single Ended Select has been modified to be a Read Write bit. Single Ended Select, for the BU-61580, is a read only bit reflecting the state of a wire bond option to enable the single ended receiver input. The BU-63825/925 uses this bit for the purpose of selecting single ended operation. Writing a logic 0 (default) to this bit will configure the 63825/925 for standard Double Ended receivers. Writing a logic 1 to this bit will configure the 63825/925 for Single Ended receivers (compatible with fiber optic receivers).

3) Internal RAM is separate “off-chip” for the BU-63825/925.

4) CPU Transfers.

   a) SELECT* is now latched on the second rising clock edge after STRBD* is asserted low Asserting SELECT* low after the second rising clock edge after STRBD* is asserted low will NOT begin a SP’ACE II transfer. This allows for address pipelining where SELECT* may change states before STRBD* is released from the previous transfer.

   b) 8-Bit transfer mode

      i) All 8 bit transfers are performed using D15 to D8 data bits (Muxed internally).
      ii) IOEN* signal has been delayed one clock cycle in 8-bit mode. Hold time on MSB/LSB, RD/WR*, and MEM/REG* is delayed one clock cycle. Transfer cycle is now 5 clocks.
      iii) MEM/REG* must be asserted to ‘0’, and a register address of 0x0000, (rather than the actual memory or register address), must be used in 8-bit Buffered Non-Zero Wait Mode during non-triggering register or memory transfers. **(Please see Appendix G for Product Advisory regarding SP’ACE and SP’ACE II operating in 8-bit Buffered Non-Zero Wait Mode.)**

   c) During read operations from reserved register address locations 18 to 1F (hex) (registers 24 through 31) the data bus will be tri-stated. The BU-63825/925 would drive the data bus with the data value from the previous CPU transfer.

   d) Transparent mode DMA timeouts have been extended.

      16MHz, 16 bit buffered RAM = 5.0 µsec (61580 = 4 µsec)
      16MHz, 8 bit buffered RAM = 4.0 µsec (61580 = 4 µsec)

12MHz, 16 bit buffered RAM = 4.5 µsec (61580 = 3.5 µsec)
12MHz, 8 bit buffered RAM = 3.5 µsec (61580 = 3.5 µsec)

5) Internal No Data signal delayed 1 µsec

   a) RT Response time increased from 5.5 µsec. Note the BU-63825/925 will extend the response time to 10 µsec if Data Transfer Grant is delayed (Transparent/DMA mode only). BU-61580 response time is fixed at 5.5 µsec.

   b) BC minimum Intermessage gap time extended from 9.5 µsec to 10.5 µsec nominal.

6) DC Parametric changes

   a) Inputs MSTCLR*, CLOCK IN and STRBD* are now at CMOS logic levels (Remaining signals are TTL). (BU-61580 has TTL input logic levels.)

   b) All outputs are now 8 mA drive (BU-61580 had 3.2 mA drive on outputs and 6.4 mA drive on bi-directionals).

   c) Pull-up resistors are present only on bi-directionals, RT address inputs, transceiver RX inputs (BU-61580 has pull-ups on all inputs and bi-directionals).

16 APPENDIX G

16.1 Product Advisory SP'ACE and SP'ACE II



Product Advisory

SP'ACE and SP'ACE II
8-bit Buffered Non-Zero Wait Interface Mode Data Corruption

Date: February 25, 2008

Attn:

Dear:

Introduction:
This is a product advisory for DDC's SP'ACE and SP'ACE II products only when used in the 8-bit buffered non-zero wait mode. **This advisory does not apply to these products when they are used in 16-bit buffered non-zero wait mode, in 16-bit buffered zero-wait mode, in 8-bit buffered zero wait, or in transparent mode.** Our records indicate that you have purchased one or more of these parts in the past.

Affected Product Part Numbers:
BU-63825xx-xxxx, BU-63925xx-xxxx, BU-61582xx-xxxx, BU-61583xx-xxxx, BU-65621F0

Detailed Description:
A condition has been identified which can cause a memory location within the SP'ACE or SP'ACE II's shared RAM to become corrupted. The condition only occurs while the device is configured for the 8-bit buffered non-zero wait interface mode (i.e. the TRANSPARENT/BUFFERED* signal is logic "0", and the 16/8*_BIT signal is logic "0", and the ZERO_WAIT* signal is logic "1"). If the device is configured for any mode other than 8-bit buffer non-zero wait then this notice does not apply.

The error that has been observed is that if the host performs a "non-triggering" read or write data transfer while the 1553 protocol engine is performing a read or write access to the SP'ACE's shared memory, it is possible for the value of the Least Significant (LS) byte to be read or written twice, therefore causing a data corruption error to the value of the Most Significant (MS) byte. That is, when the host CPU performs a read access from an affected memory location, the value of the LS byte from the corrupted 1553 protocol transfer will be read as the value of the MS byte.

Workaround:
DDC is able to recommend multiple work-around solutions to the problem described above. These include:

(1) Operate the BU-61582 SP'ACE and/or BU-63825 SP'ACE II in the 8-bit zero wait host processor interface configuration.

(2) For the case of the BU-63825 SP'ACE II, operate in the 8-bit non-zero wait mode, with modified software to perform "non-triggering" transfers to the SP'ACE II shared RAM to a *register* address (that is, with MEM/REG* asserted to '0') to register address 0x0000, rather than to the target memory address.

(3) Operate the BU-61582 SP'ACE or BU-63825 SP'ACE II in 16-bit non-zero wait mode.

(4) Modifications to software, to avoid accessing the SP'ACE or SP'ACE II during times that the SP'ACE or SP'ACE II is processing a 1553 message.

For Application support or additional technical information please contact Adolfo Biagioni at 1-631-567-5600 ext 7402 or email biagioni@ddc-web.com.

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