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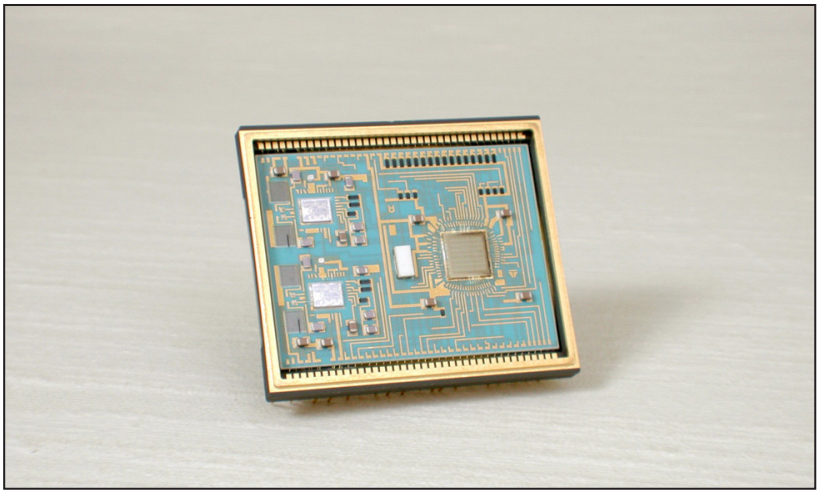
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BU-63705

MIL-STD-1553 DUAL REDUNDANT REMOTE TERMINAL HYBRID SPACE-RT-II



DESCRIPTION

The BU-63705, "SPACE-RT-II," is a Hi-Rel radiation tolerant complete dual redundant MIL-STD-1553 Remote Terminal Unit (RTU). The SPACE-RT-II is a drop in Replacement for the BU-65142. The device is based upon two DDC custom ICs, which includes two monolithic bi-polar low power transceivers and one RICMOS™ protocol chip containing data buffers and timing control logic. It supports all 13 mode codes for dual redundant operation, any combination of which can be illegalized.

Parallel data transfers are accomplished with a DMA type handshaking, compatible with most CPU types. Data transfers to/from memory are simplified by the latched command word and word count outputs.

Error detection and recovery are enhanced by BU-63705 special features. A 14-bit built-in-test word register stores RTU information, and sends it to the Bus Controller in response to the Mode Command Transmit Bit Word. The BU-63705 performs continuous on-line wrap-around self-test, and provides four error flags to the host CPU. Inputs are provided for host CPU control of 6 bits of the RTU Status Word.

Its integrated hermetic package, -55°C to +125°C operating temperature range, and complete RTU operation make the BU-63705 ideal for MIL-STD-1553 applications requiring hardware or microprocessor subsystems.

FEATURES

- Drop in Replacement for BU-65142
- Radiation Tolerant & Radiation Hardened versions for Space Based Applications
- Complete Integrated Remote Terminal Including:
  - Low-Power Transceivers
  - Complete RT Protocol
- Multiple Ordering Options; +5V (Only), +5V/-15V, and +5V/-12V
- Direct Interface to Systems with No Processor
- High Reliability Screening

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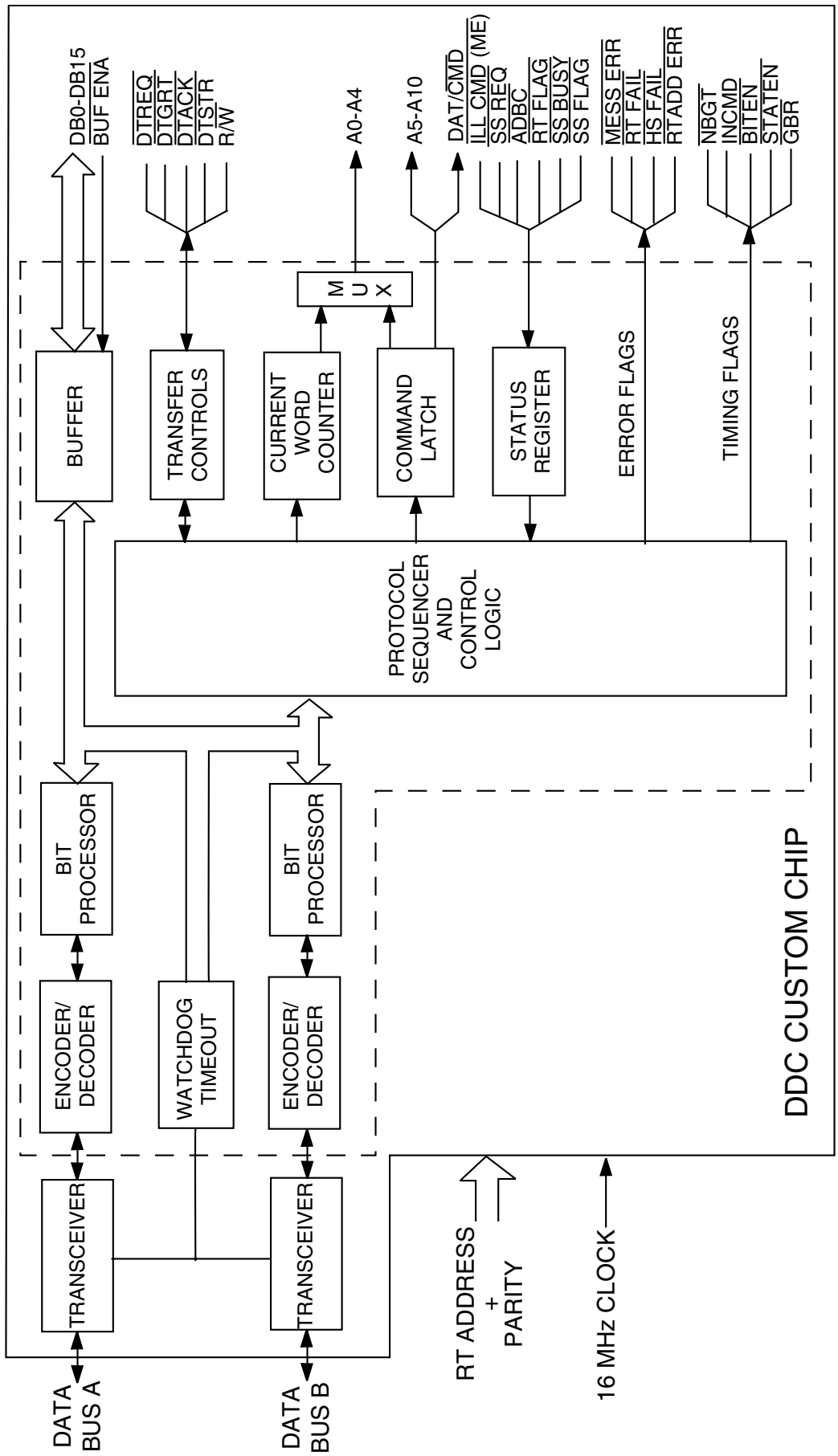


FIGURE 1. BU-63705 SERIES BLOCK DIAGRAM

TABLE 1. SPACE-RT-II SERIES SPEC'S

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATING				
Supply Voltage				
Logic +5V	-0.5		6.5	V
Transceiver +5V	-0.5		7.0	V
-15V (BU-63705X1)	-18.0		0.3	V
-12V (BU-63705X2)	-18.0		0.3	V
Receiver Differential Input Voltage			40.0	Vp-p
Logic				
Voltage Input Range for +5V	-0.5		Vcc+0.5	V
RECEIVER				
Differential Input Impedance (BU-63705 X1/X2) (DC to 1 MHz)	4.0			kΩ
Differential Input Resistance (BU-63705X3)	2.5			KΩ
Input Threshold Level				
Direct Coupled (BU-63705 X1/X2)	0.28		1.20	Vp-p
Transformer Coupled, Measured on Stub (BU-63705X3)	0.200		0.860	Vp-p
CMRR (DC to 2 MHz)	40			dB
CMV (DC to 2 MHz)	±10			V
TRANSMITTER				
Differential Output Voltage				
■ Direct Coupled Across 35 Ω, Measured on Bus	6	7	9	Vp-p
■ Transformer Coupled Across 70Ω, Measured on Stub	18	20	27	Vp-p
Output Noise, Differential (Direct Coupled)			10	mVp-p, diff
Output Offset Voltage, (Transformer Coupled Across 70 ohms)	-250		+250	mVp-p, diff
Rise/Fall Time	100	150	300	nsec
LOGIC				
V_{IH} (V_{CC} =5.5V)	2			V
V_{IL} (V_{CC} = 4.5V)			0.8	V
I_{IH} (V_{CC} = 5.5V, V_{IN} = 2.7V)				
■ 16MHz_IN	-10		+10	µA
■ All other inputs	-400		-20	µA
I_{IL} (V_{CC} = 5.5V, V_{IN} = 0.0V)				
■ 16MHz_IN	-10		+10	µA
■ All other inputs	-600		-60	µA
V_{OH} (V_{CC} = 4.5V, I_{OH} = max)	4			V
V_{OL} (V_{CC} = 4.5V, I_{OL} = max)			0.5	V
I_{OH} (V_{CC} = 4.5V) (Note 1)			-8	mA
I_{OL} (V_{CC} = 4.5V)			8	mA
C_{IN} (f = 1MHz)		20	50	pF
C_{IO} (f = 1MHz)		30	50	pF
POWER SUPPLY REQUIREMENTS				
+5V Logic Power	4.5	5.0	5.5	V
Logic Current Drain			115	mA
BU-63705X1				
+5V (Ch. A, Ch. B)	4.5	5.0	5.5	V
-15V (VA, VB)	-15.75	-15.0	-14.25	V
BU-63705X2				
+5V (Ch. A, Ch. B)	4.5	5.0	5.5	V
-12V (VA, VB)	-12.6	-12.0	-11.4	V
BU-63705X3 (+5V Only)				
+5V (Ch. A, Ch. B)	4.75	5.0	5.25	V

TABLE 1. SPACE-RT-II SERIES SPEC'S (CONT)

PARAMETER	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS (CONTINUED)				
Current Drain				
■ BU-63705X1				
-15V (Ch.A & Ch. B)				
• Idle			60	mA
• 25% Transmitter Duty Cycle			108	mA
• 50% Transmitter Duty Cycle			175	mA
• 100% Transmitter Duty Cycle			270	mA
■ BU-63705X2				
-12V (Ch.A & Ch. B)				
• Idle			60	mA
• 25% Transmitter Duty Cycle			120	mA
• 50% Transmitter Duty Cycle			185	mA
• 100% Transmitter Duty Cycle			305	mA
■ BU-63705X3				
+5V (Ch.A & Ch. B)				
• Idle			125	mA
• 25% Transmitter Duty Cycle			230	mA
• 50% Transmitter Duty Cycle			335	mA
• 100% Transmitter Duty Cycle			545	mA
POWER DISSIPATION (NOTE 2)				
Total Hybrid				
■ BU-63705X1				
• Idle			1.475	W
• 25% Transmitter Duty Cycle			1.856	W
• 50% Transmitter Duty Cycle			2.238	W
• 100% Transmitter Duty Cycle			3.000	W
■ BU-63705X2				
• Idle			1.295	W
• 25% Transmitter Duty Cycle			1.680	W
• 50% Transmitter Duty Cycle			2.065	W
• 100% Transmitter Duty Cycle			2.895	W
■ BU-63705X3				
• Idle			0.687	W
• 25% Transmitter Duty Cycle			0.92	W
• 50% Transmitter Duty Cycle			1.15	W
• 100% Transmitter Duty Cycle			1.60	W
Hottest Die				
■ BU-63705X1				
• Idle			0.680	W
• 25% Transmitter Duty Cycle			1.010	W
• 50% Transmitter Duty Cycle			1.350	W
• 100% Transmitter Duty Cycle			2.030	W
■ BU-63705X2				
• Idle			0.290	W
• 25% Transmitter Duty Cycle			0.540	W
• 50% Transmitter Duty Cycle			0.790	W
• 100% Transmitter Duty Cycle			1.290	W
■ BU-63705X3				
• Idle			0.280	W
• 25% Transmitter Duty Cycle			0.510	W
• 50% Transmitter Duty Cycle			0.750	W
• 100% Transmitter Duty Cycle			1.220	W

TABLE 1. SPACE-RT-II SERIES SPEC'S (CONT)

PARAMETER	MIN	TYP	MAX	UNITS
CLOCK INPUT				
Frequency				
• Nominal Value		16		MHz
• Long Term Tolerance				
1553A Compliance	-0.01		0.01	%
1553B Compliance	-0.10		0.10	%
• Short Term Tolerance, ONE sec				
1553A Compliance	-0.001		0.001	%
1553B Compliance	-0.01		0.01	%
• Duty Cycle				
16 MHz	40		60	%
1553 MESSAGE TIMING				
• RT -to - RT Response Timeout	17.5	18.5	19.5	µs
• RT Response Time	8		10	µs
• Transmitter Watchdog Timeout		768		µs
THERMAL				
• Thermal Resistance, Junction-to -Case, Hottest Die (ThetaJC)			7.55	°C/W
• Operating Junction Temperature	-55		150	°C
• Storage Temperature	-65		150	°C
• Lead Temperature (soldering 10 sec.)			300	°C
PHYSICAL CHARACTERISTICS				
Size				
78-pin Ceramic QIP (BU-63705D)	1.80 x 2.10 x 0.21 (45.7 x 53.3 x 5.3)			in (mm)
78-pin Ceramic Flat Pack (BU-63705F)	1.80 x 2.10 x 0.21 (45.7 x 53.3 x 5.3)			in (mm)
Weight	1.7 (48.2)			oz (g)

Notes (for TABLE 1):

1. Minus sign indicates the direction of current flow.
2. Power dissipation specifications assume a transformer coupled configuration, with external dissipation (while transmitting) of 0.14 watts for the active isolation transformer, 0.08 watts for the active coupling transformer, 0.45 watts for each of the two bus isolation resistors, and 0.15 watts for each of the two bus termination resistors.

TABLE 2. BU-63705 SERIES RADIATION SPECIFICATIONS*

PART NUMBER	TOTAL DOSE	SINGLE EVENT UPSET	SINGLE EVENT LATCHUP
BU-63705 X1/X2	300K Rad*	1.0×10^{-8} errors/device-day, (LET Threshold of 63 MeV-cm^2/mg)	Immune
BU-63705 X3	100K Rad	1.0×10^{-8} errors/device-day, (LET Threshold of 63 MeV-cm^2/mg)	Immune

* Consult factory for 1 X 10^6 Rad Version

*Note: Radiation parameters specified on this data sheet are derived from initial qualification testing by *DDC* and published data from *ASIC* manufacturers. These devices have not been evaluated for compliance to the *RHA* requirements stipulated in MIL-PRF-38534, *Appendix G*.

HIGH-REL SCREENING

DDC is committed to the design and manufacture of hybrids and transformers with enhanced processing and screening for spaceborne applications and other systems requiring the highest levels of reliability. These platforms include launch vehicles, satellites and the International Space Station.

DDC has tailored its design methodologies to optimize the fabrication of space level hybrids. The intent of the design guidelines is to minimize the number of die and wirebonds, minimize the number of substrate layers, and maximize the space between components. DDC's space grade products combine analog bipolar and rad hard CMOS technology to provide various levels of radiation tolerance.

The BU-63705 is packaged in a 78-pin ceramic package. In contrast to Kovar (metal) packages, the use of ceramic eliminates the hermeticity problems associated with the glass beads used in the metal packages. In addition, ceramic packages provide more rigid leads, better thermal properties, easier wirebonding, and lower weight.

The production of the space level hybrids can entail enhanced screening steps beyond DDC's standard flow. This includes Condition A visual inspection, SEM analysis, and element evaluation for all integrated circuit die. For the hybrids, available screening includes Particle Impact Noise Detection (PIND), 320-hour burn-in, 100% non-destructive wirebond pull (standard on this device), X-ray analysis, as well as Destructive Physical Analysis (DPA) testing, extended temperature cycling for QCI testing, and a moisture content limit of 5000 PPM. TABLE 3 summarizes the procurement screening, element evaluation, and hybrid screening used in the production of the BU-63705.

RADIATION TOLERANCE

The hybrids are inherently immune to Latchup. The transceiver is bipolar/BiCMOS, the digital logic is implemented in a Honeywell RICMOS™ IV SOI Gate Array (HX2000 Series).

TABLE 3. HIGH RELIABILITY SCREENING OPTIONS	
ELEMENT EVALUATION	**METHOD**
Visual Inspection: Integrated Circuits Transistors & Diodes Passive Components	 MIL-STD-883, Method 2010 Condition A MIL-STD-750, Method 2072 and 2073 MIL-STD-883, Method 2032 Class S
SEM Analysis for Integrated Circuits	MIL-STD-883, Method 2018
Element Evaluation: Visual, Electrical, Wire Bondability, 24-Hour Stabilization Bake,10 Temperature Cycles 3000 g's constant acceleration 240-Hour Powered Burn-In and 1000-Hour Life Test (Burn-In and 1000-Hour Life Test Are Only Required For Active Components.)	MIL-PRF-38534
ASSEMBLY & TEST	
Particle Impact Noise Detection (PIND)	MIL-STD-883, Method 2020 Condition A
320-Hour Burn-In (available on this device)	MIL-STD-883, Method 1015
100% Non-Destructive Wirebond Pull (available on this device)	MIL-STD-883, Method 2023
Radiographic (X-Ray) Analysis	MIL-STD-883, Method 2012
QCI TESTING	
Extended Temperature Cycling: 20 Cycles Including Radiographic (X-Ray) Testing	MIL-STD-883, Method 1010 Condition C and MIL-STD-883, Method 2012
Moisture Content Limit of 5000 PPM	MIL-STD-883, Method 1018

INTRODUCTION

The BU-63705 is a complete dual redundant Remote Terminal Unit (RTU). It is fully compliant with MIL-STD-1553B and supports all message formats. As shown in FIGURE 1, it includes 2 transceivers and a custom chip containing 2 encoders / decoders, 2 bit processors, an RTU protocol sequencer and control logic, output latches, and buffers. With the addition of 2 data bus transformers, the BU-63705 is ready for connection to a MIL-STD-1553 data bus.

Data is transferred to and from the subsystem host CPU over a 16-bit parallel highway, which is isolated by a set of bi-directional buffers. All transfers are made with a DMA type handshake sequence of request, grant and acknowledge. Read/write and data strobes are provided to simplify interfacing to external RAM. Also simplifying the RAM interface is the availability of a latched command word and an auto-incrementing word counter. These signals may be used as an address to map the data directly to and from RAM.

The BU-63705 allows the subsystem host CPU to control 6 of the bits in the RTU status word. Of particular interest is the Illegal Command input which may be used to set the message error bit and illegalize any command word. The BU-63705 provides four error flags to the subsystem host CPU for evaluating its condition. In addition a continuous on-line self-test is performed by the BU-63705 on every transmission. The last Transmitted Word of every message is wrapped around into the decoder and compared with the Actual Word. Any discrepancy is flagged as an error.

TIMING

Interfacing the subsystem host CPU to the BU-63705 is simple and compatible with most microprocessors. FIGURES 4 and 5 illustrate typical MIL-STD-1553 messages for Transmit data and Receive data. FIGURES 6 and 7 illustrate RT to RT transfers. In each case $\overline{\text{NBGT}}$ identifies the start of the message, and INCMD identifies that a command is being processed. The handshake sequence $\overline{\text{DTREQ}}$, DTGRT, and DTACK is used to transfer each word over the parallel data highway. $\overline{\text{DTSTR}}$ and RD/$\overline{\text{WR}}$ are used to control transfers to RAM memory. $\overline{\text{GBR}}$ identifies a "good block received", when a received message has passed all validation checks and has the correct word count. $\overline{\text{BUFENA}}$ (Buffer Enable) must be applied to enable the internal tri-state buffers.

ERROR FLAGS

Four error flags are output to the subsystem to provide information on the condition of the BU-63705.

1. The $\overline{\text{ME}}$ (Message Error) line goes LOW if any of the following error conditions exist:
   - format error
   - word count error
   - invalid word
   - sync error
   - RT to RT address error
   - T/$\overline{\text{R}}$ bit error

2. The $\overline{\text{RTFAIL}}$ (Remote Terminal Failure) line goes LOW whenever the results of a continuous wraparound self-test shows a discrepancy, or a transmitter watchdog timeout has occurred.

3. The $\overline{\text{HSFAIL}}$ (Handshake Failure) line goes LOW whenever the system does not issue a $\overline{\text{DTGRT}}$ in response to a $\overline{\text{DTREQ}}$ before timing-out.

4. The $\overline{\text{RTADR ERR}}$ (RT Address Error) line goes LOW whenever the sum of the 5 address lines and parity lines show a parity error (the terminal will not respond to commands while this error condition exists).

STATUS REGISTER

Six inputs to the BU-63705 allow the subsystem host CPU to control bits in the RTU status word. The Illegal Command input may be used to set the Message Error bit in the Status Word and suppress the transmission of data to the bus controller. This line allows illegalization of any combination of commands. The latched Command Word may be connected to the address pins of an optional external PROM, which would drive the illegal Command line LOW when it identifies a command programmed as illegal.

STATUS REGISTER BIT ASSIGNMENTS

The $\overline{\text{SRQ}}$ (Subsystem Request) line is used to set the Status Word service request bit.

The $\overline{\text{ADBC}}$ (Accept Dynamic Bus Control) line is used to set the Status Word bus control bit.

The $\overline{\text{RTFLAG}}$ (RT Flag) Line is used to set the Status Word terminal flag bit.

The $\overline{\text{BUSY}}$ (Busy) line is used to set the Status Word busy bit, and inhibit subsystem requests for data.

The $\overline{\text{SSFLAG}}$ (SubSystem Flag) line is used to set the Status Word subsystem (fault) flag.

BUILT-IN-TEST

The BU-63705 contains a 14-bit Built-In-Test (BIT) word register which stores information about the condition of the RTU. When a mode code is received to transmit the BIT word, the contents of the BIT register is transmitted over the 1553 bus. FIGURE 3 shows the fault assigned to each bit in the BIT word. Conditions monitored are; transmitter timeouts, loop test failures, transmitter shutdown, subsystem handshake failure, and the results of individual message validations.

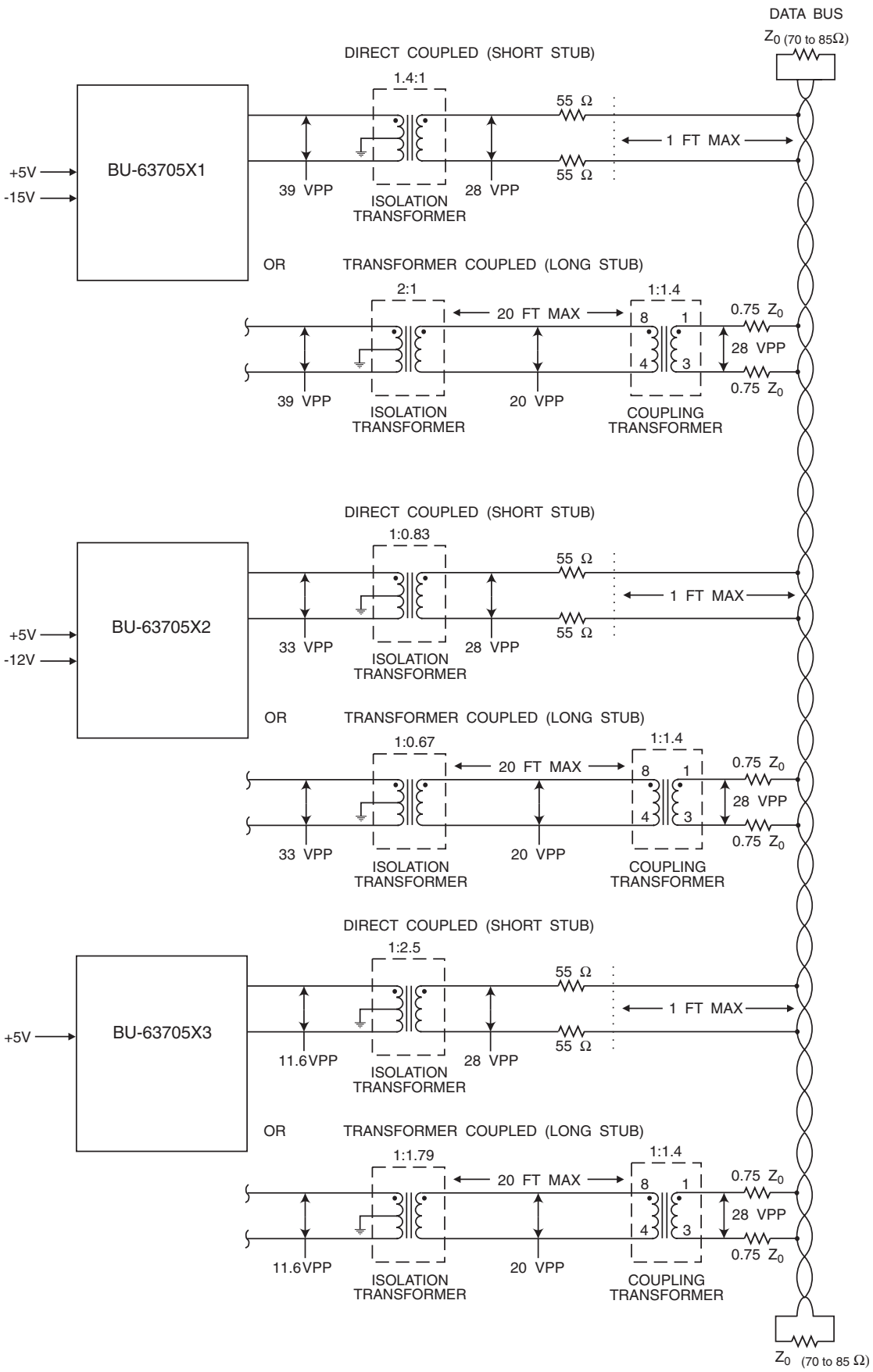


FIGURE 2. INTERFACE TO 1553 BUS

TRANSFORMER CONSIDERATIONS FOR BU-63705X3 (+5V ONLY VERSIONS)

In selecting isolation transformers to be used for the BU-63705 X3 (+5V only) versions, there is a limitation on the maximum amount of leakage inductance. If this limit is exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553. In addition, an excessive leakage imbalance may result in a transformer dynamic offset that exceeds 1553 specifications.

The maximum allowable leakage inductance is 6.0 µH, and is measured as follows:
The side of the transformer that connects to the Hybrid is defined as the "primary" winding. If one side of the primary is shorted to the primary center-tap, the inductance should be measured across the "secondary" (stub side) winding. This inductance must be less than 6.0 µH. Similarly, if the other side of the primary is shorted to the primary center-tap, the inductance measured across the "secondary" (stub side) winding must also be less than 6.0 µH.

The difference between these two measurements is the "differential" leakage inductance. This value must be less than 1.0 µH.

Beta Transformer Technology Corporation (BTTC), a subsidiary of DDC, manufactures transformers in a variety of mechanical configurations with the required turns ratios of 1:2.5 direct coupled, and 1:1.79 transformer coupled. Table 4 provides a listing of many of these transformers. For further information, contact BTTC at 631-244-7393 or at www.bttc-beta.com.

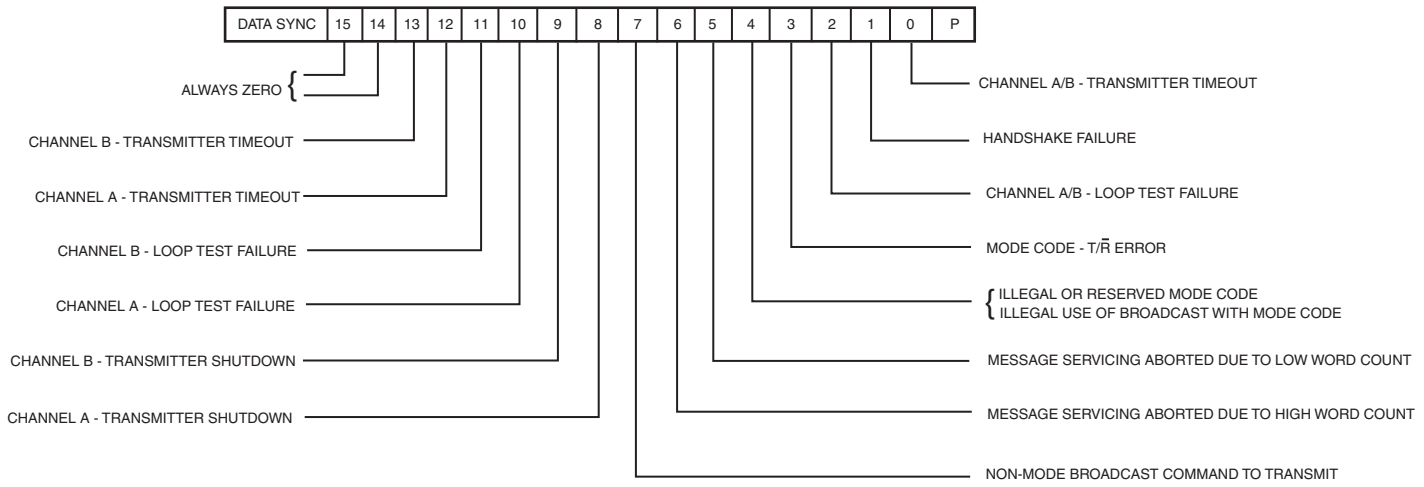
TABLE 4. BTTC TRANSFORMERS FOR USE WITH BU-63705X3

BTTC PART NUMBER	# OF CHANNELS, CONFIGURATION	COUPLING RATIO DESCRIPTION	COUPLING RATIO (1:X)	MOUNTING	MAX HEIGHT	WIDTH (INCLUDING LEADS)	LENGTH (INCLUDING LEADS)
MLP-2005	Single	Direct	(1:2.5)	SMT	0.185"	0.4"	0.52"
MLP-3005	Single	Direct	(1:2.5)	Through Hole	0.185"	0.4"	0.4"
B-3230 (-30) #	Single	Direct	(1:2.5)	Through Hole	0.25"	0.35"	0.5"
MLP-2205	Single	Transformer	(1:1.79)	SMT	0.185"	0.4"	0.52"
MLP-3205	Single	Transformer	(1:1.79)	Through Hole	0.185"	0.4"	0.4"
B-3229 (-29) #	Single	Transformer	(1:1.79)	Through Hole	0.25"	0.35"	0.5"
HLP-6015 #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	SMT	0.19"	0.63"	1.13"
B-3227 (-27) #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	SMT	0.29"	0.63"	1.13"
MLP-3305	Single	Direct & Transformer	(1:2.5) & (1:1.79)	Through Hole	0.185"	0.4"	0.4"
B-3226 (-26) #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	Through Hole	0.25"	0.625"	0.625"
HLP-6014 #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	Flat Pack	0.19"	0.63"	1.13"
B-3231 (-31) #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	Flat Pack	0.29"	0.63"	1.13"
DSS-2005	Dual (Side-by-Side)	Direct	(1:2.5)	SMT	0.13"	0.72"	0.96"
DSS-2205	Dual (Side-by-Side)	Transformer	(1:1.79)	SMT	0.13"	0.72"	0.96"
DSS-1005	Dual (Side-by-Side)	Direct & Transformer	(1:2.5) & (1:1.79)	SMT	0.165"	0.72"	0.96"
TSM-2005	Dual (Stacked)	Direct	(1:2.5)	SMT	0.32"	0.4"	0.52"
TSM-2205	Dual (Stacked)	Transformer	(1:1.79)	SMT	0.32"	0.4"	0.52"
TST-9117 #	Dual (Stacked)	Direct & Transformer	(1:2.5) & (1:1.79)	SMT	0.335"	1.125"	1.125"
TST-9107 #	Dual (Stacked)	Direct & Transformer	(1:2.5) & (1:1.79)	Through Hole	0.335"	0.625"	0.625"
TST-9127 #	Dual (Stacked)	Direct & Transformer	(1:2.5) & (1:1.79)	Flat Pack	0.335"	0.625"	0.625"

Notes:
1. All Transformers in the table above can be used with BU-6XXXXX3/6 (1553B transceivers).
2. Transformers identified with "#" in the table above are not recommended for use with the BU-6XXXXX4 (McAir-Compatable transceivers)

TABLE 5. ISOLATION TRANSFORMER GUIDE				
RT PART NUMBER	TURNS RATIO		RECOMMENDED XFORMER	
	DIRECT COUPLED	XFORMER COUPLED	PLUG-IN	SURFACE MOUNT
BU-63705X1	1.41:1	2:1	BUS-25679, B-2203, DESC M21038/27-02	B-2387, B-2343, DESC M21038/27 -12, M21038/27 -17 LPB-5002 LPB-5009 LPB-6002 LPB-6009
BU-63705X2	1:0.83	1:0.67	BUS-29854	LPB-5001 LPB-5008 LPB-6001 LPB-6008
	1.25:1 (See Note)		B-2204,DESC M21038/27-03	B-2388, DESC M21038/27 -13, B-2344, DESC M21038/27 -18
BU-63705X3	1:2.5	1:1.79	See TABLE 4	

Note: The B-2204, B-2388, and B-2344 transformers have a slightly different turns ratio on the direct coupled taps than the turns ratio of the BU-29854 direct-coupled taps. They do, however, have the same transformer coupled ratios. For transformer coupled applications, either transformer may be used. The transceiver in the BU-63705D2, and BU-63705F2 was designed to work with a 1:0.83 ratio for direct-coupled applications. For direct-coupled applications, the 1:0.83 turns ratio is recommended, but the 1.25:1 may be used. The 1.25:1 turns ratio will result in a slightly lower transmitter amplitude (approximately 3.6% lower) and a slight shift in the RT's receiver threshold.



NOTES

1. BITS 3-7 ARE CLEARED IN THE BEGINNING OF EACH NEW MESSAGE AND UPDATED AT THE END OF THE MESSAGE. THEY ONLY REFLECT THE PRESENT COMMAND WORD.
2. BITS 0-2 AND 10-13 ARE LATCHED AND ONLY CLEARED BY A MODE RESET COMMAND OR A MASTER RESET ($\overline{\text{RESET}}$).
3. BITS 8 AND 9 ARE SET ONLY BY THE MODE COMMAND FOR "TRANSMITTER SHUTDOWN" AND ARE CLEARED BY THE MODE COMMAND FOR "OVERRIDE TRANSMITTER SHUTDOWN" OR "RESET REMOTE TERMINAL". BITS 8 AND 9 ARE ALSO CLEARED BY $\overline{\text{RESET}}$.

FIGURE 3. BUILT-IN-TEST (BIT) WORD REGISTER

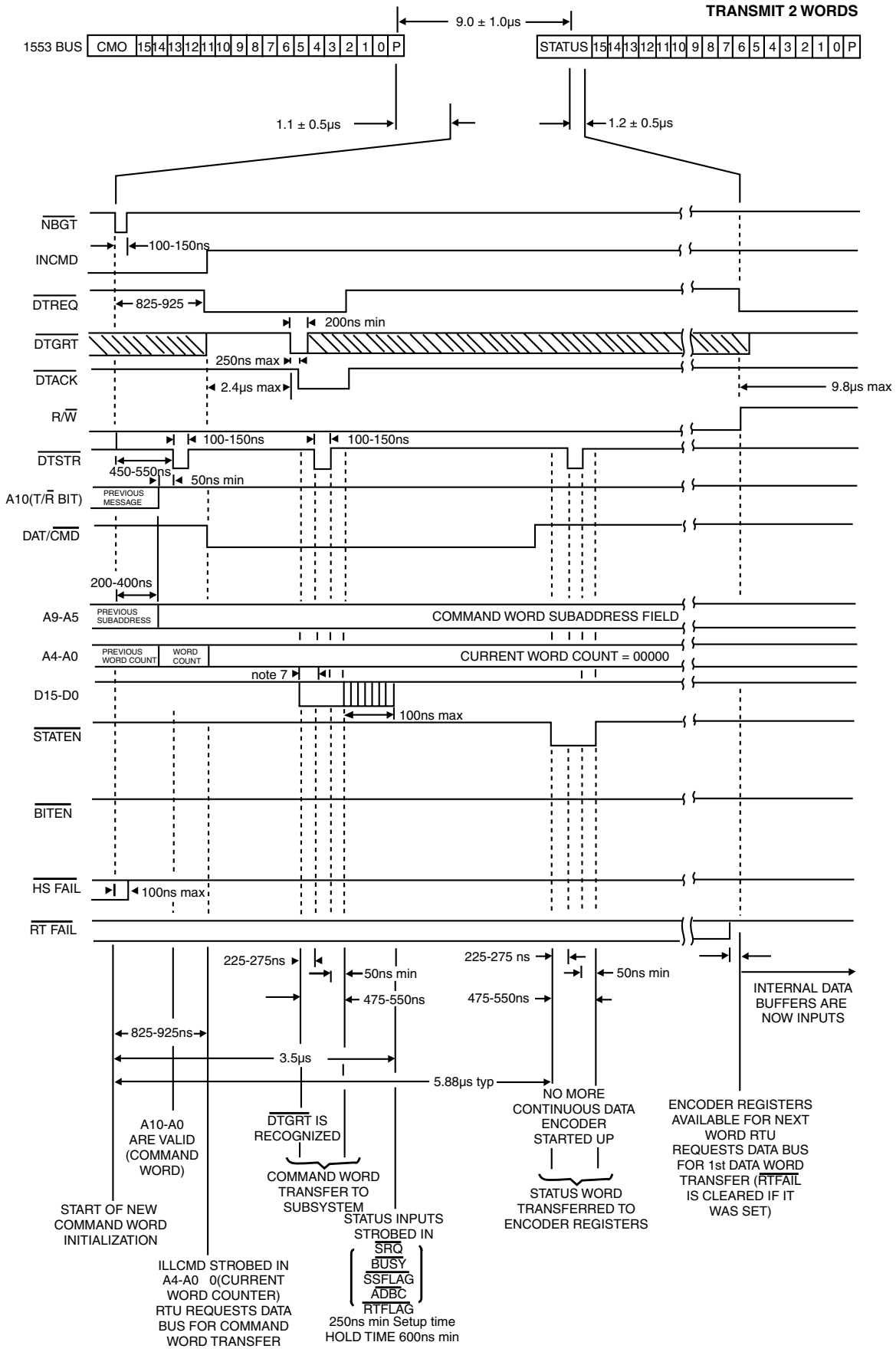
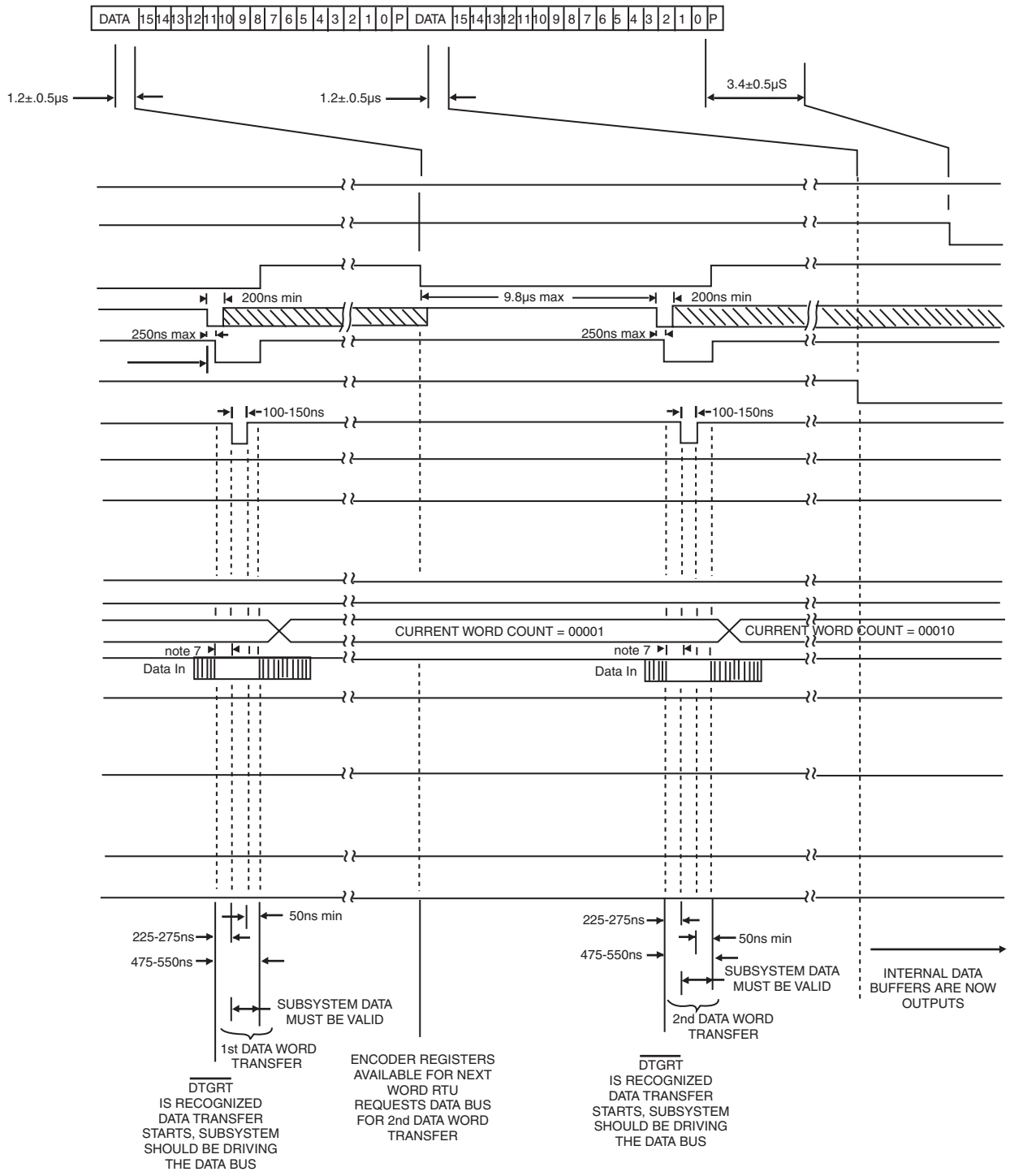


FIGURE 4. TRANSMIT TIMING DIAGRAM



NOTES

1. LEGEND
   - DON'T CARE
   - DATA BUS UNDEFINED
2. EACH WORD IS DRIVEN FOR ≅ 18-19µS ON D15-D05.
   IF BUF ENA IS ACTIVE THE LAST WORD IS AVAILABLE FOR 3.5-4µS SINCE THE STATUS WORD MUST BE SUPPORTED.
3. DATA BUS IS SHOWN WITH BUF ENA CONNECTED TO DTACK (SEE PIN FUNCTION TABLE, PIN 67)
4. THE POSITION OF DTACK WILL VARY DEPENDING ON WHEN DTGRT IS ISSUED.
5. HSFAIL IS ASSERTED UPON EXCESS DTGRT RESPONSE TIME.
   INCMD WILL SUBSEQUENTLY GO LOW, AND NO FURTHER DATA TRANSFERS WILL OCCUR.
6. RTFAIL IS CLEARED WHEN THE STATUS WORD IS TRANSMITTED. ONCE SET, FLAG WILL REMAIN SET FOR THE ENTIRE MESSAGE.
   THE INCMD FALLING EDGE CAN BE USED TO LATCH RTFAIL STATUS.
7. 100nS MIN REPRESENTS SETUP TIME FOR VALID DATA BEFORE DTSTR GOES LOW FOR A WRITE CYCLE.
   A READ CYCLE REQUIRES VALID DATA 160 nS MAX AFTER DTACK GOES LOW

FIGURE 4. TRANSMIT TIMING DIAGRAM (CONT)

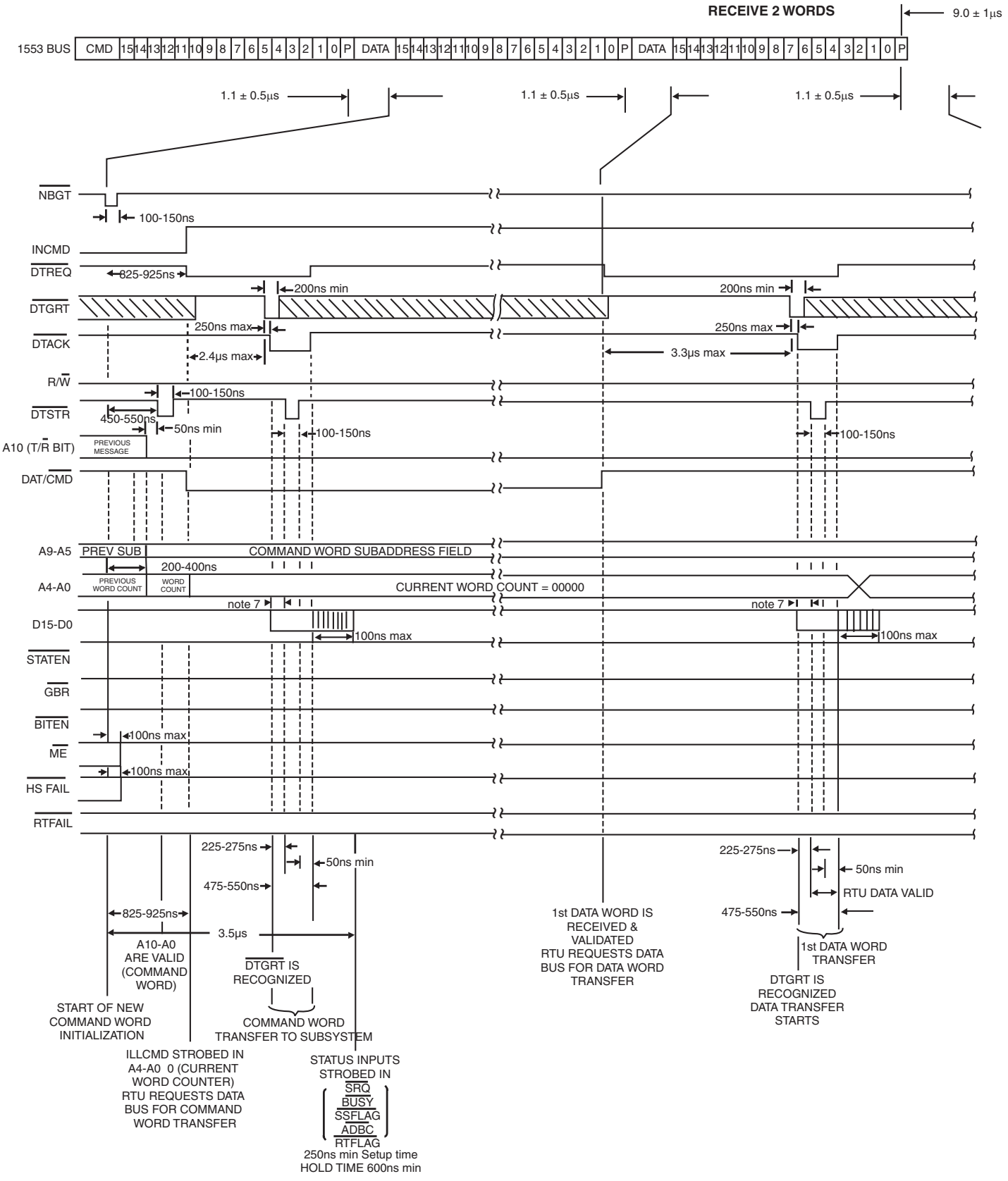
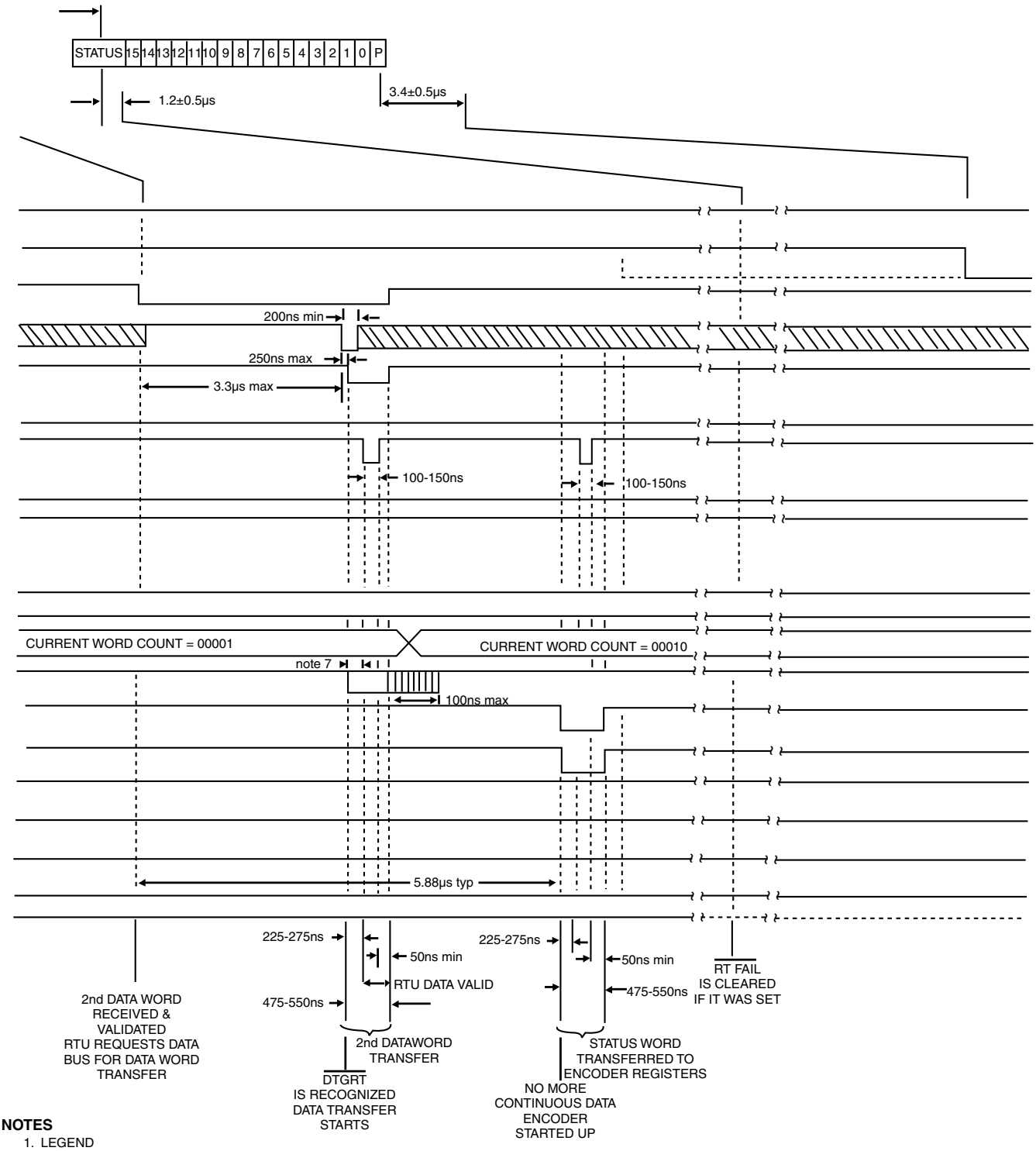


FIGURE 5. RECEIVE TIMING DIAGRAM



NOTES

1. LEGEND
   - DON'T CARE
   - DATA BUS UNDEFINED
   - ---- REPRESENTS THE SEQUENCE OF EVENTS IF THE COMMAND WAS BROADCAST.
     NOTE: NO STATUS WOULD BE TRANSMITTED ON 1553 BUS.
2. EACH WORD IS DRIVEN FOR ≅ 18-19µS ON D15-D0.
   IF BUF ENA IS ACTIVE THE LAST WORD IS AVAILABLE FOR 3.5-4µS SINCE THE STATUS WORD MUST BE SUPPORTED.
3. DATA BUS IS SHOWN WITH BUF ENA CONNECTED TO DTACK (SEE PIN FUNCTION TABLE, PIN 67)
4. THE POSITION OF DTACK WILL VARY DEPENDING ON WHEN DTGRT IS ISSUED.
5. HSFAIL IS ASSERTED UPON EXCESS DTGRT RESPONSE TIME. GBR WILL NOT BE SET.
6. RTFAIL IS CLEARED WHEN THE STATUS WORD IS TRANSMITTED. ONCE SET, FLAG WILL REMAIN SET FOR THE ENTIRE MESSAGE.
   THE INCMD FALLING EDGE CAN BE USED TO LATCH RTFAIL STATUS.
7. 100ns MIN REPRESENTS SETUP TIME FOR VALID DATA BEFORE DTSTR GOES LOW.

FIGURE 5. RECEIVE TIMING DIAGRAM (CONT)

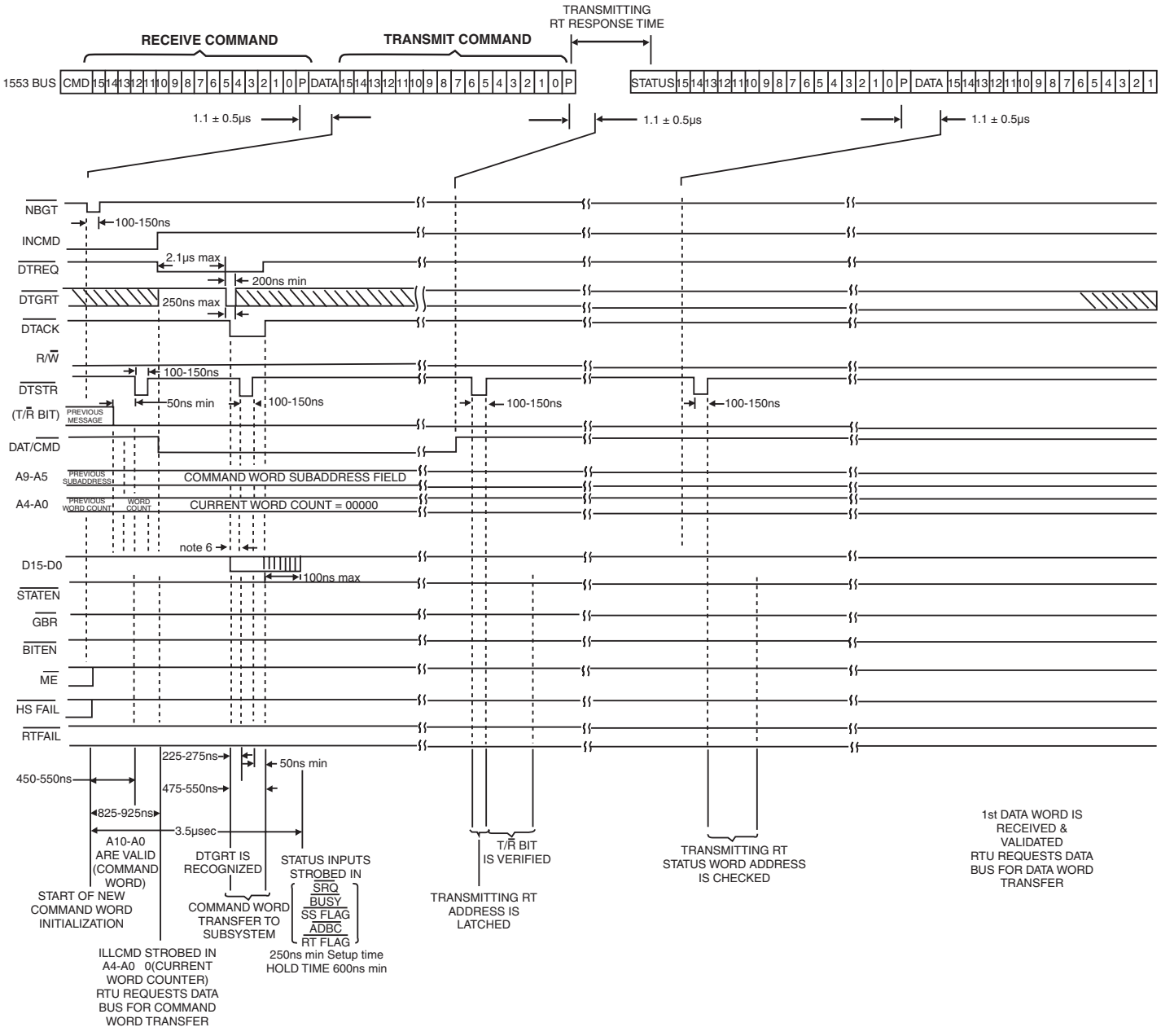
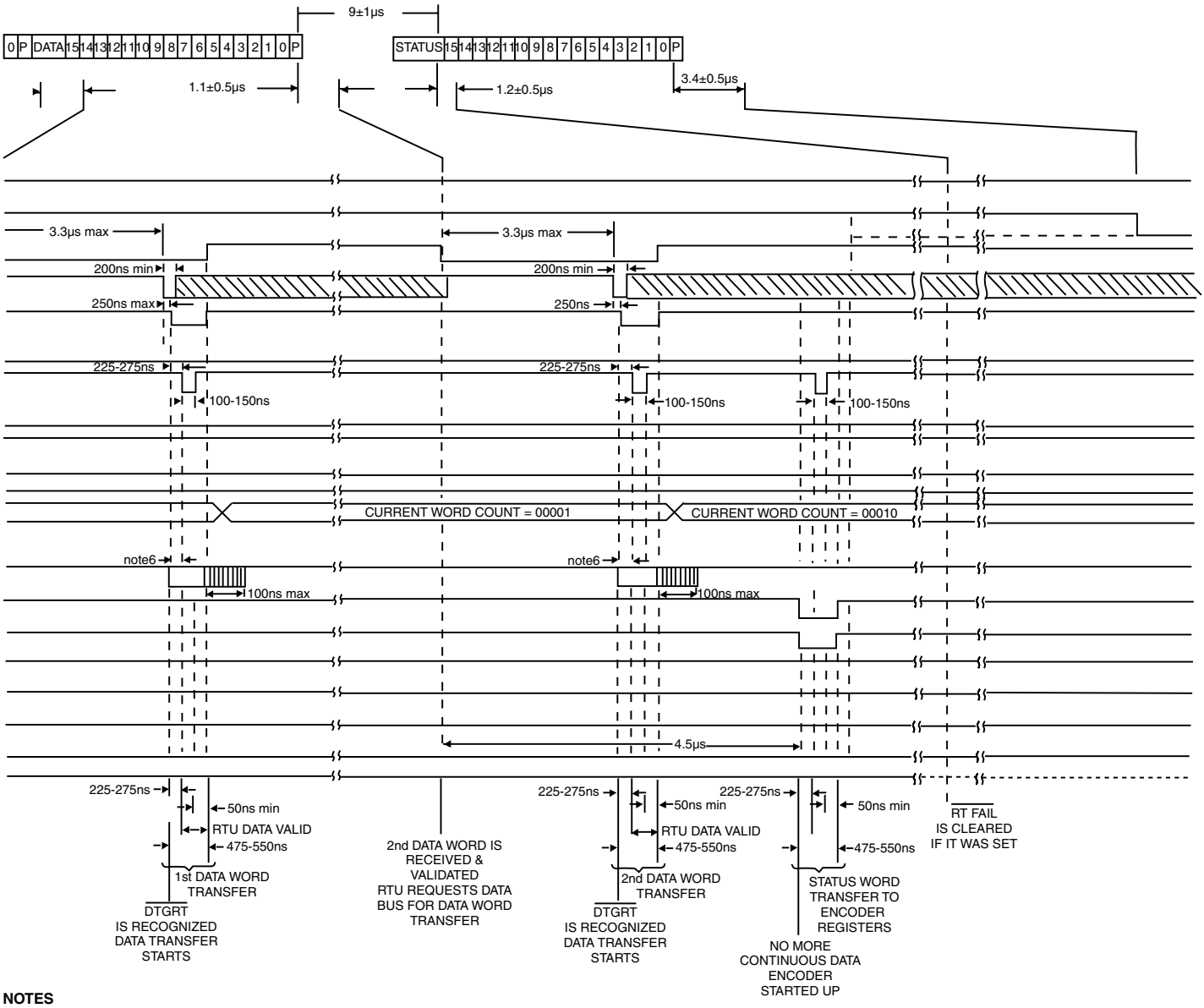


FIGURE 6. RT TO RT (RECEIVE) TIMING DIAGRAM



NOTES

1. LEGEND
   - DON'T CARE
   - DATA BUS UNDEFINED
   - ---- REPRESENTS THE SEQUENCE OF EVENTS IF THE COMMAND WAS BROADCAST.
     NOTE: NO STATUS WOULD BE TRANSMITTED ON 1553 BUS.
2. EACH WORD IS DRIVEN FOR ≅ 18-19µS ON D15-D0.
   IF $\overline{\text{BUF ENA}}$ IS ACTIVE THE LAST WORD IS AVAILABLE FOR 3.5-4µS SINCE THE STATUS WORD MUST BE SUPPORTED.
3. DATA BUS IS SHOWN WITH $\overline{\text{BUF ENA}}$ CONNECTED TO $\overline{\text{DTACK}}$ (SEE PIN FUNCTION TABLE, PIN 67)
4. THE TIMING DIAGRAM REPRESENTS A $\overline{\text{DTGRT}}$ RESPONSE TIME OF 0.92µS FOR COMMAND TRANSFER AND 2.1µS FOR DATA.
   THE MAXIMUM RESPONSE TIME FROM $\overline{\text{DTREQ}}$ TO $\overline{\text{DTGRT}}$ TO GUARANTEE A SUCCESSFUL TRANSFER IS 2.4µS FOR THE COMMAND TRANSFER AND 3.3µS FOR DATA TRANSFER TO THE SUBSYSTEM. THE POSITION OF $\overline{\text{DTACK}}$ WILL VARY DEPENDING ON WHEN $\overline{\text{DGRT}}$ IS ISSUED
5. $\overline{\text{RTFAIL}}$ IS CLEARED WHEN THE STATUS WORD IS TRANSMITTED. ONCE SET, FLAG WILL REMAIN SET FOR THE ENTIRE MESSAGE.
   THE INCMD FALLING EDGE CAN BE USED TO LATCH $\overline{\text{RTFAIL}}$ STATUS.
6. 100nS MIN REPRESENTS SETUP TIME FOR VALID DATA BEFORE $\overline{\text{DTSTR}}$ GOES LOW.

FIGURE 6. RT TO RT (RECEIVE) TIMING DIAGRAM (CONT)

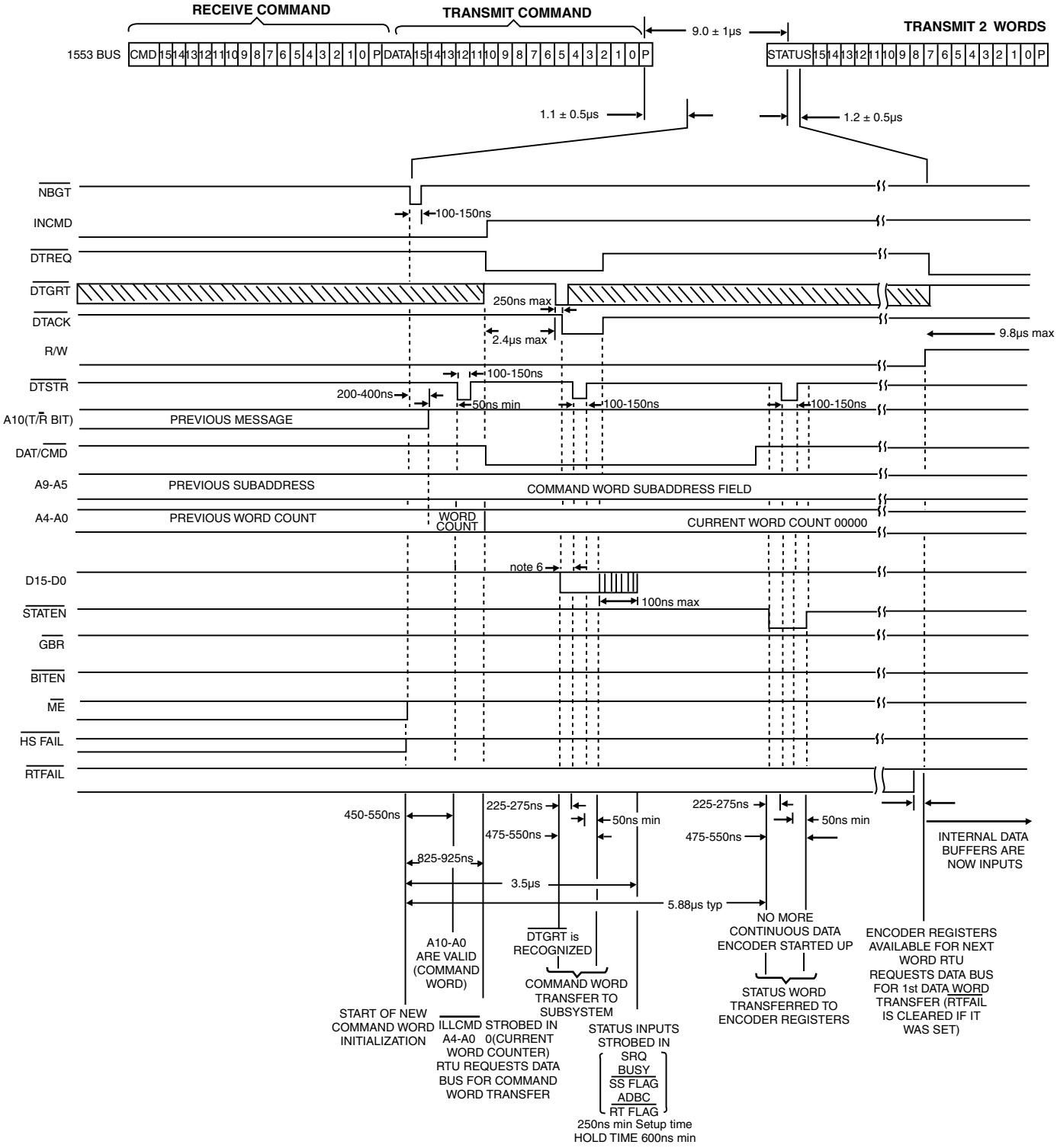
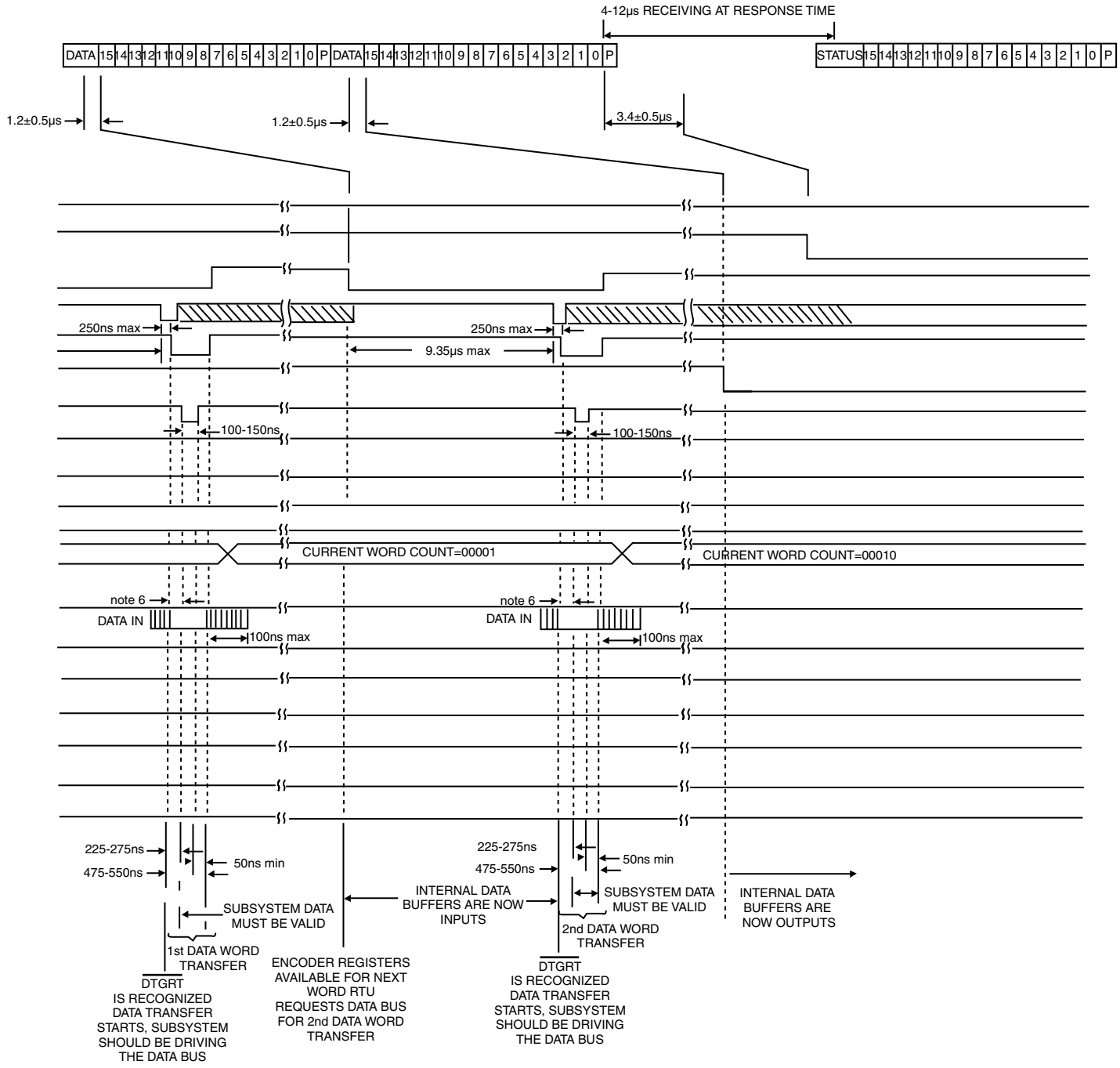


FIGURE 7. RT TO RT (TRANSMIT) TIMING DIAGRAM



NOTES

1. LEGEND
   - DON'T CARE
   - DATA BUS UNDEFINED
   - ---- REPRESENTS THE SEQUENCE OF EVENTS IF THE COMMAND WAS BROADCAST. NOTE: NO STATUS WOULD BE TRANSMITTED ON 1553 BUS.
2. EACH WORD IS DRIVEN FOR ≅ 18-19µS ON D15-D0. IF $\overline{\text{BUF ENA}}$ IS ACTIVE THE LAST WORD IS AVAILABLE FOR 3.5-4µS SINCE THE STATUS WORD MUST BE SUPPORTED.
3. DATA BUS IS SHOWN WITH $\overline{\text{BUF ENA}}$ CONNECTED TO $\overline{\text{DTACK}}$ (SEE PIN FUNCTION TABLE, PIN 67)
4. THE MAXIMUM RESPONSE TIME FROM $\overline{\text{DTREQ}}$ TO $\overline{\text{DTGRT}}$ TO GUARANTEE A SUCCESSFUL TRANSFER IS 2.4µS FROM THE COMMAND WORD AND 9.8µS FROM THE DATA TRANSFER FROM THE SUBSYSTEM. THE POSITION OF $\overline{\text{DTACK}}$ WILL VARY DEPENDING ON WHEN $\overline{\text{DGRT}}$ IS ISSUED.
5. $\overline{\text{RTFAIL}}$ IS CLEARED WHEN THE STATUS WORD IS TRANSMITTED. ONCE SET, FLAG WILL REMAIN SET FOR THE ENTIRE MESSAGE. THE INCMD FALLING EDGE CAN BE USED TO LATCH $\overline{\text{RTFAIL}}$ STATUS.
6. 100nS MIN REPRESENTS SETUP TIME FOR VALID DATA BEFORE $\overline{\text{DTSTR}}$ GOES LOW FOR A WRITE CYCLE. A READ CYCLE REQUIRES VALID DATA 150nS MAX AFTER $\overline{\text{DTACK}}$ GOES LOW.

FIGURE 7. RT TO RT (TRANSMIT) TIMING DIAGRAM (CONT)

MODE CODES

The BU-63705 implements all mode codes applicable to dual-redundant systems. Mode codes can also be illegalized using the appropriate I/O signals. Mode command illegalization and handling are detailed below in TABLE 6.

TABLE 6. MODE CODES IMPLEMENTED

DYNAMIC BUS CONTROL (00000)
MESSAGE SEQUENCE = DBC * STATUS
The RT responds with status. If the subsystem wants control of the bus, it must set DBACC.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error, DBA (SW), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits set: message error (S/W), T/$\overline{R}$ Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code, T/$\overline{R}$ Error (BIT Word).
5. **Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code (BIT Word).

SYNCHRONIZE WITHOUT DATA WORD (00001)
MESSAGE SEQUENCE = SYNC * STATUS
The RT responds with status. If sent as a broadcast, the broadcast receive bit will be set and status response suppressed.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits set: message error (S/W), T/$\overline{R}$ Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), T/$\overline{R}$ Error (BIT Word).

STATUS WORD (00010)
MESSAGE SEQUENCE = TRANSMIT WORD * STATUS
The status and BIT word registers are not altered by this command and contain the status from the previous command.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW)
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits set: message error (S/W), T/$\overline{R}$ Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), T/$\overline{R}$ Error (BIT Word).
5. **Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code (BIT Word).

INITIATE SELF-TEST (00011)
MESSAGE SEQUENCE = SELF TEST * STATUS
The RT responds with a status word. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Short-loop test is initiated on the status word transmitted. If the test fails, an RT fail flag is set.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits set: message error (S/W), T/$\overline{R}$ Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), T/$\overline{R}$ Error (BIT Word).
5. **Fault Test.** Bits set: RTFail Output Flag, A/$\overline{B}$ Loop Test Fail, Current 1553 Bus (A or B) Loop Test Fail (BIT Word)

TRANSMITTER SHUTDOWN (00100)
MESSAGE SEQUENCE =SHUTDOWN * STATUS
This command is only used with dual redundant bus systems. The RT responds with status. At the end of the status transmission, the RT inhibits any further transmission from the dual redundant channel. Once shutdown, the transmitter can only be reactivated by OVERRIDE TRANSMITTER SHUTDOWN or RESET RT commands or $\overline{\text{RESET}}$.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits set: message error (S/W), T/$\overline{R}$ Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), T/$\overline{R}$ Error (BIT Word).

***** = Status Response Time

TABLE 6. MODE CODES IMPLEMENTED (continued)

OVERRIDE TRANSMITTER SHUTDOWN (00101)
MESSAGE SEQUENCE = OVERRIDE SHUTDOWN * STATUS
This command is only used with dual redundant bus systems. The RTU responds with status. At the end of the status transmission, the RTU re-enables the transmitter of the redundant bus. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits set: message error, T/$\overline{R}$ Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), T/$\overline{R}$ Error (BIT Word).

INHIBIT TERMINAL FLAG BIT (00110)
MESSAGE SEQUENCE = INHIBIT TERMINAL FLAG * STATUS
The RTU responds with status and inhibits further internal or external setting of the terminal flag bit in the status register. Once the terminal flag has been inhibited, it can only be reactivated by an Override Inhibit Terminal Flag or Reset RT command or $\overline{\text{RESET}}$. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits set: message error (S/W), T/$\overline{R}$ Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), T/$\overline{R}$ Error (BIT Word).

OVERRIDE INHIBIT TERMINAL FLAG BIT (00111)
MESSAGE SEQUENCE = OVERRIDE INHIBIT TERMINAL FLAG * STATUS
The RTU responds with status and reactivates the terminal flag bit in the status register. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits set: message error (S/W), T/$\overline{R}$ Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), T/$\overline{R}$ Error (BIT Word).

RESET REMOTE TERMINAL (01000)
MESSAGE SEQUENCE = RESET REMOTE TERMINAL * STATUS
The RTU responds with status and internally resets. Transmitter shutdown and Inhibit Terminal Flag commands and BIT Word, will be reset. If the command was broadcast, the broadcast received bit is set and the status word is suppressed.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits Set: message error (S/W), T/$\overline{R}$ Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (S/W), T/$\overline{R}$ Error (BIT Word).

RESERVED MODE COMMAND (01001-01111)
MESSAGE SEQUENCE = RESERVED MODE COMMAND * STATUS
The RTU responds with clear status and no data. If the command is illegalized through an optional PROM, the message error bit is set and only the status word is transmitted.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW), High Word Count (BIT Word), Illegal Mode Code (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits set: message error (S/W), Illegal Mode Code (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code (BIT Word).

***** = Status Response Time

TABLE 6. MODE CODES IMPLEMENTED (continued)

TRANSMIT VECTOR WORD (10000)
MESSAGE SEQUENCE = TRANSMIT VECTOR WORD * STATUS VECTOR WORD
The RTU transmits a status word followed by a vector word.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits set: message error (S/W), Low Word Count (BIT Word) and T/$\overline{R}$ Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), T/$\overline{R}$ Error, Low Word Count (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (S/W), Illegal Mode Code, (BIT Word).

SYNCHRONIZE WITH DATA WORD (10001)
MESSAGE SEQUENCE = SYNCHRONIZE WITH DATA WORD * STATUS
The data word received following the command word is transferred to RAM. The status word is then transmitted. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits Set: message error (SW), Low Word Count (BIT Word)
3. **Command Followed by too many Data Words.** No status response. Bits Set: message error (SW), High Word Count (BIT Word)
4. **Command T/$\overline{R}$ bit Set to One.** No status response. Bits set: message error (S/W), T/$\overline{R}$ Error, High Word Count (BIT Word).
5. **Command T/$\overline{R}$ bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (S/W), High Word Count, T/$\overline{R}$ Error (BIT Word).

TRANSMIT LAST COMMAND (10010)
MESSAGE SEQUENCE = TRANSMIT LAST COMMAND * STATUS
The status and BIT word registers are not altered by this command. The SW contains the status from the previous command. The data word transmitted contains the previous valid command (providing it was not another TRANSMIT LAST COMMAND).
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW).
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits set: message error (S/W), T/$\overline{R}$ Error, Low Word Count (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No status response. Bits Set: message error (S/W), Broadcast (S/W), T/$\overline{R}$ Error (BIT Word), Low Word Count (BIT Word).
5. **Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code (BIT Word).

TRANSMIT BIT WORD (10011)
MESSAGE SEQUENCE = TRANSMIT BIT WORD * STATUS
The RTU responds with status followed by the BIT word. The BIT word is not altered by this command; however, the next SW will reflect errors i**n this transmissi**on**.**
ERROR CONDITIONS
1. Invalid Command. No response**, command ignored.**
2. **Command Fo**llowed by Data Word. No status response. Bits Set: Message Error (S/W)

***** = Status Response Time

TABLE 6. MODE CODES IMPLEMENTED (continued)

SELECTED TRANSMITTER SHUTDOWN (10100)
MESSAGE SEQUENCE = SELECTED TRANSMITTER SHUTDOWN * STATUS VECTOR WORD
The data word received is transmitted to the subsystem and status is transmitted. No other action is taken by the RTU. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Intended for use with RT's with more than one dual redundant channel.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits Set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word)
3. **Command Followed by too many Data Words.** No status response. Bits Set: message error (SW), High Word Count, Illegal Mode Code (BIT Word)
4. **Command T/$\overline{R}$ bit Set to One.** No status response. Bits set: message error (S/W), Illegal Mode Code, High Word Count (BIT Word).
5. **Command T/$\overline{R}$ bit Set to One and Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code, High Word Count (BIT Word).

OVERRIDE SELECTED TRANSMITTER SHUTDOWN (10101)
MESSAGE SEQUENCE = OVERRIDE SELECTED TRANSMITTER SHUTDOWN * STATUS
The data word received after the command is transferred to the subsystem. No other action is taken by the RTU. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits Set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word)
3. **Command Followed by too many Data Words.** No status response. Bits Set: message error (SW), High Word Count, Illegal Mode Code (BIT Word)
4. **Command T/$\overline{R}$ bit Set to One.** No status response. Bits set: message error (S/W), Illegal Mode Code, High Word Count (BIT Word).
5. **Command T/$\overline{R}$ bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (S/W), Illegal Mode Code, High Word Count (BIT Word).

RESERVED MODE CODES (10110-11111)
MESSAGE SEQUENCE = RESERVED MODE CODE (T/$\overline{R}$ = 1) * STATUS
RESERVED MODE CODE (T/$\overline{R}$ = 0) * STATUS
If Valid (T/$\overline{R}$ = 0)
The RTU responds with status. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed. If the command is illegalized through an optional PROM, the message error bit is set and only the status word is transmitted.
If Valid (T/$\overline{R}$ = 1)
Respond with status and one data word.
ERROR CONDITIONS (T/$\overline{R}$ = 1)
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).

ERROR CONDITIONS (T/$\overline{R}$ = 0)
1. **Invalid Command.** No response, command ignored.
2. **Command not followed by Contiguous Data Word.** No status response. Bits set: message error (S/W), Low Word Count, Illegal Mode Code (BIT Word).
3. **Command followed by too many Data Words.** No status response. Bits Set: message error (S/W), High Word Count, Illegal Mode Code (BIT Word).

UNDEFINED MODE CODES
(T/$\overline{R}$ = 0, MODE CODES 00000 TO 01111)
No Response, set message error bit status (T/R Error (BIT Word) [00000-01001] or Illegal Mode (BIT Word) [01001-01111]).

***** = Status Response Time

TABLE 7. PIN FUNCTIONS

PACKAGE & PIN		FUNCTION	DESCRIPTION
78-Pin QIP	78-Pin Flat-Pack		
1	1	A9 (SA4)	Latched output of the most significant bit (MSB) in the subaddress field of the command word.
2	3	A7 (SA2)	Latched output of the third most significant bit in the subaddress field of the command word.
3	5	A5 (SA0)	Latched output of the least significant bit (LSB) in the subaddress field of the command word.
4	7	DB1	Bi-directional parallel data bus Bit 1
5	9	DB3	Bi-directional parallel data bus Bit 3
6	11	DB5	Bi-directional parallel data bus Bit 5
7	13	DB7	Bi-directional parallel data bus Bit 7
8	15	DB9	Bi-directional parallel data bus Bit 9
9	17	DB11	Bi-directional parallel data bus Bit 11
10	19	DB13	Bi-directional parallel data bus Bit 13
11	21	DB15	Bi-directional parallel data bus Bit 15 (MSB)
12	23	BRO ENA	Broadcast enable - when HIGH, this input allows recognition of an RT address of all ones in the command word as a broadcast message. When LOW, it prevents response to RT address 31 unless it has the assigned terminal address.
13	25	ADDRE (RTAD4)	Input of the MSB of the assigned terminal address.
14	27	ADDRC (RTAD2)	Input of the 3rd MSB of the assigned terminal address.
15	29	ADDRA (RTAD0)	Input of the LSB of the assigned terminal address.
16	31	$\overline{\text{RTADERR}}$	Output signal used to inform subsystem of an address parity error. If LOW, indicates parity error and the RT will not respond to any command address to a single terminal. It will respond to broadcast commands if BRO ENA is HIGH.
17	33	$\overline{\text{TXDATA B}}$	LOW output to the primary side of the coupling transformer that connects B channel of the 1553 bus.
18	35	NC	
19	37	GND	Power Supply return connection.
20	39	RXDATA B	Input from the HIGH side of the primary side of the coupling transformer that connects to the B channel of the 1553 Bus.
21	78	A3 (WC3/ CWC3)	Multiplexed address line output. When INCMD is LOW or A5 thru A9 are all zeroes or all ones (Mode Command), it represents the latched output of the 2nd MSB in the word count field of the command word. When INCMD is HIGH and A5 thru A9 are not all zeroes or all ones, it represents the 2nd MSB of the current word counter.
22	76	A1 (WC1/ CWC1)	Multiplexed address line output. When INCMD is LOW or A5 thru A9 are all zeroes or all ones (Mode Command), it represents the latched output of the 2nd LSB in the word count field of the command word. When INCMD is HIGH and A5 thru A9 are not all zeroes or all ones, it represents the 2nd LSB of the current word counter.

TABLE 7. PIN FUNCTIONS (continued)

PACKAGE & PIN		FUNCTION	DESCRIPTION
78-Pin QIP	78-Pin Flat-Pack		
23	74	$\overline{\text{DTGRT}}$	Data transfer grant -- active LOW input signal from the subsystem that informs the RT, when DTREQ is asserted, to start the transfer. Once transfer is started, $\overline{\text{DTGRT}}$ can be removed.
24	72	INCMD	In-Command -- HIGH level output signal used to inform the subsystem that the RT is presently servicing a command.
25	70	$\overline{\text{HSFAIL}}$	Handshake Fail -- output signal that goes LOW and stays LOW whenever the subsystem fails to supply DTGRT in time to do a successful transfer. Cleared by the next NBGT.
26	68	$\overline{\text{DTSTR}}$	A LOW level output pulse (125ns) present in the middle of every data word transfer over the parallel data bus. Used to latch or strobe the data into memory, FIFOs, registers, etc. Recommended using the rising edge to clock data in.
27	66	(DAT/$\overline{\text{CMD}}$)	Address line output that is LOW whenever the command word is being transferred to the subsystem over the parallel data bus, and is HIGH whenever data words are being transferred.
28	64	$\overline{\text{RTFAIL}}$	Remote Terminal Failure -- latched active LOW output signal to the subsystem to flag detection of a remote terminal continuous self-test failure. Also set if the Watchdog Timeout circuit is activated. Cleared by the start of the next message transmission (status word) and set if problem is again detected.
29	62	$\overline{\text{DTREQ}}$	Data Transfer Request -- active LOW output signal to the subsystem indicating that the RT has data for or needs data from the subsystem and requests a data transfer over the parallel data bus. Will stay LOW until transfer is completed or transfer timeout has occurred.
30	60	$\overline{\text{ADBC}}$	Accept Dynamic Bus Control -- active LOW input signal from the subsystem used to set the Dynamic Bus Control Acceptance bit in the status register if the command word was a valid, legal mode command for dynamic bus control.
31	58	TEST 2	Factory test point output-DO NOT USE (see note 1)*
32	56	A10 (T/$\overline{\text{R}}$)	Latched output of the T/$\overline{\text{R}}$ bit in the command word.
33	54	$\overline{\text{ILLCMD}}$	Illegal Command -- active LOW input signal from the subsystem, strobed in on the rising edge of INCMD. Used to define the command word as illegal and to set the message error bit in the status register.
34	52	$\overline{\text{SS REQ}}$	Subsystem Service Request -- Input from the subsystem used to control the Service Request Bit in the status register. If LOW when the status word is updated, the Service Request Bit will be set; if HIGH, it will be cleared.
35	50	$\overline{\text{BITEN}}$	Built-in-Test Word Enable -- LOW level output pulse (.5µs), present when the built-in-test word is enabled on the parallel data bus.
36	48	$\overline{\text{RXDATA A}}$	Input from the LOW side of the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.

TABLE 7. PIN FUNCTIONS (continued)

PACKAGE & PIN		FUNCTION	DESCRIPTION
78-Pin QIP	78-Pin Flat-Pack		
37	46	+5VA	+5V input power supply connection for the A channel transceiver.
38	44	-VA	-15V/-12V input power supply connection for the BU-63705X1/2 A Channel transceiver (No connection for BU-63705X3).
39	42	TXDATA A	HIGH output to the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
40	40	$\overline{\text{NBGT}}$	New Bus Grant -- LOW level output pulse (125ns) used to indicate the start of a new protocol sequence in response to the command word just received.
41	2	A8 (SA3)	Latched output of the 2nd MSB in the subaddress field of the command word.
42	4	A6 (SA1)	Latched output of the 2nd LSB in the subaddress field of the command word.
43	6	DB0	Bi-directional parallel data bus Bit 0 (LSB)
44	8	DB2	Bi-directional parallel data bus Bit 2
45	10	DB4	Bi-directional parallel data bus Bit 4
46	12	DB6	Bi-directional parallel data bus Bit 6
47	14	DB8	Bi-directional parallel data bus Bit 8
48	16	DB10	Bi-directional parallel data bus Bit 10
49	18	DB12	Bi-directional parallel data bus Bit 12
50	20	DB14	Bi-directional parallel data bus Bit 14
51	22	+5V	+5V input power supply connection for RTU digital logic section.
52	24	GND	Power supply return.
53	26	ADDRD	Input of the 2nd MSB of the assigned terminal address.
54	28	ADDRB	Input of the 2nd LSB of the assigned terminal address.
55	30	ADDRP	Input of Address Parity Bit. The combination of assigned terminal address and ADDRP must be odd parity for the RT to work.
56	32	TXDATA B	HIGH, output to the primary side of the coupling transformer that connects to the B channel transceiver.
57	34	-VB	-15V/-12V input power supply connection for the BU-63705X1/2 B Channel transceiver (No connection for BU-63705X3).
58	36	+5VB	+5 V input power supply connection for the B channel transceiver.
59	38	$\overline{\text{RXDATA B}}$	Input from the LOW side of the primary side of the coupling transformer that connects to the B channel of the 1553 Bus.
60	77	A2 (WC2/ CWC2)	Multiplexed address line output. When INCMD is LOW or A5 thru A9 are all zeroes or all ones (Mode Command), it represents the latched output of the 3rd MSB in the word count field of the command word. When INCMD is HIGH and A5 thru A9 are not all zeroes or all ones, it represents the 3rd MSB of the current word counter.

TABLE 7. PIN FUNCTIONS (continued)

PACKAGE & PIN		FUNCTION	DESCRIPTION
78-Pin QIP	78-Pin Flat-Pack		
61	75	A0 (WCO/ CWCO)	Multiplexed address line output. When INCMD is LOW or A5 thru A9 are all zeroes or all ones (Mode Command), it represents the latched output of the LSB in the word count field of the command word. When INCMD is HIGH and A5 thru A9 are not all zeroes or all ones, it represents the LSB of the current word counter.
62	73	$\overline{\text{DTACK}}$	Data Transfer Acknowledge -- active LOW output signal during data transfers to or from the subsystem indicating the RTU has received the DTGRT in response to DTREQ and is presently doing the transfer. Can be connected directly to (BUF ENA) for control of tri-state data buffers; and to tri-state address buffer control lines, if they are used.
63	71	A4 (WC4/ CWC4)	Multiplexed address line output. When INCMD is LOW or A5 thru A9 are all zeroes or all ones (Mode Command), it represents the latched output of the MSB in the word count field of the command word. When INCMD is HIGH and A5 thru A9 are not all zeroes or all ones, it represents the MSB of the current word counter.
64	69	RD/$\overline{\text{WR}}$	Read/Write - output signal controls direction of the internal data bus buffers (logic "1"= reading data via D15-D0; logic "0" = writing data via D15-D0). Prior to reception of a 1553 command word, RD/$\overline{\text{WR}}$ will be logic "0", indicating that the BU(S)-65142 is writing data to the connected subsystem. Following the reception/transfer of a transmit command word, RD/$\overline{\text{WR}}$ transitions from low to high, remains high until after the last data word is read from the system for transmission on the 1553 bus. After that last data word transfer, RD/$\overline{\text{WR}}$ returns to logic "0".
65	67	$\overline{\text{GBR}}$	Good Block Received -- LOW level output pulse (.5µs) used to flag the subsystem that a valid, legal, non-mode receive command with the correct number of data words has been received without a message error and successfully transferred to the subsystem.
66	65	16MHz IN	16MHz Clock Input -- input for the master clock used to run RTU circuits.
67	63	$\overline{\text{BUF ENA}}$	Buffer Enable -- input used to enable or tri-state the internal data bus buffers when they are driving the bus. When LOW, the data bus buffers are enabled. Could be connected to DTACK, if RT is sharing the same data bus as the subsystem. (see note 2)*.
68	61	$\overline{\text{RESET}}$	Input resets entire RT when LOW.
69	59	$\overline{\text{RTFLAG}}$	Remote Terminal Flag -- Input signal used to control the terminal flag bit in the status register. If LOW when the status word is updated, the terminal flag bit would be set; if HIGH, it would be cleared. Normally connected to RTFAIL.
70	57	$\overline{\text{TEST 1}}$	Watchdog Timeout test point -- DO NOT USE. (See note 3)* (input).

TABLE 7. PIN FUNCTIONS (continued)

PACKAGE & PIN		FUNCTION	DESCRIPTION
78-Pin QIP	78-Pin Flat-Pack		
71	55	$\overline{\text{SSBUSY}}$	Subsystem Busy - input from the subsystem used to control the busy bit in the status register. If LOW when the status word is updated, the busy bit will be set, if HIGH it will be cleared. If the busy bit is set in the status register, no data will be requested from the subsystem in response to a transmit command. On receive commands, data will be transferred to the subsystem.
72	53	$\overline{\text{SSFLAG}}$	Subsystem Flag -- input from the subsystem used to control the subsystem flag bit in the status register. If LOW when the status word is updated, the subsystem flag will be set; if HIGH it will be cleared.
73	51	$\overline{\text{ME}}$	Message Error -- output signal that goes LOW and stays LOW whenever there is a format or word error with the received message over the 1553 Data Bus. Cleared by the next NGBT.
74	49	RXDATA A	Input from the HIGH side of the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
75	47	GND	Power supply return connection.
76	45	N/C	Not connected.
77	43	$\overline{\text{TXDATA A}}$	Low output to the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
78	41	$\overline{\text{STATEN}}$	Status Word Enable -- LOW level active output signal present when the status word is enabled on the parallel data bus.
_	_	N/C	These pins are not used on this package.

PIN FUNCTION TABLE NOTES (TABLE 7) :

1. TEST 2 - Factory Test Point
This pin provides the output of the BU-63705 BIT Comparison output. A logic 1 (high) indicates a mismatch. Normally this pin is left open.

2. $\overline{\text{BUFENA}}$
This pin is typically tied to $\overline{\text{DTACK}}$, causing the BU-63705 to drive the shared data bus only while $\overline{\text{DTACK}}$ is active. If desired $\overline{\text{BUFENA}}$ can be grounded. The data will remain latched on the data bus pins for 18µs from $\overline{\text{DTSTR}}$ and 3.5µs for the last word of a message as the device's status word or BIT word is transferred to the BC ($\overline{\text{STATEN}}$ or $\overline{\text{BITEN}}$ low). Once the STATUS or BIT Word transfer is complete, the data bus will automatically again contain the last data word. The BU-63705 will automatically switch the direction of the internal buffers during a transmit operation.

3. $\overline{\text{TEST 1}}$
This test allows the user to force the active channel to transmit indefinitely, in order to test the built-in Watchdog Timer feature of the BU-63705. When this pin is grounded and the active channel is stimulated with a valid transmit command, the BU-63705 will respond with a status word and contiguous data (last data word loaded or STATUS WORD if none is loaded) until the built-in time out occurs. Normally this pin is left open or an optional pull-up can be used.

4. $-V_A$ and $-V_B$ are not connected (N/C) for BU-63705X3.

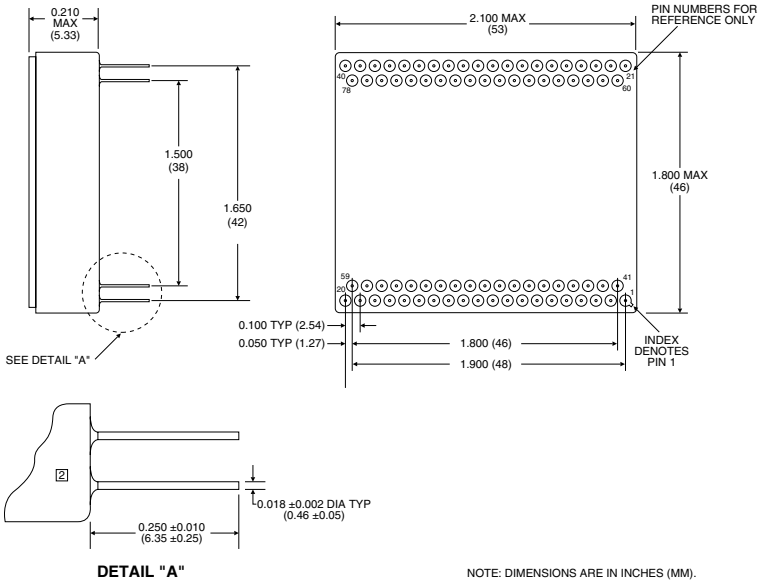
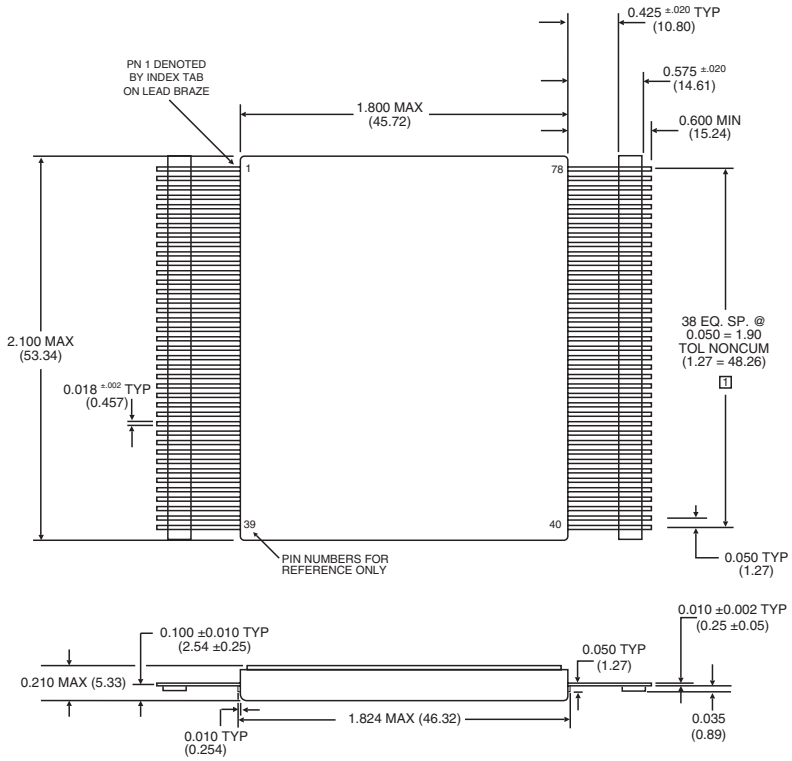


FIGURE 8. BU-63705D MECHANICAL OUTLINE (HI-REL / RADIATION TOLERANT VERSION) (78-PIN CERAMIC QIP)



NOTES:
1. LEAD CLUSTER TO BE CENTRALIZED ABOUT CASE CENTER LINE WITHIN ±0.010.
2. DIMENSIONS ARE IN INCHES (MM).

FIGURE 9. BU-63705F MECHANICAL OUTLINE (HI-REL / RADIATION TOLERANT VERSION) (78-PIN CERAMIC FLAT PACK)

ORDERING INFORMATION

BU-63705F3-120X

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = 100% Pull Test (standard on this device)
- Q = 100% Pull Test and Pre-Cap Source Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source Inspection
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source Inspection and 100% Pull Test
- Blank = None of the Above

Test Criteria:
- 0 = Standard Testing
- 1 = X-Ray

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In
- 1 = MIL-PRF-38534 Compliant **(notes 1 and 3)**
- 2 = B **(note 2)**
- 3 = MIL-PRF-38534 Compliant **(notes 1 and 3)** with PIND Testing
- 4 = MIL-PRF-38534 Compliant **(notes 1 and 3)** with Solder Dip
- 5 = MIL-PRF-38534 Compliant **(notes 1 and 3)** with PIND Testing and Solder Dip
- 6 = B **(note 2)** with PIND Testing
- 7 = B **(note 2)** with Solder Dip
- 8 = B **(note 2)** with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Transceiver Option:
- 1 = +5 Volts and -15 Volts
- 2 = +5 Volts and -12 Volts
- 3 = +5 Volts (Only)

Package Options:
- D = 78-pin QIP Package
- F = 78-pin Flatpack

Product Type:
- BU-63705 = “SPACE RT II” Radiation Tolerant Remote Terminal
- BU-K3705 = MIL-PRF-38534 Class K Compliant, “SPACE RT II” Radiation Tolerant Remote Terminal

(**Consult the Factory or Local Representative for Lead Times.)**

Notes:
1. Standard processing on this device includes 320 hours of burn-in and 100% non-destruct pull-test. (See Table 3).
2. Standard DDC Processing, with 160 hour burn-in and full temperature (-55°C to +125°C) test.
3. MIL-PRF-38534 product grading is designated with the following dash numbers:
   - Class H is a -11X, 13X, 14X, 15X, 41X, 43X, 44X, 45X
   - Class G is a -21X, 23X, 24X, 25X, 51X, 53X, 54X, 55X
   - Class D is a -31X, 33X, 34X, 35X, 81X, 83X, 84X, 85X
4. The above products contain tin-lead solder finish as applicable to solder dip requirements.
5. MIL-PRF-38534 Class K requires PIND testing, X-ray, and 100% Pull test (-X31X or -X51X with L, Q, Y, or Z as the last digit).

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 (note 1), 1030 (note 2)	TABLE 1

Notes:
1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

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