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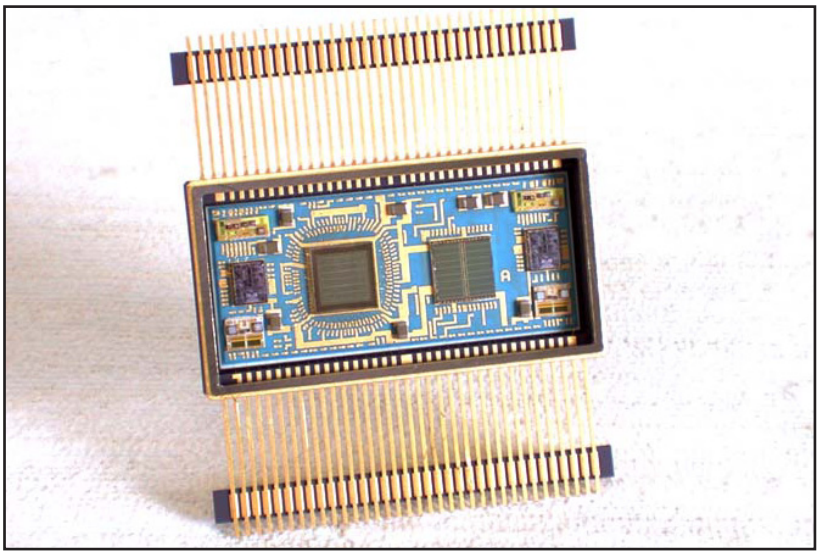
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BU-63825

# SPACE LEVEL MIL-STD-1553 BC/RT/MT ADVANCED COMMUNICATION ENGINE (SP'ACE II) TERMINAL

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## DESCRIPTION

The BU-63825(925) is a fully hardware & software compatible, direct drop-in replacement for the BU-61582(83).

DDC's BU-63825(925) Space Advanced Communication Engine (Sp'ACE II) is a radiation hardened version of the BU-61580(81) ACE terminal. DDC supplies the BU-63825 with enhanced screening for space and other high reliability applications.

The BU-63825 provides a complete integrated BC/RT/MT interface between a host processor and a MIL-STD-1553 bus. The BU-63825(925) provides functional and software compatibility with the standard BU-61580(81) product and is packaged in the same 1.9 square-inch package footprint.

As an option, DDC can supply the BU-63825 with space level screening. This entails enhancements in the areas of element evaluation and screening procedures for active and passive elements, as well as the manufacturing and screening processes used in producing the terminals.

The BU-63825 integrates dual transceiver, protocol, memory management and processor interface logic, and 16K words of RAM in the choice of 70-pin DIP or flat pack packages. Transceiverless versions may be used with an external electrical or fiber optic transceiver.

To minimize board space and 'glue' logic, the Sp'ACE II terminals provide flexibility in interfacing to a host processor and internal/external RAM.

## FEATURES

- Direct Replacement for BU-61582 and BU-61583
- Radiation Tolerant & Radiation Hardened Versions
- Fully Integrated 1553 Terminal
- Flexible Processor Interface
- 16K x 16 Internal RAM
- Automatic BC Retries
- Programmable BC Gap Times
- BC Frame Auto-Repeat
- Intelligent RT Data Buffering
- Ceramic Package
- Multiple Ordering Options;
  +5V (Only)
  +5V/-15V
  +5V/-12V
  +5V/Transceiverless
  +5V (Only, with Transmit Inhibits)

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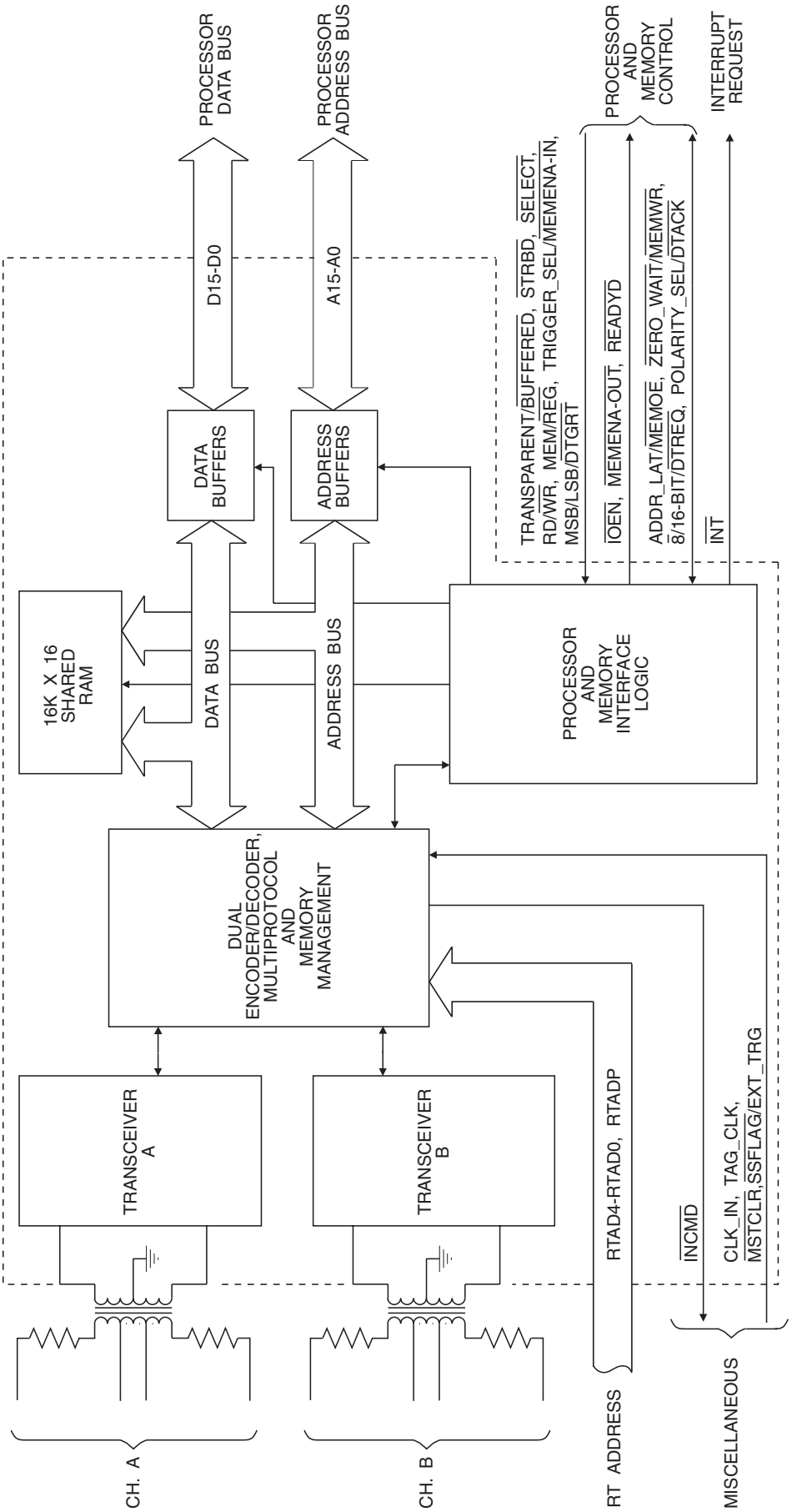



**FIGURE 1. BU-63825 BLOCK DIAGRAM**

## TABLE 1. SP'ACE II SERIES SPECIFICATIONS

| PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|
| **ABSOLUTE MAXIMUM RATING** | | | | |
| Supply Voltage | | | | |
| ■ Logic +5V | -0.5 | | 6.5 | V |
| ■ Transceiver +5V | -0.5 | | 7.0 | V |
| ■ -15V | +0.5 | | -18.0 | V |
| ■ -12V | +0.5 | | -18.0 | V |
| Logic | | | | |
| ■ Voltage Input Range | -0.5 | | $V_{CC}$+0.5 | V |
| **RECEIVER** | | | | |
| Differential Input Resistance | | | | |
| X1/X2 (Notes 1-6) | 11 | | | kΩ |
| X3/X6 (Notes 1-6) | 2.5 | | | kΩ |
| Differential Input Capacitance | | | | |
| X1/X2 (Notes 1-6) | | | 10 | pF |
| X3/X6 (Notes 1-6) | | | 25 | pF |
| Threshold Voltage, Transformer Coupled, Measured on Stub | | | 0.860 | Vp-p |
| Common Mode Voltage (Note 7) | | | 10 | Vpeak |
| **TRANSMITTER** | | | | |
| Differential Output Voltage | | | | |
| ■ Direct Coupled Across 35 Ω, Measured on Bus | 6 | 7 | 9 | Vp-p |
| ■ Transformer Coupled Across 70 Ω, Measured on Bus | 18 | 20 | 27 | Vp-p |
| Output Noise, Differential (Direct Coupled) | | | 10 | mVp-p, diff |
| Output Offset Voltage, Transformer Coupled Across 70 ohms | -250 | | 250 | mV |
| Rise/Fall Time | 100 | 150 | 300 | nsec |
| **LOGIC (Note 12)** | | | | |
| $V_{IH}$ ($V_{CC}$ = 5.5V) | | | | |
| $\overline{MSTCLR}$, CLOCK_IN, $\overline{STRBD}$ | 3.85 | | | V |
| All other inputs | 2 | | | V |
| $V_{IL}$ ($V_{CC}$ = 4.5V) | | | | |
| $\overline{MSTCLR}$, CLOCK_IN, $\overline{STRBD}$ | | | 1.35 | V |
| All other inputs | | | 0.8 | V |
| Hysteresis | | | | |
| $\overline{MSTCLR}$, CLOCK_IN, $\overline{STRBD}$ | 0.5 | | | V |
| $I_{IH}$ ($V_{CC}$=5.5V, $V_{IN}$=2.7V) | | | | |
| CLOCK_IN | -10 | | +10 | µA |
| All other inputs | -400 | | -20 | µA |
| $I_{IL}$ ($V_{CC}$=5.5V, $V_{IN}$=0.0V) | | | | |
| CLOCK_IN | -10 | | +10 | µA |
| All other inputs | -600 | | -60 | µA |
| $V_{OH}$ ($V_{CC}$=4.5V, $I_{OH}$=max) | 4 | | | V |
| $V_{OL}$=($V_{CC}$=4.5V, $I_{OL}$=max) | | | 0.5 | V |
| $I_{OH}$ ($V_{CC}$=4.5V)(Note 13) | | | -8 | mA |
| $I_{OL}$= ($V_{CC}$=4.5V) | | | 8 | mA |
| **POWER SUPPLY REQUIREMENTS** | | | | |
| Voltages/Tolerances | | | | |
| ■ BU-63825/925X0 | | | | |
| • +5V (Logic) | 4.5 | 5.0 | 5.5 | V |
| ■ BU-63825/925X1 | | | | |
| • +5V (Logic) | 4.5 | 5.0 | 5.5 | V |
| • +5V ( Ch. A, Ch. B) | 4.5 | 5.0 | 5.5 | V |
| • $V_A$ $V_B$ | -14.25 | -15.0 | -15.75 | V |
| ■ BU-63825/925X2 | | | | |
| • +5V (Logic) | 4.5 | 5.0 | 5.5 | V |
| • +5V ( Ch. A, Ch. B) | 4.5 | 5.0 | 5.5 | V |
| • $V_A$ $V_B$ | -11.4 | -12.0 | -12.6 | V |

## TABLE 1. SP'ACE II SERIES SPECIFICATIONS (CONT)

| PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS (Cont'd)** | | | | |
| Voltages/Tolerances (cont'd) | | | | |
| ■ BU-63825/925X3/X6 (+5V Only) | | | | |
| • +5V (Logic) | 4.5 | 5.0 | 5.5 | V |
| • +5V ( Ch. A, Ch. B) | 4.75 | 5.0 | 5.25 | V |
| Current Drain (Total Hybrid) | | | | |
| ■ BU-63825/925X0 | | | | |
| • +5V (Logic) | | 50 | 190 | mA |
| ■ BU-63825/925X1 | | | | |
| • +5V (Note 10) | | 140 | 240 | mA |
| • -15V Idle | | 30 | 60 | mA |
| • 25% Transmitter Duty Cycle | | 68 | 108 | mA |
| • 50% Transmitter Duty Cycle | | 105 | 175 | mA |
| • 100% Transmitter Duty Cycle | | 180 | 270 | mA |
| ■ BU-63825/925X2 | | | | |
| • +5V (Note 10) | | 140 | 240 | mA |
| • -12V Idle | | 30 | 60 | mA |
| • 25% Transmitter Duty Cycle | | 80 | 120 | mA |
| • 50% Transmitter Duty Cycle | | 130 | 185 | mA |
| • 100% Transmitter Duty Cycle | | 230 | 305 | mA |
| ■ BU-63825/925X3/X6 (+5V) (Logic, CH. A & CH. B) | | | | |
| • Idle | | | 250 | mA |
| • 25% Transmitter Duty Cycle | | | 355 | mA |
| • 50% Transmitter Duty Cycle | | | 460 | mA |
| • 100% Transmitter Duty Cycle | | | 670 | mA |
| **POWER DISSIPATION** | | | | |
| Total Hybrid | | | | |
| ■ BU-63825/925X0 | | 0.250 | 0.750 | W |
| ■ BU-63825/925X1 | | | | |
| • Idle | | 0.875 | 2.1 | W |
| • 25% Transmitter Duty Cycle | | 1.22 | 2.5 | W |
| • 50% Transmitter Duty Cycle | | 1.475 | 2.97 | W |
| • 100% Transmitter Duty Cycle | | 2.0 | 3.77 | W |
| ■ BU-63825/925X2 | | | | |
| • Idle | | 0.86 | 1.92 | W |
| • 25% Transmitter Duty Cycle | | 1.16 | 2.35 | W |
| • 50% Transmitter Duty Cycle | | 1.46 | 2.84 | W |
| • 100% Transmitter Duty Cycle | | 2.06 | 3.71 | W |
| ■ BU-63825/925X3/X6 | | | | |
| • Idle | | | 1.34 | W |
| • 25% Transmitter Duty Cycle | | | 1.57 | W |
| • 50% Transmitter Duty Cycle | | | 1.79 | W |
| • 100% Transmitter Duty Cycle | | | 2.23 | W |
| Hottest Die | | | | |
| ■ BU-63825/925X0 | | 0.225 | 0.50 | W |
| ■ BU-63825/925X1 | | | | |
| • Idle | | 0.335 | 0.68 | W |
| • 25% Transmitter Duty Cycle | | 0.600 | 1.06 | W |
| • 50% Transmitter Duty Cycle | | 0.860 | 1.45 | W |
| • 100% Transmitter Duty Cycle | | 1.385 | 2.23 | W |
| ■ BU-63825/925X2 | | | | |
| • Idle | | 0.290 | 0.59 | W |
| • 25% Transmitter Duty Cycle | | 0.590 | 0.92 | W |
| • 50% Transmitter Duty Cycle | | 0.890 | 1.36 | W |
| • 100% Transmitter Duty Cycle | | 1.490 | 2.16 | W |
| ■ BU-63825/925X3/X6 | | | | |
| • Idle | | | 0.28 | W |
| • 25% Transmitter Duty Cycle | | | 0.51 | W |
| • 50% Transmitter Duty Cycle | | | 0.75 | W |
| • 100% Transmitter Duty Cycle | | | 1.22 | W |

| TABLE 1. SP'ACE II SERIES SPECS (CONT) | | | | |
|---|---|---|---|---|
| **PARAMETER** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **CLOCK INPUT** | | | | |
| Frequency | | | | |
| ■ Nominal Value (programmable) | | | | |
| • Default Mode | | 16.0 | | MHz |
| • Option | | 12.0 | | MHz |
| ■ Long Term Tolerance | | | | |
| • 1553A Compliance | -0.01 | | 0.01 | % |
| • 1553B Compliance | -0.10 | | 0.10 | % |
| ■ Short Term Tolerance,1 second | | | | |
| • 1553A Compliance | -.001 | | 0.001 | % |
| • 1553B Compliance | -0.01 | | 0.01 | % |
| ■ Duty Cycle | 40 | | 60 | % |
| **1553 MESSAGE TIMING** | | | | |
| Completion of CPU Write (BC Start-to-Start of Next Message) | | 2.5 | | µs |
| BC Intermessage Gap (Note 8) | | 9.5 | | µs |
| BC/RT/MT Response Timeout (Note 9) | | | | |
| ■ 18.5 nominal | 17.5 | 18.5 | 19.5 | µs |
| ■ 22.5 nominal | 21.5 | 22.5 | 23.5 | µs |
| ■ 50.5 nominal | 49.5 | 50.5 | 51.5 | µs |
| ■ 128.0 nominal | 128 | 129.5 | 131 | µs |
| Transmitter Watchdog Timeout | | 668 | | µs |
| RT Response Time (Note 11) | 4 | | 7 | µs |
| **THERMAL** | | | | |
| Thermal Resistance, Junction-to-Case, | | | | |
| Hottest Die ($\theta_{JC}$) | | | | |
| ■ BU-63825/925X0 | | 7.10 | | °C/W |
| ■ BU-63825/925X1 | | 7.82 | | °C/W |
| ■ BU-63825/925X2 | | 7.82 | | °C/W |
| ■ BU-63825/925X3/X6 | | 12 | | °C/W |
| Operating Junction Temperature | -55 | | 150 | °C |
| Storage Temperature | -65 | | 150 | °C |
| Lead Temperature (soldering, 10 sec.) | | | +300 | °C |
| **PHYSICAL CHARACTERISTICS** | | | | |
| Size | | | | |
| ■ 70-pin DIP, Flat Pack, Gull Lead | 1.9 X 1.0 X 0.215 (48.26 x 25.4 x 5.46) | | | in. (mm) |
| Weight | | | | |
| ■ 70-pin DIP, Flat Pack, Gull Lead | 0.6 (17) | | | oz (g) |

TABLE 1 NOTES: Notes 1 through 6 are applicable to the Receiver Differential Resistance and Differential Capacitance specifications:
(1) Specifications include both transmitter and receiver (tied together internally).
(2) Measurement of impedance is directly between pins TX/RX A(B) and TX/RX A(B) of the Sp'ACE II Series hybrid.
(3) Assuming the connection of all power and ground inputs to the hybrid.
(4) The specifications are applicable for both unpowered and powered conditions.
(5) The specifications assume a 2 volt rms balanced, differential, sinusoidal input. The applicable frequency range is 75 kHz to 1 MHz.
(6) Minimum resistance and maximum capacitance parameters are guaranteed, but not tested, over the operating range.
(7) Assumes a common mode voltage within the frequency range of dc to 2 MHz, applied to pins of the isolation transformer on the stub side (either direct or transformer coupled), referenced to hybrid ground. Use a DDC recommended transformer or other transformer that provides an equivalent minimum CMRR.
(8) Typical value for minimum intermessage gap time. Under software control, may be lengthened to (65,535 µs minus message time), in increments of 1 µs.

TABLE 1 NOTES (cont)
(9) Software programmable (4 options). Includes RT-to-RT Timeout (Mid-Parity of Transmit Command to Mid-Sync of Transmitting RT Status).
(10) For both +5 V logic and transceiver. +5 V for channels A and B.
(11) Measured from mid-parity crossing of Command Word to mid-sync crossing of RT's Status Word.
(12) MSTCLR, CLOCK_IN, and STRBD are CMOS inputs with hysteresis. Remainder are TTL.
(13) Minus sign indicates direction of current flow.

## INTRODUCTION

DDC's Sp'ACE II series of integrated BC/RT/MT hybrids provide a complete, flexible interface between a microprocessor and a MIL-STD-1553A, B Notice 2, McAir, or STANAG 3838 bus, implementing Bus Controller, Remote Terminal (RT) and Monitor Terminal (MT) modes. Packaged in a single 1.9 square inch 70-pin DIP, surface mountable Flat Pack or Gull Lead, the Sp'ACE II series contains dual low-power transceivers and encoder/decoders, complete BC/RT/MT multiprotocol logic, memory management and interrupt logic, 16K X 16 of shared static RAM and a direct, buffered interface to a host processor bus.

The BU-63825 contains internal address latches and bidirectional data buffers to provide a direct interface to a host processor bus. The BU-63825 may be interfaced directly to both 16-bit and 8-bit microprocessors (Please see Appendix G in the ACE User's Guide for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode) in a buffered shared RAM configuration. In addition, the Sp'ACE II may connect to a 16-bit processor bus via a Direct Memory Access (DMA) interface. The BU-63825 includes 16K words of buffered RAM. Alternatively, the Sp'ACE II may be interfaced to as much as 64k words of external RAM in either the shared RAM or DMA configurations.

The Sp'ACE II RT mode is multiprotocol, supporting MIL-STD-1553A, MIL-STD-1553B Notice 2, and STANAG 3838 (including EFAbus).

The memory management scheme for RT mode provides an option for separation of broadcast data, in compliance with 1553B Notice 2. Both double buffer and circular buffer options are programmable by subaddress. These features serve to ensure data consistency and to off-load the host processor for bulk data transfer applications.

The Sp'ACE II series implements three monitor modes: a word monitor, a selective message monitor, and a combined RT/selective monitor.

Other features include options for automatic retries and programmable intermessage gap for BC mode, an internal Time Tag

Register, an Interrupt Status Register and internal command illegalization for RT mode.

## FUNCTIONAL OVERVIEW

### *TRANSCEIVERS*

For the +5 V and -15 V/-12 V front end, the BU-63825X1(X2) uses low-power bipolar analog monolithic and thin-film hybrid technology. The transceiver requires +5 V and -15 V (-12 V) only (requiring no +15 V/+12 V) and includes voltage source transmitters. The BU-63825X3(X6) utilizes low-power BiCMOS analog monolithic and thin film hybrid technology as well but requires +5V only. The voltage source transmitters provide superior line driving capability for long cables and heavy amounts of bus loading.

The receiver sections of the BU-63825 are fully compliant with MIL-STD-1553B in terms of front end overvoltage protection, threshold, common mode rejection, and word error rate. In addition, the receiver filters have been designed for optimal operation with the M-Rad chip's Manchester II decoders.

### *M-RAD DIGITAL MONOLITHIC*

The M-Rad digital monolithic represents the cornerstone element of the BU-63825 Sp'ACE II family of terminals. The M-Rad chip is actually a radiation hardened version of DDC's M' (M-prime) monolithic which is the key building block behind DDC's non-radiation hardened BU-61580 ACE series of terminals. As such, the M-Rad possesses all the enhanced hardware and software features which have made the BU-61580 ACE the industry standard 1553 interface component.

The M-Rad chip consists of a dual encoder/decoder; complete protocol for Bus Controller (BC), 1553A/B/McAir Remote Terminal (RT), and Monitor (MT) modes; memory management and interrupt logic; a flexible, buffered interface to a host processor bus and optional external RAM. Reference the region within the dotted line of FIGURE 1. Besides realizing all the protocol, memory management, and interface functions of the earlier AIM-HY series, the M-Rad chip includes a large number of enhancements to facilitate hardware and software design, and to further off-load the 1553 terminal's host processor.

### *DECODERS*

The default mode of operation for the BU-63825 BC/RT/MT requires a 16 MHz clock input. If needed, a software programmable option allows the device to be operated from a 12 MHz clock input. Most current 1553 decoders sample using a 10 MHz or 12 MHz clock. In the 16 MHz mode (or 12 MHz), the decoders sample using both clock edges; this provides a sampling rate of 32 MHz or 24 MHz. The faster sampling rate for the M-Rad's Manchester II decoders provides superior performance in terms of bit error rate and zero-crossing distortion tolerance.

For interfacing to fiber optic transceivers for MIL-STD-1773 applications, a transceiverless version of the Sp'ACE II can be used. These versions provide a register programmable option for a direct interface to the single-ended outputs of a fiber optic receiver. No external logic is needed.

### *TIME TAGGING*

The Sp'ACE II includes an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 µs per LSB. Also, the Time Tag Register may be clocked from an external oscillator. Another option allows software controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register. For each message processed, the value of the Time Tag register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for both BC and RT modes.

Additional provided options will: clear the Time Tag Register following a Synchronize (without data) mode command or load the Time Tag Register following a Synchronize (with data) mode command; enable an interrupt request and a bit setting in the Interrupt Status Register when the Time Tag Register rolls over from FFFF to 0000. Assuming the Time Tag Register is not loaded or reset, this will occur at approximately 4 second time intervals, for 64 µs/LSB resolution, down to 131 ms intervals, for 2 µs/LSB resolution.

Another programmable option for RT mode is the automatic clearing of the Service Request Status Word bit following the BU-63825's response to a Transmit Vector Word mode command.

### *INTERRUPTS*

The Sp'ACE II series components provide many programmable options for interrupt generation and handling. The interrupt output pin $\overline{\text{INT}}$ has three software programmable modes of operation: a pulse, a level output cleared under software control, or a level output automatically cleared following a read of the Interrupt Status Register. Individual interrupts are enabled by the Interrupt Mask Register. The host processor may easily determine the cause of the interrupt by using the Interrupt Status Register. The Interrupt Status Register provides the current state of the interrupt conditions. The Interrupt Status Register may be updated in two ways. In the standard interrupt handling mode, a particular bit in the Interrupt Status Register will be updated only if the condition exists and the corresponding bit in the Interrupt Mask Register is enabled. In the enhanced interrupt handling mode, a particular bit in the Interrupt Status Register will be updated if the condition exists regardless of the contents of the corresponding Interrupt Mask Register bit. In any case, the respective Interrupt Mask Register bit enables an interrupt for a particular condition.

### *RADIATION TOLERANCE*

The BU-63825 combines analog transceivers with digital CMOS logic and RAM fabricated to provide radiation survivability. To summarize,

• BU-63825(925)X0, X1, X2 utilizes BiPolar analog transceivers and has a total gamma dose immuntity of $1x10^6$ Rad and a LET threshold of 63 MeV-cm²/mg, providing a soft error rate of $2.56x10^{-5}$ errors/device-day.

• BU-63825(925)X3, X6 utilizes BiCMOS analog transceivers and has a total gamma dose immunity of $1x10^5$ Rad and a LET threshold of 63 MeV-cm²/mg, providing a soft error rate of $2.56x10^{-5}$ errors/device-day.

The digital portions of the hybrids are inherently immune to Latchup. The digital logic is implemented in a Honeywell RICMOS™ IV SOI Gate Array (HX2000 Series) and the RAM is implemented utilizing a radiation-hardened process (Honeywell HX6256).

### *HIGH-REL SCREENING*

DDC is committed to the design and manufacture of hybrids and transformers with enhanced processing and screening for spaceborne applications and other systems requiring the highest levels of reliability. These platforms include launch vehicles, satellites and the International Space Station.

DDC has tailored its design methodologies to optimize the fabrication of space level hybrids. The intent of the design guidelines is to minimize the number of die and wirebonds, minimize the number of substrate layers, and maximize the space between components. DDC's space grade products combine analog bipolar/BiCMOS and radiation hardened Honeywell RICMOS™ IV SOI Gate Array (HX2000 Series) technology to provide various levels of radiation tolerance.

The BU-63825 is packaged in a 70-pin ceramic package. In contrast to Kovar (metal) packages, the use of ceramic eliminates the hermeticity problems associated with the glass beads used in the metal packages. In addition, ceramic packages provide more rigid leads, better thermal properties, easier wirebonding, and lower weight.

The production of the space level hybrids can entail enhanced screening steps beyond DDC's standard flow. This includes Condition A visual inspection, SEM analysis, and element evaluation for all integrated circuit die. For the hybrids, available screening includes Particle Impact Noise Detection (PIND), 320-hour burn-in , 100% non-destructive wirebond pull, X-ray analysis, as well as Destructive Physical Analysis (DPA) testing, extended temperature cycling for QCI testing, and a moisture content limit of 5000 PPM. TABLE 3 summarizes the procurement screening, element evaluation, and hybrid screening used in the production of the BU-63825.

**TABLE 2. SP'ACE II SERIES RADIATION SPECIFICATIONS***

| PART NUMBER | TOTAL DOSE | SINGLE EVENT UPSET (NOTE 1) | SINGLE EVENT LATCHUP |
|---|---|---|---|
| BU-63825(925)X0<br>BU-63825(925)X1<br>BU-63825(925)X2 | $1 \times 10^6$ Rad | $2.56 \times 10^{-5}$ errors/device-day, $T_A$=25°C, Adams 90% worst case environment | Immune |
| BU-63825(925)X3<br>BU-63825(925)X6 | $1 \times 10^5$ Rad | $2.56 \times 10^{-5}$ errors/device-day, $T_A$=25°C, Adams 90% worst case environment | Immune |

*Radiation parameters specified on this data sheet are derived from initial qualification testing by *DDC* and published data from *ASIC* manufacturers. These devices have not been evaluated for compliance to the *RHA* requirements stipulated in MIL-PRF-38534, *Appendix G*.

Table 2 Notes:
1. Single Event Upset (SEU) characteristics analyzed on digital portions of BU-63825(925) design.

**TABLE 3. HIGH RELIABILITY SCREENING OPTIONS**

| ELEMENT EVALUATION | METHOD |
|---|---|
| Visual Inspection:<br>Integrated Circuits<br>Transistors & Diodes<br>Passive Components | <br>MIL-STD-883, Method 2010 Condition A<br>MIL-STD-750, Method 2072 and 2073<br>MIL-STD-883, Method 2032 Class S |
| SEM Analysis for Integrated Circuits | MIL-STD-883, Method 2018 |
| Element Evaluation:<br>Visual,<br>Electrical,<br>Wire Bondability,<br>24-Hour Stabilization Bake,<br>10 Temperature Cycles<br>3000 g's constant acceleration<br>240-Hour Powered Burn-In and 1000-Hour Life Test<br>(Burn-In and 1000-Hour Life Test Are Only Required For Active Components.) | MIL-PRF-38534 |
| **ASSEMBLY & TEST** | |
| Particle Impact Noise Detection (PIND) | MIL-STD-883, Method 2020 Condition A |
| 320-Hour Burn-In (available on this device) | MIL-STD-883, Method 1015 |
| 100% Non-Destructive Wirebond Pull (available on this device) | MIL-STD-883, Method 2023 |
| Radiographic (X-Ray) Analysis | MIL-STD-883, Method 2012 |
| **QCI TESTING** | |
| Extended Temperature Cycling:<br>20 Cycles Including Radiographic (X-Ray) Testing | MIL-STD-883, Method 1010 Condition C and MIL-STD-883, Method 2012 |
| Moisture Content Limit of 5000 PPM | MIL-STD-883, Method 1018 |

### *ADDRESSING, INTERNAL REGISTERS, AND MEMORY MANAGEMENT*

The software interface of the BU-63825 to the host processor consists of 17 internal operational registers for normal operation, an additional 8 test registers, plus 64K X 16 of shared memory address space. The BU-63825's 16K X 16 of internal RAM resides in this address space. Reference TABLE 4.

Definition of the address mapping and accessibility for the Sp'ACE II's 17 nontest registers, and the test registers, is as follows:

#### *Interrupt Mask Register:*

Used to enable and disable interrupt requests for various conditions.

#### *Configuration Registers #1 and #2:*

Used to select the BU-63825's mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-on-Error, RT Memory Management mode selection, and control of the Time Tag operation.

#### *Start/Reset Register:*

Used for "command" type functions, such as software reset, BC/MT Start, Interrupt Reset, Time Tag Reset, and Time Tag Register Test. The Start/Reset Register includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

#### *BC/RT Command Stack Pointer Register:*

Allows the host CPU to determine the pointer location for the current or most recent message when the BU-63825 is in BC or RT modes.

#### *BC Control Word/RT Subaddress Control Word Register:*

In BC mode, allows host access to the current or most recent BC Control Word. The BC Control Word contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. In RT mode, this register allows host access to the current or most recent Subaddress Control Word. The Subaddress Control Word is used to select the memory management scheme and enable interrupts for the current message. The read/write accessibility can be used as an aid for testing the Sp'ACE II hybrid.

**TABLE 4. ADDRESS MAPPING**

| ADDRESS LINES | | | | | | REGISTER DESCRIPTION/ACCESSIBILITY |
|---|---|---|---|---|---|---|
| HEX | A4 | A3 | A2 | A1 | A0 | |
| 00 | 0 | 0 | 0 | 0 | 0 | Interrupt Mask Register (RD/WR) |
| 01 | 0 | 0 | 0 | 0 | 1 | Configuration Register #1 (RD/WR) |
| 02 | 0 | 0 | 0 | 1 | 0 | Configuration Register #2 (RD/WR) |
| 03 | 0 | 0 | 0 | 1 | 1 | Start/Reset Register (WR) |
| 03 | 0 | 0 | 0 | 1 | 1 | BC/RT Command Stack Pointer Register (RD) |
| 04 | 0 | 0 | 1 | 0 | 0 | BC Control Word/RT Subaddress Control Word Register (RD/WR) |
| 05 | 0 | 0 | 1 | 0 | 1 | Time Tag Register (RD/WR) |
| 06 | 0 | 0 | 1 | 1 | 0 | Interrupt Status Register (RD) |
| 07 | 0 | 0 | 1 | 1 | 1 | Configuration Register #3 (RD/WR) |
| 08 | 0 | 1 | 0 | 0 | 0 | Configuration Register #4 (RD/WR) |
| 09 | 0 | 1 | 0 | 0 | 1 | Configuration Register #5 (RD/WR) |
| 0A | 0 | 1 | 0 | 1 | 0 | Data Stack Address Register (RD/WR) |
| 0B | 0 | 1 | 0 | 1 | 1 | BC Frame Time Remaining Register (RD/WR) |
| 0C | 0 | 1 | 1 | 0 | 0 | BC Time Remaining to Next Message Register (RD/WR) |
| 0D | 0 | 1 | 1 | 0 | 1 | BC Frame Time/RT Last Command /MT Trigger Word Register (RD/WR) |
| 0E | 0 | 1 | 1 | 1 | 0 | RT Status Word Register (RD) |
| 0F | 0 | 1 | 1 | 1 | 1 | RT BIT Word Register (RD) |
| 10 | 1 | 0 | 0 | 0 | 0 | Test Mode Register 0 |
| • | | | | | | |
| • | | | | | | |
| 17 | 1 | 0 | 1 | 1 | 1 | Test Mode Register 7 |
| 18 | 1 | 1 | 0 | 0 | 0 | reserved |
| • | | | | | | |
| • | | | | | | |
| 1F | 1 | 1 | 1 | 1 | 1 | reserved |

#### *Time Tag Register:*

Maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. The TAG_CLK input signal also may cause an external oscillator to clock the Time Tag Register. Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of RAM.

*Interrupt Status Register:*

Mirrors the Interrupt Mask Register and contains a Master Interrupt bit. It allows the host processor to determine the cause of an interrupt request by means of a single READ operation.

*Configuration Registers #3, #4, and #5:*

Used to enable many of the BU-63825's advanced features. These include all the enhanced mode features; that is, all the functionality beyond that of the previous generation product, the BUS-61559 Advanced Integrated Mux Hybrid with Enhanced RT Features (AIM-HY'er). For BC mode, the enhanced mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message. For RT mode, the enhanced mode features include the expanded RT Block Status Word, the combined RT/Selective Message Monitor mode, internal wrapping of the RTFAIL output signal (from the M-Rad chip) to the RTFLAG RT Status Word bit, the double buffering scheme for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word. For MT mode, use of the enhanced mode enables use of the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

*Data Stack Address Register:*

Used to point to the current address location in shared RAM used for storing message words (second Command Words, Data Words, RT Status Words) in the Selective Word Monitor mode.

*Frame Time Remaining Register:*

Provides a read only indication of the time remaining in the current BC frame. The resolution of this register is 100µs/LSB.

*Message Time Remaining Register:*

Provides a read only indication of the time remaining before the start of the next message in a BC frame. The resolution of this register is 1 µs/LSB.

**TABLE 5. INTERRUPT MASK REGISTER (READ/WRITE 00H)**

| BIT | DESCRIPTION |
|---|---|
| 15(MSB) | RESERVED |
| 14 | RAM PARITY ERROR |
| 13 | BC/RT TRANSMITTER TIMEOUT |
| 12 | BC/RT COMMAND STACK ROLLOVER |
| 11 | MT COMMAND STACK ROLLOVER |
| 10 | MT DATA STACK ROLLOVER |
| 9 | HS FAIL |
| 8 | BC RETRY |
| 7 | RT ADDRESS PARITY ERROR |
| 6 | TIME TAG ROLLOVER |
| 5 | RT CIRCULAR BUFFER ROLLOVER |
| 4 | BC/RT SELECTED MESSAGE |
| 3 | BC END OF FRAME |
| 2 | FORMAT ERROR |
| 1 | BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER |
| 0(LSB) | END OF MESSAGE |

*BC Frame/RT Last Command/MT Trigger Word Register:*

In BC mode, it programs the BC frame time, for use in the frame auto-repeat mode. The resolution of this register is 100 µs/LSB, with a range of 6.55 seconds; in RT mode, this register stores the current (or most previous) 1553 Command Word processed by the Sp'ACE II RT; in the Word Monitor mode, this register specifies a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

*Status Word Register and BIT Word Registers:*

Provide read-only indications of the BU-63825's RT Status and BIT Words.

*Test Mode Registers 0-7:*

These registers may be used to facilitate production or maintenance testing of the Sp'ACE II and systems incorporating the Sp'ACE II hybrid.

| TABLE 6. CONFIGURATION REGISTER #1 (READ/WRITE 01H) | | | | |
|---|---|---|---|---|
| BIT | BC FUNCTION (BITS 11-0 ENHANCED MODE ONLY) | RT WITHOUT ALTERNATE STATUS | RT WITH ALTERNATE STATUS | MONITOR FUNCTION |
| 15 (MSB) | RT/$\overline{\text{BC-MT}}$ (logic 0) | (logic 1) | (logic 1) | (logic 0) |
| 14 | MT/$\overline{\text{BC-RT}}$ (logic 0) | (logic 0) | (logic 0) | (logic 1) |
| 13 | CURRENT AREA B/$\overline{\text{A}}$ | CURRENT AREA B/$\overline{\text{A}}$ | CURRENT AREA B/$\overline{\text{A}}$ | CURRENT AREA B/$\overline{\text{A}}$ |
| 12 | MESSAGE STOP-ON-ERROR | MESSAGE MONITOR ENABLED (MMT) | MESSAGE MONITOR ENABLED (MMT) | MESSAGE MONITOR ENABLED (MMT) |
| 11 | FRAME STOP-ON-ERROR | $\overline{\text{DYNAMIC BUS CONTROL ACCEPTANCE}}$ | S10 | TRIGGER ENABLED WORD |
| 10 | STATUS SET STOP-ON-MESSAGE | $\overline{\text{BUSY}}$ | S09 | START-ON-TRIGGER |
| 9 | STATUS SET STOP-ON-FRAME | $\overline{\text{SERVICE REQUEST}}$ | S08 | STOP-ON-TRIGGER |
| 8 | FRAME AUTO-REPEAT | $\overline{\text{SUBSYSTEM FLAG}}$ | S07 | NOT USED |
| 7 | EXTERNAL TRIGGER ENABLED | $\overline{\text{RTFLAG}}$ | S06 | EXTERNAL TRIGGER ENABLED |
| 6 | INTERNAL TRIGGER ENABLED | NOT USED | S05 | NOT USED |
| 5 | INTERMESSAGE GAP TIMER ENABLED | NOT USED | S04 | NOT USED |
| 4 | RETRY ENABLED | NOT USED | S03 | NOT USED |
| 3 | DOUBLED/$\overline{\text{SINGLE}}$ RETRY | NOT USED | S02 | NOT USED |
| 2 | BC ENABLED (Read Only) | NOT USED | S01 | MONITOR ENABLED (Read Only) |
| 1 | BC FRAME IN PROGRESS (Read Only) | NOT USED | S00 | MONITOR TRIGGERED (Read Only) |
| 0 (LSB) | BC MESSAGE IN PROGRESS (Read Only) | RT MESSAGE IN PROGRESS (Read Only) | RT MESSAGE IN PROGRESS (Read Only) | MONITOR ACTIVE (Read Only) |

| TABLE 7. CONFIGURATION REGISTER #2 (READ/WRITE 02H) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | ENHANCED INTERRUPTS |
| 14 | LOGIC “0” |
| 13 | BUSY LOOKUP TABLE ENABLE |
| 12 | RX SA DOUBLE BUFFER ENABLE |
| 11 | OVERWRITE INVALID DATA |
| 10 | 256-WORD BOUNDARY DISABLE |
| 9 | TIME TAG RESOLUTION 2 (TTR2) |
| 8 | TIME TAG RESOLUTION 1 (TTR1) |
| 7 | TIME TAG RESOLUTION 0 (TTR0) |
| 6 | CLEAR TIME TAG ON SYNCHRONIZE |
| 5 | LOAD TIME TAG ON SYNCHRONIZE |
| 4 | INTERRUPT STATUS AUTO CLEAR |
| 3 | LEVEL/PULSE INTERRUPT REQUEST |
| 2 | CLEAR SERVICE REQUEST |
| 1 | ENHANCED RT MEMORY MANAGEMENT |
| 0(LSB) | SEPARATE BROADCAST DATA |

| TABLE 8. START/RESET REGISTER (WRITE 03H) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | RESERVED |
| • | • |
| • | • |
| • | • |
| 7 | RESERVED |
| 6 | BC/MT STOP-ON-MESSAGE |
| 5 | BC STOP-ON-FRAME |
| 4 | TIME TAG TEST CLOCK |
| 3 | TIME TAG RESET |
| 2 | INTERRUPT RESET |
| 1 | BC/MT START |
| 0(LSB) | RESET |

| TABLE 9. BC/RT COMMAND STACK POINTER REG. (READ 03H) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | COMMAND STACK POINTER 15 |
| • | • |
| • | • |
| • | • |
| 0(LSB) | COMMAND STACK POINTER 0 |

| TABLE 10. BC CONTROL WORD REGISTER (READ/WRITE 04H) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | RESERVED |
| 14 | M.E. MASK |
| 13 | SERVICE REQUEST BIT MASK |
| 12 | SUBSYS BUSY BIT MASK |
| 11 | SUBSYS FLAG BIT MASK |
| 10 | TERMINAL FLAG BIT MASK |
| 9 | RESERVED BITS MASK |
| 8 | RETRY ENABLED |
| 7 | BUS CHANNEL A/B |
| 6 | OFF LINE SELF TEST |
| 5 | MASK BROADCAST BIT |
| 4 | EOM INTERRUPT ENABLE |
| 3 | 1553A/B SELECT |
| 2 | MODE CODE FORMAT |
| 1 | BROADCAST FORMAT |
| 0(LSB) | RT-RT FORMAT |

| TABLE 11. RT SUBADDRESS CONTROL WORD (READ/WRITE 04H) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | RX: DOUBLE BUFFER ENABLE |
| 14 | TX: EOM INT |
| 13 | TX: CIRC BUF INT |
| 12 | TX: MEMORY MANAGEMENT 2 (MM2) |
| 11 | TX: MEMORY MANAGEMENT 1 (MM1) |
| 10 | TX: MEMORY MANAGEMENT 0 (MM0) |
| 9 | RX: EOM INT |
| 8 | RX: CIRC BUF INT |
| 7 | RX: MEMORY MANAGEMENT 2 (MM2) |
| 6 | RX: MEMORY MANAGEMENT 1 (MM1) |
| 5 | RX: MEMORY MANAGEMENT 0 (MM0) |
| 4 | BCST: EOM INT |
| 3 | BCST: CIRC BUF INT |
| 2 | BCST: MEMORY MANAGEMENT 2 (MM2) |
| 1 | BCST: MEMORY MANAGEMENT 1 (MM1) |
| 0(LSB) | BCST: MEMORY MANAGEMENT 0 (MM0) |

| TABLE 12. TIME TAG REGISTER (READ/WRITE 05H) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | TIME TAG 15 |
| • | • |
| • | • |
| • | • |
| 0(LSB) | TIME TAG 0 |

| TABLE 13. INTERRUPT STATUS REGISTER (READ 06H) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | MASTER INTERRUPT |
| 14 | RAM PARITY ERROR |
| 13 | BC/RT TRANSMITTER TIMEOUT |
| 12 | BC/RT COMMAND STACK ROLLOVER |
| 11 | MT COMMAND STACK ROLLOVER |
| 10 | MT DATA STACK ROLLOVER |
| 9 | HS FAIL |
| 8 | BC RETRY |
| 7 | RT ADDRESS PARITY ERROR |
| 6 | TIME TAG ROLLOVER |
| 5 | RT CIRCULAR BUFFER ROLLOVER |
| 4 | BC/RT SELECTIVE MESSAGE |
| 3 | BC END OF FRAME |
| 2 | FORMAT ERROR |
| 1 | BC STATUS SET/RT MODE CODE /MT PATTERN TRIGGER |
| 0(LSB) | END OF MESSAGE |

| TABLE 14. CONFIGURATION REGISTER #3 (READ/WRITE 07H) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | ENHANCED MODE ENABLE |
| 14 | BC/RT COMMAND STACK SIZE 1 |
| 13 | BC/RT COMMAND STACK SIZE 0 |
| 12 | MT COMMAND STACK SIZE 1 |
| 11 | MT COMMAND STACK SIZE 0 |
| 10 | MT DATA STACK SIZE 2 |
| 9 | MT DATA STACK SIZE 1 |
| 8 | MT DATA STACK SIZE 0 |
| 7 | ILLEGALIZATION DISABLED |
| 6 | OVERRIDE MODE T/R ERROR |
| 5 | ALTERNATE STATUS WORD ENABLE |
| 4 | ILLEGAL RX TRANSFER DISABLE |
| 3 | BUSY RX TRANSFER DISABLE |
| 2 | RTFAIL-FLAG WRAP ENABLE |
| 1 | 1553A MODE CODES ENABLE |
| 0(LSB) | ENHANCED MODE CODE HANDLING |

| TABLE 15. CONFIGURATION REGISTER #4 (READ/WRITE 08H) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | EXTERNAL BIT WORD ENABLE |
| 14 | INHIBIT BIT WORD IF BUSY |
| 13 | MODE COMMAND OVERRIDE BUSY |
| 12 | EXPANDED BC CONTROL WORD ENABLE |
| 11 | BROADCAST MASK ENABLE/$\overline{\text{XOR}}$ |
| 10 | RETRY IF -A AND M.E. |
| 9 | RETRY IF STATUS SET |
| 8 | 1ST RETRY ALT/$\overline{\text{SAME}}$ BUS |
| 7 | 2ND RETRY ALT/$\overline{\text{SAME}}$ BUS |
| 6 | VALID M.E./NO DATA |
| 5 | VALID BUSY/NO DATA |
| 4 | MT TAG GAP OPTION |
| 3 | LATCH RT ADDRESS WITH CONFIG #5 |
| 2 | TEST MODE 2 |
| 1 | TEST MODE 1 |
| 0(LSB) | TEST MODE 0 |

| TABLE 16. CONFIGURATION REGISTER #5 (READ/WRITE 09H) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | 12MHZ CLOCK SELECT |
| 14 | SINGLE ENDED SELECT |
| 13 | EXTERNAL TX INHIBIT A, read only |
| 12 | EXTERNAL TX INHIBIT B, read only |
| 11 | EXPANDED CROSSING ENABLED |
| 10 | RESPONSE TIMEOUT SELECT 1 |
| 9 | RESPONSE TIMEOUT SELECT 0 |
| 8 | GAP CHECK ENABLED |
| 7 | BROADCAST DISABLED |
| 6 | RT ADDRESS LATCH/$\overline{\text{TRANSPARENT}}$ (see Note) |
| 5 | RT ADDRESS 4 |
| 4 | RT ADDRESS 3 |
| 3 | RT ADDRESS 2 |
| 2 | RT ADDRESS 1 |
| 1 | RT ADDRESS 0 |
| 0(LSB) | RT ADDRESS PARITY |

Note: Read only, logic “0” for 63825, logic “1” for 63925.

| TABLE 17. MONITOR DATA STACK ADDRESS REGISTER (READ/WRITE 0AH) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | MONITOR DATA STACK ADDRESS 15 |
| • | • |
| • | • |
| • | • |
| 0(LSB) | MONITOR DATA STACK ADDRESS 0 |

| TABLE 18. BC FRAME TIME REMAINING REGISTER (READ/WRITE 0BH) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | BC FRAME TIME REMAINING 15 |
| • | • |
| • | • |
| • | • |
| 0(LSB) | BC FRAME TIME REMAINING 0 |

Note: resolution 100 µs per LSB

| TABLE 19. BC MESSAGE TIME REMAINING REGISTER (READ/WRITE 0CH) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | BC MESSAGE TIME REMAINING 15 |
| • | • |
| • | • |
| • | • |
| 0(LSB) | BC MESSAGE TIME REMAINING 0 |

Note: resolution = 1 µs per LSB

| TABLE 20. BC FRAME TIME/RT LAST COMMAND/ TRIGGER REGISTER (READ/WRITE 0DH) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | BIT 15 |
| • | • |
| • | • |
| • | • |
| 0(LSB) | BIT 0 |

| TABLE 21. RT STATUS WORD REGISTER (READ/WRITE 0EH) | |
|---|---|
| BIT | DESCRIPTION |
| 15(MSB) | LOGIC “0” |
| 14 | LOGIC “0” |
| 13 | LOGIC “0” |
| 12 | LOGIC “0” |
| 11 | LOGIC “0” |
| 10 | MESSAGE ERROR |
| 9 | INSTRUMENTATION |
| 8 | SERVICE REQUEST |
| 7 | RESERVED |
| 6 | RESERVED |
| 5 | RESERVED |
| 4 | BROADCAST COMMAND RECEIVED |
| 3 | BUSY |
| 2 | SUBSYSTEM FLAG |
| 1 | DYNAMIC BUS CONTROL ACCEPT |
| 0(LSB) | TERMINAL FLAG |

## TABLE 22. RT BIT WORD REGISTER (WRITE 0FH)

| BIT | DESCRIPTION |
|---|---|
| 15(MSB) | TRANSMITTER TIMEOUT |
| 14 | LOOP TEST FAILURE B |
| 13 | LOOP TEST FAILURE A |
| 12 | HANDSHAKE FAILURE |
| 11 | TRANSMITTER SHUTDOWN B |
| 10 | TRANSMITTER SHUTDOWN A |
| 9 | TERMINAL FLAG INHIBITED |
| 8 | CHANNEL B/$\overline{A}$ |
| 7 | HIGH WORD COUNT |
| 6 | LOW WORD COUNT |
| 5 | INCORRECT SYNC RECEIVED |
| 4 | PARITY/MANCHESTER ERROR RECEIVED |
| 3 | RT-RT GAP/SYNC/ADDRESS ERROR |
| 2 | RT-RT NO RESPONSE ERROR |
| 1 | RT-RT 2ND COMMAND WORD ERROR |
| 0(LSB) | COMMAND WORD CONTENTS ERROR |

**NOTE:**
**TABLES 23 TO 26 ARE NOT REGISTERS, BUT THEY ARE WORDS STORED IN RAM.**

## TABLE 23. BC MODE BLOCK STATUS WORD

| BIT | DESCRIPTION |
|---|---|
| 15(MSB) | EOM |
| 14 | SOM |
| 13 | CHANNEL B/$\overline{A}$ |
| 12 | ERROR FLAG |
| 11 | STATUS SET |
| 10 | FORMAT ERROR |
| 9 | NO RESPONSE TIMEOUT |
| 8 | LOOP TEST FAIL |
| 7 | MASKED STATUS SET |
| 6 | RETRY COUNT 1 |
| 5 | RETRY COUNT 0 |
| 4 | GOOD DATA BLOCK TRANSFER |
| 3 | WRONG STATUS ADDRESS/NO GAP |
| 2 | WORD COUNT ERROR |
| 1 | INCORRECT SYNC TYPE |
| 0(LSB) | INVALID WORD |

## TABLE 24. RT MODE BLOCK STATUS WORD

| BIT | DESCRIPTION |
|---|---|
| 15(MSB) | EOM |
| 14 | SOM |
| 13 | CHANNEL B/$\overline{A}$ |
| 12 | ERROR FLAG |
| 11 | RT-RT FORMAT |
| 10 | FORMAT ERROR |
| 9 | NO RESPONSE TIMEOUT |
| 8 | LOOP TEST FAIL |
| 7 | DATA STACK ROLLOVER |
| 6 | ILLEGAL COMMAND WORD |
| 5 | WORD COUNT ERROR |
| 4 | INCORRECT SYNC |
| 3 | INVALID WORD |
| 2 | RT-RT GAP/SYNC/ADDRESS ERROR |
| 1 | RT-RT 2ND COMMAND ERROR |
| 0(LSB) | COMMAND WORD CONTENTS ERROR |

## TABLE 25. WORD MONITOR IDENTIFICATION WORD

| BIT | DESCRIPTION |
|---|---|
| 15(MSB) | GAP TIME |
| • | • |
| • | • |
| • | • |
| 8 | GAP TIME |
| 7 | WORD FLAG |
| 6 | $\overline{\text{THIS RT}}$ |
| 5 | $\overline{\text{BROADCAST}}$ |
| 4 | ERROR |
| 3 | COMMAND/$\overline{\text{DATA}}$ |
| 2 | CHANNEL B/$\overline{A}$ |
| 1 | CONTIGUOUS DATA/$\overline{\text{GAP}}$ |
| 0(LSB) | $\overline{\text{MODE CODE}}$ |

## TABLE 26. MESSAGE MONITOR MODE BLOCK STATUS WORD

| BIT | DESCRIPTION |
|---|---|
| 15(MSB) | EOM |
| 14 | SOM |
| 13 | CHANNEL B/$\overline{A}$ |
| 12 | ERROR FLAG |
| 11 | RT-RT TRANSFER |
| 10 | FORMAT ERROR |
| 9 | NO RESPONSE TIMEOUT |
| 8 | GOOD DATA BLOCK TRANSFER |
| 7 | DATA STACK ROLLOVER |
| 6 | RESERVED |
| 5 | WORD COUNT ERROR |
| 4 | INCORRECT SYNC |
| 3 | INVALID WORD |
| 2 | RT-RT GAP/SYNC/ADDRESS ERROR |
| 1 | RT-RT 2ND COMMAND ERROR |
| 0(LSB) | COMMAND WORD CONTENTS ERROR |

## BC CONTROLLER (BC) ARCHITECTURE

The BC protocol of the BU-63825 implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of bits in the BC Control Word and the T/$\overline{R}$ bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The BU-63825's BC response timeout value is programmable with choices of 18, 22, 50, and 130 µs. The longer response timeout values allow for operation over long buses and/or the use of repeaters. FIGURE 2 illustrates BC intermessage gap and frame timing.

The BU-63825 may be programmed to process BC frames of up to 512 messages with no processor intervention. It is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally, using a programmable BC frame timer, or from an external trigger input. The internal BC frame time is programmable up to 6.55 seconds in increments of 100 µs. In addition to BC frame time, intermessage gap time, defined as the start of the current message to the start of the subsequent message, is programmable on an individual message basis. The time between individual successive messages is programmable up to 65.5 ms, in increments of 1 µs.

### BC MEMORY ORGANIZATION

TABLE 27 illustrates a typical memory map for BC mode. It is important to note that the only fixed locations for the BU-63825 in the Standard BC mode are for the two Stack Pointers (address locations 0100 (hex) and 0104) and for the two Message Count locations (0101 and 0105). Enabling the Frame Auto-Repeat mode will reserve four more memory locations for use in the Enhanced BC mode; these locations are for the two Initial Stack Pointers (address locations 102 (hex) and 106) and for the Initial Message Count locations (103 and 107). The user is free to locate the Stack and BC Message Blocks anywhere else within the 64K (16K internal) shared RAM address space.

**TABLE 27. TYPICAL BC MEMORY ORGANIZATION (SHOWN FOR 4K RAM)**

| ADDRESS (HEX) | DESCRIPTION |
|---|---|
| 0000-00FF | Stack A |
| 0100 | Stack Pointer A (fixed location) |
| 0101 | Message Count A (fixed location) |
| 0102 | Initial Stack Pointer A (see note) (Auto-Frame Repeat Mode) |
| 0103 | Initial Message Count A (see note) (Auto-Frame Repeat Mode) |
| 0104 | Stack Pointer B |
| 0105 | Message Count B |
| 0106 | Initial Stack Pointer B (see note) (Auto-Frame Repeat Mode) |
| 0107 | Initial Message Count B (see note) (Auto-Frame Repeat Mode) |
| 0108-012D | Message Block 0 |
| 012E-0153 | Message Block 1 |
| 0154-0179 | Message Block 2 |
| • | • |
| • | • |
| • | • |
| 3EC8-3EED | Message Block 416 |
| 3EEE-3EFF | Not Used |
| 3F00-3FFF | Stack B |

Note: Used only in the Enhanced BC mode with Frame Auto-Repeat enabled.

For simplicity of illustration, assume the allocation of the maximum length of a BC message for each message block in the typical BC memory map of TABLE 27. The maximum size of a BC message block is 38 words, for an RT-to-RT transfer of 32 Data Words (Control + 2 Commands + Loopback + 2 Status Words + 32 Data Words). Note, however, that this example assumes the disabling of the 256-word boundaries.

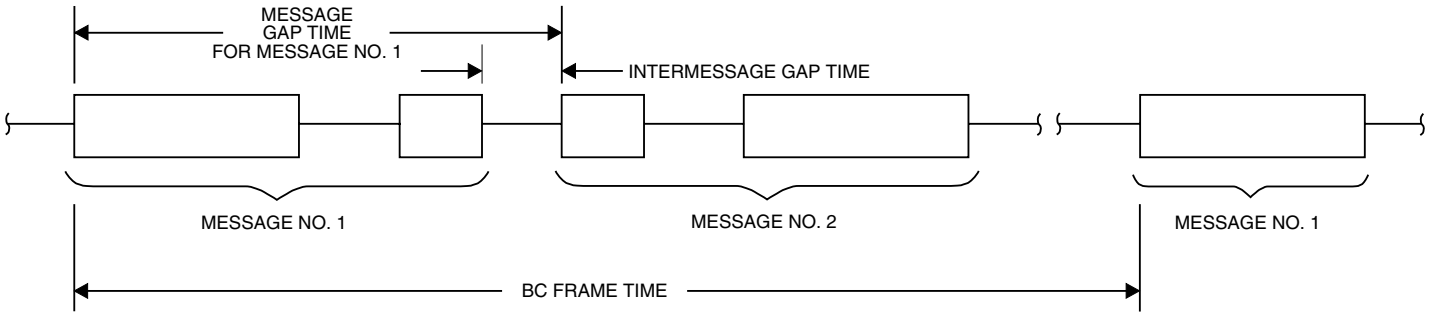



**FIGURE 2. BC MESSAGE GAP AND FRAME TIMING**

## BC MEMORY MANAGEMENT

FIGURE 3 illustrates the BU-63825's BC memory management scheme. One of the BC memory management features is the global double buffering mechanism. This provides for two sets of the various BC mode data structures: Stack Pointer and Message Counter locations, Descriptor Stack areas, and BC message blocks. Bit 13 of Configuration Register #1 selects the current active area. At any point in time, the BU-63825's internal 1553 memory management logic may access only the various data structures within the "active" area. FIGURE 3 delineates the "active" and "inactive" areas by the nonshaded and shaded areas, respectively; however, at any point in time, both the "active" and "nonactive" areas are accessible by the host processor. In most applications, the host processor will access the "nonactive" area, while the 1553 bus processes the "active" area messages.

The BC may be programmed to transmit multimessage frames of up to 512 messages. The number of messages to be processed is programmable by the Active Area Message Count location in the shared RAM, initialized by the host processor. In addition, the host processor must initialize another location, the Active Area Stack Pointer. The Stack Pointer references the four-word message block descriptor in the Stack area of shared RAM for each message to be processed. The BC Stack size is programmable with choices of 256, 512, 1024, and 2048 words.

In the BC Frame Auto-Repeat mode, the Initial Stack Pointer and Initial Message Counter locations must be loaded by the host prior to the processing of the first frame. The single frame mode does not use these two locations

The third and fourth words of the BC block descriptor are the Intermessage Gap Time and the Message Block Address for the respective message. These two memory locations must be written by the host processor prior to the start of message processing. Use of the Intermessage Gap Time is optional. The Block Address pointer specifies the starting location for each message block. The first word of each BC message block is the BC Control Word.

At the start and end of each message, the Block Status and Time Tag Words write to the message block descriptor in the stack. The Block Status Word includes indications of message in process or message completion, bus channel, Status Set, response timeout, retry count, Status address mismatch, loop test (on-line self-test) failure, and other error conditions. TABLE 23 illustrates the bit mapping of the BC Block Status word. The 16-bit Time Tag Word will reflect the current contents of the internal Time Tag Register. This read/writable register, which operates for all three modes, has programmable resolution of from 2 to 64 µs/LSB. In addition, the Time Tag register may be clocked from an external source.

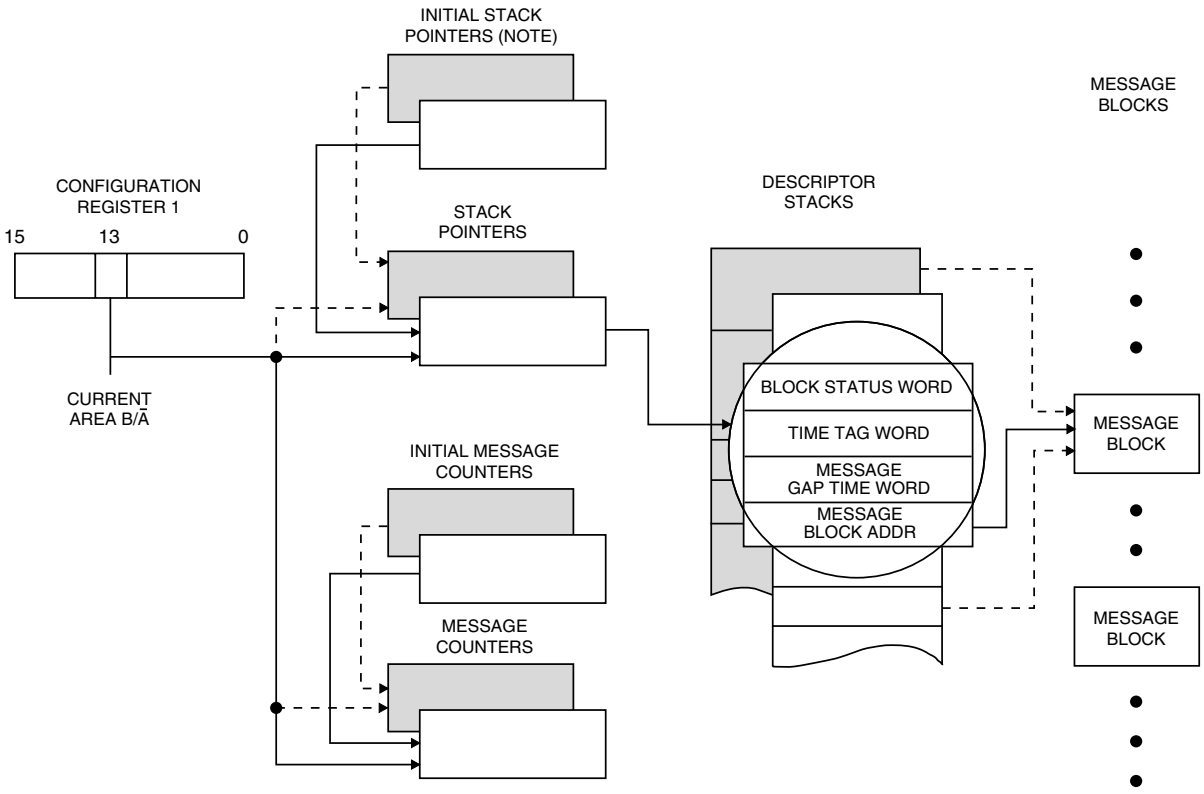



**FIGURE 3. BC MODE MEMORY MANAGEMENT**

### *BC MESSAGE BLOCK FORMATS AND BC CONTROL WORD*

In BC mode, the BU-63825 supports all MIL-STD-1553 message formats. For each 1553 message format, the BU-63825 mandates a specific sequence of words within the BC Message Block. This includes locations for the Control, Command and (transmitted) Data Words that are to be read from RAM by the BC protocol logic. In addition, subsequent contiguous locations must be allocated for storage of received Loopback, RT Status and Data Words. FIGURE 4 illustrates the organization of the BC message blocks for the various MIL-STD-1553 message formats. Note that for all of the message formats, the BC Control Word is located in the first location of the message block.

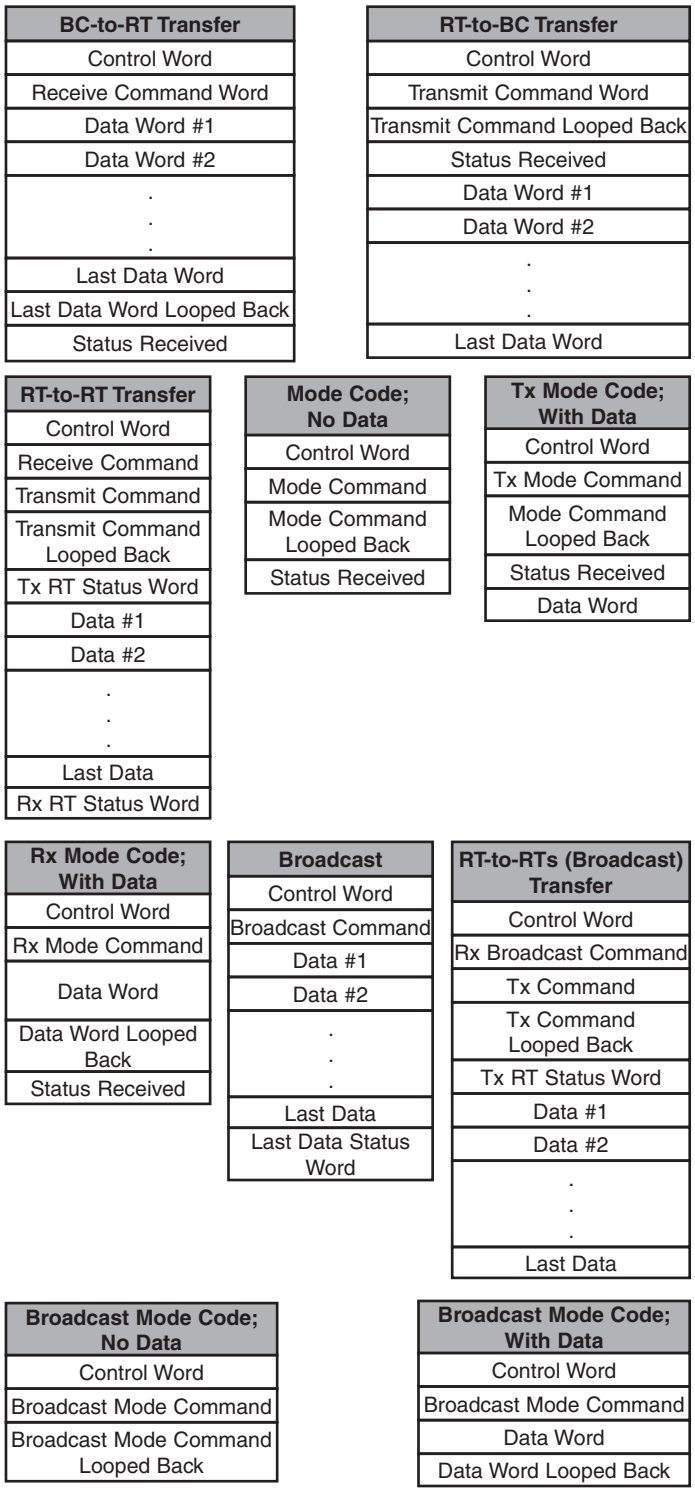



**FIGURE 4. BC MESSAGE BLOCK FORMATS**

The BC Control Word is not transmitted on the 1553 bus. Instead, it contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. The bit mapping and definitions of the BC Control Word are illustrated in TABLE 10.

The BC Control Word is followed by the Command Word to be transmitted, and subsequently by a second Command Word (for an RT-to-RT transfer), followed by Data Words to be transmitted (for Receive commands). The location after the last word to be transmitted is reserved for the Loopback Word. The loopback Word is an on-line self-test feature. The subsequent locations after the Loopback Word are reserved for received Status Words and Data Words (for Transmit commands).

### AUTOMATIC RETRIES

The BU-63825 BC implements automatic message retries. When enabled, retries will occur, following response timeout or format error conditions. As additional options, retries may be enabled when the Message Error Status Word bit is set by a 1553A RT or following a “Status Set” condition. For a failed message, either one or two message retries will occur, and the bus channel (same or alternate) is independently programmable for the first and second retry attempts. Retries may be enabled or disabled on an individual message basis.

### BC INTERRUPTS

BC interrupts may be enabled by the Interrupt Mask Register for Stack Rollover, Retry, End-of-Message (global), End-of-Message (in conjunction with the BC Control Word for individual messages), response timeout, message error, end of BC frame, and Status Set conditions. The definition of “Status Set” is programmable on an individual message basis by means of the BC Control Word. This allows for masking (“care/don’t care”) for the individual RT Status Word bits.

## REMOTE TERMINAL (RT) ARCHITECTURE

The RT protocol design of the BU-63825 represents DDC’s fifth generation implementation of a 1553 RT. One of the salient features of the Sp’ACE II’s RT architecture is its true multiprotocol functionality. This includes programmable options for support of MIL-STD-1553A, the various McAir protocols, and MIL-STD-1553B Notice 2. The BU-63825 RT response time is 2 to 5 µs dead time (4 to 7 µs per 1553B), providing compliance to all the 1553 protocols. Additional multiprotocol features of the BU-63825

include options for full software control of RT Status and Built-in-Test (BIT) words. Alternatively, for 1553B applications, these words may be formulated in real time by the BU-63825 protocol logic.

The BU-63825 RT protocol design implements all the MIL-STD-1553B message formats and dual redundant mode codes. This design is based largely on previous generation products that have passed SEAFAC testing for MIL-STD-1553B compliance. The Sp'ACE II RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. Other key features of the BU-63825 RT include a set of interrupt conditions, internal command illegalization, and programmable busy by subaddress.

## RT MEMORY ORGANIZATION

TABLE 28 illustrates a typical memory map for the Sp'ACE II in RT mode. As in BC mode, the two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. Besides the Stack Pointer, for RT mode there are several other areas of the BU-63825 address space designated as fixed locations. All RT modes of operation require the Area A and Area B Lookup Tables. Also allocated, are several fixed locations for optional features: Command Illegalization Lookup Table, Mode Code Selective Interrupt Table, Mode Code Data Table, and Busy Bit Lookup Table. It should be noted that any unenabled optional fixed locations may be used for general purpose storage (data blocks).

The RT Lookup tables, which provide a mechanism for mapping data blocks for individual Tx/Rx/Bcst-subaddresses to areas in the RAM, occupy address range locations 0140 to 01BF for Area A and 01C0 to 023F for Area B. The RT lookup tables include Subaddress Control Words and the individual Data Block Pointers. If used, address range 0300-03FF will be dedicated as the illegalizing section of RAM. The actual Stack RAM area and the individual data blocks may be located in any of the nonfixed areas in the shared RAM address space.

## RT MEMORY MANAGEMENT

Another salient feature of the Sp'ACE II series products is the flexibility of its RT memory management architecture. The RT architecture allows the memory management scheme for each transmit, receive, or broadcast subaddress to be programmable on a subaddress basis. Also, in compliance with MIL-STD-1553B Notice 2, the BU-63825 provides an option to separate data received from broadcast messages from nonbroadcast received data.

Besides supporting a global double buffering scheme (as in BC mode), the Sp'ACE II RT provides a pair of 128-word Lookup Tables for memory management control, programmable on a subaddress basis (refer to TABLE 29). The 128-word tables include 32-word tables for transmit message pointers and receive message pointers. There is also a third, optional Lookup Table for broadcast message pointers, providing Notice 2 compliance, if necessary.

**TABLE 28. TYPICAL RT MEMORY MAP (SHOWN FOR 16K RAM)**

| ADDRESS (HEX) | DESCRIPTION |
|---|---|
| 0000-00FF | Stack A |
| 0100 | Stack Pointer A (fixed location) |
| 0101-0103 | RESERVED |
| 0104 | Stack Pointer B (fixed location) |
| 0105-0107 | RESERVED |
| 0108-010F | Mode Code Selective Interrupt Table (fixed area) |
| 0110-013F | Mode Code Data (fixed area) |
| 0140-01BF | Lookup Table A (fixed area) |
| 01C0-023F | Lookup Table B (fixed area) |
| 0240-0247 | Busy Bit Lookup Table (fixed area) |
| 0248-025F | (not used) |
| 0260-027F | Data Block 0 |
| 0280-02FF | Data Block 1-4 |
| 0300-03FF | Command Illegalizing Table (fixed area) |
| 0400-041F | Data Block 5 |
| 0420-043F | Data Block 6 |
| • | • |
| • | • |
| • | • |
| 3FE0-3FFF | Data Block 476 |

The fourth section of each of the RT Lookup Tables stores the 32 Subaddress Control Words (refer to TABLE 11 and TABLE 30). The individual Subaddress Control Words may be used to select the RT memory management option and interrupt scheme for each transmit, receive, and (optionally) broadcast subaddress.

**TABLE 29. LOOK-UP TABLES**

| AREA A | AREA B | DESCRIPTION | COMMENT |
|---|---|---|---|
| 0140<br>.<br>.<br>.<br>015F | 01C0<br>.<br>.<br>.<br>01DF | Rx(/Bcst)_SA0<br>.<br>.<br>.<br>Rx(/Bcst)_SA31 | Receive (/Broadcast) Lookup Table |
| 0160<br>.<br>.<br>.<br>017F | 01E0<br>.<br>.<br>.<br>01FF | Tx_SA0<br>.<br>.<br>.<br>Tx_SA31 | Transmit Lookup Table |
| 0180<br>.<br>.<br>.<br>019F | 0200<br>.<br>.<br>.<br>021F | Bcst_SA0<br>.<br>.<br>.<br>Bcst_SA31 | Broadcast Lookup Table Optional |
| 01A0<br>.<br>.<br>.<br>01BF | 0220<br>.<br>.<br>.<br>023F | SACW_SA0<br>.<br>.<br>.<br>SACW_SA31 | Subaddress Control Word Lookup Table (Optional) |

| TABLE 30. SUBADDRESS CONTROL WORD MEMORY MANAGEMENT SUBADDRESS BUFFER SCHEME | | | | |
|---|---|---|---|---|
| **MM2** | **MM1** | **MM0** | **DESCRIPTION** | **COMMENT** |
| 0 | 0 | 0 | Single Message or Double Buffered | |
| 0 | 0 | 1 | 128-Word | Circular Buffer of Specified Size |
| 0 | 1 | 0 | 256-Word | |
| 0 | 1 | 1 | 512-Word | |
| 1 | 0 | 0 | 1024-Word | |
| 1 | 0 | 1 | 2048-Word | |
| 1 | 1 | 0 | 4096-Word | |
| 1 | 1 | 1 | 8192-Word | |

For each transmit subaddress, there are two possible memory management schemes: (1) single message; and (2) circular buffer. For each receive (and optionally broadcast) subaddress, there are three possible memory management schemes: (1) single message; (2) double buffered; and (3) circular buffer. For each transmit, receive and broadcast subaddress, there are two interrupt conditions programmable by the respective Subaddress Control Word: (1) after every message to the subaddress; (2) after a circular buffer rollover. An additional table in RAM may be used to enable interrupts following selected mode code messages.

When using the circular buffer scheme for a given subaddress, the size of the circular buffer is programmable by three bits of the Subaddress Control Word (see TABLE 30). The options for circular buffer size are 128, 256, 512, 1024, 2048, 4096, and 8192 Data Words.

## SINGLE MESSAGE MODE

FIGURE 5 illustrates the RT Single Message memory management scheme. When operating the BU-63825 in its “AIM-HY” (default) mode, the Single Message scheme is implemented for all transmit, receive, and broadcast subaddresses. In the Single Message mode (also in the Double Buffer and Circular Buffer modes), there is a global double buffering scheme, controlled by bit 13 of Configuration Register #1. This selects from between the two sets of the various data structures shown in the figure: the Stack Pointers (fixed addresses), Descriptor Stacks (user defined addresses), RT Lookup Tables (fixed addresses), and RT Data Word blocks (user defined addresses). FIGURES 5, 6, and 7 delineate the “active” and ”nonactive” areas by the non-shaded and shaded areas, respectively.

As shown, the Sp’ACE II stores the Command Word from each message received, in the fourth location within the message descriptor (in the stack) for the respective message. The T/R bit, subaddress field, and (optionally) broadcast/own address, index into the active area Lookup Table, to locate the data block pointer for the current message. The BU-63825 RT memory management logic then accesses the data block pointer to locate the starting address for the Data Word block for the current message. The maximum size for an RT Data Word block is 32 words.

For a particular subaddress in the Single Message mode, there is overwriting of the contents of the data blocks for receive/broadcast subaddresses – or overreading, for transmit subaddresses. In the single message mode, it is possible to access multiple data blocks for the same subaddress. This, however, requires the intervention of the host processor to update the respective Lookup Table pointer. To implement a data wraparound subaddress, as required by Notice 2 of MIL-STD-1553B, the Single Message scheme should be used for the wraparound subaddress. Notice 2 recommends subaddress 30 as the wraparound subaddress.

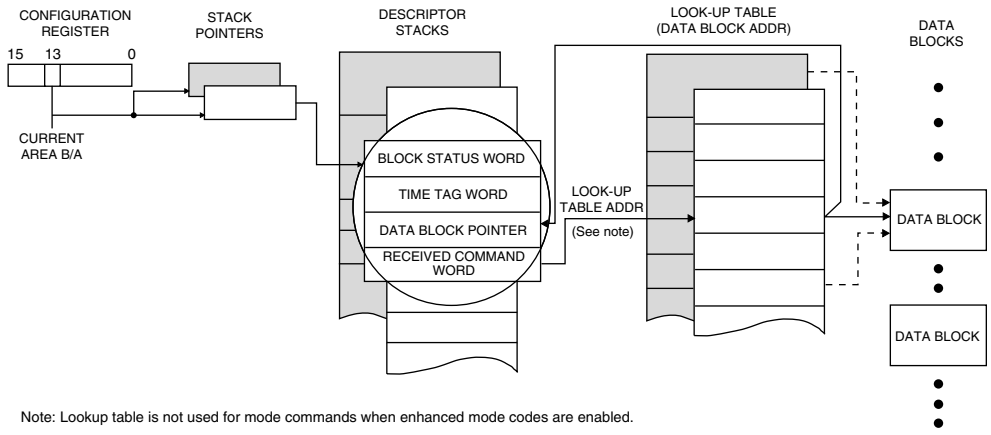
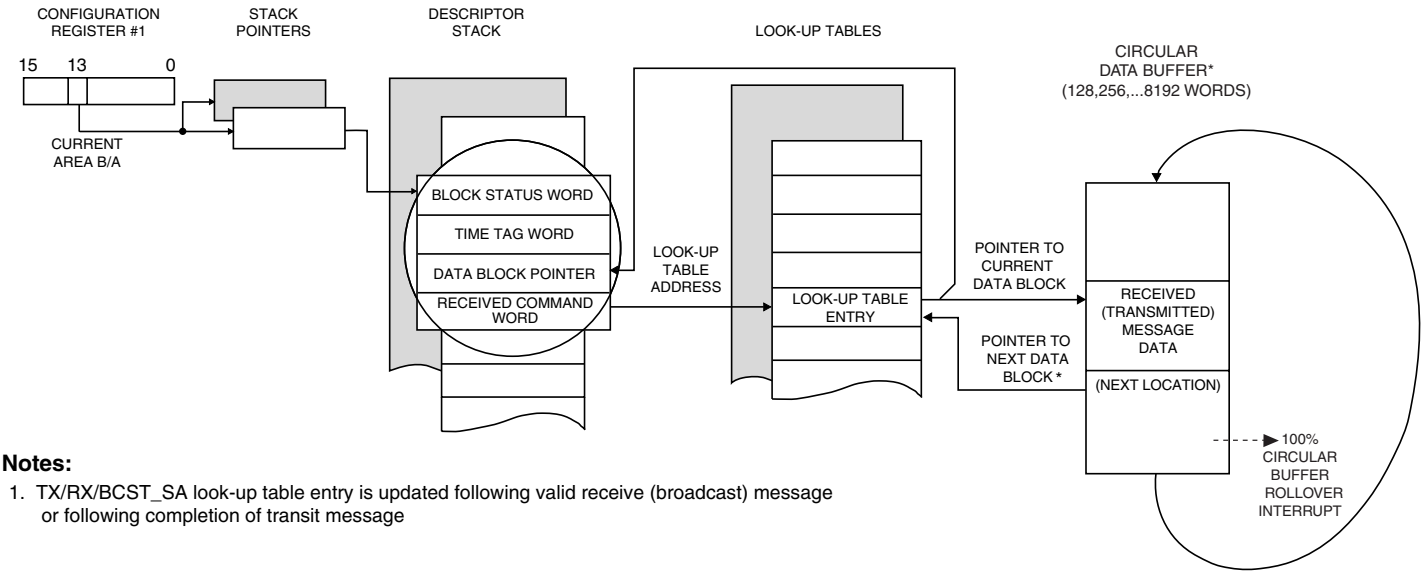



**FIGURE 5. RT MEMORY MANAGEMENT: SINGLE MESSAGE MODE**




**Notes:**

1. TX/RX/BCST_SA look-up table entry is updated following valid receive (broadcast) message or following completion of transit message

**FIGURE 6. RT MEMORY MANAGEMENT: CIRCULAR BUFFER MODE**

## CIRCULAR BUFFER MODE

FIGURE 6 illustrates the RT circular buffer memory management scheme. The circular buffer mode facilitates bulk data transfers. The size of the RT circular buffer, shown on the right side of the figure, is programmable from 128 to 8192 words (in even powers of 2) by the respective Subaddress Control Word. As in the single message mode, the host processor initially loads the individual Lookup Table entries. At the start of each message, the Sp'ACE II stores the Lookup Table entry in the third position of the respective message block descriptor in the stack area of RAM, as in the Single Message mode. The Sp'ACE II transfers Receive or Transmit Data Words to (from) the circular buffer, starting at the location referenced by the Lookup Table pointer.

At the end of a valid (or, optionally, invalid) message, the value of the Lookup Table entry updates to the next location after the last address accessed for the current message. As a result, Data Words for the next message directed to the same Tx/Rx(/Bcst) subaddress will be accessed from the next contiguous block of address locations within the circular buffer. As a recommended option, the Lookup Table pointers may be programmed to not update following an invalid receive (or broadcast) message. This allows the 1553 bus controller to retry the failed message, resulting in the valid (retried) data overwriting the invalid data. This eliminates overhead for the RT's host processor. When the pointer reaches the lower boundary of the circular buffer (located at 128, 256, . . . 8192-word boundaries in the BU-63825 address space), the pointer moves to the top boundary of the circular buffer, as FIGURE 6 shows.

### *IMPLEMENTING BULK DATA TRANSFERS*

The use of the Circular Buffer scheme is ideal for bulk data transfers; that is, multiple messages to/from the same subaddress. The recommendation for such applications is to enable the circular buffer interrupt request. By so doing, the routine transfer of multiple messages to the selected subaddress, including errors and retries, is transparent to the RT's host processor. By strategically initializing the subaddress's Lookup Table pointer prior to the start of the bulk transfer, the BU-63825 may be configured to issue an interrupt request only after it has received the anticipated number of valid Data Words to the designated subaddress.

## SUBADDRESS DOUBLE BUFFERING MODE

For receive (and broadcast) subaddresses, the BU-63825 RT offers a third memory management option, Subaddress Double Buffering. Subaddress double buffering provides a means of ensuring data consistency. FIGURE 7 illustrates the RT Subaddress Double Buffering scheme. Like the Single Message and Circular Buffer modes, the Double Buffering mode may be selected on a subaddress basis by means of the Subaddress Control Word. The purpose of the Double Buffering mode is to provide the host processor a convenient means of accessing the most recent, valid data received to a given subaddress. This serves to ensure the highest possible degree of data consistency by allocating two 32-bit Data Word blocks for each individual receive (and/or broadcast) subaddress.

At a given point in time, one of the two blocks will be designated as the "active" 1553 data block while the other will be designated as the "inactive" block. The Data Words from the next receive message to that subaddress will be stored in the "active" block.

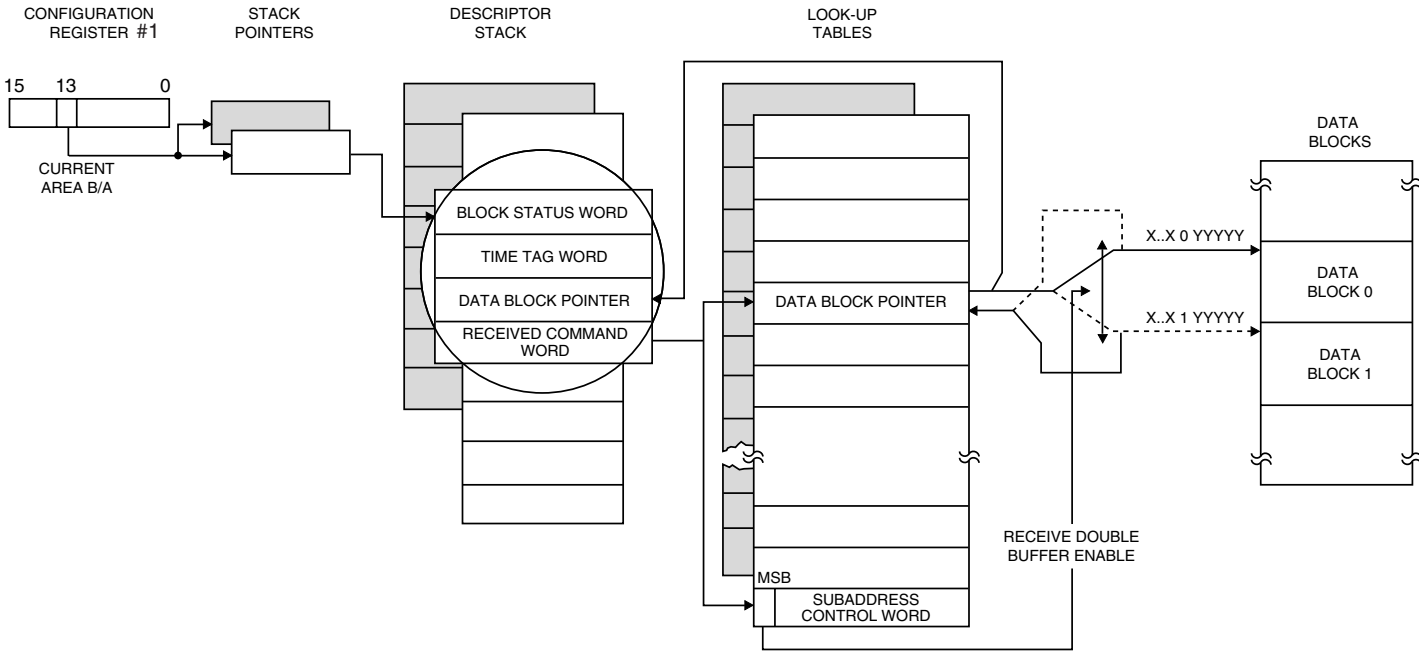



**FIGURE 7. RT MEMORY MANAGEMENT: SUBADDRESS DOUBLE BUFFERING MODE**

Upon completion of the message, provided that the message was valid and Subaddress Double Buffering is enabled, the BU-63825 will automatically switch the "active" and "inactive" blocks for the respective subaddress. The Sp'ACE II accomplishes this by toggling bit 5 of the subaddress's Lookup Table Pointer and rewriting the pointer. As a result, the most recent valid block of received Data Words will always be readily accessible to the host processor.

As a means of ensuring data consistency, the host processor is able to reliably access the most recent valid, received Data Word block by performing the following sequence:

(1) Disable the double buffering for the respective subaddress by the Subaddress Control Word. That is, temporarily switch the subaddress's memory management scheme to the Single Message mode.

(2) Read the current value of the receive (or broadcast) subaddress's Lookup Table pointer. This points to the current "active" Data Word block. By inverting bit 5 of this pointer value, it is possible to locate the start of the "inactive" Data Word block. This block will contain the Data Words received during the most recent valid message to the subaddress.

(3) Read out the words from the "inactive" (most recent) Data Word Block.

(4) Re-enable the Double Buffering mode for the respective subaddress by the Subaddress Control Word.

## RT INTERRUPTS

As in BC mode, the BU-63825 RT provides many maskable interrupts. RT interrupt conditions include End of (every) Message, Message Error, Selected Subaddress (Subaddress Control Word) Interrupt, Circular Buffer Rollover, Selected Mode Code Interrupt, and Stack Rollover.

## DESCRIPTOR STACK

At the beginning and end of each message, the BU-63825 RT stores a four-word message descriptor in the active area stack. The RT stack size is programmable, with choices of 256, 512, 1024, and 2048 words. FIGURES 5, 6, and 7 show the four words: Block Status Word, Time Tag Word, Data Block Pointer, and the 1553 received Command Word. The RT Block Status Word includes indications of message in-progress or message complete, bus channel, RT-to-RT transfer and RT-to-RT transfer errors, message format error, loop test (self-test) failure, circular buffer rollover, illegal command, and other error conditions. TABLE 24 shows the bit mapping of the RT Block Status Word.

As in BC mode, the Time Tag Word stores the current contents of the BU-63825's read/writable Time Tag Register. The resolution of the Time Tag Register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. Also, incrementing of the Time Tag counter may be from an external clock source or via software command.

The Sp'ACE II stores the contents of the accessed Lookup Table location for the current message, indicating the starting location of the Data Word block, as the Data Block Pointer. This serves as a convenience in locating stored message data blocks.

The Sp'ACE II stores the full 16-bit 1553 Command Word in the fourth location of the RT message descriptor.

## RT COMMAND ILLEGALIZATION

The BU-63825 provides an internal mechanism for RT command illegalization. In addition, there is a means for allowing the setting of the Busy Status Word bit to be only for a programmed subset of the transmit/receive/broadcast subaddresses.

The illegalization scheme uses a 256-word area in the BU-63825's address space. A benefit of this feature is the reduction of printed circuit board requirements, by eliminating the need for an external PROM, PLD, or RAM device that does the illegalizing function. The BU-63825's illegalization scheme provides maximum flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/$\overline{R}$ bit, subaddress, and word count/mode code to be illegalized. Another advantage of the RAM-based illegalization technique is that it provides for a high degree of self-testability.

### *ADDRESSING THE ILLEGALIZATION TABLE*

TABLE 31 illustrates the addressing scheme of the illegalization RAM. As shown, the base address of the illegalizing RAM is 0300 (hex). The Sp'ACE II formulates the index into the Illegalizing Table based on the values of $\overline{\text{BROADCAST}}$/OWNADDRESS ADDRESS, T/$\overline{R}$ bit, Subaddress, and the MSB of the Word Count/Mode Code field (WC/MC4) of the current Command Word.

The internal RAM has 256 words reserved for command illegalization. Broadcast commands may be illegalized separately from nonbroadcast receive commands and mode commands.

Commands may be illegalized down to the word count level. For example, a one-word receive command to subaddress 1 may be legal, while a two-word receive command to subaddress 1 may be illegalized.

The first 64 words of the Illegalization Table refer to broadcast receive commands (two words per subaddress). The next 64 words refer to broadcast transmit commands. Since nonmode code broadcast transmit commands are by definition invalid, this section of the table (except for subaddresses 0 and 31) does not need to be initialized by the user. The next 64 words correspond to nonbroadcast receive commands. The final 64 words refer to nonbroadcast transmit commands. Messages with Word Count/Mode Code (WC/MC) fields between 0 and 15 may be illegalized by setting the corresponding data bits for the respective even-numbered address locations in the illegalization table. Likewise, messages with WC/MC fields between 16 and 31 may be illegalized by setting the corresponding data bits for the respective odd-numbered address locations in the illegalization table.

The following should be noted with regards to command illegalization:

(1) To illegalize a particular word count for a given broadcast/own address-T/$\overline{R}$ subaddress, the appropriate bit position in the respective illegalization word should be set to logic 1. A bit value of logic 0 designates the respective Command Word as a legal command. The BU-63825 will respond to an illegalized nonbroadcast command with the Message Error bit set in its RT Status Word.

(2) For subaddresses 00001 through 11110, the "WC/MC" field specifies the Word Count field of the respective Command Word. For subaddresses 00000 and 11111, the "WC/MC" field specifies the Mode Code field of the respective Command Word.

(3) Since nonmode code broadcast transmit messages are not defined by MIL-STD-1553B, the sixty (60) words in the illegalization RAM, addresses 0342 through 037D, corresponding to these commands do not need to be initialized. The BU-63825 will not respond to a nonmode code broadcast transmit command, but will automatically set the Message Error bit in its internal Status Register, regardless of whether or not the corresponding bit in the illegalization RAM has been set. If the next message is a Transmit Status or Transmit Last Command mode code, the BU-63825 will respond with its Message Error bit set.

**TABLE 31. ILLEGALIZATION RAM ADDRESS DEFINITION**

| BIT | DESCRIPTION |
|---|---|
| 15(MSB) | 0 |
| 14 | 0 |
| 13 | 0 |
| 12 | 0 |
| 11 | 0 |
| 10 | 0 |
| 9 | 1 |
| 8 | 1 |
| 7 | $\overline{\text{BROADCAST}}$/OWN_ADDRESS |
| 6 | T/R |
| 5 | SA4 |
| 4 | SA3 |
| 3 | SA2 |
| 2 | SA1 |
| 1 | SA0 |
| 0(LSB) | WC4/MC4 |

### PROGRAMMABLE BUSY

As a means of providing compliance with Notice 2 of MIL-STD-1553B, the BU-63825 RT provides a software controllable means for setting the Busy Status Word bit as a function of subaddress. By a Busy Lookup Table in the BU-63825 address space, it is possible to set the Busy bit based on command broadcast/own address, T/$\overline{R}$ bit, and subaddress. Another programmable option allows received Data Words to be either stored or not stored for messages when the Busy bit is set.

### OTHER RT FUNCTIONS

The BU-63825 allows the hardwired RT Address to be read by the host processor. Also, there are options for the RT FLAG Status Word bit to be set under software control and/or automatically following a failure of the loopback self-test. Other software controllable RT options include software programmable RT Status and RT BIT words, automatic clearing of the Service Request Status Word bit following a Transmit Vector Word mode command, capabilities to clear and/or load the Time Tag Register following receipt of Synchronize mode commands, options regarding Data Word transfers for the Busy and/or Message Error (Illegal) Status Word bits, and for handling of 1553A and reserved mode codes.

## MONITOR (MT) ARCHITECTURE

The BU-63825 provides three bus monitor (MT) modes:

(1) The “AIM-HY” (default) or “AIM-HY’er” Word Monitor mode.

(2) A Selective Message Monitor mode.

(3) A Simultaneous Remote Terminal/Selective Message Monitor mode.

The strong recommendation for new applications is the use of the Selective Message Monitor, rather than the Word Monitor. Besides providing monitor filtering based on RT Address,T/$\overline{R}$ bit, and Subaddress, the Message Monitor eliminates the need to determine the start and end of messages by software. The development of such software tends to be a tedious task. Moreover, at run time, it tends to entail a high degree of CPU overhead.

### WORD MONITOR

In the Word Monitor mode, the BU-63825 monitors both 1553 buses. After initializing the Word Monitor and putting it on-line the BU-63825 stores all Command, Status, and Data Words received from both buses. For each word received from either bus, the BU-63825 stores a pair of words in RAM. The first word is the 16 bits of data from the received word. The second word is the Monitor Identification (ID), or “Tag” word. The ID Word contains information relating to bus channel, sync type, word validity, and interword time gaps. The BU-63825 stores data and ID words in a circular buffer in the shared RAM address space. TABLE 25 shows the bit mapping for the Monitor ID word.

### MONITOR TRIGGER WORD

There is a Trigger Word Register that provides additional flexibility for the Word Monitor mode. The BU-63825 stores the value of the 16-bit Trigger Word in the MT Trigger Word Register. The contents of this register represent the value of the Trigger Command Word. The BU-63825 has programmable options to start or stop the Word Monitor, and/or to issue an interrupt request following receipt of the Trigger Command Word from the 1553 bus.

### SELECTIVE MESSAGE MONITOR MODE

The BU-63825 Selective Message Monitor provides features to greatly reduce the software and processing burden of the host CPU. The Selective Message Monitor implements selective monitoring of messages from a dual 1553 bus, with the monitor filtering based on the RT Address, T/$\overline{R}$ bit, and Subaddress fields of received 1553 Command Words. The Selective Message Monitor mode greatly simplifies the host processor software by distinguishing between Command and Status Words. The Selective Message Monitor maintains two stacks in the BU-63825 RAM: a Command Stack and a Data Stack.

#### *SIMULTANEOUS RT/MESSAGE MONITOR MODE*

The Selective Message Monitor may function as a purely passive monitor or may be programmed to function as a simultaneous RT/Monitor. The RT/Monitor mode provides complete Remote Terminal (RT) operation for the BU-63825’s strapped RT address and bus monitor capability for the other 30 non-broadcast RT addresses. This allows the BU-63825 to simultaneously operate as a full function RT and “snoop” on all or a subset of the bus activity involving the other RTs on a bus. This type of operation is sometimes needed to implement a backup bus controller. The combined RT/Selective Monitor maintains three stack areas in the BU-63825 address space: an RT Command Stack, a Monitor Command Stack, and a Monitor Data Stack. The pointers for the various stacks have fixed locations in the BU-63825 address space.

#### *SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION*

TABLE 32 illustrates a typical memory map for the Sp’ACE II in the Selective Message Monitor mode. This mode of operation defines several fixed locations in the RAM. These locations allocate in a manner that is compatible with the combined RT/Selective Message Monitor mode. The fixed memory map consists of two Monitor Command Stack Pointers (location 102h and 106h), two Monitor Data Stack Pointers (locations 103h and 107h), and a Selective Message Monitor Lookup Table (0280-02FFh) based on RT Address T/$\overline{R}$, and subaddress. Assume a Monitor Command Stack size of 1K words, and a Monitor Data Stack size of 4K words.

| TABLE 32. TYPICAL SELECTIVE MESSAGE MONITOR MEMORY MAP (SHOWN FOR 16K RAM) | |
|---|---|
| **ADDRESS (HEX)** | **DESCRIPTION** |
| 0000-0101 | Not Used |
| 0102 | Monitor Command Stack Pointer A (fixed location) |
| 0103 | Monitor Data Stack Pointer A (fixed location) |
| 0104-0105 | Not Used |
| 0106 | Monitor Command Stack Pointer B (fixed location) |
| 0107 | Monitor Data Stack Pointer B (fixed location) |
| 0108-027F | Not Used |
| 0280-02FF | Selective Monitor Lookup Table (fixed area) |
| 0300-03FF | Not Used |
| 0400-07FF | Monitor Command Stack A (1K words) |
| 0800-3FFF | Monitor Command Stack B (1K words) |
| 0C00-0FFF- | Not Used (1K words) |
| 1000-1FFF | Monitor Data Stack A (4K words) |
| 2000-2FFF | Monitor Data Stack B (4K words) |
| 3000-3FFF | Not Used (4K words) |

Refer to FIGURE 8 for an illustration of the Selective Message Monitor operation. Upon receipt of a valid Command Word, the BU-63825 will reference the Selective Monitor Lookup Table (a fixed block of addresses) to check for the condition (disabled/enabled) of the current command. If disabled, the BU-63825 will ignore (and not store) the current message; if enabled, the BU-63825 will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer.

Similar to RT mode, The Sp'ACE II stores a Block Status Word, 16-bit Time Tag Word, and Data Block Pointer in the Message Descriptor, along with the received 1553 Command Word following reception of the Command Word. The Sp'ACE II writes the Block Status and Time Tag Words at both the start and end of the message. The Monitor Block Status Word contains indications of message in-progress or message complete, bus channel, Monitor Data Stack Rollover, RT-to-RT transfer and RT-to-RT transfer errors, message format error, and other error conditions. TABLE 26 shows the Message Monitor Block Status Word. The Data Block Pointer references the first word stored in the Monitor Data Stack (the first word following the Command Word) for the current message. The BU-63825 will then proceed to store the subsequent words from the message [possible second Command Word, Data Word(s), Status Word(s)] into consecutive locations in the Monitor Data Stack.

The size of the Monitor Command Stack is programmable to 256, 1K, 4K, or 16K words. The Monitor Data Stack size is programmable to 512, 1K, 2K, 4K, 8K, 16K, 32K, or 64K words.

Monitor interrupts may be enabled for Monitor Command Stack Rollover, Monitor Data Stack Rollover, and/or End-of-Message conditions. In addition, in the Word Monitor mode there may be an interrupt enabled for a Monitor Trigger condition.

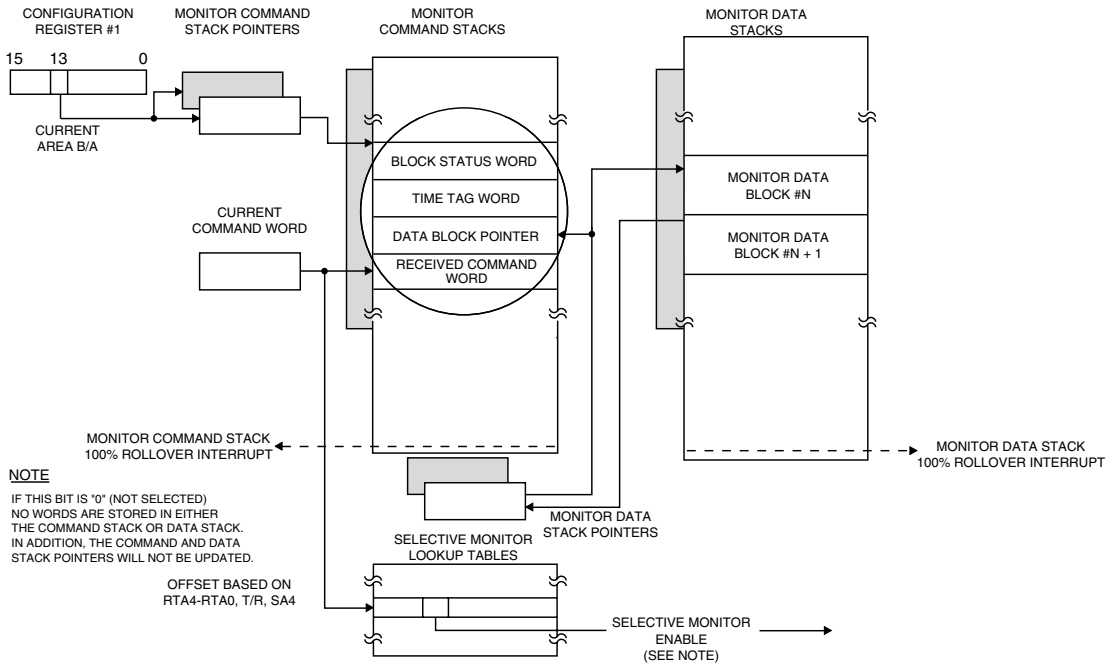



**FIGURE 8. SELECTIVE MESSAGE MONITOR OPERATION**

## PROCESSOR AND MEMORY INTERFACE

The Sp'ACE II terminals provide much flexibility for interfacing to a host processor and optional external memory. FIGURE 1 shows that there are 14 control signals, 6 of which are dual purpose, for the processor/memory interface. FIGURES 9 through 14 illustrate six of the configurations that may be used for interfacing the BU-63825 to a host processor bus. The various possible configurations serve to reduce to an absolute minimum the amount of glue logic required to interface to 8-, 16-, and 32-bit processor buses. Also included are features to facilitate interfacing to processors that do not have a "wait state" type of handshake acknowledgment. Finally, the Sp'ACE II supports a reliable interface to an external dual port RAM. This type of interface minimizes the portion of the available processor bandwidth required to access the 1553 RAM.

The 16-bit buffered mode (FIGURE 9) is the most common configuration used. It provides a direct, shared RAM interface to a 16-bit or 32-bit microprocessor. In this mode, the Sp'ACE II's internal address and data buffers provide the necessary isolation between the host processor's address and data buses and the corresponding internal memory buses. In the buffered mode, the 1553 shared RAM address space limit is the BU-63825's 16K words of internal RAM. The 16-bit buffered mode provides a pair of pin-programmable options:

(1) The logic sense of the RD/$\overline{WR}$ control input is selectable by the POLARITY_SEL input; for example, write when RD/$\overline{WR}$ is low for Motorola 680X0 processors; write when RD/$\overline{WR}$ is high for the Intel i960 series microprocessors.

(2) By strapping the input signal $\overline{ZERO\ WAIT}$ to logic "1", the Sp'ACE II terminals may interface to processors that have an acknowledge type of handshake input to accommodate hardware controlled wait states; most current processor chips have such an input. In this case, the BU-63825 will assert its $\overline{READY}$ output low only after it has latched WRITE data internally or has presented READ data on D15-D0.

By strapping $\overline{ZERO\ WAIT}$ to logic "0", it is possible to easily interface the BU-63825 to processors that do not have an acknowledge type of handshake input. An example of such a processor is Analog Device's ADSP2101 DSP chip. In this configuration, the processor can clear its strobe output before the completion of access to the BU-63825 internal RAM or register. In this case, $\overline{READY}$ goes high following the rising edge of $\overline{STRBD}$ and will stay high until completion of the transfer. $\overline{READY}$ will normally be low when $\overline{ZERO\ WAIT}$ is low.

Similar to the 16-bit buffered mode, the 16-bit transparent mode (FIGURE 10) supports a shared RAM interface to a host CPU. The transparent mode offers the advantage of allowing the buffer RAM size to be expanded to up to 64K words, using external RAM. A disadvantage of the transparent mode is that it requires external address and data buffers to isolate the processor buses from the memory/BU-63825 buses.

A modified version of the transparent mode involves the use of dual port RAM, rather than conventional static RAM. Refer to FIGURE 11. This allows the host to access RAM very quickly, the only limitation being the access time of the dual port RAM. This configuration eliminates the BU-63825 arbitration delays for memory accesses. The worst case delay time occurs only during a simultaneous access by the host and the BU-63825 1553 logic to the same memory address. In general, this will occur very rarely and the Sp'ACE II limits the delay to approximately 250 ns.

FIGURE 12 illustrates the connections for the 16-bit Direct Memory Access (DMA) mode. In this configuration the host processor, rather than the Sp'ACE II terminal, arbitrates the use of the address and data buses. The arbitration involves the two DMA output signals Request ($\overline{DTREQ}$), Acknowledge ($\overline{DTACK}$), and the input signal Grant ($\overline{DTGRT}$). The DMA interface allows the Sp'ACE II components to interface to large amounts of system RAM while eliminating the need for external buffers. For system address spaces larger than 64K words, it is necessary for the host processor to provide a page register for the upper address bits (above A15) when the BU-63825 accesses the RAM (while asserting ($\overline{DTACK}$) low).

The internal RAM is accessible through the standard Sp'ACE II interface ($\overline{SELECT}$, $\overline{STRBD}$, $\overline{READYD}$, etc). The host CPU may access external RAM by the Sp'ACE II's arbitration logic and output control signals, as illustrated in FIGURE 12. Alternatively, control of the RAM may be shared by both the host processor and the Sp'ACE II, as illustrated in FIGURE 13. The latter requires the use of external logic, but allows the processor to access the RAM directly at the full access speed of the RAM, rather than waiting for the Sp'ACE II handshake acknowledge output $\overline{READY}$.

FIGURE 14 illustrates the 8-bit buffered mode (Please see Appendix G in the ACE User's Guide for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode). This interface allows a direct connection to 8-bit microprocessors and 8-bit microcontrollers. As in the 16-bit buffered configuration, the buffer RAM limit is the BU-63825's 16K words of internal RAM. In the 8-bit mode, the host CPU accesses the BU-63825's internal registers and RAM by a pair of 8-bit registers embedded in the Sp'ACE II interface. The 8-bit interface (Please see Appendix G in the ACE User's Guide for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode) may be further configured by three strappable inputs: $\overline{ZEROWAIT}$, POLARITY_SEL, and TRIGGER_SEL. By connecting $\overline{ZEROWAIT}$ to logic "0", the BU-63825 may be interfaced with minimal "glue" logic to 8-bit microcontrollers, such as the Intel 8051 series, that do not have an Acknowledge type of handshake input. The program-

mable inputs POLARITY_SEL and TRIGGER_SEL allow the BU-63825 to accommodate the different byte ordering conventions and “A0” logic sense utilized by different 8-bit processor families (Please see Appendix G in the ACE User’s Guide for Product Advisory regarding SP’ACE and SP’ACE II operating in 8-bit Buffered Non-Zero Wait Mode).

## PROCESSOR INTERFACE TIMING

FIGURES 16 and 17 illustrate the timing for the host processor to access the Sp’ACE II’s internal RAM or registers in the 16-bit, nonzero wait buffered mode. FIGURE 16 illustrates the 16-bit, buffered, nonzero wait state mode read cycle timing while FIGURE 17 shows the 16-bit, buffered, nonzero wait state mode write cycle timing.

During a CPU transfer cycle, the signals $\overline{\text{STRB}}$ and $\overline{\text{SELECT}}$ must be sampled low on the rising edge of the system clock to request access to the BU-63825’s internal shared RAM. The transfer will begin on the second rising system clock edge when $\overline{\text{STRBD}}$ is low, provided $\overline{\text{SELECT}}$ is sampled low and the 1553 protocol/memory management unit is not accessing the internal RAM. The falling edge of the output signal $\overline{\text{IOEN}}$ indicates the start of the transfer. The Sp’ACE II latches the signals MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ internally on the first falling clock edge after the start of the transfer cycle. The address inputs latch internally on the first rising clock edge after the signal $\overline{\text{IOEN}}$ goes low. Note that the address lines may be latched at any time using the ADDR_LAT input signal.

The output signal $\overline{\text{READYD}}$ will be asserted low on the third (or 7th if it’s an internal read) rising system clock edge after $\overline{\text{IOEN}}$ goes low. The assertion of $\overline{\text{READYD}}$ low indicates to the host processor that read data is available on the parallel data bus, or that write data has been stored. At this time, the CPU should bring the signal STRBD high, completing the transfer cycle.

## ADDRESS LATCH TIMING

FIGURE 15 illustrates the operation and timing of the address input latches for the buffered interface mode. In the transparent mode, the address buffers are always transparent. Since the transparent mode requires the use of external buffers, external address latches would be required to demultiplex a multiplexed address bus. In the buffered mode however, the Sp’ACE II’s internal address latches may be used to perform the demultiplexing function.

The ADDR_LAT input signal controls address latch operation. When ADDR_LAT is high, the outputs of the latch (which drive the Sp’ACE II’s internal memory bus) track the state of address inputs A15 - A00. When low, the internal memory bus remains latched at the state of A15 - A00 just prior to the falling edge of ADDR_LAT.

## MISCELLANEOUS

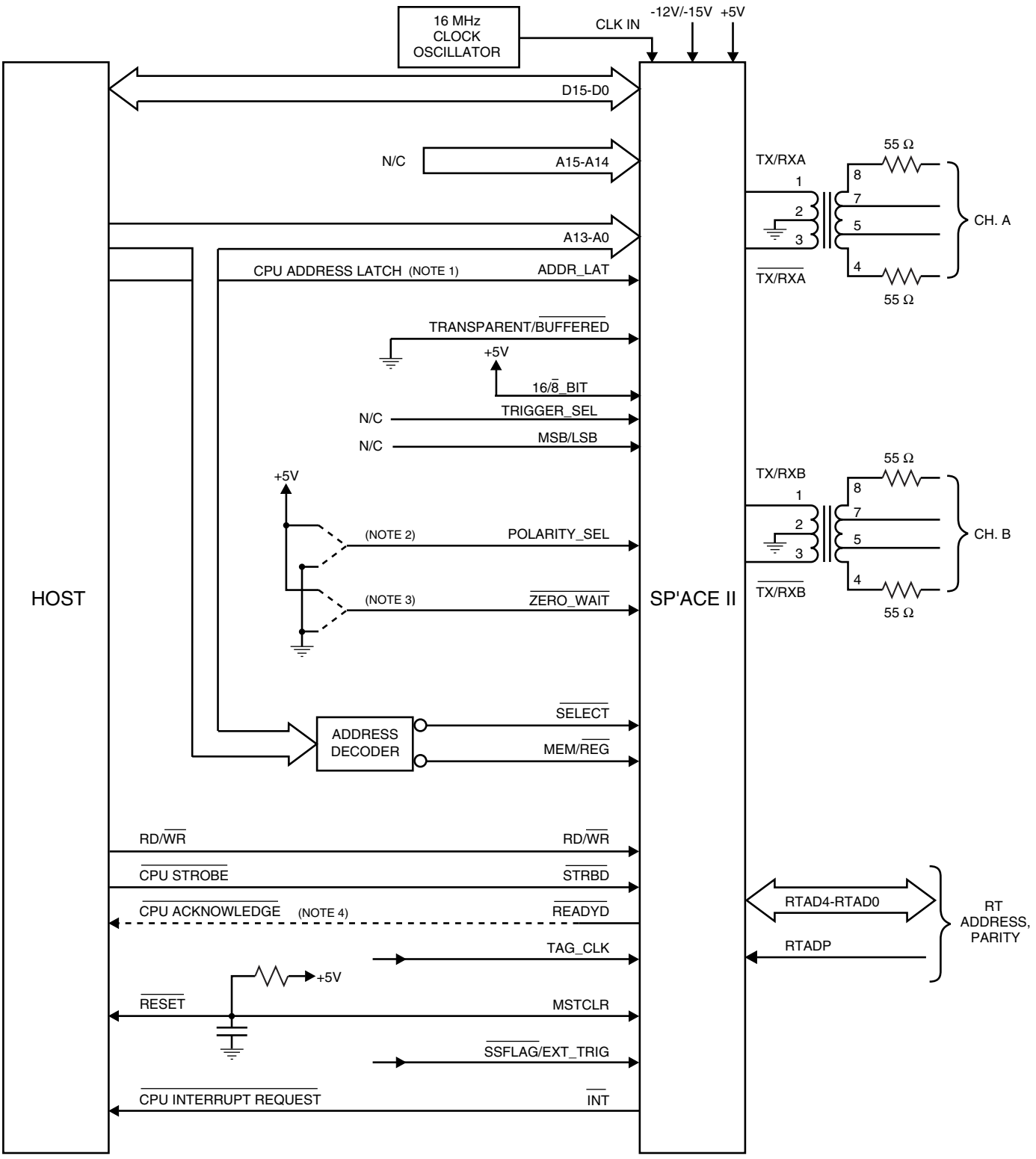
### *SELF-TEST*

The BU-63825 products incorporate several self-test features. These features include an on-line wraparound self-test for all messages in BC and RT modes, an off-line wraparound self-test for BC mode, and several other internal self-test features.

The BC/RT on-line loop test involves a wraparound test of the encoder/decoder and transceiver. The BC off-line self-test involves the encoder/decoder, but not the transceiver. These tests entail checking the received version of every transmitted word for validity (sync, encoding, bit count, parity) and checking the received version of the last transmitted word for a bit-by-bit comparison with the encoded word. The loopback test also fails if there is a timeout of the internal transmitter watchdog timer. A failure of the loop test results in setting a bit in the message’s Block Status Word and, if enabled, will result in an interrupt request. With appropriate host processor software, the BC off-line test is able to exercise the parallel and serial data paths, encoder, decoder, and a substantial portion of the BC protocol and memory management logic.

There are additional built-in self-test features, involving the use of three configuration register bits and the eight test registers. This allows a comprehensive test of the M-Rad chip’s internal logic. These tests include an encoder test, a decoder test, a register test, a protocol test, and a test of the fail-safe (transmitter timeout) timer.

In the test mode, the host processor can emulate arbitrary activity on the 1553 buses by writing to a pair of test registers. The test mode can be operated in conjunction with the Word Monitor mode to facilitate end-to-end self-tests.




NOTES:

1. CPU ADDRESS LATCH SIGNAL PROVIDED BY PROCESSORS WITH MULTIPLEXED ADDRESS/DATA BUSES.
2. IF POLARITY_SEL = "1", THEN RD/WR IS HIGH TO READ. LOW TO WRITE.
   IF POLARITY_SEL = "0", THEN RD/WR IS LOW TO READ. HIGH TO WRITE.
3. ZERO WAIT SHOULD BE STRAPPED TO LOGIC "1" FOR NON-ZERO WAIT INTERFACE AND TO LOGIC "0" FOR ZERO WAIT INTERFACE.
4. CPU ACKNOWLEDGE PROCESSOR INPUT ONLY FOR NON-ZERO WAIT TYPE OF INTERFACE.

**FIGURE 9. 16-BIT BUFFERED MODE**

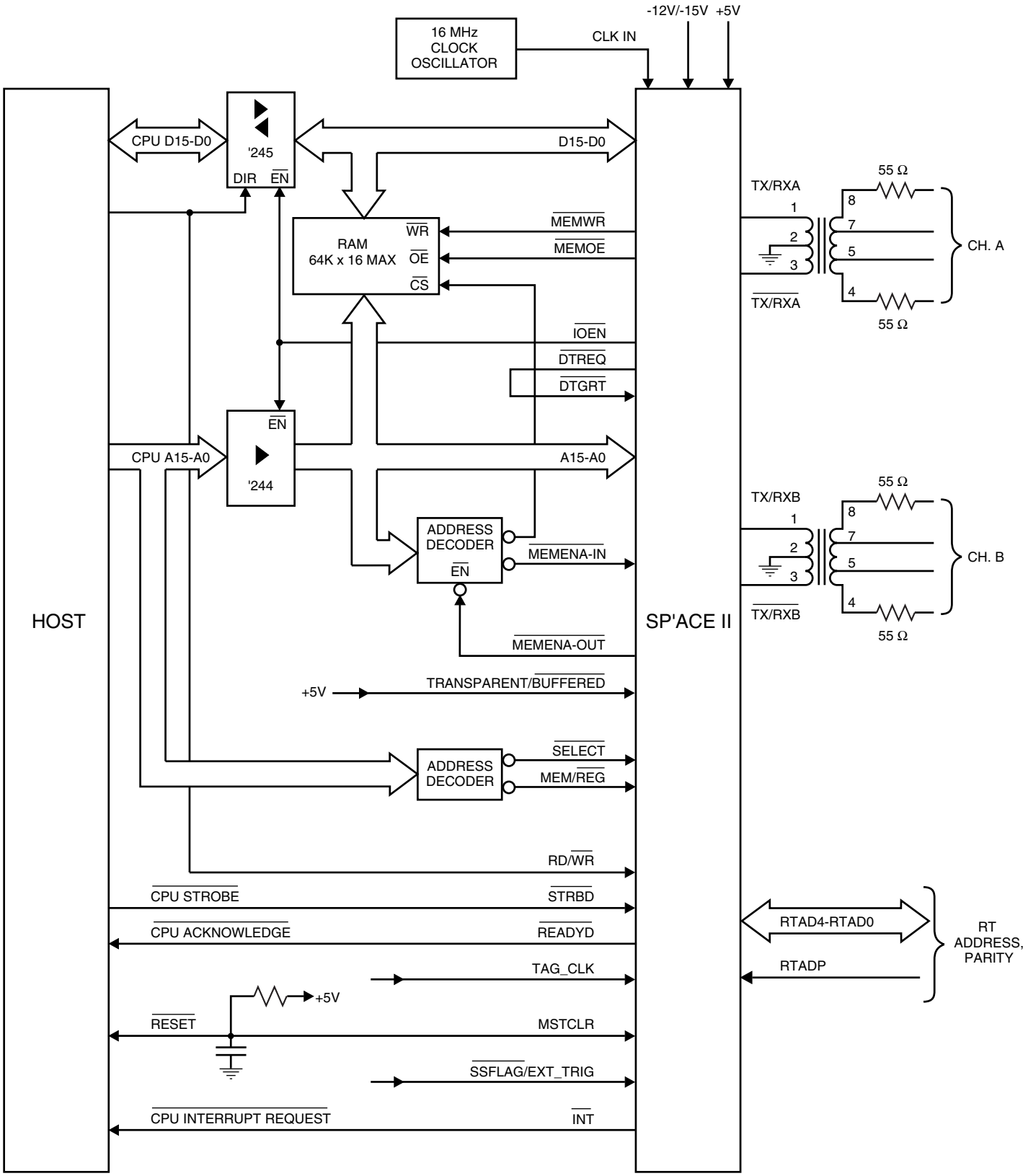



**FIGURE 10. 16-BIT TRANSPARENT MODE**

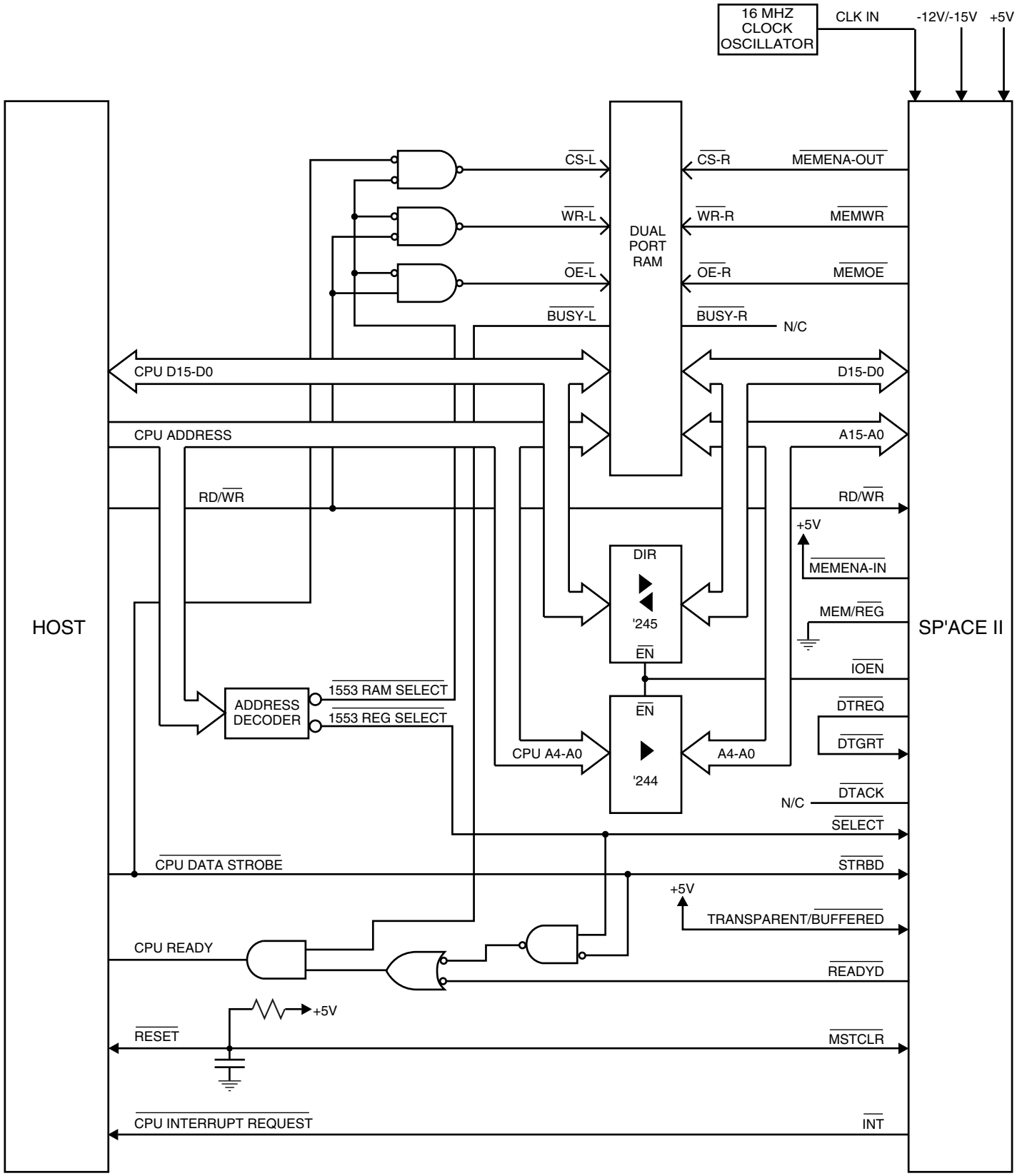



**FIGURE 11. 16-BIT TRANSPARENT MODE USING DUAL PORT RAM**

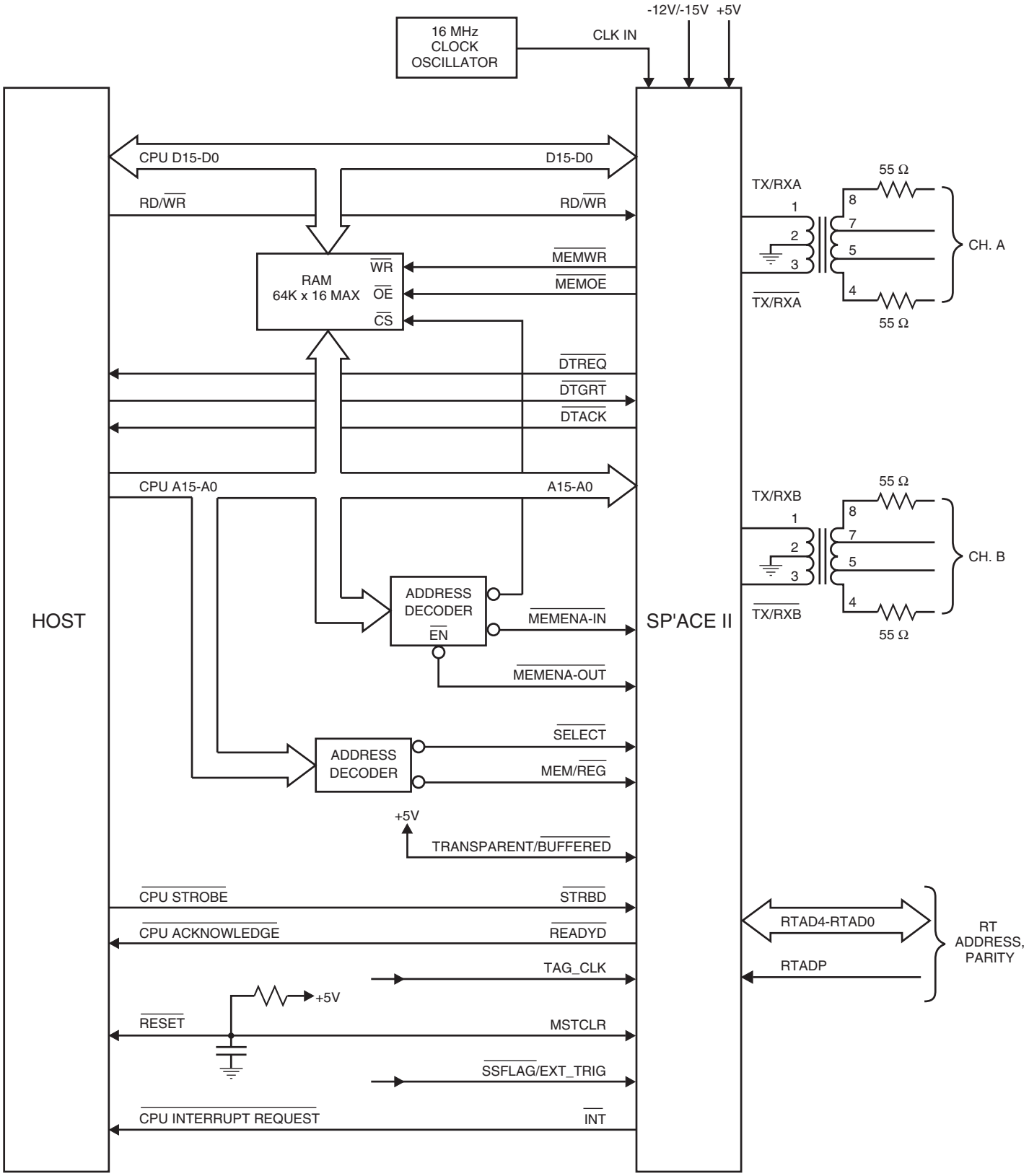



**FIGURE 12. 16-BIT DIRECT MEMORY ACCESS (DMA) MODE**

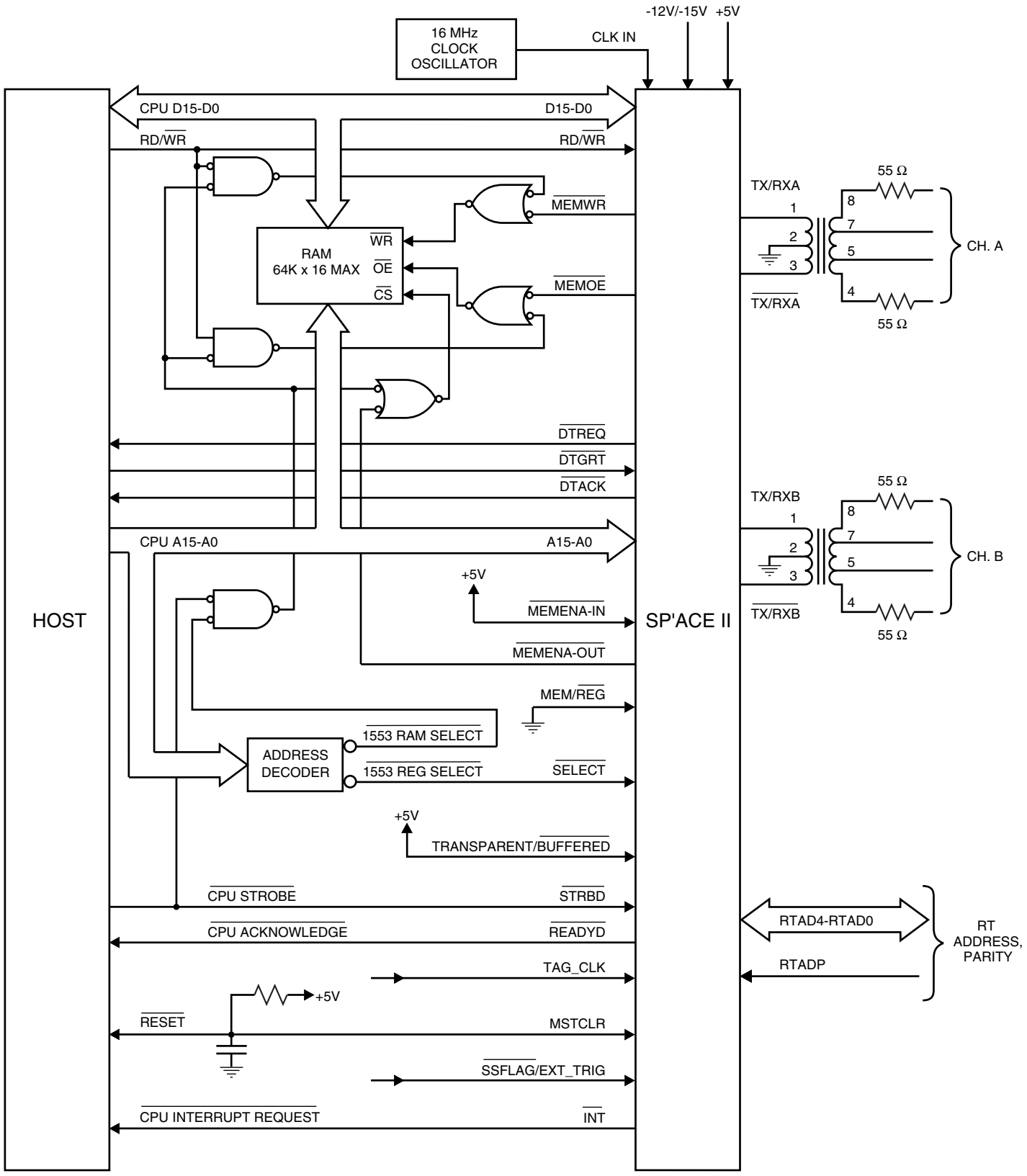
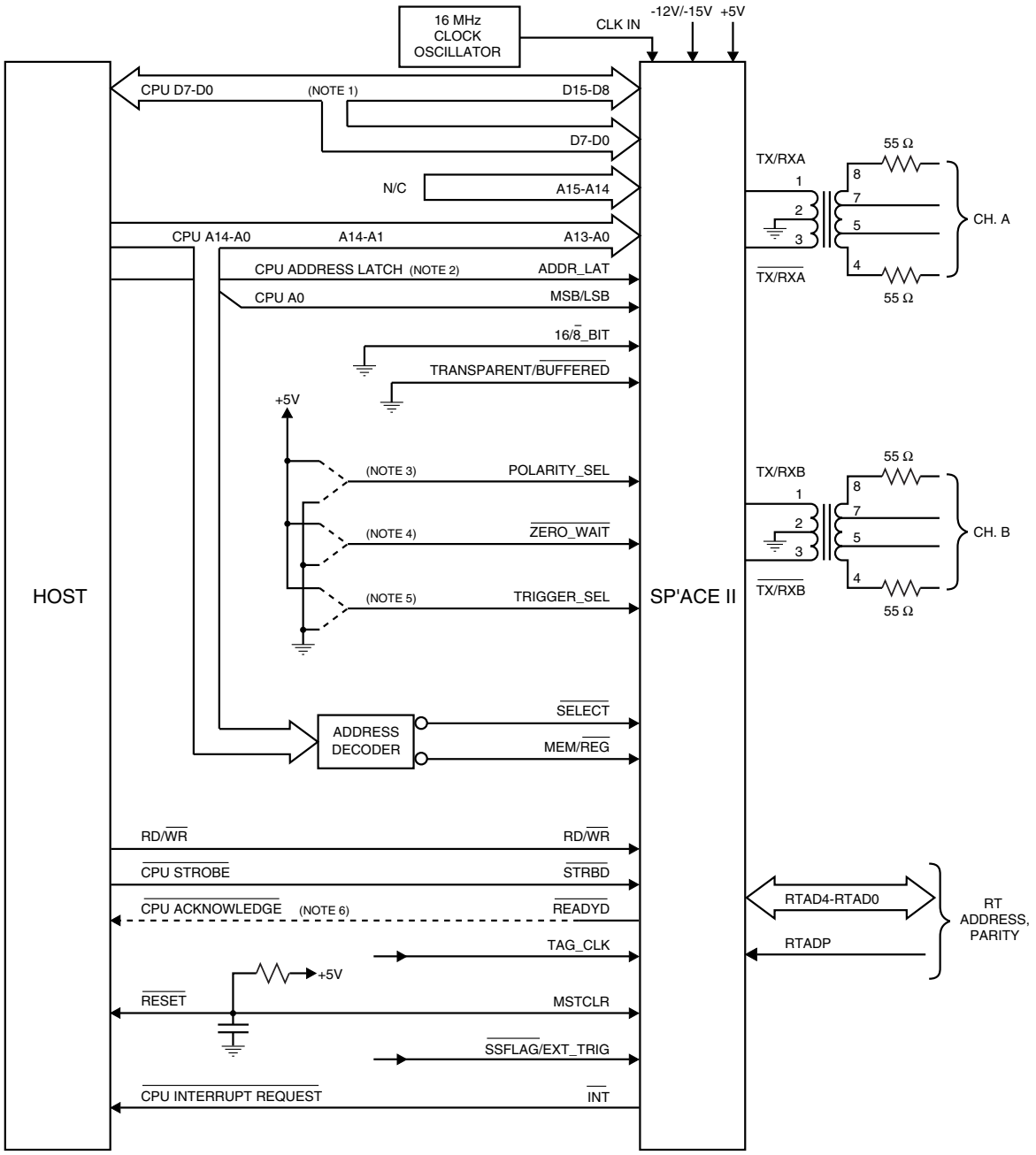



**FIGURE 13. 16-BIT DMA MODE WITH EXTERNAL LOGIC TO REDUCE PROCESSOR ACCESS TIME TO EXTERNAL RAM**

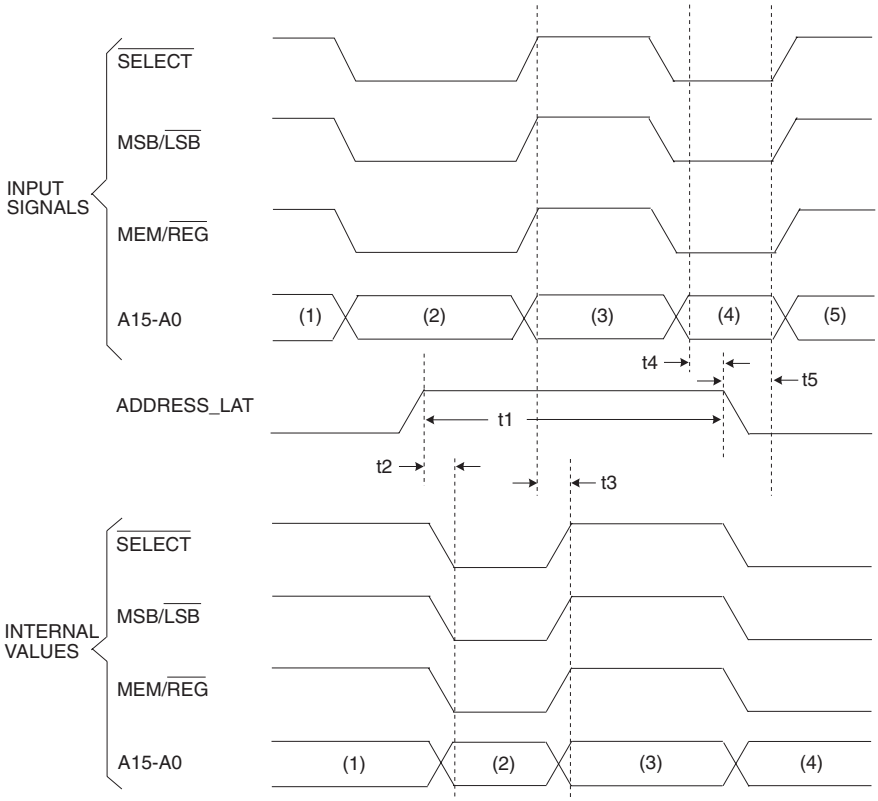



NOTES:

1. CPU D7-D0 CONNECTS TO BOTH D15-D8 AND D7-D0.
2. CPU ADDRESS LATCH SIGNAL PROVIDED BY PROCESSORS WITH MULTIPLEXED ADDRESS/DATA BUFFERS.
3. IF POLARITY_SEL = "1", THEN MSB/LSB SELECTS THE MOST SIGNIFICANT BYTE WHEN LOW, AND THE LEAST SIGNIFICANT BYTE WHEN HIGH.
   IF POLARITY_SEL = "0", THEN MSB/LSB SELECTS THE LEAST SIGNIFICANT BYTE WHEN LOW, AND THE MOST SIGNIFICANT BYTE WHEN HIGH.
4. ZERO WAIT SHOULD BE STRAPPED TO LOGIC "1" FOR NON-ZERO WAIT INTERFACE AND TO LOGIC "0" FOR ZERO WAIT INTERFACE.
5. OPERATION OF TRIGGER_SELECT INPUT IS AS FOLLOWS:
   FOR NON-ZERO WAIT INTERFACE (ZERO WAIT = "1"):
   IF TRIGGER_SEL = "1", THEN INTERNAL 16-BIT TRANSFERS ARE TRIGGERED BY THE MOST SIGNIFICANT BYTE TRANSFER READ ACCESSES AND BY THE LEAST SIGNIFICANT BYTE TRANSFER FOR WRITE ACCESSES.
   IF TRIGGER_SEL = "0", THEN INTERNAL 16-BIT TRANSFERS ARE TRIGGERED BY THE LEAST SIGNIFICANT BYTE TRANSFER FOR READ ACCESSES AND BY THE MOST SIGNIFICANT BYTE TRANSFER FOR WRITE ACCESSES.
   FOR ZERO WAIT INTERFACE (ZERO WAIT = "0"):
   IF TRIGGER_SEL = "1", THEN INTERNAL 16-BIT TRANSFERS ARE TRIGGERED BY THE LEAST SIGNIFICANT BYTE TRANSFER, FOR BOTH READ AND WRITE ACCESSES.
   IF TRIGGER_SEL = "0", THEN INTERNAL 16-BIT TRANSFERS ARE TRIGGERED BY THE MOST SIGNIFICANT BYTE TRANSFER, FOR BOTH READ AND WRITE ACCESSES.
6. CPU ACKNOWLEDGE PROCESSOR INPUT ONLY FOR NON-ZERO WAIT TYPE OF INTERFACE.

Please See Appendix G in the ACE User's Guide for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode.

**FIGURE 14. 8-BIT BUFFERED MODE**




Notes for FIGURE 15 and associated table.

1. Applicable to buffered mode only. ADDRESS, $\overline{\text{SELECT}}$ AND MEM/$\overline{\text{REG}}$ latches are always transparent in the transparent mode of operation.
2. Latches are transparent when ADDR_LAT is high. Internal values do not update when ADDR_LAT is low.
3. MSB/LSB input signal is applicable to 8-bit mode only (16/8 input = logic “0”). MSB/LSB input is a “don’t care” for 16-bit operation.

## FIGURE 15. ADDRESS LATCH TIMING

**TABLE FOR FIGURE 15. ADDRESS LATCH TIMING**

| REF | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| t1 | ADDR_LAT pulse width | 20 | | | ns |
| t2 | ADDR_LAT high delay to internal signals valid | | | 10 | ns |
| t3 | Propagation delay from external input signals to internal signals valid | | | 10 | ns |
| t4 | Input setup time prior to falling edge of ADDR_LAT | 10 | | | ns |
| t5 | Input hold time following falling edge of ADDR_LAT | 20 | | | ns |

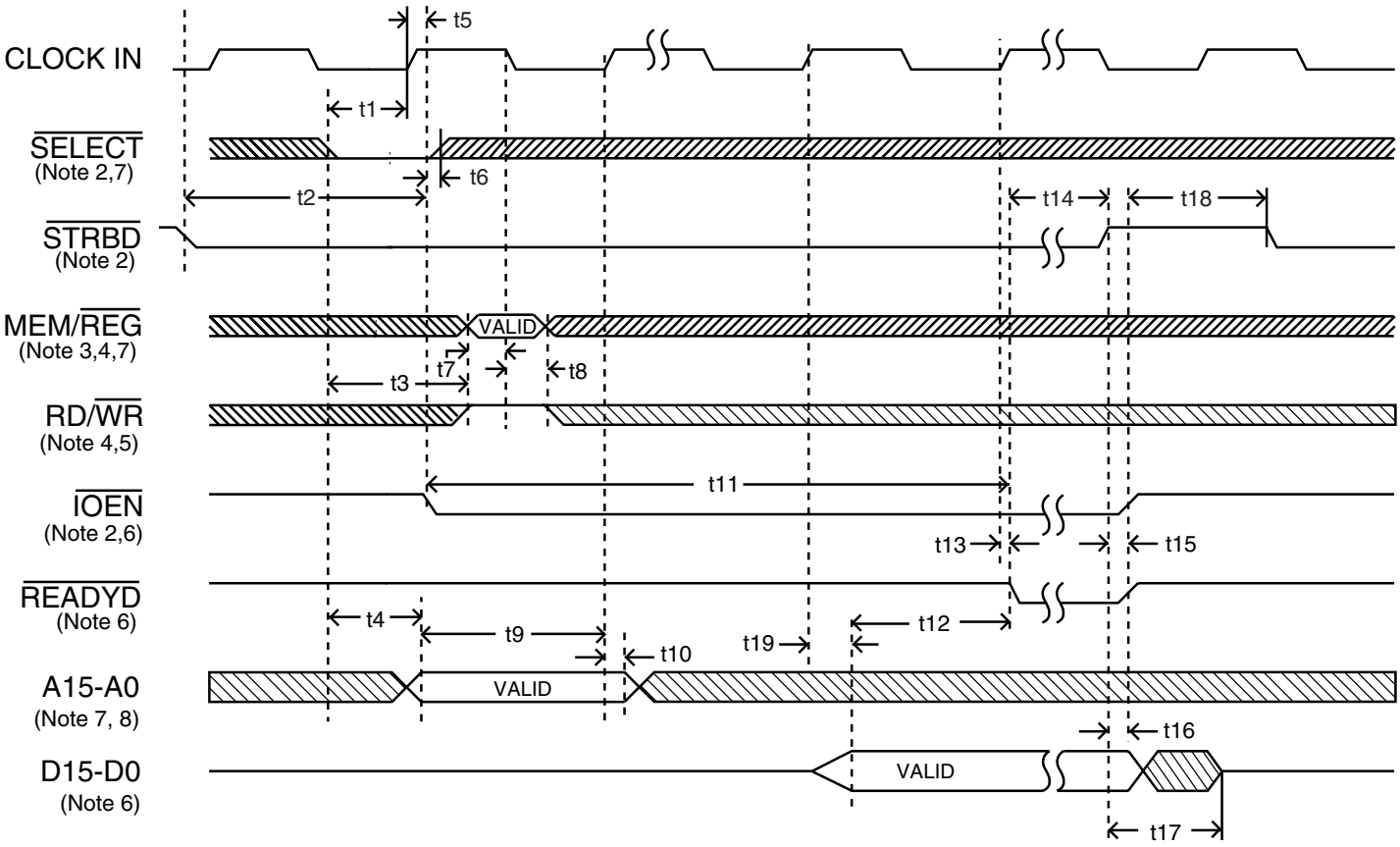



**FIGURE 16. CPU READING RAM (SHOWN FOR 16-BIT, BUFFERED, NONZERO WAIT MODE, UNCONTENDED ACCESS)**

| TABLE FOR FIGURE 16. CPU READING RAM OR REGISTERS (SHOWN FOR 16-BIT, BUFFERED, NONZERO WAIT MODE) | | | | | | |
|---|---|---|---|---|---|---|
| REF | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTE REFERENCE |
| t1 | SELECT and STRBD low setup time prior to clock rising edge | 15 | | | ns | note 2 |
| t2 | STRBD low delay to IOEN low (uncontended access @ 16 MHz) | | | 170 | ns | notes 2, 6 |
| t2 | STRBD low delay to IOEN low (contended access @ 16 MHz) | | | 5.3 | µs | notes 2, 6 |
| t2 | STRBD low delay to IOEN low (uncontended access @ 12 MHz) | | | 211.6 | ns | notes 2, 6 |
| t2 | STRBD low delay to IOEN low (contended access @ 12 MHz) | | | 7.05 | µs | notes 2, 6 |
| t3 | MEM/REG, RD/WR setup time following STRBD low(@ 16 MHz) | | | 70 | ns | |
| t3 | MEM/REG, RD/WR setup time following STRBD low(@ 12 MHz) | | | 100 | ns | |
| t4 | Address valid setup time following STRBD low (@ 16 MHz) | | | 110 | ns | |
| t4 | Address valid setup time following STRBD low (@ 12 MHz) | | | 150 | ns | |
| t5 | CLOCK IN rising edge delay to IOEN falling edge | | | 30 | ns | |
| t6 | SELECT hold time following IOEN falling | 0 | | | ns | note 2 |
| t7 | MEM/REG, RD/WR setup time prior to CLOCK IN falling edge | 10 | | | ns | notes 3, 4, 5 |
| t8 | MEM/REG, RD/WR hold time prior to CLOCK IN falling edge | 25 | | | ns | notes 3, 4, 5 |
| t9 | Address valid setup time prior to CLOCK IN rising edge | 10 | | | ns | |
| t10 | Address hold time following CLOCK IN rising edge | 25 | | | ns | note 9 |
| t11 | IOEN falling delay to READYD falling (reading RAM @ 16 MHz) | 420 | 437.5 | 455 | ns | note 6 |
| t11 | IOEN falling delay to READYD falling (reading RAM @ 12 MHz) | 565 | 583.3 | 600 | ns | note 6 |
| t11 | IOEN falling delay to READYD falling (reading registers @ 16 MHz) | 170 | 187.5 | 205 | ns | note 6 |
| t11 | IOEN falling delay to READYD falling (reading registers @ 12 MHz) | 230 | 250 | 265 | ns | note 6 |
| t12 | Output Data valid prior to READYD falling (@ 16 MHz) | 33 | | | ns | note 6 |
| t12 | Output Data valid prior to READYD falling (@ 12 MHz) | 54 | | | ns | note 6 |
| t13 | CLOCK IN rising edge delay to READYD falling | | | 30 | ns | note 6 |
| t14 | READYD falling to STRBD rising release time | | | ∞ | ns | |
| t15 | STRBD rising edge delay to IOEN rising edge and READYD rising edge | | | 40 | ns | note 6 |
| t16 | Output Data hold time following STRBD rising edge | 0 | | | ns | |
| t17 | STRBD rising delay to output Data tri-state | | | 40 | ns | |
| t18 | STRBD high hold time from READYD rising | 0 | | | ns | |
| t19 | CLOCK_IN rising edge delay to output data valid | | | 50 | ns | |

Notes for FIGURE 16 and associated table.

1. For the 16-bit buffered configuration, the inputs TRIGGER_SEL and MSB/LSB may be connected to +5 V or GND. For the nonzero wait interface ZEROWAIT, must be connected to logic “1”.

2. SELECT and STRBD may be tied together. IOEN goes low on the second rising CLK edge when STRBD is sampled low, provided SELECT is also sampled low on that CLK edge and the BU-63825/925’s protocol/memory management logic is not accessing internal RAM. If the protocol/memory management logic is accessing internal RAM, SELECT is latched on the second rising CLK edge and transfer will begin once protocol/memory management access is complete. If SELECT is sampled high on the second rising CLK edge, no transfer will take place. IOEN will not drop.

3. MEM/REG must be presented high for memory access, low for register access.

4. MEM/REG and RD/WR are buffered transparently until the first falling edge of CLK after IOEN goes low. After this CLK edge, MEM/REG and RD/WR become latched internally.

5. The logic sense for RD/WR in the diagram assumes that POLARITY_SEL is connected to logic "1". If POLARITY_SEL is connected to logic "0", RD/WR must be asserted low to read.

6. The timing for IOEN, READYD and D15-D0 assumes a 50 pf load. For loading above 50 pf, the validity of IOEN, READYD, and D15-D0 is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.

7. Timing for A15-A0 assumes ADDR-LAT is connected to logic “1”. Refer to Address Latch timing for additional details.

8. Internal RAM is accessed by A13 through A0. Registers are accessed by A4 through A0.

9. The address bus A15-A0 is internally buffered transparently until the first rising edge of CLK after IOEN, goes low. After this CLK edge, A15-A0 become latched internally.

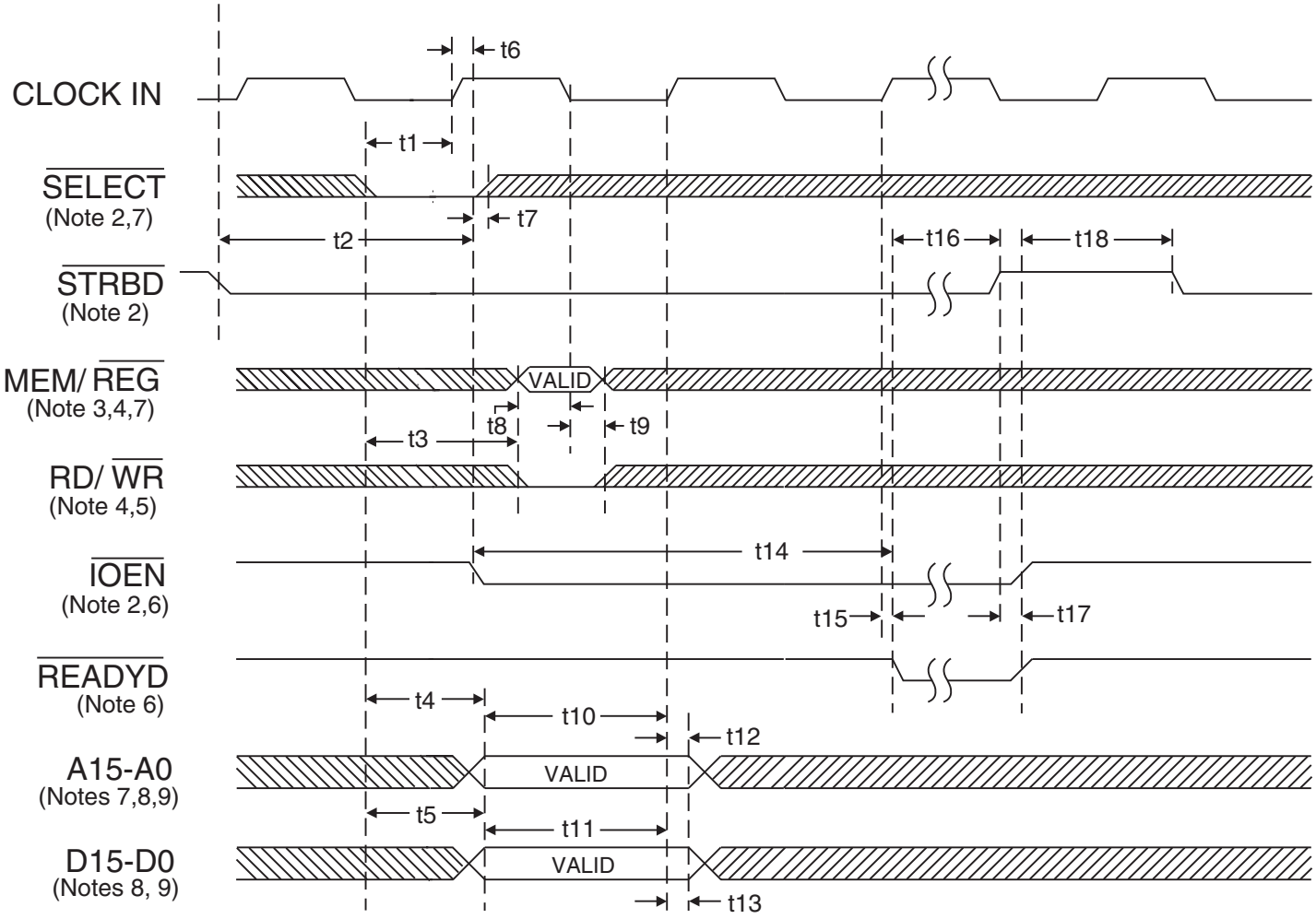



**FIGURE 17. CPU WRITING RAM (SHOWN FOR 16-BIT, BUFFERED, NONZERO WAIT MODE, UNCONTENDED ACCESS)**

| TABLE FOR FIGURE 17. CPU WRITING RAM OR REGISTERS (SHOWN FOR 16-BIT, BUFFERED, NONZERO WAIT MODE) | | | | | | |
|---|---|---|---|---|---|---|
| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTE REFERENCE |
| t1 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to clock in rising edge | 15 | | | ns | note 2 |
| t2 | $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (uncontended access @ 16 MHz) | | | 170 | ns | notes 2, 6 |
| t2 | $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (contended access @ 16 MHz) | | | 5.3 | µs | notes 2, 6 |
| t2 | $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (uncontended access @ 12 MHz) | | | 211.6 | ns | |
| t2 | $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (contended access @ 12 MHz) | | | 7.05 | µs | |
| t3 | MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ setup time following $\overline{\text{STRBD}}$ (@ 16 MHz) | | | 70 | ns | |
| t3 | MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ setup time following $\overline{\text{STRBD}}$ (@ 12 MHz) | | | 100 | ns | |
| t4 | Address valid setup following $\overline{\text{STRBD}}$ low (@ 16 MHz) | | | 110 | ns | |
| t4 | Address valid setup following $\overline{\text{STRBD}}$ low (@ 12 MHz) | | | 150 | ns | |
| t5 | Input Data valid setup following $\overline{\text{STRBD}}$ low (@ 16 MHz) | | | 110 | ns | |
| t5 | Input Data valid setup following $\overline{\text{STRBD}}$ low (@ 12 MHz) | | | 150 | ns | |
| t6 | CLOCK IN rising edge delay to $\overline{\text{IOEN}}$ falling edge | | | 30 | ns | |
| t7 | $\overline{\text{SELECT}}$ hold time following $\overline{\text{IOEN}}$ falling edge | 0 | | | ns | note 2 |
| t8 | MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time prior to CLOCK IN falling edge | 10 | | | ns | notes 3, 4, 5 |
| t9 | MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ hold time following CLOCK IN falling edge | 25 | | | ns | notes 3, 4, 5 |
| t10 | Address valid setup prior to CLOCK IN rising edge | 10 | | | ns | |
| t11 | Input Data valid setup prior to CLOCK IN rising edge | 10 | | | ns | |
| t12 | Address hold time following CLOCK IN rising edge | 25 | | | ns | note 9 |
| t13 | Input Data valid hold time following CLOCK IN rising edge | 25 | | | ns | note 9 |
| t14 | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@ 16 MHz) | 170 | 187.5 | 205 | ns | note 6 |
| t14 | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@ 12 MHz) | 230 | 250 | 265 | ns | note 6 |
| t15 | CLOCK IN rising edge delay to $\overline{\text{READYD}}$ falling edge | | | 30 | ns | |
| t16 | $\overline{\text{READYD}}$ falling to $\overline{\text{STRBD}}$ rising release time | | | ∞ | ns | |
| t17 | $\overline{\text{STRBD}}$ rising delay to $\overline{\text{IOEN}}$ rising, $\overline{\text{READYD}}$ rising | | | 40 | ns | |
| t18 | $\overline{\text{STRBD}}$ high hold time following $\overline{\text{READYD}}$ rising | 0 | | | ns | |

Notes for FIGURE 17 and associated table.

1. For the 16-bit buffered configuration, the inputs TRIGGER_SEL and MSB/LSB may be connected to +5 V or GND. For the nonzero wait interface, $\overline{\text{ZEROWAIT}}$ must be connected to logic “1.”

2. $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ may be tied together. $\overline{\text{IOEN}}$ goes low on the second rising CLK edge when $\overline{\text{STRBD}}$ is sampled low, provided $\overline{\text{SELECT}}$ is also sampled low on that CLK edge and the BU-63825/925's protocol/memory management logic is not accessing internal RAM. If the protocol/memory management logic is accessing internal RAM, $\overline{\text{SELECT}}$ is latched on the second rising CLK edge and transfer will begin once protocol/memory management access is complete. If $\overline{\text{SELECT}}$ is sampled high on the second rising CLK edge, no transfer will take place. $\overline{\text{IOEN}}$ will not drop.

3. MEM/$\overline{\text{REG}}$ must be presented high for memory access, low for register access.

4. MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ are buffered transparently until the first falling edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ become latched internally.

5. The logic sense for RD/$\overline{\text{WR}}$ in the diagram assumes that POLARITY_SEL is connected to logic “1”. If POLARITY_SEL is connected to logic "0", RD/$\overline{\text{WR}}$ must be asserted high to read.

6. The timing for the $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ outputs assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.

7. Timing for A15-A0 assumes ADDR-LAT is connected to logic “1”. Refer to Address Latch timing for additional details.

8. Internal RAM is accessed by A13 through A0. Registers are accessed by A4 through A0.

9. The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until the first rising edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, A15-A0 and D15-D0 become latched internally.

## INTERFACE TO MIL-STD-1553 BUS

FIGURE 18 illustrates the interface from the various versions of the Sp'ACE II series terminals to a 1553 bus. The figure also indicates connections for both direct (short stub) and transformer (long stub) coupling, plus the peak-to-peak voltage levels that appear at various points (when transmitting).

TABLE 33 lists the characteristics of the required isolation transformers for the various Sp'ACE II terminals, the DDC and Beta Transformer Technology Corporation corresponding part number, and the MIL (DESC) drawing number (if applicable). Beta Transformer Technology Corporation is a direct subsidiary of DDC.

For both coupling configurations, the isolation transformer is the transformer that interfaces directly to the Sp'ACE II component. For the transformer (long stub) coupling configuration, the transformer that interfaces the stub to the bus is the coupling transformer. The turns ratio of the isolation transformer varies, depending upon the peak-to-peak output voltage of the specific Sp'ACE II terminal.

The transmitter voltage of each model of the BU-63825 varies directly as a function of the power supply voltage. The turns ratios of the respective transformers will yield a secondary voltage of approximately 28 volts peak-to-peak on the outer taps (used for direct coupling) and 20 volts peak-to-peak on the inner taps (used for stub coupling).

In accordance with MIL-STD-1553B, the turns ratio of the coupling transformer is 1.0 to 1.4. Both coupling configurations require an isolation resistor to be in series with each leg connecting to the 1553 bus; this protects the bus against short circuit conditions in the transformers, stubs, or terminal components.

**TABLE 33. ISOLATION TRANSFORMER GUIDE**

| SP'ACE II PART NUMBER | TURNS RATIO | | RECOMMENDED XFORMER | |
|---|---|---|---|---|
| | DIRECT COUPLED | XFORMER COUPLED | PLUG-IN | SURFACE MOUNT |
| BU-63825X1 | 1.4:1 | 2:1 | BUS-25679, B-2203, M21038/27 -02 | B-2387 M21038/27 -12, M21038/27 -17 LPB-5002 LPB-5009 LPB-6002 LPB-6009 |
| BU-63825X2 | 1:0.83 | 1:0.67 | BUS-29854 | LPB-5001 LPB-5008 LPB-6001 LPB-6008 |
| | 1.25:1 (Note 5) | | B-2204, M21038/27 -03 | B-2388 M21038/27 -13, B-2344, M21038/27 -18 |
| BU-63825 X3/X6 | 1:2.5 | 1:1.79 | See TABLE 34 | |

Notes for TABLE 33 and FIGURE 18:

(1) Shown for one of two redundant buses that interface to the BU-63825

(2) Transmitted voltage level on 1553 bus is 6 Vp-p min, 7 Vp-p nominal, 9 Vp-p max.

(3) Required tolerance on isolation resistors is 2%. Instantaneous power dissipation (when transmitting) is approximately 0.5 W (typ), 0.8 W (max).

(4) Transformer pin numbering is correct for the DDC (e.g., BUS-25679) transformers. For the Beta transformers (e.g., B-2203) or the QPL-21038-31 transformers (e.g., M21038/27-02), the winding sense and turns ratio are mechanically the same, but with reversed pin numbering; therefore, it is necessary to reverse pins 8 and 4 or pins 7 and 5 for the Beta or QPL transformers (Note: DDC transformer part numbers begin with a BUS- prefix, while Beta transformer part numbers begin with a B- prefix).

(5) The B-2204, B-2388, and B-2344 transformers have a slightly different turns ratio on the direct coupled taps then the turns ratio of the BUS-29854 direct coupled taps. They do, however, have the same transformer coupled ratio. For transformer coupled applications, either transformer may be used. The transceiver in the BU-63825 was designed to work with a 1:0.83 ratio for direct coupled applications. For direct coupled applications, the 1.20:1 turns ration is recommended, but the 1.25:1 may be used. The 1.25:1 turns ratio will result in a slightly lower transmitter amplitude. (Approximately 3.6% lower) and a slight shift in the Sp'ACE II's receiver threshold.

## TRANSFORMER CONSIDERATIONS FOR BU-63825X3 (+5V ONLY VERSIONS)

In selecting isolation transformers to be used for the BU-63825X3 (+5V only) versions, there is a limitation on the maximum amount of leakage inductance. If this limit is exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553. In addition, an excessive leakage imbalance may result in a transformer dynamic offset that exceeds 1553 specifications.

The maximum allowable leakage inductance is 6.0 µH, and is measured as follows:

The side of the transformer that connects to the Hybrid is defined as the "primary" winding. If one side of the primary is shorted to the primary center-tap, the inductance should be measured across the "secondary" (stub side) winding. This inductance must be less than 6.0 µH. Similarly, if the other side of the primary is shorted to the primary center-tap, the inductance measured across the "secondary" (stub side) winding must also be less than 6.0 µH.

The difference between these two measurements is the "differential" leakage inductance. This value must be less than 1.0 µH.

Beta Transformer Technology Corporation (BTTC), a subsidiary of DDC, manufactures transformers in a variety of mechanical configurations with the required turns ratios of 1:2.5 direct coupled, and 1:1.79 transformer coupled. Table 33 provides a listing of many of these transformers. For further information, contact BTTC at 631-244-7393 or at www.bttc-beta.com.

**TABLE 34. BTTC TRANSFORMERS FOR USE WITH BU-63825X3/X6**

| BTTC PART NUMBER | # OF CHANNELS, CONFIGURATION | COUPLING RATIO DESCRIPTION | COUPLING RATIO (1:X) | MOUNTING | MAX HEIGHT | WIDTH (INCLUDING LEADS) | LENGTH (INCLUDING LEADS) |
|---|---|---|---|---|---|---|---|
| MLP-2005 | Single | Direct | (1:2.5) | SMT | 0.185" | 0.4" | 0.52" |
| MLP-3005 | Single | Direct | (1:2.5) | Through Hole | 0.185" | 0.4" | 0.4" |
| B-3230 (-30) # | Single | Direct | (1:2.5) | Through Hole | 0.25" | 0.35" | 0.5" |
| MLP-2205 | Single | Transformer | (1:1.79) | SMT | 0.185" | 0.4" | 0.52" |
| MLP-3205 | Single | Transformer | (1:1.79) | Through Hole | 0.185" | 0.4" | 0.4" |
| B-3229 (-29) # | Single | Transformer | (1:1.79) | Through Hole | 0.25" | 0.35" | 0.5" |
| HLP-6015 # | Single | Direct & Transformer | (1:2.5) & (1:1.79) | SMT | 0.19" | 0.63" | 1.13" |
| B-3227 (-27) # | Single | Direct & Transformer | (1:2.5) & (1:1.79) | SMT | 0.29" | 0.63" | 1.13" |
| MLP-3305 | Single | Direct & Transformer | (1:2.5) & (1:1.79) | Through Hole | 0.185" | 0.4" | 0.4" |
| B-3226 (-26) # | Single | Direct & Transformer | (1:2.5) & (1:1.79) | Through Hole | 0.25" | 0.625" | 0.625" |
| HLP-6014 # | Single | Direct & Transformer | (1:2.5) & (1:1.79) | Flat Pack | 0.19" | 0.63" | 1.13" |
| B-3231 (-31) # | Single | Direct & Transformer | (1:2.5) & (1:1.79) | Flat Pack | 0.29" | 0.63" | 1.13" |
| DSS-2005 | Dual (Side-by-Side) | Direct | (1:2.5) | SMT | 0.13" | 0.72" | 0.96" |
| DSS-2205 | Dual (Side-by-Side) | Transformer | (1:1.79) | SMT | 0.13" | 0.72" | 0.96" |
| DSS-1005 | Dual (Side-by-Side) | Direct & Transformer | (1:2.5) & (1:1.79) | SMT | 0.165" | 0.72" | 0.96" |
| TSM-2005 | Dual (Stacked) | Direct | (1:2.5) | SMT | 0.32" | 0.4" | 0.52" |
| TSM-2205 | Dual (Stacked) | Transformer | (1:1.79) | SMT | 0.32" | 0.4" | 0.52" |
| TST-9117 # | Dual (Stacked) | Direct & Transformer | (1:2.5) & (1:1.79) | SMT | 0.335" | 1.125" | 1.125" |
| TST-9107 # | Dual (Stacked) | Direct & Transformer | (1:2.5) & (1:1.79) | Through Hole | 0.335" | 0.625" | 0.625" |
| TST-9127 # | Dual (Stacked) | Direct & Transformer | (1:2.5) & (1:1.79) | Flat Pack | 0.335" | 0.625" | 0.625" |

Notes:
1. All Transformers in the table above can be used with BU-6XXXXX3/6 (1553B transceivers).
2. Transformers identified with "#" in the table above are not recommended for use with the BU-6XXXXX4 (McAir-Compatable transceivers)

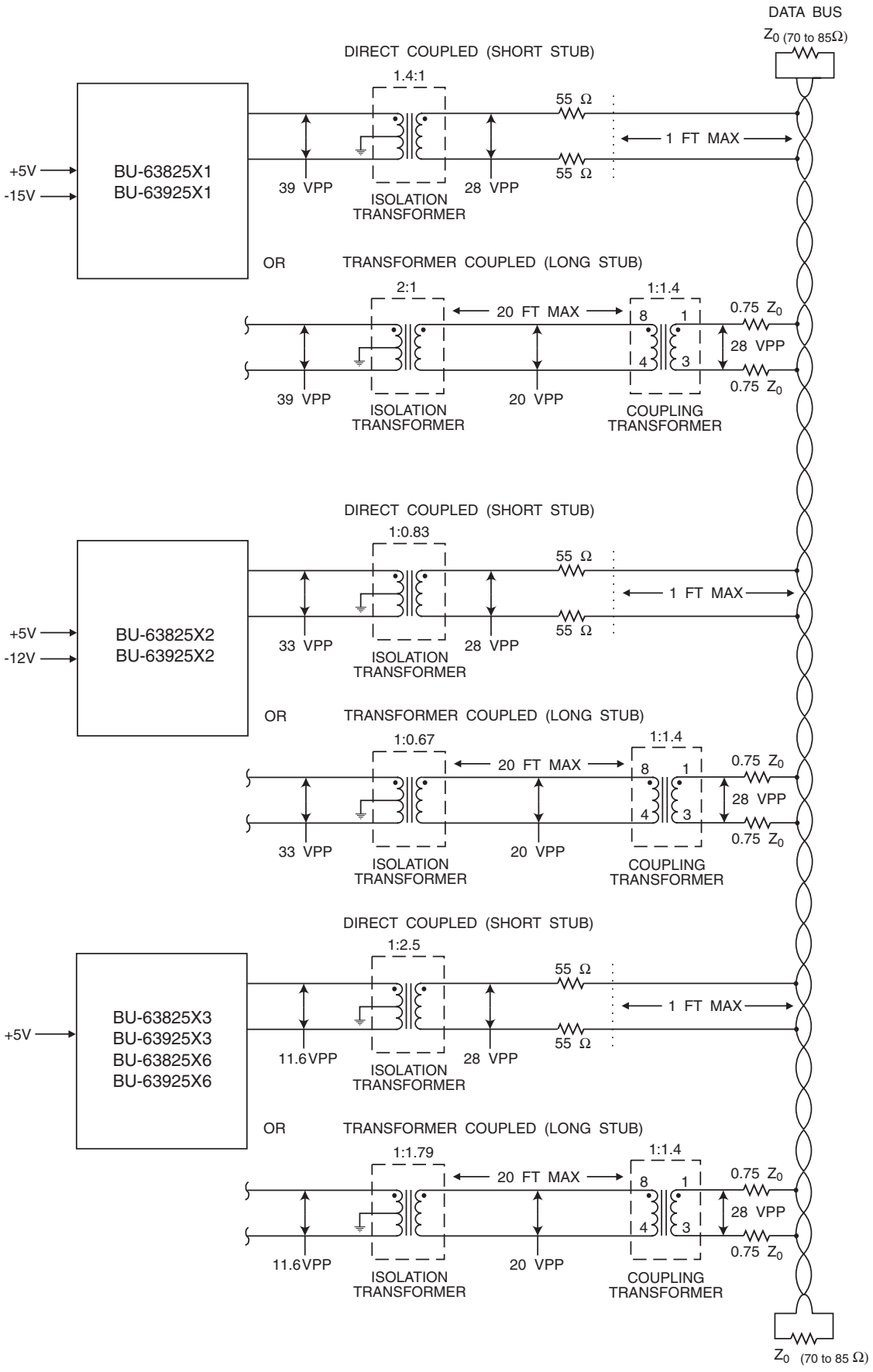



**FIGURE 18. INTERFACE TO A 1553 BUS**

| TABLE 35. SIGNAL DESCRIPTIONS, PROCESSOR/MEMORY INTERFACE AND CONTROL (15) | | |
|---|---|---|
| **SIGNAL NAME** | **PIN** | **DESCRIPTION** |
| TRANSPARENT/ BUFFERED (I) | 64 | Used to select between the Transparent/ DMA mode (when strapped to logic 1) and the Buffered mode (when strapped to logic 0) for the host processor interface. (Please see Appendix G in the ACE User's Guide for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode) |
| STRBD (I) | 4 | Strobe Data. Used with SELECT to initiate and control the data transfer cycle between the host processor and the BU-63825. |
| SELECT (I) | 3 | Generally connected to a CPU address decoder output to select the BU-63825 for a transfer to/from either RAM or register. May be tied to STRBD |
| MEM/REG (I) | 5 | Memory/Register. Generally connected to either a CPU address line or address decoder output. Selects between memory access MEM/REG = 1 (or register access MEM/REG = 0 ). |
| RD/WR (I) | 6 | Read/Write. For host processor access, selects either reading or writing. In the 16-bit buffered mode, if polarity select is logic (0), then RD/WR is low (logic 0 ) for read accesses and high (logic 1) for write accesses. If polarity select is logic 1 or the configuration of the interface is a mode other than 16-bit buffered mode, then RD/WR is high (logic 1 ) for read accesses and low (logic 0) for write accesses. |
| IOEN (O) | 67 | Tri-state control for external address and data buffers. Generally not needed in the buffered mode. When low, external buffers should be enabled to allow the host processor access to the BU-63825's RAM and registers. |
| READYD (O) | 66 | Handshake output to host processor. For a nonzero wait state read access, signals that data is available to be read on D15 through D0. For a nonzero wait state write cycle, signals the completion of data transfer to a register or RAM location. In the buffered zero wait state mode, active high output signal (following the rising edge of STRBD used to indicate the latching of address and data (write only) and that an internal transfer between the address/data latches and the RAM/registers is on-going. |
| INT (O) | 65 | Interrupt request output. If the LEVEL/PULSE interrupt bit (bit 3) of Configuration Register #2 is low, a negative pulse of approximately 500 ns in width is output on INT. If bit 3 is high, a low level interrupt request output will be asserted on INT. |
| DTREQ (O) /16/8 (I) | 31 | Data Transfer Request or 16-bit/8-bit Transfer Mode Select. In transparent mode, active low output signal used to request access to the processor interface bus (address, data, and control buses). In buffered mode, input signal used to select between the 16-bit data transfer mode (16/8 = logic 1) and the 8 bit data transfer mode (16/8 = logic 0). (Please see Appendix G in the ACE User's Guide for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode) |
| DTGRT (I) /MSB/LSB (I) | 26 | Data Transfer Grant or Most Significant Byte/Least Significant Byte. In transparent mode, active low input signal asserted, in response to the DTREQ output, to indicate that access to the processor buses has been granted to the BU-63825. In 8-bit buffered mode, input signal used to indicate which byte is being transferred (MSB or LSB). The POLARITY_SEL input controls the logic sense of MSB/LSB. (Note: only the 8-bit buffered mode uses MSB/LSB.) See description of POLARITY_SEL signal. |
| DTACK (O)/ POLARITY_SEL (I) | 32 | Data Transfer Acknowledge or Polarity Select. In transparent mode, active low output signal used to indicate acceptance of the processor interface bus in response to a data transfer grant (DTGR). In 16-bit buffered mode (TRANSPARENT/ BUFFERED = logic 0 and 16/8 = logic 1), input signal used to control the logic sense of the RD/WR signal. When POLARITY_SEL is logic 1, RD/WR must be asserted high (logic 1) for a read operation and low (logic 0) for a write operation. When POLARITY_SEL is logic 0, RD/WR must be asserted low (logic 0) for a read operation and high (logic 1) for a write operation. In 8-bit buffered mode (TRANSPARENT/BUFFERED = logic 0 and 16/8 = logic 0), input signal used to control the logic sense of the MSB/LSB signal. When POLARITY_SEL is logic 0, MSB/LSB must be asserted low (logic 0) to indicate the transfer of the least significant byte and high (logic 1) to indicate the transfer of the most significant byte. When POLARITY_SEL is logic 1, MSB/LSB must be asserted high (logic 1) to indicate the transfer of the least significant byte and low (logic 0) to indicate the transfer of the most significant byte. |
| MEMENA-OUT (O) | 28 | Memory Enable Output. Asserted low during both host processor and 1553 protocol/memory management memory transfer cycles. Used as a memory chip select (CS) signal for external RAM in the transparent mode. |
| MEMENA-IN (I) /TRIGGER_SEL (I) | 33 | Memory Enable Input or Trigger Select. In transparent mode, MEMENA_IN is an active low Chip Select (CS) input to the 16K x 16 of internal shared RAM. When only using internal RAM, connect directly to MEMENA_OUT or ground. In 8-bit buffered mode, the input signal (TRIGGER_SEL) indicates the order of byte pairs transferred to or from the BU-63825 by the host processor. This signal has no operation (can be N/C) in the 16-bit buffered mode. In the 8-bit buffered mode, TRIGGER_SEL should be asserted high (logic 1) if the byte order for both read operations and write operations is MSB followed by LSB. TRIGGER_SEL should be asserted low (logic 0) if the byte order for both read operations and write operations is LSB followed by MSB. |
| MEMOE (O)/ ADDR_ LAT (I) | 29 | Memory Output Enable or Address Latch. In transparent mode, MEMOE output will be used to enable data outputs for external RAM read cycles (normally connected to the OE signal on external RAM chips). In buffered mode, ADDR_LAT input will be used to configure the internal address latches in latched mode (when low) or transparent mode (when high). |
| MEMWR (O) /ZERO_ WAIT (I) | 30 | Memory Write or Zero Wait State. In transparent mode, active low output signal (MEMWR) will be asserted low during memory write transfers to strobe data into internal or external RAM (normally connected to the WR signal on external RAM chips). In buffered mode, input signal (ZERO WAIT) will be used to select between the zero wait mode (ZERO WAIT= logic 0) and the nonzero wait mode (ZERO WAIT = logic 1). (Please see Appendix G in the ACE User's Guide for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode) |

| TABLE 36. SIGNAL DESCRIPTIONS, MISCELLANEOUS (5) | | |
|---|---|---|
| **SIGNAL NAME** | **PIN** | **DESCRIPTION** |
| CLOCK IN (I) | 19 | 16MHz (or 12MHz) clock input. |
| $\overline{\text{MSTCLR}}$ (I) | 7 | Master Clear. Negative true Reset input, normally asserted low following power turn-on. Requires a minimum 100ns negative pulse to reset all internal logic to its “power turn-on” state. |
| $\overline{\text{INCMD}}$ (O) | 45 | In Command. In BC mode, asserted low throughout processing cycle for each message. In RT mode or Message Monitor mode, asserted low following receipt of Command Word and kept low until completion of current message sequence. In Word Monitor mode, goes low following MONITOR START command, kept low while monitor is on-line, goes high following RESET command. |
| $\overline{\text{SSFLAG}}$ (I)/ EXT_ TRIG (I) | 27 | Subsystem Flag or External Trigger input. In the Remote Terminal mode, asserting this input will set the Subsystem Flag bit in the BU-63825’s RT Status Word. A low on the $\overline{\text{SSFLAG}}$ input overrides a logic “1” of the respective bit (bit 8) of Configuration Register #1. In the Bus Controller mode, an enabled external BC Start option (bit 7 of Configuration Register #1) and a low-to-high transition on this input will issue a BC Start command, starting execution of the current BC frame. In the Word Monitor mode, an enabled external trigger (bit 7 of Configuration Register #1) and a low-to-high transition on this input will issue a monitor trigger. |
| TAG_CLK (I) | 63 | External Time Tag Clock input. Use may be designated by bits 7, 8, and 9 of Configuration Register #2. When used it increments the internal Time Tag Register/Counter. If not used, should be connected to +5V or ground. |

| TABLE 37. SIGNAL DESCRIPTIONS, RT ADDRESS (6) | | |
|---|---|---|
| **SIGNAL NAME** | **PIN** | **DESCRIPTION** |
| RTAD4 (MSB) (I) | 43 | Remote Terminal Address Inputs |
| RTAD3 (I) | 42 | |
| RTAD2 (I) | 41 | |
| RTAD1 (I) | 40 | |
| RTAD0 (LSB) (I) | 39 | |
| RTADP (I) | 44 | Remote Terminal Address Parity. Must provide odd parity sum with RTAD4-RTAD0 in order for the RT to respond to non-broadcast commands. |

| TABLE 38. SIGNAL DESCRIPTIONS, POWER AND GROUND (8) | | | | | |
|---|---|---|---|---|---|
| **SIGNAL NAME** | **PIN** | **PIN** | **PIN** | **PIN** | **DESCRIPTION** |
| | **X0*** | **X1/X2*** | **X3*** | **X6*** | |
| +5V LOGIC | 54 | 54 | 54 | 54 | Logic +5V Supply |
| GND | 18 | 18 | 18 | 18 | Ground |
| -VA | - | 70 | - | - | CH. A -15V(-12V) Supply |
| +5VA | - | 68 | 68 | 68 | CH. A +5V Supply |
| GND | - | 69 | 69 | 69 | Ground |
| -VB | - | 36 | - | - | CH. B -15V(-12V) Supply |
| +5VB | - | 38 | 38 | 38 | CH. B +5V Supply |
| GND | - | 37 | 37 | 37 | Ground |

Note: *Pin X0, X1/X2, X3, X6 refer to package option(X) and Voltage Transceiver option (0, 1, 2, 3, 6). See ordering information.

| TABLE 39. SIGNAL DESCRIPTIONS, 1553 ISOLATION TRANSFORMER INTERFACE (4) | | | | | |
|---|---|---|---|---|---|
| SIGNAL NAME | PIN X0* | PIN X1/X2* | PIN X3* | PIN X6* | DESCRIPTION |
| TX/RX-A (I/O) | - | 1 | 1 | 1 | Analog Transmit/Receive Input/Outputs. Connect directly to 1553 isolation transformers. |
| $\overline{\text{TX/RX}}$-A (I/O) | - | 2 | 2 | 2 | |
| TX/RX-B (I/O) | - | 34 | 34 | 34 | |
| $\overline{\text{TX/RX}}$-B (I/O) | - | 35 | 35 | 35 | |

Note: *Pin X0, X1/X2, X3, X6 refer to package option(X) and Voltage Transceiver option (0, 1, 2, 3, 6). See ordering information.

| TABLE 40. SIGNAL DESCRIPTIONS, ADDRESS BUS (16) | | |
|---|---|---|
| SIGNAL NAME | PIN | DESCRIPTION |
| A15 (MSB) | 8 | 16-bit bidirectional address bus. In both the buffered and transparent modes, the host CPU accesses the BU-63825 registers and 16K words of internal RAM by A13 through A0. The host CPU performs register selection by A4 through A0. In the buffered mode, A15-A0 are inputs only. In the transparent mode, A15-A0 are inputs during CPU accesses and drive outward (towards the CPU) when the 1553 protocol/memory management logic accesses up to 64K x 16 of external RAM. The address bus drives outward only in the transparent mode when the signal $\overline{\text{DTACK}}$ is low (indicating that the 63825 has control of the processor interface bus) and $\overline{\text{IOEN}}$ is high (indicating that this is not a CPU access). Most of the time, including immediately after power turn-on RESET, the A15-A0 outputs will be in their disabled (high impedance) state. |
| A14 | 9 | |
| A13 | 10 | |
| A12 | 11 | |
| A11 | 12 | |
| A10 | 13 | |
| A09 | 14 | |
| A08 | 15 | |
| A07 | 16 | |
| A06 | 17 | |
| A05 | 20 | |
| A04 | 21 | |
| A03 | 22 | |
| A02 | 23 | |
| A01 | 24 | |
| A00 | 25 | |

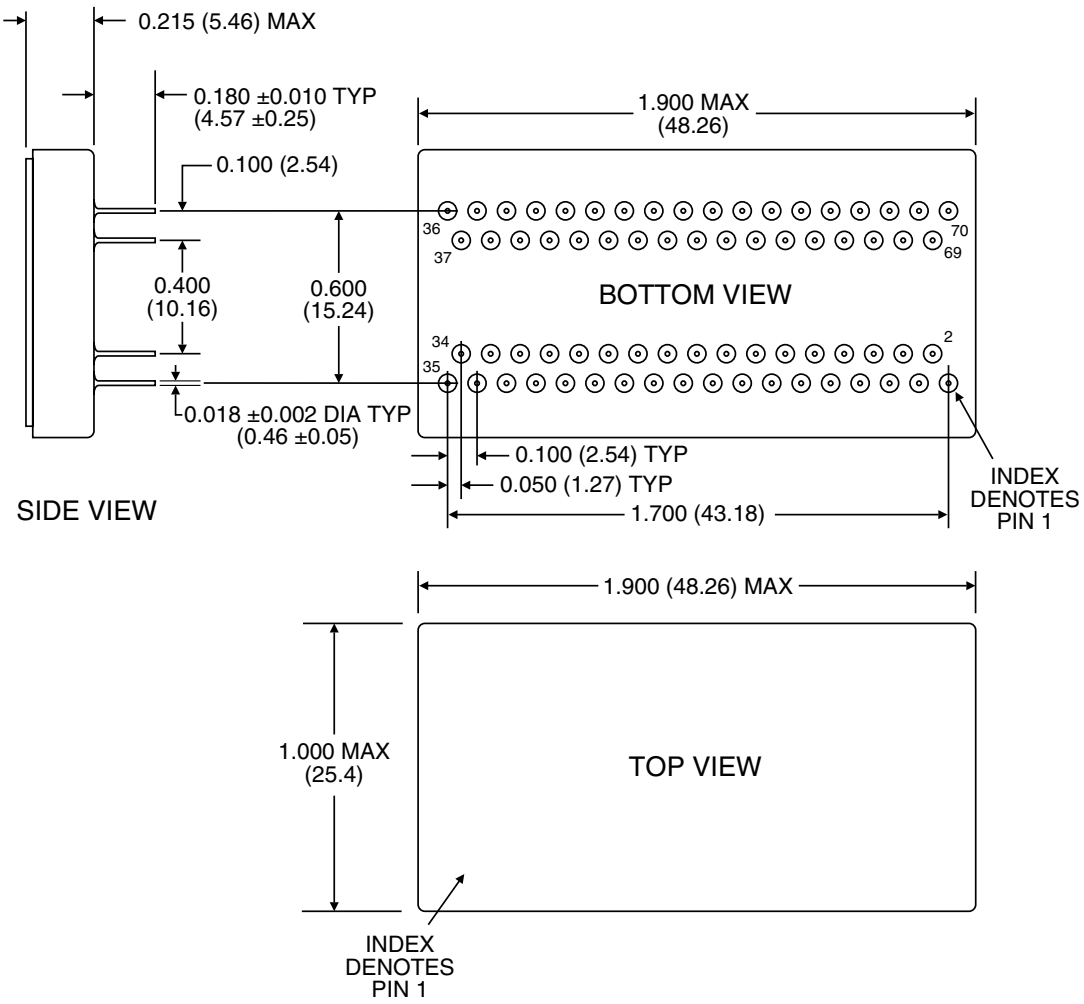
| TABLE 41. SIGNAL DESCRIPTIONS, DATA BUS (16) | | |
|---|---|---|
| **SIGNAL NAME** | **PIN** | **DESCRIPTION** |
| D15 (MSB) | 62 | 16-bit bidirectional data bus. This bus interfaces the host processor to the internal registers and 16K words of RAM. In addition, in the transparent mode, this bus allows data transfers to take place between the internal protocol/memory management logic and up to 64K x 16 of external RAM. Most of the time, the outputs for D15 through D0 are in their high impedance state. They drive outward in the buffered or transparent mode when the host CPU reads the internal RAM or registers. Or, in the transparent mode, when the protocol/memory management logic is accessing (either reading or writing) internal RAM or writing to external RAM. |
| D14 | 61 | |
| D13 | 60 | |
| D12 | 59 | |
| D11 | 58 | |
| D10 | 57 | |
| D09 | 56 | |
| D08 | 55 | |
| D07 | 53 | |
| D06 | 52 | |
| D05 | 51 | |
| D04 | 50 | |
| D03 | 49 | |
| D02 | 48 | |
| D01 | 47 | |
| D00 | 46 | |

| TABLE 42. SIGNAL DESCRIPTIONS, TRANSMITTER/RECEIVERS (14) | | | | | |
|---|---|---|---|---|---|
| **SIGNAL NAME** | **PIN X0*** | **PIN X1/X2*** | **PIN X3*** | **PIN X6*** | **DESCRIPTION** |
| TXA | 70 | - | - | - | Digital manchester biphase transmit data outputs. Connect directly to corresponding inputs to a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver. |
| $\overline{\text{TXA}}$ | 69 | - | - | - | |
| TXB | 38 | - | - | - | |
| $\overline{\text{TXB}}$ | 37 | - | - | - | |
| RXA | 1 | - | - | - | Digital manchester biphase receive data inputs. Connect directly to corresponding outputs of a MIL-STD-1553 or MIL-STD-1773 transceiver. |
| $\overline{\text{RXA}}$ | 2 | - | - | - | |
| RXB | 35 | - | - | - | |
| $\overline{\text{RXB}}$ | 34 | - | - | - | |
| TX_INH_A_IN | - | - | - | 70 | Transmitter inhibit inputs for the Channel A and Channel B MIL-STD-1553 transmitters. For normal operation, these inputs should be connected to logic "0". To force a shutdown of Channel A and/or Channel B, a value of logic "1" should be applied to the respective TX_INH input. |
| TX_INH_B_IN | - | - | - | 36 | |
| TX_INH_A_OUT | 68 | - | - | - | Digital Transmit Inhibit outputs. Connect to TX_INH_OUT inputs of a MIL-STD-1553 transceiver. Asserted high to inhibit when not transmitting on the respective bus. |
| TX_INH_B_OUT | 36 | - | - | - | |
| N/C | - | - | 36 | - | No User Connections |
| N/C | - | - | 70 | - | |

Note: *Pin X0, X1/X2, X3, X6 refer to package option(X) and Voltage Transceiver option (0, 1, 2, 3, 6). See ordering information.

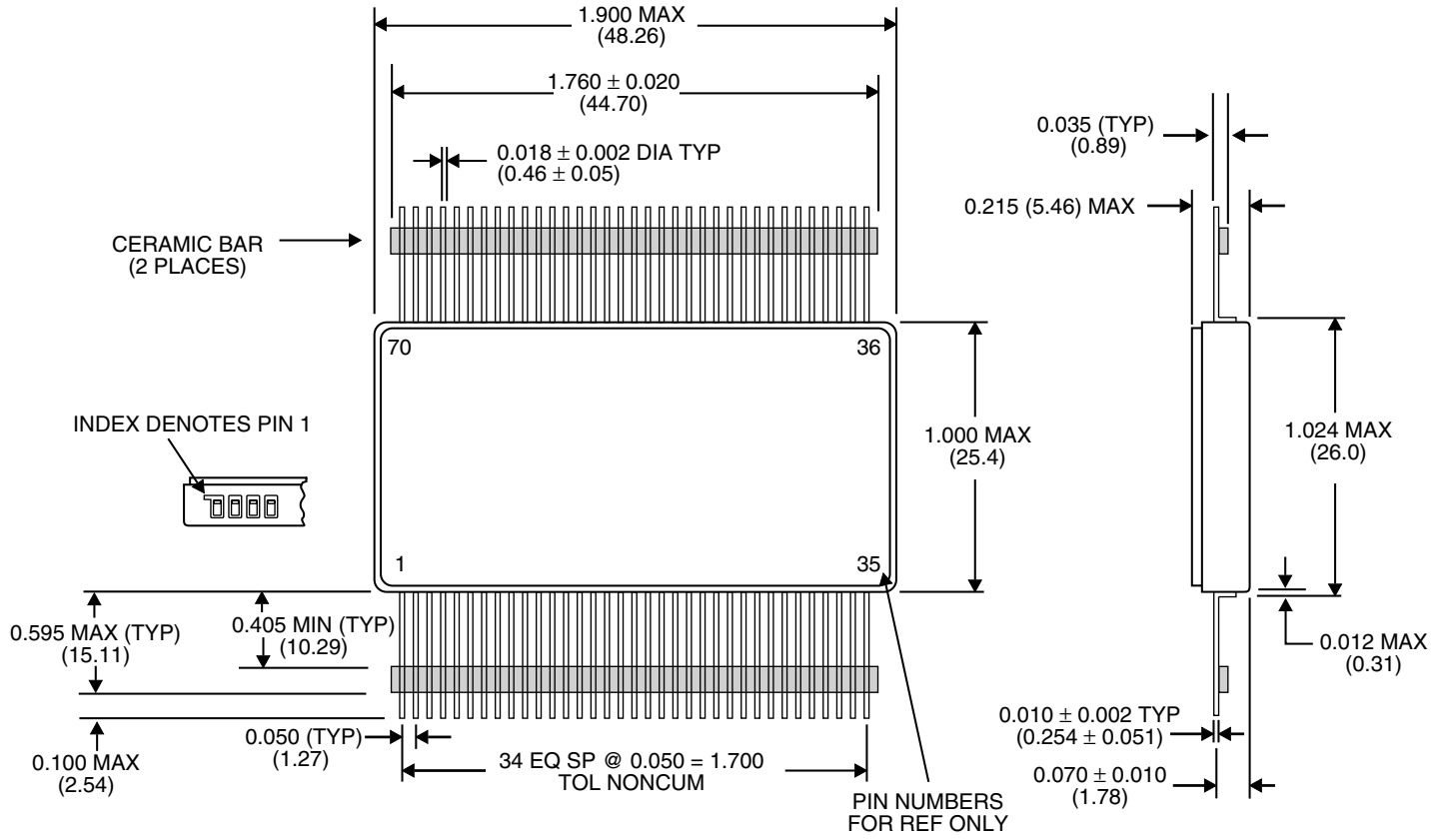
| TABLE 43. BU-63825 PIN LISTING (70-PIN DIP, FLAT PACK) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| PIN | SIGNAL NAME | | | | PIN | SIGNAL NAME | | | |
| | X0 | X1, X2 | X3 | X6 | | X0 | X1, X2 | X3 | X6 |
| 1 | RXA | TX/RX-A | | | 36 | TX_INH_OUT_B | -VB (Note 2) | N/C | TX_INH_IN_B |
| 2 | $\overline{\text{RXA}}$ | $\overline{\text{TX/RX-A}}$ | | | 37 | $\overline{\text{TXB}}$ | GND | | |
| 3 | $\overline{\text{SELECT}}$ | | | | 38 | TXB | +5VB | | |
| 4 | $\overline{\text{STRBD}}$ | | | | 39 | RTAD0 | | | |
| 5 | MEM/$\overline{\text{REG}}$ | | | | 40 | RTAD1 | | | |
| 6 | RD/$\overline{\text{WR}}$ | | | | 41 | RTAD2 | | | |
| 7 | $\overline{\text{MSTCLR}}$ | | | | 42 | RTAD3 | | | |
| 8 | A15 | | | | 43 | RTAD4 | | | |
| 9 | A14 | | | | 44 | RTADP | | | |
| 10 | A13 | | | | 45 | $\overline{\text{INCMD}}$ | | | |
| 11 | A12 | | | | 46 | D00 | | | |
| 12 | A11 | | | | 47 | D01 | | | |
| 13 | A10 | | | | 48 | D02 | | | |
| 14 | A09 | | | | 49 | D03 | | | |
| 15 | A08 | | | | 50 | D04 | | | |
| 16 | A07 | | | | 51 | D05 | | | |
| 17 | A06 | | | | 52 | D06 | | | |
| 18 | GND | | | | 53 | D07 | | | |
| 19 | CLOCK_IN | | | | 54 | +5V Logic | | | |
| 20 | A05 | | | | 55 | D08 | | | |
| 21 | A04 | | | | 56 | D09 | | | |
| 22 | A03 | | | | 57 | D10 | | | |
| 23 | A02 | | | | 58 | D11 | | | |
| 24 | A01 | | | | 59 | D12 | | | |
| 25 | A00 | | | | 60 | D13 | | | |
| 26 | $\overline{\text{DTGRT}}$/MSB/LSB | | | | 61 | D14 | | | |
| 27 | $\overline{\text{SSFLAG}}$/EXT_TRIG | | | | 62 | D15 | | | |
| 28 | $\overline{\text{MEMENA_OUT}}$ | | | | 63 | TAG_CLK | | | |
| 29 | $\overline{\text{MEMOE}}$/ADDR_LAT | | | | 64 | TRANSPARENT/$\overline{\text{BUFFERED}}$ | | | |
| 30 | MEMWR/$\overline{\text{ZERO_WAIT}}$ | | | | 65 | $\overline{\text{INT}}$ | | | |
| 31 | $\overline{\text{DTREQ}}$/16/$\overline{8}$ | | | | 66 | $\overline{\text{READYD}}$ | | | |
| 32 | $\overline{\text{DTACK}}$/POLARITY_SEL | | | | 67 | $\overline{\text{IOEN}}$ | | | |
| 33 | $\overline{\text{MEMENA_IN/TRIGGER_SEL}}$ | | | | 68 | TX_INH_OUT_A | +5VA | | |
| 34 | $\overline{\text{RX-B}}$ | TX/RX-B | | | 69 | $\overline{\text{TXA}}$ | GND | | |
| 35 | RX-B | $\overline{\text{TX/RX-B}}$ | | | 70 | TXA | -VA (Note 2) | N/C | TX_INH_IN_A |

Notes:
1) Pin X0, X1/X2, X3, X6 refer to package option(X) and Voltage Transceiver option (0, 1, 2, 3, 6). See ordering information.
2) -15V for BU-63825X1
   -12V for BU-63825X2.



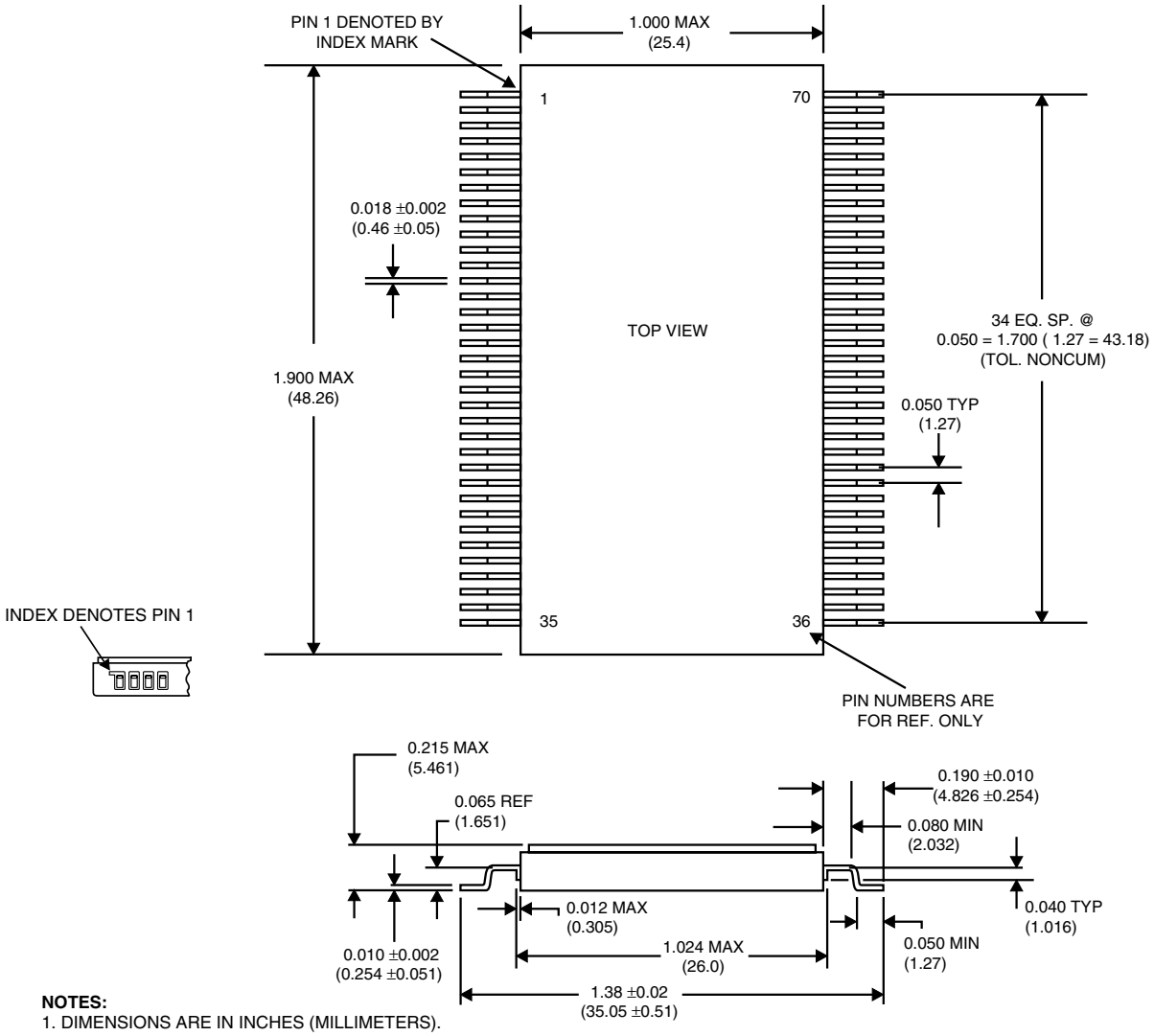

**NOTES:**
1. DIMENSIONS ARE IN INCHES (MILLIMETERS).
2. PACKAGE MATERIAL: ALUMINA ($AL_2O_3$).
3. LEAD MATERIAL: KOVAR, PLATED BY 150µ MINIMUM NICKEL, PLATED BY 50µ MINIMUM GOLD.

**FIGURE 19. BU-63825DX, 70-PIN DIP CERAMIC MECHANICAL OUTLINE**




**NOTES:**
1. DIMENSIONS ARE IN INCHES (MILLIMETERS).
2. PACKAGE MATERIAL: ALUMINA ($AL_2O_3$).
3. LEAD MATERIAL: KOVAR, PLATED BY 150µ MINIMUM NICKEL, PLATED BY 50µ MINIMUM GOLD.

**FIGURE 20. BU-63825FX, 70-PIN FLAT PACK CERAMIC MECHANICAL OUTLINE**




**NOTES:**
1. DIMENSIONS ARE IN INCHES (MILLIMETERS).
2. PACKAGE MATERIAL: ALUMINA ($AL_2O_3$).
3. LEAD MATERIAL: KOVAR, PLATED BY 150µ MINIMUM NICKEL, PLATED BY 50µ MINIMUM GOLD.

**FIGURE 21. BU-63825GX, 70-PIN GULL LEAD CERAMIC MECHANICAL OUTLINE**

## ORDERING INFORMATION

BU-X3X25XX-XXXX

**Supplemental Process Requirements:**
- S = Pre-Cap Source Inspection
- L = 100% Pull Test (standard on this device)
- Q = 100% Pull Test and Pre-Cap Source Inspection
- K = One Lot Date Code
- W = One Lot Date Code and Pre-Cap Source Inspection
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, Pre-Cap Source Inspection and 100% Pull Test
- Blank = None of the Above

**Other Criteria:**
- 0 = No X Ray
- 1 = X Ray

**Process Requirements:**
- 0 = Standard DDC Processing, no Burn-In
- 1 = MIL-PRF-38534 Compliant **(notes 1 and 3)**
- 2 = B **(note 2)**
- 3 = MIL-PRF-38534 Compliant **(notes 1 and 3)** with PIND Testing
- 4 = MIL-PRF-38534 Compliant **(notes 1 and 3)** with Solder Dip
- 5 = MIL-PRF-38534 Compliant **(notes 1 and 3))** with PIND Testing and Solder Dip
- 6 = B **(note 2)** with PIND Testing
- 7 = B **(note 2)** with Solder Dip
- 8 = B **(note 2)** with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In

**Temperature Grade/Data Requirements:**
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

**Voltage Transceiver Option:**
- 0 = No Transceiver (Contact Factory for Availability)
- 1 = +5/-15 V
- 2 = +5/-12 V
- 3 = +5/+5 V
- 6 = +5/+5 V with Transmit Inhibit (TX_INHIBIT)

**Package:**
- D = DIP
- F = Flat Pack
- G = Gull Leads (Above “Process Requirements” must include solder dip.)

**Product Type:**
- 63825 = 70-Pin BC/RT/MT with 16K x 16 Internal RAM
- 63925 = 70-Pin BC/RT/MT with 16K x 16 Internal RAM and with RT Address Latch **(note 5)**
- K3825 = MIL-PRF-38534 Class K Compliant, 70-Pin BC/RT/MT with 16K x 16 Internal RAM
- K3925 = MIL-PRF-38534 Class K Compliant, 70-Pin BC/RT/MT with 16K x 16 Internal RAM and with RT Address Latch **(note 5)**

Notes:
1. Standard processing on this device includes 320 hours of burn-in and 100% non-destruct pull-test. (See Table 3).
2. Standard DDC Processing, with 160 hour burn-in and full temperature (-55°C to +125°C) test.
3. MIL-PRF-38534 product grading is designated with the following dash numbers:
   Class H is a -11X, 13X, 14X, 15X, 41X, 43X, 44X, 45X
   Class G is a -21X, 23X, 24X, 25X, 51X, 53X, 54X, 55X
   Class D is a -31X, 33X, 34X, 35X, 81X, 83X, 84X, 85X
4. These products contain tin-lead solder finish as applicable to solder dip requirements.
5. MIL-PRF-38534 Class K requires PIND testing, X-ray, and 100% Pull test (-X31X ir -X51X with L, Q, Y, or Z as the last digit).

| STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS | | |
|---|---|---|
| TEST | MIL-STD-883 | |
| | METHOD(S) | CONDITION(S) |
| INSPECTION | 2009, 2010, 2017, and 2032 | — |
| SEAL | 1014 | A and C |
| TEMPERATURE CYCLE | 1010 | C |
| CONSTANT ACCELERATION | 2001 | 3000g |
| BURN-IN | 1015 (note 1), 1030 (note 2) | TABLE 1 |

Notes:
1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

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