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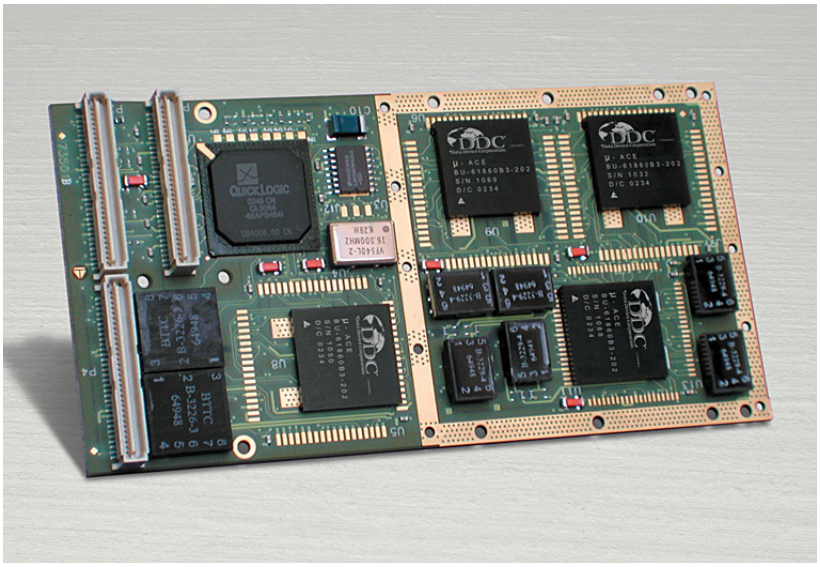
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BU-65566

MIL-STD-1553 66MHZ PMC CARD



DESCRIPTION

The BU-65566 is a single- or multi-channel MIL-STD-1553 PMC card. The design of the BU-65566 leverages DDC's industry proven Enhanced Mini-ACE. Each channel may be independently programmed for Bus Controller (BC), Remote Terminal (RT), Monitor (MT), or Remote Terminal/Monitor (RT/MT) operation.

Advanced architectural features of the Enhanced Mini-ACE include a highly autonomous bus controller, an RT providing a wide variety of buffering options, and a selective message monitor. Each Enhanced Mini-ACE channel incorporates 64K words of RAM, and utilizes 3.3-volt logic locally generated on the card to reduce power consumption.

This card includes primary and secondary thermal interfaces as per the VITA-20-2001 specification. Cards have been subjected to multi-axes shock & vibration testing.

SOFTWARE

The BU-65566 comes bundled with a C language based Applications Programmers Interface (API) Library and the appropriate device drivers to support all modes of operation in Windows 9x/2000/XP, Windows NT, Linux, VxWorks and Integrity. The library is comprised of a collection of C function calls that serves to offload a great deal of low-level tasks from the application programmer. This software supports all of the Enhanced Mini-ACE's advanced architectural features. Optional graphical user software is available for data bus monitoring, analysis, and simulation.

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FEATURES

- 32-Bit/66 MHz PMC Card
- Operates in 3.3V or 5V PCI Signaling Environments
- One to Four Dual Redundant MIL-STD-1553 Channels
- Conduction Cooled with Primary and Secondary Thermal Interfaces
- Shock and Vibration Tested
- Only 5V Supply Required, All Other Supplies Generated Locally
- Enhanced Mini-ACE BC, RT, MT, RT/MT Architecture
- Transformer-Coupled 1553 Channels (Consult Factory for Direct Coupling)
- 64K-word RAM per Channel
- 1MB Flash Memory
- Highly Autonomous Bus Controller Architecture
  - Message Scheduling
  - Bulk Data Transfers
  - Asynchronous Messages
  - Retries and Bus Switching
  - Data Block Double Buffering
- RT Buffering Options
  - Single Buffering
  - Double Buffering
  - Subaddress Circular Buffering
  - Global Circular Buffering
- Selective Message Monitor
- Supports PCI Interrupts
- Software Support for VxWorks®, Linux, Integrity® and Windows® 9x/2000/XP, Windows NT®

FOR MORE INFORMATION CONTACT:

Technical Support:
1-800-DDC-5757 ext. 7771

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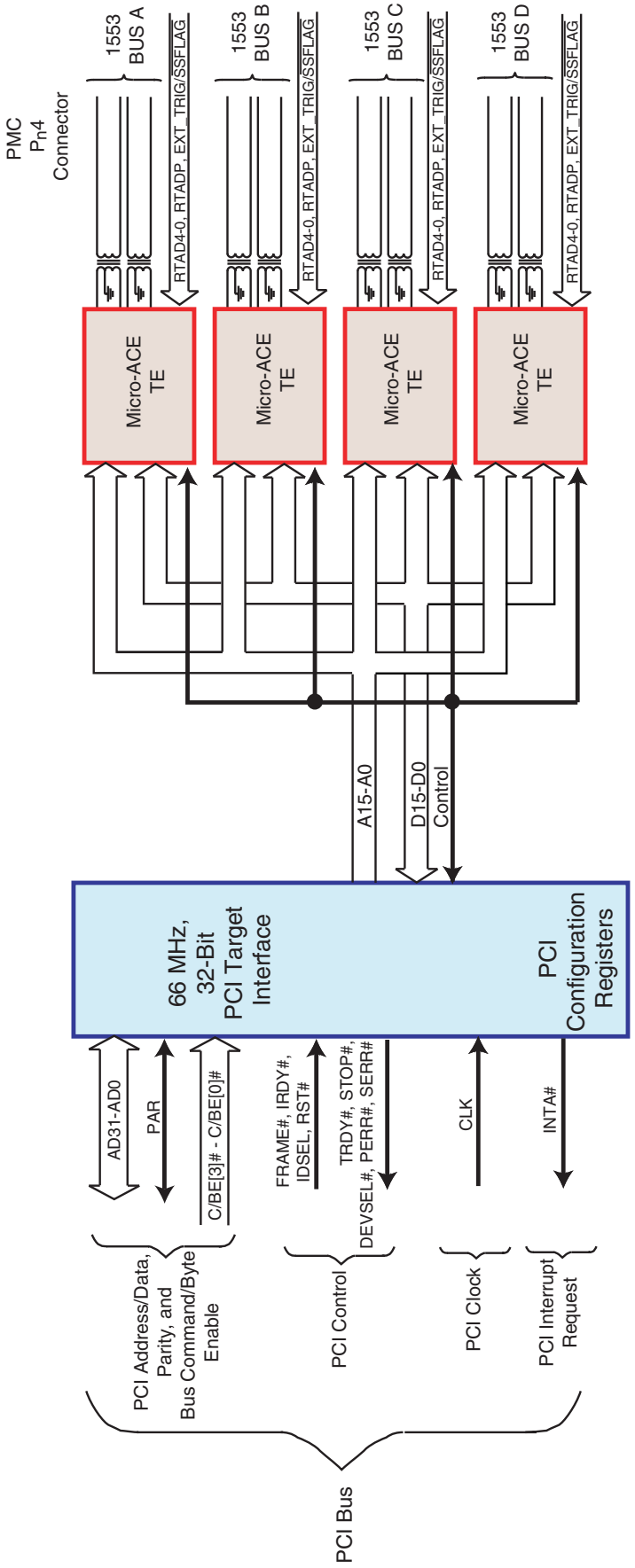


FIGURE 1. BU-65566 BLOCK DIAGRAM

TABLE 1. BU-65566 SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATINGS				
Supply Voltage (Note 9)				
+5V	-0.3		6.0	V
+3.3V (BU-65566MX only)	-0.3		4.6	V
RECEIVER				
Input Impedance, Transformer Coupled (Notes 1-3)	1.000			Kohm
Threshold Voltage, Transformer Coupled	0.200		0.860	Vp-p
Common Mode Voltage (Note 4)			10	Vpeak
TRANSMITTER				
Differential Output Voltage				
Transformer Coupled Across 70 ohms	18	20	27	Vp-p
Output Offset Voltage, Transformer Coupled Across 70 ohms	-250	150	250	mVpeak
Rise/Fall Time	100	150	300	ns
POWER SUPPLY REQUIREMENTS				
Voltage/Tolerances				
+5V	4.75	5.0	5.5	V
Current Drain				
BU-65566X1				
+5V				
• Idle		250	280	mA
• 50% Duty Transmitter Cycle		470	521	mA
• 100% Duty Transmitter Cycle		635	705	mA
BU-65566X2				
+5V				
• Idle		355	394	mA
• 50% Duty Transmitter Cycle		770	855	mA
• 100% Duty Transmitter Cycle		1.091	1.211	A
BU-65566X3				
+5V				
• Idle		455	505	mA
• 50% Duty Transmitter Cycle		1.076	1.195	A
• 100% Duty Transmitter Cycle		1.629	1.808	A
BU-65566X4				
+5V				
• Idle		550	611	mA
• 50% Duty Transmitter Cycle		1.375	1.526	A
• 100% Duty Transmitter Cycle		2.192	2.433	A
POWER DISSIPATION (NOTE 9)				
BU-65566X1				
• Idle		1.3	1.4	W
• 50% Duty Transmitter Cycle		1.6	1.9	W
• 100% Duty Transmitter Cycle		1.8	2.1	W
BU-65566X2				
• Idle		1.8	2.0	W
• 50% Duty Transmitter Cycle		2.4	2.9	W
• 100% Duty Transmitter Cycle		2.7	3.3	W
BU-65566X3				
• Idle		2.3	2.5	W
• 50% Duty Transmitter Cycle		3.3	3.9	W
• 100% Duty Transmitter Cycle		3.9	4.8	W
BU-65566X4				
• Idle		2.8	3.1	W
• 50% Duty Transmitter Cycle		4.1	4.8	W
• 100% Duty Transmitter Cycle		5.4	6.6	W
1553 MESSAGE TIMING				
Completion of CPU Write (BC Start)-to-Start of Next Message (Non-enhanced BC Mode)		2.5		µs
BC Intermessage Gap - (Note 5)				
Non-Enhanced BC mode (Mini-ACE compatible)		9.5		µs
Enhanced BC mode (Note 6)		10.1		µs

TABLE 1. BU-65566 SPECIFICATIONS (CONT.)

PARAMETER	MIN	TYP	MAX	UNITS
1553 MESSAGE TIMING (CONT)				
BC/RT/MT Response Timeout (Note 7)	17.5	18.5	19.5	µs
18.5 nominal	21.5	22.5	23.5	µs
22.5 nominal	49.5	50.5	51.5	µs
50.5 nominal	127	129.5	131	µs
128.0 nominal	4		7	µs
RT Response Time (mid-parity to mid-sync) (Note 8)		660.5		µs
Transmitter Watchdog Timeout				
THERMAL				
Operating Temperature at Thermal Rail				
BU-65566GX-200	-40		+85	°C
BU-65566GX-300	0		+55	°C
Thermal Resistance				
Junction to Thermal Interface "M"			+39	°C/W
Storage Temperature	-65		+105	°C
MECHANICAL DESIGN				
Shock: Three pulses, half sine on six (6) axes	40g's, 11 msec/axes			
Vibration: Random input, one hour each axes 40g's 11 msec/axes, three hours total, 15 to 2000 Hz	14g's rms			
Resonant Frequency: BU-65566X2 (calculated) 12Hz	12 Hz			
PHYSICAL CHARACTERISTICS				
Size	5.659 x 2.913 (144 x 74)			in. (mm)
Weight				
BU-65566X1	2.7 (76.5)			oz. (g)
BU-65566X2	3.3 (93.56)			oz. (g)
BU-65566X3	3.9 (110.6)			oz. (g)
BU-65566X4	4.5 (127.6)			oz. (g)

TABLE 1 notes:

(Notes 1 through 3 are applicable to the Input Impedance specification:)

1. The specifications are applicable for both unpowered and powered conditions.
2. The specifications assume a 2 Volt rms balanced, differential, sinusoidal input. The applicable frequency is 75 kHz to 1 MHz.
3. Minimum impedance is guaranteed over the operating range, but is not tested.
4. Assumes a common mode voltage within the frequency range of dc to 2MHz, applied to pins of the isolation transformer on the stub side (transformer coupled), and referenced to signal.
5. Typical value for minimum intermessage gap time. Under software control, this may be lengthened to 65,535 ms. If ENHANCED CPU ACCESS, bit 14 of Configuration Register #6, is set to logic "1", then host accesses during BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences could have the effect of lengthening the intermessage gap time. For each host access during an SOM or EOM sequence, the intermessage gap time will be lengthened by 6 clock cycles. Since there are 7 internal transfers during SOM, and 5 during EOM, this could theoretically lengthen the intermessage gap by up to 72 clock cycles; i.e., 4.5 µs.
6. For enhanced BC mode, the typical value for intermessage gap time is approximately 625 ns longer than for the non-enhanced BC mode.
7. Software programmable (4 options). Includes RT-to-RT Timeout (measured mid parity of transmit Command Word to mid-sync of Transmitting RT Status Word).
8. Measured from mid-parity crossing of Command Word to mid-sync crossing of RT's Status Word.
9. Power dissipation specifications assume a transformer coupled configuration with external dissipation (while transmitting) of:
   0.14 watts for the active isolation transformer,
   0.08 watts for the active bus coupling transformer,
   0.45 watts for each of the two bus isolation resistors and
   0.15 watts for each of the two bus termination resistors.
10. All power measurements are for a 33 MHz PCI bus; add 120 mA more @ 66 Mhz operation.

INTRODUCTION

The BU-65566 is a single- or multi-channel MIL-STD-1553 66MHz PMC card built in accordance with IEEE PMC Physical and Environmental Layers Standard. The BU-65566 is available with one to four dual redundant 1553 channels on a conduction-cooled card with an operating temperature of -40° to +85°C or 0° to +55°C measured at the rail.

The design of the BU-65566 leverages the field proven Enhanced Mini-ACE. Each channel may be independently programmed for BC, RT, Monitor, or RT/Monitor mode.

ENHANCED MINI-ACE

The BU-65566 PMC card incorporates a PCI bridge, along with between one and four of DDC's Enhanced Mini-ACE hybrid(s). Each Enhanced Mini-ACE comprises a complete, independent interface between the PCI bridge and a MIL-STD-1553 bus. The Enhanced Mini-ACE hybrids provide software compatibility with DDC's older generation ACE and Mini-ACE (Plus) terminals.

The card provides complete multiprotocol support of MIL-STD-1553A/B and STANAG 3838. These hybrids include dual transceivers, along with protocol, host interface, memory management logic, and 64K X 16 of RAM with built-in parity checking.

One of the features of the Enhanced Mini-ACE is its enhanced Bus Controller (BC) architecture. The Enhanced BC's autonomous message sequence control engine provides a means for offloading the host processor for implementing multi-frame message scheduling, message retry and bus switching schemes, data double buffering, and asynchronous message insertion. In addition, the Enhanced BC mode includes 8 general purpose flag bits, a general purpose queue, and user-defined interrupts, for the purpose of performing messaging to the host processor. This all serves to greatly reduce the amount of host processing bandwidth required.

Another important feature of the Enhanced Mini-ACE is the incorporation of a fully autonomous built-in self-test.

The Enhanced Mini-ACE Remote Terminal (RT) offers the choice of single, double, and circular buffering for individual subaddresses along with a global circular buffering option for multiple (or all) receive subaddresses, a 50% rollover interrupt for circular buffers, and an interrupt status queue for logging up to 32 interrupt events. The RT can be configured, via API library to reliably transfer data from RT hardware to a host buffer when one of these interrupts occurs. The library also allows for the creation of a user defined Interrupt Service Routine (ISR) on any of the available interrupts of the Enhanced Mini-ACE.

The transceivers in the Enhanced Mini-ACE series terminals are fully monolithic, requiring only a +5 volt power input. The transmitters are voltage sources, which provide improved line driving capability over current sources. This serves to improve performance on long buses with many taps. The BU-65566's transmitters may be trimmed to meet the MIL-STD-1760 requirement of a minimum of 20 volts peak-to-peak, transformer coupled (consult factory).

If required, the BU-65566 is also available with an option for McAir compatible transmitters (consult factory).

FLASH MEMORY

The BU-65566 PMC card includes an 8Mbit (1MB) flash memory. The flash memory is available to a user (via PCI mapping) for non-volatile storage. The memory may also be used to store Enhanced Mini-ACE configuration data. This configuration data is then used to auto-initialize any or all of the Enhanced Mini-ACE channels at power-on.

BUILT-IN SELF-TEST

The Enhanced Mini-ACE includes extensive, highly autonomous self-test capability. This includes both protocol and RAM self-tests. The Enhanced Mini-ACE protocol test is performed automatically following power turn-on. In addition, either or both of these self-tests may be initiated by command(s) from the BU-65566's PCI host. The API library includes functions to easily perform these tests.

THERMAL DESIGN

The thermal design of this card includes thermal vias located under the Enhanced Mini-ACE transceiver chips. The transceiver chips have the highest heat dissipation on the card: 1.22 watts maximum at 100% transmit duty cycle. Heat is conducted through the thermal vias to an inner copper plane layer, which functions as a heat spreader. The heat path includes additional thermal vias from the thermal plane layer to the two copper strips which run the width of the card (primary thermal interface) and the two copper strips which run part of the length of the card (secondary thermal interface). Thermal rails from the card base may then be bolted to the copper strips, providing a path for removing heat from the card.

The rail temperature can range from -40°C to +85°C. DDC has designed this board to operate under these temperature conditions.

MECHANICAL DESIGN

Test specimens of the BU-65566 card were subjected to Shock and Random Vibration testing. All devices were non-operational during all phases of testing and exhibited no evidence of physical damage at the conclusion of testing.

Three (3) shock pulses were applied in each of the following six (6) test directions: Horizontal (+X), Horizontal (+Z), Vertical (+Y), Horizontal (-X), Horizontal (-Z), and Vertical (-Y). Each applied shock pulse was Half-Sine in wave shape, at an input amplitude of 40 g's and a duration of 11 milliseconds.

Random vibration was independently applied for one (1) hour to each of three (3) orthogonal axes resulting in a total test time of three (3) hours. Testing was performed with the input applied along the Horizontal (X), Horizontal (Z) and Vertical (Y) test axes. Test specimens were subjected to a Random input, in the frequency range of 15 to 2000 Hz at $.1g^2$ / Hz.

PCI INTERFACE

As a means of minimizing power consumption and dissipation, the design of the standard BU-65566 card utilizes +3.3 volt power for the PCI interface and 1553 (Enhanced Mini-ACE) logic. The 1553 transceivers and RAM are powered by +5 volts. The default configuration of the BU-65566GX card provides an on board voltage regulator for applications where +3.3 volt power is not available.

DDC is able to supply a non-standard version of the BU-65566GX card where the voltage regulator is removed and the card will utilize the +3.3V power supply pins on the PMC connector (consult factory).

The BU-65566's PCI interface is a fully compliant target (slave) agent, as defined by the PCI Local Bus Specification Revision 2.2, using a 32-bit interface that operates at clock speeds of up to 66 MHz, in a +3.3 volt or +5 volt signaling environment. The interface supports PCI interrupts and contains a 72 X 32 FIFO to accelerate burst write transfers from the PCI host.

INTERRUPTS

The Enhanced Mini-ACE's may issue interrupt requests over the PCI bus. PCI interrupts are generated on the INTA# output signal to the PCI host. The interrupts from each Enhanced Mini-ACE(s) are logically Or'ed together to provide a single interrupt for the card.

REGISTER AND MEMORY ADDRESSING

The BU-65566 PCI interface contains a set of "Type 00h" PCI configuration registers that are used to map the device into the host system. The PCI configuration register space is mapped in accordance with PCI revision 2.2 specifications. These registers are arranged such that all Enhanced Mini-ACE memory and register space may be addressed through a single PCI function. The PCI configuration space of this card is described in the BU-65565/66 Card Manual. When using this card with one of DDC's drivers and the Enhanced Mini-ACE API library software, the details of these registers and memory addresses are abstracted from the user.

ENHANCED MINI-ACE REGISTER AND MEMORY ADDRESSING

The software interface between each Enhanced Mini-ACE and the PCI host consists of 24 internal operational registers for normal operation, an additional space for 40 test mode registers, and 64K words of shared memory address space.

Enhanced Mini-ACE registers may only be accessed as 16-bit words. If a 32-bit read access is attempted, the upper 16 bits will not be valid. That is, register accesses are on a 32-bit boundary (e.g., 000 = Enhanced Mini-ACE Register 0, 004 = Enhanced Mini-ACE Register 1, 008 = Enhanced Mini-ACE Register 2, etc). For normal operation, the host processor only needs to access the lower 32 register address locations (00-1F). The next 32 locations (20-3F) should be reserved, since many of these are used for factory test.

Enhanced Mini-ACE memory may be accessed as either single 16-bit words, or as a 32-bit double word. For the latter, a packed pair of 16-bit words at adjacent memory address locations will be accessed.

Note that the addressing for all Enhanced Mini-ACE pointers is word-oriented, while all PCI addressing is byte-oriented. That is, the value of a pointer stored in Enhanced Mini-ACE RAM will be half of the value of the PCI address offset from the base memory address for the particular Enhanced Mini-ACE. If not using the Enhanced Mini-ACE API Library and you would like more information about the Enhanced Mini-ACE registers and memory addresses please reference the Enhanced Mini-ACE User's Guide.

When using the API library provided with your card, the Enhanced Mini-ACE registers and memory accesses are abstracted from the end user to provide an easy-to-use High Level C programming environment.

BUS CONTROLLER (BC) ARCHITECTURE

The BC functionality for the Enhanced Mini-ACE includes two separate architectures: (1) the older, legacy mode, which provides complete compatibility with the previous ACE and Mini-ACE (Plus) generation products; and (2) the newer, Enhanced BC mode. The Enhanced BC mode offers several new powerful architectural features. This includes the incorporation of a highly autonomous BC message sequence control engine, which greatly serves to offload the operation of the host CPU. This can be a critical factor in embedded systems with real time requirements.

The Enhanced BC's message sequence control engine provides a high degree of flexibility for implementing major and minor frame scheduling; capabilities for inserting asynchronous messages in the middle of a frame; to separate 1553 message data from control/status data for the purpose of implementing double buffering and performing bulk data transfers; for implementing

message retry schemes, including the capability for automatic bus channel switchover for failed messages; and for reporting various conditions to the host processor by means of user-defined interrupts and a general purpose queue.

In both the legacy and Enhanced BC modes, the Enhanced Mini-ACE BC implements all MIL-STD-1553B message formats. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages.

When using the Enhanced Mini-ACE API library the user can easily input options to one of the aceBCMsgCreate() functions listed in the Enhanced Mini-ACE Runtime Library Software Manual to control the operations described above. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type, sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The Enhanced Mini-ACE BC response timeout value is programmable with choices of 18, 22, 50, and 130 ms by using the aceSetRespTimeOut() library function. The longer response timeout values allow for operation over long buses and/or use of the repeaters. In the Enhanced BC mode, there is no explicit limit to the number of messages that may be processed in a frame.

When using the Enhanced Mini-ACE API library this is all easily implemented by calling the BC set of functions, which allows the user to easily set up BC operation. The library abstracts all memory accesses, register accesses, and individual bit operations to make programming the Enhanced Mini-ACE simple.

BC GENERAL PURPOSE QUEUE

The Enhanced Mini-ACE BC allows for the creation of a general purpose queue. This data structure provides a means for the message sequence processor to convey information to the BC host. The BC op code repertoire provides mechanisms to push various items on this queue. These include the contents of the Time Tag Register, the Block Status Word for the most recent message, an immediate data value, or the contents of a specified memory address. The Enhanced Mini-ACE C API library uses the general-purpose queue to provide for timing messages and frame repetitions.

BC HOST BUFFER

The Enhanced Mini-ACE API library software allows for the creation of a circular software host buffer. The software will automatically log all messages and data processed by the BC to the host buffer. The user can poll the host buffer with the aceBCGetHBufMsgsRaw() function to read the contents of the host buffer or with the aceBCGetHBufMsgDecoded() function to read one message at a time. This function will read one message from the host buffer and parse all relevant information into a library structure to separate the command word, data words, and all other parts of a 1553 message. This allows the user to easily read a message without parsing the individual bits.

REMOTE TERMINAL (RT) ARCHITECTURE

The Enhanced Mini-ACE RT architecture provides multiprotocol support, with full compliance to all of the commonly used data bus standards, including MIL-STD-1553A, MIL-STD-1553B, Notice 2, STANAG 3838, General Dynamics 16PP303, and McAir A3818, A5232, and A5690. For the Enhanced Mini-ACE RT mode, there is programmable flexibility enabling the RT to be configured to fulfill any set of system requirements. This includes the capability to meet the MIL-STD-1553A response time requirement of 2 to 5 µs, and multiple options for mode code subaddresses, mode codes, RT status word, and RT BIT word.

The Enhanced Mini-ACE RT protocol design implements all of the MIL-STD-1553B message formats and dual redundant mode codes. The design has passed validation testing for MIL-STD-1553B compliance. The Enhanced Mini-ACE RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. One of the main features of the Enhanced Mini-ACE RT is its choice of memory management options. These include single buffering by subaddress, double buffering for individual receive subaddresses, circular buffering by individual subaddresses, and global circular buffering for multiple (or all) subaddresses.

Other features of the Enhanced Mini-ACE RT include a set of interrupt conditions, an interrupt status queue with filtering based on valid and/or invalid messages, internal command illegalization, programmable busy by subaddress, multiple options on time tagging, and an "auto-boot" feature which allows the RT to initialize as an online RT with the busy bit set following power turn-on.

RT COMMAND STACK

The command stack provides a chronology of all messages processed by the Enhanced Mini-ACE RT. Similar to BC mode, there is a four-word block descriptor in the Stack for each message processed. The four entries to each block descriptor are the Block Status Word, Time Tag Word, the pointer to the start of the message's data block, and the 16-bit received Command Word.

RT HOST BUFFER

The Enhanced Mini-ACE API library software allows for the creation of a circular software host buffer. The software library will automatically log all messages and data processed by the RT to the host buffer. The user can poll the host buffer with the aceRTGetHBufMsgsRaw() to read the contents of the host buffer or with the aceRTGetHBufMsgDecoded() to read one message at a time. This function will read one message from the host buffer and parse all relevant information into a library structure to separate the command word, data words, and all other parts of a 1553 message. The creation of a host buffer is commonly used

in non-deterministic operating systems such as Windows so that a buffer exists for the library to reliably transfer messages from the Command Stack and Data Stack on the hardware to ensure that no messages are lost. The library transfers messages reliably to the host buffer with no intervention from the user.

RT INTERRUPTS

The Enhanced Mini-ACE offers a great deal of flexibility in terms of RT interrupt processing. By means of the Enhanced Mini-ACE's two Interrupt Mask Registers, the RT may be programmed to issue interrupt requests for the following events/conditions: End-of-(every)Message, Message Error, Selected (transmit or receive) Subaddress, 100% Circular Buffer Rollover, 50% Circular Buffer Rollover, 100% Descriptor Stack Rollover, 50% Descriptor Stack Rollover, Selected Mode Code, Transmitter Timeout, Illegal Command, Interrupt Status Queue Rollover, End of Frame, and any user defined interrupt.

The Enhanced Mini-ACE API library can be used to configure the RT to generate interrupts and reliably transfer messages and data to the host buffer (if enabled in software) to guarantee that data will not be lost. The library also allows for users to create an ISR that will execute at any of the selected interrupt conditions.

OTHER RT FEATURES

The Enhanced Mini-ACE provides an internal mechanism for RT Command Word illegalizing. The design of the BU-65566 supports two different options for specifying the RT addresses for the individual Enhanced Mini-ACE's: (1) by means of the RT ADDRESS (and PARITY) inputs, that are brought out to the card's Pn4 connector, and latched under host software control; or (2) fully software programmable by the host, by means of an internal register. In both configurations, the RT address is readable by the host processor.

The Enhanced Mini-ACE includes options for the Terminal flag status word bit to be set either under software control and/or automatically following a failure of the loopback self-test. Other software programmable RT options include software programmable RT status and RT BIT words, automatic clearing of the Service Request bit following receipt of a Transmit vector word mode command, options regarding Data Word transfers for the Busy and Message error (illegal) Status word bits, and options for the handling of 1553A and reserved mode codes.

MONITOR (MT) ARCHITECTURE

The Enhanced Mini-ACE includes three monitor modes:

(1) A Word Monitor mode.

(2) A selective message monitor mode.

(3) A combined RT/message monitor mode.

For new applications, it is recommended that the selective message monitor mode be used, rather than the word monitor mode. Besides providing monitor filtering based on RT address, T/R bit, and subaddress, the message monitor eliminates the need to

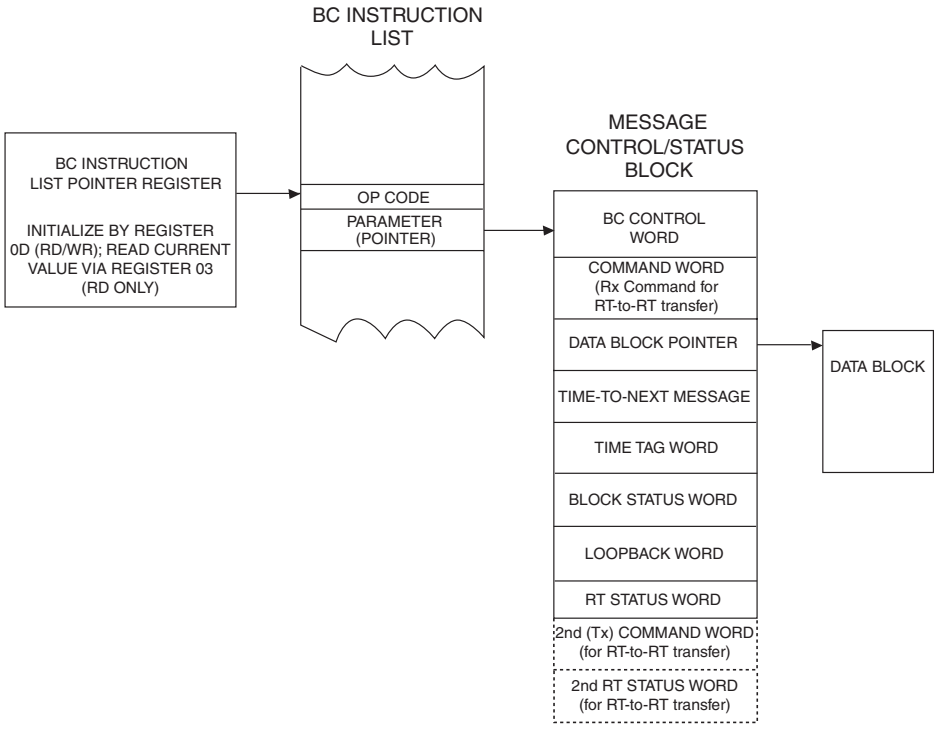


FIGURE 2. BC MESSAGE SEQUENCE CONTROL

determine the start and end of messages by software. A combined RT/MT mode allows the device to run in both modes of operation at the same time on the bus.

MT COMMAND STACK

Upon receipt of a valid Command Word, the Enhanced Mini-ACE will reference the Selective Monitor Lookup Table to determine if the current command is enabled. If the current command is disabled, the Enhanced Mini-ACE monitor will ignore (and not store) the current message. If the command is enabled, the monitor will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer, and an entry in the monitor data stack starting at the location referenced by the monitor data stack pointer.

MT HOST BUFFER

The Enhanced Mini-ACE API library software allows for the creation of a circular software host buffer. The software library will automatically log all messages and data processed by the MT to the host buffer. The user can poll the host buffer with the aceMTGetHBufMsgsRaw() function to read the contents of the host buffer or with the aceMTGetHBufMsgDecoded() function to read one message at a time. This function will read one message from the host buffer and parse all relevant information into a library structure to separate the command word, data words, and all other parts of a 1553 message. The creation of a host buffer is commonly used in non-deterministic operating systems such as Windows so that a buffer exists for the library to transfer messages from the Command Stack and Data Stack on the hardware to ensure that no messages are lost. The library transfers messages reliably to the host buffer with no intervention from the user.

MONITOR INTERRUPTS

Selective monitor interrupts may be issued for End-of-message and for conditions relating to the monitor command stack pointer and monitor data stack pointer, such as Command Stack 50% Rollover, Command Stack 100% Rollover, Data Stack 50% Rollover, and Data Stack 100% Rollover.

The Enhanced Mini-ACE API library can be used to configure an MT to generate interrupts and reliably transfer messages and data to the host buffer (if enabled in software) to guarantee that data will not be lost. The library also allows for users to create an ISR that will execute at any of the selected interrupt conditions.

SOFTWARE

The BU-69090 series Enhanced Mini-ACE software is a High-Level ANSI C language based API library of functions that provides comprehensive support for all of DDC's Enhanced Mini-ACE cards. The software package also includes device drivers for Windows 9x/2000/XP, Windows NT, Linux, Integrity, and VxWorks. The base library consists of a suite of function calls that serves to offload a great deal of low-level tasks from the application programmer. This includes register initialization, along with memory management software, and the means to implement an offline development environment.

As a means of supporting operation on multiple platforms, the BU-69090 library is written in ANSI C, and leverages component object modeling (COM). The use of ANSI C and component object modeling provides portability to different operating systems and card types. As a result, the library may be easily ported to run on platforms based on a variety of microprocessors, running under different operating systems or in some cases no operating system.

The library initialization function results in configuring the Enhanced Mini-ACE's to a specific state, depending on the mode of operation. For each mode, advanced architectural features are enabled as part of the initialization. Depending on the mode of operation that is initialized, the user may access specific data structures. For example, for BC mode, there are separate functions for accessing op codes, messages, data blocks, and frames. There are separate functions that may be invoked to release all resources for a particular device. Asynchronous messages can be easily inserted into a frame by calling a high-level API library function.

For all function calls, the library checks all parameters for validity, with invalid parameters resulting in error codes.

HOST BUFFER

For all modes of operation, the Enhanced Mini-ACE API library allows the programmer to log all messages processed. With the

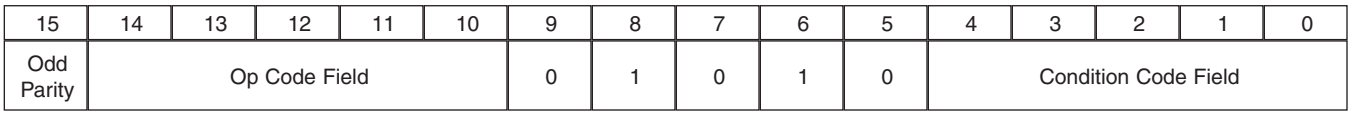


FIGURE 3. BC OP CODE FORMAT

use of the Host Buffering feature, all messages will be automatically transferred from the Enhanced Mini-ACE memory into a user-definable host buffer.

A host buffer is commonly used to ensure that messages are reliably transferred to the host buffer with no user intervention to ensure that no messages are lost. In non-deterministic systems, such as Microsoft Windows, in which the user has little or no control of how long it will take to read new messages off the Enhanced Mini-ACE stack, messages might otherwise be lost.

INTERRUPT HANDLING

Enhanced Mini-ACE interrupt handling involves the use of a thread blocking/callback mechanism. A high priority background thread, enabled via the library, blocks at the kernel level until an interrupt occurs. Once one occurs, the default library service routine, and optionally a user defined routine, is called. During application development, one must take into consideration the performance cost when incorporating user defined interrupt routines. Complicated, multi-function call, or system calls that may perform any input/output may have considerably detrimental effects on processing performance.

When the processor and then the operating system is signaled that an interrupt request has occurred, the driver reads card-specific registers to determine if a particular Enhanced Mini-ACE channel has requested interrupt service. Assuming that one of the Enhanced Mini-ACE's has issued an interrupt, the library checks to see which interrupt event(s) has occurred. If more than one interrupt event has occurred, these are processed sequentially, one at a time.

If a particular Enhanced Mini-ACE issued the interrupt request, then its "blocking" condition will be lifted. At this time, the library will then read the respective Enhanced Mini-ACE's Interrupt Status Registers. Note that there is a separate thread for each Enhanced Mini-ACE. For each Interrupt Status Register bit that is set, the library interrupt service routine checks to see if the corresponding Interrupt Mask Register bit has been set. At this point, the library references a lookup table, which will then invoke one of several specific user routines associated with specific interrupt events. In responding to specific interrupt events, the user routines may then invoke other library functions.

After a particular interrupt event has been responded to, the thread will then perform a "manual" interrupt clear (if necessary). At that time, the thread will then revert to its "blocking" condition. This is all done internally by the library and driver to ensure reliability. The user can optionally set up a user defined ISR by calling the aceSetIrqConditions() function.

VXWORKS DRIVER

The BU-69090S2 is the Enhanced Mini-ACE API library with a C language based VxWorks driver. This driver, which is designed to operate with version 5.2 of Wind River's VxWorks, was devel-

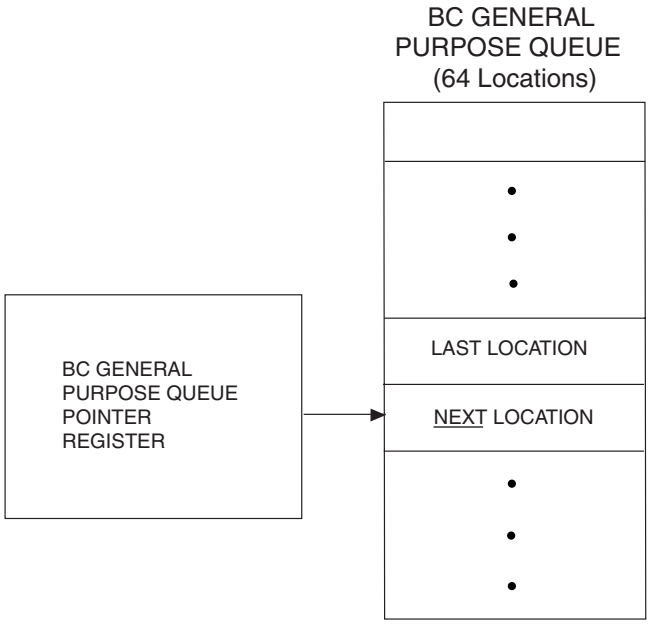


FIGURE 4. BC GENERAL PURPOSE QUEUE

oped using a Motorola MVME 2700 card, which is based on a Power PC 750 processor. The drivers were developed using Wind River's Tornado II integrated development environment. The source code for the driver and library are provided to allow the driver to be tailored to any specific host board. A version of the software for Intel platforms is also included.

The driver makes the required calls to the operating system necessary to acquire the correct address and interrupt resource information. The driver will use these resources during initialization of the card, and for read, write, and interrupt functions during normal operation. The ability to establish configuration in this manner enables a hands-off configuration of the card in any system.

LINUX DRIVER

The BU-69090S1 is the Enhanced Mini-ACE API library with a C language based Linux driver. This driver is a loadable module with source code available so that the driver can be compiled against your version of the Linux kernel source code. This allows for compatibility with any kernel version.

INTEGRITY DRIVER

The BU-69090S5 is the Enhanced Mini-ACE API Library with a C language based Integrity driver. The driver is designed to operate with Power PC hosts.

OFFLINE DEVELOPMENT ENVIRONMENT

The software includes support of an offline development environment (reference FIGURE 5). This allows code to be developed using a BU-65569 PCI card or BU-65553 PCMCIA card on an offline workstation such as a desktop PC, rather than on embedded system hardware. The Enhanced Mini-ACE library includes a function that creates two files that download into the application program for the target embedded system. The first file is a binary file that contains an image of Enhanced Mini-ACE registers and memory, and the second file is a C header file that indicates all locations to structures/frames within memory.

The Enhanced Mini-ACE API library can also be programmed without the need of an Enhanced Mini-ACE card. In simulated access mode the library allocates host memory to be used as if it were memory on the device. All application code can be developed before you actually receive hardware. Files can also be created to allow the programmer to recreate the setup inside of an embedded system.

The binary image file is stored in the embedded system nonvolatile memory. During initialization, it is then loaded into the Enhanced Mini-ACE shared RAM and registers. The header file contains a readable ASCII representation of the entire mapping of the Enhanced Mini-ACE based on the operations entered into the program. The header file includes the location and size of message blocks and other data structures.

The benefits of the use of image and header files include: (1) reduction in the size of embedded code; (2) reduced computational resources (CPU bandwidth cycles); and (3) the user has greater control over the development, validation, and documentation of flight critical and mission critical code.

TABLE 2. A SAMPLING OF BC LIBRARY FUNCTIONS	
aceBCDataBlkCreate (DevNum, nDataBlkID, wDataBlkSize,*pBuffer, wBufferSize)	This function allocates a data block to be used by any message. The data block may be 1 to 32 words long, single or double buffered.
aceBCOpCodeCreate (DevNum, nOpCodeID, wOpCodeType, wCondition, wParameter1, wParameter2, dwReserved)	This function creates an op code/parameter word pair and appends it to the BC instruction list.
aceBCMsgCreateBCtoRT (DevNum, nMsgBlkID, nDataBlkID, wRT, wSA, wWC, MsgGapTime, dwMsgOptions)	This function creates the message control/status block for a BC-to-RT transfer message. There are separate functions for RT-to-BC transfers, RT-to-RT transfers, mode code messages, BC-to-RTs broadcast transfers, BC-to-RTs broadcast messages, and broadcast mode code messages.
aceBCFrameCreate (DevNum, nFrameBlkID, wFrameType, aOpCodeIDs, wOpCodeCount, wMnrFrmTime, wFlags)	This function creates a BC frame from an array of Op Code IDs. The frame may be either a minor or major frame.
aceBCStart (DevNum, nMjrFrmID, lMjrFrmCount, pMjrFrmNode, pMsgNode, pDataNode, pFrameNode)	This function initiates the BC to process a specified major frame.

TABLE 3. A SAMPLING OF RT LIBRARY FUNCTIONS	
aceRTDataBlkCreate (DevNum, nDataBlkID, wDataBlkType, *pBuffer, wBufferSize)	This function allocates an RT data block.
aceRTDataBlkMapToSA (DevNum, nDataBlkID, wSA, wMsgType, wIrqOptions, wLegalizeSA)	This function maps a data block defined using aceRTDataBlkCreate with a specified transmit, receive, or broadcast subaddress. The function may also be used to legalize or illegalize the specified subaddress.
aceRTGetHBufMsgDecoded (DevNum, MSGSTRUCT *pMsg, *pdwMsgCount, *pdwMsgLostStk, *pdwMsgLostHBuf, wMsgLoc)	This function reads and decodes a message from the host buffer (assuming that one is present), and places the decoded message into the MSGSTRUCT parameter.
aceRTDataBlkCircBufInfo (DevNum, nDataBlkID, *pUserRWOffset, *pAceRWOffset)	This function returns information about a circular buffer, including the last read or written location performed by the user and the last location read or written by the Enhanced Mini-ACE RT.

TABLE 4. A SAMPLING OF MONITOR LIBRARY FUNCTIONS	
aceMTEnableRTFilter (DevNum, wRT, wTR, dwSAMask)	This function may be used to enable monitor selection for a specific subaddress or all subaddresses, for a specific RT address or all RT addresses.
aceMTStkToHBuf (DevNum)	This function copies all messages from the (previously active) stack to the host buffer. Once the messages have been moved to the host buffer, they can be processed by the application using either aceMTGetHBufMsgsRaw() or aceMTGetHBufMsgsDecoded().
aceMTGetHBufMsgDecoded (DevNum, MSGSTRUCT *pMsg, *pdwMsgCount, *pdwMsgLostStk, *pdwMsgLostHBuf, wMsgLoc)	This function reads either the last unread or most recently received decoded message from the host buffer.

TABLE 5. BU-65566 Pn4 CONNECTOR PIN FUNCTIONS			
PIN	FUNCTION	PIN	FUNCTION
1	RT_ADD_B0	33	RT_ADD_D3
2	SSFLG/EXT_TRIG_A	34	RT_ADD_D2
3	SSFLG/EXT_TRIG_B	35	RT_ADD_A0
4	SSFLG/EXT_TRIG_C	36	1553_1B–
5	RT_ADD_B1	37	GND
6	SSFLG/EXT_TRIG_D	38	1553_1B+
7	GND	39	RT_ADD_A1
8	1553_1D+	40	1553_2D–
9	RT_ADD_B2	41	RT_ADD_D1
10	RT_ADD_C4	42	1553_1C+
11	RT_ADD_C3	43	RT_ADD_A2
12	1553_1D–	44	1553_1C–
13	RT_ADD_B3	45	RT_ADD_D0
14	RT_ADD_C2	46	1553_2C+
15	RT_ADD_C1	47	RT_ADD_A3
16	1553_2A–	48	1553_2C–

TABLE 5. BU-65566 Pn4 CONNECTOR PIN FUNCTIONS (CONT)			
PIN	FUNCTION	PIN	FUNCTION
17	RT_ADD_B4	49	RT_ADD_DP
18	1553_2A+	50	1553_1A–
19	RT_ADD_C0	51	RT_ADD_A4
20	RT_ADD_CP	52	1553_1A+
21	RT_ADD_BP	53	CH. 1 RESET
22	1553_2B–	54	CH. 1 TX INHIBIT
23	GND	55	N/C (NO USER CONNECTIONS ALLOWED)
24	1553_2B+	56	CH. 4 RESET
25	1553_2D+	57	CH. 4 TX INHIBIT
26	RT_ADD_D4	58	N/C (NO USER CONNECTIONS ALLOWED)
27	CH. 2 RESET	59	N/C (NO USER CONNECTIONS ALLOWED)
28	CH. 2 TX INHIBIT	60	N/C (NO USER CONNECTIONS ALLOWED)
29	RT_ADD_AP	61	N/C (NO USER CONNECTIONS ALLOWED)
30	CH. 3 RESET	62	N/C (NO USER CONNECTIONS ALLOWED)
31	GND	63	N/C (NO USER CONNECTIONS ALLOWED)
32	CH. 3 TX INHIBIT	64	N/C (NO USER CONNECTIONS ALLOWED)

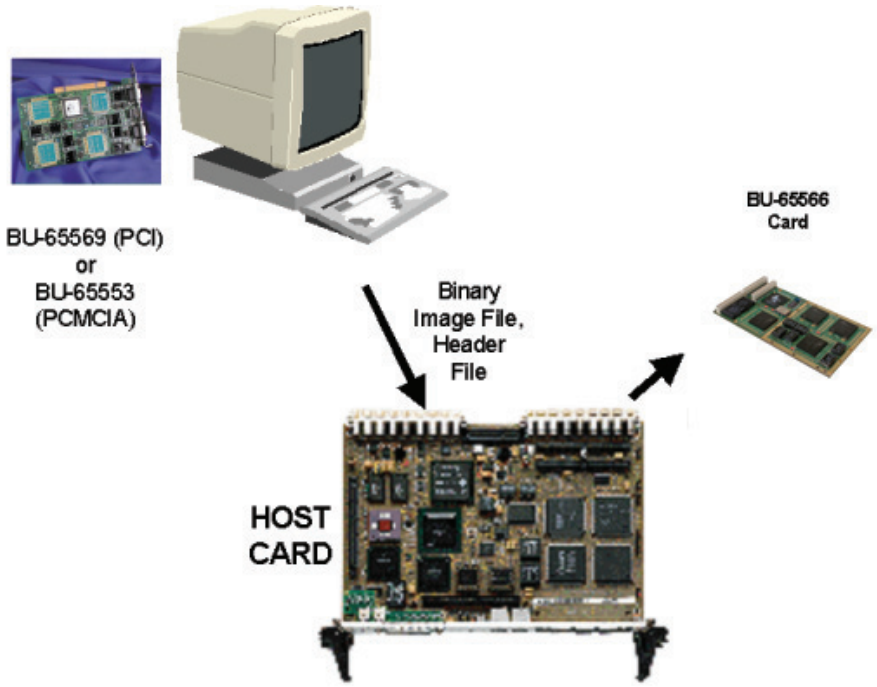
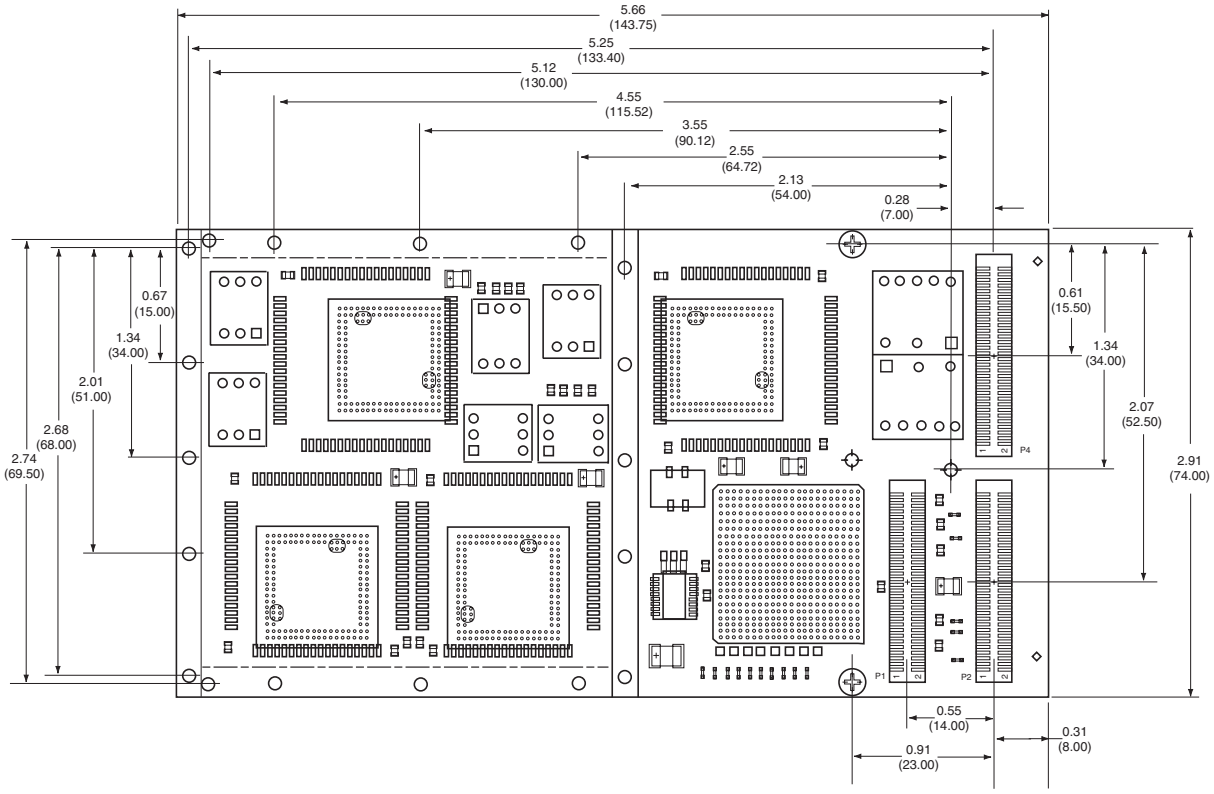
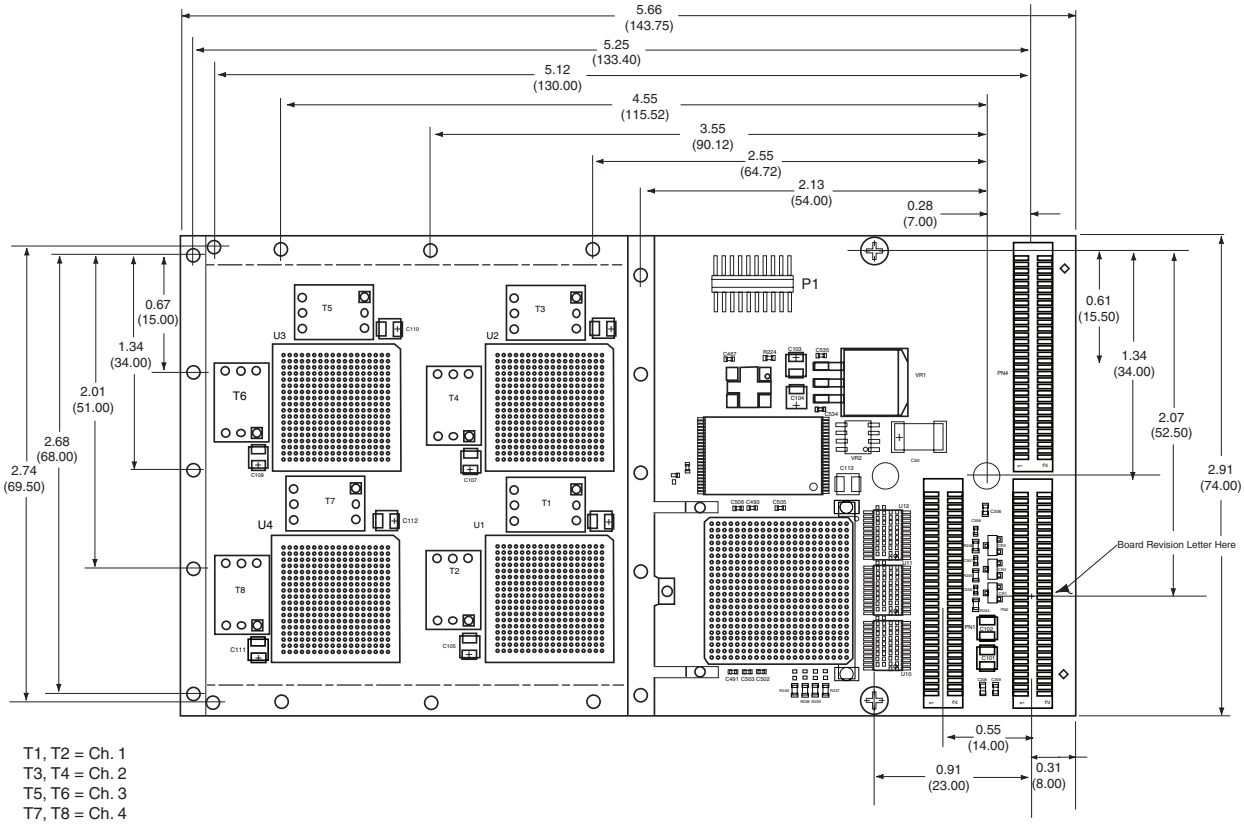


FIGURE 5. OFFLINE DEVELOPMENT ENVIRONMENT



DIMENSIONS ARE IN INCHES (MM)

FIGURE 6. BU-65566G (REV A) MECHANICAL OUTLINE



T1, T2 = Ch. 1
T3, T4 = Ch. 2
T5, T6 = Ch. 3
T7, T8 = Ch. 4

DIMENSIONS ARE IN INCHES (MM)

FIGURE 6. BU-65566G (REV B) MECHANICAL OUTLINE

ORDERING INFORMATION

BU-65566XX-X00X

Supplemental Process Requirement
N = Acrylic Conformal Coating
U = Polyurethane Conformal Coating
Blank = No Conformal Coating

Temperature Range:
2 = -40°C to +85°C (at thermal rail)
3 = 0°C to +55°C (at thermal rail)

Number of Channels:
1 = 1 Dual Redundant 1553 Channel
2 = 2 Dual Redundant 1553 Channels
3 = 3 Dual Redundant 1553 Channels
4 = 4 Dual Redundant 1553 Channels

Enhanced Mini-ACE Package Type:
G = Industrial/Commercial Version

Base Product:
BU-65566 = MIL-STD-1553 66MHz PMC Card

Note:

The above products contain tin-lead solder.

INCLUDED SOFTWARE

BU-69090 SX

Enhanced Mini-ACE API Library and Drivers
Operating System:
0 = Windows 95/98/2000/XP and Windows NT
1 = Linux
2 = VxWorks
5 = Integrity

OPTIONAL SOFTWARE

BU-69404DX

dataMARS Advanced Graphical Monitoring Software for Windows 95/98/2000/XP and Windows NT

OPTIONAL ACCESSORY

5980-0527-0001

Blank Front Panel Bezel for Air-Cooled Applications

STANDARD DDC PROCESSING FOR DISCRETE MODULES/PC BOARD ASSEMBLIES		
TEST	**METHOD(S)**	**CONDITION(S)**
INSPECTION / WORKMANSHIP	IPC-A-610	Class 3
ELECTRICAL TEST	DDC ATP	—

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