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BU-65569T/B
Hardware Manual
MIL-STD 1553 BC/RT/MT
CompactPCI Interface Card

MN-65569TX-001

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RECORD OF CHANGE

Revision	Date	Pages	Description
A	05/2002	All	Initial Release
B	09/2002	Various	Table 3, and RT Address Input Section added, plus various edits
C	11/2002	Various	Note added to Table 44, typographical errors corrected
D	2/2003	Various	Added Figure 5, and Table 4
E	5/2004	Various	Modified Tables 2 and 3, added Tables 3 and 4, renumbered Tables, misc edits.
F	6/2005	21	Figure 7, Simulated Bus Interconnections Updated
G	5/2009	118	Minor change to Storage temp in Table 57. General Layout update.

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1 PREFACE

This manual uses typographical conventions to assist the reader in understanding the content. This section will define the text formatting used in the rest of the manual.

1.1 Text Usage

- **BOLD** – text that is written in bold letters indicates important information and table, figure, and chapter references.
- ***BOLD ITALIC*** – will designate DDC Part Numbers.
- `Courier New –` is used to indicate code examples.
- <…> - Indicates user entered text or commands.

1.2 Special Handling and Cautions

The ***BU-65569T/B*** uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.



Turn off power to the PC and unplug from wall.
NEVER insert or remove card with power turned on.
Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.
Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

1.3 Trademarks

All trademarks are the property of their respective owners.

1.4 Special Notes

Unless otherwise noted, an asterisk after a signal name (i.e., MSTCLR*) denotes an active low signal.

1.5 Technical Support

In the event that problems arise beyond the scope of this manual, you can get in touch with DDC by calling:

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DDC also has an Internet World Wide Web site, which allows customers to easily download new revisions of software and documentation. The Internet address is **www.ddc-web.com**.

2 OVERVIEW

The ***BU-65569T/B*** is a single-channel or multi-channel MIL-STD-1553 CompactPCI card. The ***BU-65569T/B*** is available with one to four dual redundant Enhanced Miniature Advanced Communication Engine (Enhanced Mini-ACE™) MIL-STD-1553 channels and provides full, intelligent interfacing between the dual redundant MIL-STD-1553 Data Bus and a CompactPCI Bus. It is packaged on a 3U CompactPCI bus interface card.

The design of the ***BU-65569T/B*** leverages the BU-61864 Enhanced Mini-ACE. Each channel may be independently programmed for BC (Bus Controller), RT (Remote Terminal), Monitor, or RT/Monitor mode.

Advanced architectural features of the Enhanced Mini-ACE include a highly autonomous BC, an RT providing a wide variety of buffering options, and a selective message Monitor. Each Enhanced Mini-ACE channel incorporates 3.3 volt logic to reduce power consumption and 64K words of RAM.

The ***BU-65569T/B*** is supported by free software, including a 'C' or Runtime library, and drivers for Windows® 9x/2000/XP, Windows NT® and Linux. The libraries and drivers comprise a suite of C function calls that serves to offload a great deal of low-level tasks from the application programmer. This software supports all of the Enhanced Mini-ACE's advanced architectural features.

- 32-bit/33 MHz CompactPCI Card
- One to Four Dual Redundant MIL-STD-1553 Channels
- Enhanced Mini-ACE BC/RT/MT Architecture
- 64K-word RAM per Channel
- Highly Autonomous BC Architecture
- Conditional Messages
- Message Timing Control
- Bulk Data Transfers
- Data Block Double Buffering
- Retries and Bus Switching

- RT Buffering Options:
    - Single Buffering
    - Double Buffering
    - Subaddress Circular Buffering
    - Global Circular Buffering
- Selective Message Monitor
- Supports PCI Interrupts
- Windows 9x/2000/XP, Windows NT and Linux Software Driver

2.1 What is included in this manual?

This manual contains a detailed installation guide for the ***BU-65569T/B*** CompactPCI Card and a basic overview of the software supplied with the card. Library and Driver installations for Windows 9x/2000/XP, and Windows NT will be covered in the following sections.

The ACE family Library Software provides a level of abstraction such that it is not necessary to understand the operation of the Enhanced Mini-ACE chip set. This manual provides an introduction to the Enhanced Mini-ACE and ACE Libraries. Complete documentation for the Enhanced Mini-ACE Library is located in the ***BU-69090S0*** **Software Manual** and the ACE Library is provided in **the *BUS-69080S0* Software Manual**. For those who are interested in detailed information on the operation of the control registers and memory mapped data structures, a copy of the Enhanced Mini-ACE User's Guide may be obtained from the DDC web site at **www.ddc-web.com**.

3 HARDWARE INSTALLATION

The ***BU-65569T/B*** card may be inserted into any CompactPCI compatible slot. When installing the card, the following should be observed:

NEVER insert or remove the card with the power turned on.

ALWAYS take proper precautions to guard against static damage. Use a wrist strap if available, or ensure proper static grounding by touching the power supply cover WITH POWER OFF.

Insert the card and gently press the card into the motherboard connector. Secure with proper hardware.

Make sure that adjacent cabling and wiring does not hinder the airflow around the card.

The ***BU-65569T/B*** contains jumper blocks that allow for transformer or direct coupling for each bus connection. There are no jumpers or switches to be set for address and interrupt selection. This card is designed as a Plug-and-Play device and as such, these parameters can only be changed using the Control Panel application provided with the software.

Note: *If a B model card is used, do not install the card in a 64-bit CompactPCI bus. Card and system damage can occur.*

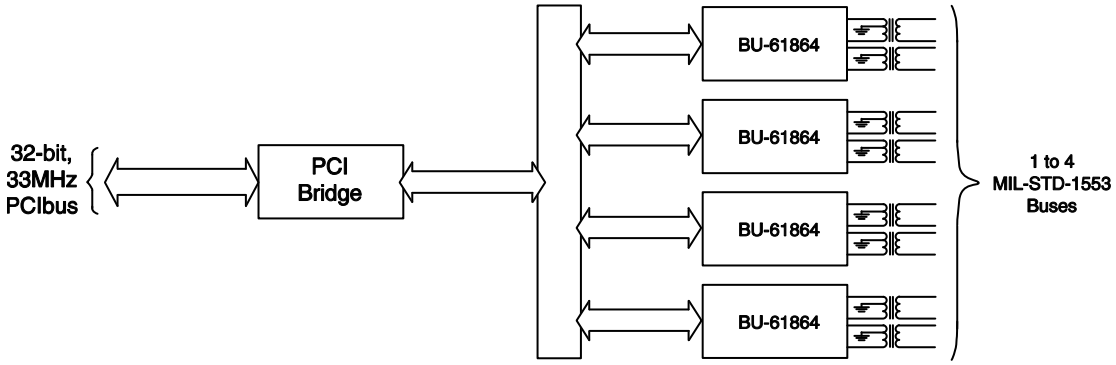
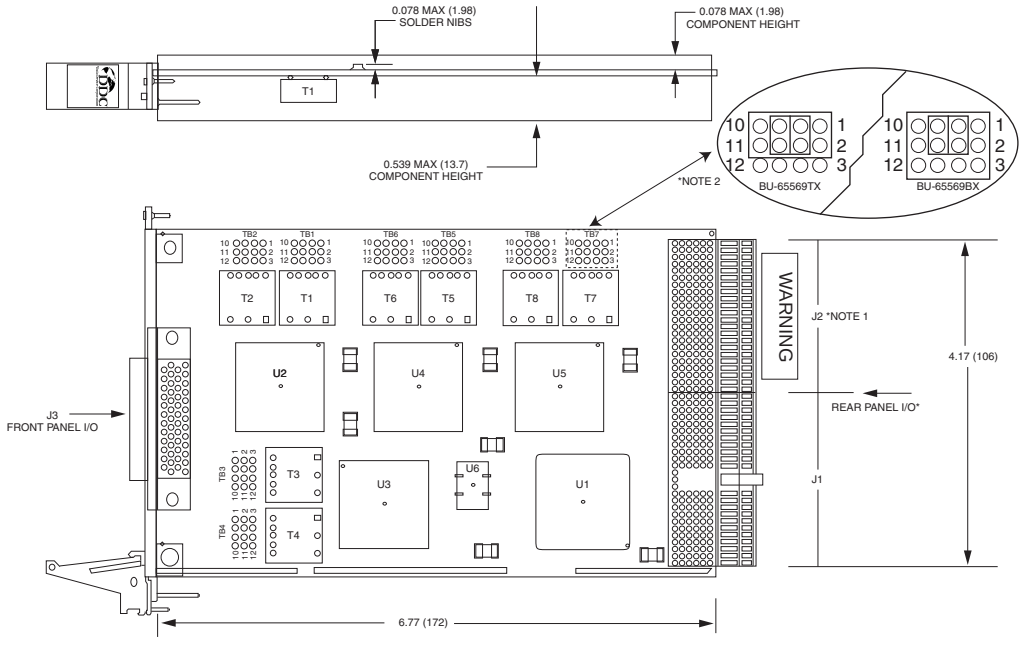


Figure 1. BU-65569T/B Block Diagram

4 HARDWARE CONFIGURATION

The ***BU-65569T/B*** is a true CompactPCI device, and as such does not require any jumpers or switches to set the Base address or interrupt values. The job of configuration for Plug-and-Play PCI configuration is performed by the PC BIOS. During the initial power on boot process, the BIOS performs an enumeration of the PCI bus and locates a configuration in the system that satisfies the card requirements. The card communicates to BIOS how much memory it requires, the interrupts that it supports, and any other operating parameters that the system needs to know by way of configuration registers built into the card. These registers are configured at the factory to contain the optimum values for the operation of the ***BU-65569T/B***. There is no need for the user to provide a specific memory location or size, or have to juggle interrupts to get their MIL-STD-1553 card installed. The PCI allows for shared interrupts, which are implemented in the ***BU-65569T/B***. The device driver that is provided with the hardware can determine which of the 1-4 Enhanced Mini-ACE devices on the ***BU-65569T/B*** generated the interrupt, and acts accordingly.



NOTES
1. J2 is a Type B, 22 column CompactPCI connector and is only installed on the BU-65569Bx card (Rear Panel I/O).
2. If using the BU-65569Tx board only the top two rows of jumpers (2x4 header) will be installed. The BU-65569Bx is supplied with three rows of jumpers (3x4 header). These pins are used to route the I/O signals to the appropriate connector, either J2 or J3.
3. Dimensions are in inches (mm).

Figure 2. *BU-65569T/B* Mechanical Outline

4.1 Bus Coupling Mode

The ***BU-65569T/B*** can be interfaced to a MIL-STD-1553 bus in either Direct or Transformer-coupled mode. The two modes are configured via eight jumper blocks labeled TB1 through TB8 on the card (refer to **Figure 3).**

In the T configuration (front panel only) two rows of jumpers are available: (F)ront, the top row, and (S)ource, the bottom row. In the B configuration (front and back panels) there are three rows of jumpers installed on the card. This version has an additional row of pins: (B)ack, which indicates the bottom row. With this board option, the user can select between routing the I/O to **either** the Front **or** Back panel connectors.

TB1-TB2: 1553 Channel 1 A and B coupling options.

TB3-TB4: 1553 Channel 2 A and B coupling options.

TB5-TB6: 1553 Channel 3 A and B coupling options.

TB7-TB8: 1553 Channel 4 A and B coupling options.

The corresponding pin outs apply to channels 1-4, jumpers TB1, TB2, TB3, TB4, TB5, TB6, TB7 and TB8. See **Figure 3**.

	D1	X1	X2	D2
F	O	O	O	O
S	O	O	O	O
B	O	O	O	O

Figure 3. ***TBx Jumper Configuration***

Table 1. Jumper Settings	
Pin Connections	**Function**
TBX **D1-F**ront to **D1-S**ource	Bus - Direct-Coupled Positive
TBX **X1-F**ront to **X1-S**ource	Bus - Transformer Coupled Positive (factory default)
TBX **X2-F**ront to **X2-S**ource	Bus - Transformer Coupled Negative (factory default)
TBX **D2-F**ront to **D2-S**ource	Bus - Direct Coupled Negative

Note: *Both buses on the same channel should be either direct or transformer coupled. Terminal blocks 1, 3, 5, 7 are bus A of their respective channels and blocks 2, 4, 6, 8 are bus B.*

Note: *If the card is a B model and back panel I/O is required, connect the respective channels' jumpers to the (B)ack and (S)ource positions.*

Note: *If a B model card is used, do not install the card in a 64-bit CompactPCI bus. Card and system damage can occur.*

Table 2. Pin Descriptions Front (J3) and Back (J2) Panel Connectors

Signal	Front (J3) pins	Back (J2) pins
CH1A	46	D3
CH1A_L	45	A4
CH1B	47	C10
CH1B_L	48	E10
CH2A	9	C6
CH2A_L	7	E6
CH2B	5	B9
CH2B_L	3	D9
CH3A	23	D5
CH3A_L	21	B5
CH3B	17	E4
CH3B_L	15	C4
CH4A	24	C12
CH4A_L	25	D11
CH4B	49	A9
CH4B_L	50	A6
SSFLAG_L_BCTRIG1	18	D13
SSFLAG_L_BCTRIG2	10	C13
SSFLAG_L_BCTRIG3	29	B13
SSFLAG_L_BCTRIG4	8	E12
CH1_RTAD4	44	E3
CH1_RTAD3	20	D4
CH1_RTAD2	16	C5
CH1_RTAD1	39	B6
CH1_RTAD0	19	A7

Table 2. Pin Descriptions Front (J3) and Back (J2) Panel Connectors		
Signal	**Front (J3) pins**	**Back (J2) pins**
CH1_RTADP	42	A8
CH2_RTAD4	1	D10
CH2_RTAD3	30	C11
CH2_RTAD2	13	B12
CH2_RTAD1	2	A13
CH2_RTAD0	32	E13
CH2_RTADP	4	E9
CH3_RTAD4	26	A12
CH3_RTAD3	27	E11
CH3_RTAD2	31	B11
CH3_RTAD1	34	A11
CH3_RTAD0	28	B10
CH3_RTADP	6	A10
CH4_RTAD4	38	E8
CH4_RTAD3	37	C7
CH4_RTAD2	33	B7
CH4_RTAD1	43	E5
CH4_RTAD0	11	A5
CH4_RTADP	22	B4
GROUND	12	C9
GROUND	14	D12
GROUND	35	D6
GROUND	36	E7
GROUND	40	-
GROUND	41	-

Table 3. J2 CompactPCI Connector Pinout (*BU-65569B* ONLY)							
PIN	**Z**	**A**	**B**	**C**	**D**	**E**	**F**
22 • • • 14	GND	NC	NC	NC	NC	NC	GND
13	GND	CH2_RTAD1	SSFLAG_L_BCTRIG_3	SSFLAG_L_BCTRIG_2	SSFLAG_L_BCTRIG_1	CH2_RTAD0	GND
12	GND	CH3_RTAD4	CH2_RTAD2	CH4A	GND	SSFLAG_L_BCTRIG4	GND
11	GND	CH3_RTAD1	CH3_RTAD2	CH2_RTAD3	CH4A_L	CH3_RTAD3	GND
10	GND	CH3_RTADP	CH3_RTAD0	CH1B	CH2_RTAD4	CH1B_L	GND
9	GND	CH4B	CH2B	GND	CH2B_L	CH2_RTADP	GND
8	GND	CH1_RTADP	NC	NC	NC	CH4_RTAD4	GND
7	GND	CH1_RTAD0	CH4_RTAD2	CH4_RTAD3	NC	GND	GND
6	GND	CH4B_L	CH1_RTAD1	CH2A	GND	CH2A_L	GND
5	GND	CH4_RTAD0	CH3A_L	CH1_RTAD2	CH3A	CH4_RTAD1	GND
4	GND	CH1A_L	CH4_RTADP	CH3B_L	CH1_RTAD3	CH3B	GND
3	GND	NC	NC	NC	CH1A	CH1_RTAD4	GND
2	GND	NC	NC	NC	NC	NC	GND
1	GND	NC	NC	NC	NC	NC	GND

Table 4. J3 Front Panel Connector Pinout			
PIN NUMBER	**DESCRIPTION**	**PIN NUMBER**	**DESCRIPTION**
1	CH2_RTAD4	26	CH3_RTAD4
2	CH2_RTAD1	27	CH3_RTAD3
3	CH2B_L	28	CH3_RTAD0
4	CH2_RTADP	29	SSFLAG_L_BCTRIG3
5	CH2B	30	CH2_RTAD3
6	CH3_RTADP	31	CH3_RTAD2
7	CH2A_L	32	CH2_RTAD0
8	SSFLAG_L_BCTRIG4	33	CH4_RTAD2
9	CH2A	34	CH3_RTAD1
10	SSFLAG_L_BCTRIG2	35	GND
11	CH4_RTAD0	36	GND
12	GND	37	CH4_RTAD3
13	CH2_RTAD2	38	CH4_RTAD4
14	GND	39	CH1_RTAD1
15	CH3B_L	40	GND
16	CH1_RTAD2	41	GND
17	CH3B	42	CH1_RTADP
18	SSFLAG_L_BCTRIG1	43	CH4_RTAD1
19	CH1_RTAD0	44	CH1_RTAD4
20	CH1_RTAD3	45	CH1A_L
21	CH3A_L	46	CH1A
22	CH4_RTADP	47	CH1B
23	CH3A	48	CH1B_L
24	CH4A	49	CH4B
25	CH4A_L	50	CH4B_L

Notes:
Signal naming convention:
1553 Bus Signals:
CH_X - X indicates the Channel, a BU-65569TX can have between 1 and 4 channels.A or B indicates one of the two 1553 BUSES associated with each channel. + or - indicates the phase of the 1553 BUS signal, (positive or negative).
RT Address Signals:
CHn_RTADX - where X indicates one of 5 RT Address bits (4:0) or the parity bit, and n indicates the Channel, (1-4).

Table 5. J1 CompactPCI Connector Pinout							
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**
1	GND	+5V	NC	NC	NC	+5V	GND
2	GND	NC	+5V	NC	TD0	TDI	GND
3	GND	INTA_L	NC	NC	+5V	NC	GND
4	GND	NC	HEALTHY #	NC	NC	NC	GND
5	GND	NC	NC	RESET_L	GND	GNT_L	GND
6	GND	REQ_L	GND	+3.3V	CLOCK	AD(31)	GND
7	GND	AD(30)	AD(29)	AD(28)	GND	AD(27)	GND
8	GND	AD(26)	GND	V(I/O)	AD(25)	AD(24)	GND
9	GND	C/BE3_L	IDSEL	AD(23)	GND	AD(22)	GND
10	GND	AD(21)	GND	+3.3V	AD(20)	AD(19)	GND
11	GND	AD(18)	AD(17)	AD(16)	GND	C/BE2_L	GND
12	KEY AREA						
13							
14							
15	GND	+3.3V	FRAME_L	IRDY_L	NC	TRDY_L	GND
16	GND	DEVSEL_L	GND	V(I/O)	STOP_L	LOCK#	GND
17	GND	+3.3V	NC	NC	GND	PERR_L	GND
18	GND	SERR_L	GND	+3.3V	PAR	C/BE1_L	GND
19	GND	+3.3V	AD(15)	AD(14)	GND	AD(13)	GND
20	GND	AD(12)	GND	V(I/O)	AD(11)	AD(10)	GND
21	GND	+3.3V	AD(09)	AD(08)	NC	C/BEO_L	GND
22	GND	AD(07)	GND	+3.3V	AD(06)	AD(05)	GND
23	GND	+3.3V	AD(04)	AD(03)	+5V	AD(02)	GND
24	GND	AD(01)	+5V	V(I/O)	AD(00)	NC	GND
25	GND	+5V	NC	NC	+3.3V	+5V	GND

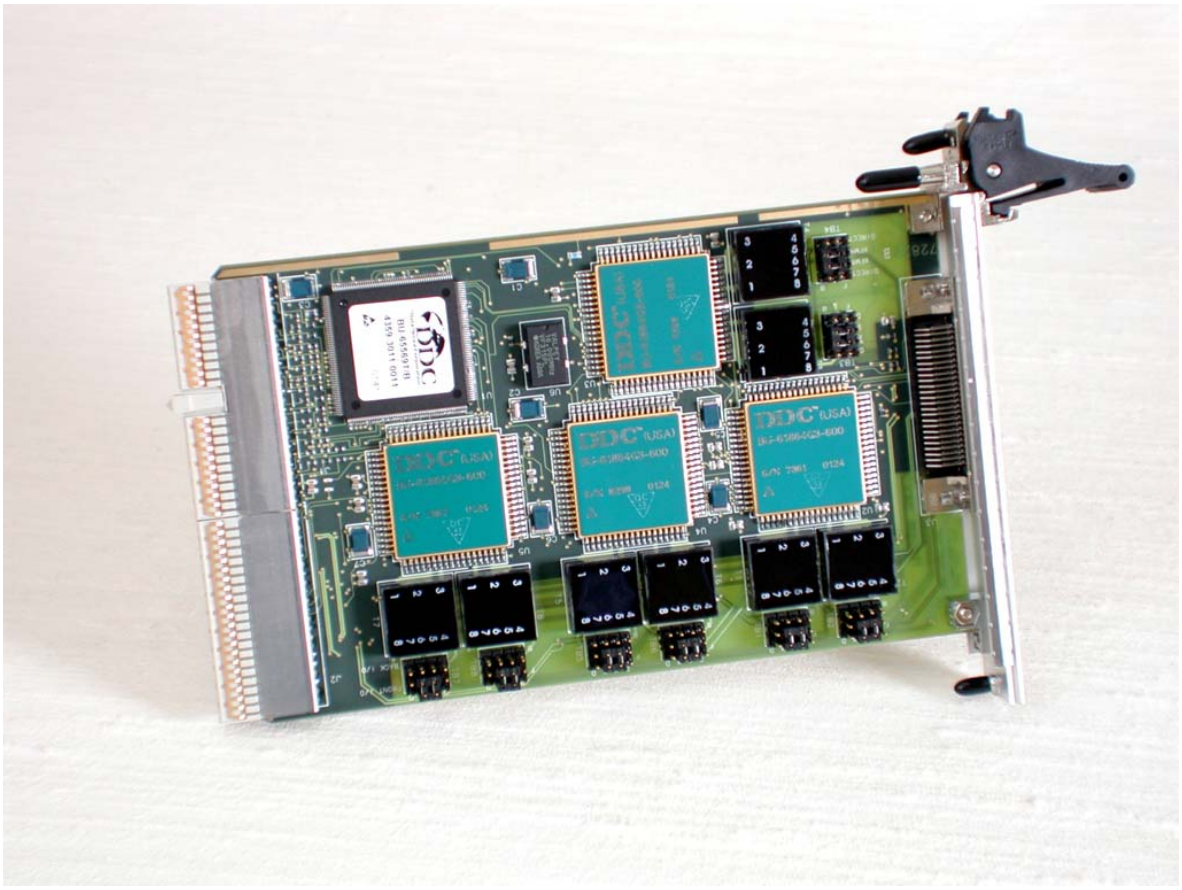


Figure 4. *BU-65569B* Model Photo

4.2 DISCRETE I/O CONNECTOR "J3"

Models BU-65569T/B include a Front-Panel mounted Discrete I/O connector "J3". This connector (Soldered on the board) is a 50-pin "Subminiature D Type" (Amp P/N 787170-5). Pin numbering designations for "J3" are as shown.

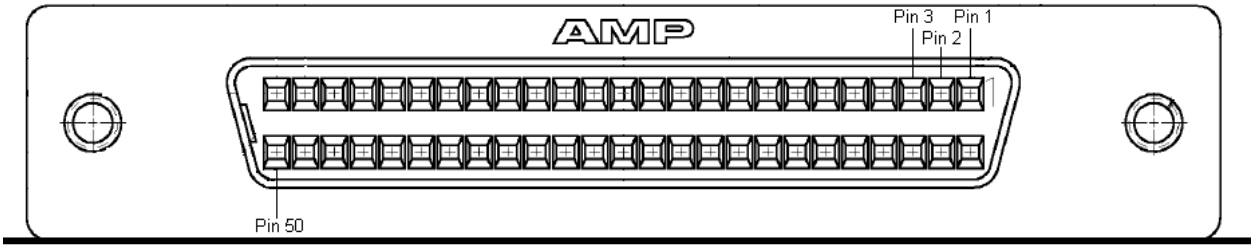


Figure 5. 50-Pin "J3" I/O Connector (As viewed from BU-65569T/B Front-Panel)

Models BU-65569T/B are shipped with "J3" mating connector and backshell are listed in the Table below.

Table 6. Supplied I/O Connector Components

Description	AMP #	Quantities
PLUG ASSEMBLY, AMPLIMITE .050 Series	749111-4	1
BACKSHELLS WITH MALE JACKSCREWS, 50 POSITION AMPLIMITE .050 Series	749080-1	1

4.3 RT Address Inputs

The RT addresses on the BU-65569T/B card can be set via either hardware or software. The RT address pins are 5V tolerant and are internally pulled up. If the RT address is assigned via these pins it is recommended that these pins be actively driven low/high, or be connected directly to VCC/GND or be pulled up (resistors less than 10K ohms)/shorted to GND.

The INTERNAL RT_AD_LAT (RT Address Latch) signal will go from Low to High shortly after the de-assertion of the PCI Reset signal. This will cause the RT address bits (which are brought out to the front/rear connector, depending upon option ordered) to be latched into the Enhanced Mini-ACE parts on the board.

After this point, the software can override this address by one of two methods.

The RT address may be "relatched" from RTAD4-RTAD0 and RTADP under software control. This operation is performed as follows:

a. Program ENHANCED MODE (bit 15 of Configuration Register #3) to logic "1".

b. Program RT ADDRESS SOURCE (bit 5 of Configuration Register #6) to logic "0".

c. Program LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5 (bit 3 of Configuration Register #4) to logic "1".

d. Perform a write operation to Configuration Register #5. This will cause the Enhanced Mini-ACE's RT address to be latched from the values presented on RTAD4-RTAD0 and RTADP.

Note: *For this operation, the logic values written by the host (on D5-D0)* ***do not*** *effect the value of the Enhanced Mini-ACE's internal RT address.*

e. To prevent the RT address from being inadvertently overwritten by a subsequent write to Configuration Register #5, it is recommended to then program LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5 (bit 3 of Configuration Register #4) to logic "0".

The second method allows for a fully software programmable RT address. This operation is performed as follows:

a. Program ENHANCED MODE (bit 15 of Configuration Register #3) to logic “1”.

b. Program RT ADDRESS SOURCE (bit 5 of Configuration Register #6) to logic “1”.

c. Program LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5 (bit 3 of Configuration Register #4) to logic “1”.

d. Perform a write operation to Configuration Register #5. The value of the Enhanced Mini-ACE’s internal RT address bits 4-0 will be latched from processor data bus bits 5-1 (D5-D1), and internal RTADP to be latched from processor data bus bit 0 (D0).

e. To prevent the RT address from being inadvertently overwritten by a subsequent write to Configuration Register #5, it is suggested to then program LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5 (bit 3 of Configuration register #4) to logic “0”.

Please refer to the “RT Address Inputs” section of the “Enhanced Mini-ACE Users Guide” for more information.

4.4 SSFLG*/EXT_TRIG_X inputs

These pins are an optional input for each Enhanced Mini-ACE part. These inputs are 5V tolerant and are internally pulled up. This pin can serve as either the subsystem flag in RT mode (with standard status word) or external trigger in BC/Word monitor mode.

In RT mode with standard status word, if this input is asserted low, the Subsystem Flag bit will be set in the Enhanced Mini-ACE’s RT Status Word. If the SSFLAG* input is logic “0” while bit 8 of Configuration Register #1 has been programmed to logic “1” (cleared), the Subsystem Flag RT Status Word bit will become logic “1”, but bit 8 of Configuration Register #1, SUBSYSTEM FLAG*, will return logic “1” when read. That is, the sense on the SSFLAG* input **has no effect** on the SUBSYSTEM FLAG* register bit. This input has no meaning in RT mode with alternate status word.

In the non-enhanced BC mode, this signal operates as an External Trigger input. In BC mode, if the external BC Start option is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a BC Start command, starting execution of the current BC frame.

In the enhanced BC mode, during the execution of a Wait for External Trigger (WTG) instruction, the Enhanced Mini-ACE BC will wait for a low-to-high transition on EXT_TRIG before proceeding to the next instruction.

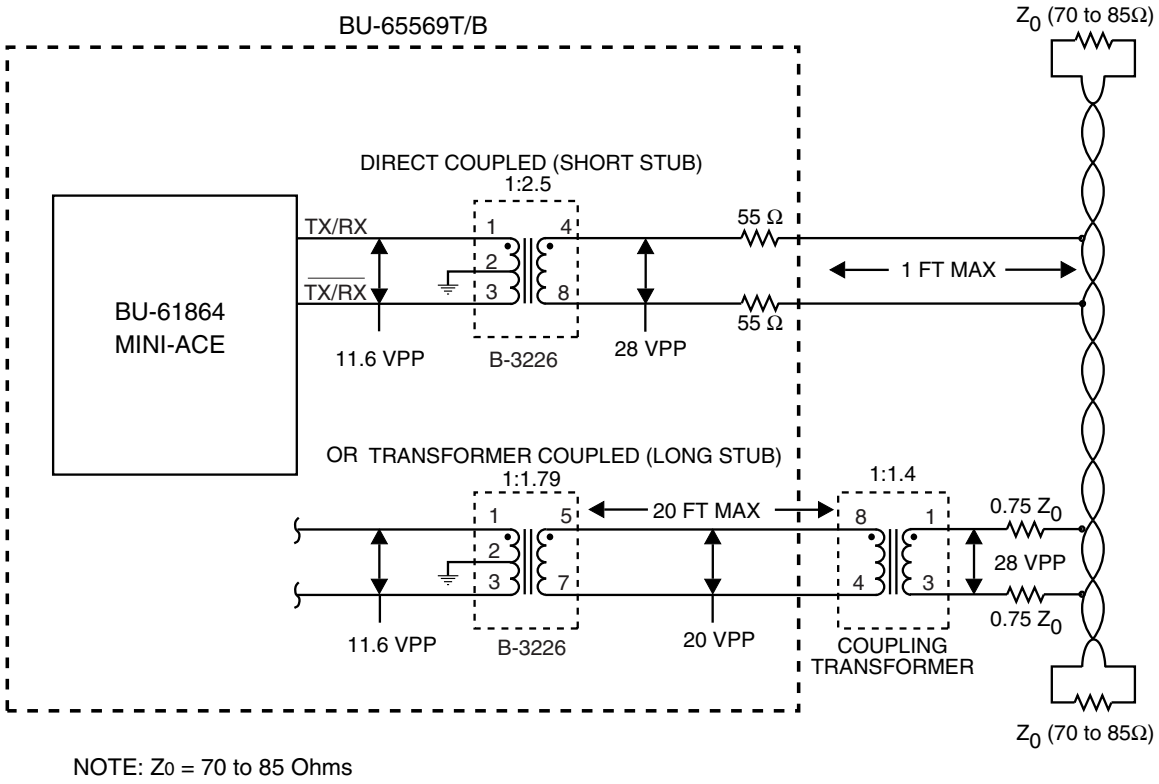
Please refer to the Configuration Register 1 section of the “Enhanced Mini-ACE Users Guide” for more detailed information.

4.5 Interface to a MIL-STD-1553 Bus

Figure 6 on page **17** illustrates the interface from the ***BU-65569T/B*** to a MIL-STD-1553 bus for either transformer (long stub) or direct (short stub) coupling, plus the peak-to-peak voltage levels that appear at various points (when transmitting). Note that this diagram is applicable for each of the four terminals available on the card. Each ***BU-65569T/B*** terminal/channel pair can be switched to use either transformer or direct coupling by configuring the correct jumper (refer to “Bus Coupling Mode” on page 6).

Both transformer- and direct-coupled configurations require the use of an isolation transformer that is located on the ***BU-65569T/B*** card. For the transformer (long stub) coupling configuration, a second transformer (referred to as a bus-coupling transformer) is required to connect to the 1553 bus. The isolation resistors are housed inside of the bus coupler. The bus coupler is not supplied with the card. In accordance with MIL-STD-1553B, the turns ratio of the coupling transformer is 1.0:1.4.

Both coupling configurations also require an isolation resistor to be placed in series with each leg of the transformer connecting to the 1553 bus; this protects the bus against short circuit conditions in the transformers, stubs, or terminal components. For the direct-coupled mode, these isolation resistors are supplied on the ***BU-65569T/B*** card. For the transformer-coupled mode, the bus coupler supplies these resistors.



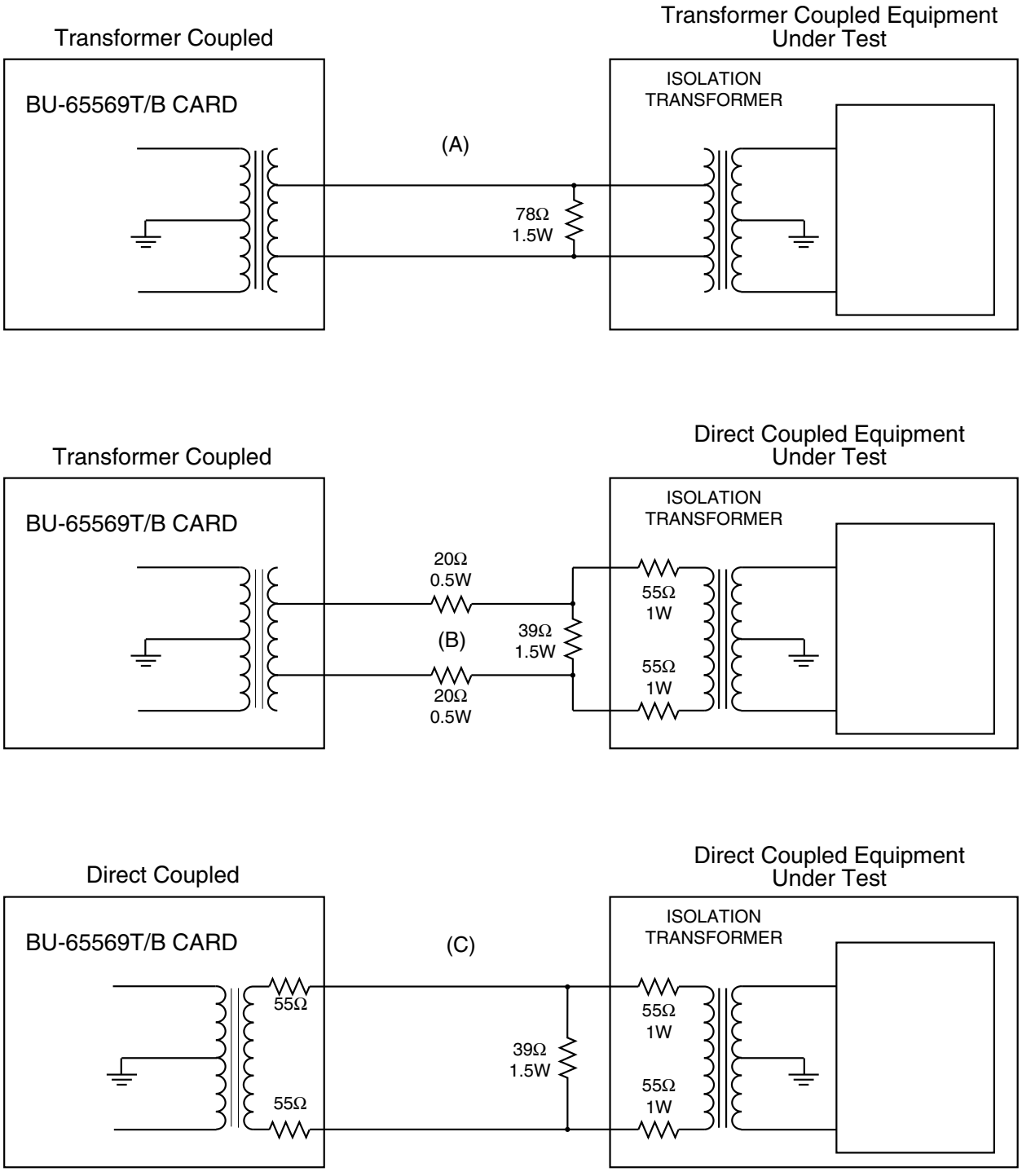
NOTE: Z_0 = 70 to 85 Ohms

Figure 6. BU-65569T/B Interface to a MIL-STD-1553 Bus

4.6 "Simulated Bus" (Lab Bench) Interconnections

For purposes of software development and system integration, it is generally not necessary to integrate with the required couplers, terminators, etc. that comprise a complete MIL-STD-1553B bus. In most instances, a simplified electrical configuration will suffice. The interconnection methods illustrated in Figure 7 allow the ***BU-65569T/B*** CompactPCI Card to be interfaced over a "simulated bus" to simulation and test equipment. The length of this "simulated bus" should not exceed 5 feet.

It is important to note **that the termination resistors indicated are necessary** (if not already present within the test/simulation equipment) in order to ensure reliable communications between the CompactPCI Card and the simulation/test equipment. As illustrated in Figure 7, the 78 ohm and the 39 ohm termination resistors should be physically located as close as possible to the test/simulation equipment.



(A) Transformer Coupled-to-Transformer Coupled
(B) Transformer Coupled-to-Direct Coupled
(C) Direct Coupled-to-Direct Coupled

Figure 7. Simulated Bus Interconnections

5 SOFTWARE INSTALLATION

5.1 Enhanced Mini-ACE Software Library Compatibility

The ***BU-65569T/B*** card is compatible with the ***BUS-69080*** ACE software. To use the enhanced properties of the ***BU-65569T/B*** card the 32-Bit Enhanced Mini-ACE Runtime Library series ***BU-69090*** libraries must be used. The libraries and requirements are described in Table 7.

Table 7. ACE/Enhanced Mini-ACE Software

Part Number	Description	Requirements
BU-69090S0	32-Bit Enhanced Mini-ACE Runtime Library and Device Drivers	Win 9x/NT/2000/XP 486 or better CPU
BU-69090S1	32-Bit Enhanced Mini-ACE Software for Linux	Linux 486 or better CPU
BU-69090S2	32-Bit Enhanced Mini-ACE Software Toolbox for VxWorks	VxWorks 486 or better CPU
BUS-69082S0	32-Bit ACE Runtime Library and Device Drivers	Win 95/98 486 or better CPU
BUS-69083S0	32-Bit ACE Runtime Library and Device Drivers	Win NT/2000/XP 486 or better CPU
BUS-69084S0	32-Bit ACE Menu Software	Win 95/98 486 or better CPU
BUS-69085S0	32-Bit ACE Menu Software	Win NT/2000/XP 486 or better CPU

5.2 Software Driver Installation Overview

The ***BU-65569T/B*** CompactPCI Card is supplied with Drivers, Runtime Libraries, and a Windows Menu for Windows 9x/2000/XP and Windows NT. Please note that the 16-bit versions of the library and menu are not supplied and they are not supported for the PCI version of the ACE hardware. The basic installation for Windows 9x/2000/XP is listed below. Refer to page 24 for Windows NT installation instructions.

Windows 9x/2000/XP will recognize new hardware and ask for a driver disk.

Note: *16-bit is not supported.*

Insert DDC's **Data Bus Software CD** into the appropriate drive or, if using floppy disks, insert disk 1 into the appropriate drive, and run the setup.exe program.

Supply the necessary information during setup.

5.2.1 Driver Installation – Windows 9x/2000/XP

If you have Windows 9x/2000/XP use the following installation instructions. If you are using Windows NT refer to page 24.

Note: *User must have administrator rights when using Windows 2000/XP.*

1) Install the card as described in the beginning of the **HARDWARE INSTALLATION** section.

2) Turn on the computer.

3) The **Found New Hardware Wizard** window will appear after boot-up:

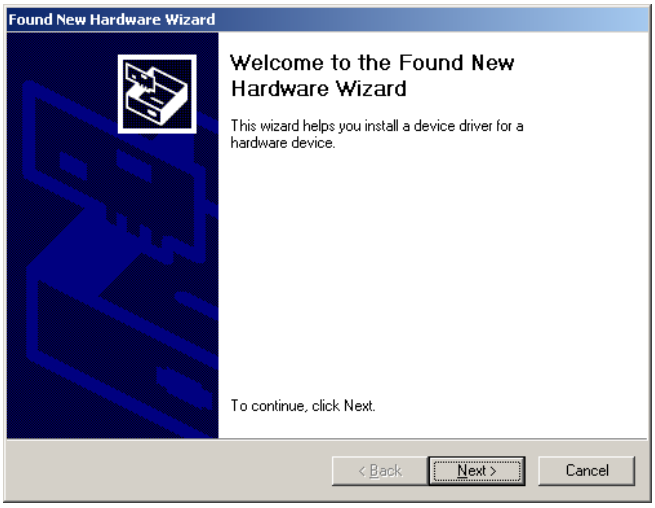


Figure 8. Found New Hardware

4) Click on the **Next** button.



Figure 9. Search for Driver

5) Click on Search for a suitable driver for my device.

6) Click on the **Next** button.

7) Insert the **Data Bus Software CD** or, if using floppy disks, disk 1 (or the “Drivers” disk, if provided) into the appropriate drive.

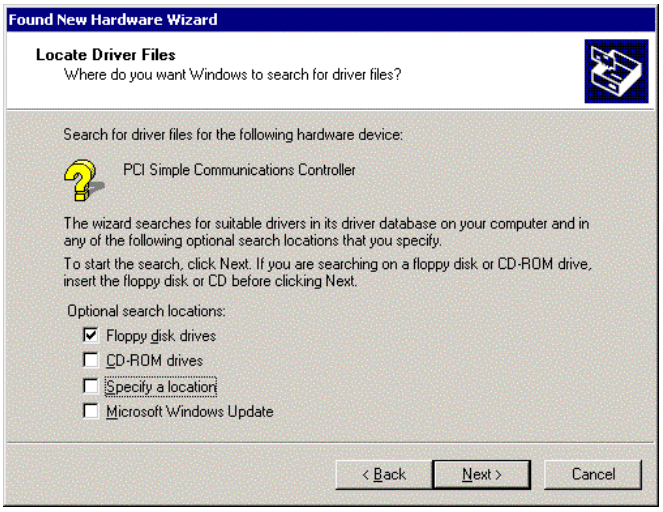


Figure 10. Specify Driver Location

8) Select the Checkbox for the appropriate drive type option, or select the **Specify a location** option to browse for the driver. **Figure 10** illustrates a dialog box for a floppy disk drive type option.



Figure 11. Found Driver

9) Once the driver has been located, click on the **Next** button to install the device driver.

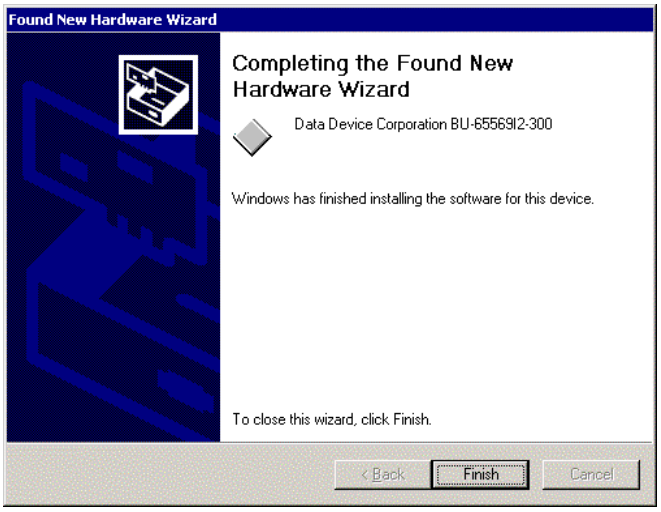


Figure 12. Finished Install of Driver

10) Click on the **Finish** button to confirm the installation.

11) Continue configuring the device by installing the Enhanced Mini-ACE and ACE Runtime Libraries. Refer to page 27 and page 31.

5.2.2 Driver Installation – Windows NT

5.2.2.1 Installation

The installation for the drivers, Enhanced Mini-ACE and ACE libraries is slightly different for Windows NT than it is for Windows 9x/2000/XP. Windows NT 4.0 will not automatically recognize the ***BU-65569T/B*** even though it is a PnP CompactPCI card. The drivers will be installed with the rest of the **Enhanced Mini-ACE** or **ACE Runtime Library** when the installation program is run from the CD.

Note: *User must have administrator rights when using Windows NT.*

After the hardware is installed in the PC, install the driver and library by selecting the appropriate package from the **Data Bus Software CD**. This will install the system files, the library files and the control panel **DDC 1553 Card Manager**. When the setup program is running, a dialog will be presented to the user to select the card type to install. If the computer has multiple ACE cards, select one type now. Other cards may be installed later using the **DDC 1553 Card Manager**, which is located under Control Panel.

Note: *If a previous version of software has already been installed the user will be prompted to uninstall the older version. Uninstallation of the old version is recommended. Check our web site at www.ddc-web.com for the latest software.*

After the Setup program is finished, reboot the computer.

5.2.2.2 Final Installation Procedures

The final steps in installing the new ACE software require the device number selection for each installed card. This is performed via the control panel **DDC 1553 Card Manager**. Access the control panel and double click on the **DDC 1553 Card Manager**. When the applet is opened, the status of any installed cards is displayed.

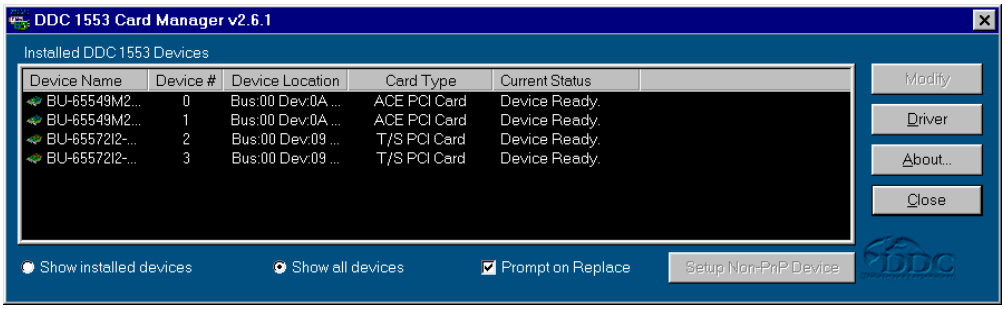


Figure 13. 1553 Card Manager

There are four buttons to the right side of the dialog box, and a status window in the center. The four buttons are **MODIFY**, **DRIVER**, **ABOUT**, **CLOSE**. The 3rd column, device location, consists of the PCI Bus, PCI Device and board channel number.

Note: *The **Modify** button presents a dialog that allows the device number to be selected and modified. A different device number can be selected for each channel on the card. **A device must be selected before the Modify operation can be completed**.*

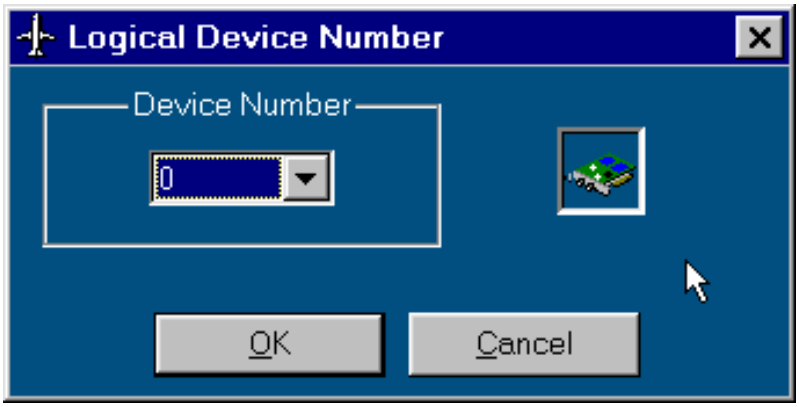


Figure 14. 1553 Card Manager Modify Device Number

The **Driver** button presents a dialog that shows the status of the installed drivers. Note that the version numbers are subject to change.

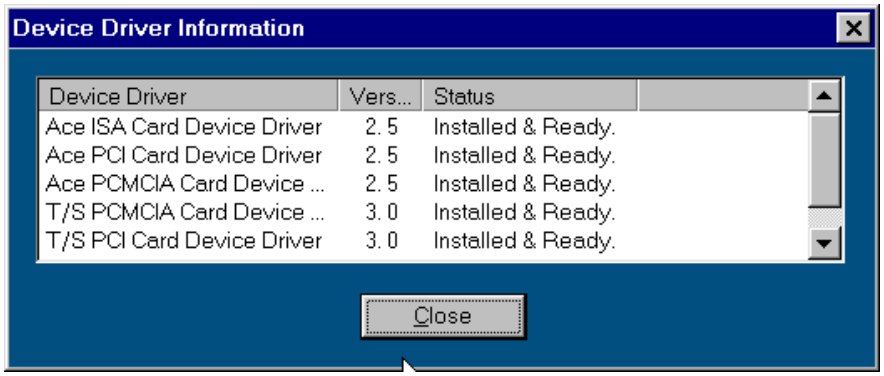


Figure 15. 1553 Card Manager Driver

The **About** button shows the version of the **DDC 1553 Card Manager**.



Figure 16. About DDC 1553 Card Manager

Pressing the 1553 CARD MANAGER **Close** button will cause all changes to be saved, and the **DDC 1553 Card Manager** dialog to be closed. This action will return to the previous process.

5.3 *BU-69090S0* Enhanced Mini-ACE Runtime Library (RTL)

5.3.1 Enhanced Mini-ACE RTL Installation - Windows 9x/2000/XP

5.3.1.1 CD-ROM Installation:

1) Insert the **Data Bus Software CD** into the appropriate drive and allow to autorun.

2) Select the card type, then the software type.

3) Click on the Install Software icon, then refer to the InstallShield wizard instructions below.

5.3.1.2 Floppy Disk Installation:

1) From the ***BU-69090S0*** installation disk set, insert disk 1 into the appropriate drive.

2) Run the setup.exe program, then refer to the InstallShield wizard instructions below.

5.3.1.3 InstallShield Wizard Instructions:

1) The InstallShield wizard will launch the Welcome screen. Click Next to continue.

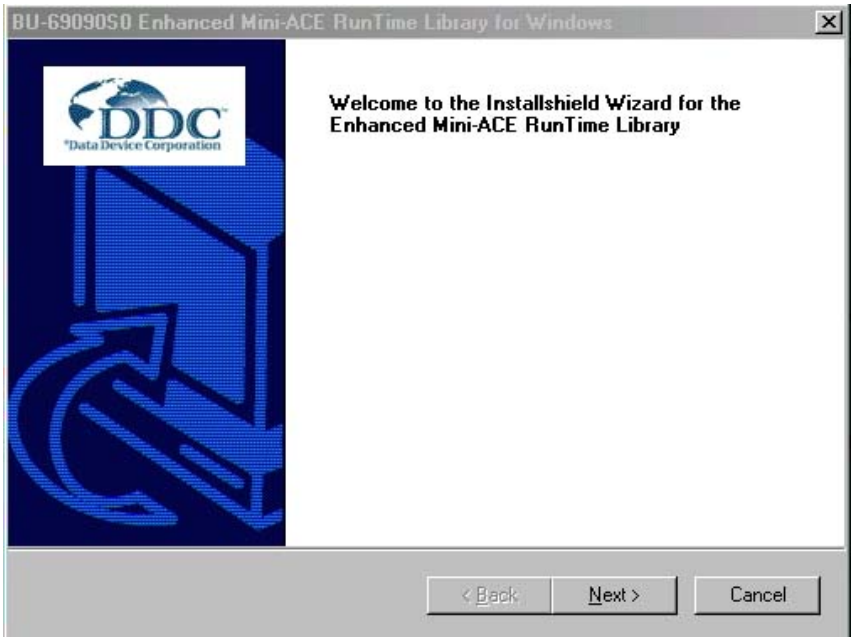


Figure 17. Welcome Screen

2) After reading the License Agreement click Yes to accept the terms, or No to disagree with them. (Choosing No will end the installation).

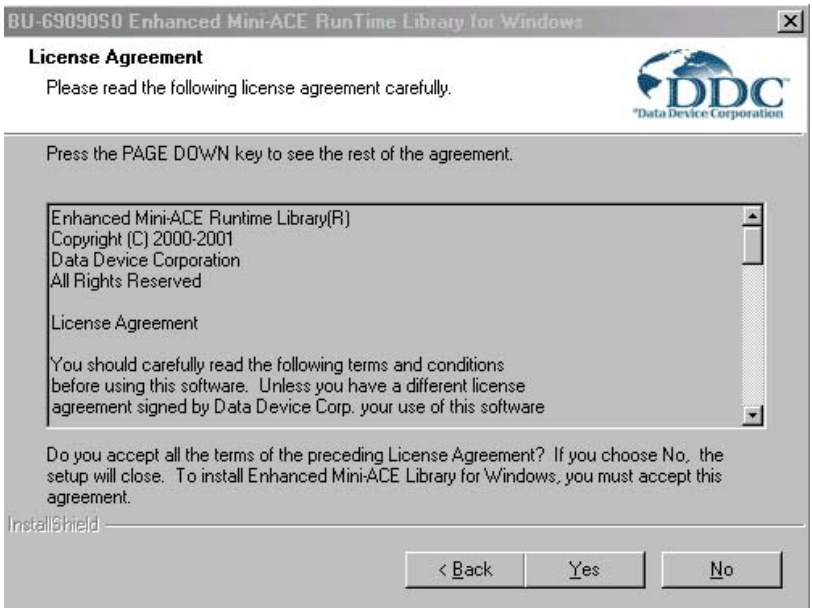


Figure 18. Software License Agreement

Note: *If a previous version of software has already been installed the user will be prompted to uninstall the older version. Uninstallation of the old version is recommended. Check our web site at www.ddc-web.com for the latest software.*

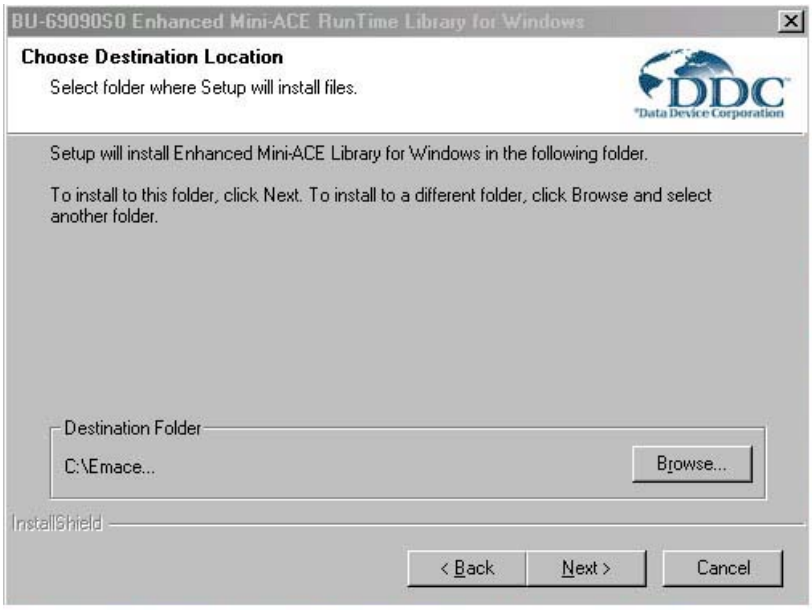


Figure 19. Destination Folder

3) Click Next to choose the default installation folder, or Browse to locate a custom folder destination.

4) Click Next to choose the default Program Folder location.

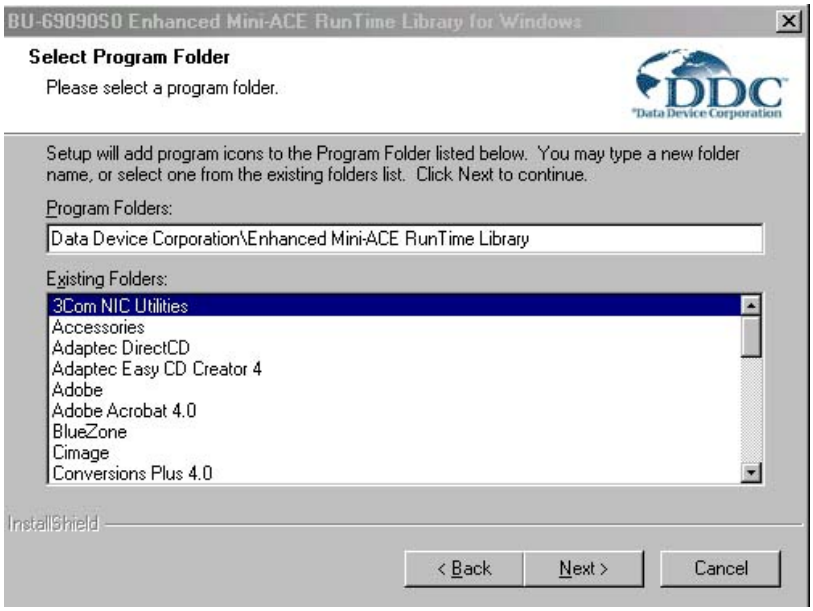


Figure 20. Program Folder Location

5) Select or clear the various components available for custom installation. The default is all checked.

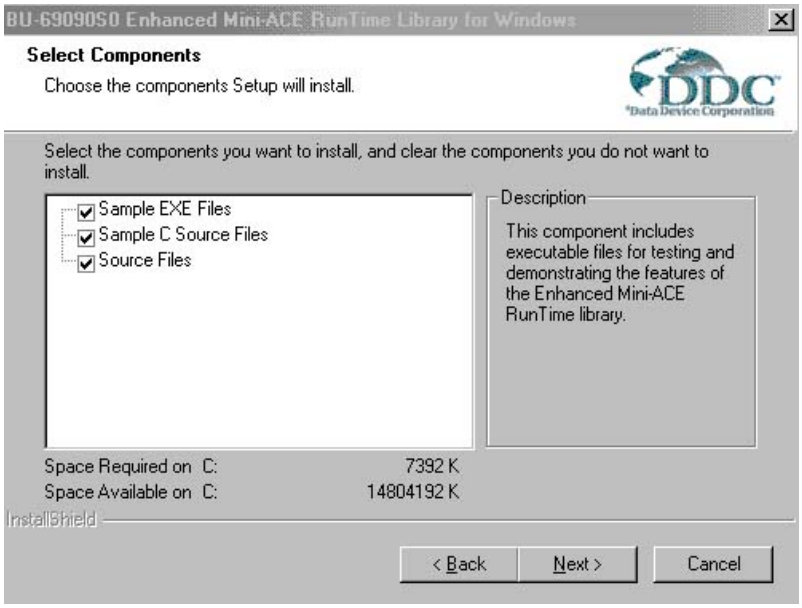


Figure 21. Select Components

6) Click Finish when installation is complete.

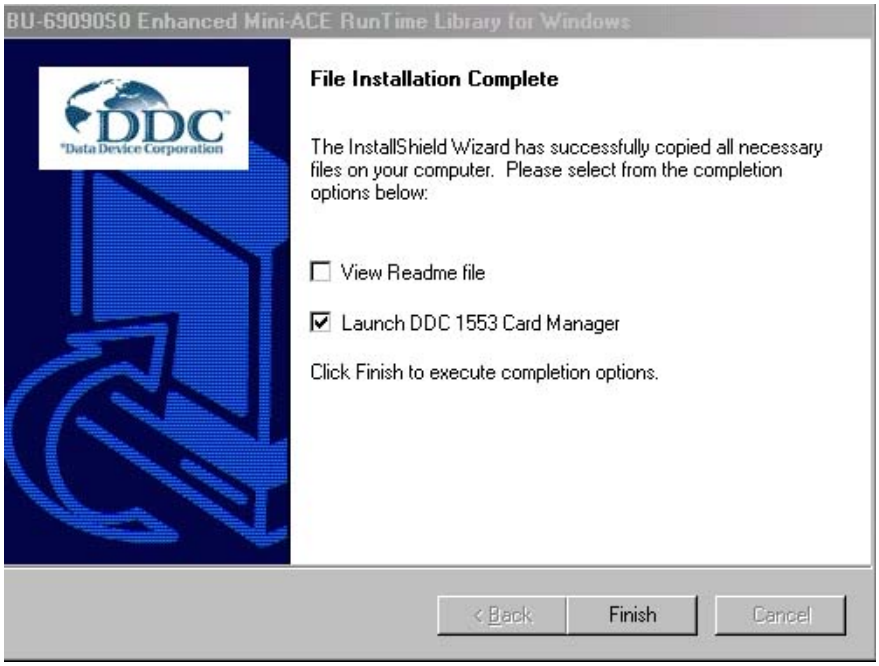


Figure 22. Setup Complete

7) The **DDC 1553 Card Manager** will be launched. Double click the ***BU-65569T*** card entry in the list to pop up the Logical Device Number dialog box. Any device that you wish to actively use must be assigned a logical device number. It is customary to assign device numbers starting with Device Number 0. Select a device number then click OK. Click Close when finished.

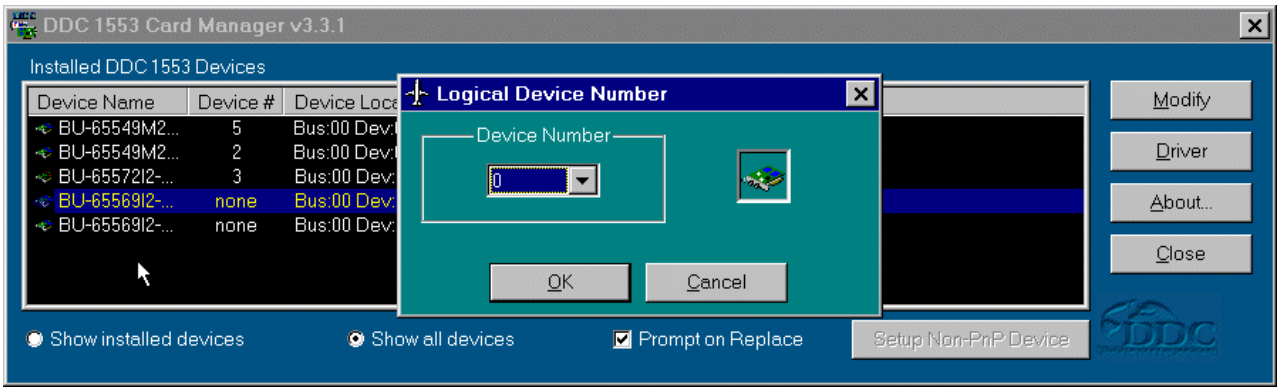


Figure 23. Select Device Number

8) Allow the installation program to reboot the computer.

5.3.2 Enhanced Mini-ACE RTL Installation - Windows NT

If you are installing the **Enhanced Mini-ACE RTL** in a Windows NT environment refer to Page 24 for installation instructions.

5.4 *BUS-69082/83S0* ACE Runtime Library (RTL)

The **ACE Runtime Library** is supplied for Windows 9x/2000/XP and Windows NT. The ACE Runtime Library package includes sample files and utilities and must be installed on the target O/S. The user is free to use the example source code, in part or in its entirety.

5.4.1 ACE RTL Installation - Windows 9x/2000/XP

5.4.1.1 Installation Overview

Once the drivers have been correctly installed, the new software libraries may be installed. The installation of the 32-bit software and menus use the InstallShield® utility. This allows for a consistent user interface when installing and removing software. If you are not familiar with this utility, follow the instructions below. If you wish to remove any of the 32-bit ACE products, you can use the Start/Settings/Control Panel / Add/Remove Software utility.

The driver installation will be initiated automatically the first time the PC is powered up after the hardware has been installed. When the BIOS enumerator discovers the new hardware, it will signal the system that new hardware has been found, and then the system (Windows 9x/2000/XP) will instruct the user to provide a disk with the appropriate drivers.

With the drivers loaded, the libraries may be loaded next. Refer to Table 7 for a summary of the various software types available.

5.4.1.2 CD-ROM Installation:

1) Insert the **Data Bus Software CD** into the appropriate drive and allow to autorun.

2) Select the card type, then the software type.

3) Click on the Install Software icon, then refer to the InstallShield wizard instructions below.

5.4.1.3 Floppy Disk Installation:

1) From the ***BUS-69082S0*** or ***BUS-69083S0*** installation disk set, insert disk 1 into the appropriate drive.

2) Run the setup.exe program, then refer to the InstallShield wizard instructions below.

5.4.1.4 InstallShield Wizard Instructions:

1) The InstallShield wizard will launch the Welcome screen. Click Next to continue.

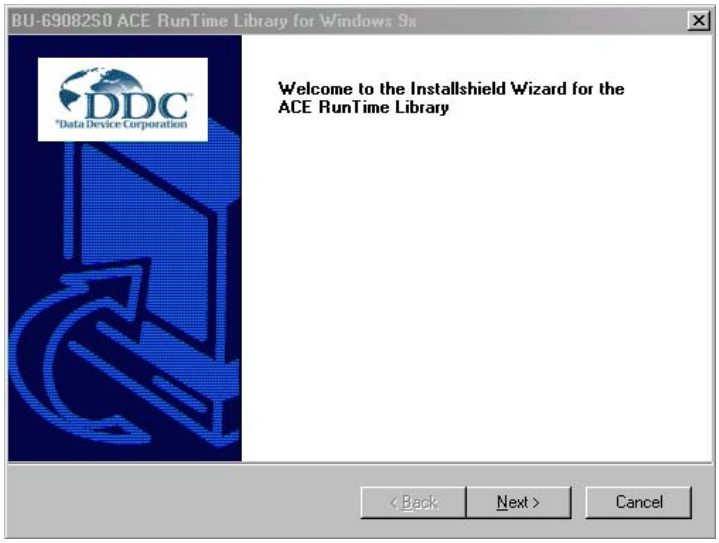


Figure 24. Welcome Screen

Note: *If a previous version of software has already been installed the user will be prompted to uninstall the older version. Uninstallation of the old version is recommended. Check our web site at www.ddc-web.com for the latest software.*

2) After reading the License Agreement click Yes to accept the terms, or No to disagree with them. (Choosing No will end the installation).

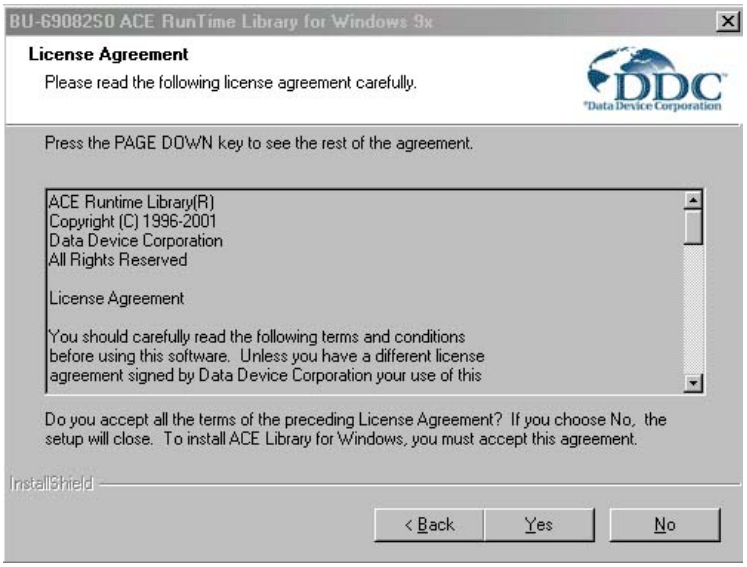


Figure 25. Software License Agreement

3) Click Next to choose the default installation folder, or Browse to locate a custom folder destination.

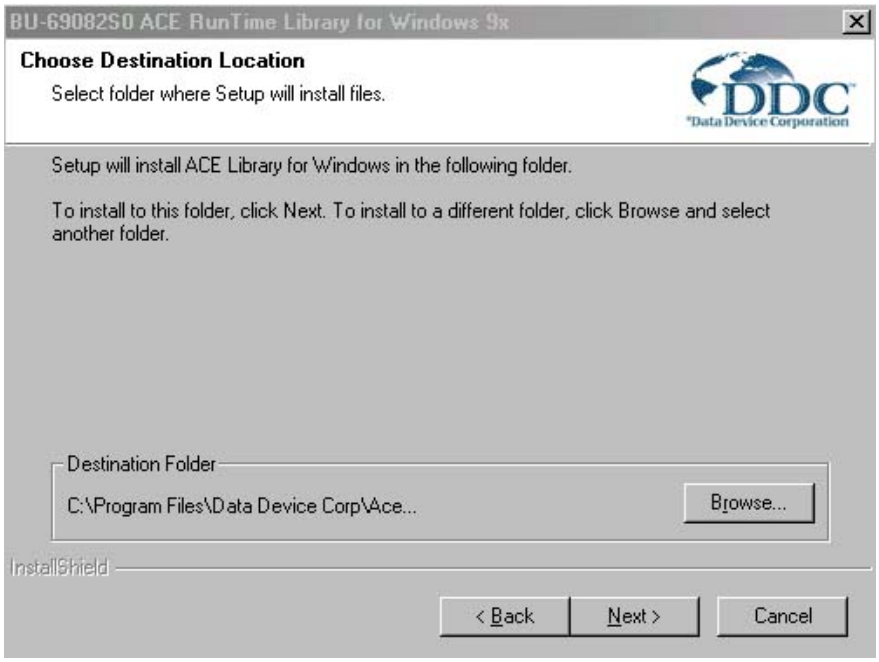


Figure 26. Destination Folder

4) Click Next to choose the default Program Folder location.

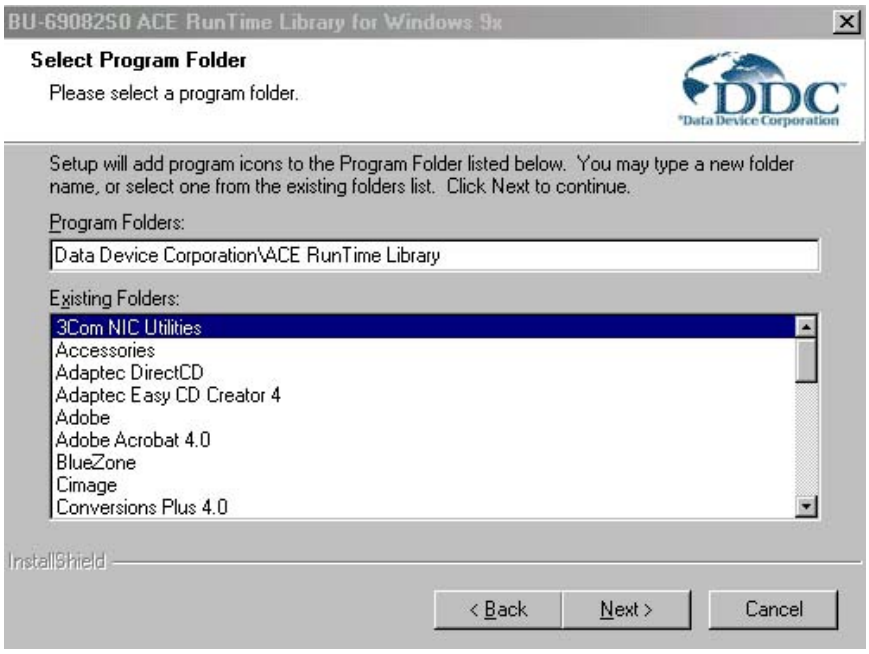


Figure 27. Folder Location

5) Select or clear the various components available for custom installation. The default is all checked.

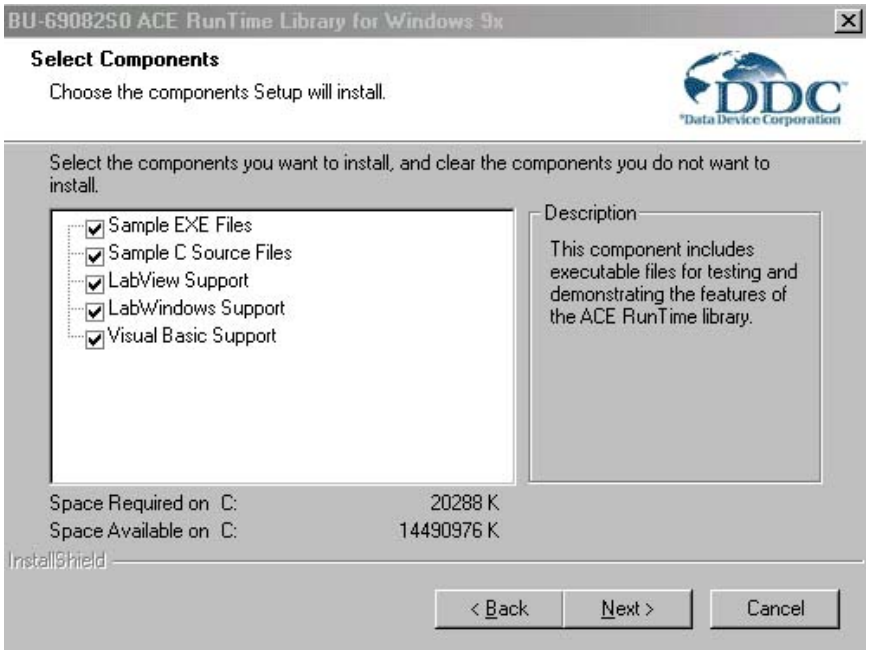


Figure 28. Select Components

6) If LabVIEW files are to be installed, choose the recommended LabVIEW folder destination, or Browse to use a custom folder destination.



Figure 29. LabVIEW Files Destination

7) Click Finish when installation is complete.

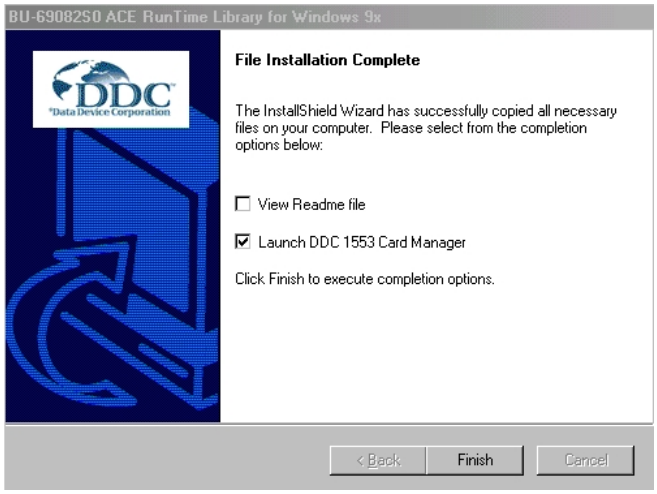


Figure 30. Setup Complete

8) The **DDC 1553 Card Manager** will be launched. Double click the ***BU-65569T*** card entry in the list to pop up the Logical Device Number dialog box. Any device that you wish to actively use must be assigned a logical device number. It is customary to assign device numbers starting with Device Number 0. Select a device number then click OK. Click Close when finished.

9) Allow the installation program to reboot the computer.

Please refer to the section ‘Testing the Installation’ on page 36.

5.4.2 ACE RTL Installation - Windows NT

If you are installing the **ACE Runtime Library** in a Windows NT environment, refer to Page 24 for installation instructions.

5.4.3 Testing the Installation

Once the hardware and software is installed, you can test the installation by running one of the sample programs that is shipped with the software. Follow the steps below to test the installation.

5.4.3.1 Testing the ACE RTL

From a Command prompt, change to the directory ‘<disk>: \Program Files\Data Device Corporation\Ace <*version*>\exe.

Run the selftst2.exe program with the command line `< SELFTST2 0 >`. This program requires a device parameter. The 0 indicates that the hardware is defined as 0 in the 1553 CARD MANAGER. This parameter will be modified as required per the installation. If you have more than one device installed in the system, then running SELFTST2 with the appropriate parameter, 0, 1, 2 or 3 should test each of the cards individually.

5.4.3.2 Testing the Enhanced Mini-ACE RTL

From a Command prompt, change to the directory ‘<disk>:\ \EMACE <*version* >\exe’.

Run the Tester.exe program. This program requires a logical device number. A 0 indicates that the hardware is defined as 0 in the 1553 CARD MANAGER. This parameter will be entered as required per the installation. If you have more than one device installed in the system, then running Tester with the appropriate parameter, 0, 1, 2 or 3 should test each of the cards individually.

If all elements of the test passed, the 1553 card/software is ready for use.

If one or more elements did not pass, refer to the section on Troubleshooting the Installation on page 37 of this manual or visit the DDC web site at **www.ddc-web.com**.

5.4.4 Troubleshooting the Installation

In most cases, the installation should complete without any problems, and running the self-test should result in all tests passing. The usual problems that result from incorrect resource selection are not relevant since BIOS and Windows configure the PCI bus. There are, however, some situations that can cause problems during the installation. The most common situation is a BU-107 error.

A BU-107 error is returned when an attempt to run the SELFTEST or any of the other sample programs. This fault is usually related to an incorrectly assigned device number. Be sure that a device number was correctly assigned through the **DDC 1553 Card Manager**.

5.5 ACE Menu for Windows

The **ACE Menu** (***BUS-69084S0/BU-69085S0***) is a powerful user interface to the MIL-STD-1553 bus and runs on top of the Windows GUI (graphical user interface). The **ACE Menu** for Windows 9x/2000/XP and Windows NT is included as standard software supplied with the ***BU-65569T/B***. The **ACE Menu** software, setup files, and stack files are 100% compatible with all other ACE based 1553 PC boards supplied by DDC.

When using the **ACE Menu**, the user has full control of the Bus Controller, Remote Terminal, Monitor and Self-Test functions from an easy to use interface. Using the intuitively designed controls in this menu, the user has the capability of setting up messages, minor frames, major frames, timing, filtering and many other functions required by the beginning and advanced MIL-STD-1553 user. Without programming a line of code, the ACE Menu enables the user to quickly get started using the ACE family products. This software requires the successful installation of the ACE 32-bit drivers and the ***BU-65569T/B*** hardware.

The ACE 32-bit Menu is supplied on either floppy disk or CD-ROM and requires approximately 4 Meg of hard disk space. The installation uses InstallShield, which provides a standard user interface for installation and removal of software products.

As a general rule, all active programs should be closed during installation of any software.

5.5.1 ACE Menu Installation For Windows 9x/2000/XP and Windows NT

5.5.1.1 CD-ROM Installation:

1) Insert the **Data Bus Software CD** into the appropriate drive and allow to autorun.

2) Select the card type, then the software type.

3) Click on the Install Software icon, then refer to the InstallShield wizard instructions below.

5.5.1.2 Floppy Disk Installation:

1) From the ***BUS-69084/5S0*** installation disk set, insert disk 1 into the appropriate drive.

2) Run the setup.exe program, then refer to the InstallShield wizard instructions below.

5.5.1.3 InstallShield Wizard Instructions:

1) The InstallShield wizard will launch the Welcome screen. Click Next to continue.

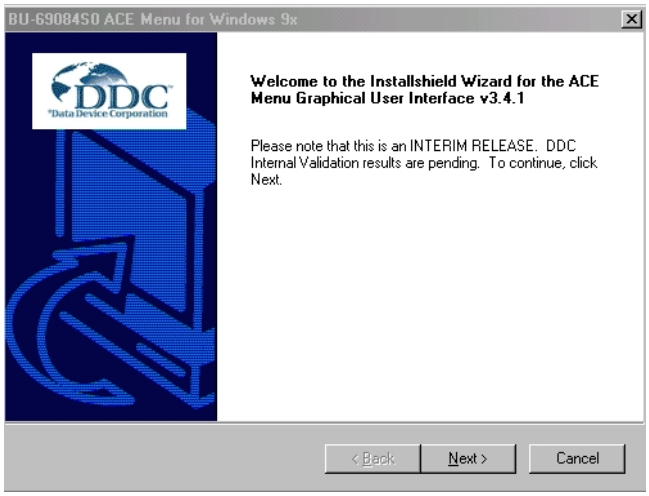


Figure 31. Welcome Screen

Note: *If a previous version of software has already been installed the user will be prompted to uninstall the older version. Uninstallation of the old version is recommended. Check our web site at www.ddc-web.com for the latest software.*

2) After reading the License Agreement click Yes to accept the terms, or No to disagree with them. (Choosing No will end the installation).

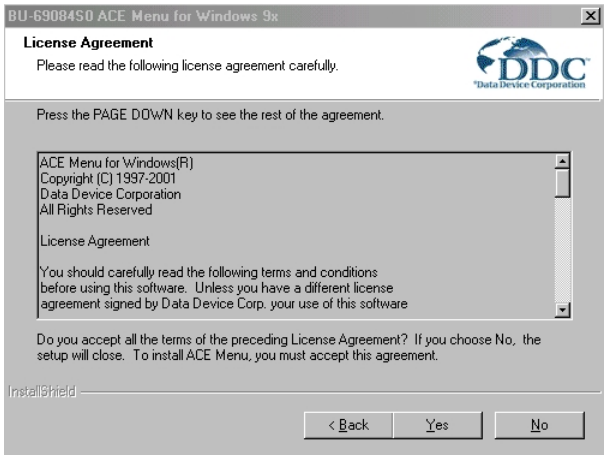


Figure 32. Software License Agreement

3) Click Next to choose the default installation folder, or Browse to locate a custom folder destination.

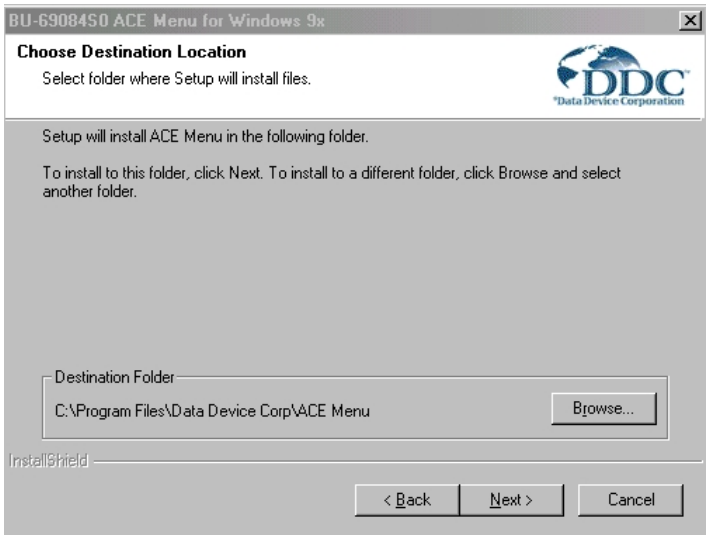


Figure 33. Destination Folder

4) Click Next to choose the default Program Folder location.

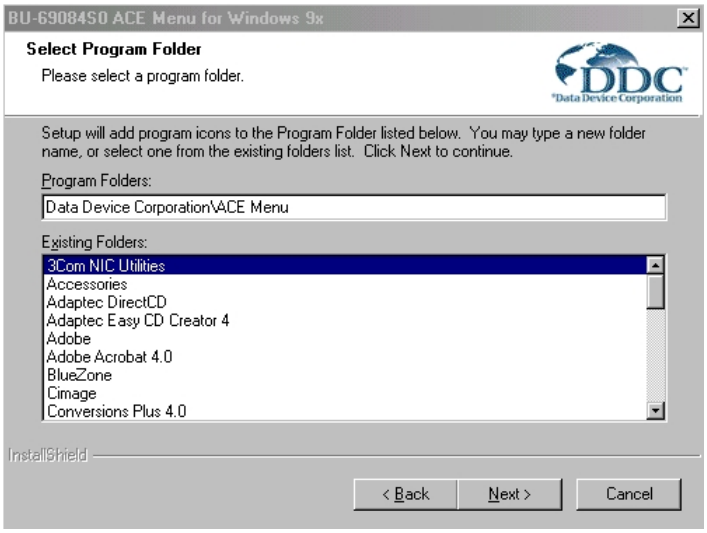


Figure 34. Program Folder Location

5) Select or clear the various components available for custom installation. The default is all checked.

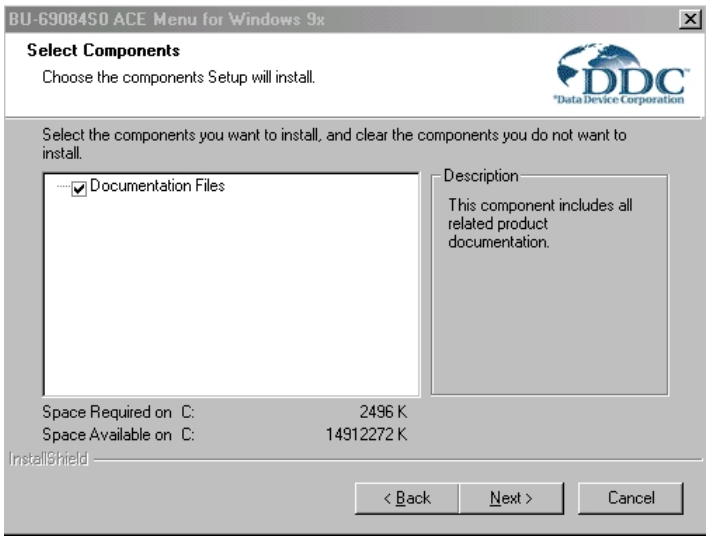


Figure 35. Select Components

6) Click Finish when installation is complete.

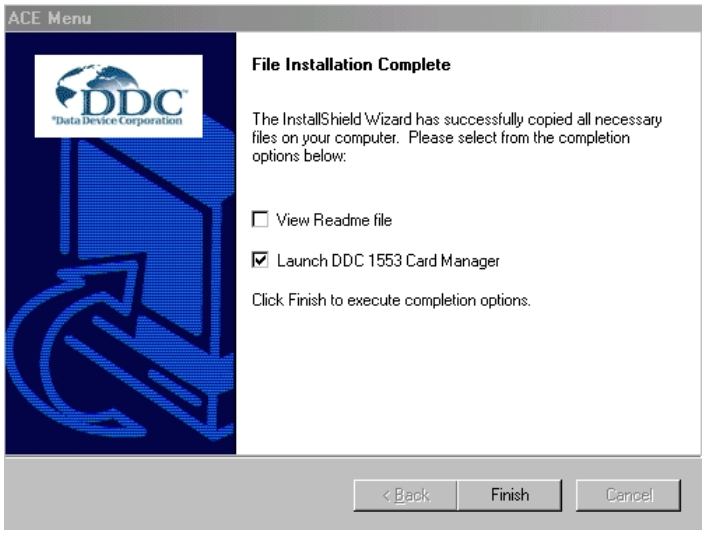


Figure 36. Setup Complete

You do not have to reboot the system for this installation.

To run the ACE Menu for Windows, select '**START/PROGRAMS/Data Device Corporation/ACE Menu /ACE Menu**. To insure everything is working correctly, access the FILE menu and click the NEW menu entry. Click on File > Set card configuration and verify that the number displayed matches the number assigned in the DDC 1553 Card Manager. Click the TEST button or select Test from the menu. Next click the ALL button. This will perform a basic test of the ACE hardware registers, protocol, memory, and interrupts. If the test passes, the system

is ready for operation. If the test fails, check the installation of the ACE library and drivers, or contact technical support.

For detailed operating instructions refer to the online Help topics listed under the Help menu item.

5.6 Other Considerations for Installation

5.6.1 Memory Base Address Selection

The ***BU-65569T/B*** card needs 64K words (128K bytes) for each ACE terminal installed on the board. BIOS will assign all of the memory required by the card's 64K words (128K words for a dual ACE card) from an area of addressable memory space well above the last word of RAM. This search for a free memory location is generally started at the top of memory space (4Gig). BIOS will reliably locate the memory needed for the interface, and during Windows Boot, will pass this information to Windows. There is no user intervention required for the configuration process.

5.6.2 Interrupt Level Selection

The interrupt request level (IRQ) is selected by BIOS during the power up boot process. Since the PCI interrupts are shared, there should be no problems with conflicts.

5.7 Software Development Libraries

The software development libraries supplied with the ***BU-65569T/B*** are written in 'C'. The Libraries for Microsoft and Borland (***BUS-69080S0*** series only) Compilers supporting Windows 9x/2000/XP and Windows NT 32-bit applications are provided in the .\ACE <*version*>\LIB directory.

All of the 32-bit examples are supplied as both executable and source. The 32-bit ACE source is written in 'C', and found in the .\ACE <*version*>\SAMPLES subdirectory. The 32-bit ACE executables are found in the .\ACE <*version*>\exe directory. Additionally, as new samples are created, they will be placed on the DDC web site at www.ddc-web.com.

The 32-bit Enhanced Mini-ACE RTL follows the same directory structure, but is installed into the …\EMACE <*version*> path.

5.7.1 16-Bit ACE Runtime Library

The 16-bit version of the ACE Runtime Library is not supported for the ***BU-65569T/B*** CompactPCI card.

5.7.2 32-Bit ACE and Enhanced Mini-ACE Runtime Libraries

The ***BU-69090S0, BUS-69082S0*** and ***BUS-69083S0*** Runtime Libraries provide the framework for developing near “real-time” applications for the ***BU-65569T/B*** CompactPCI Card. The libraries, written in C, support Windows 9x/2000/XP and Windows NT 32-bit applications using development tools from both Microsoft and Borland (ACE library only). For detailed information on the ACE Runtime Library and its Dynamic Link Library (DLL) refer to the ***BU-69090*** Enhanced Mini-ACE RUNTIME LIBRARY SOFTWARE MANUAL and the ‘***BUS-69080***, ***69082***, ***69083*** ACE RUNTIME LIBRARY SOFTWARE MANUAL’.

6 REFERENCE

6.1 Introduction

The ***BU-65569T/B*** is a single-channel or multi-channel MIL-STD-1553 CompactPCI card. The ***BU-65569T/B*** is available with one to four dual redundant 1553 channels.

The design of the ***BU-65569T/B*** leverages the ***BU-61864*** Enhanced Mini-ACE. Each channel may be independently programmed for BC, RT, Monitor, or RT/Monitor mode.

Advanced architectural features of the Enhanced Mini-ACE include a highly autonomous bus controller, an RT providing a wide variety of buffering options, and a selective message monitor. Each Enhanced Mini-ACE channel incorporates 3.3 volt logic to reduce power consumption and 64K words of RAM.

The ***BU-65569T/B*** is supported by free software, including a C++ library, Windows 9x/2000/XP, Windows NT and Linux driver. The library and driver comprise a suite of C function calls that serves to offload a great deal of low-level tasks from the application programmer. This software supports all of the Enhanced Mini-ACE's advanced architectural features.

6.2 Enhanced Mini-ACE

The ***BU-65569T/B*** CompactPCI card incorporates a PCI bridge, along with between one and four of DDC's ***BU-61864G3*** Enhanced Mini-ACE hybrids. Each Enhanced Mini-ACE comprises a complete, independent interface between the PCI bridge and a MIL-STD-1553 bus. The Enhanced Mini-ACE hybrids provide software compatibility with the DDC's older generation ACE and Mini-ACE (Plus) terminals.

The ***BU-61864*** Enhanced Mini-ACE provides complete multiprotocol support of MIL-STD-1553A/B/McAir and STANAG 3838. These hybrids include dual transceiver; along with protocol, host interface, memory management logic; and 64K X 16 of RAM. There is built-in parity checking for this RAM.

The Enhanced Mini-ACEs include a 5V, voltage source transceiver for improved line driving capability, with options for MIL-STD-1760 compliance (20 V_{P-P} minimum transmitter voltage) or McAir compatibility

(consult factory). As a means of reducing power consumption, the Mini-ACE's logic is powered by 3.3V.

One of the new salient features of the Enhanced Mini-ACE is its new bus controller architecture. The Enhanced BC's highly autonomous message sequence control engine provides a means for offloading the host processor for implementing multi-frame message scheduling, message retry and bus switching schemes, data double buffering, and asynchronous message insertion. In addition, the Enhanced BC mode includes 8 general purpose flag bits, a general purpose queue, and user-defined interrupts, for the purpose of performing messaging to the host processor.

Another important feature for the Enhanced Mini-ACE is the incorporation of a fully autonomous built-in self-test. This test provides comprehensive testing of the internal protocol logic. A separate test verifies the operation of the Enhanced Mini-ACE's internal RAM. Since the self-tests are fully autonomous, they eliminate the need for the host to write and read stimulus and response vectors.

The Enhanced Mini-ACE RT offers the choice of single, double, and circular buffering for individual subaddresses or a global circular buffering option for multiple (or all) receive subaddresses, a 50% rollover interrupt for circular buffers, an interrupt status queue for logging up to 32 interrupt events, and an option to automatically initialize to RT mode with the Busy bit set.

6.3 Transceivers

The transceivers in the Enhanced Mini-ACE series terminals are fully monolithic, requiring only a +5 volt power input. The transmitters are voltage sources, which provide improved line driving capability compared to current sources. This serves to improve performance on long buses with many taps. The ***BU-65569T/B's*** transmitters may be trimmed to meet the MIL-STD-1760 requirement of a minimum of 20 volts peak-to-peak, transformer coupled (consult factory).

To provide compatibility to McAir specs, the ***BU-65569T/B*** is also available with an option for sinusoidal transmitters (consult factory).

Besides eliminating the demand for an additional power supply, the use of a +5V-only transceiver entails the use of a step-up, rather than step-down, isolation transformer. This provides the advantage of a higher terminal input impedance than is possible for a 15 volt or 12 volt

transmitter. As a result, there is a greater margin for the input impedance test, as mandated by the MIL-STD-1553 RT validation test. This characteristic allows for longer cable lengths between the ***BU-65569T/B's*** (1553 I/O) connector and the system connector.

The receiver sections of the Enhanced Mini-ACE are fully compliant with MIL-STD-1553B Notice 2 in terms of front end overvoltage protection, threshold, common mode rejection, and word error rate.

6.4 Software

The ***BU-69090*** C software library provides comprehensive support of the ***BU-65569T/B*** card. This library, which was developed in Microsoft Visual C++, comprises a suite of function calls that serves to offload a great deal of low-level tasks from the application programmer.

6.4.1 Memory Allocation.

For each mode of operation - BC, RT, and Monitor - the library and driver operate under an open/access/close model, in which areas of RAM are autonomously allocated and de-allocated by means of low-level routines. While these functions may be invoked directly by an application, in general their operation is transparent to the application programmer. The library's memory manager module performs autonomous allocation of shared memory for stacks and data blocks. This provides a high degree of flexibility for sizing various data structures.

The memory management functions make use of handles consisting of starting addresses and sizes of memory blocks, along with status information delineating whether particular areas of shared RAM are unused, used, or protected. For each mode, there are functions to transfer data between shared RAM data blocks and buffers in host memory. In addition, there are functions to access consolidated data structures providing both message status information, as well as 1553 message words.

6.4.2 Mode-Specific Software.

For BC mode, there is comprehensive support of the enhanced bus controller capabilities, allowing the user to leverage function calls and macros invoking the BC instruction set. Some of the functions support higher level tasks such as minor and major frame timing control and asynchronous message insertion. For the enhanced BC, the software

also supports the offline development and compilation of BC message scenarios on (for example) a desktop PC. The binary images created from these may then be downloaded to the target processor environment.

For BC mode, the Enhanced Mini-ACE Runtime Library encapsulates all opcodes, data blocks, messages, and frames (major, minor, and asynchronous). This allows the user to create the desired 1553 BC activity, without the overhead of memory management. The library includes a function that creates two files which allow the user to view the opcode sequence generated by the library. The first file is a binary file which contains an image of ACE memory, and the second file is a 'C' header file that shows all locations to structures/frames within memory.

For RT mode, there is high-level operation for configuring and utilizing the Enhanced Mini-ACE's single-buffer, double buffer, and circular buffered subaddress memory management schemes. This includes methods for accessing synchronously and asynchronously received message data. There is also a mechanism provided for automatically reading and accessing the most recently received message. In addition, there is high-level support of subaddress illegalization and use of the busy bit, enhanced mode code handling, along with functions allowing for accessing user programmable status and BIT words.

For the message monitor mode, functions are provided for programming the command and data stack sizes, programming of the monitor "filter" table (which addresses/T-R/subaddresses to monitor), along with high-level tools that decode monitored messages, and transfer status information and message words to host RAM in a consolidated stack data structure.

6.5 PCI Interface

As a means of minimizing power consumption and dissipation, the design of the standard ***BU-65569T/B*** board utilizes +3.3 volt power for the PCI interface and 1553 (Enhanced Mini-ACE) logic, and +5 volt power for the 1553 transceivers and RAM.

The ***BU-65569T/B's*** CompactPCI interface is a fully compliant target (slave) agent, as defined by the PCI Local Bus Specification Revision 2.2, using a 32-bit interface that operates at clock speeds of up to 33 MHz, in a 3.3 volt and 5 volt signaling environment. The interface supports PCI interrupts and contains a 64 deep by 32 wide FIFO to accelerate burst write transfers from the PCI host. That is, it's possible to perform a burst write of 32 16-bit words (i.e., all of the data words of a

1553 message) by means of sixteen 32-bit PCI transfers in approximately 1.5 µs.

The ***BU-65569T/B*** contains only a single set of configuration registers such that all of the Enhanced Mini-ACE(s) memory and register space may be addressed through a single PCI function.

Internal registers implement the Subsystem Vendor and Device ID, and control the Fail-Safe operation of the device. There are two Base Address Registers, utilized to implement the Enhanced Mini-ACE memory space (BAR0) and register space (BAR1). The Base Address Register mapping is contained in PCI configuration register space.

The ACE register mapping is located in PCI memory space, allowing for full PCI access to all 1553 terminals. The ***BU-65569T/B*** configuration registers and the Enhanced Mini-ACE RAM (64K X 16 each) are accessed in 32-bit words, while all ACE registers are accessed as 16-bit words. If a 32-bit read is performed from the PCI bus in ACE register space only the first 16 bits of data are valid. ACE memory may also be accessed in 16-bit words, but memory is accessed sequentially, allowing for 32-bits of data to be written to or read from the PCI bus.

That is, if a 32-bit PCI memory read is performed, the first 16 bits of data would be read from the requested address, the next 16 bits of data would be read from the initial address + 2. The ***BU-65569T/B*** supports 32-bit and 16-bit read and write operations only. 8-bit accesses are illegal.

6.6 Interrupts

The Enhanced Mini-ACEs may issue interrupt requests over the PCI bus. PCI Interrupts are generated on the INTA# output signal to the PCI host. The interrupts from each of Enhanced Mini-ACE(s) are functionally OR'd together to provide a single interrupt.

6.7 Register and Memory Addressing

The ***BU-65569T/B*** CompactPCI interface contains a set of "Type 00h" PCI configuration registers that are used to map the device into the host system. The PCI configuration register space is mapped in accordance with PCI revision 2.2 specifications.

Table 8. PCI Configuration Register Space												
Addr	31			24	23			16	15		8	7		0
00h	Device ID								Vendor ID					
	See Table 9								DDC Manufacturer Device ID value ($4DDC_H$)					
04h	Status Register								Command Register					
08h	Class Code = 078000 h											Rev ID = 01		
0Ch	BIST (not implemented)				Header Type 00h				Latency Timer			Cache Line Size		
10h	Base Address Register 0 (for Enhanced Mini-ACE RAM)													
	R/W				R/W and 0's see text				00h			04h		
14h	Base Address Register 1 (for Enhanced Mini-ACE registers)													
	R/W				R/W				R/W and 0's see text			04h		
18h- 24h Base Address Registers 2 through 5 (not used)	00000000h													
28h	Card Bus CIS pointer (not used) 00000000h													
2Ch	Subsystem Device and Subsystem Vendor ID Same as Configuration Register 0, Alias Reads to Configuration Register													
30h	Expansion ROM Base Address (Not Used, bit 0 = 0)													
34h-38h	Reserved													
3Ch	Max Lat. 00h				Min Gnt 00h				Interrupt Pin 01h			Interrupt Line R/W		

Vendor ID field contains the vendor's ID configuration register. Data Device Corporation's ID code is 4DDCh.

Device ID field is used to indicate the device being used. Refer to Table 9.

Table 9. Device ID per Model Number

Model Number	Device ID
BU-65569T1	0C01
BU-65569T2	0C02
BU-65569T3	0C03
BU-65569T4	0C04
BU-65569B1	0C05
BU-65569B2	0C06
BU-65569B3	0C07
BU-65569B4	0C08

Status Register will be 0280h after reset, indicating that the BU-65569T/B is fast back-to-back capable and has medium device select timing.

Base Address Registers are used to identify EMA memory space (BAR0) and EMA register space (BAR1). BARs 2 through 5 are not used and will return all zeroes when read.

BAR0 is used to define EMA memory space.

When all ONEs are written to BAR0, the following values will be read back. Besides defining the address space window size and base, the lower 4 bits of BAR0 will read back as zeroes, indicating that these are Memory BARs. The memory can be mapped anywhere in the 32-bit memory space and the memory is NOT prefetchable.

Table 10. BAR0 Readback Value (after all ONEs are written to BAR0)	
# of ACES	**BAR0 readback value**
1	FFFE0000 (128k byte window)
2	FFFC0000 (256k byte window)
3	FFF80000 (512k byte window)
4	FFF80000 (512k byte window)

The BAR0 address space is partitioned according to the following table.

Table 11. (BAR0) ACE Memory Map	
ADDRESS OFFSET	**DEFINITION**
00000 – 1FFFC	ACE 1 Memory Space
20000 – 3FFFC	ACE 2 Memory Space (if available)
40000 – 5FFFC	ACE 3 Memory Space (if available)
60000 – 7FFFC	ACE 4 Memory Space (if available)

Note: *The ACE memory is packed two ACE memory words per PCI doubleword location. In other words, a 32-bit PCI read of BAR0 offset 0h will return ACE 1 memory location 0 (lower 16 bits) and ACE 1 memory location 1 (upper 16 bits)*

BAR 1 is used to access EMA registers and the EMA-PCI interface (Global Activity) register. BAR1 will read back as FFFFF000h (4K bytes address window, minimum size recommended in PCI spec) when all ONEs are written to it. Since the lower 4 bits of BAR0 read back as zeroes, this indicates that these are Memory BARs. The memory can be mapped anywhere in the 32-bit memory space and the memory is NOT prefetchable.

Table 12. (BAR1) ACE Control Registers – 4K byte Total Space		
PCI ADDRESS OFFSET	**NAME**	**DEFINITION /ACCESSIBILITY**
000-0FC	ACE1	ACE 1 Register Space
100-1FC	ACE2	ACE 2 Register Space (if ACE 2 present)
200-2FC	ACE3	ACE 3 Register Space (if ACE 3 present)
300-3FC	ACE4	ACE 4 Register Space (if ACE 4 present)
800	ACE-PCI IF	Global Activity

ACE REGISTER SPACE (ACE1 – ACE4): This address space allows access to ACE registers. The lower four 256-byte segments of allocated address space allow access to a total of 64 ACE registers per segment.

Note: *The ACE registers are packed ONE ACE register per PCI doubleword location. The internal ACE registers are only 16-bits wide: the upper 16 bits of a Dword (32 bit) read will be all zeroes. Register access is on a 32-bit boundary (e. g., BAR1 + 000h = ACE1 REG 0, BAR1 + 004h = ACE1 REG 1, BAR1 + 008h = ACE1 REG 2, etc). All reads of EMA registers are via DRR (Delayed Read Request) transactions on the PCI bus.*

Table 13. Global Activity Register (BAR1 + 800h)	
BIT	**DESCRIPTION**
31 (MSB)	RESERVED (0)
30	RESERVED (0)
29	RESERVED (0)
28	RESERVED (0)
27	RESERVED (0)
26	RESERVED (0)
25	NUMBER OF ACE'S PRESENT – BIT 1 (MSB)
24	NUMBER OF ACE'S PRESENT – BIT 0 (LSB)
23	RESERVED (0)
22	RESERVED (0)
21	RESERVED (0)
20	RESERVED (0)

Table 13. Global Activity Register (BAR1 + 800h)	
BIT	**DESCRIPTION**
19	ACE 4 INTERRUPT ACTIVE
18	ACE 3 INTERRUPT ACTIVE
17	ACE 2 INTERRUPT ACTIVE
16	ACE 1 INTERRUPT ACTIVE
15	RESERVED (0)
•	•
•	•
•	•
0 (LSB)	RESERVED (0)

Note: *This register is directly readable and does not generate a DRR PCI transaction.*

NUMBER OF ACE'S PRESENT: Bits 25 (MSB) and 24 (LSB) provide a binary representation of the number of ACE terminals presently installed and operating. The BU-65569T/B card supports up to four ACE terminals and may be configured for 1, 2, 3, or 4 EMA devices.

ACE INTERRUPT ACTIVE: Bits 19 to 16 reflect the interrupt status of the EMAs. All EMA interrupts must be programmed for level operation. When an EMA interrupt occurs, the corresponding ACE INTERRUPT ACTIVE bit gets set to a ONE. Bits 19 to 16 are cleared when the respective EMA clears its interrupt request line.

6.8 Enhanced Mini-ACE Register and Memory Addressing

The software interface between each Enhanced Mini-ACE and the PCI host consists of 24 internal operational registers for normal operation, an additional 24 test registers, plus 64K words of shared memory address space.

The Enhanced Mini-ACE registers are 16 bits wide and “unpacked” with respect to the PCI bus. Registers may be accessed as either single 16-bit words or 32-bit doublewords. Doubleword reads contain all zeroes in the upper 16 bits. Because the registers are unpacked, register alignment is on a PCI **32-bit boundary** (e.g., BAR1+000 = Enhanced Mini-ACE Register 0, BAR1+004 = Enhanced Mini-ACE Register 1, BAR1+008 = Enhanced Mini-ACE Register 2, … etc).

Enhanced Mini-ACE memory may be accessed as either single 16-bit words, or as a 32-bit double word. For the latter, a packed pair of 16-bit words at adjacent memory address locations will be read or written.

Note that the addressing for all Enhanced Mini-ACE pointers is **word-oriented**, while all PCI addressing is byte-oriented. That is, the value of a pointer stored in Enhanced Mini-ACE RAM will be **half** of the value of the PCI address offset from the base memory address for the particular Enhanced Mini-ACE.

For normal operation, the host processor only needs to access the lower 32 register address locations (00-1F). The next 32 locations (20-3F) should be reserved, since many of these are used for factory test.

6.8.1 Enhanced Mini-ACE Registers

The address mapping for the Enhanced Mini-ACE registers is illustrated in **Table 14**.

Table 14. Enhanced Mini-ACE Registers

ACE LOCAL BUS ADDRESS LINES					BAR 1 ADDR OFFSET	REGISTER
A4	A3	A2	A1	A0		DESCRIPTION / ACCESSIBILITY
0	0	0	0	0	00h	Interrupt Mask Register #1 (RD/WR)
0	0	0	0	1	04h	Configuration Register #1 (RD/WR)
0	0	0	1	0	08h	Configuration Register #2 (RD/WR)
0	0	0	1	1	0Ch	Start/Reset Register (WR)
0	0	0	1	1	0Ch	Non-Enhanced BC or RT Command Stack Pointer/Enhanced BC Instruction List Pointer Register (RD)
0	0	1	0	0	10h	BC Control Word/RT Subaddress Control Word Register (RD/WR)
0	0	1	0	1	14h	Time Tag Register (RD/WR)
0	0	1	1	0	18h	Interrupt Status Register #1 (RD)
0	0	1	1	1	1Ch	Configuration Register #3 (RD/WR)
0	1	0	0	0	20h	Configuration Register #4 (RD/WR)
0	1	0	0	1	24h	Configuration Register #5 (RD/WR)
0	1	0	1	0	28h	RT/Monitor Data Stack Address Register (RD/WR)
0	1	0	1	1	2Ch	BC Frame Time Remaining Register (RD)
0	1	1	0	0	30h	BC Time Remaining to Next Message Register (RD)
0	1	1	0	1	34h	BC Frame Time/Enhanced BC Initial Instruction Pointer/RT Last Command/MT Trigger Word Register (RD/WR)
0	1	1	1	0	38h	RT Status Word Register (RD)
0	1	1	1	1	3Ch	RT BIT Word Register (RD)
1	0	0	0	0	40h	Test Mode Register 0
1	0	0	0	1	44h	Test Mode Register 1
1	0	0	1	0	48h	Test Mode Register 2
1	0	0	1	1	4Ch	Test Mode Register 3

Table 14. Enhanced Mini-ACE Registers						
ACE LOCAL BUS ADDRESS LINES					BAR 1 ADDR OFFSET	REGISTER
A4	A3	A2	A1	A0		DESCRIPTION / ACCESSIBILITY
1	0	1	0	0	50h	Test Mode Register 4
1	0	1	0	1	54h	Test Mode Register 5
1	0	1	1	0	58h	Test Mode Register 6
1	0	1	1	1	5Ch	Test Mode Register 7
1	1	0	0	0	60h	Configuration Register #6 (RD/WR)
1	1	0	0	1	64h	Configuration Register #7 (RD/WR)
1	1	0	1	0	68h	RESERVED
1	1	0	1	1	6Ch	BC Condition Code Register (RD)
1	1	0	1	1	6Ch	BC General Purpose Flag Register (WR)
1	1	1	0	0	70h	BIT Test Status Register (RD)
1	1	1	0	1	74h	Interrupt Mask Register #2 (RD/WR)
1	1	1	1	0	78h	Interrupt Status Register #2 (RD)
1	1	1	1	1	7Ch	BC General Purpose Queue Pointer/RT-MT Interrupt Status Queue Pointer Register (RD/WR)

Table 15. Interrupt Mask Register (RD/WR 00h)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	RAM PARITY ERROR
13	BC/RT TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAILURE
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	BC MSG/RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

Table 16. Configuration Register #1 (RD/WR 04h)				
BIT	**BC FUNCTION (Bits 11-0 Enhanced Mode Only)**	**RT WITHOUT ALTERNATE STATUS**	**RT WITH ALTERNATE STATUS (Enhanced Mode Only)**	**MONITOR FUNCTION (Enhanced Mode Only, bits 12-0)**
15 MSB	RT/$\overline{\text{BC - MT}}$ (Logic 0)	(Logic 1)	(Logic 1)	(Logic 0)
14	MT/$\overline{\text{BC - MT}}$ (Logic 0)	(Logic 0)	(Logic 0)	(Logic 1)
13	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)
11	FRAME STOP-ON-ERROR	$\overline{\text{DYNAMICBUS}}$ $\overline{\text{CONTROL ACCEPTANCE}}$	S10	TRIGGER ENABLED WORD
10	STATUS SET STOP-ON-MESSAGE	$\overline{\text{BUSY}}$	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	$\overline{\text{SERVICEREQUEST}}$	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	$\overline{\text{SSFLAG}}$	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	$\overline{\text{RTFLAG}}$ (enhanced mode only)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	INTER-MESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLE/$\overline{\text{SINGLE}}$ RETRY	NOT USED	S02	NOT USED
2	BC ENABLED (read only)	NOT USED	S01	MONITOR ENABLED (read only)
1	BC FRAME IN PROGRESS (read only)	NOT USED	S00	MONITOR TRIGGERED (read only)
0 LSB	BC MESSAGE IN PROGRESS (read only)	RT MESSAGE IN PROGRESS (enhanced mode only) (read only)	RT MESSAGE IN PROGRESS (read only)	MONITOR ACTIVE (read only)

Table 17. Configuration Register #2 (RD/WR 08h)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED INTERRUPTS
14	RAM PARITY ENABLE
13	BUSY LOOK UP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDR DISBL
9	TIME TAG RESOLUTION 2 (TTR2)
8	TIME TAG RESOLUTION 1 (TTR1)
7	TIME TAG RESOLUTION 0 (TTR0)
6	CLEAR TIME TAG ON SYNCHRONIZE
5	LOAD TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/PULSE INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST
1	ENHANCED RT MEMORY MANAGEMENT
0(LSB)	SEPARATE BROADCAST DATA

Table 18. Start/Reset Register (WR 0Ch)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	RESERVED
13	RESERVED
12	RESERVED
11	CLEAR RT HALT
10	CLEAR SELF-TEST REGISTER
9	INITIATE RAM SELF-TEST
8	RESERVED
7	INITIATE PROTOCOL SELF-TEST
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0(LSB)	RESET

Table 19. BC/RT Command Stack Pointer Register (RD 0Ch)	
BIT	**DESCRIPTION**
15(MSB)	COMMAND STACK POINTER 15
•	•
•	•
•	•
0(LSB)	COMMAND STACK POINTER 0

Table 20. BC Control Word Register (RD/WR 10h)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	MESSAGE ERROR MASK
13	SERVICE REQUEST BIT MASK
12	SUBSYS BUSY BIT MASK
11	SUBSYS FLAG BIT MASK
10	TERMINAL FLAG BIT MASK
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/$\overline{B}$
6	OFF LINE SELF TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-TO-RT FORMAT

Table 21. RT Subaddress Control Word (RD/WR 10h)	
BIT	**DESCRIPTION**
15(MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

Table 22. Time Tag Register (RD/WR 14h)	
BIT	**DESCRIPTION**
15(MSB)	TIME TAG 15
•	•
•	•
•	•
0(LSB)	TIME TAG 0

Table 23. Interrupt Status Register (RD/WR 18h)	
BIT	**DESCRIPTION**
15(MSB)	MASTER INTERRUPT
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAILURE
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

Table 24. Configuration Register #3 (RD/WR 1Ch)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/$\overline{R}$ ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER ENABLE
2	$\overline{\text{RTFAIL}}$/$\overline{\text{RTFLAG}}$ WRAP ENABLE
1	1553A MODE CODES ENABLE
0(LSB)	ENHANCED MODE CODE HANDLING

Table 25. Configuration Register #4 (RD/WR 20h)	
BIT	**DESCRIPTION**
15(MSB)	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BROADCAST MASK ENA/$\overline{\text{XOR}}$
10	RETRY IF -A AND M.E.
9	RETRY IF STATUS SET
8	1ST RETRY ALT/$\overline{\text{SAME BUS}}$
7	2ND RETRY ALT/$\overline{\text{SAME BUS}}$
6	VALID M.E./NO DATA
5	VALID BUSY/NO DATA
4	MT TAG GAP OPTION
3	LATCH RT ADDR WITH CONFIG. REG. #5
2	TEST MODE 2
1	TEST MODE 1
0(LSB)	TEST MODE 0

Table 26. Configuration Register #5 (RD/WR 24h)	
BIT	**DESCRIPTION**
15(MSB)	LOGIC ZERO “0”
14	SINGLE-ENDED SELECT
13	EXTERNAL TX INHIBIT A
12	EXTERNAL TX INHIBIT B
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	RT ADDR LATCH/$\overline{\text{TRANSPARENT}}$
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0(LSB)	RT ADDRESS PARITY

Table 27. RT/Monitor Data Stack Address Register (RD/WR 28h)	
BIT	**DESCRIPTION**
15(MSB)	RT/MONITOR DATA STACK ADDRESS 15
•	•
•	•
•	•
0(LSB)	RT/MONITOR DATA STACK ADDRESS 0

Table 28. BC Frame Time Remaining Register (RD/WR 2Ch)	
BIT	**DESCRIPTION**
15(MSB)	BC FRAME TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC FRAME TIME REMAINING 0

NOTE: Resolution = 100 μs per LSB

Table 29. BC Message Time Remaining Register (RD 30h)	
BIT	**DESCRIPTION**
15(MSB)	BC MESSAGE TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC MESSAGE TIME REMAINING 0

NOTE: Resolution = 1 μs per LSB

Table 30. BC Frame Time/RT Last Command/MT Trigger Register (RD/WR 34h)	
BIT	**DESCRIPTION**
15(MSB)	BIT 15
•	•
•	•
•	•
0(LSB)	BIT 0

Table 31. RT Status Word Register (RD 36h)	
BIT	**DESCRIPTION**
15(MSB)	LOGIC ‘0’
14	LOGIC ‘0’
13	LOGIC ‘0’
12	LOGIC ‘0’
11	LOGIC ‘0’
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPT
0(LSB)	TERMINAL FLAG

Table 32. RT BIT Word Register (RD 3Ch)	
BIT	**DESCRIPTION**
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	BIT TEST FAIL
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

Table 33. Configuration Register #6 (RD/WR 60h)	
BIT	**DESCRIPTION**
15 (MSB)	ENHANCED BUS CONTROLLER
14	ENHANCED CPU ACCESS
13	COMMAND STACK POINTER INCREMENT ON EOM (RT, MT)
12	GLOBAL CIRCULAR BUFFER
11	GLOBAL CIRCULAR BUFFER SIZE 2
10	GLOBAL CIRCULAR BUFFER SIZE 1
9	GLOBAL CIRCULAR BUFFER SIZE 0
8	INVALID MESSAGES TO INTERRUPT STATUS QUEUE
7	VALID MESSAGES TO INTERRUPT STATUS QUEUE
6	INTERRUPT STATUS QUEUE ENABLE
5	RT ADDRESS SOURCE
4	ENHANCED MESSAGE MONITOR
3	RESERVED
2	64-WORD REGISTER SPACE
1	LOGIC ZERO “0”
0 (LSB)	LOGIC ZERO “0”

Table 34. Configuration Register #7 (RD/WR 64h)	
BIT	**DESCRIPTION**
15 (MSB)	MEMORY MANAGEMENT BASE ADDRESS 15
14	MEMORY MANAGEMENT BASE ADDRESS 14
13	MEMORY MANAGEMENT BASE ADDRESS 13
12	MEMORY MANAGEMENT BASE ADDRESS 12
11	MEMORY MANAGEMENT BASE ADDRESS 11
10	MEMORY MANAGEMENT BASE ADDRESS 10
9	RESERVED
8	RESERVED
7	RESERVED
6	RESERVED
5	RESERVED
4	RT HALT
3	1553B RESPONSE TIME
2	ENHANCED TIME TAG SYNCHRONIZE
1	ENHANCED BC WATCHDOG TIMER ENABLED
0 (LSB)	MODE CODE RESET/$\overline{\text{INCMD}}$ SELECT

Table 35. BC Condition Code Register (RD 6Ch)	
BIT	**DESCRIPTION**
15 (MSB)	ALWAYS
14	RETRY 1
13	RETRY 0
12	BAD MESSAGE
11	MASKED STATUS SET
10	GOOD BLOCK TRANSFER
9	FORMAT ERROR
8	NO RESPONSE
7	GENERAL PURPOSE FLAG 7
6	GENERAL PURPOSE FLAG 6
5	GENERAL PURPOSE FLAG 5
4	GENERAL PURPOSE FLAG 4
3	GENERAL PURPOSE FLAG 3
2	GENERAL PURPOSE FLAG 2
1	LESS THAN/GENERAL PURPOSE FLAG 1
0 (LSB)	EQUAL FLAG/GENERAL PURPOSE FLAG 0

Table 36. BC General Purpose Flag Register (WR 6Ch)	
BIT	**DESCRIPTION**
15 (MSB)	CLEAR GENERAL PURPOSE FLAG 7
14	CLEAR GENERAL PURPOSE FLAG 6
13	CLEAR GENERAL PURPOSE FLAG 5
12	CLEAR GENERAL PURPOSE FLAG 4
11	CLEAR GENERAL PURPOSE FLAG 3
10	CLEAR GENERAL PURPOSE FLAG 2
9	CLEAR GENERAL PURPOSE FLAG 1
8	CLEAR GENERAL PURPOSE FLAG 0
7	SET GENERAL PURPOSE FLAG 7
6	SET GENERAL PURPOSE FLAG 6
5	SET GENERAL PURPOSE FLAG 5
4	SET GENERAL PURPOSE FLAG 4
3	SET GENERAL PURPOSE FLAG 3
2	SET GENERAL PURPOSE FLAG 2
1	SET GENERAL PURPOSE FLAG 1
0 (LSB)	SET GENERAL PURPOSE FLAG 0

Table 37. BIT Test Status Register (RD 70h)	
BIT	**DESCRIPTION**
15 (MSB)	PROTOCOL BUILT-IN TEST COMPLETE
14	PROTOCOL BUILT-IN TEST IN PROGRESS
13	PROTOCOL BUILT-IN TEST PASSED
12	PROTOCOL BUILT-IN TEST ABORT
11	LOGIC “1”
10	LOGIC “0”
9	LOGIC “0”
8	LOGIC “0”
7	RAM BUILT-IN TEST COMPLETE
6	RAM BUILT-IN TEST IN PROGRESS
5	RAM BUILT-IN TEST PASSED
4	LOGIC “0”
3	LOGIC “0”
2	LOGIC “0”
1	LOGIC “0”
0 (LSB)	LOGIC “0”

Table 38. Interrupt Mask Register #2 (RD/WR 74h)	
BIT	**DESCRIPTION**
15 (MSB)	NOT USED
14	BC OP CODE PARITY ERROR
13	ILLEGAL COMMAND
12	GENERAL PURPOSE QUEUE/INTERRUPT STATUS QUEUE ROLLOVER
11	CALL STACK POINTER REGISTER ERROR
10	BC TRAP OP CODE
9	RT COMMAND STACK 50% ROLLOVER
8	RT CIRCULAR BUFFER 50% ROLLOVER
7	MONITOR COMMAND STACK 50% ROLLOVER
6	MONITOR DATA STACK 50% ROLLOVER
5	ENHANCED BC IRQ3
4	ENHANCED BC IRQ2
3	ENHANCED BC IRQ1
2	ENHANCED BC IRQ0
1	BIT TEST COMPLETE
0 (LSB)	NOT USED

Table 39. Interrupt Status Register #2 (RD 78h)	
BIT	**DESCRIPTION**
15 (MSB)	MASTER INTERRUPT
14	BC OP CODE PARITY ERROR
13	ILLEGAL COMMAND
12	GENERAL PURPOSE QUEUE/INTERRUPT STATUS QUEUE ROLLOVER
11	CALL STACK POINTER REGISTER ERROR
10	BC TRAP OP CODE
9	RT COMMAND STACK 50% ROLLOVER
8	RT CIRCULAR BUFFER 50% ROLLOVER
7	MONITOR COMMAND STACK 50% ROLLOVER
6	MONITOR DATA STACK 50% ROLLOVER
5	ENHANCED BC IRQ3
4	ENHANCED BC IRQ2
3	ENHANCED BC IRQ1
2	ENHANCED BC IRQ0
1	BIT TEST COMPLETE
0 (LSB)	INTERRUPT CHAIN BIT

Table 40. BC: General Purpose Queue Pointer Register (RD/WR, 7Ch), RT, MT: Interrupt Status Queue Pointer Register (RD/WR, 7Ch)	
BIT	**DESCRIPTION**
15 (MSB)	QUEUE POINTER BASE ADDRESS 15
• • •	• • •
6	QUEUE POINTER BASE ADDRESS 15
5	QUEUE POINTER ADDRESS 5
• • •	• • •
0 (LSB)	QUEUE POINTER ADDRESS 0

The data listed in **Table 41** through **Table 46** are not registers, but are words stored in RAM:

Table 41. BC Mode Block Status Word

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

Table 42. RT Mode Block Status Word

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

Table 43. 1553 Command Word	
BIT	**DESCRIPTION**
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
•	•
•	•
•	•
11	REMOTE TERMINAL ADDRESS BIT 0
10	TRANSMIT RECEIVE
9	SUBADDRESS/MODE CODE BIT 4
•	•
•	•
•	•
5	SUBADDRESS/MODE CODE BIT 0
4	DATA WORD COUNT/MODE CODE BIT 4
•	•
•	•
•	•
0(LSB)	DATA WORD COUNT/MODE CODE BIT 0

Table 44. Word Monitor Identification Word	
BIT	**DESCRIPTION**
15(MSB)	GAP TIME
•	•
•	•
•	•
8	GAP TIME
7	WORD FLAG
6	$\overline{\text{THIS RT}}$
5	$\overline{\text{BROADCAST}}$
4	ERROR
3	COMMAND/$\overline{\text{DATA}}$
2	CHANNEL B/$\overline{\text{A}}$
1	CONTIGUOUS DATA/$\overline{\text{GAP}}$
0(LSB)	$\overline{\text{MODE_CODE}}$

Table 45. Message Monitor Mode Block Status Word	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

Table 46. 1553B Status Word	
BIT	**DESCRIPTION**
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
14	REMOTE TERMINAL ADDRESS BIT 3
13	REMOTE TERMINAL ADDRESS BIT 2
12	REMOTE TERMINAL ADDRESS BIT 1
11	REMOTE TERMINAL ADDRESS BIT 0
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPTANCE
0(LSB)	TERMINAL FLAG

The following is a summary of the functions of the Enhanced Mini-ACE's 24 non-test registers:

Interrupt Mask Registers #1 and #2

The Interrupt Mask Registers #1 and #2 are used to enable and disable interrupt requests for various conditions.

Configuration Registers #1 and #2

The Configuration Registers #1 and #2 are used to select the Enhanced Mini-ACE's mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-On-Error, RT Memory Management mode selection, and control of the Time Tag operation.

Start/Reset Register

The Start/Reset Register is used for "command" type functions such as software reset, BC/MT Start, Interrupt reset, Time Tag Reset, Time Tag Register Test, Initiate protocol self-test, Initiate RAM self-test, Clear self-test register, and Clear RT Halt. The Start/Reset Register also includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

BC/RT Command Stack Register

The BC/RT Command Stack Register allows the host CPU to determine the pointer location for the current or most recent message.

BC Instruction List Pointer Register

The BC Instruction List Pointer Register may be read to determine the current location of the Instruction List Pointer for the Enhanced BC mode.

BC Control Word/RT Subaddress Control Word Register

In BC mode, this register allows host access to the current word or most recent BC Control Word. The BC Control Word contains bits

that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. In RT mode, this register allows host access to the current or most recent Subaddress Control Word. The Subaddress Control Word is used to select the memory management scheme and enable interrupts for the current message. The read/write accessibility can be used as an aid for testing the Enhanced Mini-ACE.

Time Tag Register

The Time Tag Register maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 μs/LSB. The Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of the RAM.

Interrupt Status Registers #1 and #2

The Interrupt Status Registers #1 and #2 allow the host processor to determine the cause of an interrupt request by means of one or two read accesses. The interrupt events of the two Interrupt Status Registers are mapped to correspond to the respective bit positions in the two Interrupt Mask Registers. Interrupt Status Register #2 contains an INTERRUPT CHAIN bit, used to indicate an interrupt event from Interrupt Status Register #1.

Configuration Registers #3, #4, and #5

The Configuration Registers #3, #4, and #5 are used to enable many of the Enhanced Mini-ACE's advanced features that were implemented by the prior generation products, the ACE and Mini-ACE (Plus). For BC, RT, and MT modes, use of the ENHANCED MODE enables the various read-only bits in Configuration Register #1. For the BC mode, the enhanced mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message. For RT mode, the enhanced mode features include the expanded RT Block Status Word, combined RT/Selective Message Monitor mode, internal wrapping of the $\overline{\text{RTFAIL}}$ output signal to the $\overline{\text{RTFAIL}}$ RT Status Word bit;

subaddresses, and the alternate (fully software programmable) RT Status Word. For MT mode, use of the enhanced mode enables the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

RT/Monitor Data Stack Address Register

The RT/Monitor Data Stack Address Register provides a read/write indication of the last data word stored for RT or Monitor modes.

BC Frame Time Remaining Register

The BC Frame Time Remaining Register provides a read-only indication of the time remaining in the current BC frame. The resolution of this register is 100 μs/LSB.

BC Time Remaining to Next Message Register

The BC Time Remaining to Next Message Register provides a read-only indication of the time remaining before the start of the next message in a BC frame. The resolution of this register is 1 μs/LSB.

BC Frame Time/RT Last Command/MT Trigger Word Register.

In BC mode, this register is used to program the BC frame time, for use in the frame auto-repeat mode. The resolution of this register is 100 μs/LS, with a range up to 6.55 seconds. In RT mode, this register stores the current (or most previous) 1553 Command Word processed by the Enhanced Mini-ACE RT. In the Word Monitor mode, this register is used to specify a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

BC Initial Instruction List Pointer Register

The BC Initial Instruction List Pointer Register enables the host to assign the starting address for the BC Instruction List.

RT Status Word Register and BIT Word Registers

The RT Status Word Register and BIT Word Registers provide read-only indications of the RT Status and BIT Words.

Test Mode Registers 0-7

These registers are included for factory test. In normal operation, these registers do not need to be accessed by the host processor.

Configuration Registers #6 and #7

The Configuration Registers #6 and #7 are used to enable features of Enhanced Mini-ACE's that extend beyond the architecture of the ACE/Mini-ACE (Plus). These include the Enhanced BC mode; RT Global Circular Buffer (including buffer size); the RT/MT Interrupt Status Queue, including valid/invalid message filtering; enabling a software-assigned RT address; clock frequency selection; a base address for the "non-data" portion of Enhanced Mini-ACE memory; LSB filtering for the Synchronize (with data) time tag operations; and enabling a watchdog timer for the Enhanced BC message sequence control engine.

BC Condition Code Register

The BC Condition Code Register is used to enable the host processor to read the current value of the Enhanced BC Message Sequence Control Engine's condition flags.

BC General Purpose Flag Register

The BC General Purpose Flag Register allows the host processor to be able to set, clear, or toggle any of the Enhanced BC Message Sequence Control Engine's General Purpose condition flags.

BIT Test Status Register

The BIT Test Status Register is used to provide read-only access of the status of the protocol and RAM built-in self-tests (BIT).

BC General Purpose Queue Pointer

The BC General Purpose Queue Pointer provides a means for initializing the pointer for the General Purpose Queue, for the Enhanced BC mode. In addition, this register enables the host to determine the current location of the General Purpose Queue pointer, which is incremented internally by the Enhanced BC message sequence control engine.

RT/MT Interrupt Status Queue Pointer Register

The RT/MT Interrupt Status Queue Pointer Register provides a means for initializing the pointer for the Interrupt Status Queue, for RT, MT, and RT/MT modes. In addition, this register enables the host to determine the current location of the Interrupt Status Queue pointer, which is incremented internally by the RT/MT message processor.

6.9 Bus Controller (BC) Architecture

The BC functionality for the Enhanced Mini-ACE includes two separate architectures: (1) the older, non-Enhanced mode, which provides complete compatibility with the previous ACE and Mini-ACE (Plus) generation products; and (2) the newer, Enhanced BC mode. The Enhanced BC mode offers several new powerful architectural features. These include the incorporation of a highly autonomous BC message sequence control engine, which greatly serves to offload the operation of the host CPU.

The Enhanced BC's message sequence control engine provides a high degree of flexibility for implementing major and minor frame scheduling; capabilities for inserting asynchronous messages in the middle of a frame; to separate 1553 message data from control/status data for the purpose of implementing double buffering and performing bulk data transfers; for implementing message retry schemes, including the capability for automatic bus channel switchover for failed messages; and for reporting various conditions to the host processor by means of 4 user-defined interrupts and a general purpose queue.

In both the non-Enhanced and Enhanced BC modes, the Enhanced Mini-ACE BC implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of the BC Control Word and the T/$\overline{R}$ bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The Enhanced Mini-ACE BC response timeout value is programmable with choices of 18, 22, 50,

and 130 μs. The longer response timeout values allow for operation over long buses and/or use of the repeaters.

In its non-Enhanced mode, the Enhanced Mini-ACE may be programmed to process BC frames of up to 512 messages with no processor intervention. In the Enhanced BC mode, there is no explicit limit to the number of messages that may be processed in a frame. In both modes, it is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally, using a programmable BC frame timer, or from an external trigger input.

Enhanced BC Mode: Message sequence control. One of the major new architectural features of the Enhanced Mini-ACE series is its advanced capability for BC message sequence control. The Enhanced Mini-ACE supports highly autonomous BC operation, which greatly offloads the operation of the host processor.

The operation of the Enhanced Mini-ACE's message sequence control engine is illustrated in **Figure 37**. The BC message sequence control involves an instruction list pointer register; an instruction list which contains multiple 2-word entries; a message control/status stack, which contains multiple 8-word or 10-word descriptors; and data blocks for individual messages.

The initial value of the instruction list pointer register is initialized by the host processor (via Register 0D), and is incremented by the BC message sequence processor (host readable via Register 03). During operation, the message sequence control processor fetches the operation referenced by the instruction list pointer register from the instruction list.

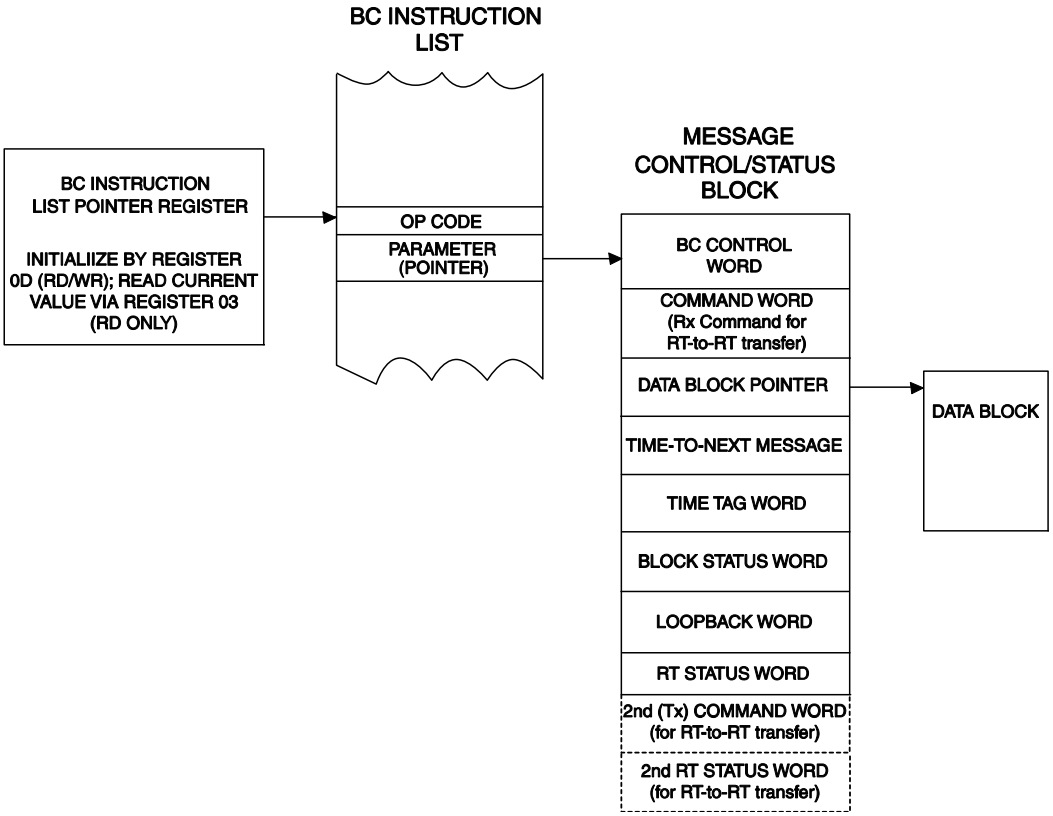


Figure 37. BC Message Sequence Control

Note: *The pointer parameter referencing the first word of a message's control/status block (the BC Control Word) must contain an address value that is* ***modulo 8****. Also, note that if the message is an RT-to-RT transfer, the pointer parameter must contain an address value that is* ***modulo 16****.*

Op Codes. The instruction list pointer register references a pair of words in the BC instruction list: an op code word, followed by a parameter word. The format of the op code word, which is illustrated in **Figure 38**, includes a 5-bit op code field and a 5-bit condition code field. The op code identifies the instruction to be executed by the BC message sequence controller.

Most of the operations are conditional, with execution dependent on the contents of the condition code field. Bits 3-0 of the condition code field identify the particular condition. Bit 4 of the condition code field identifies the logic sense ("1" or "0") of the selected condition code on which the conditional execution is dependent. **Table 47** lists all the op codes, along with their respective mnemonic, code value, parameter, and description. **Table 48** defines all the condition codes.

Eight of the condition codes (8 through F) are set or cleared as the result of the most recent message. The other eight are defined as "General Purpose" condition codes GP0 through GP7. There are three mechanisms for programming the values of the General Purpose Condition Code bits: (1) They may be set, cleared, or toggled by the host processor, by means of the BC GENERAL PURPOSE FLAG REGISTER; (2) they may be set, cleared, or toggled by the BC message sequence control processor, by means of the GP Flag Bits (FLG) instruction; and (3) GP0 and GP1 **only** (but none of the others) may be set or cleared by means of the BC message sequence control processor's Compare Frame Timer (CFT) or Compare Message Timer (CMT) instructions.

The host processor also has read-only access to the BC condition codes by means of the BC CONDITION CODE REGISTER.

Note: *Four (4) instructions are* ***unconditional****. These are Compare to Frame Timer (CFT), Compare to Message Timer (CMT), GP Flag Bits (FLG), and Execute and Flip (XQF). For these instructions, the Condition Code Field is "don't care". That is, these instructions are* ***always*** *executed, regardless of the result of the condition code test.*

All other instructions are conditional. That is, they will only be executed if the condition code specified by the condition code field in the op code word tests true. If the condition code field tests false, the instruction list pointer will skip down to the next instruction.

As shown in **Table 47**, many of the operations include a single-word parameter. For an XEQ (execute message) operation, the parameter is a pointer to the start of the message's control/status block. For other operations, the parameter may be an address, a time value, an interrupt pattern, a mechanism to set or clear general purpose flag bits, or an immediate value. For several op codes, the parameter is "don't care" (not used).

As described above, some of the op codes will cause the message sequence control processor to execute messages. In this case, the parameter references the first word of a message control/status block. With the exception of RT-to-RT transfer messages, all message status/control blocks are eight words long: a block control word, time-to-next-message parameter, data block pointer, command word, status word, loopback word, block status word, and time tag word.

In the case of an RT-to-RT transfer message, the size of the message control/status block increases to 16 words. However, in this case, the last six words are not used; the ninth and tenth words are for the second command word and second status word.

The third word in the message control/status block is a pointer that references the first word of the message's data word block.

Note: *The data word block stores **only** data words, which are to be either transmitted or received by the BC. By segregating data words from command words, status words, and other control and "housekeeping" functions, this architecture enables the use of convenient, usable data structures, such as circular buffers and double buffers.*

Other operations support program flow control; i.e., jump and call capability. The call capability includes maintenance of a call stack which supports a maximum of **four (4)** entries; there is also a return instruction. In the case of a call stack overrun or underrun, the BC will issue an CALL STACK POINTER REGISTER ERROR interrupt, if enabled.

Other op codes may be used to delay for a specified time; start a new BC frame; wait for an external trigger to start a new frame; do comparisons based on frame time and time-to-next message; load the time tag or frame time registers; halt; and issue host interrupts. In the case of host interrupts, the message control processor passes a 4-bit user-defined interrupt vector to the host, by means of the Enhanced Mini-ACE's Interrupt Status Register.

The purpose of the FLG instruction is to enable the message sequence controller to set, clear, or toggle the value(s) of any or all of the eight general purpose condition flags.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Odd Parity	OpCode Field					0	1	0	1	0	Condition Code Field				

Figure 38. BC Op Code Format

The op code parity bit encompasses all sixteen bits of the op code word. This bit must be programmed for odd parity. If the message sequence control processor fetches an undefined op code word, an op code word with even parity, or bits 9-5 of an op code word do not have a binary pattern of 01010, the message sequence control processor will immediately halt the BC's operation. In addition, if enabled, a BC TRAP OP CODE interrupt will be issued. Also, if enabled, a parity error will result in an OP CODE PARITY ERROR interrupt.

Table 47. BC Operations for Message Sequence Control					
Instruction	**Mnemonic**	**Op Code (hex)**	**Parameter**	**Conditional or Unconditional**	**Description**
Execute Message	XEQ	0001	Message Control/Status Block Address	Conditional (See NOTE)	Executes the message at the specified Message Control/Status Block Address if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Jump	JMP	0002	Instruction List Address	Conditional	Jump to the OpCode specified in the Instruction List if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Subroutine Call	CAL	0003	Instruction List Address	Conditional	Jump to the OpCode specified by the Instruction List Address and push the Address of the Next OpCode on the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. Note that the maximum depth of the subroutine call stack is **four**.
Subroutine Return	RTN	0004	Not Used (Don't Care)	Conditional	Return to the OpCode popped off the Cal Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Interrupt Request	IRQ	0006	Interrupt Bit Pattern in 4 LS bits	Conditional	Generate an interrupt if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. The passed parameter (IRQ Bit Pattern) specifies which of the ENHANCED BC IRQ bit(s) (bits 5-2) will be set in Interrupt Status Register #2. Only the four LSBs of the passed parameter are used. A parameter where the four LSBs are logic "0" will **not** generate an interrupt.
Halt	HLT	0007	Not Used (Don't Care)	Conditional	Stop execution of the Message Sequence Control Program until a new BC Start is issued by the host if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.

NOTE: While the XEQ (Execute Message) instruction is conditional, not all condition codes may be used to enable its use. The ALWAYS and NEVER condition codes may be used. The eight general purpose flag bits, GP0 through GP7, may also be used. However, if GP0 through GP7 are used, it is imperative that the host processor **not** modify the value of the specific general purpose flag bit that enabled a particular message while that message is being processed. Similarly, the LT, GT-EQ, EQ, and NE flags, which the BC only updates by means of the CFT and CMT instructions, may also be used. However, these two flags are dual use. Therefore, if these are used, it is imperative that the host processor **not** modify the value of the specific flag (GP0 or GP1) that enabled a particular message while that message is being processed. The NORESP, FMT ERR, GD BLK XFER, MASKED STATUS SET, BAD MESSAGE, RETRY0, and RETRY1 condition codes are **not** available for use with the XEQ instruction and should not be used to enable its execution.

Table 47. BC Operations for Message Sequence Control					
Instruction	**Mnemonic**	**Op Code (hex)**	**Parameter**	**Conditional or Unconditional**	**Description**
Delay	DLY	0008	Delay Time Value (resolution = 1 μs/LSB)	Conditional	Delay the time specified by the Time parameter before executing the next OpCode if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay. The delay generated will use the Time to Next Message Timer.
Wait Until Frame Timer = 0	WFT	0009	Not Used (Don't care)	Conditional	Wait until Frame Time counter is equal to Zero before continuing execution of Message Sequence Control Program if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Compare to Frame Timer	CFT	000A	Delay Time Value (resolution = 100 μs/LSB)	Unconditional	Compare Time Value to Frame Time Counter. The LT/GP0 and EQ/GP1 flag bits are set or cleared based on the results of the compare. If the value of the CFT's parameter is less than the value of the frame time counter, then the LT/GP0 and NE/$\overline{GP1}$ flags will be set, while the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be cleared. If the value of the CFT's parameter is equal to the value of the frame time counter, then the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be set, while the LT/GP0 and NE/$\overline{GP1}$ flags will be cleared. If the value of the CFT's parameter is greater than the current value of the frame time counter, then the GT-EQ/$\overline{GP0}$ and NE/$\overline{GP1}$ flags will be set, while the LT/GP0 and EQ/GP1 flags will be cleared.

Table 47. BC Operations for Message Sequence Control

Instruction	Mnemonic	Op Code (hex)	Parameter	Conditional or Unconditional	Description
Compare to Message Timer	CMT	000B	Delay Time Value (resolution = 1 μs/LSB)	Unconditional	Compare Time Value to Message Time Counter. The LT/GP0 and EQ/GP1 flag bits are set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 and NE/$\overline{GP1}$ flags will be set, while the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be cleared. If the value of the CMT's parameter is equal to the value of the message time counter, then the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be set, while the LT/GP0 and NE/$\overline{GP1}$ flags will be cleared. If the value of the CMT's parameter is greater than the current value of the message time counter, then the GT-EQ/$\overline{GP0}$ and NE/$\overline{GP1}$ flags will be set, while the LT/GP0 and EQ/GP1 flags will be cleared.
GP Flag Bits	FLG	000C	Used to set, clear, or Toggle GP (General Purpose) flag bits (see description)	Unconditional	Used to set, toggle, or clear any or all of the eight general purpose flags. The table below illustrates the use of the GP Flag Bits instruction for the case of GP0 (General Purpose Flag 0). Bits 1 and 9 of the parameter byte affect flag GP1, bits 2 and 10 effect GP2, etc., according to the following rules:
					Bit 8 | Bit 0 | Effect on GP0
					0 | 0 | No change
					0 | 1 | Set Flag
					1 | 0 | Clear Flag
					1 | 1 | Toggle Flag
Load Time Tag Counter	LTT	000D	Time Value. Resolution (μs/LSB) is defined by bits 9, 8, and 7 of Configuration Register #2.	Conditional	Load Time Tag Counter with Time Value if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.

Table 47. BC Operations for Message Sequence Control					
Instruction	**Mnemonic**	**Op Code (hex)**	**Parameter**	**Conditional or Unconditional**	**Description**
Load Frame Timer	LFT	000E	Time Value (resolution = 100 μs/LSB)	Conditional	Load Frame Timer Register with the Time Value parameter if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Start Frame Timer	SFT	000F	Not Used (Don't Care)	Conditional	Start Frame Time Counter with Time Value in Time Frame register if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Time Tag Register	PTT	0010	Not Used (Don't Care)	Conditional	Push the value of the Time Tag Register on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Block Status Word	PBS	0011	Not Used (Don't Care)	Conditional	Push the Block Status Word for the most recent message on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Immediate Value	PSI	0012	Immediate Value	Conditional	Push Immediate data on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Indirect	PSM	0013	Memory Address	Conditional	Push the data stored at the specified memory location on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Wait for External Trigger	WTG	0014	Not Used (Don't Care)	Conditional	Wait until a logic "0"-to-logic "1" transition on the EXT_TRIG input signal before proceeding to the next OpCode in the instruction list if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Execute and Flip	XQF	0015	Message Control/Status Block Address	Unconditional	Execute (unconditionally) the message for the Message Control/Status Block Address. Following the processing of this message, if the condition flag tests TRUE, then flip bit 4 in the Message Control/Status Block

Table 47. BC Operations for Message Sequence Control					
Instruction	**Mnemonic**	**Op Code (hex)**	**Parameter**	**Conditional or Unconditional**	**Description**
					Address, and store the new Message Block Address as the updated value of the parameter following the XQF instruction code. As a result, the **next** time that this line in the instruction list is executed, the Message Control/Status Block at the **updated** address (**old address XOR 0010h**), rather than the old address, will be processed.

Table 48. BC Condition Codes			
BIT CODE	**NAME (Bit 4 = 0)**	**INVERSE (Bit 4 = 1)**	**FUNCTIONAL DESCRIPTION**
0000	LT/GP0	GT-EQ/$\overline{GP0}$	Less than or GP0 flag. This bit is set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 and NE/$\overline{GP1}$ flags will be set, while the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be cleared. If the value of the CMT's parameter is equal to the value of the message time counter, then the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be set, while the LT/GP0 and NE/$\overline{GP1}$ flags will be cleared. If the value of the CMT's parameter is greater than the current value of the message time counter, then the GT-EQ/$\overline{GP0}$ and NE/$\overline{GP1}$ flags will be set , while the LT/GP0 and EQ/GP1 flags will be cleared. Also, General Purpose Flag 1 may also be set or cleared by a FLG operation.
0001	EQ/GP1	NE/$\overline{GP1}$	Equal Flag. This bit is set or cleared after CFT or CMT operation. If the value of the CMT's parameter is equal to the value of the message time counter, then the EQ/GP1 flag will be set and the NE/$\overline{GP1}$ bit will be cleared. If the value of the CMT's parameter is not equal to the value of the message time counter, then the NE/$\overline{GP1}$ flag will be set and the EQ/GP1 bit will be cleared. Also, General Purpose Flag 1 may also be set or cleared by a FLG operation.
0002	GP2	$\overline{GP2}$	General Purpose Flags set or cleared by FLG operation or by host processor. The host processor can set, clear, or toggle these flags in the same way as the FLG instruction by means of the BC GENERAL PURPOSE FLAG REGISTER.
0003	GP3	$\overline{GP3}$	
0004	GP4	$\overline{GP4}$	
0005	GP5	$\overline{GP5}$	
0006	GP6	$\overline{GP6}$	
0007	GP7	$\overline{GP7}$	
0008	NORESP	RESP	NORESP indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The Enhanced Mini-ACE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 μs (±1 μs) by means of bits 10 and 9 of Configuration Register #5.
0009	FMT ERR	$\overline{FMT_ERR}$	FMT ERR indicates that the received portion of the most recent message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the RT's status word received from a responding RT

Table 48. BC Condition Codes

BIT CODE	NAME (Bit 4 = 0)	INVERSE (Bit 4 = 1)	FUNCTIONAL DESCRIPTION
			contained an incorrect RT address field.
000A	GD BLK XFER	BAD BLK XFER	For the most recent message, GD BLK XFER will be set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is **always** logic "0" following a BC-to-RT transfer, a mode code with data, or a mode code without data. The Loop Test has **no effect** on GOOD DATA BLOCK TRANSFER. GOOD DATA BLOCK TRANSFER may be used to determine if the transmitting portion of an RT-to-RT transfer was error free.
000B	MASKED STATUS SET	MASKED STATUS CLR	Indicates that one or both of the following conditions have occurred for the most recent message: (1) If one (or more) of the Status Mask bits (14 through 9) in the BC Control Word is logic "0" **and** the corresponding bit(s) is (are) set (logic "1") in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0," any or all of the 3 Reserved Status bits being set will result in a MASKED STATUS SET condition; **and/or** (2) If BROADCAST MASK ENABLED/ $\overline{\text{XOR}}$ (bit 11 of Configuration Register #4) is logic "1" **and** the MASK BROADCAST bit of the message's BC Control Word is logic "0" **and** the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1".
000C	BAD MESSAGE	GOOD MESSAGE	Indicates either a format error, loop test fail, or no response error for the most recent message. Note that a “Status Set” condition has **no effect** on the “BAD MESSAGE/GOOD MESSAGE” condition code.
000D	RETRY0	$\overline{\text{RETRY0}}$	These two bits reflect the retry status of the most recent message. The number of times that the message was retried is delineated by these two bits as shown below: RETRY COUNT 1 (bit 14) / RETRY COUNT 0 (bit 13) / Number of Message Retries 0 / 0 / 0 0 / 1 / 1 1 / 0 / N/A 1 / 1 / 2
000E	RETRY1	$\overline{\text{RETRY1}}$	
000F	ALWAYS	NEVER	The ALWAYS flag should be set (bit 4 = 0) to designate an instruction as unconditional. The NEVER bit (bit 4 = 1) can be used to implement an NOP or “skip” instruction.

The Enhanced Mini-ACE BC message sequence control capability enables a high degree of offloading of the host processor. This includes

using the various timing functions to enable autonomous structuring of major and minor frames. In addition, by implementing conditional jumps and subroutine calls, the message sequence control processor greatly simplifies the insertion of asynchronous, or “out-of-band” messages.

Execute and Flip Operation. The Enhanced Mini-ACE BC’s XQF, or “Execute and Flip” operation, provides some unique capabilities. Following execution of this unconditional instruction, if the condition code tests TRUE, the BC will modify the value of the current XQF instruction’s pointer parameter by toggling bit 4 in the pointer. That is, if the selected condition flag tests true, the value of the parameter will be updated to the value = old address XOR 0010h. As a result, the **next** time that this line in the instruction list is executed, the Message Control/Status Block at the **updated** address (**old address XOR 0010h**), rather than the one at the old address, will be processed. The operation of the XQF instruction is illustrated in **Figure 39**.

There are multiple ways of utilizing the “execute and flip” functionality. One is to facilitate the implementation of a double buffering data scheme for individual messages. This allows the message sequence control processor to “ping-pong” between a pair of data buffers for a particular message. By so doing, the host processor can access one of the two Data Word blocks, while the BC reads or writes the alternate Data Word block.

A second application of the “execute and flip” capability is in association with message retries. This allows the BC to not only switch buses when retrying a failed message, but to automatically switch buses **permanently** for all future times that the same message is to be processed. This not only provides a high degree of autonomy from the host CPU, but saves BC bandwidth, by eliminating future attempts to process messages on an RT’s failed channel.

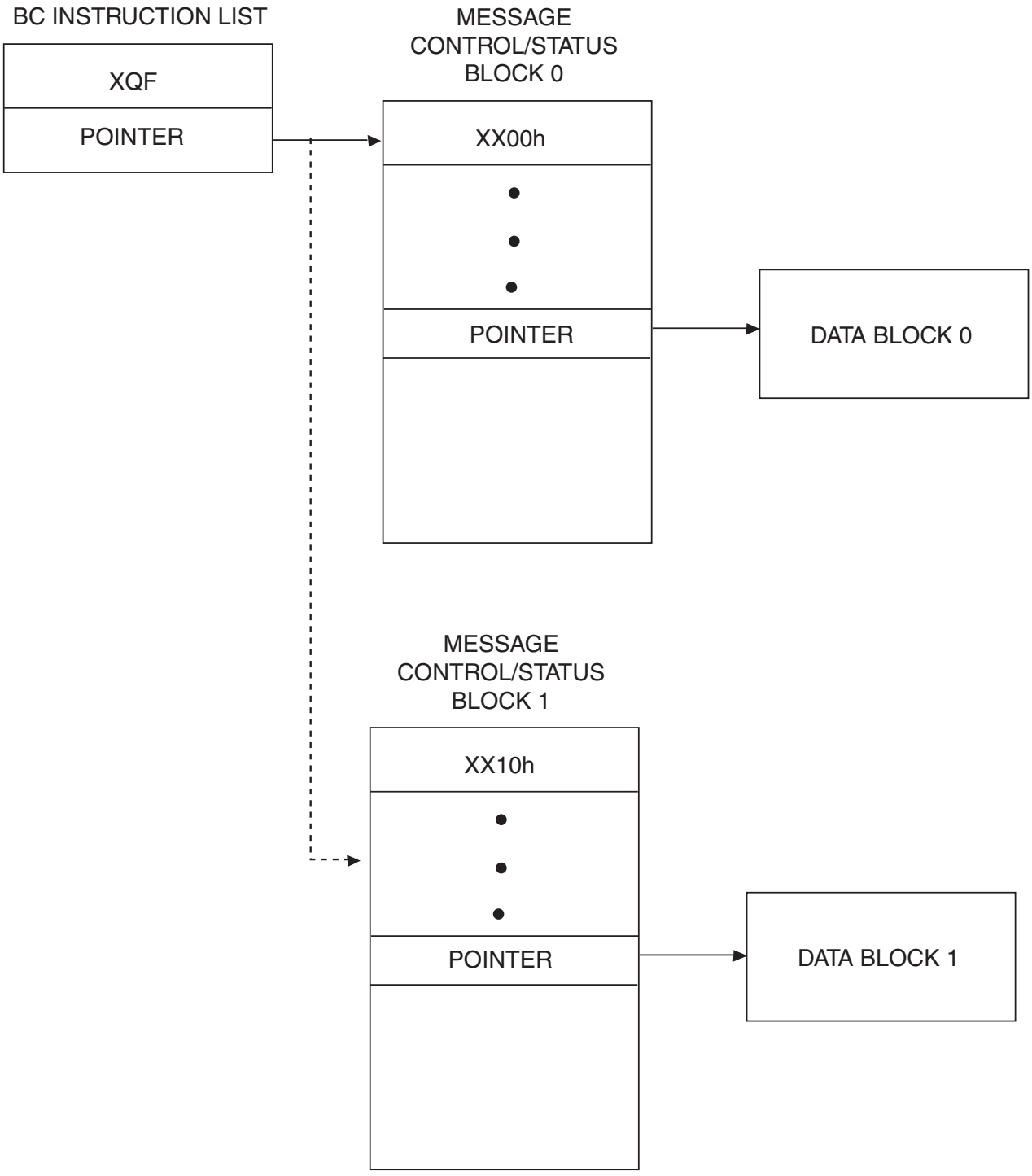


Figure 39. Execute and Flip (XQF) Operation

General Purpose Queue. The Enhanced Mini-ACE BC allows for the creation of a general purpose queue. This data structure provides a means for the message sequence processor to convey information to the BC host. The BC op code repertoire provides mechanisms to push various items on this queue. These include the contents of the Time Tag Register, the Block Status Word for the most recent message, an immediate data value, or the contents of a specified memory address. **Figure 40** illustrates the operation of the BC General Purpose Queue. Note that the BC General Purpose Queue Pointer Register will always point to the **next** address location (modulo 64); that is, the location **following** the last location written by the BC message sequence control engine.

If enabled, a BC GENERAL PURPOSE QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word boundary.

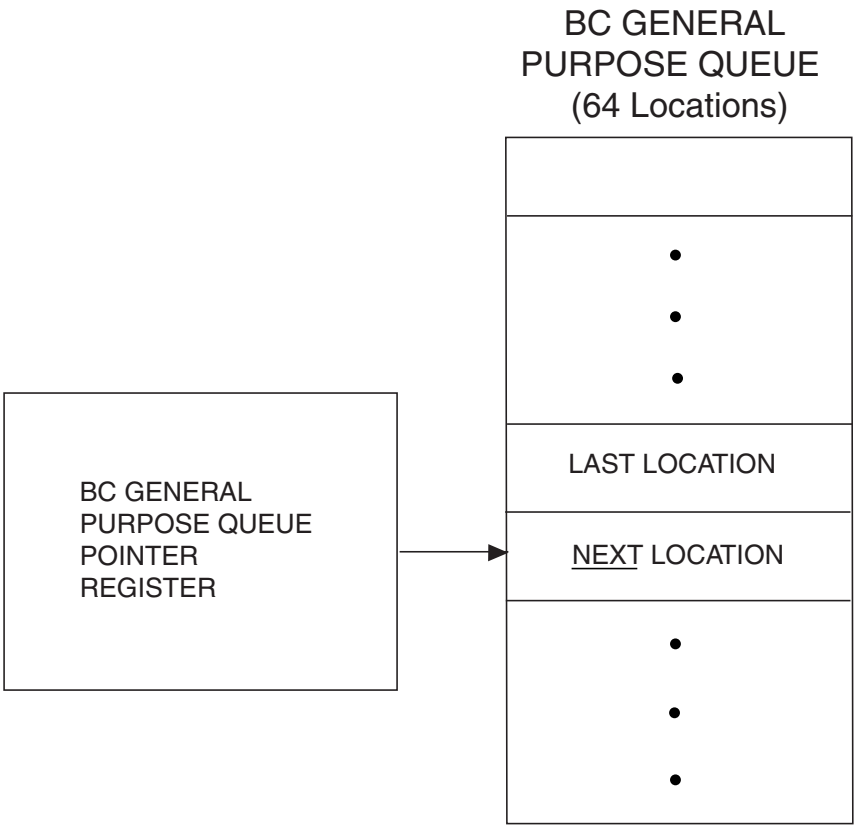


Figure 40. BC General Purpose Queue

6.10 Remote Terminal (RT) Architecture

The Enhanced Mini-ACE RT architecture provides multiprotocol support, with full compliance to all of the commonly used data bus standards, including MIL-STD-1553A, MIL-STD-1553B, Notice 2, STANAG 3838, General Dynamics 16PP303, and McAirA3818, A5232, and A5690. For the Enhanced Mini-ACE RT mode, there is programmable flexibility enabling the RT to be configured to fulfill any set of system requirements. This includes the capability to meet the MIL-STD-1553A response time requirement of 2 to 5 μs, and multiple options for mode code subaddresses, mode codes, RT status word, and RT BIT word.

The Enhanced Mini-ACE RT protocol design implements all of the MIL-STD-1553B message formats and dual redundant mode codes. The design has passed validation testing for MIL-STD-1553B compliance. The Enhanced Mini-ACE RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. One of the main features of the Enhanced Mini-ACE RT is its choice of memory management options. These include single buffering by subaddress, double buffering for individual receive subaddresses, circular buffering by individual subaddresses, and global circular buffering for multiple (or all) subaddresses.

Other features of the Enhanced Mini-ACE RT include a set of interrupt conditions, an interrupt status queue with filtering based on valid and/or invalid messages, internal command illegalization, programmable busy by subaddress, multiple options on time tagging, and an “auto-boot” feature which allows the RT to initialize as an online RT with the busy bit set following power turn-on.

6.10.1 RT Memory Organization

Table 49 illustrates a typical memory map for an Enhanced Mini-ACE RT, showing the lower 4K X 16 of shared RAM. The two Stack Pointers reside in fixed locations in the PCI address space: address 0200-0201 (hex) for the Area A Stack Pointer and address 0208-0209 for the Area B Stack Pointer. In addition to the Stack Pointer, there are several other areas of the shared RAM address space that are designated as fixed locations (all shown in **bold**). These are for the Area A and Area B lookup tables, the illegalization lookup table, the busy lookup table, and the mode code data tables.

The RT lookup tables (reference **Table 50**) provide a mechanism for allocating data blocks for individual transmit, receive, or broadcast subaddresses. The RT lookup tables include subaddress control words as well as the individual data block pointers. If command illegalization is used, address range 0300-03FF is used for command illegalizing. The descriptor stack RAM area, as well as the individual data blocks, may be located in any of the non-fixed areas in the shared RAM address space.

Note that in **Table 49**, there is no area allocated for "Stack B". This is shown for purpose of illustration. Also note that the allocated area for the RT command stack is 256 words. However, larger stack sizes are possible. That is, the RT command stack size may be programmed for 256 words (64 messages), 512, 1024, or 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register 3.

Table 49. Typical RT Memory Map (Shown For Lower 4k X 16 RAM)	
PCI ADDRESS OFFSET (hex)	**DESCRIPTION (fixed locations shown in bold)**
0000-01EE	Stack A
0200-0201	Stack Pointer A
0202-0203	Global Circular Buffer A Pointer
0204-0206	RESERVED
0208-0209	Stack Pointer B
020A-020B	Global Circular Buffer A Pointer
020C-020F	RESERVED
0210-021F	Mode Code Selective Interrupt Table
0220-026F	Mode Code Data
0280-037F	Lookup Table A
0380-047F	Lookup Table B
0480-048F	Busy Bit Lookup Table
0490-04BF	(not used)
04C0-04FF	Data Block 0
0500-05FF	Data Block 1-4
0600-07FF	Command Illegalizing Table
0800-083F	Data Block 5
087C-087F	Data Block 6
•	•
•	•
•	•
1FC0-1FFF	Data Block 100

6.10.2 RT Memory Management

The Enhanced Mini-ACE provides a variety of RT memory management capabilities. As with the ACE and Mini-ACE, the choice of memory management scheme is fully programmable on a transmit/receive/broadcast subaddress basis.

In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from non-broadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block, a double buffered configuration (two alternating Data Word blocks), or a variable-sized (128 to 8192 words) subaddress circular buffer may be allocated for data storage. The memory management scheme for individual subaddresses is designated by means of the subaddress control word (reference **Table 51**).

For received data, there is also a global circular buffer mode. In this configuration, the data words received from multiple (or all) subaddresses are stored in a common circular buffer structure. Like the subaddress circular buffer, the size of the global circular buffer is programmable, with a range of 128 to 8192 data words.

The double buffering feature provides a means for the host processor to easily access the most recent, complete received block of valid Data Words for any given subaddress. In addition to helping ensure data sample consistency, the circular buffer options provide a means of greatly reducing host processor overhead for multi-message bulk data transfer applications.

End-of-message interrupts may be enabled either globally (following all messages), following error messages, on a transmit/receive/broadcast subaddress or mode code basis, or when a circular buffer reaches its midpoint (50% boundary) or lower (100%) boundary. A pair of interrupt status registers allow the host processor to determine the cause of all interrupts by means of a single read operation.

Table 50. RT Lookup Tables (Addresses are PCI address offsets (hex))			
AREA A	**AREA B**	**DESCRIPTION**	**COMMENT**
0280-0281 • • • 02BE-02BF	0380-0381 • • • 03BE-03BF	Rx(/Bcst) SA0 • • • Rx(/Bcst) SA31	Receive (/Broadcast) Lookup Pointer Table
02C0-02C1 • • • 02FE-02FF	03C0-03C1 • • • 03FE-03FF	Tx SA0 • • • Tx SA31	Transmit Lookup Pointer Table
0300-0301 • • • 033E-033F	0400-0401 • • • 043E-043F	Bcst SA0 • • • Bcst SA31	Broadcast Lookup Pointer Table (Optional)
0340-0341 • • • 037E-037F	0440-0441 • • • 047E-047F	SACW SA0 • • • SACW SA31	Subaddress Control Word Lookup Table (Optional)

Table 51. RT Subaddress Control Word Memory Management Options					
Double-Buffered or Global Circular Buffer (bit 15)	Subaddress Control Word Bits			Memory Management Subaddress Buffer Scheme Description	
	MM2	MM1	MM0		
0	0	0	0	Single Message	
1	0	0	0	For Receive or Broadcast: Double Buffered For Transmit: Single Message	
0	0	0	1	128-Word	Subaddress-specific Circular Buffer Of Specified Size
0	0	1	0	256-Word	
0	0	1	1	512-Word	
0	1	0	0	1024-Word	
0	1	0	1	2048-Word	
0	1	1	0	4096-Word	
0	1	1	1	8192-Word	
1	1	1	1	(for receive and/or broadcast messages only) Global Circular Buffer. The buffer size is specified by bits 11-9 of Configuration Register 6.	

6.10.3 Single Buffered Mode

The operation of the single buffered RT mode is illustrated in **Figure 41**. In the single buffered mode, the respective lookup table entry must be written by the host processor. Received data words are written to, or transmitted data words are read from the data word block with starting address referenced by the lookup table pointer. In the single buffered mode, the current lookup table pointer is not updated by the Enhanced Mini-ACE memory management logic. Therefore, if a subsequent message is received for the same subaddress, the same Data Word block will be overwritten or overread.

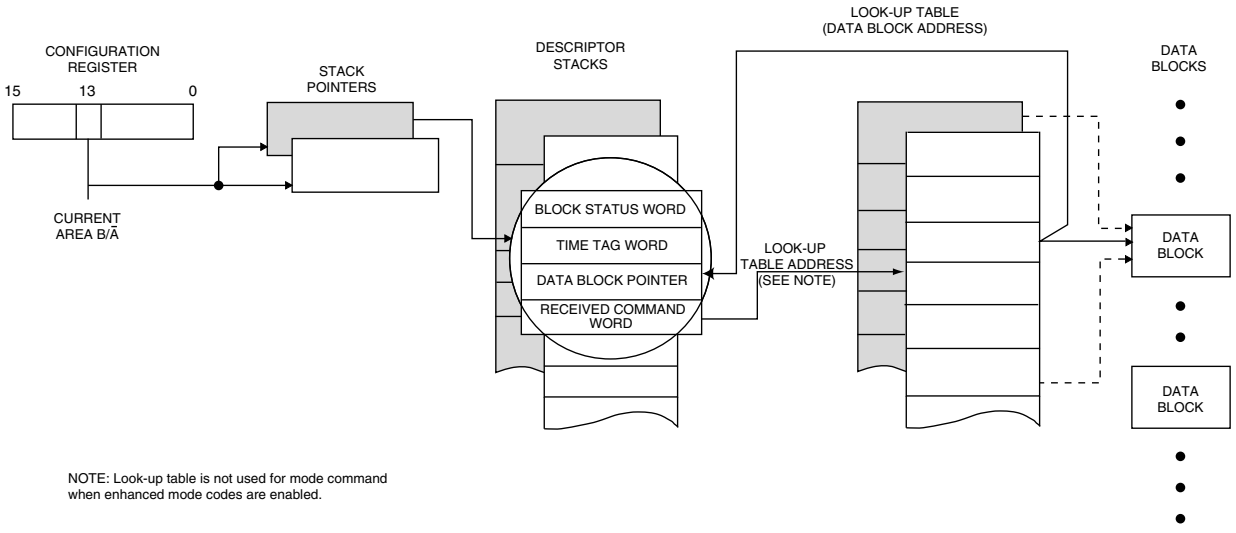


Figure 41. RT Single Buffered Mode

6.10.4 Subaddress Double Buffering Mode

The Enhanced Mini-ACE provides a double buffering mechanism for received data, that may be selected on an individual subaddress basis for any and all receive (and/or broadcast) subaddresses. This is illustrated in **Figure 42**. It should be noted that the Subaddress Double Buffering mode is applicable for receive data only, not for transmit data. Double buffering of transmit messages may be easily implemented by software techniques.

The purpose of the subaddress double buffering mode is to provide data sample consistency to the host processor. This is accomplished by allocating two 32-word data word blocks for each individual receive (and/or broadcast receive) subaddress. At any given time, one of the blocks will be designated as the “active”1553 block while the other will be considered as “inactive”. The data words for the next receive command to that subaddress will be stored in the active block. Following receipt of a valid message, the Enhanced Mini-ACE will automatically switch the active and inactive blocks for that subaddress. As a result, the latest, valid, complete data block is always accessible to the host processor.

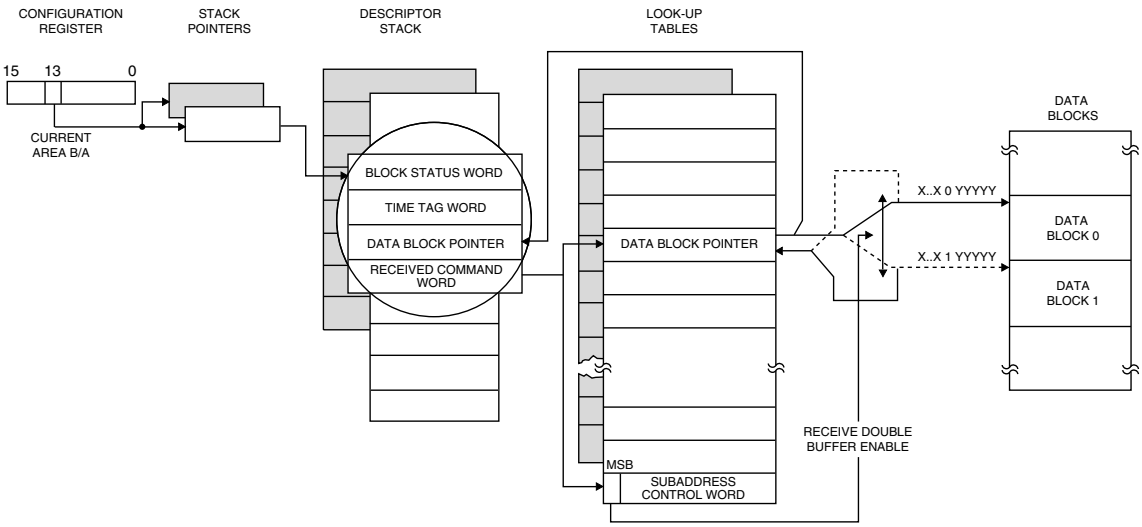


Figure 42. RT Double Buffered Mode

6.10.5 Circular Buffer Mode

The operation of the Enhanced Mini-ACE's circular buffer RT memory management mode is illustrated in **Figure 43**. As in the single buffered and double buffered modes, the individual lookup table entries are initially loaded by the host processor. At the start of each message, the lookup table entry is stored in the third position of the respective message block descriptor in the descriptor stack area of RAM. Receive or transmit data words are transferred to (from) the circular buffer, starting at the location referenced by the lookup table pointer.

In general, the location after the last data word written or read (modulo the circular buffer size) during the message is written to the respective lookup table location during the end-of-message sequence. By so doing, data for the next message for the respective transmit, receive(/broadcast), or broadcast subaddress will be accessed from the next lower contiguous block of locations in the circular buffer.

For the case of a receive (or broadcast receive) message with a data word error, there is an option such that the lookup table pointer will only be updated following receipt of a valid message. That is, the pointer will not be updated following receipt of a message with an error in a data word. This allows failed messages in a bulk data transfer to be retried without disrupting the circular buffer data structure, and without intervention by the RT's host processor.

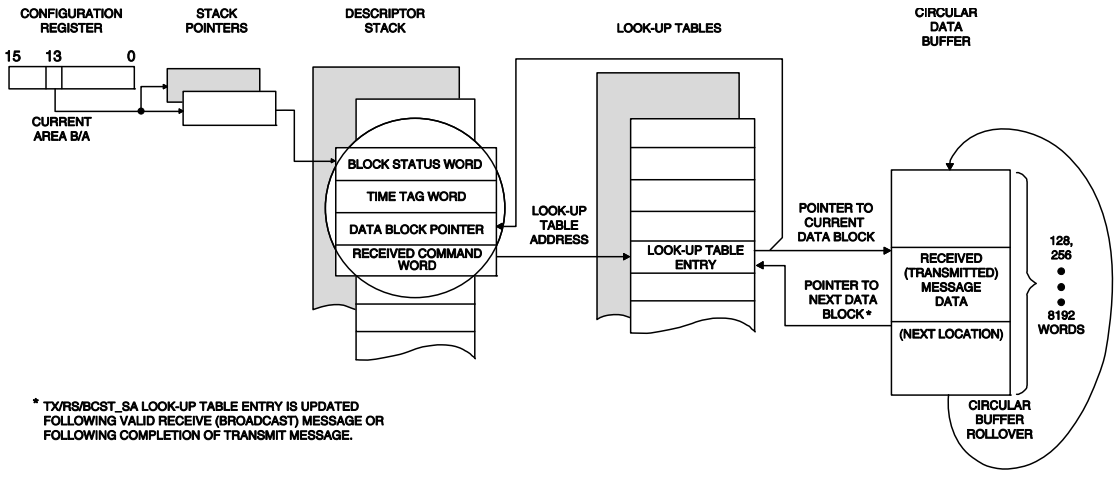


Figure 43. RT Circular Buffered Mode

6.10.6 Global Circular Buffer

Beyond the programmable choice of single buffer mode, double buffer mode, or circular buffer mode, programmable on an individual subaddress basis, the Enhanced Mini-ACE RT architecture provides an additional option, a variable sized **global** circular buffer. The Enhanced Mini-ACE RT allows for a mix of single buffered, double buffered, and individually circular buffered subaddresses, **along with** the use of the global double buffer for any arbitrary group of receive(/broadcast) or broadcast subaddresses.

In the global circular buffer mode, the data for **multiple** receive subaddresses is stored in the same circular buffer data structure. The size of the global circular buffer may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words, by means of bits 11, 10, and 9 of Configuration Register #6. As shown in **Table 51**, individual subaddresses may be mapped to the global circular buffer by means of their respective subaddress control words.

The pointer to the Global Circular Buffer will be stored in location 0101 (for Area A), or location 0105 (for Area B).

The global circular buffer option provides a highly efficient method for storing received message data. It allows for frequently used subaddresses to be mapped to individual data blocks, while also providing a method for asynchronously received messages to infrequently used subaddresses to be logged to a common area. Alternatively, the global circular buffer provides an efficient means for storing the received data words for **all** subaddresses. Under this method, all received data words are stored chronologically, regardless of subaddress.

6.10.7 RT Descriptor Stack

The descriptor stack provides a chronology of all messages processed by the Enhanced Mini-ACE RT. Reference **Figure 41**, **Figure 42**, and **Figure 43**. Similar to BC mode, there is a four-word block descriptor in the Stack for each message processed. The four entries to each block descriptor are the Block Status Word, Time Tag Word, the pointer to the start of the message's data block, and the 16-bit received Command Word.

The RT Block Status Word includes indications of whether a particular message is ongoing or has been completed, what bus channel it was received on, indications of illegal commands, and flags denoting various message error conditions. For the double buffering, subaddress circular buffering, and global circular buffering modes, the data block pointer may be used for locating the data blocks for specific messages. Note that for mode code commands, there is an option to store the transmitted or received data word as the third word of the descriptor, in place of the data block pointer.

The Time Tag Word provides a 16-bit indication of relative time for individual messages. The resolution of the Enhanced Mini-ACE's time tag is programmable from among 2, 4, 8, 16, 32, or 64 µs/LSB. There is also a provision for using an external clock input for the time tag (consult factory). If enabled, there is a time tag rollover interrupt, which is issued when the value of the time tag rolls over from FFFF(hex) to 0. Other time tag options include the capabilities to clear the time tag register following receipt of a Synchronize (without data) mode command and/or to set the time tag following receipt of a Synchronize (with data) mode command. For that latter, there is an added option to filter the "set" capability based on the LSB of the received data word being equal to logic "0".

6.10.8 RT Interrupts

The Enhanced Mini-ACE offers a great deal of flexibility in terms of RT interrupt processing. By means of the Enhanced Mini-ACE's two Interrupt Mask Registers, the RT may be programmed to issue interrupt requests for the following events/conditions: End-of-(every)Message, Message Error, Selected (transmit or receive) Subaddress, 100% Circular Buffer Rollover, 50% Circular Buffer Rollover, 100% Descriptor Stack Rollover, 50% Descriptor Stack Rollover, Selected Mode Code, Transmitter Timeout, Illegal Command, and Interrupt Status Queue Rollover.

Interrupt for 50% Rollovers of Stacks, Circular Buffers. The Enhanced Mini-ACE RT and Monitor are capable of issuing host interrupts when a subaddress circular buffer pointer or stack pointer crosses its mid-point boundary. For RT circular buffers, this is applicable for both transmit and receive subaddresses. Reference **Figure 44**. There are four interrupt mask and interrupt status register bits associated with the 50% rollover function: (1) RT circular buffer; (2) RT command (descriptor) stack; (3) Monitor command (descriptor) stack; and (4) Monitor data stack.

The 50% rollover interrupt is beneficial for performing bulk data transfers. For example, when using circular buffering for a particular receive subaddress, the 50% rollover interrupt will inform the host processor when the circular buffer is half full. At that time, the host may proceed to read the received data words in the upper half of the buffer, while the Enhanced Mini-ACE RT writes received data words to the lower half of the circular buffer. Later, when the RT issues a 100% circular buffer rollover interrupt, the host can proceed to read the received data from the lower half of the buffer, while the Enhanced Mini-ACE RT continues to write received data words to the upper half of the buffer.

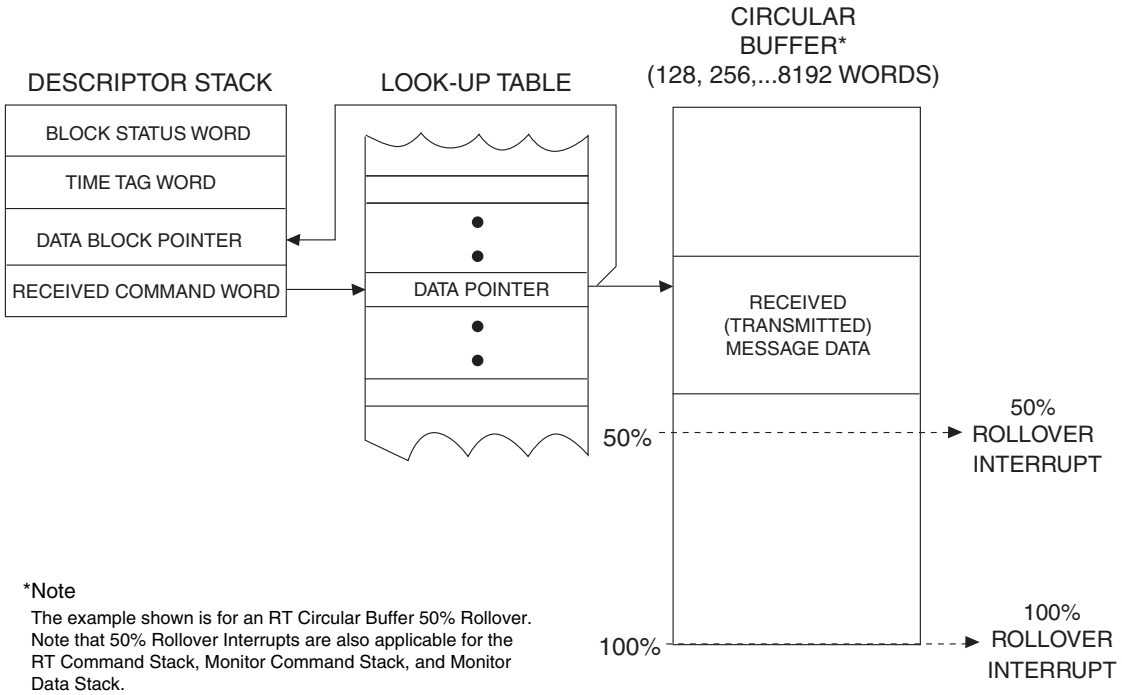
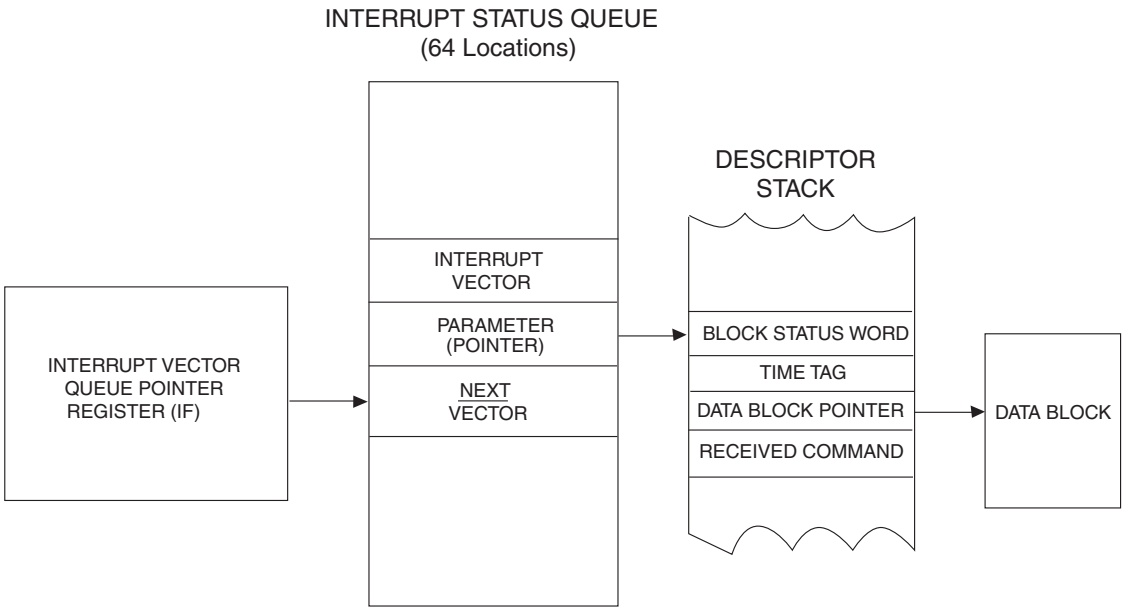


Figure 44. 50% and 100% Rollover Interrupts

Interrupt status queue. The Enhanced Mini-ACE RT, Monitor, and combined RT/Monitor modes include the capability for generating an interrupt status queue. As illustrated in **Figure 45**, this provides a chronological history of interrupt generating events and conditions. In addition to the Interrupt Mask Register, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in the creation of an entry to the Interrupt Status Queue.



(shown for message interrupt event)

Figure 45. RT (and Monitor) Interrupt Status Queue

The pointer to the Interrupt Status Queue is stored in the INTERRUPT VECTOR QUEUE POINTER REGISTER (register address 1F). This register must be initialized by the host, and is subsequently incremented by the RT message processor. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages.

The queue rolls over at addresses of modulo 64. The events that result in queue entries include both message-related and non-message related events. Note that the Interrupt Vector Queue Pointer Register will always

point to the next location (modulo 64) **following** the last vector/pointer pair written by the Enhanced Mini-ACE RT, Monitor, or RT/Monitor.

Each event that causes an interrupt results in a two-word entry to be written to the queue. The first word of the entry is the interrupt vector. The vector indicates which interrupt event(s)/condition(s) caused the interrupt.

The interrupt events are classified into two categories: message interrupt events and non-message interrupt events. Message-based interrupt events include End-of-Message, Selected mode code, Format error, Subaddress control word interrupt, RT Circular buffer Rollover, Handshake failure, RT Command stack rollover, transmitter timeout, and RT Circular buffer 50% rollover. Non-message interrupt events/conditions include Time tag rollover, RT address parity error, MT data stack rollover, MT command stack rollover, RAM parity error, RT Command stack 50% rollover, MT data stack 50% rollover, MT command stack 50% rollover, and BIT completed.

Bit 0 of the interrupt vector (interrupt status) word indicates whether the entry is for a message interrupt event (if bit 0 is logic "1") or a non-message interrupt event (if bit 0 is logic "0"). It is **not** possible for one entry on the queue to indicate both a message interrupt and a non-message interrupt.

As illustrated in **Figure 45**, for a message interrupt event, the parameter word is a pointer. The pointer will reference the first word of the RT or MT command stack descriptor (i.e., the Block Status Word).

For a RAM Parity Error non-message interrupt, the parameter will be the RAM address where the parity check failed. For the RT address Parity Error and Protocol Self-test Complete non-message interrupts, the parameter is not used; it will have a value of 0000. For a Time Tag Rollover non-message interrupt, the parameter will be a pointer to the descriptor stack.

If enabled, an INTERRUPT STATUS QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word address boundary.

6.10.9 RT Command Illegalization

The Enhanced Mini-ACE provides an internal mechanism for RT Command Word illegalizing. By means of a 256-word area in shared RAM, the host processor may designate that any message be illegalized, based on the command word T/R bit, subaddress, and word count/mode code fields. The Enhanced Mini-ACE illegalization scheme provides the maximum in flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/$\overline{R}$ bit, subaddress, and word count/mode code to be illegalized.

The address map of the Enhanced Mini-ACE's illegalizing table is illustrated in Table 52.

Table 52. Illegalization Table Memory Map

PCI ADDRESS OFFSET (hex)	DESCRIPTION
0600-0601	Brdcst/Rx, SA 0, MC15-0
0602-0603	Brdcst/SA 0, MC31-16
0604-0605	Brdcst/Rx, SA 1, WC15-0
0606-0607	Brdcst/Rx, SA 1, WC31-16
• • •	• • •
067E-067F	Brdcst/Rx, SA 0, MC15-0
0680-0681	Brdcst/Tx, SA 0, MC31-16
0682-0683	Brdcst/Tx, SA 1, WC15-0
0684-0685	Brdcst/Tx, SA 1, WC31-16
• • •	• • •
06FA-06FB	Brdcst/Tx, SA 30, WC 31-16
06FC-06FD	Brdcst/Tx, SA 31, MC 15-0
06FE-06FF	Brdcst/Tx, SA 31, MC 31-16
0700-0701	Own Addr/Rx, SA 0, MC 15-0
0702-0703	Own Addr/Rx, SA 0, MC 31-16
0704-0705	Own Addr/Rx, SA 1, WC 15-0
0706-0707	Own Addr/Rx, SA 1, WC 31-15

Table 52. Illegalization Table Memory Map	
PCI ADDRESS OFFSET (hex)	**DESCRIPTION**
• • •	• • •
077C-077D	Own Addr/RX, SA 31, MC 15-0
077E-077F	Own Addr/Rx, SA 31, MC 31-16
0780-0781	Own Addr/Tx, SA 0, MC 15-0
0782-0783	Own Addr/Tx, SA 0, MC 31-16
0784-0785	Own Addr/Tx, SA 1, WC 15-0
0786-0787	Own Addr/Tx, SA 1, WC 31-16
• • •	• • •
07F8-07F9	Own Addr/Tx, SA 30, WC 15-0
07FA-07FB	Own Addr/Tx, SA 30, WC 31-16
07FC-07FD	Own Addr/Tx, SA 31, MC 15-0
07FE-07FF	Own Addr/TX, SA 31, MC 31-16

6.10.10 Busy Bit

The Enhanced Mini-ACE RT provides two different methods for setting the Busy status word bit: (1) globally, by means of Configuration Register #1; or (2) on a T/R-bit/subaddress basis, by means of a RAM lookup table. If the host CPU asserts the $\overline{\text{BUSY}}$ bit low in Configuration Register #1, the Enhanced Mini-ACE RT will respond to **all** non-broadcast commands with the Busy bit set in its RT Status Word.

Alternatively, there is a Busy lookup table in the Enhanced Mini-ACE shared RAM. By means of this table, it is possible for the host processor to set the busy bit for any selectable subset of the 64 combinations of T/R bit and subaddress, and for transmit broadcast mode commands.

If the busy bit is set for a transmit command, the Enhanced Mini-ACE RT will respond with the busy bit set in the status word, but will not transmit any data words. If the busy bit is set for a receive command, the RT will also respond with the busy status bit set. There are two programmable

options regarding the reception of data words for a non-mode code receive command for which the RT is busy: (1) to transfer the received data words to shared RAM; or (2) to **not** transfer the data words to shared RAM.

6.10.11 RT Address

The design of the ***BU-65569T/B*** supports two different options for specifying the RT addresses for the individual Enhanced Mini-ACEs: (1) by means of the RT ADDRESS (and ODD PARITY) inputs, that are brought out to the card's J2/J3 connector, and latched under PCI host software control; or (2) fully software programmable by the PCI host, by means of an internal register. In both configurations, the RT address is readable by the host processor.

6.10.12 RT Built-In Test (BIT) Word

The bit map for the Enhanced Mini-ACE's internal RT Built-in-Test (BIT) Word is indicated in Table 53.

Table 53. RT BIT Word

Bit	DESCRIPTION
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	BIT TEST FAIL
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

6.10.12.1 RT Auto-Boot Option

DDC can supply a non-standard version of the ***BU-65569T/B*** card which allows one or more of the card's Enhanced Mini-ACEs to automatically initialize as an active remote terminal with the Busy status word bit set to logic "1" immediately following power turn-on. This is a useful feature for MIL-STD-1760 applications, in which the RT is required to be responding within 150 ms after power-up. This feature is available for versions of the Enhanced Mini-ACE with 4K words of RAM. For this option, please consult factory.

6.10.12.2 Other RT Features

The Enhanced Mini-ACE includes options for the Terminal flag status word bit to be set either under software control and/or automatically following a failure of the loopback self-test. Other software programmable RT options include software programmable RT status and RT BIT words, automatic clearing of the Service Request bit following receipt of a Transmit vector word mode command, options regarding Data Word transfers for the Busy and Message error (illegal) Status word bits, and options for the handling of 1553A and reserved mode codes.

6.11 Monitor Architecture

The Enhanced Mini-ACE includes three monitor modes:

A Word Monitor mode.

A selective message monitor mode.

A combined RT/message monitor mode.

For new applications, it is recommended that the selective message monitor mode be used, rather than the word monitor mode. Besides providing monitor filtering based on RT address, T/R bit, and subaddress, the message monitor eliminates the need to determine the start and end of messages by software.

6.11.1 Word Monitor Mode

In the Word Monitor Terminal mode, the Enhanced Mini-ACE monitors both 1553 buses. After the software initialization and Monitor Start sequences, the Enhanced Mini-ACE stores all Command, Status, and Data Words received from both buses. For each word received from either bus, a pair of words is stored to the Enhanced Mini-ACE's shared RAM. The first word is the word received from the 1553 bus. The second word is the Monitor Identification (ID), or "Tag" word. The ID word contains information relating to bus channel, word validity, and inter-word time gaps. The data and ID words are stored in a circular buffer in the shared RAM address space.

6.11.2 Word Monitor Memory Map

A typical word monitor memory map is illustrated in Table 54. Table 54 assumes a 64K address space for the Enhanced Mini-ACE's monitor. The Active Area Stack pointer provides the address where the first monitored word is stored. In the example, it is assumed that the Active Area Stack Pointer for Area A (location 0200-0201) is initialized to 0000. The first received data word is stored in location 0000-0001, the ID word for the first word is stored in location 0002-0003, etc.

The current Monitor address is maintained by means of a counter register. This value may be read by the CPU by means of the Data Stack Address Register. It is important to note that when the counter reaches the Stack Pointer address of 0100 or 0104, the initial pointer value stored

in this shared RAM location **will be overwritten** by the monitored data and ID Words. When the internal counter reaches an address of FFFF, the counter rolls over to 0000.

Table 54. Typical Word Monitor Memory Map

PCI ADDRESS OFFSET (hex)	FUNCTION
0000-0001	First Received 1553 Word
0002-0003	First Identification Word
0004-0005	Second Received 1553 Word
0006-0007	Second Identification Word
0008-0009	Third Received 1553 Word
000A-000B	Third Identification Word
• • •	• • •
0200-0201	Stack Pointer (Fixed Location – gets overwritten)
• • •	• • Received 1553 words and Identification words • •
FFFE-FFFF	

6.11.3 Word Monitor Trigger

In the Word Monitor mode, there is a pattern recognition trigger and a pattern recognition interrupt. The 16-bit compare word for both the trigger and the interrupt is stored in the Monitor Trigger Word Register. The pattern recognition interrupt is enabled by setting the MT Pattern Trigger bit in the Interrupt Mask Register. The pattern recognition trigger is enabled by setting the Trigger Enable bit in Configuration Register #1 and selecting either the Start-on-trigger or the Stop-on-trigger bit in Configuration Register #1.

The Word Monitor may also be started by means of a low-to-high transition on the EXT_TRIG input signal.

6.11.4 Selective Message Monitor Mode

The Enhanced Mini-ACE Selective Message Monitor provides monitoring of 1553 messages with filtering based on RT address, T/R bit, and subaddress with no host processor intervention. By autonomously distinguishing between 1553 command and status words, the Message Monitor determines when messages begin and end, and stores the messages into RAM, based on a programmable filter (RT address, T/R bit, and subaddress).

The selective monitor may be configured as just a monitor, or as a combined RT/Monitor. In the combined RT/Monitor mode, the Enhanced Mini-ACE functions as an RT for one RT address (including broadcast messages), and as a selective message monitor for the other 30 RT addresses. The Enhanced Mini-ACE Message Monitor contains two stacks, a command stack and a data stack, that are independent from the BC/RT command stack. The pointers for these stacks are located at fixed locations in the RAM.

6.11.4.1 Monitor Selection Function

Following receipt of a valid command word in Selective Monitor mode, the Enhanced Mini-ACE will reference the selective monitor lookup table to determine if this particular command is enabled. The address for this location is determined by means of an offset based on the RT Address, T/$\overline{R}$ bit, and Subaddress bit 4 of the current command word, and concatenating it to the monitor lookup table base address of 0500-0501 (hex). The bit location within this word is determined by subaddress bits 3-0 of the current command word.

If the specified bit in the lookup table is logic “0”, the command is not enabled, and the Enhanced Mini-ACE will ignore this command. If this bit is logic “1”, the command is enabled and the Enhanced Mini-ACE will create an entry in the monitor command descriptor stack (based on the monitor command stack pointer), and store the data and status words associated with the command into sequential locations in the monitor data stack. In addition, for an RT-to-RT transfer in which the receive command is selected, the second command word (the transmit command) is stored in the monitor data stack.

The address definition for the Selective Monitor Lookup Table is illustrated in Table 55.

Table 55. Monitor Selection Table Lookup Address Note: The bit mapping shown in this table is for the "Enhanced Mini-ACE" word-oriented address space. To compute the byte-oriented PCI address offset, it is necessary to multiply the "Enhanced Mini-ACE" address by two.	
Address Bit	**Description**
15 (MSB)	Logic "0"
14	Logic "0"
13	Logic "0"
12	Logic "0"
11	Logic "0"
10	Logic "0"
9	Logic "1"
8	Logic "0"
7	Logic "1"
6	RTAD_4
5	RTAD_3
4	RTAD_2
3	RTAD_1
2	RTAD_0
1	TRANSMIT/$\overline{\text{RECEIVE}}$
0 (LSB)	SUBADDRESS_4

6.11.5 Selective Message Monitor Memory Organization

A typical memory map for the ACE in the Selective Message Monitor mode, assuming a 4K RAM space, is illustrated in **Table 56**. This mode of operation defines several fixed locations in the RAM. These locations are allocated in a way in which none of them overlap with the fixed RT locations. This allows for the combined RT/Selective Message Monitor mode.

The fixed memory map consists of two Monitor Command Stack Pointers (locations 102 and 106 hex), two Monitor Data Stack Pointers (locations 0206-0207 and 020E-020F hex), and a Selective Message Monitor Lookup Table (locations 0500-0501 through 05FE-05FF hex) with lookup based on RT Address, T/$\overline{\text{R}}$, and subaddress. For this example, the Monitor Command Stack size is assumed to be 1K words, and the Monitor Data Stack size is assumed to be 2K words.

Table 56. Typical Selective Message Monitor Memory Map (shown for 4K RAM for "Monitor only" mode)	
PCI ADDRESS OFFSET (hex)	**DESCRIPTION**
0200-0203	**Not Used**
0204-0205	Monitor Command Stack Pointer A (fixed location)
0206-0207	Monitor Data Stack Pointer A (fixed location)
0208-0209	Not Used
020C-020D	Monitor Command Stack Pointer B (fixed location)
020E-020F	Monitor Data Stack Pointer B (fixed location)
0210-04FF	**Not Used**
0500-05FF	Selective Monitor Lookup Table
0600-07FF	**Not Used**
0800-0FFF	Monitor Command Stack A
1000-1FFF	Monitor Data Stack A

Figure 46 illustrates the Selective Message Monitor operation. Upon receipt of a valid Command Word, the Enhanced Mini-ACE will reference the Selective Monitor Lookup Table to determine if the current command is enabled. If the current command is disabled, the Enhanced Mini-ACE monitor will ignore (and not store) the current message. If the command is enabled, the monitor will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer, and an entry in the monitor data stack starting at the location referenced by the monitor data stack pointer.

The format of the information in the data stack depends on the format of the message that was processed. For example, for a BC-to-RT transfer (receive command), the monitor will store the command word in the monitor command descriptor stack, with the data words and the receiving RT's status word stored in the monitor data stack.

The size of the monitor command stack is programmable, with choices of 256, 1K, 4K, or 16K words. The monitor data stack size is programmable with choices of 512, 1K, 2K, 4K, 8K, 16K, 32K or 64K words.

Monitor Interrupts. Selective monitor interrupts may be issued for End-of-message and for conditions relating to the monitor command stack pointer and monitor data stack pointer. The latter includes Command

Stack 50% Rollover, Command Stack 100% Rollover, Data Stack 50% Rollover, and Data Stack 100% Rollover.

The 50% rollover interrupts may be used to inform the host processor when the command stack or data stack is half full. At that time, the host may proceed to read the received messages in the upper half of the respective stack, while the Enhanced Mini-ACE monitor writes messages to the lower half of the stack. Later, when the monitor issues a 100% stack rollover interrupt, the host can proceed to read the received data from the lower half of the stack, while the Enhanced Mini-ACE monitor continues to write received data words to the upper half of the stack.

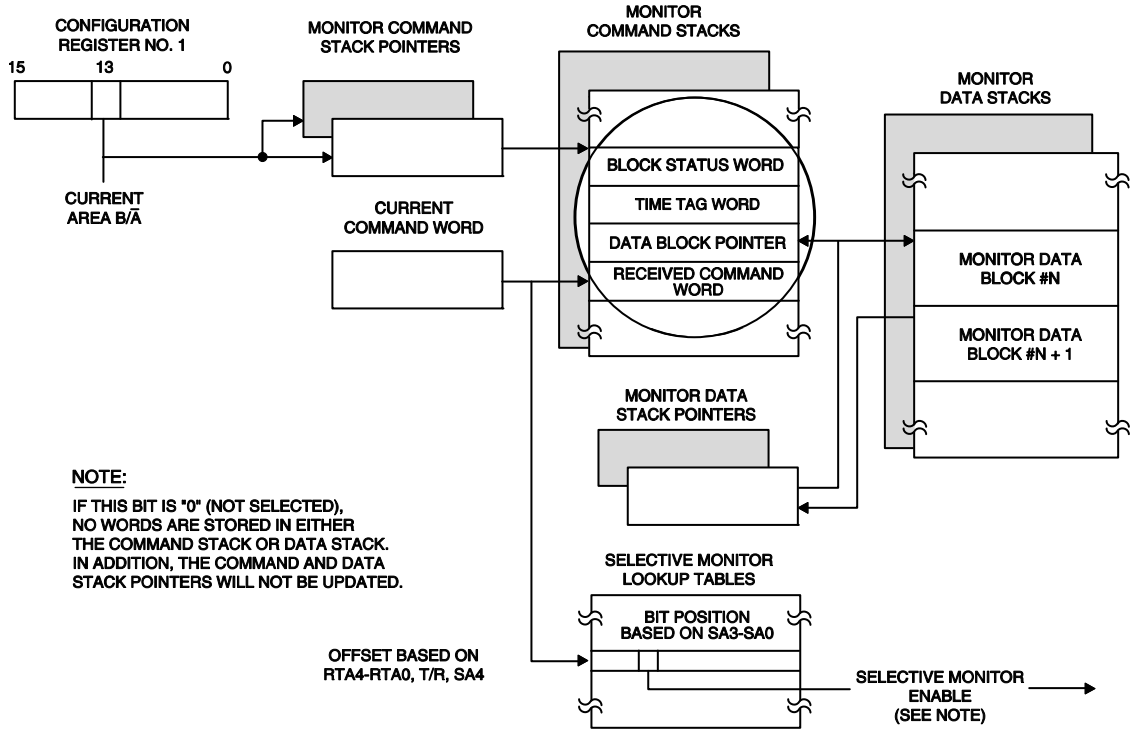


Figure 46. Selective Message Monitor Memory Management

6.11.6 Interrupt Status Queue

Like the Enhanced Mini-ACE RT, the Selective Monitor mode includes the capability for generating an interrupt status queue. As illustrated in Figure 45, this provides a chronological history of interrupt generating events. Besides the two Interrupt Mask Registers, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in entries to the Interrupt Status Queue. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 monitored messages.

6.12 Time Tag

The Enhanced Mini-ACE includes an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 μs per LSB. Another option allows software controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register. For each message processed, the value of the Time Tag Register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for both the BC and RT modes.

The functionality involving the Time Tag Register that's compatible with ACE/Mini-ACE (Plus) includes: the capability to issue an interrupt request and set a bit in the Interrupt Status Register when the Time Tag Register rolls over FFFF to 0000; for RT mode, the capability to automatically clear the Time Tag Register following reception of a Synchronize (without data) mode command, or to load the Time Tag Register following a Synchronize (with data) mode command.

Additional time tag features supported by the Enhanced Mini-ACE include the capability for the BC to transmit the contents of the Time Tag Register as the data word for a Synchronize (with data) mode command; the capability for the RT to "filter" the data word for the Synchronize with data mode command, by only loading the Time Tag Register if the LSB of the received data word is "0"; an instruction enabling the BC Message Sequence Control engine to autonomously load the Time Tag Register; and an instruction enabling the BC Message Sequence Control engine to write the value of the Time Tag Register to the General Purpose Queue.

6.13 Interrupts

The Enhanced Mini-ACE series components provide many programmable options for interrupt generation and handling. Individual interrupts are enabled by the two Interrupt Mask Registers (#1 or #2). The host processor may easily determine the cause of the interrupt by using the Interrupt Status Register (#1 or #2). The two Interrupt Status Registers (#1 and #2) provide the current state of the interrupt conditions. The Interrupt Status Registers may be updated in two ways. In the one interrupt handling mode, a particular bit in the Interrupt Status Register (#1 or #2) will be updated only if the event occurs and the corresponding bit in the Interrupt Mask Register (#1 or #2) is enabled. In the Enhanced interrupt handling mode, a particular bit in the Interrupt Status Register (#1 or #2) will be updated if the condition exists regardless of the contents of the corresponding Interrupt Mask Register

bit. In any case, the respective Interrupt Mask Register (#1 or #2) bit enables an interrupt for a particular condition.

The Enhanced Mini-ACE supports all the interrupt events from ACE/Mini-ACE (Plus), including RAM Parity Error, Transmitter Timeout, BC/RT Command Stack Rollover, MT Command Stack and Data Stack Rollover, Handshake Error, BC Retry, RT Address Parity Error, Time Tag Rollover, RT Circular Buffer Rollover, BC Message, RT Subaddress, BC End-of-Frame, Format Error, BC Status Set, RT Mode Code, MT Trigger, and End-of-Message.

For the Enhanced Mini-ACE's Enhanced BC mode, there are four user-defined interrupt bits. The BC Message Sequence Control Engine includes an instruction enabling it to issue these interrupts at any time.

For RT and Monitor modes, the Enhanced Mini-ACE architecture includes an Interrupt Status Queue. This provides a mechanism for logging messages that result in interrupt requests. Entries to the Interrupt Status Queue may be filtered such that only valid and/or invalid messages will result in entries on the queue.

Enhanced Mini-ACE incorporates additional interrupt conditions beyond ACE/Mini-ACE (Plus), based on the addition of Interrupt Mask Register #2 and Interrupt Status Register #2. This is accomplished by chaining of the two Interrupt Status Registers (#1 and #2) using one of the bits in Interrupt Status Register #2 to indicate an interrupt has occurred in Interrupt Status Register #1. Additional interrupts include "Self Test Completed", masking bits for the Advanced BC Control Interrupts, 50% Rollover interrupts for RT Command Stack, RT Circular Buffers, MT Command Stack, and MT Data Stack; BC Op Code Parity Error, (RT) Illegal Command, (BC) General Purpose Queue or (RT/MT) Interrupt Status Queue Rollover, Call Stack Pointer Register Error, BC Trap Op Code, and four User-Defined interrupts for the Enhanced BC mode.

Table 57. BU-65569T/B Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
ABSOLUTE MAXIMUM RATINGS				
Supply Voltage				
+3.3V	-0.3		6.0	V
+5 V	-0.3		7.0	V
RECEIVER				
Input Impedance, Transformer Coupled (Notes 1-3)	1.000			kohm
Threshold Voltage, Transformer Coupled	0.200		0.860	V_{P-P}
Common Mode Voltage (Note 4)			10	V_{PEAK}
TRANSMITTER				
Differential Output Voltage				
Transformer Coupled Across 70 ohms	18	20	27	V_{P-P}
Output Offset Voltage, Transformer Coupled Across 70 ohms	-250	150	250	mV_{PEAK}
Rise/Fall Time	100	150	300	ns
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances (Note 9)				
+3.3 V (logic power)	3.0	3.3	3.6	V
+5 V (RAM and transceiver power)	4.75	5.0	5.5	V
Current Drain				
BU-65569T/B-1				
+5 V				
• Idle			100	mA
• 25% Duty Transmitter Cycle			210	mA
• 50% Duty Transmitter Cycle			320	mA
• 100% Duty Transmitter Cycle			540	mA
+3.3 V (Logic)			80	mA
BU-65569T/B-2				
+5 V				
• Idle			200	mA
• 25% Duty Transmitter Cycle			420	mA
• 50% Duty Transmitter Cycle			640	mA
• 100% Duty Transmitter Cycle			1.08	A
+3.3 V (Logic)			120	mA

Table 57. BU-65569T/B Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
BU-65569T/B-3				
+5 V				
• Idle			300	mA
• 25% Duty Transmitter Cycle			630	mA
• 50% Duty Transmitter Cycle			960	mA
• 100% Duty Transmitter Cycle			1.62	A
+3.3 V (Logic)			160	mA
BU-65569T/B-4				
+5 V				
• Idle			400	mA
• 25% Duty Transmitter Cycle			840	mA
• 50% Duty Transmitter Cycle			1.28	A
• 100% Duty Transmitter Cycle			2.16	A
+3.3 V (Logic)			200	mA
Power Dissipation				
BU-65569T/B-1				
Idle			0.84	W
25% Duty Transmitter Cycle			1.12	W
50% Duty Transmitter Cycle			1.41	W
100% Duty Transmitter Cycle			1.98	W
BU-65569T/B-2				
Idle			1.53	W
25% Duty Transmitter Cycle			2.10	W
50% Duty Transmitter Cycle			2.67	W
100% Duty Transmitter Cycle			3.81	W
BU-65569T/B-3				
Idle			2.23	W
25% Duty Transmitter Cycle			3.08	W
50% Duty Transmitter Cycle			3.93	W
100% Duty Transmitter Cycle			5.64	W
BU-65569T/B-4				
Idle			2.92	W
25% Duty Transmitter Cycle			4.06	W
50% Duty Transmitter Cycle			5.20	W

Table 57. BU-65569T/B Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
100% Duty Transmitter Cycle			7.47	W
1553 MESSAGE TIMING				
Completion of CPU Write (BC Start)-to-Start of		2.5		µs
Next Message (Non-enhanced BC mode)				
BC Intermessage Gap – (Note 5)				
Non-Enhanced (Mini-ACE compatible) BC mode		9.5		µs
Enhanced BC mode (Note 6)		10.0 to 10.5		µs
BC/RT/MT Response Timeout (Note 7)				
18.5 nominal	17.5	18.5	19.5	µs
22.5 nominal	21.5	22.5	23.5	µs
50.5 nominal	49.5	50.5	51.5	µs
128.0 nominal	127	129.5	131	µs
RT Response Time (mid-parity to mid-sync) (Note 8)	4		7	µs
Transmitter Watchdog Timeout		660.5		µs
THERMAL				
Operating Temperature				
(BU-65569TX-300)	0		+55	°C
(BU-65569TX-200)	-40		+85	°C
Storage Temperature	-55		+125	°C
PHYSICAL CHARACTERISTICS				
Size				
"3U" CompactPCI Spec, PICMG 2.0 R3.0		6.299 (L) X 3.937 (H)		in
		160 X 100		mm
Weight				
BU-65569T4		6.3 (180)		oz (g)
BU-65569B4		6.9 (198)		oz (g)

Notes 1 through 3 are applicable to the Input Impedance specification:

1. The specifications are applicable for both unpowered and powered conditions.
2. The specifications assume a 2 volt rms balanced, differential, sinusoidal input. The applicable frequency range is 75 kHz to 1 MHz
3. Minimum impedance is guaranteed over the operating range, but is not tested.

4. Assumes a common mode voltage within the frequency range of dc to 2 MHz, applied to pins of the isolation transformer on the stub side (transformer coupled), and referenced to signal.
5. Typical value for minimum intermessage gap time. Under software control, this may be lengthened to 65,535 μs - message time, in increments of 1 μs. If ENHANCED CPU ACCESS, bit 14 of Configuration Register #6, is set to logic "1", then host accesses during BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences could have the effect of lengthening the intermessage gap time. For each host access during an SOM or EOM sequence, the intermessage gap time will be lengthened by 6 clock cycles. Since there are 7 internal transfers during SOM, and 5 during EOM, this could theoretically lengthen the intermessage gap by up to 72 clock cycles; i.e., up to 7.2 μs with a 10 MHz clock, 6.0 μs with a 12 MHz clock, 4.5 μs with a 16 MHz clock, or 3.6 μs with a 20 MHz clock.
6. For enhanced BC mode, the typical value for intermessage gap time is approximately 10 clock cycles longer than for the non-enhanced BC mode. That is, an addition of 1.0 μs at 10 MHz, 833 ns at 12 MHz, 625 ns at 16 MHz, or 500 ns at 20 MHz.
7. Software programmable (4 options). Includes RT-to-RT Timeout (measured mid parity of transmit Command Word to mid-sync of Transmitting RT Status Word).
8. Measured from mid-parity crossing of Command Word to mid-sync crossing of RT's Status Word.
9. The standard ***BU-65569T/B*** board requires +3.3 volt and +5 volt power. For applications where +3.3 volts is not available, DDC is able to supply a non-standard version of the ***BU-65569T/B*** card requiring only +5 volts (consult factory).

7 GLOSSARY

Active

The active areas of the ACE memory are those locations that are currently available for use by the ACE. There are some situations, such as Double-Buffered RT messages, where one buffer is for use by the ACE, while the Host CPU designates the other buffer for use.

Bus Coupling

The coupling mode of a bus may be either direct or transformer coupled. Direct-coupled terminals will have an isolation transformer at the 1553 terminal, and must be no greater than 1 foot from the 1553 bus. A transformer-coupled terminal will have an isolation transformer at the 1553 terminal, a transformer coupler at the bus, and may be connected to the bus with no more that 20 feet of 1553 bus cable.

Driver

This is the lower level software that provides access to the hardware. All applications must use this level of software to access the hardware. The drivers for the ***BU-65569T/B*** are supplied with the card and installed according to the installation instructions.

Enumeration

Enumeration is the process that BIOS performs to determine the identification and resource requirements of all PCI devices that are used in the computer. Many of these PCI devices are not plug-in cards. They could be the disk driver controller, timers, memory bridges, etc.

ESD

Electrostatic Discharge (ESD) is caused by a potential difference in the static charge (accumulated electrons) between two objects. This is most commonly identified by an emitted spark when the two objects are moved into close proximity. Under normal conditions, the voltage potential needed to create a spark of 1 centimeter in air is 25000 volts. Obviously the generated spark will cause major catastrophic damage to many of the parts used on the ***BU-65569T/B*** board, but the spark is not the only cause of ESD damage. If the potential difference between an object and the conductive wires of the ***BU-65569T/B*** or any of the semiconductor devices is large enough (e.g., greater than 1000 volts), damage will be caused to the devices without the generation of a spark.

Inactive

The inactive areas of ACE memory are those locations that are designated for use by the Host CPU. These areas will not be written or read by the ACE device until the Host CPU releases them by toggling the applicable area control bit. This would be bit 15 of the Sub-address control word in the case of double-buffered RT messages.

RTL

The Runtime Library supplies the programming API (Application Programming Interface) to access the ***BU-65569T/B*** software functions. When these functions are used in a C program, and compiled and linked with the proper library, an executable file will be created that can be used to operate the ***BU-65569T/B***.

SEAFAC Testing

Testing performed by a US Government Agency located at Wright-Patterson Air Force Base. This testing validated the operation of military systems, including the 1553 data links. This testing is no longer performed.

Side Effects

When used in reference to ACE access, side effects are defined as unexpected actions to a performed operation. This can be seen in the access of the Interrupt Status Register. The ACE can be configured to clear this register when it is read. This would be known as a side effect. If the host CPU tries to access this register, and it is read, but the PCI transfer is halted, the CPU will have to try the read again. The second time it reads this register it will have been cleared by the previous read, and therefore report erroneous data.

8 APPENDIX A – REFERENCES

PCI System Architecture

Third Edition, copyright © 1995 by MindShare, Inc. Written by Tom Shanley and Don Anderson. Published by Addison-Wesley Publishing Company

ACE User's Guide

ACE Series BC/RT/MT Advanced Communication Engine Integrated 1553 Terminal User's Guide, Data Device Corporation, Revision J.

ACE Runtime Library Software Manual

Data Device Corporation, Revision D

MIL-STD-1553 Designer's Guide

Data Device Corporation, Sixth Edition

9 APPENDIX B – ACRONYMS

ACARS	Aircraft Communication, Addressing and ReportingSystem
ACE	Advanced Communication Engine
ACMS	Aircraft Condition Monitoring System
ATE	Automated Test Equipment
CGA	Color Graphics Adapter
CMC	Central Maintenance Computer
CMOS	Complementary Metal Oxide Semiconductor
CS	Chip Set
DADC	Digital Air Data Computer
DOS	Disk Operating System
DPRAM	Dual-Port Random Access Memory
EFIS	Electronic Flight Instruments System
EGA	Enhanced Graphics Adapter
EIU	Electronic Interface Unit
EMA	Enhanced Mini-ACE
EPROM	Erasable Programmable Read Only Memory
FIFO	First In First Out Memory
FMC	Flight Management Computer
GND	Ground (electrical)
I/O	Input/Output
IDT	Integrated Device Technology
IDU	Integrated Display Unit
IRS	Inertial Reference Unit
LRU	Line Replaceable Unit
MCDU	Multi-Control Display Unit
MHZ	Megahertz
Mini-ACE	Mini – Advanced Communication Engine
N/A	Not available
PC	Personal Computer
PCI	Peripheral Component Interconnect
PMC	PCI Mezzanine Card
RAM	Random Access Memory
ROM	Read Only Memory
RX	Receiver
TTL	Transistor-Transistor Logic
TX	Transmitter
UUT	Unit Under Test
VDC	Voltage Direct Current
VGA	Video Graphics Adapter

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