Hardware Manual
For the 1 to 4 Channel
MIL-STD-1553 Tester/Simulator
VME/VXI Interface Card

MN-65572v-001

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RECORD OF CHANGE

Revision	Date	Pages	Description
C	06/02	All	Removed Software Section

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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HOW TO USE THIS MANUAL

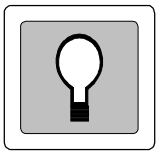
This manual uses typographical and iconic conventions to assist the reader in understanding the content. This section will define the text formatting and icons used in the rest of the manual. This manual is formatted with a 'Scholar Margin' where many tips, symbols or icons will be located.

For the full text of this manual, ***BU-65572v*** will be used to identify both the ***BU-65572v*** and the ***BU-65570v***. In those cases where there is a difference, the appropriate part number will be identified.

Text Usage

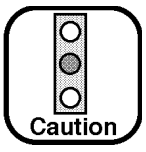
- **BOLD**–text that is written in bold letters indicates important information and table, figure, and chapter references.
- ***BOLD ITALIC***–will designate DDC Part Numbers.
- `Courier New`–is used to indicate code examples.
- <…> - Indicates user entered text or commands.

Symbols and Icons



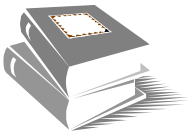
The Idea/Tip icon will be used to identify a handy bit of supplementary information that may be useful to the user.

The Note Icon signifies important supplementary information that will be useful to the user.

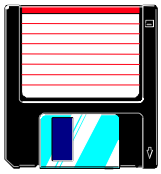


The Caution icon identifies important information that presents a possibility of damage to the product if not heeded.

Much stronger than a Caution, the Warning icon presents information pertaining to hazards that will cause damage to the product and possible injury to the user.



The Reference icon indicates that there is related material in this manual or in another specified document.



The Disk Icon describes information that is related to software.

Special Handling and Cautions

The ***BU-65572v*** uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.

- Turn off power to the VME/VXI chassis and unplug from wall.
- **NEVER** insert or remove card with power turned on.
- Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.
- Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

INTRODUCTION

The ***BU-65572v*** provides full, intelligent interfacing between one to four MIL-STD-1553 Data Buses and a VME/VXI chassis. The ***BU-65572v*** is packaged on a 'B' sized Euro card for operation in a VME chassis. The card can also be used in a VXI chassis with the use of an extender card.

Features of the board include:

- VXI Plug-and-Play (PnP) compatible for easy installation
- Onboard processor operating at 40MHz for each installed channel
- 64K Words of on-board Program RAM for each installed channel
- 64K Words of shared static RAM for each installed channel
- DMA transfer of monitored data to host data buffer via VME Master Operation
- IRIG-B time tagging combined with 32-bit onboard time tag counter
- Software configuration of Bus Coupling and Termination
- Variable output transceivers, 0 to approximately 21.5 volts with 1024 incremental steps (***BU-65572v*** only).
- Replay of previously recorded Bus Traffic via Menu and Runtime Library

Included with each ***BU-65572v*** VME/VXI Card is the DDC Menu ***BUS-69065S0*** (for Windows® 95/98/2000, Windows NT® and MXI-II compliant systems) and the Runtime Library (RTL) with example source. The RTL supports application development under Windows 95/98/NT/2000 (***BUS-69068S0***) and WindRiver's VxWorks®/Tornado II 'C' (***BUS-69068S2***) programming environments.

The 1553 Tester Simulator Menu software has the capability to simulate Bus Controller, all 31 Remote Terminals, and Monitor simultaneously on each of the installed buses. There is additional capability to synchronize the onboard time tags of all of the operating cards with one command.

What is included in this manual?

This manual contains a complete description of hardware installation and use for the ***BU-65572v*** VME/VXI Card.

System Requirements

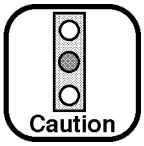
PC SUPPORT

- An IBM compatible PC with a '486 processor or better. DDC recommends a Pentium® 200MHz processor or faster
- Windows 95, 98, NT or 2000 operating system
- A National Instruments™ MXI-II connection to a VME/VXI chassis
- One available VME/VXI slot in the chassis

VME/VXI EMBEDDED SUPPORT

- A single board computer (SBC) acting as a slot-0 controller. DDC's VxWorks driver was developed using a MV2700 PowerPC™ single board computer.
- WindRiver's VxWorks Tornado II operating system
- One available VME/VXI slot in the chassis

HARDWARE INSTALLATION



The ***BU-65572v*** card is a VME/VXI Master/Target device and may be inserted into any VME/VXI compatible slot other than slot '0'. When installing the card, the following should be observed:

NEVER insert or remove the card with the power turned on.

- **ALWAYS** take proper precautions to guard against static damage. Use a wrist strap if available, or ensure proper static grounding by touching the power supply cover **WITH POWER OFF**.
- Secure with proper hardware.
- Make sure that adjacent cabling and wiring do not hinder the airflow around the card.

The ***BU-65572v*** contains configuration jumpers for selection of its Logical Address (LA), the state of its MODID line (used or unused), its memory address space (A24/A32), and the IRIG bus loading configuration. Refer to the section Hardware Configuration for more details.

Selection of direct or transformer coupling for each installed channel is performed by way of functions provided in the RTL. The DDC 1553 Card Manager will handle the translation of the MXI-II addressing (assigned through the National Instruments Resource Manager), and will allow the user to set the desired IRQ level. A logical device number will need to be assigned to each channel of the ***BU-65572Vx*** card. This logical device number is used by DDC's software to access the device.

HARDWARE CONFIGURATION

The ***BU-65572v*** is a VME/VXI device that supports VXI Plug and Play.

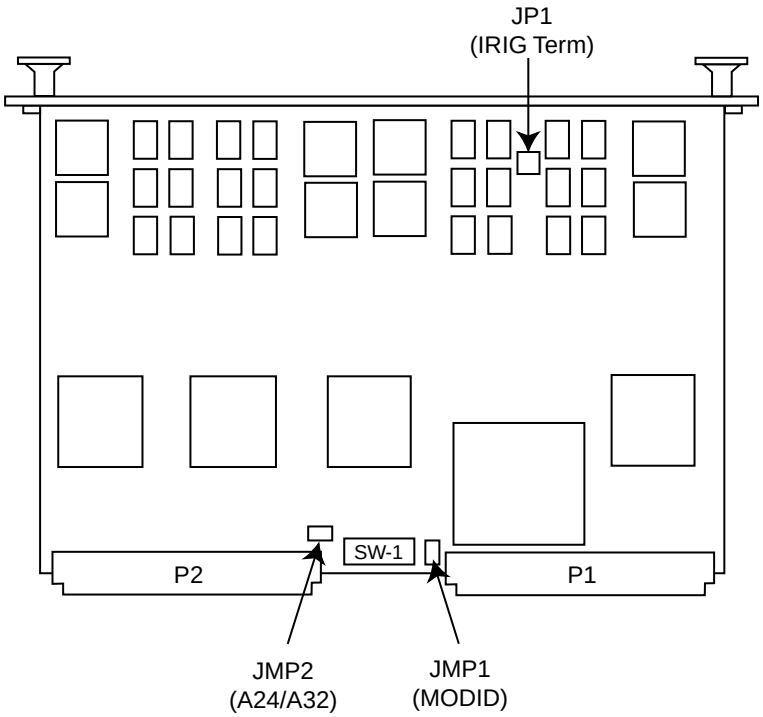


Figure 1 - Mechanical Outline

Applying the jumper at JMP1 enables the VME/VXI Plug-and-Play capability. This will apply the MODID signal at P2-A38.

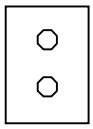


Figure 2 - JMP1 MODID

If this jumper is installed, the VXI system will attempt to determine the memory requirements of the card. The system will access the value that is set in the eight-position DIP switch (SW-1). This switch allows the user to set all eight bits of the Logical Address of the card.

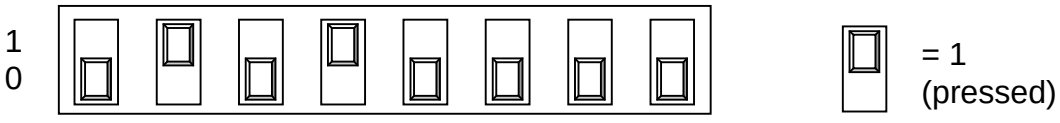


Figure 3 - SW-1, 8 Position - Logical Address

A jumper (JMP2) will specify 24-bit or 32-bit memory address space. The 24-bit address space will be specified if this jumper is in, and the 32-bit address space will be used if the jumper is out.

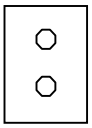


Figure 4 - JMP2 Address Space (A24/A32)

Finally, there is a 3-tap jumper block (JP1) that allows the user to select the termination for the modulated IRIG.

1 - 2: 10K ohms
3 - 4: 600 ohms
5 - 6: 50 ohms

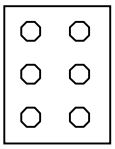


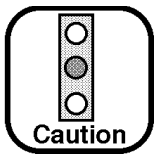
Figure 5 - JP1 IRIG Termination

Card Pinout

This section describes pinouts for the card. The card has three connectors; two DB-9 connectors that are used for 1553 Bus I/O and a DB-37 that is used for discrete, power and IRIG I/O.

The triax connectors are on the cable attachment ***DDC-71412*** that plugs into the DB 9-F connectors at J2 and J3. See Table 2 and Table 3 for pin functions. They are standard BJ77 types manufactured by Trompeter Electronics Inc. The mating connector required on the stub cable is Trompeter PL75 or equivalent (four mating connectors are supplied with the card). The connectors may be configured for transformer coupling or direct coupling. The ***BU-65572v*** card should be connected to a bus as specified by MIL-STD-1553B, refer to Figure 10 or Figure 11.

Due to heat dissipation limitations, the triax connectors should NOT be shorted for more than a few seconds while transmitting. The connector's center pin is positive during the first half of a command sync. The cables are labeled channel 1 (A and B) and channel 2 (A and B) for a 2 channel board. A four-channel board will require another cable for channels 3 and 4. Refer to Figure 6.



NOTE: All ground returns are connected to the chassis ground.

The pinouts for these connectors are shown in the following tables:

Table 1 - J1: Discrete I/O, Triggers, and IRIG

Pin	Description	Pin	Description
1	+5VDC (fuse protected)	19	Channel 1, BC Trigger In
2	IRIG Mod In	20	Chassis Ground
3	Chassis Ground	21	IRIG (Pulse) In
4	Discrete Out 16	22	Discrete Out 15
5	Discrete Out 14	23	Discrete Out 13
6	Discrete Out 12	24	Discrete Out 11
7	Discrete Out 10	25	Discrete Out 9
8	Discrete Out 8	26	Discrete Out 7
9	Discrete Out 6	27	Discrete Out 5
10	Discrete Out 4	28	Discrete Out 3
11	Discrete Out 2	29	Discrete Out 1
12	Channel 4, BC Trigger Out	30	Channel 4, Monitor Trigger Out
13	Channel 4, BC Trigger In	31	Channel 4, Monitor Trigger In
14	Channel 3, BC Trigger Out	32	Channel 3, Monitor Trigger Out
15	Channel 3, BC Trigger In	33	Channel 3, Monitor Trigger In
16	Channel 2, BC Trigger Out	34	Channel 2, Monitor Trigger Out
17	Channel 2, BC Trigger In	35	Channel 2, Monitor Trigger In
18	Channel 1, BC Trigger Out	36	Channel 1, Monitor Trigger Out
		37	Channel 1, Monitor Trigger In

Table 2 - J2: 1553 Bus 1 and 2 Connector

Pin	Description
1	CH1_TXA_L
2	CH1_TXA
3	CH1_TXB
4	CH1_TXB_L
5	GND (connected to shell)
6	CH2_TXA_L
7	CH2_TXA
8	CH2_TXB
9	CH2_TXB_L

Table 3 - J3: 1553 Bus 3 and 4 Connector

Pin	Description
1	CH3_TXA_L
2	CH3_TXA
3	CH3_TXB
4	CH3_TXBL
5	GND (connected to shell)
6	CH4_TXA_L
7	CH4_TXA
8	CH4_TXB
9	CH4_TXB_L

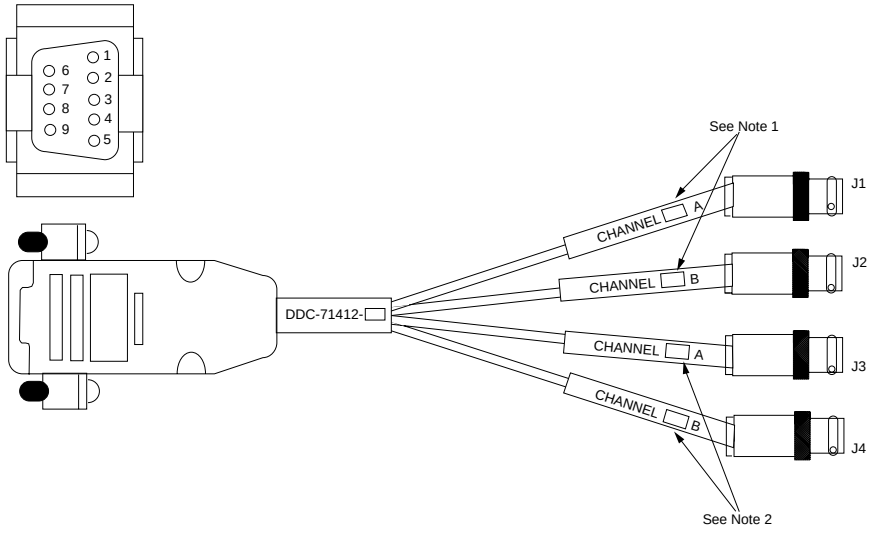


Figure 6 - DDC-71412 Cable

Fuse

There is a fuse that is located at the J1 connector. This fuse protects the Vcc (5 volt) output that is available at the connector at pin number 1. The value of this fuse is 500mA.

VME Registers

Table 4 lists the VME Registers on the ***BU-65572v*** card. Registers 0x000 through 0x0008 are standard VXI registers. Registers 0x0012, 0x0014, and 0x0028 through 0x002E are reserved. The Channel Select Register (0x000A), selects the channel for registers 0x0010 – 0x0026.

Table 4 - VME Registers

Address	Register
0	ID Register
2	Device Type Register
4	Status/Configuration Register
6	Offset Register
8	Attribute Register
A	FPGA Rev. ID / Channel Select Register
C	IRQ Level Register
E	IRQ Vector Register
10	Channel Reset Register
12	Reserved
14	Reserved
16	Channel General IRQ Register
18	Channel DAC Register
1A	Channel Relay Register
1C	Channel IRIG Enable Register
1E	Channel IRQ Status Register
20	Channel DMA Destination Register (Low)
22	Channel DMA Destination Register (High)
24	Channel DMA Block Size (Bytes)
26	Channel DMA Status
28 - 2E	Reserved
30	VME Interface Chip Write Register
32	IRIG Low Word
34	IRIG High Word
36 – 3E	Reserved

ID Register (0x0000) The ID Register is a 16-bit read-only register. Bits 15 – 14 are set to 00 and are used for Device Class Memory. Bits 13-12 are set to 00 for a A24 configured card, or 01 for a A32 card. Bits 11-0 (FE8) specify the manufacturer's ID for the card.

Device Type Register (0x0002) The Device Type register is a 16-bit read-only register. Bits 15 -12 are set to 0100 for A24 cards. For A32 cards bits 15 – 12 will be set to 1100. Bits 11 – 0 are model codes.

- A01 -- BU-65570V1
- A02 -- BU-65570V2
- A03 -- BU-65570V3
- A04 -- BU-65570V4
- A09 -- BU-65572V1
- A0A -- BU-65572V2
- A0B -- BU-65572V3
- A0C -- BU-65572V4

Status/Configuration Register (0x0004) The Status/Configuration Register is a 16-bit Read/Write register. Bit 15 is used to enable Memory Read and Writes. Bit 14 is used for the MODID. Bits 13 – 4 are used for the revision of the hardware device. Bits 3 – 0 are set to 1100.

Offset Register (0x0006) The Offset Register is a 16-bit Read/Write Register, which is used when the card is using A24 or A32 memory.

Attribute Register (0x0008) The Attribute Register is a 16-bit Read/Write Register. Bits 15 – 14 are set to "11" and are used for RAM. Bit 13 will be set to a 1 and is used for Non-Privileged and Supervisory Access. Bit 12 will be set to 0, which is used to support block transfers. Bit 11 will be set to logic 1, which is for volatile RAM. Bits 10 – 8 will be set to 000 for fast RAM. Bit 7 will be set to logic 1 for D16 and D8 only. Bits 6 – 0 will be set to 0.

FPGA Device ID / Channel Select Register (0x000A) The Channel Select register is a 2-bit Read/Write Register used to select the active channel. To set the active channel on the card to 1, write a "00" to bits 1 – 0 of the Channel Select Register. For Channel 2 write a "01", for Channel 3 write a "10", and for Channel 4 write "11" to the Channel select register. A read of this register also yields the revision of VME interface FPGA in bits 15 – 8. A write to the register does not affect the FPGA Rev. ID which is hard coded inside the FPGA.

IRQ Level Register (0x000C) The IRQ Level Register is a 3-Bit Read/Write Register which allows the user to select the IRQ level. Below are the values the register may be set to:

000 = No IRQ

001 = IRQ 1

010 = IRQ 2

011 = IRQ 3

100 = IRQ 4

101 = IRQ 5

110 = IRQ 6

111 = IRQ 7

IRQ Vector Word Register (0x000E) The IRQ Vector Word is an 8-Bit Read/Write Register. The Vector word put on the VME bus is in response to an IACK cycle. The default word is loaded with the device's logical address upon every Reset.

Channel Reset Register (0x0010) The Channel Reset Register is a 2-bit Read/Write register. Setting Bit 0 to a "0" will reset the channel. Setting the bit to a "1" will disable the reset. Setting Bit 1 to a "0" will boot the card from the EPROM, while a "1" will boot the card from the Dual Port Ram.

Channel General IRQ Register (0x0016) The Channel General IRQ Register is a 1-Bit Read/Write register that is used for the DSP IRQ signal.

Channel DAC Register (0x0018) The Channel DAC Register is a 12-Bit Register.

Channel Relay Register (0x001A) The Channel Relay Register is a 6-Bit Read/Write Register, which configures the load and coupling of the bus. A list of bit values is shown below:

Bit 0:	0 = Transformer Coupled	1 = Direct Coupled Primary Bus
Bit 1 - 2:	0 = No Load	1 = One Load Each
Bit 3:	0 = Transformer Coupled	1 = Direct Coupled Secondary Bus
Bit 4 - 5:	0 = No Load	1 = One Load Each

Channel IRIG Enable (0x001C) The Channel IRIG Enable Register is a 1-Bit Read/Write Register, which allows you to enable or disable IRIG. Writing a "1" to this register will enable IRIG which synchronizes the Time-tag with the IRIG signal. Writing a "0" to the register will disable IRIG allowing the Time-tag to run freely.

Channel IRQ Status (0x001E) The Channel IRQ status Register is a 2-Bit Read-only Register which tells the status of the IRQ. Bit 0 is used to indicate that a standard interrupt occurred. Bit 1 is used to indicate that an interrupt occurred due to a DMA transfer completion.

Channel DMA Destination Address Low (0x0020) The Channel DMA Destination Address Low Register is a 16-Bit Read/Write Register. This Register is the first 16 Bits (0-15) of the DMA Destination address.

Channel DMA Destination Address High (0x0022) The Channel DMA Destination Address High Register is a 16-Bit Read/Write Register. This Register is the last 16 Bits (16-31) of the DMA Destination address.

VME Interface Chip Write Register (0x0030) The VME Interface Chip Write Register is a 16-Bit Read/Write Register that reads or writes data to a given Vic address. Bits 15 – 8 are the VME Interface Chip Address that is to be written to, while bits 7 – 0 are the data that is being written.

IRIG Low (0x0032) IRIG Low is a 16-Bit Read/Write Register, which reads the IRIG lower 16-bit timestamp. A write will load the IRIG Register.

IRIG High (0x0034) IRIG High is a 16-Bit Read/Write Register, which reads the IRIG upper 16-bit timestamp. A write will load the IRIG Register. Data from the High word is not loaded until a Low Register Write is done.

Channel DMA Block Size (0x0024) The Channel DMA Block Size Register is a 16-bit Read-only register. Following a DMA block transfer, this register stores the number of bytes transferred.

Channel DMA Status (0x0026) The Channel DMA Status Register is an 8-bit Read-only register. Following a DMA block transfer, Bits 7 – 0 store DMA Status information as follows:

Bit 0:	Don't Care
Bit 1:	Local Bus Error occurred during DMA transfer (when "1")
Bit 2:	VME Bus Error occurred during DMA transfer (when "1")
Bits 7 – 3:	Don't Care

HARDWARE OPERATION

General

The ***BU-65572v*** is the next generation DDC VME/VXI Tester/Simulator which can simultaneously simulate a MIL-STD-1553 BC, all RTs, and an intelligent MT simultaneously on four 1553 buses.

Full error detection features are provided in all modes of operation. In addition, user specified errors, including bit count and Manchester II errors, may be injected in BC and any of the emulated RT modes.

Operational characteristics of the ***BU-65572v*** such as output voltage level, bus termination, and coupling configuration are all software controllable using functions provided in the software library.

Note: *The* ***BU-65570v*** *does not support the variable output voltage feature.*

All capabilities specified below are available for each of the installed channels on the card.

Bus Controller Mode

The ***BU-65572v*** Bus Controller supports all MIL-STD-1553B message formats. Up to 1024 unique receive, transmit, mode code, and RT to RT messages may be defined at one time for each of the installed channels. A frame can contain up to 1024 unique messages.

Programmable attributes within a message include time to next message, bus (channel A or channel B), intermessage routines, and injected error. The time to next message defines the time from the start of the present message to the start of the next message. The time to next message is programmable up to 65,535 µsec in 1-µsec increments.

MINOR AND MAJOR FRAMES

The execution of messages is controlled by a message list referred to as a frame. The frame specifies the contents and timing of complete communication runs by the BC. Each entry in the frame is either a reference to a message or a special frame symbol. The entire frame is referred to as a major frame and is divided into minor frames each of equal time duration.

Loading message ID handles into a U16BIT array specifies a frame. Each message ID uniquely identifies a message that was previously defined by the function ddcDefMessage. Other elements that can be placed into a frame list are ‘Frame Symbols’. The frame symbols identify special operations that should be performed at that point. For example the symbol ‘END_OF_MINOR’ specifies that the BC must stop message processing until the minor frame time counter expires. Then, once the timer expires, the

counter is reset with the Minor frame time, and the next message in the list will be processed.

Every frame list must have at least one entry of 'END_OF_MAJOR'.

The minor frame time is based on a programmable 32-bit counter with 1 μsec resolution. The ***BU-65572v*** supports major frames of up to 1024 messages per installed channel, with a period of up to 72 minutes.

BC ERROR INJECTION

Error conditions may be injected on a message-by-message basis. The ***BU-65572v*** supports three categories of injected BC Errors: length errors, encoding errors, and gap errors. Length Errors include both word count errors and bit count errors. Word Counts of -32 to +1 words may be programmed. Bit counts of +3, +2, +1, -3, -2, or -1 bit may be programmed on any word within the message.

Encoding errors are implemented though the use of two simple yet powerful mechanisms for modifying the output of the ***BU-65572v***'s Manchester encoder. The two modifying functions are glitch and inverse. A glitch error will force the output of the encoder to an idle bus condition for the specified period of time.

An inverse error will invert the output of the encoder for the specified period of time. The word number, starting time, and width specify the placement of the error. The error may be placed in any word within the message and its starting time may be programmed in 50 nsec increments with a width of up to 3 μsec. This error injection is capable of generating a host of errors including invalid sync patterns, parity errors, and Manchester bi-phase errors.

A gap of 3 to 32 μsec (measured mid-parity crossing to mid-sync crossing) may be inserted between any two words in a message. This allows for a "dead time" gap between words of 1, 2, or 3 μsec.

INSERTING ASYNCHRONOUS MESSAGES

The ***BU-65572v*** allows an asynchronous message to be inserted while the card is running. The inserted message will be executed upon completion of the current message. The user will define all asynchronous messages after the END_OF_MAJOR frame symbol and insert the message into the running frame by calling the insert message routine. The hardware does all of the work.

Once the frame has been defined and the BC is running, asynchronous messages may be inserted at any time by asserting the 'ddcInsertMessage' routine. This routine specifies which 1553 device the operation should be processed by, and the message index in the frame list that should be inserted. The asynchronous message will be inserted immediately following the present message.

It should be noted that if enough messages are inserted into a minor frame, the messages could overrun the minor frame time. In this case, all of the messages will be processed, and the first message of the next minor frame will occur immediately.

BC INTERMESSAGE ROUTINES

Upon completion of a BC message, the ***BU-65572v***'s on-board processor will execute up to 2 intermessage routines. Intermessage routines are used to implement automatic retries on failed messages as well as other "end of message" functions.

Intermessage routines are used to signal the user application that an interrupt has been generated. This can occur at the end of a message for BC operation, when a data table has been accessed in RT operation, or when the Monitor stack is 1/3 full (approximately 2K words).

Another use of intermessage routines is to signal external hardware that a specific event occurred. As messages are being processed by the ***BU-65572v***, discrete signals can be set and cleared at the 37 pin 'D' connector. These discrete signals can be used to synchronize an oscilloscope or other external device.

There are also intermessage routines that will listen at the 'D' connector for inputs that can be used to initiate operations in the ***BU-65572v***.

RESPONSE TIMEOUT

The ***BU-65572v*** BC RT's and MT support programmable response timeout values ranging from 2 to 29 μsecs in 1-μsec increments.

RT Mode

The ***BU-65572v*** can simultaneously simulate the operation of 31 unique remote terminals (RTs) plus a broadcast address for each of the installed channels. The ***BU-65572v*** maintains "last status" and "last command" words allowing for full support of transmit last command and transmit status mode commands. The ***BU-65572v*** supports full RT command illegalization for each transmit or receive message based on RT address and sub-address. In addition, individual mode commands may be illegalized.

RT ERROR INJECTION

Error conditions may be injected on an individual RT/SA basis. The ***BU-65572v*** supports five categories of injected RT errors: length errors, encoding errors, gap errors, status address errors, and response errors. Length errors include both word count errors and bit count errors. Word

counts of -32 to +1 words may be programmed. Bit counts of +3, +2, +1, -3, -2, or -1 bit may be programmed on any word within the message.

Error specifications are attached to the data tables that are mapped to an RT and Sub-address combination. This provides for a large number of possibilities for injecting errors. An application can map more than one data table to any given RT/SA combination. This means that the RT can respond with different errors each time it is accessed.

Encoding errors are implemented though the use of two simple yet powerful mechanisms for modifying the output of the ***BU-65572v***'s Manchester encoder. The two modifying functions are glitch and inverse. A glitch will force the output of the encoder to an idle bus condition for the specified period of time. An inverse will invert the output of the encoder for the specified period of time. The word number, starting time, and width specify the placement of this error. The error may be placed in any word within the message. The starting time is programmed in 500 nsec increments from the beginning of the specified word. The width of the error is specified in 50 nsec increments up to 3 μsec. This error injection scheme lends itself to generating a host of errors including invalid sync patterns, parity errors, and Manchester bi-phase errors.

A gap of 3 to 32 μsec (measured mid parity crossing to mid-sync crossing) may be inserted between any two words in the message. This allows for a "dead time" gap between words of 1, 2, or 3 μsec. A status address error may be injected in which the RT responds with a status word containing an RT address, which does not match the terminal's RT address. The RT may be programmed to respond with any value from zero to 31 in its status response.

The ***BU-65572v*** supports three types of response errors: no response, a late response, or a response on the wrong bus. No response errors may be programmed for a single bus (Bus A or Bus B) or for both buses. Injecting a no response error on one bus provides a simple mechanism for testing bus controller retry conditions. A late response may be programmed in the range of 2 to 30 μsecs in 1 μsec increments.

RT INTERMESSAGE ROUTINES

The RT section of the ***BU-65572v*** also supports intermessage routines. Upon completion of a RT message the ***BU-65572v***'s on-board processor executes two intermessage routines. The data table that was used by the RT for a given message specifies which intermessage routines will be executed.

As with the Bus Controller operation, the RT intermessage routines specify special actions to take place at the end of the current message processing. One of the more common actions that are taken is to signal the application that the hardware completed the message by generating an interrupt to the system. Other actions will cause discretes to be set or cleared and data tables to be swapped. And since each RT / Sub-address can be assigned a block of data tables, each message to the RT can result in different actions being taken.

BC/RT Data Tables

For each of the installed 1553 channels, the ***BU-65572v*** maintains 1024 data tables within the shared RAM. Each data table may be up to 32 words in length. The total memory allocation for all data tables is restricted to 12K words. These data tables are common to both BC and RT. Internal lookup tables map each RT address, T/R, sub-address combination (RT mode) and message number (BC mode) to a chosen data table. Data tables may be read or written to in real time by the user ('ddcReadData' or 'ddcWriteData') and may be either single or double buffered. Double buffering can be used to avoid the memory access contention that occurs when the PC's application and the 1553 bus access data tables simultaneously. The ***BU-65572v*** provides an optional block data mode in which the data table number associated with a given RT message is incremented after completion of the message. The block data mode is implemented as a circular data structure. Each RT command (RT address, T/R, and sub-address) has three data table numbers associated with it: first, last, and current. The current data table number will be incremented after completion of message until the value of 'last' is reached, at which point the current table number will rollover to the value of first. The incrementing of the current data table is accomplished through the use of an intermessage routine.

Monitor Mode

The ***BU-65572v*** contains an independent message monitor for each bus with the ability to filter messages in real time. Monitor selection or filtering is performed through the use of a lookup table based on the RT address, T/R, and sub-address of command words. Monitored messages are stored in the shared RAM on the ***BU-65572v***, which allocates 6K words for the monitor stack. Each entry in the monitor stack contains a header followed by a variable number of data words. Contained with the message header are the receive/transmit command(s), receive/transmit status, message format, Bus (A or B), a capture flag, word count (actual number of words in the message), a detected error field, and a 32-bit time tag (1 μsec resolution).

The transfer of the messages from the card's circular buffer to the host memory/disk is determined by the capture flag, which is set upon detection of a predefined event as specified by the 'ddcCaptureEvent' command. Capture events include immediate, command template match, exception, or trigger. The command template event is based on a 16-bit command word with a 16-bit mask. Exception events may be programmed for any exception: invalid command, invalid data, invalid status, gap preceding data, response time error, wrong RT address error, status set condition or an illegal command. The trigger event uses one of the four monitor input pins on the 37-pin D-type connector as a trigger input.

DMA transfers are possible using the VME/VXI Master Mode. The Monitor mode can autonomously transfer monitored data to host buffer without host CPU intervention. This greatly improves the efficiency of both the host and the ***BU-65572v***.

Interrupts

For each of the installed channels, both the BC/RT and the Monitor may generate interrupts on a common output to the VME/VXI back plane (VME vector). The hardware interrupt vector used by the ***BU-65572v*** is selected by the Plug-and-Play capability of the VME/VXI backplane and BIOS. An important aspect of VME/VXI interrupts is that they are sharable. This means that the ***BU-65572v*** can share an interrupt for all installed channels on the card and all ***BU-65572v*** cards in the computer.

As interrupts are generated, the ***BU-65572v*** device driver will acknowledge the interrupt by clearing the computer hardware and then enter an interrupt vector onto a queue that can contain up to 64 interrupt actions. Each vector on the queue will be sent by the system to the user application. This will only occur when the applications interrupt service routine (ISR) is completed processing all previous interrupts. This action ensures that the user ISR is not interrupted.

DMA INTERRUPT GENERATION

DMA interrupts are generated at the completion of a DMA cycle. After a DMA interrupt occurs the host DMA buffer is checked. If it is more than half full a DMA software interrupt is generated and the data in the host buffer is processed: cleared out.

BC INTERRUPT GENERATION

BC interrupts may be enabled by a global interrupt mask for successful messages, communication errors, status set conditions, or on selected frame symbols (skip, break point, major frame, and minor frame symbols). The criteria for a status set condition are programmed globally through the status mask. The status mask allows any of the 16 bits within the RT status word to be ignored. The status mask affects the generation of interrupts as well as the detected error field that is stored in the message structure.

BC interrupts are issued by the intermessage routines associated with messages allowing for selective interrupt generation on a message-by-message basis. A two-word vector is pushed onto a circular queue for each interrupt request and is transparent to the user. The queue can hold up to 64 interrupt vectors; thus, the host computer is not required to immediately acknowledge the interrupt request.

RT INTERRUPT GENERATION

RT interrupts may be enabled by a global interrupt mask for transmit/receive messages with no message error, mode commands with no message error, transmit/receive messages with the message error bit set, or mode commands with the message error bit set.

RT interrupts are issued by intermessage routines associated with data tables allowing for selective interrupt generation on a message by message basis. A two-word vector is pushed onto a circular queue for each interrupt and is transparent to the user. The queue can hold up to 64 interrupt vectors; thus, the host computer is not required to immediately acknowledge the interrupt request.

MONITOR INTERRUPTS

Monitor interrupts may be generated after each message is received or after one third of the monitor's circular buffer has been filled (approximately 2K words). This allows for either real-time analysis or mass collection/storage of monitored data.

Variable Amplitude Transceiver

The ***BU-65572v*** (only) provides variable amplitude transceivers for each 1553 channel installed on the card. The output of the variable transceiver is software controllable in the range of 0.0 volts to approximately 21.5 volts. This range is covered in 1024 steps. The user application is able to modify this amplitude in real time by calling the 'ddcSetAmp' library function.

The transceiver outputs can be individually controlled for each of the installed channels, while the two transceivers for a given channel will be varied simultaneously. Functions for controlling the transceiver outputs are available in the 'C' library that is provided with the card.

NOTE: *All ground returns are connected to the chassis ground.*

IRIG-B Support

Support for the Inter-Range Instrument Group (IRIG) Standard 200-95 is provided in the ***BU-65572v*** boards. The implementation of this standard into the 1553 Tester/Simulator board enables all messages to be tagged with time-of-day information, allowing accurate correlation between messaging on the 1553 bus and other hardware and software events that are occurring in the system. This is especially useful when trying to identify the cause of a system problem that may be directly related to message data sent over the 1553 bus. The IRIG-B timestamp for each of the installed channels may be individually selected. This allows one channel to use the internal 32-bit Time-Tag clock, while another channel will stamp the messages with the IRIG-B time. The IRIG-B timestamp, if enabled, will be combined with the internal timestamp to provide µsec accuracy.

When IRIG is enabled on the card, the monitor message header will contain two more words than in the previous versions. These two words, which are tacked onto the end of the header, specify the IRIG high and IRIG low words of the timestamp. These two words are shown in Figure 8 and Figure 9. A feature of adding new entries to the header is the ability to maintain the

existing 32-bit internal time tag of the ***BU-65572v***. When this feature is operating, the internal 32-bit time tag is reset to zero each time a new IRIG signal is received (about once per second). This means that the long-term accuracy of the time tags is as good as the IRIG generator in the system.

A three-tap jumper plug (JP1) is provided on the card that can be used to specify the loading termination of the IRIG bus. There are four choices of loading:

- No termination
- 10K ohms
- 600 ohms
- 50 ohms

IRIG-B SPECIFICATIONS

- IRIG receiver
- Rate-scaled serial time code
- 1st word is time-of-year in BCD notation including days, hours, minutes, seconds, and fractions of seconds
- DDC Usage - Mode B, Not using Straight Binary Seconds
- Range = 1 Second to 1 Year
- The initial time 0h 0m 0s January 1 of the present year
- Pulse Code Modulation on 1kHz carrier
- One full Time Code is received every second.

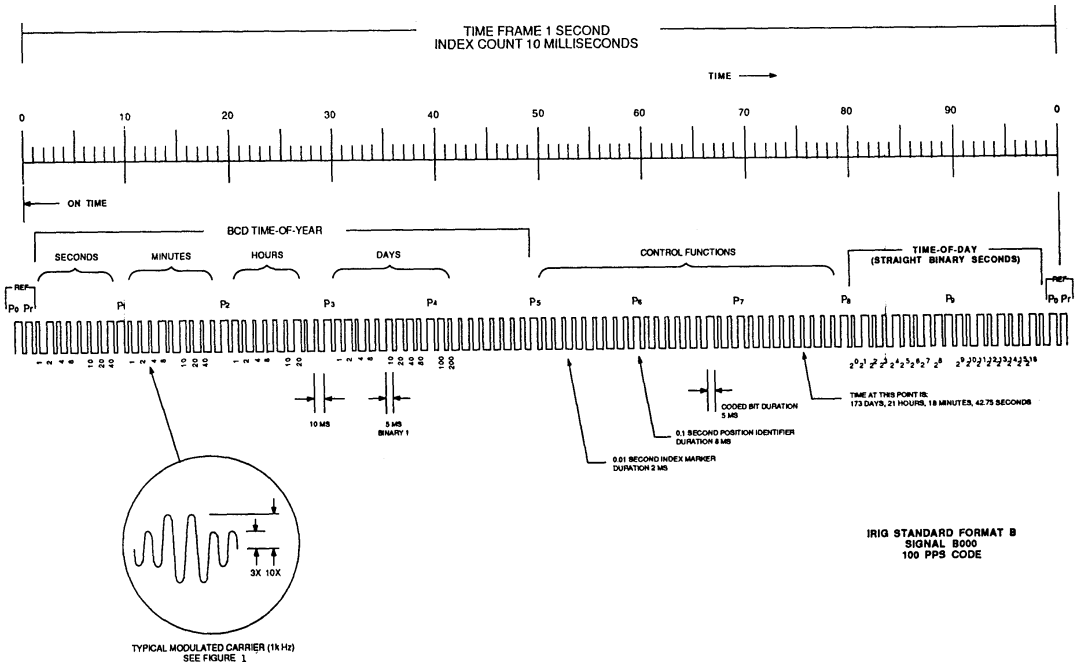


Figure 7 - Sample IRIG Signal Timing

200	100	80	40	20	10	8	4	2	1	20	10	8	4	2	1
Days										Hours					
15															0

Figure 8 - Upper Word Bit Definitions of IRIG

If Bit 14 of the Low Word is High, then the time may not be a valid IRIG time. Both IRIG inputs may not be present, which would cause the time to be automatically incremented based on the clock frequency and may drift over time.

X	FAIL	40	20	10	8	4	2	1	40	20	10	8	4	2	1
N/A	Pass_L	Minutes							Seconds						
15															0

Figure 9 - Low Word Bit Definitions of IRIG

Monitor DMA to Host Buffer

The ***BU-65572v*** is fully compliant to the VME/VXI standards for both Target and Master applications. As a VME/VXI master, the ***BU-65572v*** is capable of performing DMA block data transfers from the monitor buffers on the card to a buffer in the host memory. This will allow the transfer of data without interrupting the host processor, enabling it to perform other more important tasks.

When the application calls the 'ddcEnableDma' routine, the size of the DMA buffer must be specified. The DMA buffer size must be greater than 32K words. If it is not greater than this size, then the routine will return with an error. If the size of the DMA buffer is too large, than the system may not be able to allocate it and again the routine will fail. Since this buffer is dynamically allocated from non-swappable system resources, the DMA buffer size should not be too large. The buffer size can affect system operation if too much memory is requested.

The DMA buffer is not directly accessible to the application. All operations that will be performed on the DMA buffer must be made through the appropriate RLT routines.

Software Control Of Bus Configuration

The ***BU-65572v*** has the capability of being connected to the bus as either Transformer Coupled or Direct Coupled. Transformer coupling enables the card to be connected to the 1553 bus with a long stub of up to 20 feet. Direct coupling requires that the card be connected to the 1553 bus by a stub of no more than 1 foot. The coupling configuration is dynamically configurable via functions provided in the 'C' library. Relays on the board are used to select the correct signal path direct or transformer coupled for each of the installed channels.

The ***BU-65572v*** (only) has the capability of modifying the bus termination to one of three different loads. If the bus termination is set to None, then the effective impedance is 'open'. If the bus is set to Full, then the bus termination will be 37.5 ohms. A setting of half will cause a bus termination of 75.0 ohms. This control makes it quite simple to connect the ***BU-65572v*** directly to another 1553 device without the need of an external load. As with the bus coupling mode, the bus termination mode is dynamically configurable via software functions provided in the 'C' library which control relays for each installed channel.

Discrete I/O

This new Tester/Simulator design includes four discrete outputs per channel. These four outputs are set to logic ‘1’ and cleared to logic ‘0’ by use of eight new intermessage routines. The format of the routine names is SET_DISCRETE_X and RESET_DISCRETE_X. These discrete outputs may be used for signaling external equipment when a specific event or message has occurred. The intermessage routine can be attached to any message, data table, or frame symbol providing a wide variety of debug possibilities.

BC Trig Out is active at the start of a BC frame. When the Tester/Simulator starts a BC cycle, this pin will be strobed to a logic “1” for at least 3 µsec.

Monitor Trigger in waits for a valid logic to be presented at this input. Once the level is validated (true for more than 5 µsec), the monitor will start writing data to the hard drive. The program will call the routine “ddcCaptureEvent()’ with the event parameter (parameter 2) set to CAPTURE_TRIGGER. Parameters 3 and 4 are not used.

Monitor Trigger Out waits for the monitor to trigger and then strobes this pin to a logic “1” for at least 3 µsec. This allows any device that is connected to the monitor output to be signaled when the monitor is active.

BC Trigger In (RT Wait Intermessage routine). If the intermessage routine ‘Wait For Input Trigger’ is active during a message, the BC (or RT) ACE processor will remain in a halt state until the signal on this pin is activated.

APPENDIX A

Figure 10 illustrates the interface of the ***BU-65572v*** card and a MIL-STD-1553 bus using direct coupling. The diagram shows the connections of the four dual-redundant channels on the ***BU-65572v*** connected to a single bus.

The ***BU-65572v*** card has three connectors; two DB9, and one DB37 connector. The two DB9 connectors are used to connect the card to the bus.

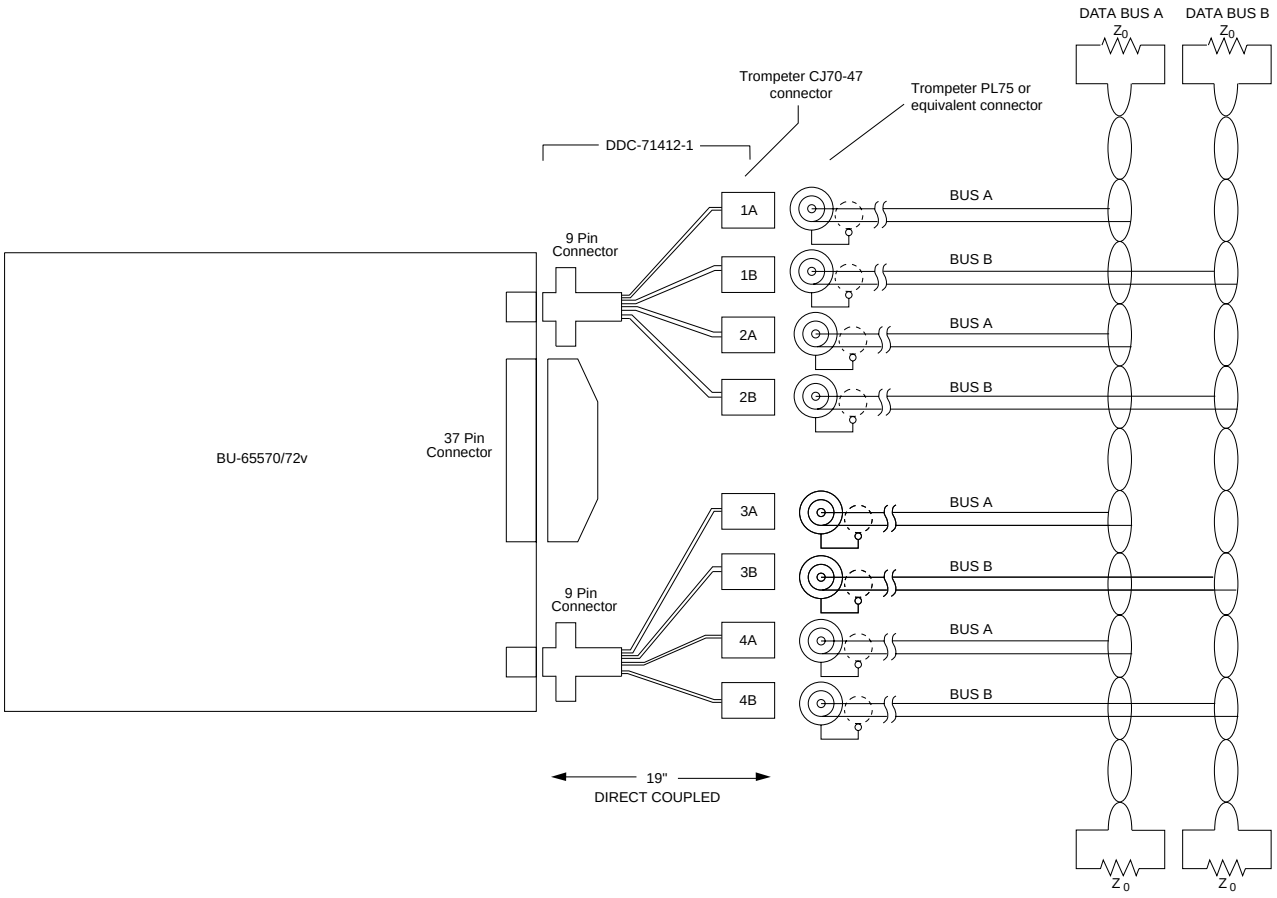


Figure 10 - Bus Configuration – Direct Coupling

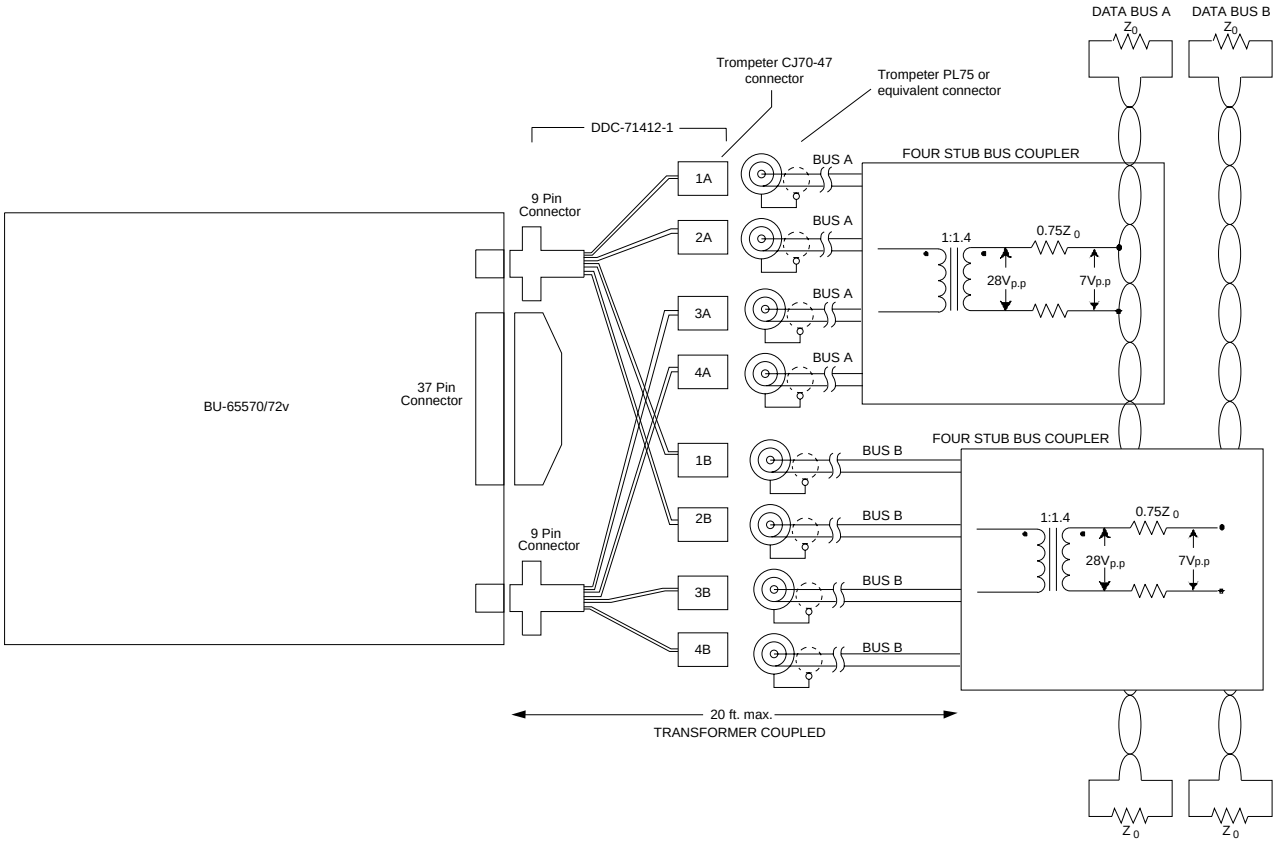


Figure 11 - Bus Configuration – Transformer Coupling

Figure 11 shows a common bus configuration for Transformer Coupling using the ***BU-65572v*** card.

APPENDIX B

Acronyms

ACARS	Aircraft Communication, Addressing and Reporting System
ACMS	Aircraft Condition Monitoring System
ATE	Automated Test Equipment
CGA	Color Graphics Adapter
CMC	Central Maintenance Computer
CMOS	Complementary Metal Oxide Semiconductor
CS	Chip Set
DADC	Digital Air Data Computer
DOS	Disk Operating System
DPRAM	Dual-Port Random Access Memory
EFIS	Electronic Flight Instruments System
EGA	Enhanced Graphics Adapter
EIU	Electronic Interface Unit
EPROM	Erasable Programmable Read Only Memory
FIFO	First In First Out Memory
FLS	Fixed Length Stack
FMC	Flight Management Computer
GND	Ground (electrical)
GUI	Graphical User Interface
I/O	Input/Output
IDT	Integrated Device Technology
IDU	Integrated Display Unit
IRIG	Inter Range Instrument Group
IRS	Inertial Reference Unit
LRU	Line Replaceable Unit
MCDU	Multi-Control Display Unit
MHz	Megahertz
N/A	Not available
PC	Personal Computer
RAM	Random Access Memory
ROM	Read-Only Memory
RX	Receiver
TTL	Transistor-Transistor Logic
TX	Transmitter
UUT	Unit Under Test
VDC	Voltage Direct Current
VGA	Video Graphics Adapter

APPENDIX C

Hardware Characteristics

Table 5 - BU-65570v/72v Hardware Specifications

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATINGS				
+5 V Supply Voltage	-0.3		7.0	V
RECEIVER				
Threshold Voltage, Transformer Coupled, Measured on Stub		0.56		V_{P-P}
TRANSMITTER				
Differential Output Voltage – Transformer Coupled, Measured on Stub				
• BU-65570V	18	20	27	V_{P-P}
• BU-65572V				
- Minimum Programmable Voltage		0		V_{P-P}
- Maximum Programmable Voltage (programmable in 1024 steps)		21.5		V_{P-P}
POWER SUPPLY REQUIREMENTS Per 1553 Bus				
Voltages/Tolerances				
• + 5 V	4.5		5.5	V
Current Drain @ + 5.0 V				
Idle	220		240	mA
50% Duty Cycle	720		800	mA
100% Duty Cycle (See Note 1)	870		1000	mA
1553 MESSAGE TIMING				
RT Response Time (See Note 2)	4		7	µsec
BC Intermessage Gap (See Note 3)	25			µsec
BC/RT/MT Response Timeout (See Note 4)	2		29	µsec
Transmitter Watchdog Timeout		668		µsec
MT Minimum gap for capture	4			µsec
THERMAL				
BU-65570V/72V				
Operating Temperature	0		+55	°C
Storage Temperature	-40		+85	°C
PHYSICAL CHARACTERISTICS				
Size “B”	6.3(H) x 9.2(W) (160 x 223.7)			in (mm)
Weight	20.0 (567)			oz (gm)

NOTES:

1. (100% Duty Cycle at MAX Transmit Amplitude [27 V_{PP}])
2. This time assumes that this card is not emulating BC.
3. This hardware time is enforced by the firmware. If an attempt to reduce this time is made, the time will be stretched to 25 µsec.
4. This time is programmable from 2 µsec to 29 µsec in 1 µsec increments

INDEX