ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Find the *DDC BU-66318G0-110 and BU-61864G3-100* at our website: *Click HERE*

BU-66318
ACE-BRIDGE

Make sure the next Card you purchase has...

DDC on Board®



FEATURES

- PCI to Local Bus Bridge
- Local Bus Compatible with ACE, Mini-ACE, Enhanced Mini-ACE, Micro-ACE and Mini-ACE Mark3 Series Generations
- PCI Bus Interface Connects up to Six DDC 1553 Terminals with no Glue Logic
- Full Military Temperature Range
- Fully Compliant PCI Revision 2.2 Specifications
- 3.3V PCI Logic
- Supports Optional Local Microprocessor and Shared RAM
- 32 Deep Double Word Wide PCI Write FIFO
- Interrupt Support
- 1.1" X 1.1" 208 Pin Flat Pack Design (LQFP)

DESCRIPTION

The BU-66318 ACE-Bridge provides a simple, complete and tested solution for interfacing any of DDC's ACE series (including the ACE, Mini-ACE™, Enhanced Mini-ACE, Micro-ACE and Mini-ACE Mark3 series) MIL-STD-1553 terminals to a PCI bus.

The ACE-Bridge connects directly to any 3.3 volt PCI bus as a Target Device. With its interrupt support and a 32 deep by 32-bit wide FIFO allowing for burst write transfers, the BU-66318 can significantly reduce system overhead by utilizing the efficiency of the PCI bus.

The BU-66318 may be connected to up to six ACE series MIL-STD-1553 terminals directly without any "glue logic."

Utilizing a SELECT and STROBE handshake method, the BU-66318 accesses all of its MIL-STD-1553 terminals RAM and Registers through a 16 bit Address / Data bus.

Support for an optional local microprocessor is included in the ACE-Bridge. If a local microprocessor is added, the BU-66318 uses a DMA type handshake method to arbitrate for the local bus. A shared RAM interface is also included.

DDC® ©Data Device Corporation

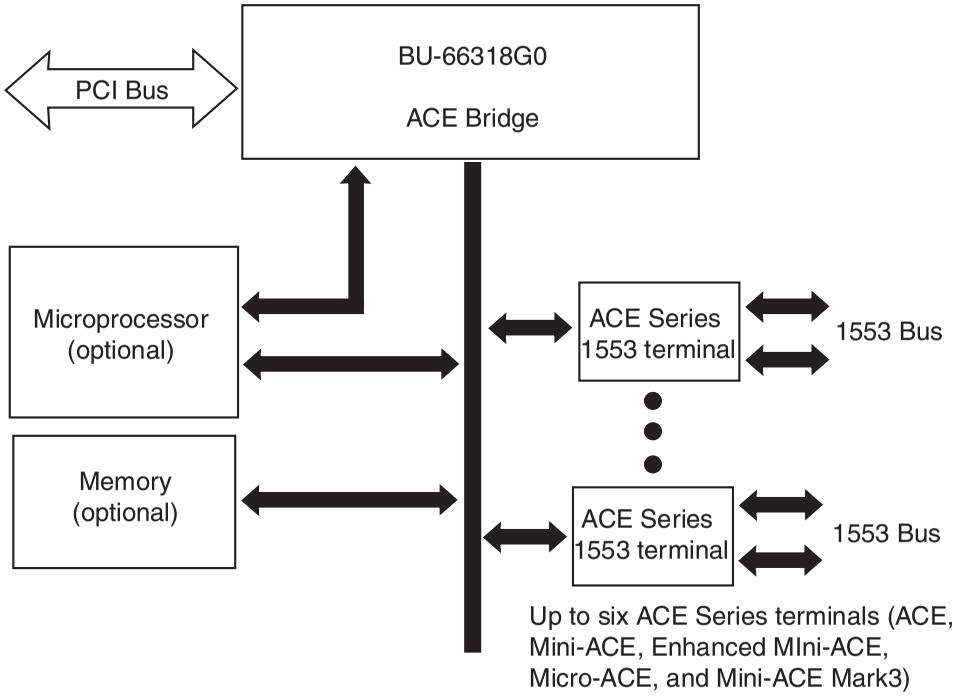
Data Device Corporation
105 Wilbur Place
Bohemia, New York 11716
631-567-5600 Fax: 631-567-7358
www.ddc-web.com

FOR MORE INFORMATION CONTACT:

Technical Support:
1-800-DDC-5757 ext. 7771

All trademarks are the property of their respective owners.

© 2004 Data Device Corporation



Note: The ACE Bridge supports from one to six 1553 terminals.

FIGURE 1. ACE-BRIDGE SYSTEM BLOCK DIAGRAM WITH OPTIONAL PROCESSOR

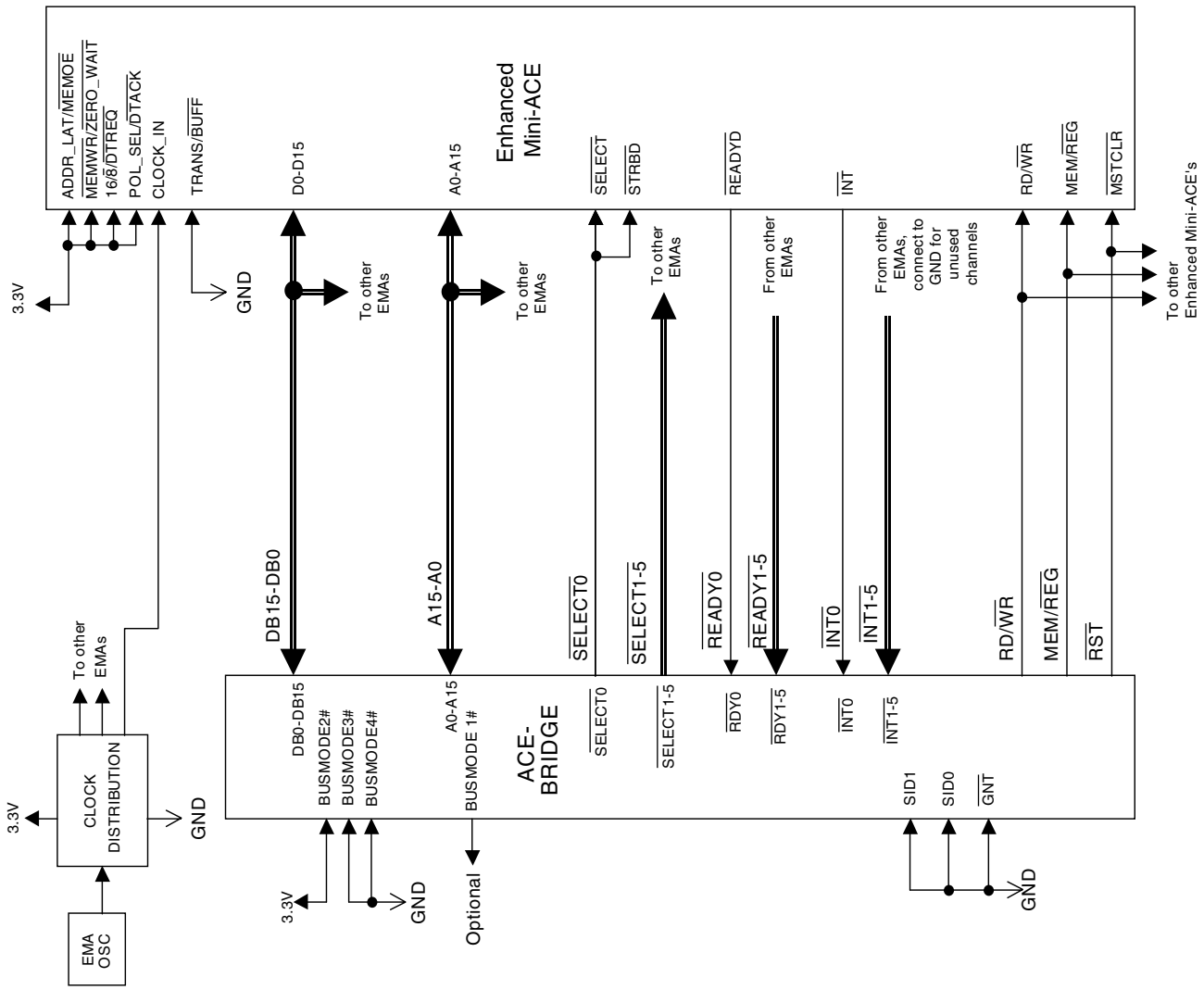


FIGURE 2. "NON-INTELLIGENT" APPLICATION

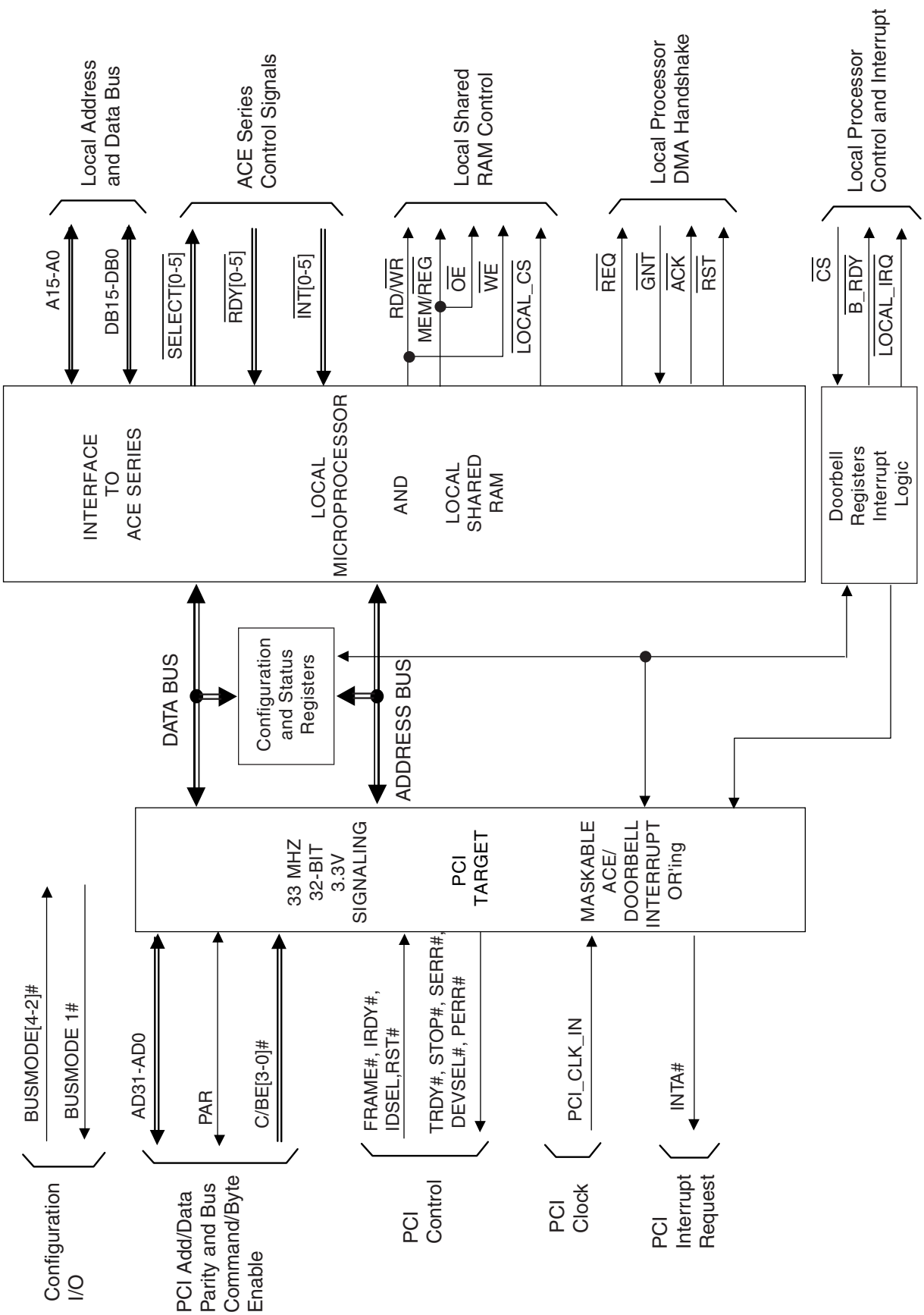


FIGURE 3. ACE-BRIDGE DIAGRAM

TABLE 1. BU-66318 SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATINGS				
Vcc Supply Voltage	-0.3	3.3	4.0	V
Logic				
PCI voltage Input Range (see PCI spec for AC)	-0.3		Vcc +0.3	V
Local bus voltage input range (5V tolerant)	-0.3		6.0	V
LOGIC				
V_{IH} All signals except PCI, Factory Test, SID0, SID1	2.1			V
V_{IL} All signals except PCI, Factory Test, SID0, SID1			0.7	V
$V_{HYSTERESIS}$ All signals except PCI, Factory Test, SID0, SID1		0.4		V
V_{IH} Signals Factory Test, SID0, SID1	0.8•V_{CC}			V
V_{IL} Signals Factory Test, SID0, SID1			0.2•V_{CC}	V
$V_{HYSTERESIS}$ Signals Factory Test, SID0, SID1		0.8		V
I_{IH} (V_{CC}=3.6V, V_{IN}=V_{CC}) All signals except PCI	-1		+1	µA
I_{IL} (V_{CC}=3.6V, V_{IN}=0.0V) All signals except PCI	-25		-91	µA
V_{OH} (V_{CC}=3.0V, I_{OH}=max) All signals except PCI	2.4			V
V_{OL} (V_{CC}=3.0V, I_{OL}=max) All signals except PCI			0.4	V
I_{OL} All signals except PCI	7.35			mA
I_{OH} All signals except PCI			-7.35	mA
C_I (Input Capacitance)			12	pf
PCI LOGIC: see PCI spec 3.3V signaling environment spec				
C_{IO} (Bi-directional signal Input Capacitance)			12	pf
PCI pin capacitance		7	12	pf
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
+3.3 V	3.0	3.3	3.6	V
Current Drain				
+3.3 V			40	mA
POWER DISSIPATION				
BU-66318			132	mW
THERMAL				
Thermal Resistance, Junction-to-ambient (θ_{JA})			20	°C/W
Operating Junction Temperature (Note 1)	-55		+125	°C
Storage Temperature	-65		+150	°C
Lead Temperature (soldering, 10 seconds)			300	°C
PHYSICAL CHARACTERISTICS				
Moisture Sensitivity Level		MSL-3		-
Body Size		1.1 X 1.1 X 0.063		in
		(28 X 28 X 1.4)		(mm)
Weight		0.1(3.5)		oz (g)

TABLE 1 NOTES:
(1) This device is only tested at -40°C to +125°C, but is guaranteed at -55°C to +125°C.

INTRODUCTION

The BU-66318 ACE-Bridge comprises a complete integrated interface between a PCI bus and up to six Enhanced Mini-ACE, Mini-ACE, Mini-ACE Mark3, or Micro-ACE series MIL-STD-1553 terminals. Note that the term "ACE" is used extensively in this document and can apply to any of the four generations of part series, unless a specific part series is mentioned, such as the Enhanced Mini-ACE series. The BU-66318 also includes an interface between the PCI bus and a local microprocessor and shared RAM. The local processor/RAM interface does not have to be used and can be disabled easily. The BU-66318 may be used to configure one to six MIL-STD-1553 terminals.

The ACE-Bridge is a fully compliant target agent, as defined by the PCI Local Bus Specification Revision 2.2, using a 32 bit interface that operates at clock speeds of up to 33 Mhz, from a 3.3V signaling bus. It supports both PCI and Local CPU / ACE interrupts and contains a 32 deep, double word wide FIFO that handles PCI burst write transfer cycles. The BU-66318 comes packaged in a low profile 208 pin 1.1 square inch package.

The BU-66318 contains only a single set of configuration registers so that all of the ACE hybrid memory and register space may be addressed through a single PCI function. Internal registers keep track of how many ACE devices are connected to the local bus, indicate if a local CPU is present, control the Subsystem Vendor and Device ID, enable/disable interrupts, and control the Fail-Safe operation of the device. There is also a 32-bit register available for general purpose use.

There are three Base Address Registers utilized to implement ACE memory space (BAR0), register space (BAR1), and local RAM space (BAR2). Base Address Register mapping is contained in PCI configuration register space.

For designs without a local bus processor, the register function/mapping presented to driver software is very similar to that provided by DDC's Enhanced Mini-ACE based PCI cards (BU-65569i, for example), so that drivers for these cards can be used with very little or no modification. The Enhanced Mini-ACE register and memory mapping is the same as that in the BU-65569i. The PCI-ACE interface control registers in the BAR1800-81Ch space are a superset of the BU-65569i and contain extra interrupt enable bits.

The ACE register mapping is located in PCI memory space, allowing for full PCI access to all 1553 terminals. Although the BU-66318 can be accessed in 32-bit words, all ACE registers are internally accessed in 16 bit word reads / writes. If a 32-bit read is performed from the PCI bus in ACE register space the lower word contains the ACE register and the upper word is all zeroes. ACE memory is also accessed internally in 16-bit words, but memory is accessed sequentially allowing for 32-bits of data to be read from the PCI bus. In other words, if a 32-bit PCI read is performed the first 16 bits of data would be read from the requested address, the next 16 bits of data would be read from the initial ACE memory address + 1. The BU-66318 supports 32-bit and 16-bit read and write operations only, 8-bit writes are illegal, and 8-bit reads will return 16-bit data.

NUMBER OF ACE CHANNELS

An internal register keeps track of how many ACE devices are attached to the BU-66318, along with whether a local microprocessor is present. The ACE's are detected by the use of the INT (interrupt) signals. If an interrupt line is tied low on power-up that channel is defined as not populated. When a PCI reset signal occurs (RST#), a Master Clear is issued to all ACE devices. The BU-66318 will then poll all six ACE interrupt inputs and record their status. All unused INT signals should be grounded so as to indicate channel population.

LOCAL MICROPROCESSOR

The local microprocessor is detected via the $\overline{\text{GNT}}$ signal. When a PCI reset signal occurs (RST#), the BU-66318 will poll the $\overline{\text{GNT}}$ signal. If the $\overline{\text{GNT}}$ signal is tied low on power-up, the BU-66318 determines no processor to be present. It is very important to note that whether a local CPU is found or not will control if the local bus signals are to be tri-stated.

LOCAL BUS INTERFACE

A local bus interface is available on the ACE-Bridge device. When the local bus interface is not used, the user must tie the $\overline{\text{GNT}}$ input signal low in order to bypass the local bus mode. When the local bus interface is used, the MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$, ADDRESS, DATA and SELECT buses will be tri-stated unless the bus is granted to the Bolt-On-PCI device. The bus will be granted when the ACE-Bridge receives a $\overline{\text{GNT}}$ back. The bus will remain in control of the ACE-Bridge device until $\overline{\text{ACK}}$ and $\overline{\text{GNT}}$ both go high. The $\overline{\text{ACK}}$ signal will be asserted low when the Bolt-On-PCI device has control of the bus signals. If the local bus interface is not used all control signals are two-state, not tri-state.

In addition, the ACE-Bridge provides the local bus signals, $\overline{\text{CS}}$ and $\overline{\text{B_RDY}}$, to the local processor to allow read/write access by the local processor to the ACE-Bridge internal registers.

INTERRUPTS

PCI Interrupts are generated on the INTA# output signal to the host bus. The interrupts from each ACE and local CPU, if used, are functionally or'd together to provide a single interrupt. ACE hybrids should be programmed to generate level mode interrupts to the ACE-Bridge. Interrupts may be sent through the PCI bus to the local bus processor (if present) by the use of the "Interrupt Vector From PCI" control register contained in BAR1. Writing to this location from the PCI bus causes a local CPU interrupt. A read from this location by the local CPU will clear the register.

TABLE 2. BU-66318 CONFIGURATION REGISTER SPACE				
ADDRESS	**31 24**	**23 16**	**15 8**	**7 0**
00h	Device ID(0401h)		Vendor ID(4DDCh)	
04h	Status Register		Command Register	
08h	Class Code = 078000 h			Rev ID = 02
0Ch	BIST(not implemented)(00h)	Header Type(00h)	Latency Timer,Not Used (00h)	Cache Line SizeNot Used (00h)
10h	Base Address Register 0 (for ACE memory)			
	R/W	R/W and 0's, see text	00h	00h
14h	Base Address Register 1 (for ACE registers)			
	R/W	R/W	R/W and 0's, see text	00h
18h	Base Address Register 2 (for local RAM) 128K byte window			
1Ch-24h	Base Address Registers 3 through 5 (not used) 00000000h			
28h	Card Bus CIS pointer (not used) 00000000h			
2Ch	Subsystem Device and Subsystem Vendor IDUser configurable (see text)			
30h	Expansion ROM Base Address (Not Used, bit 0 = 0)			
34h-38h	Reserved(0000h)			
3Ch	Max Lat. 00h	Min Gnt 00h	Interrupt Pin 01h	Interrupt Line R/W

REGISTER AND MEMORY ADDRESSING

The BU-66318 ACE-Bridge contains a set of "Type 00h" PCI configuration registers that are used to map the device into the host system. The PCI configuration register space is mapped in accordance with PCI revision 2.2 specifications.

PCI COMMAND REGISTER

TABLE 3. PCI COMMAND REGISTER	
BIT	**DESCRIPTION**
15:10	Reserved, 0s
9	0
8	SERR# Enable
7	0
6	Parity Error Control
5:2	0
1	Memory Space
0 (LSB)	0

Reserved: These bits are read-only and return zeroes when read.

SERR# Enable: This is an enable bit for the SERR# driver. A value of 0b disables the driver. A value of 1b enables the driver. The value after RST# is 0b.

Parity Error Control: This bit controls the device's response to parity errors. When the bit is 1b, the device will take its normal action when a parity error is detected. When this bit is 0b, the device will ignore any parity errors that it detects and continue normal operation. The value after RST# is 0b.

Memory Space: This bit controls the device's response to memory space accesses. A value of 0b disables the device response. A value of 1b allows the device to respond to memory space accesses. The value after RST# is 0b.

PCI STATUS REGISTER

This register records status information for PCI bus related events. Reads to this register behave normally, but writes can only reset bits. A bit is reset whenever the register is written and the data in the corresponding bit location is a 1.

TABLE 4. PCI STATUS REGISTER	
BIT	**DESCRIPTION**
31	Detected Parity Error
30	Signaled System Error
29:28	0
27	Signaled Target Abort
26:25	DEVSEL# Timing = 01 (medium)
24	0
23	Fast Back-to-Back Capable = 1
22:21	0
20:16	Reserved, 0s

Detected Parity Error: The device will set this bit whenever it detects a parity error, even if the Parity Error Control bit in the PCI Control register is 0b.

Signaled System Error: This bit indicates when the device has asserted SERR#. The value after RST# is 0b.

Signaled Target Abort: This bit is set whenever the device terminates a transaction with a Target-Abort. The value after RST# is 0b.

DEVSEL# Timing: The ACE-Bridge is 01b, medium.

Fast Back-to-Back Capable: This bit is set to 1b and indicates that the device is capable of accepting fast back-to-back transactions.

Reserved: These bits are read-only and return zeroes when read.

This data sheet describes only the PCI registers that are specific to configuring the BU-66318 for interfacing to local ACE terminals, a local microprocessor, and the shared RAM. For specifics or definitions on other PCI bus configuration registers, please see the PCI Local Bus specification revision 2.2.

The **Vendor ID** field contains the vendor's ID configuration register. Data Device Corporation's ID code is 4DDCh.

The **Device ID** field is used to indicate the device being used. This field will contain a value of 0401h.

The **Subsystem Vendor ID** field is a programmable register that contains the Subsystem Vendor ID information.

The **Subsystem Device ID** field is a programmable register that contains the Subsystem Device ID.

The Subsystem Vendor ID and the Subsystem Device ID fields are configured via two Subsystem ID pins (SID0 and SID1). The use of these two signals will allow for four programming options.

TABLE 5. SUBSYSTEM VENDOR AND SUBSYSTEM DEVICE ID SOURCE

SID 0	SID 0	DESCRIPTION
0	0	Subsystem Vendor and Device ID's default to the same as the System ID's
0	1	Subsystem Vendor and Device ID's are loaded by the local processor within 2^{25} PCI clocks after RESET is de-asserted.
1	0	Subsystem Vendor and Device ID's are read by the BU-66318 from an external RAM or registers. Subsystem Vendor ID will be read from address 0000h and Subsystem Device id will be read from address 0001h.
1	1	Subsystem Vendor and Device ID's are read by the BU-66318 from an external RAM or registers. Subsystem Vendor ID will be read from address FFFFh and Subsystem Device id will be read from address FFFEh.

Base Address Registers are used to implement ACE memory space (BAR0), ACE register and ACE-PCI interface control register space (BAR1), and local RAM space (BAR2). Base Address Registers 3 through 5 are not used.

BAR0 is used to access ACE memory space. Each ACE is allotted a maximum of 128K bytes (64K words) for its memory space:

TABLE 6. BAR0 READBACK VALUE (AFTER ALL FS ARE WRITTEN TO BAR0)

# OF ACES	BAR0 READBACK VALUE
1	FFFE0000
2	FFFC0000
3	FFF80000
4	FFF80000
5	FFF00000
6	FFF00000

The lower 4 bits being 0 indicate that BAR0 is memory space, the address decoder is 32 bits wide and the memory is non-prefetchable.

TABLE 7. (BAR0) ACE MEMORY MAP

ADDRESS OFFSET	DEFINTITION
00000 - 1FFFC	ACE 1 Memory Space
20000 - 3FFFC	ACE 2 Memory Space (if available)
40000 - 5FFFC	ACE 3 Memory Space (if available)
60000 - 7FFFC	ACE 4 Memory Space (if available)
80000 - 9FFFC	ACE 5 Memory Space (if available)
A0000 - BFFFC	ACE 6 Memory Space (if available)

Not all locations may be applicable, if an ACE device is not present (Target Abort) or the ACE does not contain 64K words. Target aborts will result when accesses are made to:

ACE 4 when only 3 ACES are present

ACE 6 when only 5 ACES are present

Because ACE memory cannot meet PCI bus latency requirements directly, the BAR0 memory space is read via "delayed read requests" and the FIFO is used for writes.

BAR1 is used to access ACE register locations (BAR1 offset 000h-5FCh) and the ACE-PCI interface control registers (offset 800h-81Ch). BAR1 will read back as FFFFF000h after all ONEs are written to it. The lower 4 bits being 0 indicate that BAR1 is memory space, the address decoder is 32 bits wide and the memory is non-prefetchable.

For typical non-local bus processor applications the only PCI-ACE interface control registers (BAR1 + 800-81Ch) that must be accessed by driver software are the first two registers. These registers contain the following critical functions: the 800h register indicates how many ACEs are present and which ACEs are interrupting and the 804h register enables interrupts for specific ACEs. For typical applications, the other registers or other bits within the 800 and 804 registers can be left at their default values.

Because ACE registers cannot meet PCI bus latency requirements directly, the BAR1 ACE register space (BAR1 000-5FCh) is read via "delayed read requests" and the FIFO is used for writes.

The "ACE-PCI interface control registers" (BAR1 800-81Ch) are part of the PCI interface portion of the die and are written and read directly from the PCI bus, without use of the write FIFO or delayed read request logic.

ACE REGISTER SPACE (ACE1 - ACE6): This address space allows access to ACE registers. Each 252-byte segment of allocated address space allows access to a total of 64 ACE registers per segment. Register access is on a 32-bit boundary (E.G. BAR1 + 000 = ACE1 REG 0, BAR1 + 004 = ACE 1 REG 1, BAR1 + 008 = ACE 1 REG 2, etc).

TABLE 8. (BAR1) ACE/ CONTROL REGISTERS - 4K BYTE TOTAL SPACE

ADDRESS OFFSET	NAME	TYPE	BITS	DEFINITION / ACCESSIBILITY
000-0FC	ACE1		15-0	ACE 1 REGISTER SPACE Register Accesses are on a 32-bit boundary. Last 2 bits of PCI address dropped to form ACE Address.
100-1FC	ACE2		31-16	0
			15-0	ACE 2 Register Space (if ACE 2 present)
200-2FC	ACE3		31-16	0
			15-0	ACE 3 Register Space (if ACE 3 present)
300-3FC	ACE4		31-16	0
			15-0	ACE 4 Register Space (if ACE 4 present)
400-4FC	ACE5		31-16	0
			15-0	ACE 5 Register Space (if ACE 5 present)
500-5FC	ACE6		31-16	0
			15-0	ACE 6 Register Space (if ACE 6 present)
				Note: If an access is attempted in an ACE REGISTER space where the ACE is not present, the access will be terminated with a target abort.
ACE-PCI INTERFACE CONTROL REGISTERS				
800	REG0	R	31-0	GLOBAL ACTIVITY
804	REG1	R/W	31-0	FAIL-SAFE OPERATION / INTERRUPT
808	REG2	R	31-0	FAIL-SAFE TIMER
80C	REG3	R/W	31-0	FAIL-SAFE TIMER VALUE
810	REG4	R	31-0	DISCARD TIMER
814	REG5	R/W	31-0	DISCARD TIMER VALUE
818	REG6	R/W	31-0	RESERVED
81C	REG7	W	31-0	TIMER CONTROL / INTERRUPT

TABLE 9. REG0 GLOBAL ACTIVITY REGISTER REG0 GLOBAL ACTIVITY REGISTER (READ 800H)	
BIT	**DESCRIPTION**
31 (MSB)	PCI INTERRUPT ACTIVE
30	FIFO NOT EMPTY
29	0
28	LOCAL CPU PRESENT
27	0
26	NUMBER OF ACE'S PRESENT - BIT 2 (MSB)
25	NUMBER OF ACE'S PRESENT - BIT 1
24	NUMBER OF ACE'S PRESENT - BIT 0 (LSB)
23	BAR1 DRR DATA DISCARD
22	FAIL-SAFE ERROR
21	ACE 6 INTERRUPT ACTIVE
20	ACE 5 INTERRUPT ACTIVE
19	ACE 4 INTERRUPT ACTIVE
18	ACE 3 INTERRUPT ACTIVE
17	ACE 2 INTERRUPT ACTIVE
16	ACE 1 INTERRUPT ACTIVE
15	INTERRUPT VECTOR TO PCI - BIT 15 (MSB)
•	
•	
•	
0	INTERRUPT VECTOR TO PCI - BIT 0 (LSB)

PCI INTERRUPT ACTIVE: Active HIGH

FIFO NOT EMPTY: When set to '1', indicates that the write FIFO is not empty. The Write FIFO being not empty impacts the latency of PCI BAR0 and BAR1 ACE register read operations. See "PCI read of ACE memory/registers" section for more information.

LOCAL CPU PRESENT: This bit reflects whether the BU-66318 detected a local CPU during initialization. The BU-66318 polls its $\overline{\text{GNT}}$ input signal for a ground condition following power-up. If the $\overline{\text{GNT}}$ signal is found to be LOW during power-up, this bit will be defined as "no local CPU present" and will be set to a value of zero.

When a CPU is found the Local Bus Mode is enabled and the BU-66318 will arbitrate for the local bus whenever access is required. In Local Bus Mode, when the BU-66318 is not in control of the local bus, all of its control signals will be tri-stated.

NUMBER OF ACE'S PRESENT: Bits 26 (MSB) to 24 (LSB) provide a binary representation of the number of ACE terminals presently installed and operating. The BU-66318 supports up to six ACE terminals and may be configured for 1, 2, 3, 4, 5 or 6 ACE devices.

BAR1 DRR DATA DISCARD: If the data discard timer times out while waiting for a retry on a BAR1 access, this bit will be set. If BAR1 read is discarded, it may have caused an action (for example clearing an ACE interrupt) that has not been recognized by the PCI MASTER.

FAIL-SAFE ERROR: If not in FAIL-SAFE OFF mode and fail-safe error occurs (local CPU or ACE does not respond), this bit will be set.

ACE INTERRUPT ACTIVE: Bits 21 to 16 reflect the status of the $\overline{\text{INT5}}$ to $\overline{\text{INT0}}$ signal inputs (respectively). The signals $\overline{\text{INT5}}$ to $\overline{\text{INT0}}$ also represent the state of the ACE6 to ACE1 interrupt output signals (respectively). All ACE interrupts must be programmed for level operation. When an ACE interrupt signal occurs, the corresponding ACE INTERRUPT ACTIVE bit gets set to a ONE. Bits 21 to 16 are cleared when the ACE clears its interrupt request line.

Any unused ACE channel should have the corresponding $\overline{\text{INT[5:0]}}$ input grounded.

INTERRUPT VECTOR TO PCI: Writing to this location by the local processor causes a PCI interrupt if at least one of the bits (15-0) is a '1'. Reading this location from the PCI bus clears the register. This register can be read by local processor to see if PCI master has read it yet and will not cause it to clear.

Subsequent writes occurring to this register by the local processor prior to a PCI Master read can set new bits in the register. Any bits previously set cannot be cleared by new writes. A PCI Master read can only clear bits in this register.

TABLE 10. REG1 FAIL-SAFE OPERATION/INTERRUPT REGISTER (READ/WRITE 804H)	
BIT	**DESCRIPTION**
31 (MSB)	DRR HOLD
30	VECTOR IRQ DISABLE
29	SETUP DELAY FOR LOCAL BUS - BIT 1 (MSB)
28	SETUP DELAY FOR LOCAL BUS - BIT 0 (LSB)
27	LOCAL PROCESSOR INTERRUPT ENABLE
26	ACE6 INTERRUPT ENABLE
25	ACE5 INTERRUPT ENABLE
24	ACE4 INTERRUPT ENABLE
23	ACE3 INTERRUPT ENABLE
22	ACE2 INTERRUPT ENABLE
21	ACE1 INTERRUPT ENABLE
20	BAR1 DRR DATA DISCARD INTERRUPT ENABLE
19	FAILSAFE INTERRUPT ENABLE
18	FAILSAFE INTERRUPT AUTOCLEAR ENABLE
17	FAILSAFE MODE - BIT 1 (MSB)
16	FAILSAFE MODE - BIT 0 (LSB)
15	INTERRUPT VECTOR FROM PCI - BIT 15 (MSB)
•	
•	
•	
0	INTERRUPT VECTOR FROM PCI - BIT 0 (LSB)

DRR HOLD: Default is '0'. When = '0', delayed read request is discarded if ACE-Bridge has obtained requested data and a different transaction is requested. When = '1', delayed read request is held until master repeats original request or timeout occurs.

VECTOR IRQ DISABLE: Default is '0'. When VECTOR IRQ DISABLE = '0', the 16 bits of interrupt field act as a vector - that is, all 16 bits are written to '0' or '1' corresponding to the input data of the current write operation. When VECTOR IRQ DISABLE = '1', the interrupt no longer acts as a vector. Once a bit in the 16 bit interrupt field is set to '1', it cannot be written back to '0'. The interrupt recipient clears bits only upon a read.

SETUP DELAY FOR LOCAL BUS: Data setup delay (TABLE 11) is expressed in the number of clock cycles prior to control signal.

The Control signal = strobe for an ACE write or

$\overline{CS}$ for a BAR2 RAM write or

$\overline{B_RDY}$ for a local processor read

(In all 3 cases, data is driven by the ACE-Bridge onto the local data bus.)

Note: X will vary depending upon the type of transfer (ACE write, RAM write, local proc read), whether data is changing from the last transfer, and whether transfer is an upper word or lower word transfer.

TABLE 11. SETUP DELAY

BIT 29	BIT 28	SETUP DELAY
0	0	0 (default) Data Setup = X clocks
0	1	1 Data Setup = X + 1 clocks
1	0	2 Data Setup = X + 2 clocks
1	1	3 Data Setup = X + 3 clocks

LOCAL PROCESSOR INTERRUPT ENABLE: Enables PCI interrupt if any of the local_irq_vec bits are set [reg0, 15:0]

ACE INTERRUPT ENABLE: These bits must set for any ACEs that are present that need to generate PCI interrupts, in addition to enabling the appropriate interrupts in the ACEs themselves.

BAR1 DRR DATA DISCARD INTERRUPT ENABLE: Enables interrupt to occur on a BAR1 delayed read timeout.

FAILSAFE INTERRUPT ENABLE: When set to a 1, an interrupt is generated if not in FAILSAFE OFF mode and a FAILSAFE error is detected.

FAILSAFE INTERRUPT AUTOCLEAR ENABLE: If set, causes interrupt and the Failsafe Error bit (REG0-bit 22) to be cleared whenever upper word of REG0 is read by the PCI MASTER.

FAILSAFE MODE: Failsafe Errors occur when either an ACE or the Local Processor fail to assert a hand-shake signal (e.g. ACE Ready or Bus Grant) within 1 millisecond (programmable) of when the Strobe or Request signal is asserted. If a failsafe error occurs in any failsafe mode except FAILSAFE OFF, an interrupt will be generated only if the FAILSAFE INTERRUPT ENABLE has been previously set, and the FAILSAFE ERROR bit in REG0 will be set whether the FAILSAFE INTERRUPT ENABLE has been set or not. In FAILSAFE OFF mode, a FAILSAFE interrupt will not occur (even if it has been enabled) and the FAILSAFE ERROR bit will not be set. There are four possible FAILSAFE Modes. They are shown in TABLE 12.

TABLE 12. FAILSAFE MODE

BIT 17	BIT 16	FAILSAFE MODE
0	0	OFF
0	1	RETRY
1	0	HALT
1	1	SKIP

00-FAILSAFE OFF: The ACE-Bridge will wait indefinitely for the transaction to complete. The local bus could hang as a result. The ACE-Bridge will load any subsequent writes into an internal FIFO and respond normally on the PCI bus until it is full. Then it will respond with PCI retries. If Bus Grant or ACE READY finally occurs, the initial transfer and all transfers pending in the FIFO will be completed.

01-FAILSAFE RETRY: The ACE-Bridge will retry the transfer on the local bus when the FAILSAFE timer times out. When Bus Grant or ACE READY occurs, the retried request is completed along with any pending requests in the FIFO.

10-FAILSAFE HALT: Once the FAILSAFE timer times out, all future PCI transfers will be terminated with a target abort until the PCI master clears the interrupt. When local bus access is granted, it will complete the first request only, since no subsequent requests are loaded into the FIFO.

11-FAILSAFE SKIP: Once the FAILSAFE timer times out, the current transaction is discarded or skipped and the next transaction, whether a stored write in the FIFO or a new transaction, will be attempted. ACE-Bridge will keep skipping down through the FIFO entries every time the timer times out and restarts.

INTERRUPT VECTOR FROM PCI: Writing to this location by the PCI Master causes a local processor interrupt only if at least one of the bits (15-0) is a '1'. Reading this location by the local processor clears the register. The PCI Master may read back

this register to determine if the local processor has read it yet and will not cause it to clear.

Subsequent writes occurring to this register by the PCI Master prior to a local processor read can set new bits in the register. Any bits previously set cannot be cleared by new writes. A local processor read can only clear bits in this register.

TABLE 13. REG2 FAIL-SAFE TIMER REGISTER (READ 808H)

BIT	DESCRIPTION
31 (MSB)	0
•	•
•	•
•	•
16	0
15	FAIL-SAFE TIMER COUNT - BIT 15 (MSB)
•	•
•	•
•	•
0 (LSB)	FAIL-SAFE TIMER COUNT - BIT 0 (LSB)

FAIL-SAFE TIMER COUNT: Read this register to obtain the current value of the fail-safe timer. Default is 8400h.

TABLE 14. REG3 FAIL-SAFE TIMER VALUE REGISTER (READ/WRITE 80CH)

BIT	DESCRIPTION
31 (MSB)	0
•	•
•	•
•	•
16	0
15	FAIL-SAFE TIMER VALUE - BIT 15 (MSB)
•	•
•	•
•	•
0 (LSB)	FAIL-SAFE TIMER VALUE - BIT 0 (LSB)

FAIL-SAFE TIMER VALUE: Write this register to set the value for the fail-safe timer. The default value is 8400h. The timer has a 30ns resolution (PCI clock). The timer is loaded when an access is initiated on the local bus and counts down until the access is completed. It will time out if it reaches 0. For test purposes, the failsafe timer can be loaded and decremented via fail safe timer load write and decrement operations generated through REG7.

TABLE 15. REG4 DISCARD TIMER REGISTER (READ 810H)

BIT	DESCRIPTION
31 (MSB)	0
•	•
•	•
•	•
16	0
15	DISCARD TIMER REGISTER - BIT 15 (MSB)
•	•
•	•
•	•
0 (LSB)	DISCARD TIMER REGISTER - BIT 0 (LSB)

DISCARD TIMER REGISTER: Read this register to obtain the current value of the DISCARD TIMER. Default is 0000h.

TABLE 16. REG5 DISCARD TIMER VALUE REGISTER (READ/WRITE 814H)

BIT	DESCRIPTION
31 (MSB)	0
•	•
•	•
•	•
16	0
15	DISCARD TIMER VALUE - BIT 15 (MSB)
•	•
•	•
•	•
0 (LSB)	DISCARD TIMER VALUE - BIT 0 (LSB)

DISCARD TIMER VALUE: Write this register to set the value to be used for the discard timer. The default value is 0. The timer has a 30ns resolution (PCI clock). The timer is loaded on the completion of a local bus read. The discard timer will then count up. If the PCI retry has not occurred by the time that bit 15 becomes a 1, the timer stops and the data is discarded. For test purposes, the discard timer can be loaded and incremented via discard timer load and increment operations generated through REG7.

TABLE 17. REG6 RESERVED REGISTER (READ/WRITE 818H)

BIT	DESCRIPTION
31 (MSB)	RESERVED
•	•
•	•
•	•
0 (LSB)	RESERVED

TABLE 18. TIMER CONTROL / INTERRUPT REGISTER (WRITE 81CH)	
BIT	**DESCRIPTION**
31 (MSB)	0
•	•
•	•
•	•
6	0
5	LOAD DISCARD TIMER
4	INCREMENT DISCARD TIMER
3	LOAD FAILSAFE TIMER
2	DECREMENT FAILSAFE TIMER
1	CLEAR FAILSAFE INTERRUPT
0 (LSB)	ACE RESET
NOTE: All REG7 functions occur when a '1' is written to the corresponding bit.	

LOAD DISCARD TIMER: (for test purposes with the value stored in REG5).

INCREMENT DISCARD TIMER: (for test purposes).

LOAD FAILSAFE TIMER: (for test purposes with the value stored in REG3).

DECREMENT FAILSAFE TIMER: (for test purposes).

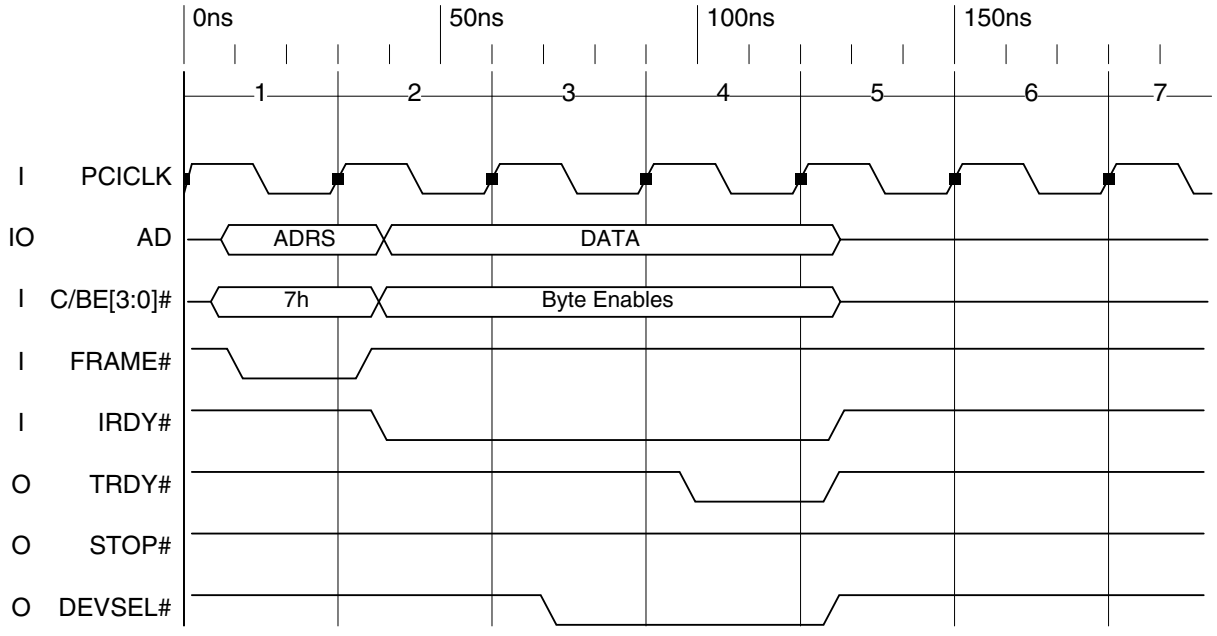
CLEAR FAILSAFE INTERRUPT: Writing a "1" will clear the failsafe error irq and resume normal operation.

ACE RESET: Writing a "1" to REG7 will generate a reset pulse to the ACE's.

BAR2 is used to access the 128 Kbytes (64K words) of Local RAM, if present. BAR2 returns FFFE0000h when all Fs are written to it.

PCI BUS OPERATIONS

The basic ACE-Bridge PCI transaction takes 3 PCI clocks, on top of the command phase. For example, a single write to any location within the ACE-Bridge memory space takes 4 PCI clocks, as shown in FIGURE 4. Note that this is a single write, not an attempted burst write: FRAME# is not held asserted by the master. Also note that a write to the ACE registers or ACE memory is actually a write into the write FIFO whereas a write to the PCI interface registers (BAR1 800-81Ch) is a write to the registers themselves.



PCI single write to any legal memory location (C/BE# = 7h)

FIGURE 4. PCI SINGLE MEMORY WRITE TO ACE-BRIDGE

For easy reference, TABLE 19 provides the timing parameters for 3.3V PCI signaling environments applicable to the ACE-Bridge, and FIGURE 6 shows the timing reference points. The timing parameters apply to the other timing diagrams, but are not illustrated. The ACE-Bridge conforms to revision 2.2 of the PCI Local Bus specification. The timing parameters are provided here for ease of reference only.

TABLE 19. PCI INTERFACE TIMINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS
tv	CLK to signal valid delay	2	11	ns
tsu	Input setup time to CLK	7		ns
th	Input hold time from CLK	0		ns

FIGURE 5 illustrates a PCI read from the ACE-Bridge's configuration space. The ACE-Bridge only responds to Type Zero configuration access: AD[1:0] must be 00 during the command phase. The ACE-Bridge will drive a full Dword on the AD lines independent of which byte enables are asserted during the configuration read.

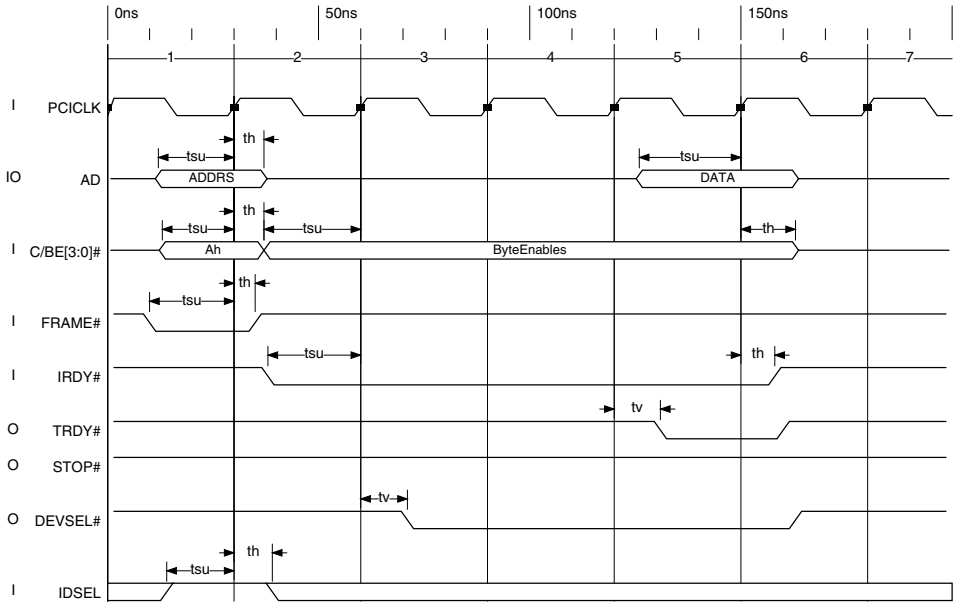
FIGURE 6 illustrates a PCI single write to ACE-Bridge configuration space. The ACE-Bridge only responds to Type Zero configuration access: AD[1:0] must be 00 during the command phase. Note that all combinations of byte enables for configuration writes are supported. If no byte enables are asserted during a burst write to configuration space no internal write will occur, but the internal address will be incremented.

FIGURE 8 illustrates the process of reading an ACE memory (BAR0) or ACE register (BAR1 000-5FCh) location, assuming that there is an ACE present in the specific memory space. The actual read shown is that of a single word read, due to the ~600 nS response time shown, see following text and timing formula tables. If the write FIFO is empty and there isn't a previous Delayed Read Request (DRR) pending, a read from these locations enques a DRR, which is then processed by the ACE-Bridge. If either of these conditions is true, the ACE-Bridge will respond with a Retry, but will not enque any new DRR. The ACE-Bridge uses a DRR mechanism to respond to BA0 and BAR1 000-5FCh reads because the time required to fetch these locations from the ACEs present on the local bus is greater than the PCI data latency rules.

The ACE-Bridge responds to the first read with a Retry. By PCI rules the master must repeat the same exact request until it completes. This is shown by the master's second read attempt, which also produces a Retry. Each repeated read request from the master will be target terminated with a Retry until the data from the enqued DRR is present in the ACE-Bridge's PCI interface. The successful completion is shown at the third read request, which produces a Disconnect with Data.

This process applies to any memory read from legal address space **other** than the PCI-ACE interface registers at BAR1 offset 800-81Ch.

When reading ACE memory (BAR0), any combination of byte enables is supported, but the ACE-Bridge will drive the entire



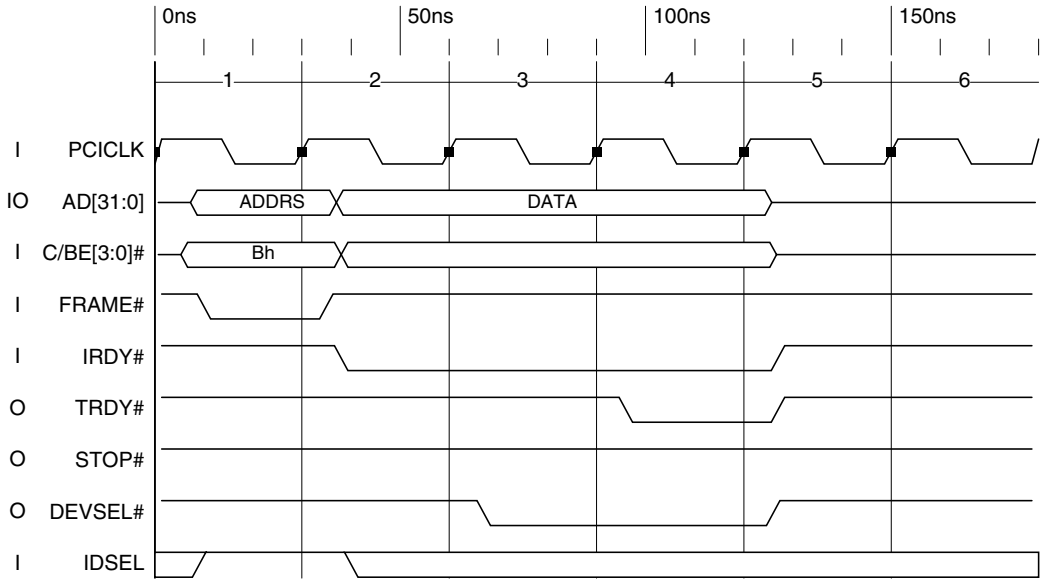
PCI single read from PACE configuration space (C/BE# = Ah)
with PCI timing parameters. AD[31:0]: address driven by master; data driven by PACE

FIGURE 5 PCI SINGLE READ OF CONFIGURATION SPACE WITH TIMING

word onto the AD lines when only a single byte enable in the word is asserted.

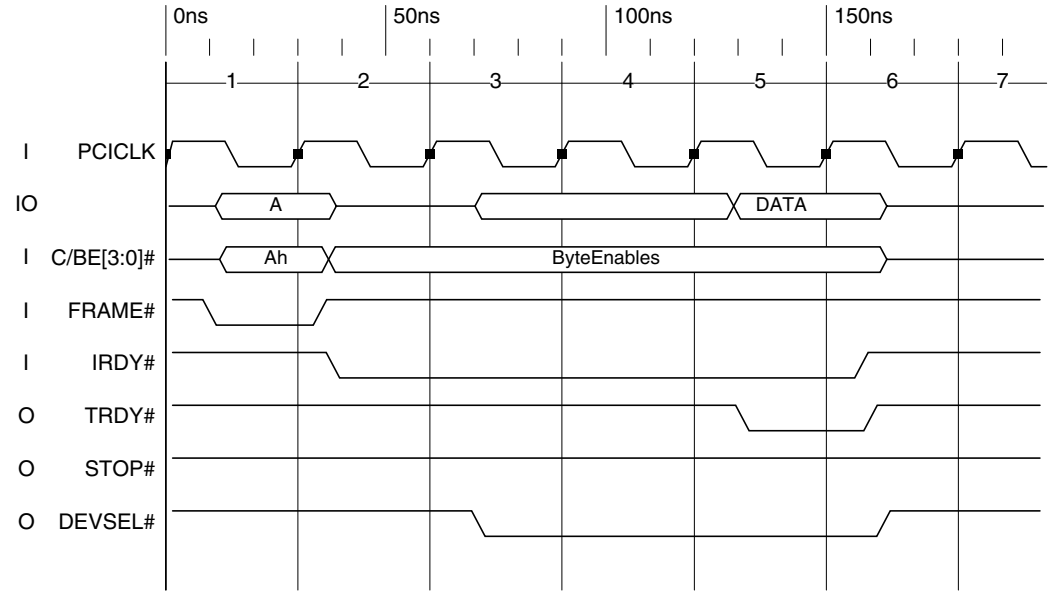
When reading ACE registers (BAR1 00-FCh), byte enable combinations where only a single byte within a word is requested will cause the ACE-Bridge to terminate the transaction with a target abort. The ACE-Bridge will drive all zeros onto the AD lines if only the upper word byte enables or no byte enables are asserted.

With relation to actual timing, PCI double word reads of ACE memory (BAR0) will take longer to complete than single word ACE memory reads because the local bus data path is 16 bits wide. In addition, read cycles will take longer to complete with slower ACE clocks. See TABLE 20 for min/max formulas for calculating completion time for the various types of reads.



PCI single write to PACE configuration space (C/BE# = Bh)

FIGURE 6. PCI SINGLE WRITE TO CONFIGURATION SPACE



PCI read of PCI-ACE IF Registers (BAR1 800 - 81Ch)

FIGURE 7. PCI READ OF PCI-ACE IF REGISTERS (BAR1 800-81CH)

TABLE 20. MIN/MAX DELAYED READ FORMULAS		
TYPE OF READ	**MIN TIME FORMULA**	**MAX TIME FORMULA**
ACE memory (BAR0), double word	13 x PCI_CLKperiod + 11 x ACE_CLKperiod	16 x PCI_CLKperiod + 14 x ACE_CLKperiod
ACE memory (BAR0) single word or ACE register (BAR1, double word or lower word)	8 x PCI_CLKperiod + 5 x ACE_CLKperiod	10 x PCI_CLKperiod + 6 x ACE_CLKperiod
No CBEN# asserted or ACE register (BAR1) upper word	3 x PCI_CLKperiod	3 x PCI_CLKperiod

The third case returns all zeroes and is shown only for completeness.

The following examples have the same conditions: PCI clock = 33MHz, ACE clock = 16MHz, no ACE contention.

Single word read
Min time = 8 x 30 ns + 5 x 62.5 ns = 552.5 ns
Max time = 10 x 30ns + 6 x 62.5 ns = 675 ns

Double word read
Min time = 13 x 30 ns + 11 x 62.5 ns = 1077.5 ns
Max time = 16 x 30ns + 14 x 62.5 ns = 1167.5 ns

In addition, the following amount of ACE clocks should be added for maximum time if the ACE is active.

TABLE 21. ADDITIONAL DRR DELAY FOR CONTESTED ACE RAM ACCESS	
ACE OPERATING MODE	**MAX ADDITIONAL ACE CLOCKS**
Enhanced CPU access enabled, single word transfer	3
Enhanced CPU access enabled, double word transfer	6
Enhanced CPU access disabled, single word transfer	67
Enhanced CPU access disabled, double word transfer	74
Enhanced CPU access is a feature of the Enhanced Mini-ACEs and Micro-ACEs ONLY and is controlled by bit 14 of Configuration Register #6.	

Note that one of the conditions for enquing a DRR is that the write FIFO must be empty. Theoretically, for efficient use of PCI bus bandwidth, the driver software should be written such that it checks the FIFO condition (BAR1 800-81CH registers are directly readable, bypassing the DRR mechanism) before reading from the other ACE-Bridge locations. If the FIFO is not empty (BAR1 800h bit 30 is the FIFO not empty flag) and a read is attempted, the bus master will be using PCI bandwidth repeating the read request while the FIFO empties, **before** the read request is actually enqued as a DRR in the ACE-Bridge. The FIFO "drain" delay will increase the overall read delay further.

A typical situation where the extra FIFO "drain" delay might be encountered is during diagnostics of the internal RAM. When a RAM pattern is written to the device the FIFO can fill completely and the readback of the pattern might occur immediately after the pattern is written. In this case, the first read attempt will produce a retry which will cause the master to start repeating the read request. AFTER the FIFO drains fully the next repeated read request will actually cause the ACE-Bridge to enque the read request, which will start the DRR mechanism described earlier.

The FIFO drain speed is dependent upon the ACE clock and how full the FIFO is. On average, a 16MHz ACE clock can drain a 16 bit word from the FIFO every ~600nS. For example, if the FIFO is full when a PCI read is attempted, the read will complete in ~ (32 x 0.6µs) + 1 µs = 20.2µs.

This delay is something to be aware of when using the ACE-Bridge with PCI bridges/controllers that have PCI retry counters. Examples of such devices for the PPC environment are the CPC710, GT-64260, etc. If the retry counters are enabled in these devices the value should be set to a large enough value so that the counter does not reach the maximum value when reading from the ACE-Bridge. Typically, the power-on default value is on these devices is 0, which will defeat the counter and allows infinite retries.

The minimum retry period is determined by how quickly the ACE-Bridge terminates a transaction and the PCI rule that a master "must deassert REQ# for two consecutive clocks, one of which while the bus is Idle, before any transaction that was target terminated can be repeated". The ACE-Bridge terminates a PCI transaction in 5 clocks, as shown in FIGURE 8. The "deassert REQ#" rule involves the bus arbiter during bus reacquisition by the master.

Actual measurements of a PCI-Enhanced Mini-ACE being read by the PCI motherboard host in a hi-performance X86 system (**not** the timing shown in FIGURE 8) show that a read can be retried every 8 PCI clocks. Since it is the motherboard PCI controller, the arbiter parks the PCI bus on this controller, which allows such fast retry speeds.

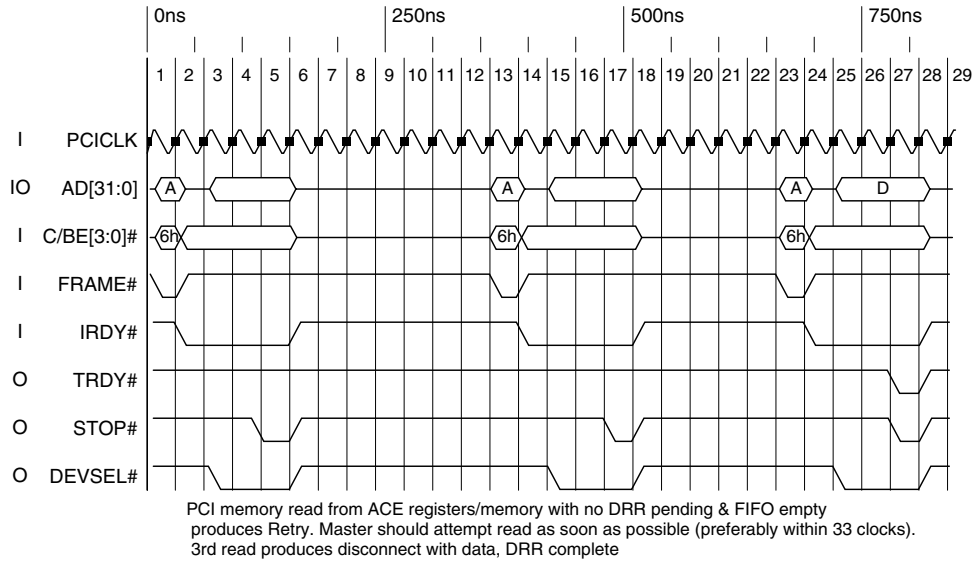
Therefore, in this extreme case, the motherboard host can repeat the read 84 times (20.2µs/(8x30ns)) before data is presented, so the PCI retry counter should be set to a value higher than 84.

FIGURE 9 illustrates a 16 Dword (32 word) PCI memory write burst, with the write FIFO empty (or with enough free space to absorb the 16 Dwords in the FIFO). The write FIFO accepts PCI memory writes to the ACE memory (BAR0) and ACE registers (BAR1 offset 00h - FCh). It does not accept writes to the PCI interface registers at BAR1 offset 800-81Ch. Writes to the BAR1 800-81Ch space go directly into the PCI interface registers. The 32 byte write shown could be an entire 1553 message being written to ACE memory.

Writes into the BAR 0 space must be word or Dword. If only one byte enable is asserted in a word, the PCI Enhanced Mini-ACE terminates the transaction with a Target-Abort.

Writes into the BAR 1 00-FCh space must be word or Dword. If only one byte enable is asserted in a word, the PCI Enhanced Mini-ACE terminates the transaction with a Target-Abort. Since the ACE registers in this space are really 16-bit registers packed into the lower word of a 32-bit structure, only lower word or Dword writes transfer bits into these ACE registers.

In addition, as per PCI spec, a Memory Write and Invalidate (C/BE[3:0]# = Fh) command will be aliased to the basic Memory Write command and the timing diagram would look the same as FIGURE 4.



PCI memory read from ACE registers/memory with no DRR pending & FIFO empty produces Retry. Master should attempt read as soon as possible (preferably within 33 clocks). 3rd read produces disconnect with data, DRR complete

FIGURE 8. PCI READ OF ACE MEMORY/REGISTER

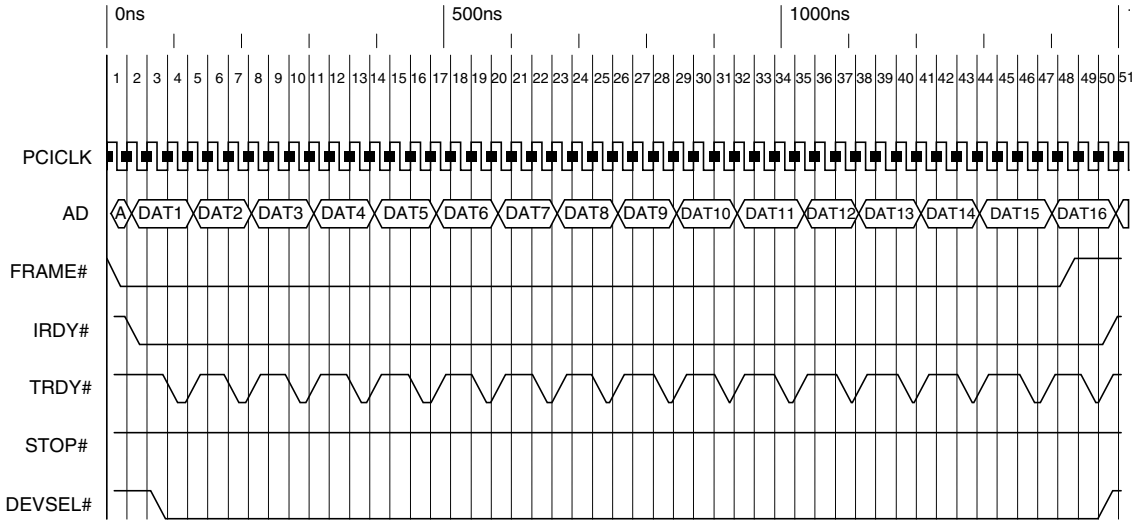


FIGURE 9. PCI WRITE BURST TO ACE MEMORY WITH FIFO EMPTY

LOCAL PROCESSOR INTERFACE

DMA INTERFACE

The control signals include the standard DMA handshake signals REQ, GNT, ACK, as well as the transfer control outputs MEM/REG and RD/WR, the ACE handshake signals SELECT [5:0] and RDY [5:0], and LOCAL_CS which is used as a chip select for RAM access.

The BU-66318 ACE-Bridge supports a DMA type local bus interface when a local processor is utilized. When a local CPU is detected on power-up, via the GNT signal, the local bus interface is enabled. If the local bus interface is used, the OE/MEM/REG, WE/RD/WR, ADDRESS, and DATA buses will be tri-stated unless the bus is granted to the Bolt-On-PCI device or if the ACE-Bridge is being written to from the local bus (CS asserted). The ACE-Bridge will take control of the local bus after it asserts REQ and receives a GNT back. The bus will remain in control of the ACE-Bridge until it negates ACK. If the local bus interface is not used all control signals are two-state, not tri-state.

Data transfers between the subsystem (subsystem is defined as the entire local bus) and the BU-66318 are initiated by means of a DMA handshake, initiated by the BU-66318. A data read operation is defined to be the transfer of data from the subsystem to the BU-66318. Conversely, a data write operation transfers data from the BU-66318 to the subsystem. Data is transferred as a single 16-bit word.

DMA READ FROM RAM OPERATION

In response to a PCI read, if the requested address falls within the local RAM window, the BU-66318 needs to read data words from the local RAM. To initiate a data word read transfer, the ACE-Bridge asserts the signal REQ low. Assuming that the local processor asserts GNT in time, the BU-66318 will then present a valid address and assert the control signals OE and LOCAL_CS low, along with ACK low, to enable data to be read from the local RAM.

Each 32-bit word PCI read operation causes two consecutive 16-bit words reads to occur from the local RAM. The address is presented for the first word, and then after the Data Word has been written, the value of the address bus outputs A15 - A0 are incremented.

DMA WRITE TO RAM OPERATION

In response to a PCI write, if the requested address falls within the local RAM window, the BU-66318 needs to write data words to the local RAM. To initiate a data word write transfer, the ACE-Bridge presents valid address and asserts the signal REQ low. Assuming that the local processor asserts GNT in time, the BU-66318 will then assert the control signals WE low and LOCAL_CS, along with ACK low, to enable data to be written to the local RAM.

All write operations are transferred through the BU-66318 to the subsystem in a contiguous burst. Each 32-bit word PCI write operation causes two single 16-bit words writes to the local RAM. The address is presented for the first word, and then after the Data Word has been written, the value of the address bus outputs A15 - A0 are incremented.

DMA READ FROM ACE OPERATION

In response to a PCI read, if the requested address is directed towards ACE RAM or ACE register space, the BU-66318 needs to read data words from the appropriate ACE RAM or register. To initiate a data word read transfer, the ACE-Bridge asserts the signal REQ low. Assuming that the local processor asserts GNT in time, the BU-66318 will then present valid address and assert the control signals RD high and MEM/REG high for memory access or MEM/REG low for register access, along with ACK low. Following the latter, SELECT is asserted low. The SELECT [5:0] signal is tied to the corresponding ACEs SELECT and STRBD inputs. Data is read from the ACE once the RDY [5:0] signal is asserted low (ACE READYD signal is asserted by the ACE).

Each 32-bit word PCI read operation causes two consecutive 16-bit word reads to occur from the ACE memory. When reading ACE registers only a single 16-bit read occurs. In other words, if the requested read is of an ACE register, only the first half of the 32-bit word transferred back to the PCI bus is valid

DMA WRITE TO ACE OPERATION

In response to a PCI write, if the requested address is directed towards ACE RAM or ACE register space, the BU-66318 needs to write the data words to the appropriate ACE RAM or register. To initiate a data word write transfer, the ACE-Bridge asserts the signal REQ low. Assuming that the local processor asserts GNT in time, the BU-66318 will then present valid address and data, assert the control signals WR low and MEM/REG high for memory access or MEM/REG low for register access, along with ACK low. Following the latter, SELECT is asserted low. The SELECT [5:0] signal is tied to the corresponding ACEs SELECT [5:0] and STRBD inputs. Data is sampled by the ACE following the RDY [5:0] signal is asserted low (ACE READYD signal is asserted by the ACE).

Each 32-bit word PCI write operation causes two consecutive 16-bit word writes to occur to ACE memory. When writing to ACE registers only the first 16-bits of the 32-bit PCI word are written.

ACE ACCESS

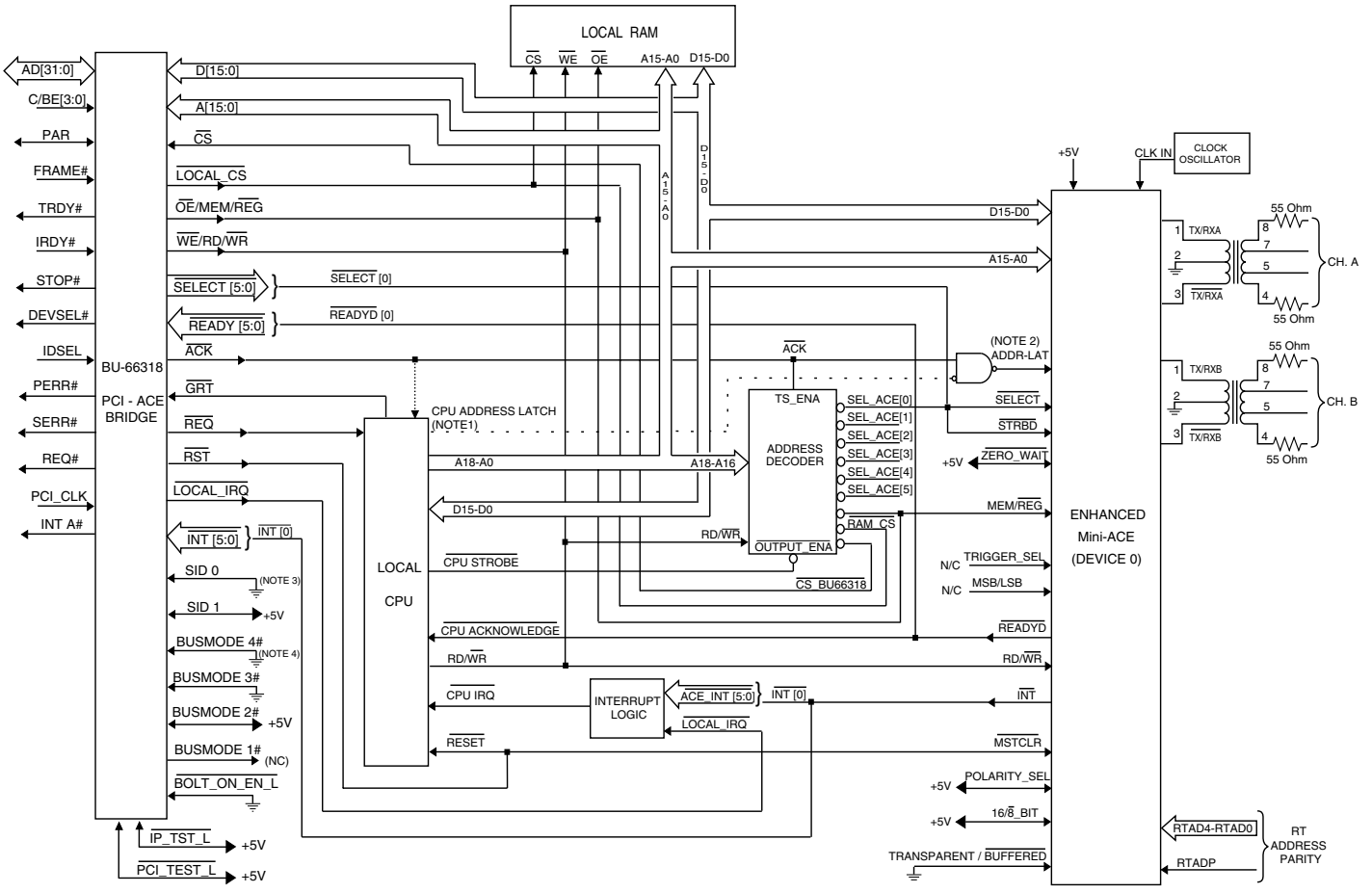
The ACE-Bridge accesses the ACE hybrid via the SELECT and STROBE handshake method. Although the BU-66318 can access the entire ACE family, the Enhanced Mini-ACE series is the MIL-STD-1553 terminal of choice. The Enhanced Mini-ACE is the fastest and contains the most functionality. The Enhanced Mini-ACE has also remained compatible with software from the older ACE series parts.

Processor access to the Enhanced Mini-ACE has been greatly improved. The Enhanced Mini-ACE's maximum host holdoff time (time prior to the assertion of the READYD handshake signal)

has been significantly reduced. For ACE/Mini-ACE, this maximum holdoff time is 10 internal word transfer cycles, resulting in an overall holdoff time of approximately 2.8 µs, using a 16 MHz clock. When the Enhanced Mini-ACE's ENHANCED CPU ACCESS feature is used, this worst-case holdoff time is reduced to a single internal transfer cycle. For example, when operating the Enhanced Mini-ACE in its 16-bit buffered, non-zero wait configuration with a 16 MHz clock input, this results in a maximum overall host transfer cycle time of 632 ns for a read cycle, or 570 ns for a write cycle.

FIGURE 10 illustrates a generic connection diagram between the BU-66318, a 16-bit microprocessor, a local RAM, and an Enhanced Mini-ACE (decoder configuration is shown to allow for up to 6 Enhanced Mini-ACEs). The Enhanced Mini-ACE is configured for the 16-bit buffered, Non-Zero Wait configuration. This configuration may be used to interface between 16-bit or 32-bit microprocessors and an Enhanced Mini-ACE. In this mode, only the Enhanced Mini-ACE's 4K or 64K words of internal RAM are used for storing 1553 message data and associated "housekeeping" functions. In this configuration the Enhanced Mini-ACE will never attempt to access memory on the host bus.

FIGURE 11 illustrates the ACE-Bridge reading from an ACE, and FIGURE 12 illustrates writing to the RAM using "DMA-type" arbitration for the bus.



NOTES
1. CPU ADDRESS LATCH SIGNAL PROVIDED BY PROCESSORS WITH MULTIPLEXED ADDRESS/DATA BUSES.
2. FOR PROCESSORS WITH SEPARATE ADDRESS/DATA BUSES, CONNECT ADDR-LAT TO +5V.
3. ASSUMES SUB-SYSTEM VENDOR AND DEVICE ID'S ARE LOADED INTO THE BU-66318 BY THE CPU ON POWER-UP.
4. BUSMODE SIGNALS MUST BE TIED AS LISTED FOR PCI APPLICATIONS.

FIGURE 10. BU-66318 ACE-BRIDGE WITH LOCAL CPU, RAM, AND ENHANCED MINI-ACE

FIGURE 12 illustrates a write by the ACE-Bridge into the local bus RAM. The figure includes local bus arbitration showing the ACE-Bridge acquiring control of the local bus. Note that the timing is shown with zero extra setup time (Reg 1 bits 29 & 28 = 0). Also note that the example shows the ACE-Bridge releasing the bus after the double word write. If the bus arbiter "parked" $\overline{GNT}$ (GNT# remains asserted after $\overline{ACK}$ is asserted) at the ACE-Bridge and the ACE-Bridge had other words to write to the RAM, the ACE-Bridge would NOT release the bus until $\overline{GNT}$ was negated (and it completed it's write cycle) or it emptied it's write FIFO. In this case, with GNT# negated after ACK# was asserted, the ACE-Bridge would have to renegotiate for the local bus if the ACE-Bridge had more words to transfer from it's write FIFO to the local bus.

LOCAL PROCESSOR TO BU-66318 MEMORY MAP

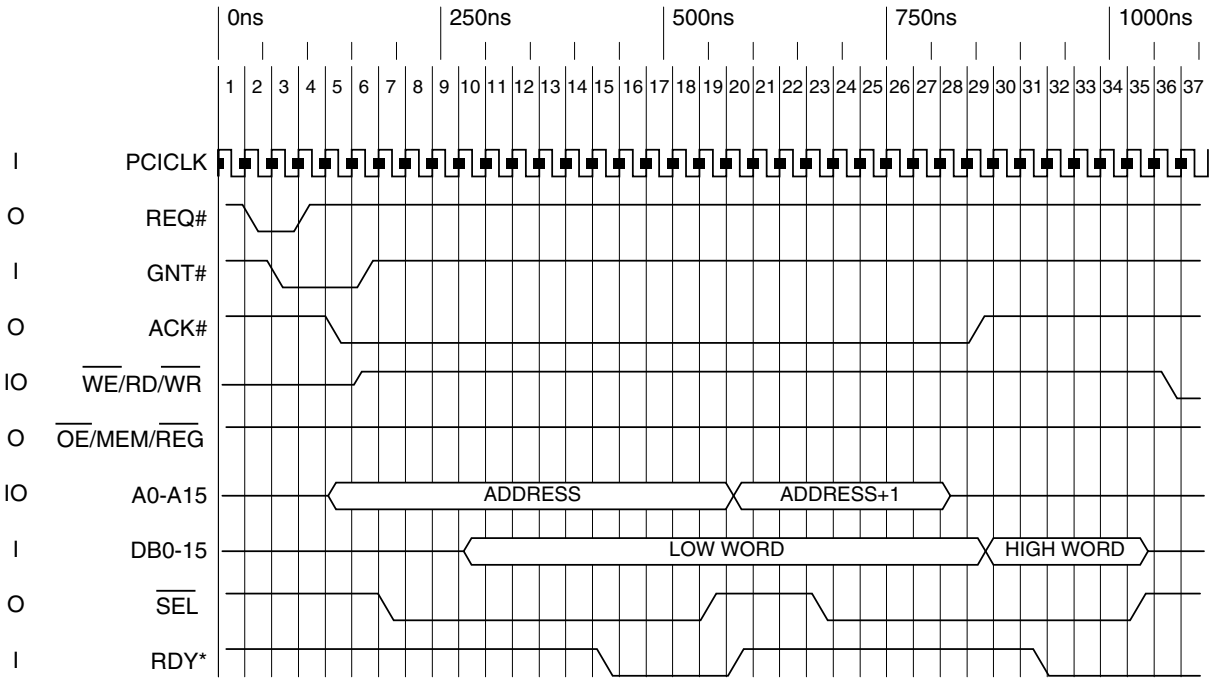
The BU-66318 ACE-Bridge contains a register area that is accessible by the local CPU. These register locations are mapped out and are accessed by the lower two bits of the address bus (A1 - A0).

Although there are eight addresses mapped, there are currently four useable registers contained in the mapping. Registers are used to write and read the subsystem vendor and subsystem device ID's, and to read and write the IRQ registers.

The local CPU accesses ACE-Bridge register space by first asserting the $\overline{CS}$ signal low and then driving a valid address onto the address bus. Following a valid address being read, the BU-66318 will then either drive the requested information onto the data bus, or will read information from the data bus and store it in the requested register. $\overline{B_RDY}$ is the ACE-Bridge's handshake signal that indicates the data bus is valid for a read operation or that the data bus has been written to the selected internal register.

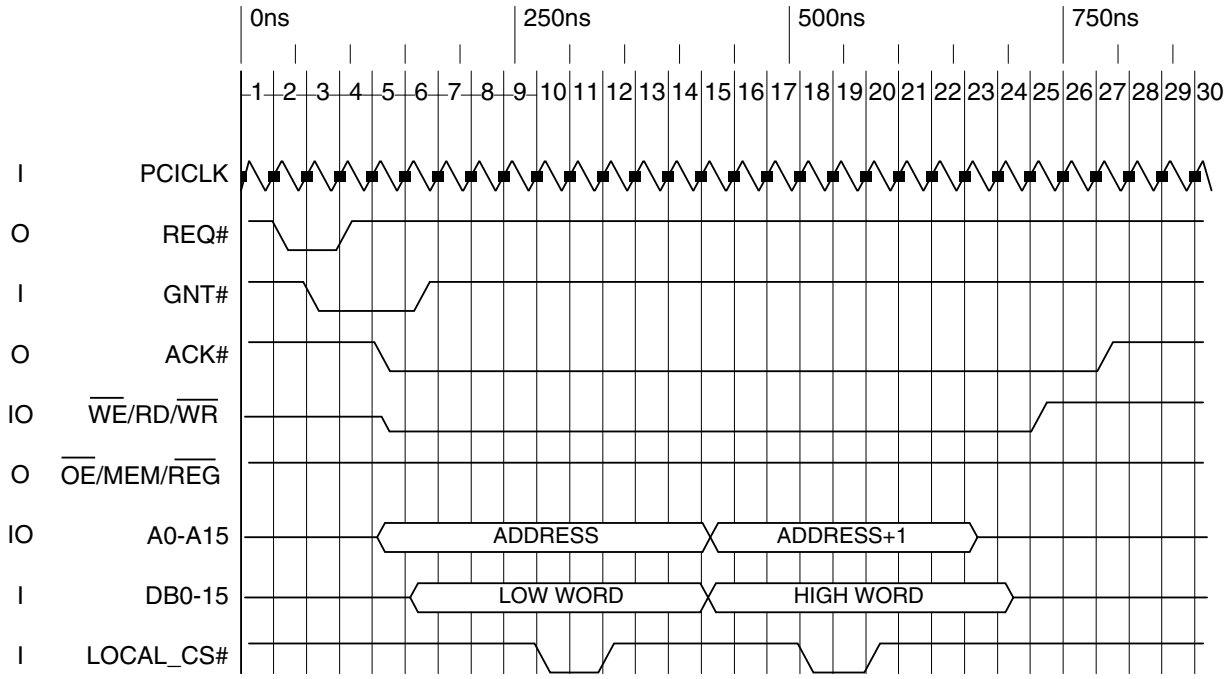
TABLE 22. LOCAL PROCESSOR TO BU-66318 MEMORY MAP

RD/$\overline{WR}$	A1	A2	FUNCTION
0	0	0	Write to ACE-Bridge IRQ register (generates a PCI interrupt)
0	0	1	not used
0	1	0	Write to Sub-System Vendor ID
0	1	1	Write to Sub-System Device ID
1	0	0	Read ACE-Bridge IRQ register
1	0	1	not used
1	1	0	Read Sub-System Vendor ID
1	1	1	Read Sub-System Device ID



Local bus RAM Double word read with local bus arbitration, without extra setup delay

FIGURE 11. BU-66318 ACE-BRIDGE READ FROM ACE



Local bus RAM write with local bus arbitration, without extra setup delay

FIGURE 12. ACE-BRIDGE DWORD WRITE TO RAM

SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS

TABLE 23. POWER AND GROUND

SIGNAL NAME	PIN	DESCRIPTION
+3.3V - LOGIC(Vcc)	20, 28, 29, 38, 47, 48, 71, 76, 79, 80, 86, 90, 98, 99, 116, 123, 124, 133, 141, 150, 151, 169, 170, 184, 185, 194, 202, 203	Logic power (Vcc)
GROUND	6, 7, 21, 30, 31, 39, 58, 59, 72, 73, 81, 82, 89, 91, 109, 110, 117, 125, 126, 134, 142, 162, 163, 171, 173, 186, 187, 195,	Ground

TABLE 24. LOCAL DATA BUS

SIGNAL NAME	PIN	DESCRIPTION
DB15 (MSB)	201	16-bit bi-directional data bus. This bus interfaces the BU-66318 to the local processor, local RAM, and to the ACE terminals. This bus allows data transfers to take place between the internal ACE protocol/memory management logic and up to 64K x 16 of external RAM. If a local processor is detected by means of the $\overline{GNT}$ signal being high at power-up, the outputs for D15 through D0 are in the high impedance state when data is not being driven onto the local bus.
DB14	200	
DB13	199	
DB12	198	
DB11	197	
DB10	196	
DB9	193	
DB8	192	
DB7	191	
DB6	190	
DB5	189	
DB4	188	
DB3	183	
DB2	182	
DB1	181	
DB0 (LSB)	180	

TABLE 25. LOCAL ADDRESS BUS		
SIGNAL NAME	**PIN**	**DESCRIPTION**
A15 (MSB)	127	16-bit address bus. This bus interfaces the BU-66318 to the local processor, local RAM, and to the ACE terminals. This bus allows data transfers to take place between the internal ACE protocol/memory management logic and up to 64K x 16 of external RAM. If a local processor is detected by means of the $\overline{GNT}$ signal being high at power-up, the outputs for A15 through A0 are in the high impedance state when address is not being driven onto the local bus.
A14	128	
A13	129	
A12	130	
A11	131	
A10	132	
A9	135	
A8	136	
A7	137	
A6	138	
A5	139	
A4	140	
A3	143	
A2	144	
A1	145	Lower 2 bits of 16-bit address bus. The host CPU accesses the ACE-Bridge registers by means of A1 - A0.See the "Local Processor to BU-66318 memory map" section
A0 (LSB)	146	

TABLE 26. LOCAL BUS INTERFACE CONTROL		
SIGNAL NAME	**PIN**	**DESCRIPTION**
$\overline{\text{SELECT0}}$ (O)	66	Connected to the respective device [5:0] ACE terminal's $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ signal pins. Address decoder output to select the ACE for a transfer to/from either RAM or register.
$\overline{\text{SELECT1}}$ (O)	67	
$\overline{\text{SELECT2}}$ (O)	68	
$\overline{\text{SELECT3}}$ (O)	83	
$\overline{\text{SELECT4}}$ (O)	149	
$\overline{\text{SELECT5}}$ (O)	177	
$\overline{\text{RDY0}}$ (I)	69	Handshake input from the respective ACE device [5:0] $\overline{\text{READYD}}$ signal pins. For a read access, $\overline{\text{RDY}}$ is asserted at the end of a host transfer cycle to indicate that data is available to be read on D15 through D0 when asserted (low). For a write cycle, $\overline{\text{RDY}}$ is asserted at the end of the cycle to indicate that data has been transferred to a register or RAM location. For both reads and writes, the BU-66318 asserts SELECT / $\overline{\text{STRBD}}$ low until $\overline{\text{READYD}}$ is asserted low.
$\overline{\text{RDY1}}$ (I)	70	
$\overline{\text{RDY2}}$ (I)	122	
$\overline{\text{RDY3}}$ (I)	97	
$\overline{\text{RDY4}}$ (I)	112	
$\overline{\text{RDY5}}$ (I)	119	
$\overline{\text{INT0}}$ (I)	44	Interrupt request input from respective ACE devices [5:0]$\overline{\text{INT}}$ signal pins. ACE interrupts are active low signals.Following a PCI RST#, all connected ACE devices should drive their INT signals inactive high. At this time the BU-66318 tests its INT [5:0] signals for a low condition. If an active low signal is present, the corresponding ACE device is recorded as "not present".Any unused ACE channel should have its corresponding INT [5:0] signal grounded.
$\overline{\text{INT1}}$ (I)	61	
$\overline{\text{INT2}}$ (I)	120	
$\overline{\text{INT3}}$ (I)	93	
$\overline{\text{INT4}}$ (I)	96	
$\overline{\text{INT5}}$ (I)	113	
RD / $\overline{\text{WR}}$ (I/O)	78	Read / Write. For ACE or local RAM access, RD/$\overline{\text{WR}}$ selects between reading (RD/$\overline{\text{WR}}$ = 1) and writing (RD/$\overline{\text{WR}}$ = 0). When the local processor is accessing the ACE-Bridge's internal registers ($\overline{\text{CS}}$=0) this signal determines whether an internal register is being written or read.
MEM / $\overline{\text{REG}}$ (O)	75	Memory / Register. For ACE access, MEM/$\overline{\text{REG}}$ selects between ACE memory (MEM/$\overline{\text{REG}}$ = "1") or register access (MEM/$\overline{\text{REG}}$ = "0"). When performing a local RAM read, this pin is an output.
$\overline{\text{REQ}}$(O)	179	Data Transfer Request. Active low level output signal used to request access of the local bus from the local CPU.
$\overline{\text{GNT}}$ (I)	164	Data Transfer Grant. Active low input signal asserted by the local CPU in response to the $\overline{\text{REQ}}$ output to indicate that control of the local bus has been transferred from the local microprocessor to the ACE-Bridge. Once asserted, $\overline{\text{GNT}}$ may not be de-asserted prior to the assertion of $\overline{\text{ACK}}$. $\overline{\text{GNT}}$ must be connected to ground when a local CPU is not used.
$\overline{\text{ACK}}$(O)	178	Data Transfer Acknowledge. Active low output signal used to indicate acceptance of the local bus in response to a data transfer grant $\overline{\text{GNT}}$. The local bus is always controlled by the BU-66318 during the time that $\overline{\text{ACK}}$ is asserted low.The BU-66318 will drive all ACE control signals to their in-active (logic '1') state prior to beginning a transaction and again after completing a transaction, prior to de-asserting $\overline{\text{ACK}}$.
$\overline{\text{CS}}$(I)	175	Chip Select signal input from local CPU indicating that it is accessing BU-66318 internal registers.This signal must be pulled-up when a local CPU is not used.
$\overline{\text{LOCAL_CS}}$(O)	9	Chip select signal asserted by BU-66318 when a transfer to local RAM is being performed. When local RAM is accessed ACE signals RD/WR and MEM/REG will be utilized to generate $\overline{\text{OE}}$ and $\overline{\text{WE}}$.
$\overline{\text{LOCAL_IRQ}}$(O)	11	Interrupt signal to the local processor asserted by the ACE-Bridge in response to any bit being set in REG1 from a PCI write. This signal will remain asserted until the local processor performs a read from the ACE-Bridge IRQ register.
$\overline{\text{RST}}$(O)	10	Reset signal to the local bus asserted active low following a PCI RST#.
$\overline{\text{B_RDY}}$(O)	77	Local bus handshake signal to indicate data is valid during a read of the ACE-Bridge's local bus registers OR that the ACE-Bridge has accepted the data during a write to the ACE-Bridge's internal registers

TABLE 27. PCI BUS ADDRESS AND DATA SIGNALS

SIGNAL NAME	PIN	DESCRIPTION
AD31 (MSB) (I/O)	12	32-Bit PCI Bus Address / Data lines. Address and Data are multiplexed on the same pins. Each bus operation consists of an address phase followed by one or more data phases. Address phases are identified when the control signal FRAME# is asserted. Data transfers occur during those clock cycles in which the control signals IRDY# and TRDY# are both asserted.
AD30 (I/O)	14	
AD29 (I/O)	16	
AD28 (I/O)	17	
AD27 (I/O)	18	
AD26 (I/O)	19	
AD25 (I/O)	22	
AD24 (I/O)	23	
AD23 (I/O)	26	
AD22 (I/O)	32	
AD21 (I/O)	36	
AD20 (I/O)	43	
AD19 (I/O)	45	
AD18 (I/O)	46	
AD17 (I/O)	62	
AD16 (I/O)	63	
AD15 (I/O)	64	
AD14 (I/O)	65	
AD13 (I/O)	85	
AD12 (I/O)	87	
AD11 (I/O)	92	
AD10 (I/O)	94	
AD9 (I/O)	95	
AD8 (I/O)	111	
AD7 (I/O)	114	
AD6 (I/O)	115	
AD5 (I/O)	121	
AD4 (I/O)	147	
AD3 (I/O)	165	
AD2 (I/O)	166	
AD1 (I/O)	167	
AD0 (I/O) (LSB)	168	
C/BE[3]# (I)	24	Bus Command and Byte Enables. These signals are multiplexed on the same pins. During the address phase of a bus operation, these pins identify the bus command, as shown in the table of ACE-Bridge commands below. During the data phase of a bus operation, these pins are used as Byte Enables, with C/BE[0]# enabling byte 0 (LSB) and C/BE[3]# enabling byte 3 (MSB). C/BE[3:0]# — Description (during address phase) 0 1 1 0 — Memory Read 0 1 1 1 — Memory Write 1 0 1 0 — Configuration Read 1 0 1 1 — Configuration Write 1 1 0 0 — Memory Read - MULTIPLE
C/BE[2]# (I)	37	
C/BE[1]# (I)	84	
C/BE[0]# (I)	148	
PAR(I/O)	35	Parity. This signal is even parity across the entire AD[31:0] field along with the C/BE[3:0]# field. The parity is stable in the clock following the address phase and is sourced by the Bus Master. During the data phase for write operations, the Bus Master sources this signal on the clock following IRDY# active. During the data phase for read operations, this signal is sourced by the Target and is valid on the clock following TRDY# active. The PAR signal therefore has the same timing as AD[31:0], delayed by one clock.

TABLE 28. PCI BUS SYSTEM SIGNALS		
SIGNAL NAME	**PIN**	**DESCRIPTION**
PCI_CLK_IN (I)	172	Clock input. The rising edge of this signal is the reference upon which all other clock signals are based, with the exception of RST# and INTA#. The maximum frequency accepted is 33 MHz and the minimum is 0 Hz.
RST# (I)	88	Reset. This signal is used to bring all other signals within this device, and on the local bus, to a known, consistent state. All PCI bus interface output signals are not driven (tri-stated), and open drain signals are floated.

TABLE 29. PCI BUS CONTROL SIGNALS		
SIGNAL NAME	**PIN**	**DESCRIPTION**
FRAME#(I)	25	Frame. This signal is driven by the current bus master and identifies both the beginning and duration of a bus operation. When FRAME# is first asserted, it indicates that a bus transaction is beginning and that valid addresses and a corresponding bus command are present on the AD[31:0] and C/BE[3:0] lines. FRAME# remains asserted during the data transfer portion of a bus operation and is deasserted to signify the final data phase.
IRDY#(I)	27	Initiator Ready. This signal is sourced by the bus master and indicates that the bus master is able to complete the current data phase of a bus transaction. For write operations, it indicates that valid data is on the AD[31:0] pins. Wait states occur until both TRDY# and IRDY# are asserted together.
TRDY#(O)	34	Target Ready. This signal is sourced by the selected target and indicates that the target is able to complete the current data phase of a bus transaction. For read operations, it indicates that the target is providing valid data is on the AD[31:0] pins. Wait states occur until both TRDY# and IRDY# are asserted together.
STOP#(O)	41	Stop. The Stop signal is sourced by the selected target and conveys a request to the bus master to stop the current transaction.
IDSEL(I)	13	Initialization Device Select. This pin is used as a chip select during configuration read or write operations.
DEVSEL#(O)	33	Device Select. This signal is sourced by an active target upon decoding that its address and bus commands are valid. For bus masters, it indicates whether any device has decoded the current bus cycle. (The BU-66318 operates as a target agent only)
PERR#(O)	40	Parity Error. This pin is used for reporting parity errors during the data portion of the bus transaction for all cycle except a Special Cycle. It is sourced by the agent receiving data and driven active two clocks following the detection of an error. This signal is driven inactive (high) two clocks prior to returning to the tri-state condition.
SERR#(O)	42	System Error. This pin is used for reporting address parity errors, data parity errors on Special Cycle commands, or any other condition having a catastrophic system impact.
INTA#(O)	15	Interrupt A. This pin is a level sensitive, active low interrupt to the host.

TABLE 30. BU-66318 MODE CONFIGURATION PINS		
SIGNAL NAME	**PIN**	**DESCRIPTION**
SID0(I)	8	Sub-System ID configuration pins. See TABLE 2 for details.
SID1(I)	60	
BUSMODE4#(I)	176	Bus Mode Of Operation. If the BU-66318 is used in a PMC backplane these signals pins are tied directly to the bus. When the BU-66318 is used in a PCI backplane these signals must be configured accordingly: BUSMODE4# - GND BUSMODE3# - GND BUSMODE2# - VCC BUSMODE1# - FLOAT
BUSMODE3#(I)	118	
BUSMODE2#(I)	74	
BUSMODE1#(O)	174	

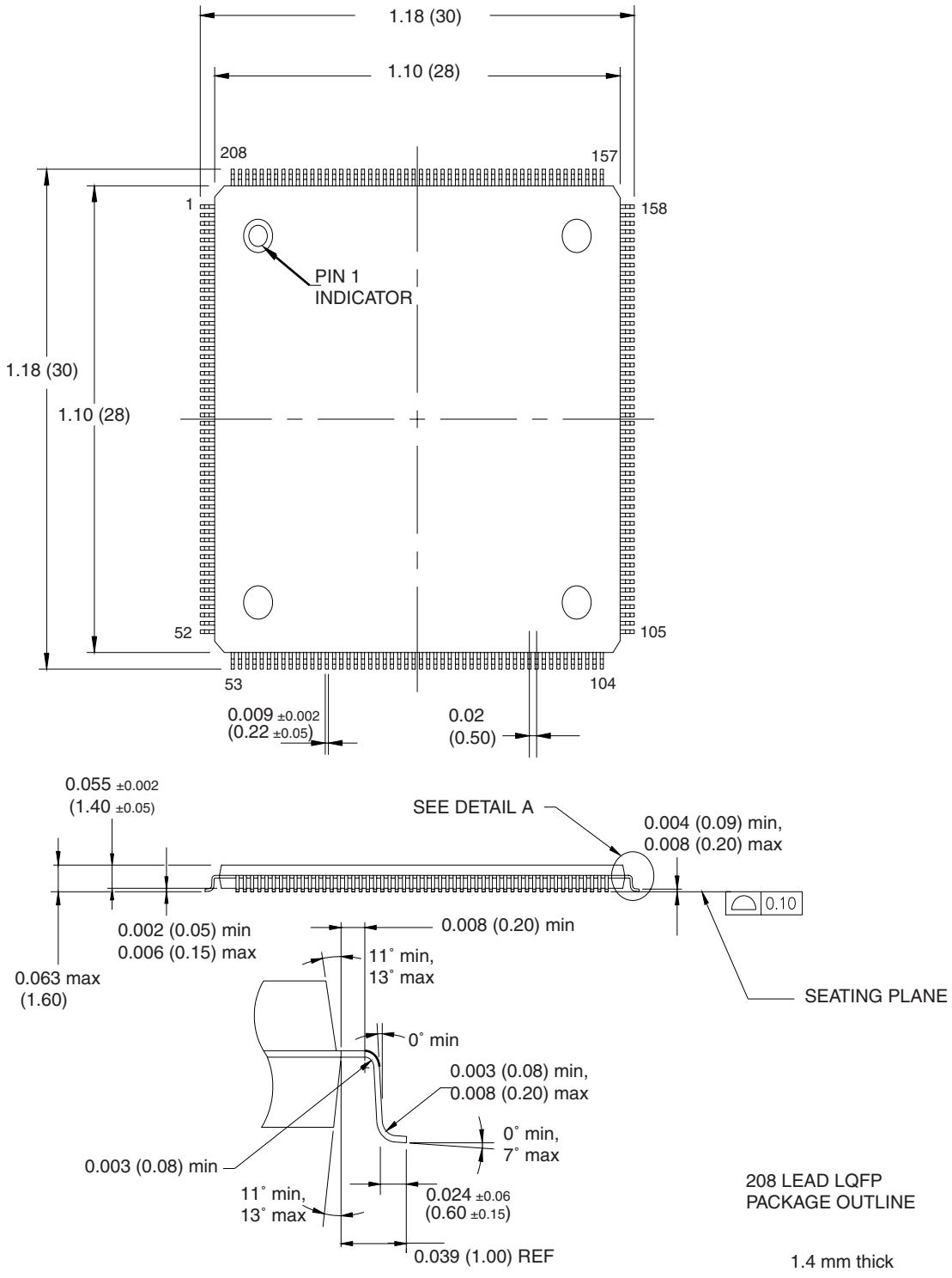
TABLE 31. PINOUTS

PQFP	BU-66318	SIGNAL TYPE	PQFP	BU-66318	SIGNAL TYPE
1	N/C	N/A	53	N/C	N/A
2	N/C	N/A	54	N/C	N/A
3	N/C	N/A	55	N/C	N/A
4	N/C	N/A	56	N/C	N/A
5	N/C	N/A	57	N/C	N/A
6	GND	GND	58	GND	GND
7	GND	GND	59	GND	GND
8	SID0	I	60	SID1	I
9	$\overline{\text{LOCAL_CS}}$	O	61	$\overline{\text{INT1}}$	I
10	$\overline{\text{RST}}$	O	62	AD17	PCI-I/O
11	$\overline{\text{LOCAL_IRQ}}$	O	63	AD16	PCI-I/O
12	AD31	PCI - I/O	64	AD15	PCI-I/O
13	IDSEL	PCI - I	65	AD14	PCI-I/O
14	AD30	PCI - I/O	66	$\overline{\text{SELECT0}}$	O
15	INTA#	PCI - O	67	$\overline{\text{SELECT1}}$	O
16	AD29	PCI - I/O	68	$\overline{\text{SELECT2}}$	O
17	AD28	PCI - I/O	69	$\overline{\text{RDY0}}$	I
18	AD27	PCI - I/O	70	$\overline{\text{RDY1}}$	I
19	AD26	PCI - I/O	71	Vcc	Vcc
20	Vcc	Vcc	72	GND	GND
21	GND	GND	73	GND	GND
22	AD25	PCI - I/O	74	BUSMODE2#	I
23	AD24	PCI - I/O	75	MEM/$\overline{\text{REG}}$	O
24	C/BE[3]#	PCI - I	76	Vcc	I (FACTORY TEST)
25	FRAME#	PCI - I	77	B_RDY_L	O
26	AD23	PCI - I/O	78	RD/$\overline{\text{WR}}$	O
27	IRDY#	PCI - I	79	Vcc	Vcc
28	Vcc	Vcc	80	Vcc	Vcc
29	Vcc	Vcc	81	GND	GND
30	GND	GND	82	GND	GND
31	GND	GND	83	$\overline{\text{SELECT3}}$	O
32	AD22	PCI-I/O	84	C/BE[1]#	PCI-I
33	DEVSEL#	PCI-O	85	AD13	PCI-I/O
34	TRDY#	PCI-O	86	Vcc	I (FACTORY TEST)
35	PAR	PCI-I/O	87	AD12	PCI-I/O
36	AD21	PCI-I/O	88	RST#	PCI-I
37	C/BE[2]#	PCI-I	89	GND	I (FACTORY TEST)
38	Vcc	Vcc	90	Vcc	Vcc
39	GND	GND	91	GND	GND
40	PERR#	PCI-O	92	AD11	PCI-I/O
41	STOP#	PCI-O	93	$\overline{\text{INT3}}$	I
42	SERR#	PCI-O	94	AD10	PCI-I/O
43	AD20	PCI-I/O	95	AD09	PCI-I/O
44	$\overline{\text{INT0}}$	I	96	$\overline{\text{INT4}}$	I
45	AD19	PCI-I/O	97	$\overline{\text{RDY3}}$	I
46	AD18	PCI-I/O	98	Vcc	Vcc
47	Vcc	Vcc	99	Vcc	Vcc
48	Vcc	Vcc	100	N/C	N/A
49	N/C	N/A	101	N/C	N/A
50	N/C	N/A	102	N/C	N/A
51	N/C	N/A	103	N/C	N/A
52	N/C	N/A	104	N/C	N/A

N/C = No user connections to these pins allowed.

TABLE 31. PINOUTS (CONTINUED)					
PQFP	BU-66318	SIGNAL TYPE	PQFP	BU-66318	SIGNAL TYPE
105	N/C	N/A	157	N/C	N/A
106	N/C	N/A	158	N/C	N/A
107	N/C	N/A	159	N/C	N/A
108	N/C	N/A	160	N/C	N/A
109	GND	GND	161	N/C	N/A
110	GND	GND	162	GND	GND
111	AD08	PCI-I/O	163	GND	GND
112	$\overline{\text{RDY4}}$	I	164	$\overline{\text{GNT}}$	I
113	$\overline{\text{INT5}}$	I	165	AD03	PCI-I/O
114	AD07	PCI-I/O	166	AD02	PCI-I/O
115	AD06	PCI-I/O	167	AD01	PCI-I/O
116	Vcc	Vcc	168	AD00	PCI-I/O
117	GND	GND	169	Vcc	Vcc
118	BUSMODE3#	I	170	Vcc	Vcc
119	$\overline{\text{RDY5}}$	I	171	GND	GND
120	$\overline{\text{INT2}}$	I	172	PCI_CLK_IN	PCI-I
121	AD05	PCI-I/O	173	GND	GND
122	$\overline{\text{RDY2}}$	I	174	BUSMODE1#	O
123	Vcc	Vcc	175	$\overline{\text{CS}}$	I
124	Vcc	Vcc	176	BUSMODE4#	I
125	GND	GND	177	$\overline{\text{SELECT5}}$	O
126	GND	GND	178	$\overline{\text{ACK}}$	O
127	A15	O	179	$\overline{\text{REQ}}$	O
128	A14	O	180	DB00	I/O
129	A13	O	181	DB01	I/O
130	A12	O	182	DB02	I/O
131	A11	O	183	DB03	I/O
132	A10	O	184	Vcc	Vcc
133	Vcc	Vcc	185	Vcc	Vcc
134	GND	GND	186	GND	GND
135	A09	O	187	GND	GND
136	A08	O	188	DB04	I/O
137	A07	O	189	DB05	I/O
138	A06	O	190	DB06	I/O
139	A05	O	191	DB07	I/O
140	A04	O	192	DB08	I/O
141	Vcc	Vcc	193	DB09	I/O
142	GND	GND	194	Vcc	Vcc
143	A03	O	195	GND	GND
144	A02	I/O	196	DB10	I/O
145	A01	I/O	197	DB11	I/O
146	A00	I/O	198	DB12	I/O
147	AD04	PCI-I/O	199	DB13	I/O
148	C/BE[0]#	PCI-I	200	DB14	I/O
149	$\overline{\text{SELECT4}}$	O	201	DB15	I/O
150	Vcc	Vcc	202	Vcc	Vcc
151	Vcc	Vcc	203	Vcc	Vcc
152	N/C	N/A	204	N/C	N/A
153	N/C	N/A	205	N/C	N/A
154	N/C	N/A	206	N/C	N/A
155	N/C	N/A	207	N/C	N/A
156	N/C	N/A	208	N/C	N/A

N/C = No user connections to these pins allowed.



Unless otherwise specified, dimensions are in inches (millimeters).

FIGURE 13. BU-66318 MECHANICAL OUTLINE

ORDERING INFORMATION

BU-66318 G 0 -1 1 0

- Test Criteria:
  0 = As per process
- Process Requirements:
  1 = MIL-PRF-38535 Compliant, Class N
- Temperature Grade/Data Requirements:
  1 = -55°C to +125°C
- Package Type:
  G = 208-Lead "Gull Wing" (Formed Lead) package
- Base Product Type:
  BU-66318 = ACE-Bridge

Note : The above products contain tin-lead solder finish as applicable to solder dip requirements.

STANDARD DDC PROCESSING FOR PLASTIC MONOLITHIC PRODUCTS		
TEST	**MIL-STD-883**	
	METHOD(S)	**CONDITION(S)**
INSPECTION / WORKMANSHIP	2017	—
ELECTRICAL TEST	DDC ATP	—

The information in this data sheet is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith.
Specifications are subject to change without notice.

Please visit our Web site at **www.ddc-web.com** for the latest information.

105 Wilbur Place, Bohemia, New York, U.S.A. 11716-2482

For Technical Support - 1-800-DDC-5757 ext. 7771

Headquarters, N.Y., U.S.A. - Tel: (631) 567-5600, Fax: (631) 567-7358
Southeast, U.S.A. - Tel: (703) 450-7900, Fax: (703) 450-6610
West Coast, U.S.A. - Tel: (714) 895-9777, Fax: (714) 895-4988
United Kingdom - Tel: +44-(0)1635-811140, Fax: +44-(0)1635-32264
Ireland - Tel: +353-21-341065, Fax: +353-21-341568
France - Tel: +33-(0)1-41-16-3424, Fax: +33-(0)1-41-16-3425
Germany - Tel: +49-(0) 89-150012-11, Fax: +49-(0) 89-150012-22
Japan - Tel: +81-(0)3-3814-7688, Fax: +81-(0)3-3814-7689
World Wide Web - http://www.ddc-web.com

DATA DEVICE CORPORATION
REGISTERED TO ISO 9001:2000
FILE NO. A5976

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP