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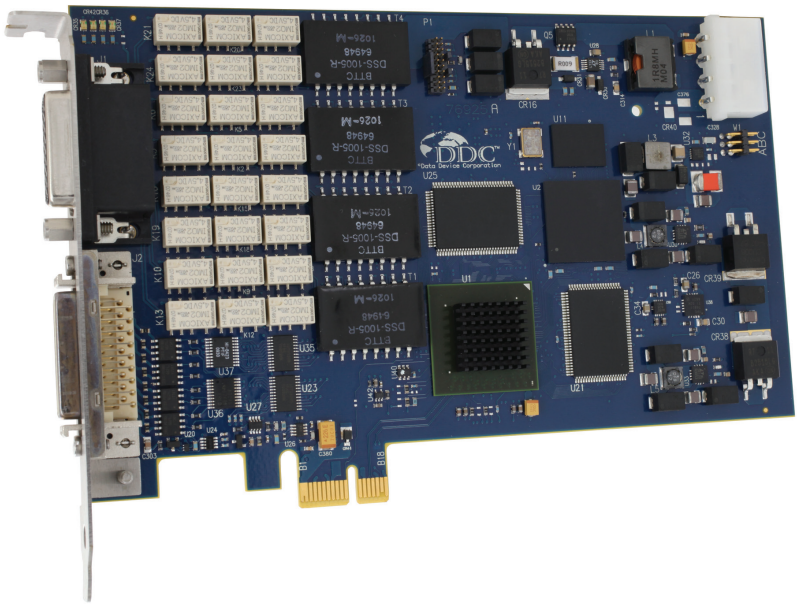
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MIL-STD-1553 PCI Express Card

Hardware Manual

Model: BU-67x06K



DDC's MIL-STD-1553 PCI-Express Card is designed with a one lane PCIe interface to be compatible with all PCIe slots in standard desktop computers. The combination of 1553 with digital and avionics Discrete I/Os offers flexibility that makes the card ideal for test applications.

Applications

- New Product Development
- Simulation
- Systems Integration
- Bus or Network Analysis
- Production Test
- System Troubleshooting
- Data Recording
- Automatic Test Applications (ATP)

Custom Design Capability - DDC can customize designs for all cards, ranging from simple modifications of standard products to fully customized solutions for commercial, military, aerospace, and industrial applications.

For more information: www.ddc-web.com/BU-62706K

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DDC's Data Networking Solutions

MIL-STD-1553 | ARINC 429 | Fibre Channel

As the leading global supplier of data bus components, cards, and software solutions for the military, commercial, and aerospace markets, DDC's data bus networking solutions encompass the full range of data interface protocols from MIL-STD-1553 and ARINC 429 to USB, and Fibre Channel, for applications utilizing a spectrum of form-factors including PMC, PCI, Compact PCI, PC/104, ISA, and VME/VXI.

DDC has developed its line of high-speed Fibre Channel and Extended 1553 products to support the real-time processing of field-critical data networking netween sensors, compute notes, data storage displays, and weapons for air, sea, and ground military vehicles.

Whether employed in increased bandwidth, high-speed serial communications, or traditional avionics and ground support applications, DDC's data solutions fufill the expanse of military requirements including reliability, determinism, low CPU utilization, real-time performance, and ruggedness within harsh environments. Out use of in-house intellectual property ensures superior mutli-generational support, independent of the life cycles of commercial devices. Moreover, we maintain software compatibility between product generations to protect our customers' investments in software development, system testing, and end-product qualification.

MIL-STD-1553

DDC provides an assortment of quality MIL-STD-1553 commercial, military, and COTS grade cards and components to meet your data conversion and data interface needs. DDC supplies MIL-STD-1553 board level products in a variety of form factors including AMC, USB, PCI, cPCI, PCI-104, PCMCIA, PMC, PC/104, PC/104-Plus, VME/VXI, and ISAbus cards. Our 1553 data bus board solutions are integral elements of military, aerospace, and industrial applications. Our extensive line of military and space grade components provide MIL-STD-1553 interface solutions for microprocessors, PCI buses, and simple systems. Our 1553 data bus solutions are designed into a global network of aircraft, helicopter, and missle programs.

ARINC 429

DDC also has a wide assortment of quality ARINC-429 commercial, military, and COTS grade cards and components, which will meet your data conversion and data interface needs. DDC supplies ARINC-429 board level products in a variety of form factors including AMC, USB, PCI, PMC, PCI-104, PC/104 Plus, and PCMCIA boards. DDC's ARINC 429 components ensure the accurate and reliable transfer of flight-critical data. Our 429 interfaces support data bus development, validation, and the transfer of flight-critical data aboard commercial aerospace platforms.

Fibre Channel

DDC has developed its line of high-speed Fibre Channel network access controllers and switches to support the real-time processing demands of field-critical data networking between sensors, computer nodes, data storage, displays, and weapons, for air, sea, and ground military vehicles. Fibre Channel's architecture is optimized to meet the performance,reliability, and demanding environmental requirements of embedded, real time, military applications, and designed to endure the multi-decade life cycle demands of military/aerospace programs.



BU-67X06K FOUR-CHANNEL MIL-STD-1553 INTERFACE PCI EXPRESS CARD HARDWARE MANUAL

MN-67106KX-001

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Revision	Date	Pages	Description
A	Jan., 2009	All	Preliminary
B	March 2009	6 – 11	Removed non-existant part number in table 1.
C	Aug., 2009	20	Edited Pins 12, 31, 33, 34, 25, 28, 10, & 30 in Table 4.
D	Feb., 2010	17, 18	Update to pinout information. Figure 4 added. Manual placed in updated format.
E	Aug., 2010	All	Added the BU-67206K Multi-Function Version Information throughout the document.
F	Oct, 2010	6 21	removed section 2.6.1 Added description of variable voltage transceivers
G	Feb, 2011	38	In section 5.10.4.4, p. 38, changed "IRIG Standard 106-04" to "IRIG Standard 200-04"
H	March, 2012	34	Update to Figure 8
J	Oct, 2012	35	update to Figure 8
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1 PREFACE

This manual uses typographical conventions to assist the reader in understanding the content. This section will define the text formatting used in the rest of the manual

1.1 Text Usage

- **BOLD**–indicates important information and table, figure, and chapter references.
- ***BOLD ITALIC***–designates DDC Part Numbers.
- `Courier New`–indicates code examples.
- <…> - indicates user-entered text or commands.

1.2 Special Handling and Cautions

The ***BU-67x06K*** uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.



Warnings: Turn off power to the computer hardware and unplug from wall.

NEVER insert or remove card with power turned on.

Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.

Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

1.3 Trademarks

All trademarks are the property of their respective owners.

1.4 What is included in this manual?

This manual contains a complete description of hardware installation and use.

1.5 Technical Support

In the event that problems arise beyond the scope of this manual, you can contact DDC by the following:

US Toll Free Technical Support:
1-800-DDC-5757, ext. 7771

Outside of the US Technical Support:
1-631-567-5600, ext. 7771

Fax:
1-631-567-5758 to the attention of DATA BUS Applications

DDC Website:
www.ddc-web.com/ContactUs/TechSupport.aspx

Please note that the latest revisions of Software and Documentation are available for download at DDC's Web Site, www.ddc-web.com.

2 OVERVIEW

The ***BU-67x06K*** is a half-length PCI Express x1 card supporting one to four dual redundant MIL-STD-1553 channels. This form factor is designed for use in standard desktops or servers that provide a standard height PCI Express slot. The PCI Express specifications require interoperability of the X1 card in any link width PCIe slot (x1, x4, x8 or x16) and any current PCI Express generation (1.0a/1.1/2.0).

The operating temperature range for these environments is 0°C to +55°C with air exchange inside the enclosure. All customer I/O is made via two connectors on the standard I/O bracket.

The design of the ***BU-67x06K*** leverages the full capabilities of DDC's new ***AceXtreme***™ Architecture. Features include a highly autonomous bus controller with expanded instruction set, an RT providing a wide variety of buffering options, a selective message monitor that allows you to store data in an industry standard IRIG-106 Chapter 10 format, 48-bit 100 nanosecond resolution IRIG-B time code inputs and 48-bit 100 nanosecond resolution Time Tag for each MIL-STD-1553 channel. Each ***AceXtreme*** channel contains 512K X 36 (2MB w/parity) of RAM to allow for storage of 1553 messages.

The ***BU-67206K*** adds the Multi-Function ***AceXtreme*** architecture, allowing numerous additional test features.

The AceXtreme architecture is backwards compatible with the industry standard, field proven, Enhanced Mini-ACE software and is supported by the ***BU-69092SX AceXtreme C Software Development Kit (SDK)***, along with source code samples, and detailed documentation.

2.1 Features

- Half Length, Standard Height PCI Express x1 Form Factor
- Each channel can be independently programmed for BC, Multi-RT, Monitor or true Multi-RT/Monitor
- Programmable BC operation
- Transformer-coupled or direct-coupled bus connection via software control
- 1553 bus can be terminated on-board via software control
- 512K X 36 RAM (2MB) per 1553 channel
- Up to Four Dual Redundant 1553 Channels
- Eight User-Programmable Digital Discrete I/Os

- Eight User-Programmable Avionics (28V) Discrete I/Os
- 48-bit / 100ns Time Stamp
- External Time-Tag Clock Input/Output
- IRIG-B Input/Output
- IRIG-106 Chapter 10 Monitor Format
- DMA Engine for Low CPU Utilization
    - ***BU-67x06K*** uses this in MT-I mode
- ***AceXtreme***™ BC/Multi-RT/MT Architecture
    - Optional Multi-Function availability
- API Compatible with ***Enhanced Mini-ACE® Plus SDK***
- Built-In Self Test
- Windows® 2000/XP/Vista/7, Linux® and VxWorks®

Additional Test and Simulation features included on the *BU-67206K* (Multi-Function):

- Each 1553 channel can run the BC, RTs and MT concurrently
- Programmable RT Response Times
- Programmable Response Timeout
- Intermessage Routines
- Programmable Intermessage Gap
- Advanced Error Monitor
- Error injection
- Triggers
- Dynamic Bus Control
- Replay Function

Applications Include:

- New Product Development
- Simulation
- Systems Integration
- Bus or Network Analysis
- Production Test
- System Troubleshooting

- Data Recording
- Automatic Test Applications (ATP)

The ***BU-67x06K*** is supported by the ***BU-69092S*** MIL-STD-1553 ***AceXtreme C Software Development Kit (SDK)***. The SDK includes a high-level C Library that allows the application programmer to set up the device in any operating mode without any underlying knowledge of how the hardware works. A device driver for Windows 2000/XP/Vista/7 is included. Operating system specific device drivers will be available for Linux for both x86 and Power PC based host computers. Please contact the factory for Linux driver availability.

2.2 Standard I/O Features

The ***BU-67x06K*** card's standard I/O features include 8 digital discrete I/O, eight avionics discrete I/O, IRIG-B time code inputs (AM or PWM), external clock input with enable, and 10 MHz clock output along with numerous software configurable register options.

2.3 MIL-STD-1553 Features

The ***BU-67x06K*** implements up to 4 MIL-STD-1553 channels utilizing the DDC AceXtreme Architecture. Each 1553 channel can be independently programmed for BC, Multi-RT, Monitor or true Multi-RT/Monitor and is configured with 2MB of onboard RAM per installed channel.

Each MIL-STD-1553 interface implements a transformer-coupled or direct-coupled dual-redundant bus connection (software selectable). Each connection utilizes separate Harris Interface type 1553 transceivers to achieve true redundancy.

2.4 System Requirements

"Standard" desktop or server PC with a full height PCIe 1.0/1/2.0 compatible slot. A supported operating system.

2.5 Applications

The design of the ***BU-67x06K*** leverages the full capabilities of DDC's AceXtreme Architecture. Features include a highly autonomous BC with expanded instruction set, an RT providing a wide variety of buffering options, a selective message monitor, 48-bit, 100 nanosecond resolution IRIG-B time code inputs and 48-bit, 100 nanosecond resolution Time Tag. Each AceXtreme channel contains 1MB of parity-protected RAM.

2.6 Mechanical Design

The card is designed for a standard height, non-rugged, non-extended temperature PCI Express environment.

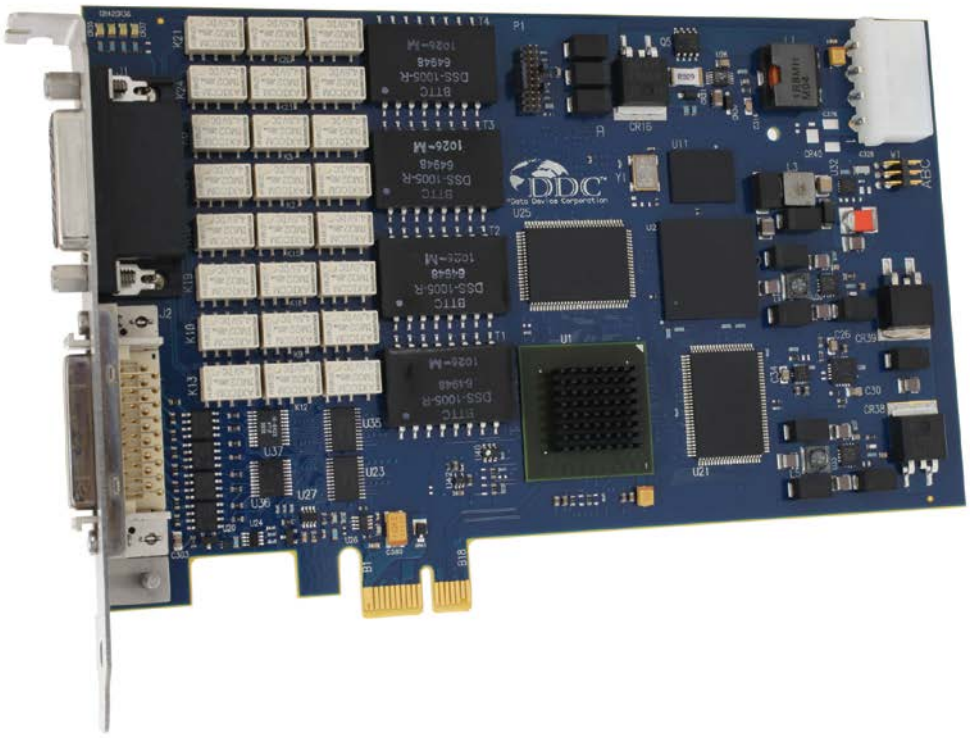


Figure 1. BU-67x06K PCI Express x1 Four-Channel 1553 Interface Card

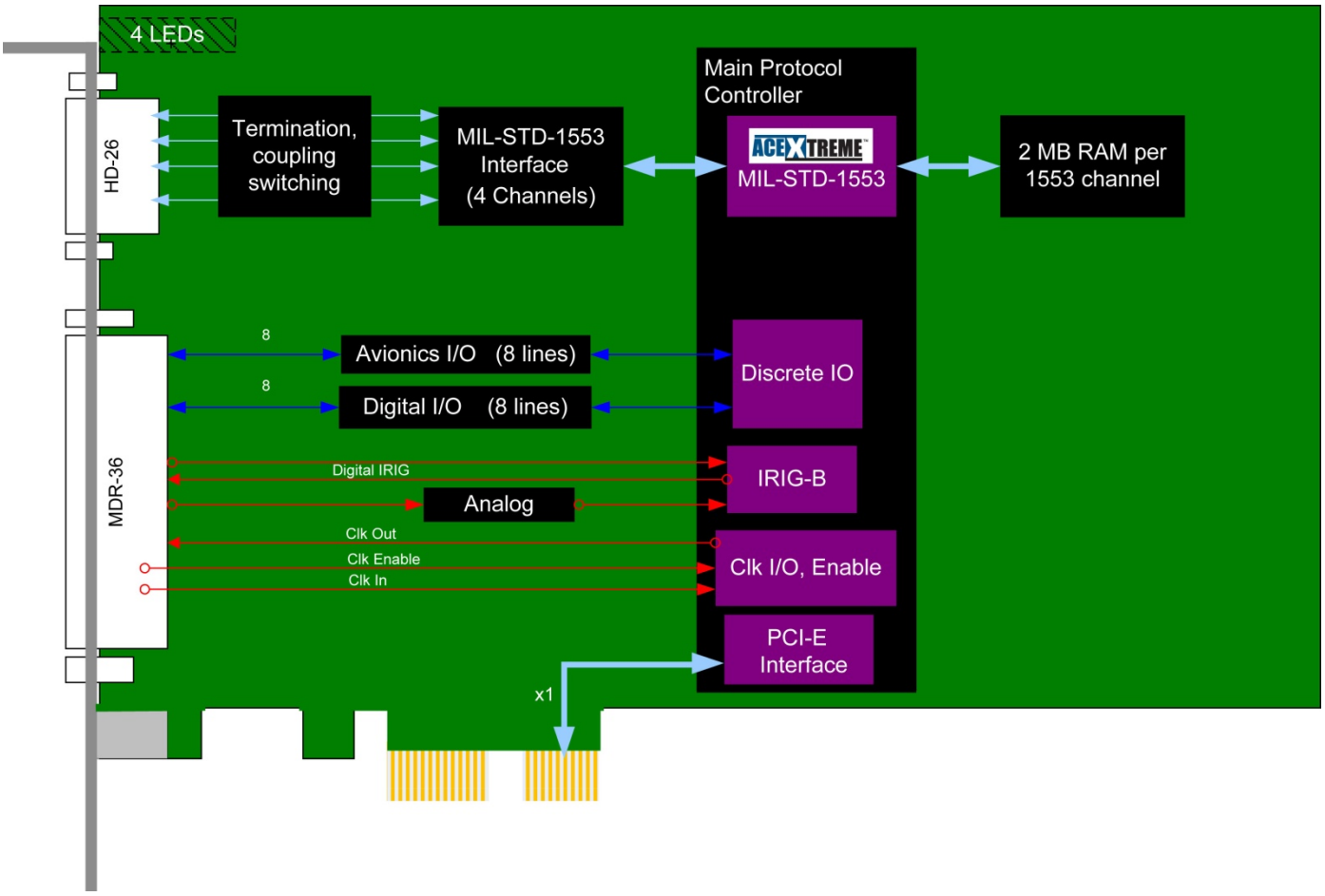


Figure 2. BU-67x06K Architecture

2.7 Card Specifications

Table 1. BU-67x06K SPECIFICATION TABLE

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATING				
Supply Voltage (PCIe)				
+3.3 V	0		5.5	V
+12.0 V	0		18	V
Supply Voltage (Aux)				
+5.0 V	0		6.5	V
I/O Voltages				
Avionics I/O	0		35	V
Digital I/O	0		5	V
Analog IRIG			12	Vpp

Table 1. BU-67x06K SPECIFICATION TABLE				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances (per PCIe CEM)				
+3.3 V	3.003	3.3	3.597	V
+12 V	11.04	12.0	12.96	V
Voltages/Tolerances (per Intel PS DG Rev 1.1, +12 V unused)				
Aux Connector Voltage	4.75	5.0	5.25	V
• One channel current draws (***BU-67x06K100***)				
•MIL-STD-1553				
+12V current (Note 10)				
Idle		150		mA
25% Transmitter Duty Cycle		150		mA
50% Transmitter Duty Cycle		150		mA
100% Transmitter Duty Cycle		150		mA
+3.3V current (Note 10)				
Idle		440		mA
25% Transmitter Duty Cycle		725		mA
50% Transmitter Duty Cycle		1.00		A
100% Transmitter Duty Cycle		1.5		A
• Two channel current draws (***BU-67x06K200***)				
•MIL-STD-1553				
+12V current (Note 10)				
Idle		150		mA
25% Transmitter Duty Cycle		150		mA
50% Transmitter Duty Cycle		150		mA
100% Transmitter Duty Cycle		150		mA
+3.3V current (Note 10)				
Idle		460		mA
25% Transmitter Duty Cycle		1.25		A
50% Transmitter Duty Cycle		1.60		A
100% Transmitter Duty Cycle		2.70		A

Table 1. BU-67x06K SPECIFICATION TABLE				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLY REQUIREMENTS (Cont'd)				
• Four channel current draws (***BU-67x06K400*** with all channels operating)				
•MIL-STD-1553				
+12V current (Note 10)				
Idle		160		mA
25% Transmitter Duty Cycle		160		mA
50% Transmitter Duty Cycle		160		mA
100% Transmitter Duty Cycle		160		mA
+3.3V current (Note 10)				
Idle		500		mA
25% Transmitter Duty Cycle		500		mA
50% Transmitter Duty Cycle		500		mA
100% Transmitter Duty Cycle		500		mA
+5.0V aux current (Note 10)				
Idle		100		mA
25% Transmitter Duty Cycle		800		mA
50% Transmitter Duty Cycle		1.50		A
100% Transmitter Duty Cycle		2.90		A
POWER DISSIPATION On Board (Note 9)				
• One Channel (***BU-67x06K100***)				
Idle		3.25		W
25% Transmitter Duty Cycle		3.90		W
50% Transmitter Duty Cycle		4.50		W
100% Transmitter Duty Cycle		6.60		W
• Two Channel (***BU-67x06K200***)				
Idle		3.30		W
25% Transmitter Duty Cycle		5.40		W
50% Transmitter Duty Cycle		5.90		W
100% Transmitter Duty Cycle		8.40		W
• Four Channel (***BU-67x06K400*** with all channels operating)				
Idle		4.10		W
25% Transmitter Duty Cycle		6.40		W
50% Transmitter Duty Cycle		8.70		W
100% Transmitter Duty Cycle		13.30		W

Table 1. BU-67x06K SPECIFICATION TABLE				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL LOGIC (DIO & AIO)				
V_{IH}				
DIO	2.0		5.0	V
AIO	4.0		35.0	V
V_{IL}				
DIO			0.8	V
AIO			3.0	V
I_{IH}, I_{IL}				
DIO I_{IH}	-130		+200	µA
DIO I_{IL}	-330			µA
AIO I_{IH}			5	mA
AIO I_{IL}	-100			µA
V_{OH}				
DIO V_{OH} (I_{OH}=max)	2.4			V
V_{OL}				
DIO V_{OL} (I_{OL}=max)			0.4	V
AIO V_{OL} (I_{OL}=max)			0.5	V
I_{OL}, I_{OH}				
DIO I_{OL}	+12			mA
DIO I_{OH}	-12			mA
AIO I_{OL}			0.5	A
AIO I_{OH} (V_{IH}= AIO Max)			5	mA
MIL-STD-1553 RECEIVER				
Input Impedance, Transformer Coupled (Notes 1-3)	1.000			Kohm
Threshold Voltage, Transformer Coupled	0.200		0.860	Vp-p
Common-Mode Voltage (Note 4)			10	Vpeak
MIL-STD-1553 TRANSMITTER				
Differential Output Voltage, Transformer Coupled Across 70 Ohm				
• ***BU-67106K***	19	20.5	27	Vp-p
• ***BU-67206K*** (Programmable Range)	0		20.5	Vp-p
(Maximum Setting Tolerance)	19	20.5	27	Vp-p
Output Offset Voltage, Transformer Coupled Across 70 Ohm	-250	150	250	mVpeak
Rise/Fall Time	100	150	300	ns

Table 1. BU-67x06K SPECIFICATION TABLE				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG IRIG INPUT RANGES				
Hi Range	2.5		10	Vpp
Lo Range	0.2		2.5	Vpp
MIL-STD-1553 MESSAGE TIMING				
BC Intermessage Gap				
• ***BU-67106K*** (Note 5)	7	10.1	65536	µs
MIL-STD-1553 MESSAGE TIMING (Cont'd)				
• ***BU-67206K*** (Programmable, See Note 7)	3.5		32000	µs
BC/RT/MT Response Timeout (Note 8)				
• ***BU-67106K*** (Programmable, See Note 6)	17.5		131	µs
• ***BU-67206K*** (Programmable, See Note 7)	3.5		30	µs
RT Response Time				
• ***BU-67106K***	4		7	µs
• ***BU-67206K*** (Programmable, See Note 7)	3.5		30	µs
Transmitter Watchdog Timeout		660.5		µs
THERMAL				
Card Operating Temperature				
• ***BU-67x06K*** w/air exchange in case	0		+55	°C
Storage Temperature				
• ***BU-67x06K***	-45		+85	°C
FORM FACTOR/SPECIFICATION	PCIe CEM 1.1 (Standard height, Half length, PCI Express x1)			
PHYSICAL CHARACTERISTICS				
PCB Size (Full height, half length per CEM 1.1)	4.376 H X 6.6 L (111.15 x 167.65)			in. (mm)
Weight				
• ***BU-67x06K100*** (one channel)	4.8 (139)			oz. (g)
• ***BU-67x06K200*** (two channel)	5.0 (146)			oz. (g)
• ***BU-67x06K400*** (four channel)	6.0 (171)			oz. (g)

Table 1. BU-67x06K SPECIFICATION TABLE				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**

Notes For TABLE 1:
(Notes 1 through 3 are applicable to the input Impedance specification)

1. The specifications are applicable for both unpowered and powered conditions.
2. The specifications assume a 2 Volt rms balanced, differential, sinusoidal input. The applicable frequency is 75 kHz to 1 MHz.
3. Minimum impedance is guaranteed over the operating range, but is not tested.
4. Assumes a common mode voltage within the frequency range of DC to 2MHz, applied to pins of the isolation transformer on the stub side (transformer coupled), and referenced to signal.
5. Typical value for minimum intermessage gap time. Under software control, this may be lengthened to 65, 535 ms. If ENHANCED CPU ACCESS, bit 14 of Configuration Register #6, is set to logic “1”, then host accesses during BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences could have the effect of lengthening the intermessage gap time. For each host access during an SOM or EOM sequence, the intermessage gap time will be lengthened by 6 clock cycles. Since there are 7 internal transfers during SOM, and 5 during EOM, this could theoretically lengthen the intermessage gap by up to 72 clock cycles; i.e., 4.5 µs.
6. Software programmable (4 options: 18.5µs, 22.5µs, 50.5µs, 128µs) includes RT-to-RT Timeout (measure mid parity of transmit Command Word to mid-sync of Transmitting RT Status Word).
7. In ½ µsecond increments.
8. Measured from mid-parity crossing of Command Word to mid-sync crossing of RT’s Status Word.
9. Current drain and power dissipation specifications are preliminary and subject to change. All power measurements assume transformer-coupled configuration with external bus termination resistors.
10. All power measurements were taken over the PCIe CEM voltage range with the PCIe x1 bus.

3 HARDWARE INSTALLATION

The ***BU-67x06K*** card is a PCI Express x1 1.0a compliant card that can be inserted in any standard height PCI Express 1.0a/1.1/2.0 compliant slot.

When installing the card, the following should be observed:

- **NEVER** insert or remove the card with the power turned on.
- **ALWAYS** take proper precautions to guard against static damage.
- Use a wrist strap if available, or ensure proper static grounding by touching the power supply cover **WITH POWER OFF**.
- If the card is a ***BU-67x06K400***, it might be more convenient to connect the aux power connector first. See Section 5.10.1 regarding this connector.
- If the card is not in its factory configuration, please check the jumpers listed in Section 5.9.1.
- Insert the card and gently press into the PCI Express mating connector. Secure the rear I/O panel with the proper hardware.
- Make sure that adjacent cabling and wiring do not hinder the airflow around the card.

The card is a true Plug and Play device. Interrupts and memory selections will be performed by the operating system as the boot system progresses.

4 SOFTWARE INSTALLATION

Numerous software packages are available for the ***BU-67x06K***. The DDC software packages are developed to allow shorter design cycles while allowing all ***BU-67x06K*** functionality to be accessed by user level code.

The following Software packages are available from DDC to operate with this device:

- AceXtreme SDK (BU-69092Sx)
- BusTracer MIL-STD-1553 Graphical Monitor/Generator (BU-69066)
- LabView Support Package for MIL-STD-1553 and ARINC-429 (BU-69093)
- dataSims Avionics Data Bus Test and Analysis (BU-69414)

4.1 1553 Software (BU-69092Sx) Overview

The AceXtreme SDK (BU-69092Sx) package includes:

- MIL-STD-1553 API Library (BU-69092Sx)
- AceXtreme FLASH Utility
- Device Drivers (included in the BU-69092Sx MIL-STD-1553 package)

The card is supplied with the ***BU-69092S*** MIL-STD-1553 ***AceXtreme C Software Development Kit (SDK)***, with versions available for multiple OS configurations. This software development kit includes a runtime library that provides the user with a hardware abstraction layer for the DDC 1553 hardware. This software layer includes routines that dramatically reduce software development time by providing high level C functions for the application programmer to interface to the ***BU-67x06K*** card. Demo programs are included with the library to demonstrate the capabilities of the card in each mode. The ***BU-69092S*** software manual can be downloaded from the DDC web site at www.ddc-web.com.

Table 2. MIL-STD-1553 AceXtreme C SDK Part Number Descriptions

MIL-STD-1553 AceXtreme C SDK Part Number	Description	Requirements
BU-69092S0	32/64-Bit Library and Device Drivers for Windows	Windows 2000/XP/Vista/7
BU-69092S1 (contact factory for availability)	32/64-Bit Library and Device Drivers for Linux	Linux Kernel versions 2.6.x
BU-69092S2	32-Bit Library and Device Drivers for WindRiver VxWorks	WindRiver VxWorks® versions 6.x
* Contact Factory for other Operating Systems		

Additional software tools available include a Flash Utility. Documentation for this tool can be found on our web site under Generic Documentation in the Library section of our web site at www.ddc-web.com.

4.1.1 Windows (BU-69092S0)

Software installation is performed by InstallShield®. This install script will make all necessary registry modifications and will create the required directory structures. A Windows 2000/XP/Vista/7 operating system specific driver is installed, along with the high-level C library functions and all supplied demos.

4.1.2 Linux (BU-69092S1)

The SDK for Linux includes a Linux specific loadable module driver and source code so that the user can compile it against a specific version of the Linux kernel. The driver was developed and tested with Linux kernel version 2.6.z. Installation instructions are included in the ***BU-69092S1*** software package.

4.1.3 VxWorks (BU-69092S2)

The SDK for VxWorks is supplied as a single driver/library. Files can be linked to the VxWorks Kernel with a full rebuild of the kernel, or it can be built as a downloadable module that is loaded and unloaded by the user.

Extracting the ZIP file using an appropriate utility performs the installation of the software, which can then be used with the WindRiver Workbench IDE.

4.2 Testing the Installation

Once the hardware and software is installed, the user can test the installation by running one of the sample programs that is shipped with the software. Follow the steps below to test the installation.

4.2.1 Testing the Software Installation

Run the Tester.exe program. This program requires a logical device number (LDN) also referred to as the channel. A 0 indicates that the hardware is defined as 0 in the DDC CARD MANAGER. This parameter will be entered as required per the installation. If you have more than one device installed in the system, then running Tester with the appropriate parameter, 0, 1, 2 or 3 should test each of the channels or cards individually.

If all elements of the test passed, the 1553 card/software is ready for use. Note that some functions may not be supported in newer hardware and you may see a

message that the function is not supported. This test is left in the tester code for legacy cards.

If one or more elements did not pass, refer to the section below on Troubleshooting the Installation.

4.2.2 Troubleshooting the Installation

Usually the installation will be successful, and the self-test will pass. There are, however, some situations that can cause problems during the installation. The most common are detailed below.

An error is returned when an attempt is made to run the SELFTEST or any of the other sample programs. This fault is almost always related to an incorrectly assigned device number. Be sure that a device number was correctly assigned through the DDC Card Manager.

If an error is encountered and the device number appears to be correctly assigned, check the operating system resources to verify that the card has been given a valid memory region by the operating system. Errors have sometimes been observed in Windows 2000 or Windows XP operating systems. The BIOS setting for a PnP operating system is sometimes set to YES, which can cause a problem. This BIOS option was originally created by manufacturers to distinguish between Windows NT and Windows 9x based operating systems. Since Windows 2000 and Windows XP are extensions of the Windows NT kernel this BIOS option must be set for NO under these operating systems. The operating system, as well as all hardware on your system, will still maintain PnP compatibility; it will not be necessary to manually configure resources for PnP cards.

4.3 Updating the Flash Firmware

Detailed instructions on using the DDC Card Manager to update the firmware on the **BU-67x06K** can be found in the ***E²MA/AceXtreme*** Flash Utility Instructions available for download from DDC's BU-67X06K product web page (Direct document link – http://www.ddc-web.com/Pub/194/446.ashx).

To update the Flash, the user will need to install a shunt on the "Flash Write Enable" jumper (Figure 7) or drive the FLASH_WRITE_EN_L signal low (Table 6).

5 DETAILED DESIGN AND ARCHITECTURE

5.1 Hardware Configuration and Operation

The ***BU-67x06K*** card is a PCIe device, and as such does not require any jumpers or switches to set the Base address or interrupt values. The job of configuration for Plug-and-Play PCIe is performed by the operating system.

During the initial power on boot process, the system performs an enumeration of the PCIe bus and allocates a resource configuration that satisfies the card requirements. The system will save the configuration information in the ***BU-67x06K's*** PCI configuration space registers. These registers are configured at the factory to contain information that identifies the card type, vendor, required memory sizes, and interrupt resources.

When the driver loads it will access the configuration registers and identify how the system has configured the card. After identifying each of the installed cards, the device driver will enumerate each of the channels on the card and create a configuration structure that defines the allocated address and interrupt. This information is directly available to the MIL-STD-1553 ***AceXtreme C Software Development Kit*** and is necessary for read, write and interrupt operations. The end user does not need to know this information if using one of the supplied C API libraries to operate the card.

5.2 PCI/PCIe Interface

The card natively supports PCI Express CEM 1.1.

The PCI endpoint in the ***BU-67x06K*** is PCI 2.2 compliant. The PCI interface on the cards contains a set of "Type 00h" PCI configuration registers that are used to map the device into the host system.

When using the card with the supplied ***BU-69092S*** MIL-STD-1553 ***AceXtreme C Software Development Kit (SDK)*** and drivers there is no need to reference the PCI configuration registers. These registers are listed in Appendix A for reference.

There are four Base Address Registers (BARs) used by this card. All BAR mapping is located in PCI configuration register space.

- BAR 0 is 512-bytes long and is used for PCI control registers
- BAR 1 is 256-bytes long and is used for PCI control registers

- BAR 2 is 8-Mbytes long and is used for 1553 RAM of all available channels
- BAR 3 is 8-Kbytes long and is dedicated to 1553 registers

5.2.1 Interrupts

The card may issue interrupt requests over the PCIe bus via “virtual wire” interrupt messages or Message Signal Interrupts (MSI). The interrupts from each of the channels are functionally OR’d together to provide a single interrupt. The operations to be taken during the interrupt cycle will be determined by both the device driver requirements and a service routine that is specified by the user application. The device driver will determine which of the channels on the card generated the interrupt, read the interrupt status registers and queue, transfer this information to an interrupt structure and then signal the appropriate application that the interrupt occurred. The ***AceXtreme*** library provides the necessary routines for generating user Interrupt Service Routines and hooking them into the device driver.

5.2.2 DMA Design

The card’s Direct Memory Access (DMA) engine is host initiated via the AceXtreme library.

The AceXtreme library (Host) will initiate the DMA transfer by writing to the PCI controller on the card.

The Card will issue an interrupt once a DMA transfer has been completed.

The AceXtreme library will implement a round robin scheduling mechanism in order to arbitrate the one DMA channel over the 1553 channels. A software DMA work queue may be implemented in order to adhere to this scheduling mechanism.

5.2.3 Register & Memory Addressing

The ***BU-67x06K*** PCI interface contains a set of "Type 00h" PCI configuration registers that are used to map the device into the host system. The configuration register space is mapped in accordance with PCI Revision 2.2 specifications. These registers are arranged such that all memory and register space may be addressed through a single PCI function.

Configuration registers implement the Subsystem Vendor and Device ID, and control the Fail-Safe operation of the device. There are four Base Address

Registers (BAR) used on the design of this card. All BAR mapping is located in PCI configuration register space.

When using the card with the BU-69092Sx API Library and drivers, the details of these registers and memory addresses are abstracted from the user to provide an easy-to-use High Level “C” programming environment.

5.3 1553 Architecture

5.3.1 Combination Modes

The ***BU-67106K*** Single-Function AceXtreme architecture has the ability to run the following concurrent modes:

(1) BC and MT-I

(2) RT and MT-I

(3) RT and MT

(4) Multi-RT and MT-I

The ***BU-67206K*** Multi-Function AceXtreme architecture has the ability to run the BC, Multi-RT, and MT-I modes concurrently on a single 1553 channel. Any combination of these modes is supported. By running more than one mode at one time, the user can have a variety of information and features readily available. Each channel’s mode is configurable through software.

5.3.2 Bus Controller (BC) Architecture

The AceXtreme BC mode offers several new powerful architectural features. This includes the incorporation of a highly autonomous BC message sequence control engine, which greatly serves to offload the operation of the host CPU. This can be a critical factor in embedded systems with real time requirements.

The Enhanced BC's message sequence control engine provides a high degree of flexibility for:

- Implementing major and minor frame scheduling
- Inserting asynchronous messages in the middle of a frame
- Separating 1553 message data from control/status data for the purpose of implementing double buffering and performing bulk data transfers

- Implementing message retry schemes, including the capability for automatic bus channel switchover for failed messages
- Reporting various conditions to the host processor by means of user defined interrupts and a general purpose queue
- Dynamic BC message and frame modification

The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type, sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. In the Enhanced BC mode, there is no explicit limit to the number of messages that may be processed in a frame.

The Multi-Function AceXtreme BC (***BU-67206K*** option) provides additional features with the Test and Simulation Toolkit (See section 5.4.1):

5.3.2.1 BC Programmable Message Timing

The AceXtreme Architecture provides the capability of programming the time to next message through software. The time to next message defines the time from the start of the current message to the start of the subsequent message as shown in Figure 3 below. However, the uncertainty of the RT's response can cause the gap time interval between the end of the message and the beginning of the following message to vary.

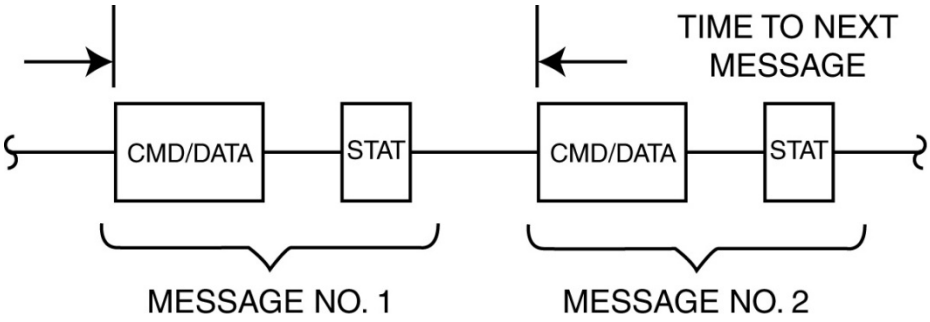


Figure 3. Time To Next Message

The Test and Simulation toolkit also allows an additional timing mode, which is useful in cases where high-accuracy and violating the 1553 minimums is required. Please see section 5.4.1.3 for further information on this mode.

5.3.3 Multiple Remote Terminal (Multi-RT) Architecture

The ***AceXtreme*** provides the capability of implementing up to 31 RTs on a single channel of the ***BU-67x06K*** device. The Multi-RT architecture provides multi-protocol support, with full compliance to all of the commonly used data bus standards, including MIL-STD-1553A, MIL-STD-1553B (Notice 2), and is compatible with MIL-STD-1760. Programmable flexibility enables the RT to be configured to fulfill any set of system requirements. This includes the capability to meet the MIL-STD-1553A response time requirement of 2μs to 5μs, and multiple options for mode code subaddresses, mode codes, RT status word, and RT BIT word.

The ***AceXtreme*** RT protocol design implements all of the MIL-STD-1553B message formats and dual redundant mode codes. The design has passed validation testing for MIL-STD-1553B compliance. The ***AceXtreme*** RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. One of the main features of the ***AceXtreme*** RT is its choice of memory management options. These include single buffering by subaddress, double buffering for individual receive subaddresses, circular buffering by individual subaddresses, and global circular buffering for multiple (or all) subaddresses.

The ***AceXtreme*** RT provides an internal mechanism for RT Command Word illegalizing. The design of the ***BU-67x06K*** supports different options for specifying the RT addresses for the individual channels (See section 5.3.6). In all configurations, the RT address is readable by the host processor.

The Multi-Function ***AceXtreme*** RT (***BU-67206K*** option) provides additional features with the Test and Simulation Toolkit (See section 5.4.2)

5.3.4 Monitor (MT) Architecture

The Multi-Function ***AceXtreme*** Architecture includes a native MIL-STD-1553 Monitor (MT-I). The MT natively operates as an IRIG-106 Chapter 10 monitor. It can also be configured with the following options:

1. Message Error Capture (MEC) see section 5.3.4.2
2. Advanced Error Sampling (AES) (Multi-Function Only) see section 5.4.3

Triggers can also be used to start/stop Monitor operation and automatically insert mark indicators into MT-I packets. (See section 5.4.5)

5.3.4.1 IRIG-106 Chapter 10 Monitor (MT-I)

The IRIG-106 Chapter 10 Monitor (MT-I) provides a definitive solution for systems requiring IRIG-106 Chapter 10 support. In addition, MT-I mode adds DMA support, flexible event notification, and performance enhancements to maximize monitor data throughput.

IRIG-106 is a comprehensive standard developed to ensure interoperability in aeronautical telemetry applications. IRIG-106 is developed and maintained by the Telemetry Group of the Range Commanders Council. Chapter 10 addresses the Digital On-board Recorder Standard, which defines the operation and interfaces for digital flight data recorders. This new file format standard supports MIL-STD-1553, as well as other telemetry protocols such as PCM and ARINC 429.

The MT-I Monitor creates IRIG-106 Chapter 10 data packets, including a packet header and trailer, containing any monitored 1553 traffic (after filter is applied). The MT-I data packet is compliant to MIL-STD-1553, Format 1.

5.3.4.2 Message Error Capture (MEC)

IRIG-106 Chapter 10 defines that the data for messages with errors is not be stored. In certain cases for debug and analysis of MIL-STD-1553 buses, the error data may be required to be stored. With MEC enabled in the MT-I, the monitor will store the data from multiple message errors including the following:

1. Word Count Error
2. No Response
3. Gap Time Error

5.3.5 1553 Transceivers

Every ***AceXtreme*** 1553 channel provides complete multi-protocol support of MIL-STD-1553A/B and STANAG 3838, with voltage source transceivers for improved line driving capability. The ***BU-67x06K*** transceivers are compatible with MIL-STD-1760. The receiver sections of each ***AceXtreme*** 1553 channel are fully compliant with MIL-STD-1553B Notice 2 in terms of front-end overvoltage protection, threshold, common-mode rejection, and word error rate.

The ***BU-67206K*** adds the ability to set the differential output voltage for the 1553 transceivers. The voltage can be set in 1024 steps from 0 to a nominal setting of 20.5 V. Settings are controlled independently per channel, but both transceivers on a given channel will be set to the same level.

5.3.6 RT Address Selection

RT addresses for each 1553 channel are set via software.

The ***AceXtreme*** "C" API library abstracts all individual register and memory operations from the application programmer to make card programming a simple task. To set the RT address with the ***AceXtreme*** "C" API library, simply call the aceRTSetAddress() function. All of the functions in the ***AceXtreme*** API library are described in complete detail in the ***AceXtreme*** Runtime Library Software Manual.

5.3.7 MIL-STD-1553 Time Tag

The architecture includes an internal MIL-STD-1553 read/write Time Tag Register. This register is a CPU read/write 48-bit counter capable of 100 nanoseconds (10 MHz) resolution. Another option allows software-controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register. The clock source of the counter, either external or internal, is also under software control. See the **aceSetTimeTagRes()** function in the ***AceXtreme C SDK*** software manual for detailed information on selecting the clock source, resolution and test mode of the counter.

For each message processed, the value of the Time Tag Register is loaded into the second location of the respective descriptor stack entry ("TIME TAG 48-bit WORD") for both the BC and RT modes.

In addition, the time tag register can be incremented by an external input, allowing use of a customer provided time base. Use of the external clock input allows resolutions down to 100ns (10 MHz external), allowing implementation of IRIG-106 relative time stamps. A Clock Enable input pin allows resetting of the timestamp register. The clock can also be driven onto an output pin.

Furthermore, the card supports IRIG-B inputs, both analog and digital, and a digital IRIG-B output. The analog IRIG-B has a software selectable range to support a wide range of input levels.

The functionality involving the Time Tag Register includes the capability to issue an interrupt request and set a bit in the Interrupt Status Register when the Time Tag Register rolls over from 0xFFFF FFFF FFFF to 0x0000 0000 0000. RT mode has the capability to automatically clear the Time Tag Register following reception of a Synchronize (without data) mode command, or to load the Time Tag Register following a Synchronize (with data) mode command.

Additional time tag features supported by the card include:

- The capability for the BC to transmit the contents of the Time Tag Register (lower 16-bits only) as the data word for a Synchronize (with data) mode command
- The capability for the RT to “filter” the data word for the Synchronize with data mode command, by only loading the Time Tag Register if the LSB of the received data word is “0”
- An instruction enabling the BC Message Sequence Control engine to autonomously load the Time Tag Register
- An instruction enabling the BC Message Sequence Control engine to write the value of the Time Tag Register to the General Purpose Queue

5.3.8 MIL-STD-1553 Interrupt Handling

The software API library allows the user to implement custom Interrupt Service routines, which are operated on by the driver using a callback function. This allows for a high-level of scalability while maintaining the ease-of-use, which the API library affords.

The MIL-STD-1553 interfaces are capable of generating interrupts on numerous events. The specific conditions available to generate interrupts can be found in the ***AceXtreme C Software Development Kit (SDK)*** manual (Document # MN-69092SX-002). This manual can be found on the AceXtreme SDK Product Page of the DDC web site.

5.4 Test and Simulation ToolKit (Multi-Function Only)

5.4.1 BC Test and Sim Toolkit features

The Multi-Function ***AceXtreme*** BC (***BU-67206K*** option) provides for the following additional features:

- Programmable Response Timeout
- Intermessage Routines
- Programmable Intermessage Gap Time
- Error Injection (See section 5.4.4)
- Triggers (See section 5.4.5)

5.4.1.1 BC Programmable Response Timeout

The ***BU-67206K*** device supports a response timeout for the BC that is software programmable. The response timeout dictates how long the BC will wait for an RT status word. This allows the user control over when the BC will designate a particular message as a NO RESPONSE and move onto the next message. The longer response timeout values allow for operation over long buses and/or the use of repeaters. The BC supports a programmable timeout from 3.5 µseconds to 30 µseconds with a resolution of 0.5 µseconds.

5.4.1.2 BC Intermessage Routines (IMRs)

IMRs are events that occur upon completion of a BC message. The Multi-Function ***AceXtreme*** Architecture can allow the execution of up to 2 IMRs. The following is a list of the available IMRs:

- Set/Clear Discrete I/Os
- Automatic retries upon failed messages
- Skip next message
- Interrupt on End of Message
- Set/Clear status bits
- Increment data table
- Set/Clear triggers

Refer to Table 13 in the ***BU-69092SX ACEXTREME™ C SDK*** **SOFTWARE MANUAL** (document #MN-69092SX-002) for a detailed summary of the ***BU-67206K*** 's IMRs.

5.4.1.3 BC Inter-Message Gap Time

The intermessage gap time is defined as the time from the mid-parity bit crossing of the last word of one message to the time of the mid-sync crossing of the command word of the subsequent message (See Figure 4).

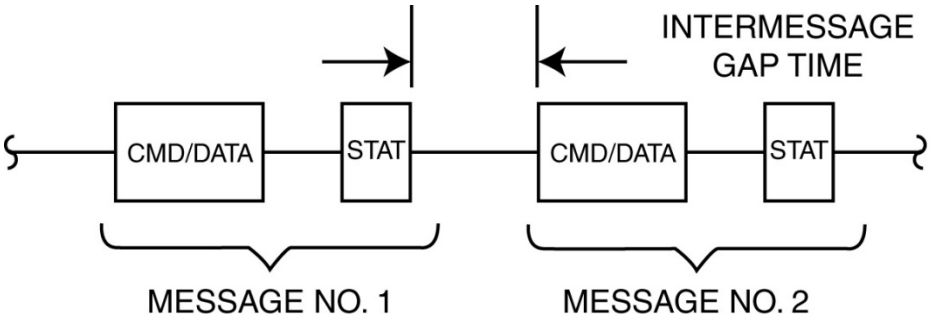


Figure 4. Intermessage Gap Time

To have a determinate time interval between messages, the new Multi-Function ***AceXtreme*** Architecture allows the user to define this gap time. The intermessage gap time is programmable between 3.5 µseconds and 32,000 µseconds with a resolution of 0.5 µseconds.

5.4.2 Multi-RT Test and Sim Toolkit features

The Multi-Function ***AceXtreme*** RT (***BU-67206K*** option) provides for the following additional features:

- Programmable Response Times
- Programmable Response Timeout
- Intermessage Routines
- Error Injection (See section 5.4.4)
- Triggers (See section 5.4.5)

5.4.2.1 Multi-RT Programmable Response Times

The ***BU-67206K*** device supports a response time for the RTs that is software programmable. The RT response time is defined as the time it takes an RT to send back a status word as shown in below. The programmable response time allows the user control over when the RT will respond to a MIL-STD-1553 command word. The RT supports a programmable response time from 3.5 µseconds to 30 µseconds with a resolution of 0.5 µseconds.

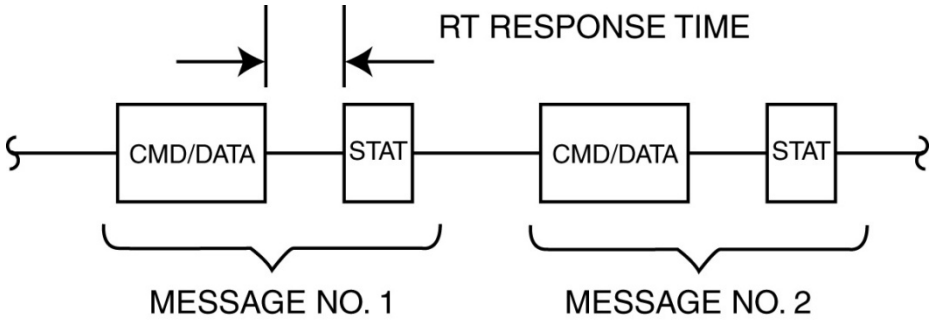


Figure 5. RT Response Time

5.4.2.2 Multi-RT Programmable Response Timeout

The ***BU-67206K*** device supports an RT response timeout that is software programmable. Setting the RT's response timeout value is used for RT to RT commands. The RT response timeout dictates how long the RT will wait for an RT status word. The programmable response timeout allows the user control over when the RT will designate a particular message as a NO RESPONSE and wait for the next message. The RT supports a programmable timeout from 3.5 µseconds to 30 µseconds with a resolution of 0.5 µseconds.

5.4.2.3 Multi-RT Intermessage Routines (IMRs)

IMRs are events that occur upon completion of an RT message. The Multi-Function ***AceXtreme*** Architecture can allow the execution of up to 2 IMRs. The following is a list of the available IMRs:

- Set/Clear Discrete I/Os
- Interrupt after mode code commands
- Store Time-Tag in a circular queue
- Set/Clear status bits
- Interrupt after accessing TX/RX data table
- Increment data table
- Set/Clear triggers

Refer to Table 57 in the ***BU-69092SX ACEXTREME™ C SDK* SOFTWARE MANUAL** (document #MN-69092SX-002) for a detailed summary of the ***BU-67206K***'s IMRs.

5.4.3 MT Advanced Error Sampling (AES)

The Monitor in the ***AceXtreme*** Multi-Function product provides the additional ability to capture Advanced Errors using a sampling mode. The types of errors captured in this mode include Manchester, Parity, and general glitch errors. These errors can then be emulated using the Replay feature (See Section 5.4.7). The AES mode generates the same packet header as MT-I but uses a slightly different packet trailer. The MT will determine if the message contains an error by using the error flag of the Block Status Word (BSW). If an error is detected, the MT will start sampling the bus at a 50 ns sample rate in order to capture this error.

5.4.4 Error Injection

Errors can be injected on either a BC Message or via an RT response on the ***BU-67206K***. The error types that can be injected by the BC and RTs are Length errors and Encoding errors. Refer to below for a list of available errors.

Length Errors include modifying data Word Count, or Bit Count Errors for a specific message.

Encoding Errors include Glitch or Inverse errors which can be anywhere in the message (command words, or datawords). The Glitch and Inverse errors allow for error types such as invalid sync patterns, parity errors, and Manchester bi-phase errors.

Table 3. Error Injection

Error	Mode	Description	Value
Word Count	BC/RT	Increasing or decreasing the number of data words in a message.	-32 to +32 Words
Bit Count	BC/RT	Adding or removing bits from a specific word for a given message.	-3 to +3 Bits
Glitch	BC/RT	Forces the output of the encoder to an idle bus connection for a specific time period.	50 to 3000 ns (50 ns steps)
Inverse	BC/RT	Invert the output of the encoder for a specific time period.	50 to 3000 ns (50 ns steps)

5.4.5 Triggers

The ***BU-67206K*** has a new Trigger component in each channel as a part of the Multi-Function ***AceXtreme*** Architecture.

Each channel can configure up to 18 different triggers. Each trigger configured can have up to twelve different available trigger events associated with it that

would occur at the time the trigger condition is met. Refer to Table 5 in the ***BU-69092SX ACEXTREME™ C SDK SOFTWARE MANUAL*** (document #MN-69092SX-002) for a detailed summary of the available trigger events.

Among the 18 triggers, two are Time-Message Triggers (TMT) and the other 16 are General Purpose Triggers (GPT).

The inputs to TMTs can be configured through software for either a time delay of x µs/ms or a specific number of messages processed. The inputs to the GPTs can be message patterns captured by the monitor. As a result, the use of GPTs requires an MT running concurrently in the same channel. These message patterns are user-defined through software.

GPTs can also have discrete I/Os as their trigger input. A GPT can only have its corresponding discrete I/O number linked to its input, i.e. GPT0 can only be triggered by DIO0.

Both TMTs and GPTs can be triggered by another trigger's output.

A block diagram of the Trigger component can be found in Figure 6.

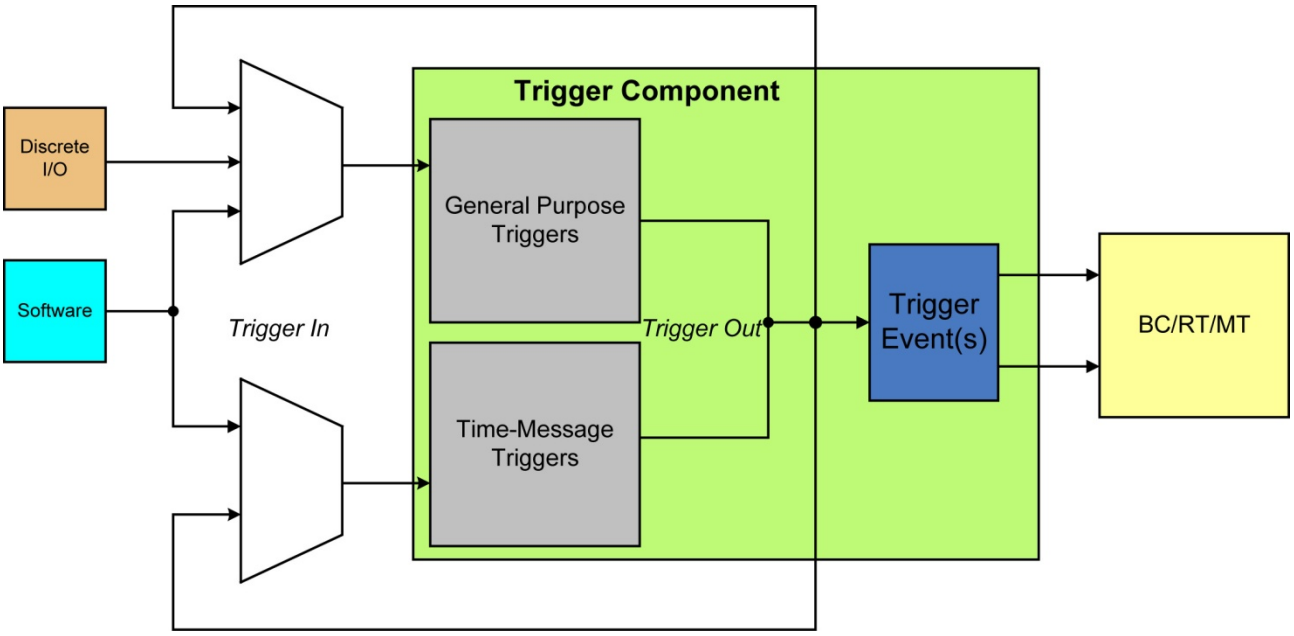


Figure 6. Trigger Component Block Diagram

5.4.6 Dynamic Bus Control

The Multi-Function ***AceXtreme*** BC has the option to enable a user-specified RT address after receiving the DBC acceptance RT status. The RT that is to be enabled does not need to be currently inactive.

The Multi-Function ***AceXtreme*** Multi-RT allows for multiple RTs to be configured to accept a DBC request. To enable an RT with DBC a hold-off time must be specified. The hold-off time is defined as the time that an RT must wait after accepting a DBC request before deactivating itself and then activating the BC in the same channel. The hold-off time is software programmable from 40 µs to 130,000 µs.

5.4.7 Replay Function

The ***BU-67206K*** Multi-Function ***AceXtreme*** Architecture provides the ability to replay bus traffic from captured MT-I/MT-R packets. The MT-I and MT-R modes have the capability to capture bus traffic data and store it into a file. The Replay function can use this file to replay the captured traffic data.

The Replay function has several configurable options and features such as the following:

- Start/Reset/Pause/Stop replay activity
- Emulate up to 31 RTs
- Loop replay a specific number of times
- Trigger conditions to start/stop replay activity
- Replay message errors

The Replay engine will replay captured 1553 streams stored in IRIG106 Chapter 10 packet formats (See Section 5.3.4). If the Advanced Error Sampling (AES) was enabled during the 1553 stream capture, the errors will be replayed. A software configurable option allows for the Replay engine to skip packets containing errors when AES was enabled. If AES was not enabled during the capture then all errors are automatically ignored during Replay.

In order to play back traffic, the user will need to configure the BC for replay mode and input a valid file containing a captured 1553 stream. See the **acexBCReplayStart()** function in the ***AceXtreme C SDK*** software manual for detailed information.

5.5 Discrete Digital I/O Option

The ***BU-67x06K*** card can be configured to include up to eight discrete digital signals that are individually programmable as inputs or outputs. The discrete outputs can be used for a variety of applications, including triggering events, indicating status, or general purpose use.

Discrete digital I/O channel 1 is the LSB and channel 8 is the MSB for any software accesses to these signals.

The discrete digital I/O signals are 5V tolerant with 10K pull-up resistors to +3.3V. These I/O signals default to inputs after power up. The outputs are +3.3V totem-pole type with 12mA drive capability. See Table 1 for more detail.

In the Enhanced BC Mode, during the execution of a Wait for External Trigger (WTG) instruction, the BC will wait for a low-to-high transition on DIO X, where X is the channel number, before proceeding to the next instruction. This feature must first be enabled using the aceBCExtTriggerEnable function.

(MF Option)The ***BU-67206K*** architecture also allows for the discrete digital I/O signals to be linked to triggers. When a trigger is linked to a discrete I/O, the number of the trigger is the same as the number of the discrete I/O, i.e. GPTn is linked to DIOn.

The discrete digital I/O signals can also be linked to BC/RT IMRs. BC IMRs can only be linked to DIO 0-3, while RT IMRs can only be linked to DIO 4-7

5.6 Avionics Discrete I/O Option

The ***BU-67x06K*** card includes eight Avionics Level Discrete I/O Channels that are individually programmable as inputs or outputs. As outputs they are Open-Drain type drivers. When used as inputs these channels are configured to sense Ground / Open discrete inputs with +35V input voltage tolerance.

Avionics Discrete digital I/O channel 1 is the LSB and channel 8 is the MSB for any software accesses to these signals.

Avionics I/O channels are limited to 0.5A capability per channel.

(MF Option) The ***BU-67206K*** Multi-Function architecture also allows for the avionics discrete I/O signals to be linked to triggers. When a trigger is linked to a discrete I/O, the number of the trigger is the same as the number of the discrete I/O, i.e. GPTn is linked to DIOn.

The avionics discrete I/O signals can also be linked to BC/RT IMRs. BC IMRs can only be linked to AIO 0-3, while RT IMRs can only be linked to AIO 4-7

5.7 External 10 MHz Time Tag Clock Input

Besides an internal clock source for the time tag counter, the ***BU-67x06K*** provides support for an external time tag clock with an external counter reset control. This external time tag clock input may be driven by a 10 MHz clock source to implement relative time stamps as defined in IRIG-106 Chapter 10. These signals are internally pulled-up to +3.3V and are +5V tolerant.

To switch the time tag counter to use the external clock and clock enable signals, please see the aceSetTimeTagRes() function in the ***AceXtreme C SDK Software Manual***. When the time tag counter is switched to use the external signals, the following applies. Driving CLK_ENABLE_IN to a digital logic high enables the time tag counter to increment. The internal time tag register will increment on each rising edge of the external time tag clock while the CLK_ENABLE_IN is logic “1”. Driving the CLK_ENABLE IN signal low will clear the time tag counter.

5.8 IRIG Time Code

IRIG-B, B123 time code standardization allows equipment to be synchronized to a known reference time. The ***BU-67x06K*** card can accept an IRIG-B input via digital signal or amplitude modulated (AM) coding on an audio sine wave carrier signal. Digital or demodulated analog data is read once per second.

The IRIG Time can be fed to the 1553 channels to be used as the Time-Tag instead of the local timers included for each channel.

Refer to the ***AceXtreme C SDK*** **Software Manual** (document #MN-69092SX-002) for more information.

5.9 Board Configuration

Although the PCI interface is automatically configured by the system, there are other configuration options which the user must manually configure.

5.9.1 Configuration Jumpers

There are three user configuration jumpers (W1A, B, C) grouped into the W1 jumper block at the end of the card, furthest from the rear panel bracket. The card is shipped without the corresponding shorting plugs installed, which allows

normal operation. The jumper pins and corresponding shorting plugs are 2 mm pitch.

The functionality of the three configuration jumpers is as follows:

- W1A - BACK UP FLASH IMAGE = Boot FPGA using back-up flash image when jumper is ON
- W1B -RESERVED FOR FUTURE USE
- W1C - FLASH WRITE ENABLE = Enable re-writing of FPGA flash device when jumper is ON

Note: *W1C is logically in parallel with the corresponding signal on the J2 rear panel connector.*

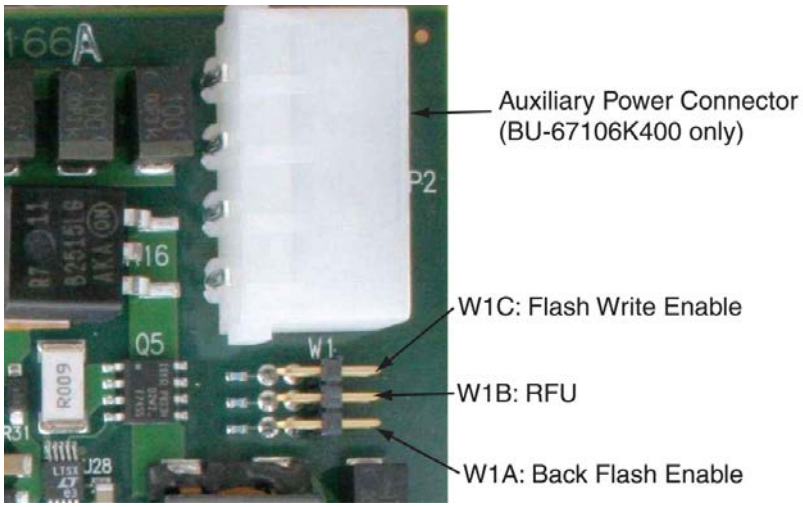


Figure 7. Configuration Jumpers W1A, B, C

5.9.2 Board Soft Jumpers

These cards have “soft jumpers” in the onboard Flash memory. The soft jumpers are manipulated via a configuration utility included in the BU-69092SX Software Package. For more information on the utility programs please reference DDC’s application note *AN/B-50: AceXtreme™ Transmit Inhibit and Bus Controller Disable Features*, available for download from DDC’s BU-67X06K product web page (Direct document link – http://www.ddc-web.com/Pub/211/560.ashx).

The soft jumpers are write protected via the same mechanism as the rest of the Flash memory: via the Flash Write Enable jumper (Table 5) and FLASH_WRITE_EN_L signal (Table 6).

The soft jumpers can control the following:

- Tx Inhibit
- BC disable Hardware

After reset, the soft jumpers are read by the on-board AceXtreme channel logic from the reserved, write protected, flash locations to implement TX Inhibit and/or BC disable.

5.10 Card Pinouts

This section delineates the user's pinouts for the card. The connectors described here are the two connectors on the I/O bracket, the few configuration jumpers on the board itself, and the aux power connector (***BU-67206K400x*** cards only).

5.10.1 Aux Power Connector

The four channel version of the ***BU-67x06K*** has an Aux Power Connector located at the end of the card, furthest from the customer I/O connectors. Plug a PC "peripheral power connector" cable into the aux power connector. The peripheral power connector cable is the 4-conductor cable attached to the PC's power supply. The "peripheral power connector" terminology is used by the various ATX/EPS/etc. specifications. This cable is also known as the "4 pin Molex power cable" and is used to power PATA hard drives, PATA optical drives, etc. These connectors are keyed and can only go in one way.

If the PC does not have an unused "peripheral power connector" cable, please obtain a Y-cable. Plug the Y-cable into one of the used connections and the plug remaining end of the Y-cable into the card's aux power connector.

5.10.2 I/O Connector Overview

All customer I/O is via the I/O bracket connectors J1 and J2 (see Figure 9). J1 is the "uppermost" connector, closest to the I/O bracket's mounting screw.

J1 contains all of the 1553 bus differential signals and is a HD-26 D-Subminiature type female connector. An HD-26 connector is a High Density 26 contact three-row connector that fits into a "DB-15" shell. The mating HD-26 male connector is secured with mounting screws.

All of the various other signals are in the 36-contact MDR-type receptacle connector. The mating MDR plug connector is secured with a squeeze-to-release latch mechanism.

The I/O characteristics of the various signals in these connectors are defined in Table 1.

The card is supplied with the mating I/O connector components (listed in Table 4) and J1 cable assembly. The supplied J1 cable (see Figure 8) breaks the 1553 channels out to standard Trompeter 3-lug jack (socket) connectors. The mates for these connectors (not supplied) are Trompeter PL75 (plug) or equivalent connectors.

If desired, the customer can mate with the J1 HD-26 connector directly. Standard male HD-26 connectors and backshells can be used. Examples are L-Com's SDH26P (male connector) and SDC15AG (Backshell).

A J2 cable is not supplied due to the application specific nature of each customer's non-1553 wiring. Instead, the J2 connector's mate and backshell is supplied. The supplied MDR plug breaks out the connectors' contacts to four rows of solder cups. The solder cups allowing easy construction of customer specific cables without specific tooling equipment. The solder cups accept 24 to 30 AWG discrete wires.

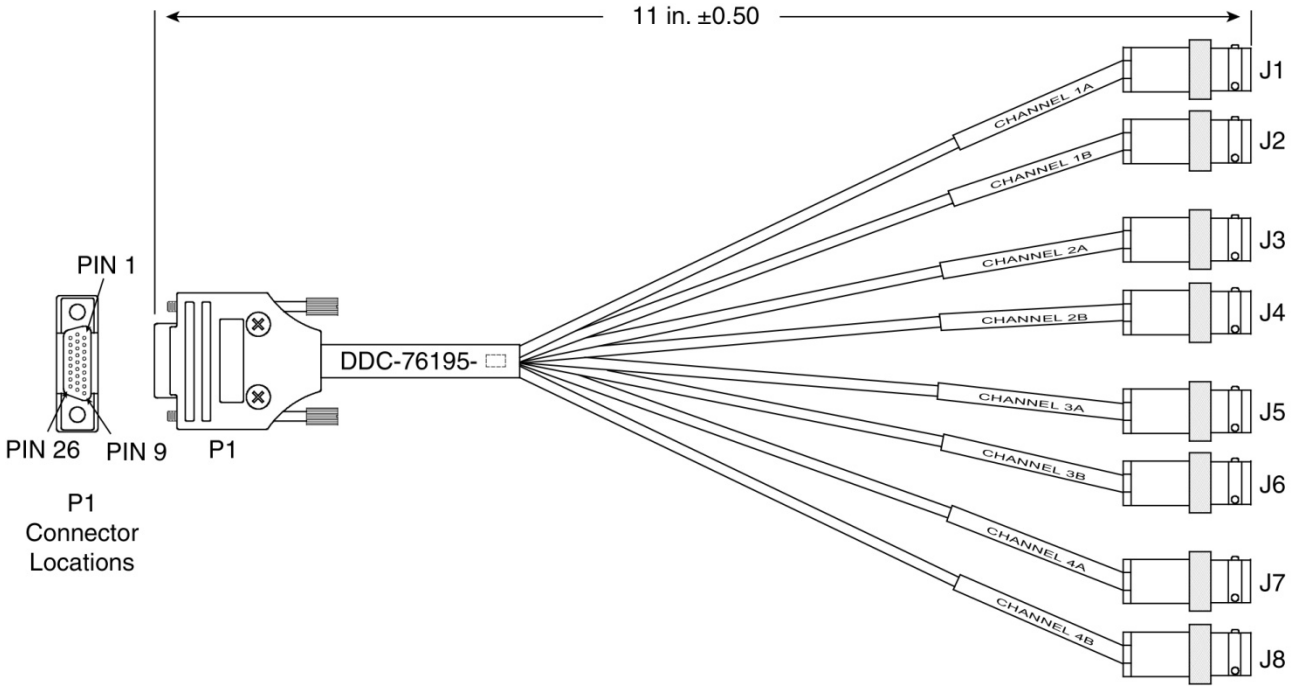


Figure 8. J1 Cable Assembly

Table 4. Supplied I/O Components

Card Version	Included 1553 Cable Assembly	Mate for J2: 36 contact MDR connector, plug	Mate for J2: Backshell for MDR connector
BU-67x06K100	DDC-76195-1	1x 3M 10136-3000PE	1
BU-67x06K200	DDC-76195-2	1x 3M 10136-3000PE	1
BU-67x06K400	DDC-76195-3	1x 3M 10136-3000PE	1

5.10.3 Physical Pinout orientation for I/O Connectors

The I/O bracket of the card and the I/O connectors are shown in .

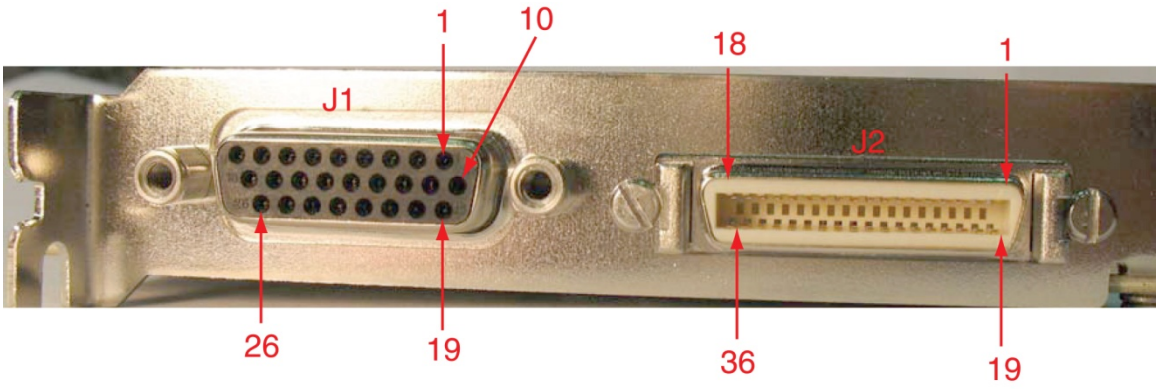


Figure 9. I/O Connectors

5.10.4 Signal Naming Convention for I/O Connector

5.10.4.1 1553 Bus Signals

J1 contains the MIL-STD-1553 bus signals, which are listed in Table 5.

The 1553 signal naming is scheme is listed below.

BUS#**XY** = Where "#" indicates the channel, (1:4), "**X**" indicates the bus (A or B) and "**Y**" indicates the phase (+ or -) of the 1553 BUS signal.

Examples:

BUS1B+ is 1553, channel 1, bus B, positive
BUS4A- is 1553, channel 4, bus A, negative

Table 5. J1 Connector Pinouts		
Pin	**Signal Name**	**Description**
1	BUS2B-	1553 Channel 2B Negative side
2	BUS2B+	1553 Channel 2B Positive side
3	BUS2A-	1553 Channel 2A Negative side
4	BUS2A+	1553 Channel 2A Positive side
5	BUS3B-	1553 Channel 3B Negative side
6	BUS3B+	1553 Channel 3B Positive side
7	BUS3A-	1553 Channel 3A Negative side
8	BUS3A+	1553 Channel 3A Positive side
9	BUS4B-	1553 Channel 4B Negative side
10	BUS1A-	1553 Channel 1A Negative side
11	BUS1A+	1553 Channel 1A Positive side
12	N/C	No Connect
13	N/C	No Connect
14	N/C	No Connect
15	N/C	No Connect
16	N/C	No Connect
17	BUS4A-	1553 Channel 4A Negative side
18	BUS4B+	1553 Channel 4B Positive side
19	BUS1B-	1553 Channel 1B Negative side
20	BUS1B+	1553 Channel 1B Positive side
21	N/C	No Connect
22	N/C	No Connect
23	CHS GND	Ground shield connection
24	N/C	No Connect
25	GND	Ground reference connection
26	BUS4A+	1553 Channel 4A Positive side

The J2 connector's pinout is listed in Table 6, with a description of the signals following the table.

Table 6. J2 Connector Pinouts		
Pin	**Signal Name**	**Description**
1	EXT_CLK_OUT	10MHz synchronous clock output. This clock is synchronous to the internal clock.
2	EXT_CLK_IN	External Time-Tag clock input

Table 6. J2 Connector Pinouts		
Pin	**Signal Name**	**Description**
3	CLK_ENABLE_IN	External Time-Tag Counter enable: 0 = Time-Tag counter reset (when external) 1 = Time-Tag counter enabled (when external)
4	GND	Ground reference connection
5	GND	Ground reference connection
6	AV_IO1	Avionics Discrete I/O 1 (+35V)
7	GND	Ground reference connection
8	AV_IO2	Avionics Discrete I/O 2 (+35V)
9	GND	Ground reference connection
10	DIG_IO7	Discrete I/O 7 (Digital Logic levels)
11	GND	Ground reference connection
12	DIG_IO1	Discrete I/O 1 (Digital Logic levels)
13	GND	Ground reference connection
14	AV_IO6	Avionics Discrete I/O 6 (+35V)
15	GND	Ground reference connection
16	AV_IO3	Avionics Discrete I/O 3 (+35V)
17	GND	Ground reference connection
18	AV_IO4	Avionics Discrete I/O 4 (+35V)
19	GND	Ground reference connection
20	IRIG_ANA_IN	Modulated IRIG-B time code input supporting 48-bit time-tags. If using AM Modulated IRIG-B signal, then connect to this input and leave the IRIG_DIG signal unconnected.
21	GND	Ground reference connection
22	AV_IO7	Avionics Discrete I/O 7 (+35V)
23	GND	Ground reference connection
24	AV_IO8	Avionics Discrete I/O 8 (+35V)
25	DIG_IO5	Discrete I/O 5 (Digital Logic levels)
26	GND	Ground reference connection
27	AV_IO5	Avionics Discrete I/O 5 (+35V)
28	DIG_IO6	Discrete I/O 6 (Digital Logic levels)
29	GND	Ground reference connection
30	DIG_IO8	Discrete I/O 8 (Digital Logic levels)
31	DIG_IO2	Discrete I/O 2 (Digital Logic levels)
32	FLASH_WR_EN_L	Flash Write enable control 0 = Flash Write enabled 1 = Flash Write disabled

Table 6. J2 Connector Pinouts		
Pin	**Signal Name**	**Description**
33	DIG_IO3	Discrete I/O 3 (Digital Logic levels)
34	DIG_IO4	Discrete I/O 4 (Digital Logic levels)
35	IRIG_DIG_OUT	Digital IRIG-B time code output. This output complies with IRIG-200-04
36	IRIG_DIG_IN	Digital IRIG-B time code input supporting 48-bit time-tags. If using PWM IRIG-B signal, then connect to this input and leave the IRIG_MOD signal unconnected.

5.10.4.2 Digital I/O

DIG_IO# = Where "#" indicates the bit (1:8). Internally pulled-up to +3.3V via 10K resistors. These signals are +5V tolerant. When the pin is configured as an output, it is driven by a +3.3V output. These signals can also be used as trigger inputs. Please consult the software manuals for more information.

5.10.4.3 Avionics Discrete l I/O

AV_IO# = Where "#" indicates the bit (1:8). These contacts are for Avionics I/O signaling that uses a nominal avionics +28V rail. These signals are +35V tolerant. When the pin is configured as an output, it is driven by a MOSFET connected to ground. As an output, the pin does not have any internal current limiting. Current through this pin must be limited externally to one amp or less.

These signals can also be used as trigger inputs. Please consult the software manuals for more information.

5.10.4.4 IRIG Inputs

The card accepts both Modulated and Digital IRIG-B time code input(s). The card is in compliance with IRIG Standard 200-04.

IRIG_DIG_IN = External input for Digital IRIG-B time code. Internally pulled-up to +3.3V and +5V tolerant.

IRIG_ANA_IN = External input for Modulated IRIG-B time code.

Please consult the software manuals for more information on the usage of these signals.

5.10.4.5 IRIG Output

IRIG_DIG_OUT= Digital IRIG output signal.

5.10.4.6 External 10 MHz Time Tag Clock Inputs

The card provides support for an external time tag clock. Both of the signals related to this capability are internally pulled-up to +3.3V and +5V tolerant

The external time tag clock input may be driven by a 10MHz clock source to implement relative time stamps as defined in IRIG-106 Chapter 10.

5.10.4.7 CLK_ENABLE_IN

The external time tag clock also offers an external reset input that may be used for clock synchronization purposes. The internal timestamp register will be held in reset while a logic “0” is presented to the CLK_ENABLE_IN pin. The internal time tag register will increment on each rising edge of the external time tag clock while the external enable is logic “1”.

Please consult the software manuals for more information on enabling/disabling this input.

5.10.4.8 FLASH_WR_EN_L

FLASH_WR_EN_L = The card’s FLASH can be re-written when this signal is pulled low. Note that this signal is logically in parallel with the on-card jumper W1. This signal is pulled up to +3.3V.

5.10.4.9 EXT_CLK_OUT L

EXT_CLK_OUT = The card’s clock output.

Please consult the software manuals for more information on enabling/disabling this output.

6 APPENDIX A

The following tables describe the content and use of the PCI configuration registers as they are defined by the ***BU-67x06K***. For a complete description of the generic use of these registers, refer to any PCI system architecture manual.

6.1 BU-67x06K PCI Register Definition

Table 7. BU-67x06K PCI Configuration Header

Address	Word Contents			
	31 24	23 16	15 8	7 0
00h	Device ID = 1C00h		Vendor ID = 4DDCh	
04h	Status Register		Command Register	
08h	Class Code = 078000 h			Rev ID = 01
0Ch	BIST(not implemented)	Header Type 00h	Latency Timer	Cache Line Size
10h	Base Address Register 0			
14h	Base Address Register 1			
18h	Base Address Register 2 (for ***AceXtreme*** RAM)			
1Ch	Base Address Register 3 (for ***AceXtreme*** Registers)			
20 - 24h	Base Address Register 4 (not used)			
28h	Card Bus CIS pointer (not used) 00000000h			
2Ch	Subsystem Device and Subsystem Vendor ID Same as Configuration Register 0, Alias Reads to Configuration Register User configurable			
30h	Expansion ROM Base Address (Not Used, bit 0 = 0)			
34h-38h	Reserved			
3Ch	Max Lat. 00h	Min Gnt 00h	Interrupt Pin 01h	Interrupt Line R/W

Vendor ID is 4DDCh, which is DDC's vendor ID.

Device ID field is used to indicate the device being used.

Device ID = 1C00h

Status Register will be 02B0h after reset, indicating that the ***BU-67x06K*** is fast back-to-back capable and has medium device select timing.

Base Address Registers (BARs) are used to identify ***AceXtreme*** memory space **(BAR2)** and ***AceXtreme*** register space **(BAR3). BAR0** and **BAR1** are for PLX specific control registers.

7 ORDERING INFORMATION

BU-67x 06K X00R- JL 0

Test Criteria:
0 = none

Environmental Temperature Options:
JL = 0°C to +55°C Operating Temperature Range

Lead Free:
R = RoHS Compliant

I/O Options:
1 = 1 dual redundant MIL-STD-1553 Channel
2 = 2 dual redundant MIL-STD-1553 Channels
4 = 4 dual redundant MIL-STD-1553 Channels

Card Type:
06K = PCI Express X1 Card

Options:
1 = Single-Function
2 = Multi-Function

Family:
67 = AceXtreme Architecture

Included Accessories:

- I/O Interface MIL-STD-1553 Cable
- 36-Position Mating Connector
- 36-Position Mating Backshell

Included Software:

BU69092SX- AceXtreme C Software Development Kit (SDK)

Operating System:
0 = Windows 2000/XP/Vista/7
1 = Linux
2 = VxWorks

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