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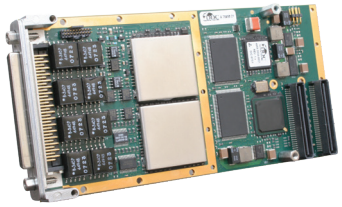
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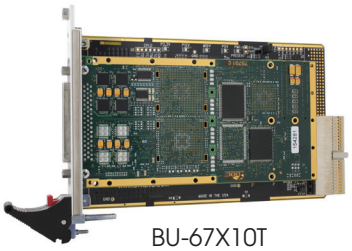
MIL-STD-1553
1/2/4/8 Channel Cards

Hardware Manual

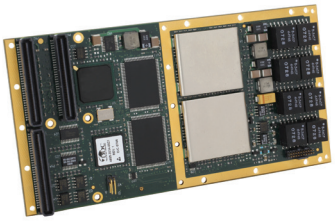
Model: BU-6711XWX



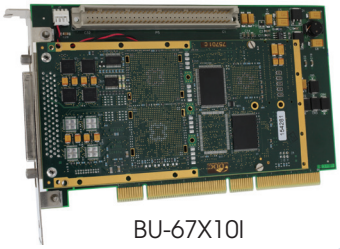
BU-67X10F



BU-67X10T



BU-67X10M



BU-67X10I

The BU-67X10 series' unique I/O mix and high channel count reduces space, power, weight, and cost. These cards contain up to eight dual redundant MIL-STD-1553 channels, feature advanced Multi-RT data bus functionality, and are a perfect fit for military aerospace applications. For added versatility, these cards can be ordered with front or rear I/O and can be used in conduction or convection cooled applications.

Applications

- Mission Computers
- Flight Data Recorders
- Ground Vehicles
- Embedded Systems
- Test and Simulation

Need a Custom Solution? DDC can customize designs for all controllers, ranging from simple modifications of standard products to fully customized solutions for commercial, military, aerospace, and industrial applications.

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DDC's Data Networking Solutions

MIL-STD-1553 | ARINC 429 | Fibre Channel | Ethernet

As the leading global supplier of data bus components, cards, and software solutions for the military, civil, and aerospace markets, DDC's data bus networking solutions encompass the full range of data interface protocols to support the real-time processing demands of field-critical data networking between systems and subsystems on military vehicles. These products, along with our traditional MIL-STD-1553 solutions, represent a wide and flexible array of performance and cost solutions, enabling DDC to support multi-generational programs.

Whether employed in increased bandwidth, high-speed serial communications, or traditional avionics and ground support applications, DDC's data solutions fulfill the expanse of military requirements including reliability, determinism, low CPU utilization, real-time performance, and ruggedness within harsh environments. Our use of in-house intellectual property ensures superior multi-generational support, independent of the life cycles of civil devices. Moreover, we maintain software compatibility between product generations to protect our customers' investments in software development, system testing, and end-product qualification.

MIL-STD-1553

DDC provides an assortment of quality MIL-STD-1553 rugged embedded and lab grade cards and components to meet your data conversion and data interface needs. Our 1553 data bus board solutions are integral elements of military, aerospace, and industrial applications. Our extensive line of military and space grade components provide MIL-STD-1553 interface solutions for microprocessors, PCI buses, and simple systems. Our 1553 data bus solutions are designed into a global array of aircraft, helicopter, unmanned vehicles, and missile programs.

ARINC 429

DDC also has a wide assortment of quality ARINC 429 embedded and lab grade cards and components, which will meet your data conversion and data interface needs. DDC's ARINC 429 components ensure the accurate and reliable transfer of flight-critical data. Our 429 interfaces support data bus development, validation, and the transfer of flight-critical data aboard civil aerospace platforms.

Fibre Channel

DDC has developed its line of high-speed Fibre Channel network access controllers and switches to support the real-time processing demands of field-critical data networking between sensors, computer nodes, data storage, displays, and weapons, for air, sea, and ground military vehicles. Fibre Channel's architecture is optimized to meet the performance,reliability, and demanding environmental requirements of embedded, real time, military applications, and designed to endure the multi-decade life cycle demands of military/aerospace programs.

Ethernet

DDC offers a convenient solution to convert MIL-STD-1553, ARINC 429, and Ethernet protocol in any direction, in real-time, without a host computer.

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DDC supplies MIL-STD-1553 and ARINC 429 board level products in a variety of form factors including USB, PCI-Express, PCMCIA, ExpressCard, AMC, PMC, XMC, PCI-104, PC/104-Plus, PC/104, PCI, cPCI, VME, and ISAbus boards. Our laboratory simulation and in-flight products include multi-function and single-function for system integration and production test environments. Our extensive line of military and space grade components provide MIL-STD-1553 interface solutions for microprocessors and simple systems. Our software is supplied in the form of menus, libraries, and drivers. We also offer additional software to expand our data networking range of options.



BU-67X10F/M/I/T PMC, PCI, CPCI/PXI CARD WITH UP TO 8 MIL-STD-1553 CHANNELS HARDWARE MANUAL MN-67110FX-001

The information provided in this Manual is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise connection therewith.

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Revision	Date	Pages	Description
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Rev B	August 2010	Throughout	Added BU-67210F/M/I/T sections
Rev C	Nov., 2010	Front Cover	Added 1/2/4/8 Channel on front cover of header
Rev D	Jan., 2011	30	Updates to sections 5.4 and 5.5. Updates to Tables 6 and 10.
Rev E	April, 2011	40, 41	Update to table 5, created new table 6.
Rev F	June, 2011	54	Update to Order Information
Rev G	June, 2012	14, 27	Update to table 2, Update to section 5.3.5
Rev H	April, 2013	14, 27, 29, 51	Clarified BU-67210M transmitter specifications in Table 2. Added BU-67210M descriptive text to section 5.3.5. Added enhanced BC mode description to Section 5.4. Ordering Information updates.
Rev J	June, 2016	5, 10, 27, 45	Variable voltage added throughout document. Interface cables edited for leaded version. Update to Figure 3.
Rev K	Jan., 2025	Front Cover, 19-20, 43, 51	Updated BU-67X10F image, Updated operating system support, Table 8 Connector kit details

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1 PREFACE

This manual uses typographical conventions to assist the reader in understanding the content. This section will define the text formatting used in the rest of the manual.

1.1 Text Usage

- **BOLD**–indicates important information and table, figure, and chapter references.
- ***BOLD ITALIC***–designates DDC Part Numbers.
- `Courier New`–indicates code examples.
- <…> - indicates user-entered text or commands.

1.2 Special Handling and Cautions

The ***BU-67x10F/M/i/T*** uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.



Warnings: Turn off power to the computer hardware and unplug from wall.

NEVER insert or remove card with power turned on.

Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.

Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

1.3 Standard Definitions

PCI Peripheral Component Interconnect

PMC PCI Mezzanine Card

CCPMC Conduction Cooled PMC

cPCI Compact Peripheral Component Interconnect

1.4 Trademarks

All trademarks are the property of their respective owners.

1.5 What is included in this manual?

This manual contains a complete description of hardware installation and use.

1.6 Technical Support

In the event that problems arise beyond the scope of this manual, you can contact DDC by the following:

US Toll Free Technical Support:
1-800-DDC-5757, ext. 7771

Outside of the US Technical Support:
1-631-567-5600, ext. 7771

DDC Website:
www.ddc-web.com/ContactUs/TechSupport.aspx

Please note that the latest revisions of Software and Documentation are available for download at DDC's Web Site, www.ddc-web.com.

2 OVERVIEW

The ***BU-67x10F/M*** is a one to eight channel MIL-STD-1553 PMC, whose base specification is IEEE P1386/1386.1. In addition, the boards are designed to the Conduction Cooled PMC specification (ANSI/VITA 20), but can also be used in air-cooled environments (see pictures in Figure 1 and Figure 4). The cards are built in many variants, including front I/O (***BU-67x10Fy***) or rear I/O (***BU-67x10My***). The "y" suffix in the previous model numbers denotes how many 1553 channels the card contains. See Table 1 for the full list of configuration options. In addition, the card is available in Commercial and Industrial operating temperature ranges. See the ordering information section for the full model numbering scheme.

The ***BU-67x10i*** is a PCI Card utilizing all of the powerful features of the ***BU-67x10F*** in a PCI form factor. This device is designed for use in a desktop PC environment, under commercial operating conditions.

The ***BU-67x10T*** is a cPCI Card utilizing all of the powerful features of the ***BU-67x10F*** in a cPCI form factor. This device is designed for use in a cPCI/PXI chassis environment, under commercial operating conditions.

The PCI interface is 32-bit, universal signaling, 33/66MHz Local Bus Revision 2.2 compliant.

Block diagrams in Figure 2 and Figure 5 provide an overview of the card capabilities and signal connections.

The design of the ***BU-67x10F/M/i/T*** leverages the full capabilities of DDC's AceXtreme® Architecture. Features include a highly autonomous BC with expanded instruction set, an RT providing multi-RT capability and a wide variety of buffering options, a selective message monitor, 48-bit, 100 nanosecond resolution IRIG-B time code inputs and 48-bit, 100 nanosecond resolution Time Tag. Each AceXtreme channel contains 1 MB (with parity) of RAM.

The ***BU-67210F/M/i/T*** adds the Multi-Function AceXtreme Architecture, allowing numerous additional test features.

The AceXtreme architecture is backwards compatible with the industry standard, field proven, Enhanced Mini-ACE software, is supported by the ***BU-69092SX*** AceXtreme C Software Development Kit (SDK), along with source code samples, and detailed documentation.

2.1 Features

- Up to Eight Dual Redundant 1553 channels ***(BU-672XX cards are limited to 4 channels)***
- Each 1553 channel can be independently programmed for BC, Multi-RT, Monitor
- Programmable BC operation

- Supports Transformer Coupled 1553 Interfaces
- 1 MB RAM per 1553 Channel
- IRIG-B Time Code Input
- IRIG-B Output/Generator
- 48-bit / 100 ns Time Stamp
- External Time-Tag Clock Input, External Time-Tag Clock Output
- IRIG-106 Chapter 10 Monitor Format
- DMA Engine for Low CPU and PCI Utilization, used in MT-I mode
- AceXtreme® BC/RT/MT Architecture
    - Optional Multi-Function availability
- API Compatible with Enhanced Mini-ACE® Plus SDK
- 16 MB Flash Memory
    - User Storage
- Shock and Vibration Tested
- SW initiated RAM Built-In Self Test

Additional Test and Simulation features included on the ***BU-672xx*** cards (Multi-Function):

- Each 1553 channel can run the BC, RTs and MT concurrently
- Programmable RT Response Times
- Programmable Response Timeout
- Intermessage Routines
- Programmable Intermessage Gap
- Advanced Error Monitor
- Error injection
- Triggers
- Dynamic Bus Control
- Replay Function
- Variable Voltage

Standard I/O Features of the card include:

- Eight User Programmable, Discrete Digital I/O's (GPIO) *
- Eight User Programmable, +35V Avionics Discrete I/O's (GPIO) *

***** Note:** ***BU-67X10MX*** *(Rear I/O versions) contain 16 Avionics Discrete I/O's and no Discrete Digital I/O's*

2.2 Standard I/O Features

The **BU-67x10** card's standard I/O features include up to 8 digital discrete I/O, up to 16 avionics discrete I/O, IRIG-B time code inputs (AM or PWM), external clock input with enable, and 10 MHz clock output along with numerous software configurable register options.

2.3 MIL-STD-1553 Features

The **BU-67x10** implements up to 8 MIL-STD-1553 channels utilizing the DDC AceXtreme® Architecture. Each 1553 channel can be independently programmed for BC, RT, Monitor or true RT/Monitor and is configured with 1MB of onboard RAM per installed channel.

2.4 System Requirements

PMC site supporting either 3.3V or 5V PCI signaling (see Table 7 for connector pinouts).

PMC site with +5V & ±12V supply voltages available.

A supported operating system. (See Table 3 for the list of operating systems.)

For the ***BU-67x10i/T***:

PCI/cPCI connector supporting 3.3V or 5V PCI signaling (See "Use with 5V PCI Signaling")

PCI/cPCI connector with +5V & ±12V supply voltage available.

A supported operating system.

2.5 Configuration Options

Table 1. Configuration Options BU-67x10F/M/I/T

Channel Types	Option 1 Channel Count	Option 2 Channel Count	Option 4 Channel Count	Option 8 Channel Count (BU-671XX only)
1553	1	2	4	8
Discrete Digital I/O	8	8	8	8
Avionics Discrete I/O	8	8	8	8
IRIG-B Input	Yes	Yes	Yes	Yes
IRIG-B Output	Yes	Yes	Yes	Yes

2.6 Applications

The card's rugged construction and ability to operate over the industrial temperature range make it ideal for use in mission computers, flight data recorders, ground vehicles, and other embedded systems that require a military grade card. The card can be ordered with front or rear I/O and can be used in conduction or air-cooled applications. The ***BU-67210F/M/i/T*** can also be useful for test and lab applications.

The design of the ***BU-67x10F/M/i/T*** leverages the full capabilities of DDC's AceXtreme® Architecture. Features include a highly autonomous BC with expanded instruction set, an RT providing a wide variety of buffering options, a selective message monitor, 48-bit, 100 nanosecond resolution IRIG-B time code inputs and 48-bit, 100 nanosecond resolution Time Tag. Each AceXtreme channel contains 1MB of parity-protected RAM. The ***BU-67210F/M/i/T*** adds the Multi-Function capability to the AceXtreme architecture, allowing the concurrent operation of a BC, Multi-RT, and MT on a single 1553 channel.

2.7 Mechanical Design

These PMCs come in two main mechanical variants: ***BU-67x10Fx*** for front panel I/O or ***BU-67x10Mx*** for rear I/O. Both variants follow IEEE P1386 (CMC).

The "M" version has all four primary and secondary conduction cooled thermal interfaces with PMC connectors Pn1, Pn2 and Pn4 for I/O and is also fully compliant to the Conduction Cooled PMC standard [ANSI/VITA 20-2001 (R2005)]. See Figure 6 for the detailed mechanical outline drawing. The air-cooled ordering option for the "M" version provides a PMC bezel (shown mounted in the mechanical outline drawing) to seal the host's PMC bezel hole, if needed. Note that DDC only provides mounting screws for the 10mm standoffs and bezel (if air-cooled variant).

The "F" version provides a 68-pin front panel connector instead of Pn4. This version comes with a front bezel, due to its primary application in air-cooled environments. This card does include most of the features of conduction cooled PMCs but has a PCB that is "standard" PMC length (149 mm), not CCPMC length (143.75 mm). However, the CCPMC defined features it does have can provide a more rugged solution for harsh air-cooled environments. For example, the card has mounting holes for the primary CC thermal interface that bisects the card. These mounting holes can be used with rugged air-cooled hosts that have a stiffening rib in that area. Note that the host card manufacturer provides the stiffening rib, if available. Note also that DDC provides only the mounting screws for the bezel and 10 mm standoffs.

The ***BU-67x10F/M*** card is designed to meet or exceed vibration requirements as specified in ANSI/VITA 47 for a class V3 in conduction cooled applications and class V2 in air-cooled applications. Test specimens of the card were subjected to Shock and Random Vibration testing. All devices were non-operational during all phases of testing. The test sample exhibited no evidence of physical damage at the conclusion of testing and passed factory testing before and after shock and vibration testing. In addition, the ***BU-67x10F/M*** cards feature CCPMC connector "anti-fretting" mounting holes per ANSI/VITA 20-2001 (R2005).

Three (3) shock pulses were applied in each of the following six (6) test directions: Horizontal (+X), Horizontal (+Z), Vertical (+Y), Horizontal (-X), Horizontal (-Z), and Vertical (-Y). Each applied shock pulse was Half-Sine in wave shape.

Random vibration was independently applied for one (1) hour to each of three (3) orthogonal axes resulting in a total test time of three (3) hours. Testing was performed with the input applied along the Horizontal (X), Horizontal (Z) and Vertical (Y) test axes. Test specimens were subjected to a Random input over a wide frequency range.

The ***BU-67x10*** card is designed to meet or exceed the humidity requirements of ANSI/VITA 47 and has been tested to withstand 95% humidity as specified.

The ***BU-67x10F/M*** card is offered in two PC board layout configurations, one with front panel I/O, and one with rear I/O. Both versions are available in commercial and industrial temperature ranges.

The ***BU-67x10i/T*** is a non-ruggedized configuration intended for applications operating in a commercial environment.

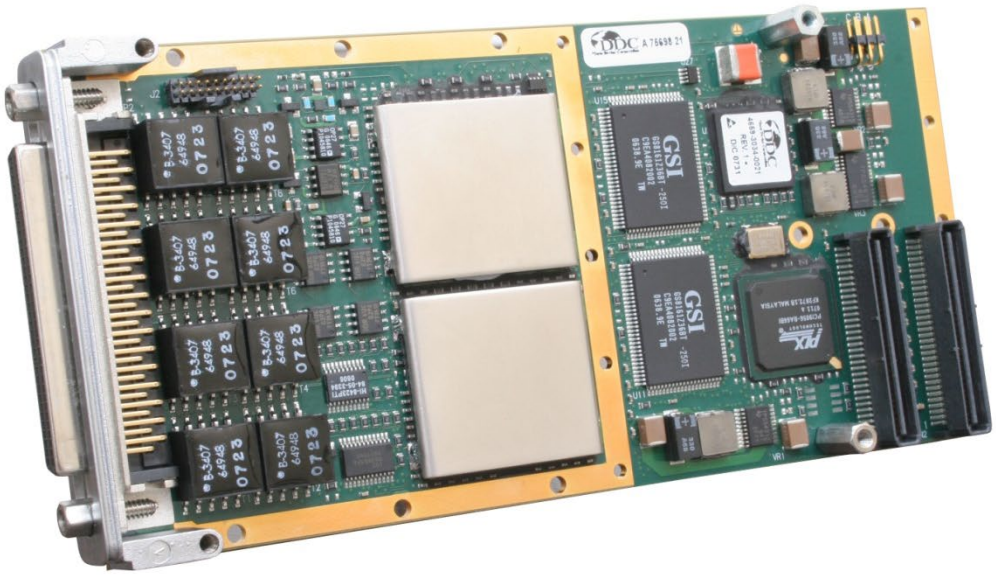


Figure 1. BU-67x10F Front I/O PMC Card

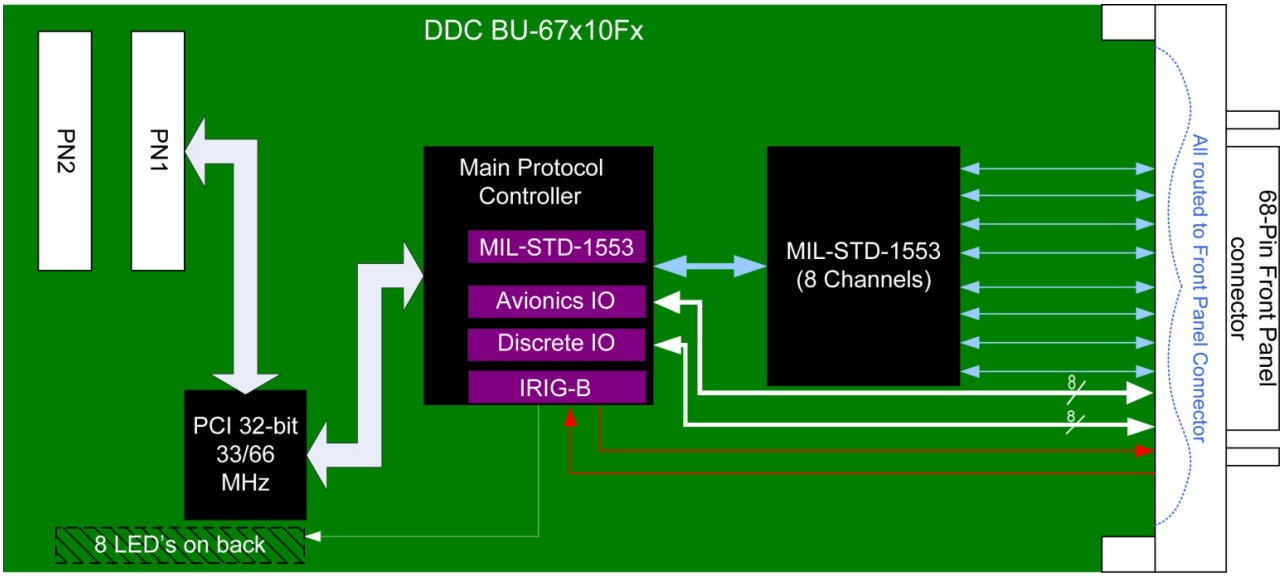
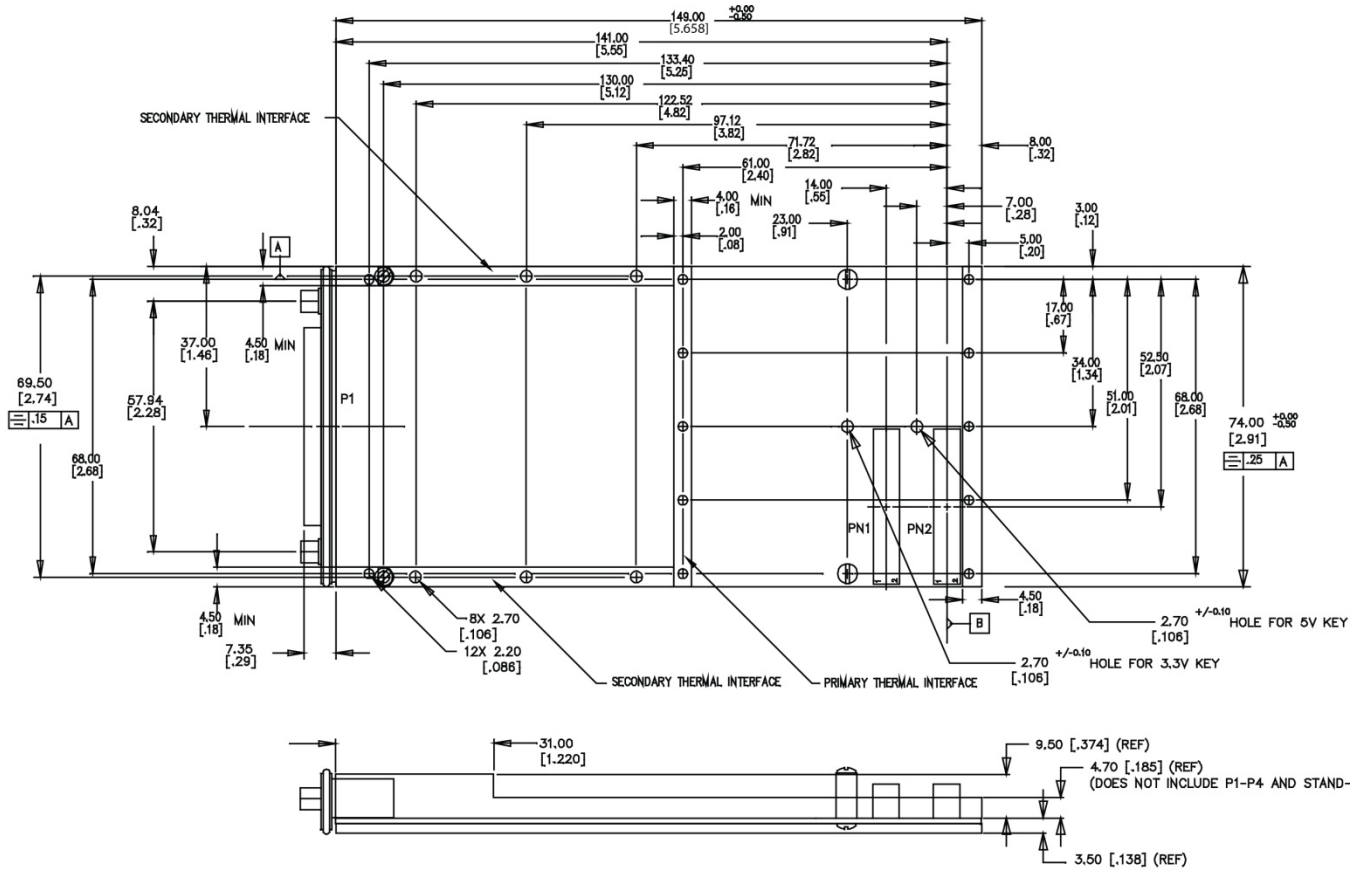


Figure 2. BU-67x10F Block Diagram



NOTE:
1. ASSEMBLY IS NOT TO BE SUBMERGED OR SPRAY CLEANED WITH ANY TYPE OF SOLVENT. EXPOSURE TO ANY SOLVENT MAY COMPROMISE RELIABILITY OF PRODUCT.

Figure 3. BU-67x10F Mechanical Outline

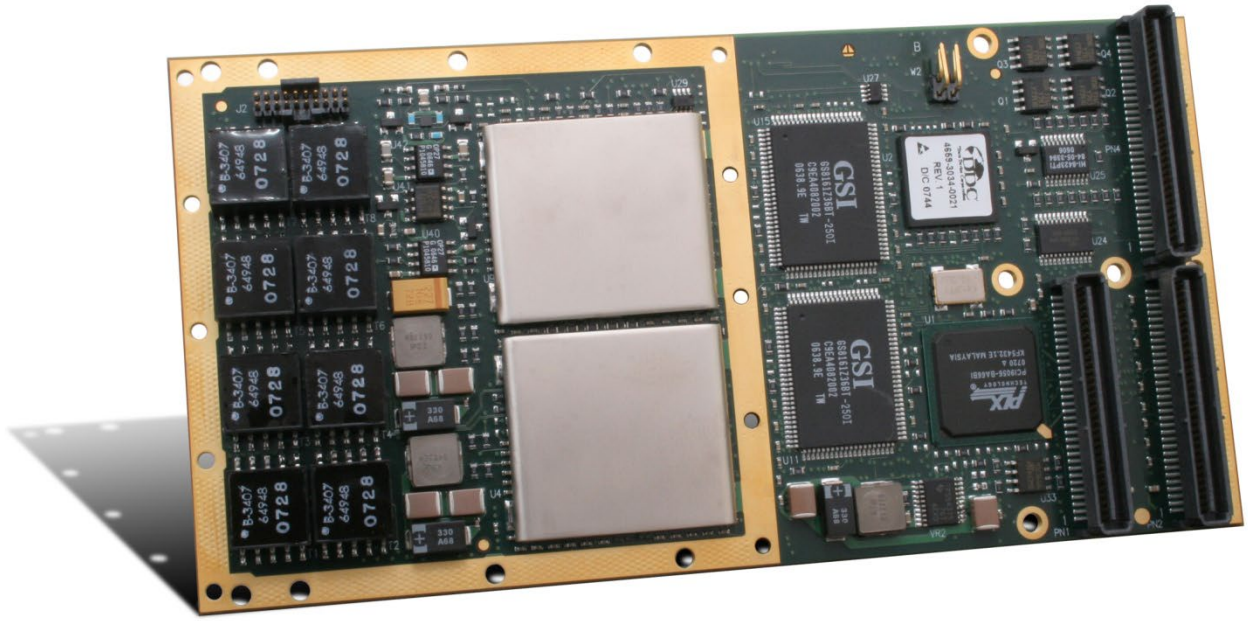


Figure 4. BU-67x10M Rear I/O PMC Card

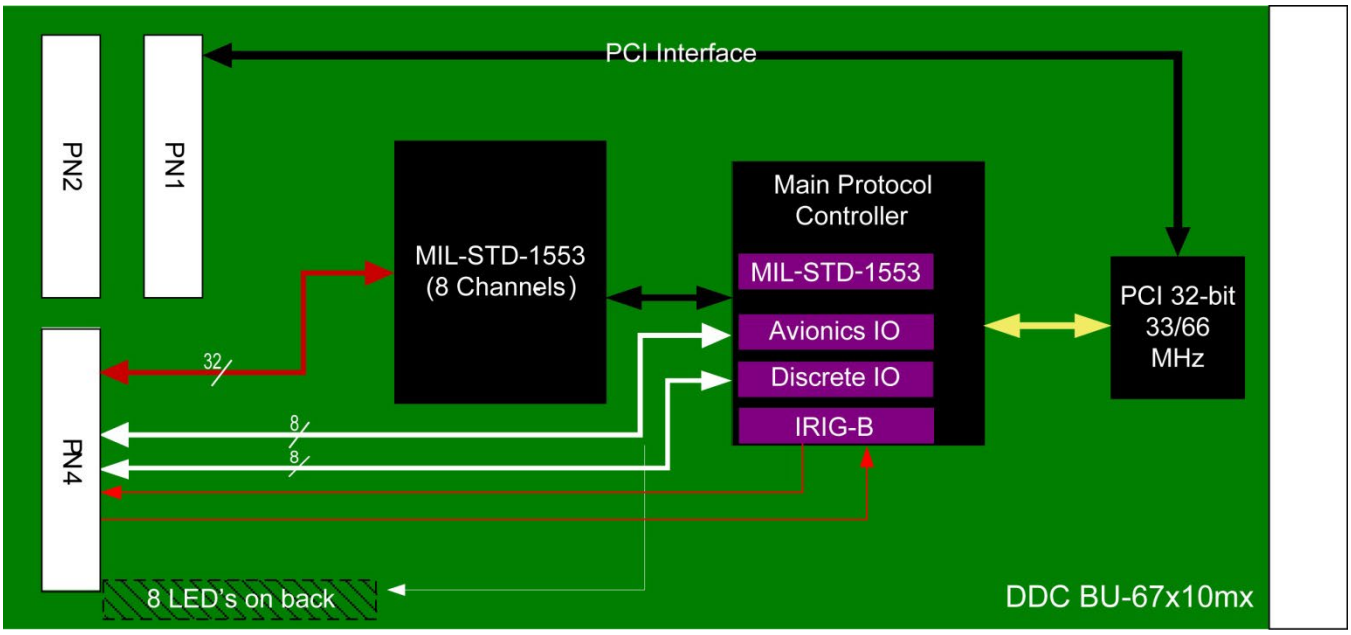
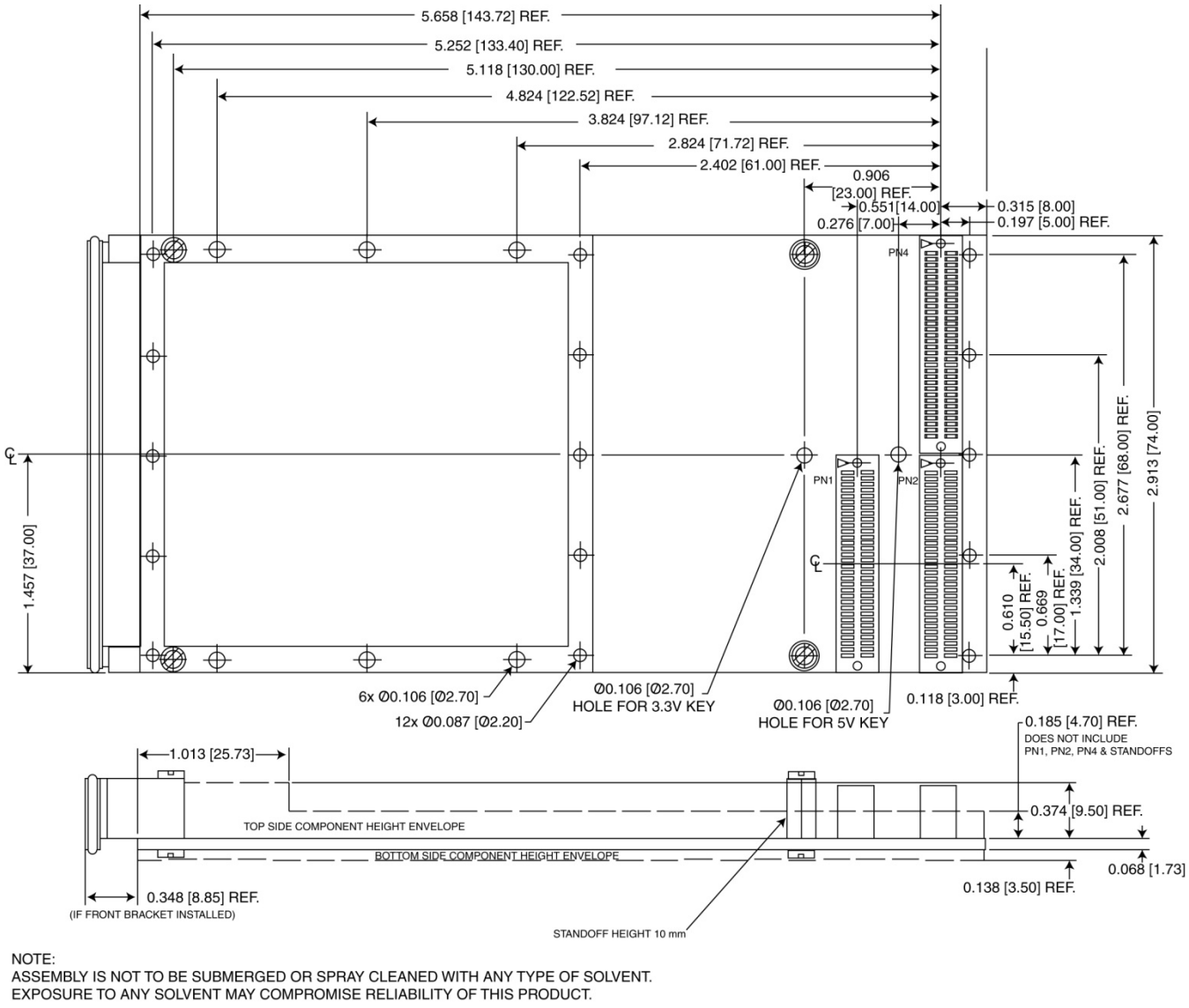


Figure 5. BU-67x10M Block Diagram



NOTE:
ASSEMBLY IS NOT TO BE SUBMERGED OR SPRAY CLEANED WITH ANY TYPE OF SOLVENT.
EXPOSURE TO ANY SOLVENT MAY COMPROMISE RELIABILITY OF THIS PRODUCT.

Figure 6. BU-67x10M Mechanical Outline

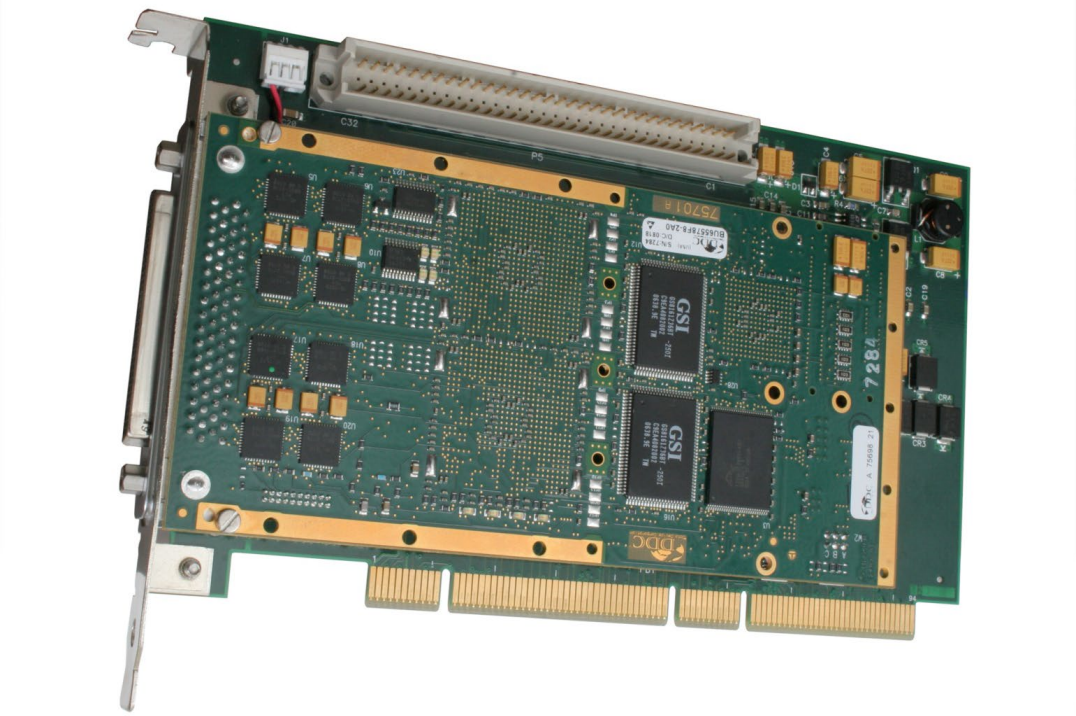


Figure 7. BU-67x10i Front I/O PCI Card

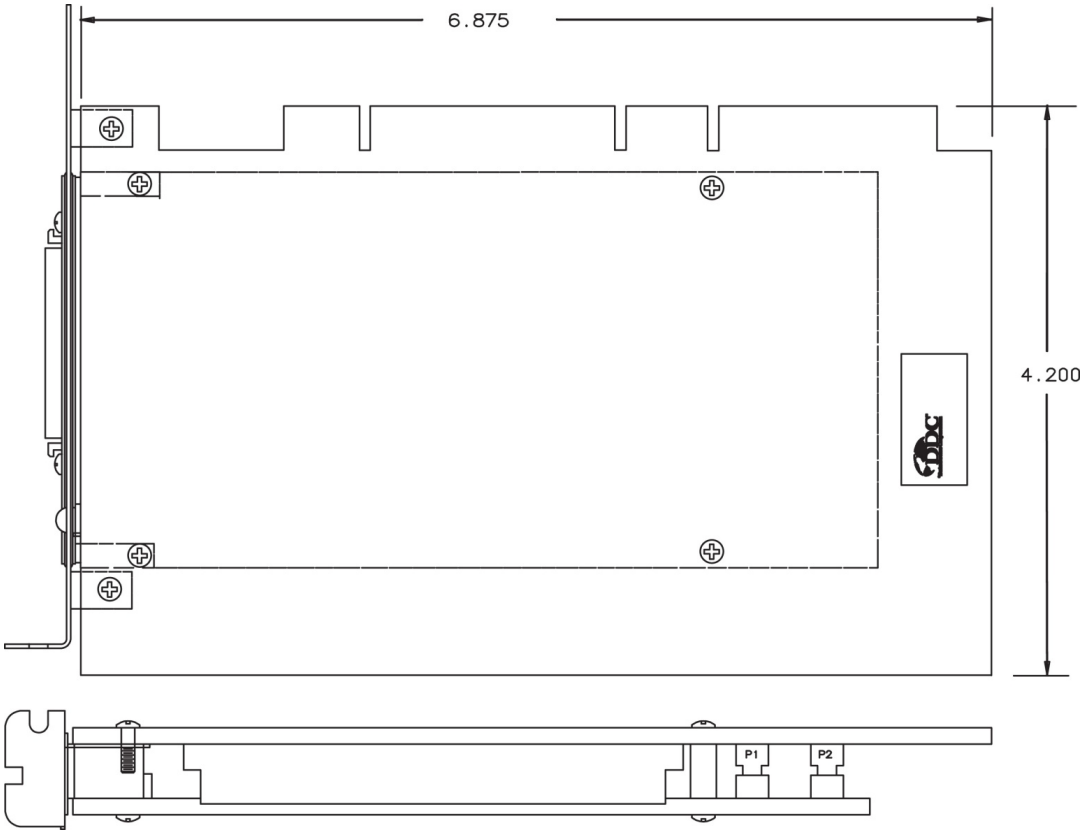


Figure 8. BU-67x10i Mechanical Outline

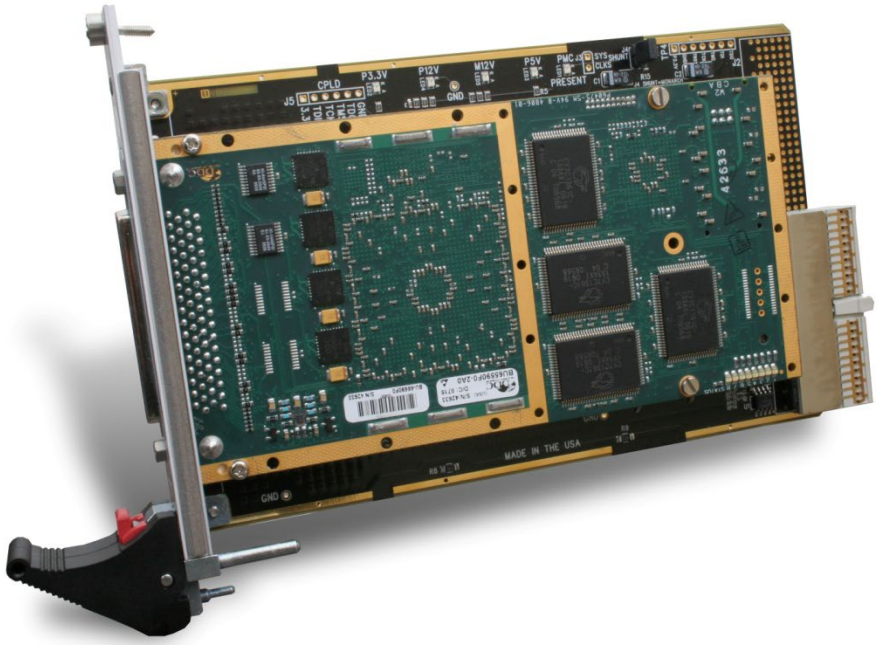


Figure 9. BU-67x10T 3U cPCI/PXI Card

2.8 Environmental Options

The **BU-67x10F** and **BU-67x10M** cards are available in three different environmental ordering options aside from the I/O options described in the Introduction section of this manual. The options include a mix of commercial temperature (0°C to +71°C), industrial temperature (-40°C to +85°C), and rugged and non-rugged cards. These options are specified in the "–xyz" model number suffix in the full model number. See the Thermal section of Table 2 for more details on the environmental parameters. The **BU-67x10i/T** is available in a commercial, non-rugged PCI form factor.

The rugged air-cooled card meets or exceeds the shock and vibration requirements specified in ANSI/VITA 47 for air-cooled cooled cards.

The rugged conduction-cooled card meets or exceeds the shock and vibration requirements specified in ANSI/VITA 47 for conduction cooled cards.

All cards meet the humidty requirements listed in ANSI/VITA 47.

The cards are available conformal coated, please see the ordering information section for more details.

2.9 Specifications

Table 2. BU-67x10F/M/I/T Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
ABSOLUTE MAXIMUM RATING				
+5 V Supply Voltage	-0.3		6.0	V
+12.0 V Supply Voltage	0		+18	V
-12.0 V Supply Voltage	0		-18	V
RECEIVER				
Input Impedance,				
Transformer Coupled (Notes 1-3)	1.000			Kohm
Threshold Voltage,				
Transformer Coupled	0.200		0.860	Vpp
Common-Mode Voltage (Note 4)			10	Vpeak
TRANSMITTER				
Differential Output Voltage,				
Transformer Coupled Across 70 Ohm				
• BU-67110, BU-67210M	19	20.5	27	Vpp
• BU-67210F/i/T				
- Programmable Range	0	—	20.5	Vpp
- Maximum Setting Tolerance	19	20.5	27	Vpp
Output Offset Voltage,				
Transformer Coupled Across 70 Ohm	-250	150	250	mVpeak
Rise/Fall Time	100	150	300	ns
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
+5 V	4.75	5.0	5.25	V
+12 V	11.4	12.0	12.6	V
-12 V	-11.4	-12.0	-12.6	V
Current Drain @ +12.0V	10.0	30.0	50.0	mA
Current Drain @ -12.0V	-50.0	-30.0	-10.0	mA
Current Drain @ +5.0V				
• BU-67x10y1				
Idle		0.277	0.285	A
25% Transmitter Duty Cycle		0.403	0.417	A
50% Transmitter Duty Cycle		0.525	0.546	A
75% Transmitter Duty Cycle		0.646	0.675	A
100% Transmitter Duty Cycle		0.763	0.798	A

Table 2. BU-67x10F/M/I/T Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLY REQUIREMENTS (Con't)				
• BU-67x10y2				
Idle		0.276	0.284	A
25% Transmitter Duty Cycle		0.530	0.550	A
50% Transmitter Duty Cycle		0.774	0.810	A
75% Transmitter Duty Cycle		1.02	1.07	A
100% Transmitter Duty Cycle		1.33	1.39	A
• BU-67x10y4				
Idle		0.326	0.335	A
25% Transmitter Duty Cycle		0.840	0.880	A
50% Transmitter Duty Cycle		1.35	1.42	A
75% Transmitter Duty Cycle		1.88	1.98	A
100% Transmitter Duty Cycle		2.47	2.61	A
• BU-67110y8 (No BU-672XX option)				
Idle		0.519	0.540	A
25% Transmitter Duty Cycle		1.53	1.60	A
50% Transmitter Duty Cycle		2.59	2.74	A
75% Transmitter Duty Cycle		3.70	3.91	A
100% Transmitter Duty Cycle		4.83	5.13	A
POWER DISSIPATION (NOTE 9)				
• BU-67x10y1				
Idle		1.4	1.5	W
25% Transmitter Duty Cycle		1.6	1.8	W
50% Transmitter Duty Cycle		1.8	2.0	W
75% Transmitter Duty Cycle		2.0	2.3	W
100% Transmitter Duty Cycle		2.1	2.5	W
• BU-67x10y2				
Idle		1.4	1.5	W
25% Transmitter Duty Cycle		1.8	2.0	W
50% Transmitter Duty Cycle		2.2	2.5	W
75% Transmitter Duty Cycle		2.5	3.0	W
100% Transmitter Duty Cycle		3.2	3.9	W
• BU-67x10y4				
Idle		1.6	1.8	W
25% Transmitter Duty Cycle		2.5	2.9	W
50% Transmitter Duty Cycle		3.3	4.0	W

Table 2. BU-67x10F/M/I/T Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
75% Transmitter Duty Cycle		4.2	5.3	W
100% Transmitter Duty Cycle		5.5	6.8	W
POWER DISSIPATION (NOTE 9) (Con't)				
• BU-67110y8 (No BU-672XX option)		2.6	2.8	W
Idle		4.2	5.0	W
25% Transmitter Duty Cycle		6.2	7.5	W
50% Transmitter Duty Cycle		8.2	10.2	W
75% Transmitter Duty Cycle		10.5	13.2	W
100% Transmitter Duty Cycle				
DIGITAL DISCRETE SPECIFICATIONS (NOTE 10):				
V_{IL}			0.8	V
V_{IH}	2.0			V
V_{OL} (I = 12mA)			0.4	V
V_{OH} (I = 12mA)	2.6			V
AVIONICS DISCRETE SPECIFICATIONS:				
V_{IL}			3.5	V
V_{IH}	4.0			V
V_{OL}			0.5	V
I_{Leak}			500	µA
MIL-STD-1553 MESSAGE TIMING				
BC Intermessage Gap				
• ***BU-67110X*** (Note 5)	7	10.1	65536	µS
• ***BU-67210X*** (Programmable, See Note 7)	3.5		32000	µS
BC/RT/MT Response Timeout, See Note 8)				
• ***BU-67110X*** (Programmable, See Note 6)	17.5		131	µS
• ***BU-67210X*** (Programmable, See Notes 7)	3.5		30	µS
RT Response Time				
• ***BU-67110X***	4		7	µS
• ***BU-67210X*** (Programmable, See Note 7)	3.5		30	µS
Transmitter Watchdog Timeout		660.5		µS
THERMAL				
CARD OPERATING TEMPERATURE				
• BU-67x10yz-2A0	+71°C inlet air temperature with 5 CFM airflow @ 100% duty cycle on all 8 channels; component case is –40°C to +85°C			

Table 2. BU-67x10F/M/I/T Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
• BU-67x10Mz-2C0 (Mz model only) • BU-67x10yz-3L0	-40°C to +85°C thermal rail temperature @ 100% duty cycle on all 8 channels 0°C to +71°C ambient			
Storage Temperature	-65		+150	°C
PHYSICAL CHARACTERISTICS Size Weight • BU-67x10y8	5.863 X 2.913 (148.9 X 74) 4.80 136			 in. (mm) oz. g.

Notes (For TABLE 2):

1. Specifications are applicable for both unpowered and powered conditions.
2. Specifications assume a 2 volt rms balanced, differential, sinusoidal input. Applicable frequency range is 75 kHz to 1 MHz.
3. Minimum impedance is guaranteed over the operating range, but is not tested.
4. Assumes a common-mode voltage within the frequency range of dc to 2 MHz, applied to pins of the isolation transformer on the stub side (transformer coupled), and referenced to signal.
5. Typical value for minimum time to next message. Under software control, this may be lengthened to 65,536 ms - message time, in increments of 1 µs. If ENHANCED CPU ACCESS is enabled then host accesses during BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences could have the effect of lengthening the time to next message. For each host access during an SOM or EOM sequence, the time to next message will be lengthened by 6 clock cycles. Since there are 7 internal transfers during SOM, and 5 during EOM, this could theoretically lengthen the time to next message by up to 72 clock cycles; i.e., up to 7.2 µs with a 10 MHz clock, 6.0 µs with a 12 MHz clock, 4.5 µs with a 16 MHz clock, or 3.6 µs at 20 MHz clock.
6. Software programmable (4 options). Includes RT-to-RT Timeout (measured mid parity transmit Command Word to mid-sync of Transmitting RT Status Word).
7. In ½ µseconds increments.
8. Measured from mid-parity crossing of Command Word to mid-sync crossing of RT's Status word.
9. Current drain and power dissipation specifications are preliminary and subject to change. Power dissipation specifications assume a transformer coupled configuration with external dissipation (while transmitting with 100% duty cycle) of 1.72W, which is the power delivered to the 1553 fault isolation resistors, the power delivered to the bus termination resistors, the copper losses in the transceiver isolation transformer and the bus coupling transformer.
10. All Digital Discrete lines are pulled up to +3.3V via 10K ohm resistors. This current is part of the 12mA current rating.

3 HARDWARE INSTALLATION

The **BU-67x10F** card is a 32-bit, 33/66MHz PCI Local Bus Rev. 2.2 compliant device that may be inserted into any PMC compatible site. The **BU-67x10M** card is a 32-bit, 33/66MHz PCI Local Bus Rev. 2.2 compliant device that may be inserted into any PMC or CCPMC compatible site that also has a Pn4 I/O connector.

The **BU-67x10i** card is a 32-bit, 33/66MHz PCI Rev 2.2 PCI peripheral card that may be inserted into any PCI 32-bit or 64-bit expansion slot.

The **BU-67x10T** card is a 32-bit, 33/66MHz PCI Rev 2.2 Compact PCI peripheral card that may be inserted into a 32-bit cPCI or PXI Chassis.

When installing the card, the following should be observed:

NEVER insert or remove the card with the power turned on.

ALWAYS take proper precautions to guard against static damage.

Use a wrist strap if available, or ensure proper static grounding by touching the power supply cover **WITH POWER OFF**.

Insert the card and then gently press into the host's PMC mating connectors. Secure with proper hardware. See the "Mechanical Design" section for what hardware is provided with which card variant.

Make sure that adjacent cabling and wiring do not hinder the airflow around the card.

The card is a true Plug and Play device. Interrupts and memory selections will be performed by the operating system as the boot system progresses.

4 SOFTWARE INSTALLATION

Numerous software packages are available for the **BU-67x10F/M/I/T**. The DDC software packages are developed to allow shorter design cycles while allowing all **BU-67x10F/M** functionality to be accessed by user level code.

The following Software packages are available from DDC to operate with this device:

- AceXtreme® SDK (***BU-69092Sx***)
- BusTrACEr™ MIL-STD-1553 Graphical Monitor/Generator (***BU-69066***)
- LabVIEW® Support Package for MIL-STD-1553 and ARINC-429 (***BU-69093***)
- data*Sims* Avionics Data Bus Test and Analysis (***BU-69414***)

4.1 1553 Software (BU-69092Sx) Overview

The AceXtreme SDK (***BU-69092Sx***) package includes:

- MIL-STD-1553 API Library (***BU-69092Sx***)
- AceXtreme FLASH Utility
- Device Drivers (included in the ***BU-69092Sx*** MIL-STD-1553 package)

The card is supplied with the **BU-69092Sx *MIL-STD-1553 AceXtreme C Software Development Kit (SDK)***, with versions available for multiple OS configurations. This software development kit includes a runtime library that provides the user with a hardware abstraction layer for the DDC 1553 hardware. This software layer includes the routines that dramatically reduce software development time by providing high-level C functions for the application programmer to interface to the **BU-67x10F/M/I/T** card. Demo programs are included with the library to demonstrate the capabilities of the card in each mode. Table 3 shows a summary of the supported software.

Table 3. MIL-STD-1553 AceXtreme C SDK Part Number Descriptions

Part Number	Description	Requirements
BU-69092S0	32-Bit/64-Bit Library and Device Drivers for Windows	Windows® 10/11
BU-69092S1	32-Bit/64-Bit Library and Device Drivers for Linux	Linux® Kernel version 5.x
BU-69092S2	32-Bit Library and Device Drivers for WindRiver VxWorks	WindRiver VxWorks® versions 7
* Contact Factory for other Operating Systems		

4.1.1 Windows (BU-69092S0)

Software installation is performed by InstallShield®. This install script will make all necessary registry modifications and will create the required directory structures. A Windows 10/11 operating system specific driver is installed, along with the high-level C library functions.

4.1.2 Linux (BU-69092S1)

The SDK for Linux includes a Linux specific loadable module driver and source code so that the user can compile it against a specific version of the Linux kernel. The driver was developed and tested with Linux kernel version 2.6.z. Installation instructions are included in the ***BU-69092S1*** software package.

4.1.3 VxWorks (BU-69092S2)

The SDK for VxWorks is supplied as a single driver/library. Files can be linked to the VxWorks Kernel with a full rebuild of the kernel, or it can be built as a downloadable module that is loaded and unloaded by the user.

Extracting the ZIP file using an appropriate utility performs the installation of the software, which can then be used with the WindRiver Workbench IDE.

4.2 Testing the Installation

Once the hardware and software is installed, you can test the installation by running one of the sample programs that is shipped with the software. Follow the steps below to test the installation.

4.2.1 Testing the MIL-STD-1553 Software Installation

Run the Tester.exe program. This program requires a Logical Device Number (LDN) also referred to as the channel. A 0 indicates that channel is defined with the LDN of 0 in the DDC CARD MANAGER. This parameter will be entered as required per the installation. If you have more than one channel installed in the system, then running Tester with the appropriate parameter, 0, 1, 2 or 3 and so on, should test each of the channels or cards individually.

If all elements of the test passed, the 1553 card/software is ready for use.

If one or more elements did not pass, refer to the section below on Troubleshooting the Installation.

4.2.2 Troubleshooting the Installation

Usually the installation will be successful, and the self-test will pass. There are, however, some situations that can cause problems during the installation. The most common are detailed below.

An error is returned when an attempt is made to run the SELFTEST or any of the other sample programs. This fault is almost always related to an incorrectly assigned device number. Be sure that a device number was correctly assigned through the DDC Card Manager.

If an error is encountered and the device number appears to be correctly assigned, check the operating system resources to verify that the card has been given a valid memory region by the operating system. Errors have sometimes been observed in Windows 2000 or Windows XP operating systems. The BIOS setting for a PnP operating system is sometimes set to YES, which can cause a problem. This BIOS option was originally created by manufacturers to distinguish between Windows NT and Windows 9x based operating systems. Since Windows 2000 and Windows XP are extensions of the Windows NT kernel this BIOS option must be set for NO under these operating systems. The operating system, as well as all hardware on your system, will still maintain PnP compatibility; it will not be necessary to manually configure resources for PnP cards.

4.3 Updating the Flash Firmware

Detailed instructions on using the DDC Card Manager to update the firmware on the **BU-67x10F/M/I/T** can be found in the E2MA/AceXtreme® Flash Utility Instructions available for download from DDC's BU-67x10F/M/I/T product web page (Direct document link – http://www.ddc-web.com/Pub/211/446.ashx).

To update the Flash, the user will need to install a shunt on the "Flash Write Enable" jumper (Table 5) or drive the FLASH_WRITE_EN_L signal low (Table 7).

5 DETAILED DESIGN AND ARCHITECTURE

5.1 Hardware Configuration and Operation

The **BU-67x10F/M/I/T** card utilizes the PCI interface, and as such does not require any jumpers or switches to set the Base address or interrupt values. The job of configuration for Plug-and-Play PCI is performed by the operating system. During the initial power on boot process, the system performs an enumeration of the PCI bus and allocates a resource configuration that satisfies the card requirements. The system will save the configuration information in the **BU-67x10F/M/I/T's** PCI configuration space registers. These registers are configured at the factory to contain information that identifies the card type, vendor, required memory sizes, and interrupt resources. When the driver loads it will access the configuration registers and identify how the system has configured the card. After identifying each of the installed cards, the device driver will enumerate each of the channels on the card and create a configuration structure that defines the allocated address and interrupt. This information is directly available to the ***MIL-STD-1553 AceXtreme® C Software Development Kit*** and is necessary for read, write and interrupt operations. The end user does not need to know this information if using one of the supplied C API libraries to operate the card.

5.2 PCI Interface

The card supports universal PCI signaling and is keyed accordingly: it has both 3.3V and 5V PCI signaling holes.

The card is a 32-bit PCI target. In addition, it will operate as a bus master when writing data to the host memory in DMA assisted MT-I mode (see 5.3.4.1).

The card is capable of 66 MHz PCI operation. Although 1553, ARINC, or serial I/O may not require the additional bandwidth of a 66MHz bus, the **BU-67x10F/M/I/T** 66MHz PMC card allows the hosts' PCI bus to run at 66MHz, allowing other high-speed devices on the bus to take advantage of the higher bandwidth. Otherwise, if a 33MHz PMC card were placed on a 66MHz bus, the bus speed would be forced to slow down to 33MHz.

When using the card with the BU-69092Sx API Library and drivers there is no need to reference the PCI configuration registers.

The card supports 32-bit and 16-bit read and write operations only. All 8-bit accesses are illegal, but will not generate a target abort.

5.2.1 Interrupts

The card may issue interrupt requests over the PCI bus. PCI Interrupts are generated on the INTA# output signal to the PCI host. The interrupts from each of the channels are functionally OR'ed together to provide a single interrupt. The operations to be taken during the interrupt cycle will be determined by both the device driver requirements and a service routine that is specified by the user

application. The device driver will determine which of the channels on the card generated the interrupt, read the interrupt status registers and queue, transfer this information to an interrupt structure and then signal the appropriate application that the interrupt occurred. The AceXtreme® library provides the necessary routines for generating user Interrupt Service Routines and then hooking them into the device driver.

5.2.2 DMA Design

The card's Direct Memory Access (DMA) engine is host initiated via the AceXtreme library. The AceXtreme library (Host) will initiate the DMA transfer by writing to the PCI controller on the card.

The Card will issue an interrupt once a DMA transfer has been completed.

The AceXtreme library will implement a round robin scheduling mechanism in order to arbitrate the one DMA channel over the 1553 channels. A software DMA work queue may be implemented in order to adhere to this scheduling mechanism.

5.2.3 Register & Memory Addressing

The **BU-67x10F/M/I/T** PCI interface contains a set of "Type 00h" PCI configuration registers that are used to map the device into the host system. The configuration register space is mapped in accordance with PCI Revision 2.2 specifications. These registers are arranged such that all memory and register space may be addressed through a single PCI function.

Configuration registers implement the Subsystem Vendor and Device ID, and control the Fail-Safe operation of the device. There are four Base Address Registers (BAR) used on the design of this card. All BAR mapping is located in PCI configuration register space.

When using the card with the ***BU-69092Sx*** API Library and drivers, the details of these registers and memory addresses are abstracted from the user to provide an easy-to-use High Level "C" programming environment.

5.3 1553 Architecture

5.3.1 Combination Modes

The ***BU-67110*** Single-Function AceXtreme® architecture has the ability to run the following concurrent modes:

(1) BC and MT-I

(2) RT and MT-I

(3) RT and MT

(4) Multi-RT and MT-I

The ***BU-67210*** Multi-Function AceXtreme architecture has the ability to run the BC, Multi-RT, and MT-I modes concurrently on a single 1553 channel. Any combination of these modes is supported. By running more than one mode at one time, the user can have a variety of information and features readily available. Each channel's mode is configurable through software.

5.3.2 Bus Controller (BC) Architecture

The AceXtreme BC mode offers several new powerful architectural features. This includes the incorporation of a highly autonomous BC message sequence control engine, which greatly serves to offload the operation of the host CPU. This can be a critical factor in embedded systems with real time requirements.

The Enhanced BC's message sequence control engine provides a high degree of flexibility for:

- Implementing major and minor frame scheduling
- Inserting asynchronous messages in the middle of a frame
- Separating 1553 message data from control/status data for the purpose of implementing double buffering and performing bulk data transfers
- Implementing message retry schemes, including the capability for automatic bus channel switchover for failed messages
- Reporting various conditions to the host processor by means of user defined interrupts and a general purpose queue
- Dynamic BC message and frame modification

The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type, sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. In the Enhanced BC mode, there is no explicit limit to the number of messages that may be processed in a frame.

The Multi-Function AceXtreme® BC (***BU-67210*** option) provides additional features with the Test and Simulation Toolkit (See section 5.8.1)

5.3.2.1 BC Programmable Message Timing

The AceXtreme Architecture provides the capability of programming the time to next message through software. The time to next message defines the time from the start of the current message to the start of the subsequent message as shown in Figure 10 below. However, the uncertainty of the RT's response can cause the gap time interval between the end of the message and the beginning of the following message to vary.

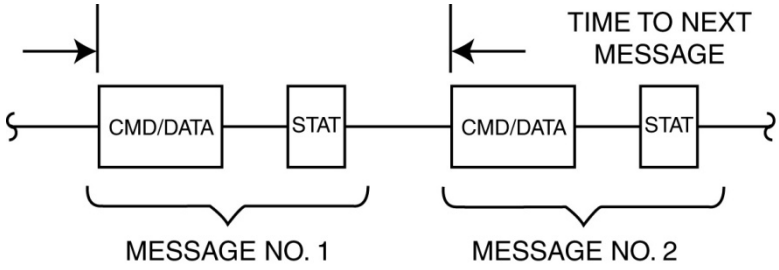


Figure 10. Time To Next Message

The Test and Simulation toolkit also allows an additional timing mode, which is useful in cases where high-accuracy and violating the 1553 minimums is required. Please see section 5.8.1.3 for further information on this mode.

5.3.3 Multiple Remote Terminal (Multi-RT) Architecture

The AceXtreme provides the capability of implementing up to 31 RTs on a single channel of the ***BU-67x10F/M/I/T*** device. The Multi-RT architecture provides multi-protocol support, with full compliance to all of the commonly used data bus standards, including MIL-STD-1553A, MIL-STD-1553B (Notice 2), and MIL-STD-1760. Programmable flexibility enables the RT to be configured to fulfill any set of system requirements. This includes the capability to meet the MIL-STD-1553A response time requirement of 2µs to 5µs, and multiple options for mode code subaddresses, mode codes, RT status word, and RT BIT word.

The AceXtreme® RT protocol design implements all of the MIL-STD-1553B message formats and dual redundant mode codes. The design has passed validation testing for MIL-STD-1553B compliance. The AceXtreme RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. One of the main features of the AceXtreme RT is its choice of memory management options. These include single buffering by subaddress, double buffering for individual receive subaddresses, circular buffering by individual subaddresses, and global circular buffering for multiple (or all) subaddresses.

The AceXtreme RT provides an internal mechanism for RT Command Word illegalizing. The design of the ***BU-67x10F/M/I/T*** supports different options for specifying the RT addresses for the individual channels (See section 5.3.6). In all configurations, the RT address is readable by the host processor.

The Multi-Function AceXtreme RT (***BU-67210*** option) provides additional features with the Test and Simulation Toolkit (See section 5.8.2)

5.3.4 Monitor (MT) Architecture

The AceXtreme Architecture includes a native MIL-STD-1553 Monitor (MT-I). The MT natively operates as an IRIG-106 Chapter 10 monitor. It can also be configured with the following options:

1. Message Error Capture (MEC) see section 5.3.4.2
2. Advanced Error Sampling (AES) (Multi-Function Only) see section 5.8.3

Triggers can also be used to start/stop Monitor operation and automatically insert mark indicators into MT-I packets. (See section 5.8.5)

5.3.4.1 IRIG-106 Chapter 10 Monitor (MT-I)

The IRIG-106 Chapter 10 Monitor (MT-I) provides a definitive solution for systems requiring IRIG-106 Chapter 10 support. In addition, MT-I mode adds DMA support, flexible event notification, and performance enhancements to maximize monitor data throughput.

IRIG-106 is a comprehensive standard developed to ensure interoperability in aeronautical telemetry applications. IRIG-106 is developed and maintained by the Telemetry Group of the Range Commanders Council. Chapter 10 addresses the Digital On-board Recorder Standard, which defines the operation and interfaces for digital flight data recorders. This new file format standard supports MIL-STD-1553, as well as other telemetry protocols such as PCM and ARINC 429.

The MT-I Monitor creates IRIG-106 Chapter 10 data packets, including a packet header and trailer, containing any monitored 1553 traffic (after filter is applied). The MT-I data packet is compliant to MIL-STD-1553, Format 1.

5.3.4.2 Message Error Capture (MEC)

IRIG-106 Chapter 10 defines that the data for messages with errors is not be stored. In certain cases for debug and analysis of MIL-STD-1553 buses, the error data may be required to be stored. With MEC enabled in the MT-I, the monitor will store the data from multiple message errors including the following:

1. Word Count Error
2. No Response
3. Gap Time Error

5.3.5 1553 Transceivers

Every AceXtreme® 1553 channel provides complete multi-protocol support of MIL-STD-1553A/B and STANAG 3838, with voltage source transceivers for improved line driving capability. The ***BU-67x10F/M/I/T*** transceivers are compatible with MIL-STD-1760. The receiver sections of each AceXtreme 1553 channel are fully compliant with MIL-STD-1553B Notice 2 in terms of front-end overvoltage protection, threshold, common-mode rejection, and word error rate.

The ***BU-67210F/i/T*** adds the ability to set the differential output voltage for the 1553 transceivers. This is also known as the Variable Voltage feature. The voltage can be set in 1024 steps from 0 to a nominal setting of 20.5V. Settings are controlled independently per channel, but both transceivers on a given channel will be set to the same level. Software API's are in place to control this feature. This feature is not available on the ***BU-67210M***.

5.3.6 RT Address Selection

There are two options available to set the RT Address:

1. Full Software configuration
2. Configuration from dedicated external signals (Channels 1 and 2 only)

5.3.6.1 Full Software configuration

The AceXtreme® "C" API library abstracts all individual register and memory operations from the application programmer to make card programming a simple task. To set the RT address with the AceXtreme "C" API library, simply call the ***aceRTSetAddress()*** function. All of the functions in the AceXtreme API library are described in complete detail in the AceXtreme Runtime Library Software Manual.

5.3.6.2 Configuration from dedicated external signals

For channels 1 and 2, the RT address is read from dedicated external signals upon a reset event (see sections 5.4 and 5.5). Upon the device leaving reset, the RT Address for Channels 1 and 2 will be set. It is important to maintain ODD parity on the RT_ADP signal if an externally initialized RT address is required. Additionally, this value can be read from the external pins through the AceXtreme SDK (***BU-69092Sx***), using the functions ***aceRTSetAddrSource()*** and ***aceRTRelatchAddr()***.

5.3.7 MIL-STD-1553 Time Tag

The architecture includes an internal MIL-STD-1553 read/write Time Tag Register. This register is a CPU read/write 48-bit counter capable of 100 nanoseconds (10 MHz) resolution. Another option allows software-controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register. The clock source of the counter, either external or internal, is also under software control. See the **aceSetTimeTagRes()** function in the AceXtreme C SDK software manual for detailed information on selecting the clock source, resolution and test mode of the counter.

For each message processed, the value of the Time Tag Register is loaded into the second location of the respective descriptor stack entry ("TIME TAG 48-bit WORD") for both the BC and RT modes.

The functionality involving the Time Tag Register includes the capability to issue an interrupt request and set a bit in the Interrupt Status Register when the Time Tag Register rolls over from 0xFFFFFFFFFFFF to 0x000000000000; for RT mode, the capability to automatically clear the Time Tag Register following reception of a Synchronize (without data) mode command, or to load the Time Tag Register following a Synchronize (with data) mode command.

Additional time tag features supported by the card include the capability for the BC to transmit the contents of the Time Tag Register (lower 16-bits only) as the data word for a Synchronize (with data) mode command; the capability for the RT to "filter" the data word for the Synchronize with data mode command, by only loading the Time Tag Register if the LSB of the received data word is "0"; an instruction enabling the BC Message Sequence Control engine to autonomously load the Time Tag Register; and an instruction enabling the BC Message Sequence Control engine to write the value of the Time Tag Register to the General Purpose Queue.

5.3.8 MIL-STD-1553 Interrupt Handling

The software API library allows the user to implement custom Interrupt Service routines, which are operated on by the driver using a callback function. This allows for a high-level of scalability while maintaining the ease-of-use, which the API library affords.

The MIL-STD-1553 interfaces are capable of generating interrupts on numerous events. The specific conditions available to generate interrupts can be found in the AceXtreme® C Software Development Kit (SDK) manual (Document # MN-69092SX-002). This manual can be found on the AceXtreme SDK Product Page of the DDC web site.

5.4 Discrete Digital I/O Option*

The ***BU-67x10F/I/T*** card includes eight discrete digital signals that are individually programmable as inputs or outputs. Discrete digital I/O channel 1 is the LSB and channel 8 is the MSB for any software accesses to these signals.

The discrete digital I/O signals are 5V tolerant with 10K pull-up resistors to +3.3V. These I/O signals default to inputs after power up. The outputs are +3.3V totem-pole type with 12mA drive capability. See Table 2 for more detail.

In the enhanced BC mode, during the execution of a Wait for External Trigger (WTG) instruction, the BC will wait for a low-to-high transition on DIO X (where X is the channel number) before proceeding to the next instruction. This feature must first be enabled using the aceBCExtTriggerEnable function.

Discrete Digital I/O channels 3-8 also function as RT address inputs for 1553 channel #2.

The discrete digital I/O signals can also be linked to BC/RT IMRs. BC IMRs can only be linked to DIO 0-3, while RT IMRs can only be linked to DIO 4-7

*** *BU-67X10MX*:** No Discrete Digital I/O's exist on the BU-67X10MX (Rear I/O version) of the device

****(MF Option)** The BU-67210 architecture also allows for the discrete digital I/O signals to be linked to triggers. When a trigger is linked to a discrete I/O, the number of the trigger is the same as the number of the discrete I/O, i.e. GPTn is linked to DIOn.

5.5 Avionics Discrete I/O Option*

The ***BU-67x10F/I/T*** card includes eight Avionic Level Discrete I/O Channels that are individually programmable as inputs or outputs. Avionics Discrete digital I/O channel 1 is the LSB and channel 8 is the MSB for any software accesses to these signals. As outputs they are Open-Drain type drivers. When used as inputs these channels are configured to sense Ground / Open discrete inputs with +35V input voltage tolerance.

If an Avionics Discrete is used with an external Avionics Input, an external 2K ohm resistor should be connected between the AIO signal and system power to ensure full swing of the discrete signal, unless the other device has an internal pull-up of no greater than 2K ohms.

Avionics I/O channels 3-8 also function as RT address inputs for 1553 channel #1.

*** *BU-67X10MX*:** The following differences exist for the Rear I/O Version:

- Avionics I/O channels are limited to 0.5A capability per channel
- 16 Avionics I/O channels exist
- Avionics I/O Channels 11-16 also function as RT address inputs for 1553 Channel #2

(MF Option) The ***BU-67210* Multi-Function architecture also allows for the avionics discrete I/O signals to be linked to triggers. When a trigger is linked to a discrete I/O, the number of the trigger is the same as the number of the discrete I/O, i.e. GPTn is linked to DIOn.

5.6 External 10 MHz Time Tag Clock Input

Besides an internal clock source for the time tag counter, the ***BU-67x10F/M/I/T*** provides support for an external time tag clock with an external counter reset control. This external time tag clock input may be driven by a 10 MHz clock source to implement relative time stamps as defined in IRIG-106 Chapter 10. These signals are internally pulled-up to +3.3V and are +5V tolerant.

To switch the time tag counter to use the external clock and clock enable signals, please see the aceSetTimeTagRes() function in the "AceXtreme® C SDK Software Manual". When the time tag counter is switched to use the external signals, the following applies. Driving CLK_ENABLE_IN to a digital logic high enables the time tag counter to increment. The internal time tag register will increment on each rising edge of the external time tag clock while the CLK_ENABLE_IN is logic "1". Driving the CLK_ENABLE IN signal low will clear the time tag counter.

5.7 IRIG Time Code

IRIG-B, B123 time code standardization allows equipment to be synchronized to a known reference time. The ***BU-67x10F/M/I/T*** card can accept an IRIG-B input via digital signal or amplitude modulated (AM) coding on an audio sine wave carrier signal. Digital or demodulated analog data is read once per second.

The IRIG Time can be fed to the 1553 channels to be used as the Time-Tag instead of the local timers included for each channel.

Refer to the "AceXtreme® C SDK Software Manual" (document #MN-69092SX-002) for more information.

5.8 Test and Simulation ToolKit (BU-672XX Models Only)

5.8.1 BC Test and Sim Toolkit features

The Multi-Function AceXtreme® BC (***BU-67210*** option) provides for the following additional features:

- High Resolution Response Timeout
- Intermessage Routines
- Programmable Inter-message Gap Time
- Error Injection (See section 5.8.4)

- Triggers (See section 5.8.5)

5.8.1.1 BC High Resolution Response Timeout

The ***BU-67210F/M/I/T*** device supports a response timeout for the BC that is software programmable. The response timeout dictates how long the BC will wait for an RT status word. This allows the user control over when the BC will designate a particular message as a NO RESPONSE and move onto the next message. The longer response timeout values allow for operation over long buses and/or the use of repeaters. The BC supports a programmable timeout from 3.5 µseconds to 30 µseconds with a resolution of 0.5 µseconds.

5.8.1.2 BC Intermessage Routines (IMRs)

IMRs are events that occur upon completion of a BC message. The Multi-Function AceXtreme® Architecture can allow the execution of up to 2 IMRs. The following is a list of the available IMRs:

- Set/Clear Discrete I/Os
- Automatic retries upon failed messages
- Skip next message
- Interrupt on End of Message
- Set/Clear status bits
- Increment data table
- Set/Clear triggers

Refer to Table 13 in the BU-69092SX AceXtreme C SDK Software Manual (document# MN-69092SX-002) for a detailed summary of the ***BU-67210F/M/I/T***'s IMRs.

5.8.1.3 BC Inter-Message Gap Time

The inter-message gap time is defined as the time from the mid-parity bit crossing of the last word of one message to the time of the mid-sync crossing of the command word of the subsequent message. See Figure 11 below.

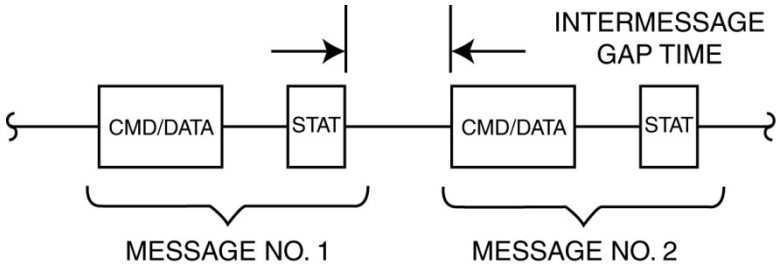


Figure 11. Inter-message Gap Time

To have a determinate time interval between messages, the new Multi-Function AceXtreme® Architecture allows the user to define this gap time. The inter-message gap time is programmable between 3.5 µseconds and 32,000 µseconds with a resolution of 0.5 µseconds.

5.8.2 Multi-RT Test and Sim Toolkit features

The Multi-Function AceXtreme BC (BU-67210 option) provides for the following additional features:

- High Resolution Response Timeout
- Intermessage Routines
- Programmable Inter-message Gap Time
- Error Injection (See section 5.8.4)
- Triggers (See section 5.8.5)

5.8.2.1 Multi-RT Programmable Response Times

The ***BU-67210F/M/I/T*** device supports a response time for the RTs that is software programmable. The RT response time is defined as the time it takes an RT to send back a status word as shown in Figure 12 below. The programmable response time allows the user control over when the RT will respond to a MIL-STD-1553 command word. The RT supports a programmable response time from 3.5 µseconds to 30 µseconds with a resolution of 0.5 µseconds.

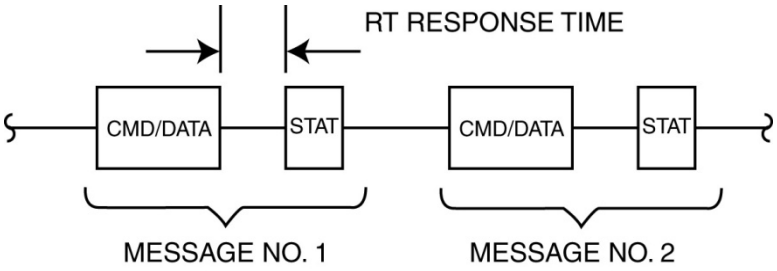


Figure 12. RT Response Time

5.8.2.2 Multi-RT High Resolution Response Timeout

The ***BU-67210F/M/I/T*** device supports an RT response timeout that is software programmable. Setting the RT's response timeout value is used for RT to RT commands. The RT response timeout dictates how long the RT will wait for an RT status word. The programmable response timeout allows the user control over when the RT will designate a particular message as a NO RESPONSE and wait for the next message. The RT supports a programmable timeout from 3.5 µseconds to 30 µseconds with a resolution of 0.5 µseconds.

5.8.2.3 Multi-RT Intermessage Routines (IMRs)

IMRs are events that occur upon completion of an RT message. The Multi-Function AceXtreme® Architecture can allow the execution of up to 2 IMRs. The following is a list of the available IMRs:

- Set/Clear Discrete I/Os
- Interrupt after mode code commands
- Store Time-Tag in a circular queue
- Set/Clear status bits
- Interrupt after accessing TX/RX data table
- Increment data table
- Set/Clear triggers

Refer to Table 57 in the ***BU-69092SX ACEXTREME C SDK SOFTWARE MANUAL*** (document #MN-69092SX-002) for a detailed summary of the ***BU-67210F/M/I/T***'s IMRs.

5.8.3 MT Advanced Error Sampling (AES)

The Monitor in the AceXtreme® Multi-Function product provides the additional ability to capture Advanced Errors using a sampling mode. The types of errors captured in this mode include Manchester, Parity, and general glitch errors. These errors can then be emulated using the Replay feature (See section 5.8). The AES mode generates the same packet header as MT-I but uses a slightly different packet trailer. The MT will determine if the message contains an error by using the error flag of the Block Status Word (BSW). If an error is detected, the MT will start sampling the bus at a 50 ns sample rate in order to capture this error.

5.8.4 Error Injection

Errors can be injected on either a BC message or via an RT response on the ***BU-67210F/M/I/T***. The error types that can be injected by the BC and RTs are Length errors and Encoding errors. Refer to Table 4 below for a list of available errors.

Length Errors include modifying data Word Count, or Bit Count Errors for a specific message.

Encoding Errors include Glitch or Inverse errors which can be anywhere in the message (command words, or data words). The Glitch and Inverse errors allow for error types such as invalid sync patterns, parity errors, and Manchester bi-phase errors.

Table 4. Error Injection Options

Error	Mode	Description	Value
Word Count	BC/RT	Increasing or decreasing the number of data words in a message.	-32 to +32 Words
Bit Count	BC/RT	Adding or removing bits from a specific word for a given message.	-3 to +3 Bits
Glitch	BC/RT	Forces the output of the encoder to an idle bus connection for a specific time period.	50 to 3000 ns (50 ns steps)
Inverse	BC/RT	Invert the output of the encoder for a specific time period.	50 to 3000 ns (50 ns steps)

5.8.5 Triggers

The ***BU-67210F/M/I/T*** has a new Trigger component in each channel as a part of the Multi-Function AceXtreme® Architecture.

Each channel can configure up to 18 different triggers. Each trigger configured can have up to twelve different available trigger events associated with it that would occur at the time the trigger condition

is met. Refer to Table 5 in the ***BU-69092SX ACEXTREME C SDK SOFTWARE MANUAL*** (document #MN-69092SX-002) for a detailed summary of the available trigger events.

Among the 18 triggers, two are Time-Message Triggers (TMT) and the other 16 are General Purpose Triggers (GPT).

The inputs to TMTs can be configured through software for either specific time intervals in either microseconds or milliseconds, or for a specified message count. The inputs to the GPTs can be message patterns captured by the monitor. As a result, the use of GPTs requires an MT running concurrently in the same channel. These message patterns are user-defined through software.

GPTs can also have discrete I/Os as their trigger input. A GPT can only have its corresponding discrete I/O number linked to its input, i.e. GPT0 can only be triggered by DIO0.

Both TMTs and GPTs can be triggered by another trigger's output.

A block diagram of the Trigger component can be found below in Figure 13.

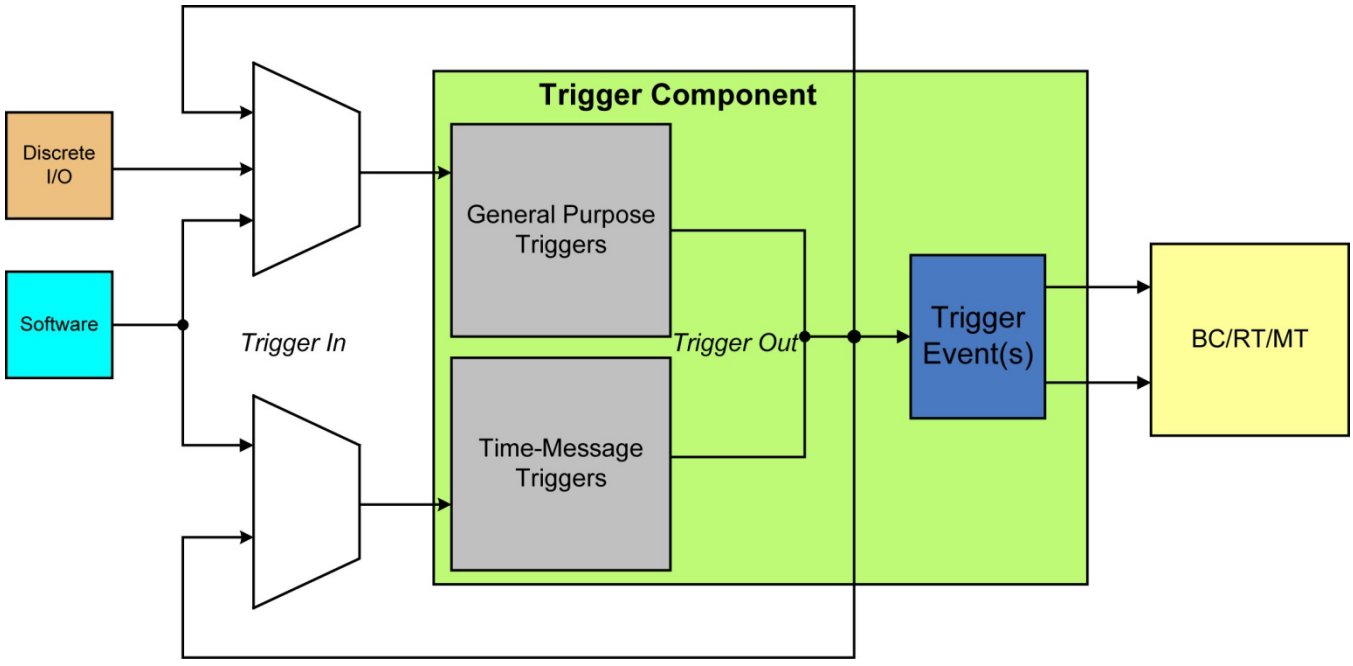


Figure 13. Trigger Component Block Diagram

5.8.6 Dynamic Bus Control

The Multi-Function AceXtreme® BC has the option to enable a user-specified RT address after receiving the DBC acceptance RT status. The RT that is to be enabled does not need to be currently inactive.

The Multi-Function AceXtreme Multi-RT allows for multiple RTs to be configured to accept a DBC request. To enable an RT with DBC a hold-off time must be specified. The hold-off time is defined as the time that an RT must wait after accepting a DBC request before deactivating itself and then activating the BC in the same channel. The hold-off time is software programmable from 40 µs to 130,000 µs.

5.8.7 Replay Function

The ***BU-67210*** Multi-Function AceXtreme Architecture provides the ability to replay bus traffic from captured IRIG 106 Chapter 10 packets. The MT-I mode has the capability to capture bus traffic data and store it into a file. The Replay function can use this file to replay the captured traffic data.

The Replay function has several configurable options and features such as the following:

1. Start/Reset/Pause/Stop replay activity
2. Emulate up to 31 RTs
3. Loop replay a specific number of times
4. Trigger conditions to start/stop replay activity
5. Replay message errors

The Replay engine will replay captured 1553 streams stored in IRIG106 Chapter 10 packet formats (See section 5.3.4.1). If the Advanced Error Sampling (AES) was enabled during the 1553 stream capture, the errors will be replayed. A software configurable option allows for the Replay engine to skip packets containing errors when AES was enabled. If AES was not enabled during the capture then all errors are automatically ignored during Replay.

In order to play back traffic, the user will need to configure the BC for replay mode and input a valid file containing a captured 1553 stream. See the **acexBCReplayStart()** function in the AceXtreme® C SDK software manual for detailed information.

5.9 Board Configuration

Although the PCI interface is automatically configured by the system, there are other configuration options which the user must manually configure.

5.9.1 Board Physical Jumpers

A right angle jumper block, **W2**, is located on the main component side of the card, across the board from the PN1 and PN2 connectors. It controls basic functionality, as dictated below in the table.

Table 5. W2 Jumper Block Description for the BU-67x10F/I/T

Pins	Jumper	Description
1-2	A	BOOT From BACKUP – If installed, allows the card to utilize the backup Firmware image installed on the card at the factory.
3-4	B	Do NOT install – Reserved for Factory use
5-6	C	FLASH Write Enable – If installed, enables Flash writes to update the card Firmware image

Table 6. W2 Jumper Block Description for the BU-67x10M

Pins	Jumper	Description

1-2	A	BOOT From BACKUP – If installed, allows the card to utilize the backup Firmware image installed on the card at the factory.
3-4	B	FLASH Write Enable – If installed, enables Flash writes to update the card Firmware image

5.9.2 Board Soft Jumpers

These cards have "soft jumpers" in the onboard Flash memory. The soft jumpers are manipulated via a configuration utility included in the ***BU-69092SX*** Software Package. For more information on the utility programs please reference DDC's application note *AN/B-50: AceXtreme® Transmit Inhibit and Bus Controller Disable Features*, available for download from DDC's BU-67x10F/M/I/T product web page (Direct document link – http://www.ddc-web.com/Pub/211/560.ashx).

The soft jumpers are write protected via the same mechanism as the rest of the Flash memory: via the Flash Write Enable jumper (Table 5) and FLASH_WRITE_EN_L signal (Table 7).

The soft jumpers can control the following:

- Tx Inhibit
- BC disable Hardware

After reset, the soft jumpers are read by the on-board AceXtreme channel logic from the reserved, write protected, flash locations to implement TX Inhibit and/or BC disable.

5.10 Card I/O Pinouts

This section delineates the pinouts for the card. The front-panel configuration (***BU-67x10F/I/T***) has a 68-pin "SCSI-II" type I/O connector. The rear-panel version (***BU-67x10M***) uses the PMC Pn4 connector.

Only the Pn4 and front panel P1 connectors are described in the following pages. The PMC specific Pn1 & Pn2 pinouts are listed in the IEEE P1386.1 specification.

5.10.1 Signal List

Table 7 dictates the pinouts of the Pn4 connector for the ***BU-67x10M8***, and the P1 connector for the ***BU-67x10F/I/T8***. As 1553 channels are reduced, they are removed from the highest 1553 channel number first.

Table 7. Connector Pinouts			
SIGNAL NAME	**Pn4 Pin**	**P1 Pin**	**Description**
1553_CH1A_BUS_MINUS	50	35	1553 Channel 1A Negative side
1553_CH1A_BUS_PLUS	52	37	1553 Channel 1A Positive side
1553_CH1B_BUS_MINUS	16	36	1553 Channel 1B Negative side
1553_CH1B_BUS_PLUS	18	38	1553 Channel 1B Positive side
1553_CH2A_BUS_MINUS	36	1	1553 Channel 2A Negative side
1553_CH2A_BUS_PLUS	38	3	1553 Channel 2A Positive side
1553_CH2B_BUS_MINUS	22	2	1553 Channel 2B Negative side
1553_CH2B_BUS_PLUS	24	4	1553 Channel 2B Positive side
1553_CH3A_BUS_MINUS	44	51	1553 Channel 3A Negative side
1553_CH3A_BUS_PLUS	42	49	1553 Channel 3A Positive side
1553_CH3B_BUS_MINUS	48	45	1553 Channel 3B Negative side
1553_CH3B_BUS_PLUS	46	47	1553 Channel 3B Positive side
1553_CH4A_BUS_MINUS	12	44	1553 Channel 4A Negative side
1553_CH4A_BUS_PLUS	8	46	1553 Channel 4A Positive side
1553_CH4B_BUS_MINUS	40	11	1553 Channel 4B Negative side
1553_CH4B_BUS_PLUS	25	13	1553 Channel 4B Positive side
1553_CH5A_BUS_MINUS	56	59	1553 Channel 5A Negative side
1553_CH5A_BUS_PLUS	55	61	1553 Channel 5A Positive side
1553_CH5B_BUS_MINUS	54	60	1553 Channel 5B Negative side
1553_CH5B_BUS_PLUS	53	62	1553 Channel 5B Positive side
1553_CH6A_BUS_MINUS	30	27	1553 Channel 6A Negative side
1553_CH6A_BUS_PLUS	32	29	1553 Channel 6A Positive side
1553_CH6B_BUS_MINUS	26	26	1553 Channel 6B Negative side
1553_CH6B_BUS_PLUS	28	28	1553 Channel 6B Positive side
1553_CH7A_BUS_MINUS	64	65	1553 Channel 7A Negative side
1553_CH7A_BUS_PLUS	63	67	1553 Channel 7A Positive side
1553_CH7B_BUS_MINUS	62	66	1553 Channel 7B Negative side
1553_CH7B_BUS_PLUS	61	68	1553 Channel 7B Positive side
1553_CH8A_BUS_MINUS	60	31	1553 Channel 8A Negative side
1553_CH8A_BUS_PLUS	59	33	1553 Channel 8A Positive side
1553_CH8B_BUS_MINUS	58	32	1553 Channel 8B Negative side
1553_CH8B_BUS_PLUS	57	34	1553 Channel 8B Positive side

Table 7. Connector Pinouts			
SIGNAL NAME	**Pn4 Pin**	**P1 Pin**	**Description**
(BU-67X10MX) AV_DIS_I/O_9 (All Other P/N's) DIS_I/O_1	3	6	(BU-67X10MX) Avionics Discrete I/O 9 (+35V) (All Other P/N's) Discrete I/O 1 (Digital Logic levels)
(BU-67X10MX) AV_DIS_I/O_10 (All Other P/N's) DIS_I/O_2	19	40	(BU-67X10MX) Avionics Discrete I/O 10 (+35V) (All Other P/N's) Discrete I/O 2 (Digital Logic levels)
1.1 (BU-67X10MX) AV_DIS_I/O_11 /CH2_RTAD0 (All Other P/N's) DIS_I/O_3 /CH2_RTAD0	1	7	**I/O Signal** - (BU-67X10MX) Avionics Discrete I/O 11 (+35V) - (All Other P/N's) Discrete I/O 3 (Digital Logic levels) **RT Address Input** - (Upon Reset) Channel 2 External RT Address Input bit 0
(BU-67X10MX) AV_DIS_I/O_12 /CH2_RTAD1 (All Other P/N's) DIS_I/O_4 /CH2_RTAD1	5	41	**1.2 I/O Signal** - (BU-67X10MX) Avionics Discrete I/O 12 (+35V) - (All Other P/N's) Discrete I/O 4 (Digital Logic levels) **1.3 RT Address Input** - (Upon Reset) Channel 2 External RT Address Input bit 1
(BU-67X10MX) AV_DIS_I/O_13 /CH2_RTAD2 (All Other P/N's) DIS_I/O_5 /CH2_RTAD2	9	53	**I/O Signal** - (BU-67X10MX) Avionics Discrete I/O 13 (+35V) - (All Other P/N's) Discrete I/O 5 (Digital Logic levels) **RT Address Input** - (Upon Reset) Channel 2 External RT Address Input bit 2
(BU-67X10MX) AV_DIS_I/O_14 /CH2_RTAD3 (All Other P/N's) DIS_I/O_6 /CH2_RTAD3	13	42	**I/O Signal** - (BU-67X10MX) Avionics Discrete I/O 14 (+35V) - (All Other P/N's) Discrete I/O 6 (Digital Logic levels) **RT Address Input** - (Upon Reset) Channel 2 External RT Address Input bit 3
(BU-67X10MX) AV_DIS_I/O_15 /CH2_RTAD4 (All Other P/N's) DIS_I/O_7 /CH2_RTAD4	17	9	**I/O Signal** - (BU-67X10MX) Avionics Discrete I/O 15 (+35V) - (All Other P/N's) Discrete I/O 7 (Digital Logic levels) **RT Address Input** - (Upon Reset) Channel 2 External RT Address Input bit 4
(BU-67X10MX) AV_DIS_I/O_16 /CH2_RTADP (All Other P/N's) DIS_I/O_8 /CH2_RTADP	21	43	**I/O Signal** - (BU-67X10MX) Avionics Discrete I/O 16 (+35V) - (All Other P/N's) Discrete I/O 8 (Digital Logic levels) **RT Address Input** - (Upon Reset) Channel 2 External RT Address Odd Parity
AV_DIS_I/O_1	27	16	Avionics Discrete I/O 1 (+35V)

Table 7. Connector Pinouts			
SIGNAL NAME	**Pn4 Pin**	**P1 Pin**	**Description**
AV_DIS_I/O_2	34	18	Avionics Discrete I/O 2 (+35V)
AV_DIS_I/O_3/CH1_RTAD0	35	20	Dual-Function signal: - Avionics Discrete I/O 3 (+35V) - (Upon Reset) Channel 1 External RT Address Input bit 0
AV_DIS_I/O_4/CH1_RTAD1	39	22	Dual-Function signal: - Avionics Discrete I/O 4 (+35V) - (Upon Reset) Channel 1 External RT Address Input bit 1
AV_DIS_I/O_5/CH1_RTAD2	43	12	Dual-Function signal: - Avionics Discrete I/O 5 (+35V) - (Upon Reset) Channel 1 External RT Address Input bit 2
AV_DIS_I/O_6/CH1_RTAD3	47	14	Dual-Function signal: - Avionics Discrete I/O 6 (+35V) - (Upon Reset) Channel 1 External RT Address Input bit 3
AV_DIS_I/O_7/CH1_RTAD4	51	8	Dual-Function signal: - Avionics Discrete I/O 7 (+35V) - (Upon Reset) Channel 1 External RT Address Input bit 4
AV_DIS_I/O_8/CH1_RTADP	29	10	Dual-Function signal: - Avionics Discrete I/O 8 (+35V) - (Upon Reset) Channel 1 External RT Address Input ODD Parity
CLK_ENABLE_IN	4	24	External Time-Tag Counter enable: 0 = Time-Tag counter reset (when external) 1 = Time-Tag counter enabled (when external)
EXT_CLK_OUT	14	25	10MHz synchronous clock output. This clock is synchronous to the internal clock.
EXT_CLK_IN	11	57	External Time-Tag clock input
IRIG_OUT	2	55	Digital IRIG-B time code output. This output complies with IRIG-200-04
IRIG_DIG	10	58	Digital IRIG-B time code input supporting 48-bit time-tags. If using PWM IRIG-B signal, then connect to this input and leave the IRIG_MOD signal unconnected.
IRIG_MOD	6	63	Modulated IRIG-B time code input supporting 48-bit time-tags. If using AM Modulated IRIG-B signal, then connect to this input and leave the IRIG_DIG signal unconnected.
FLASH_WRITE_EN_L	15	NA	Flash Write enable control 0 = Flash Write enabled 1 = Flash Write disabled

Table 7. Connector Pinouts			
SIGNAL NAME	**Pn4 Pin**	**P1 Pin**	**Description**
GND	7, 20, 23, 31, 33, 37, 41, 45, 49	5, 15, 17, 19, 21, 23, 30, 39, 48, 50, 52, 54, 56, 64	Ground reference connection

5.10.2 Rear Pn4 IO Version (M)

5.10.2.1 Rear Pn4 I/O Connector

Model ***BU-67x10M*** provides rear I/O via connector "Pn4". This connector (Soldered on the board) is a 64-pin "Mezzanine IEEE 1386 Board-to-Board Plug, Dual Row, SMT Vertical Stacking" (Molex P/N 71436-2164). See Figure 14 for connector location and pin numbering. See Table 7 for pinouts.

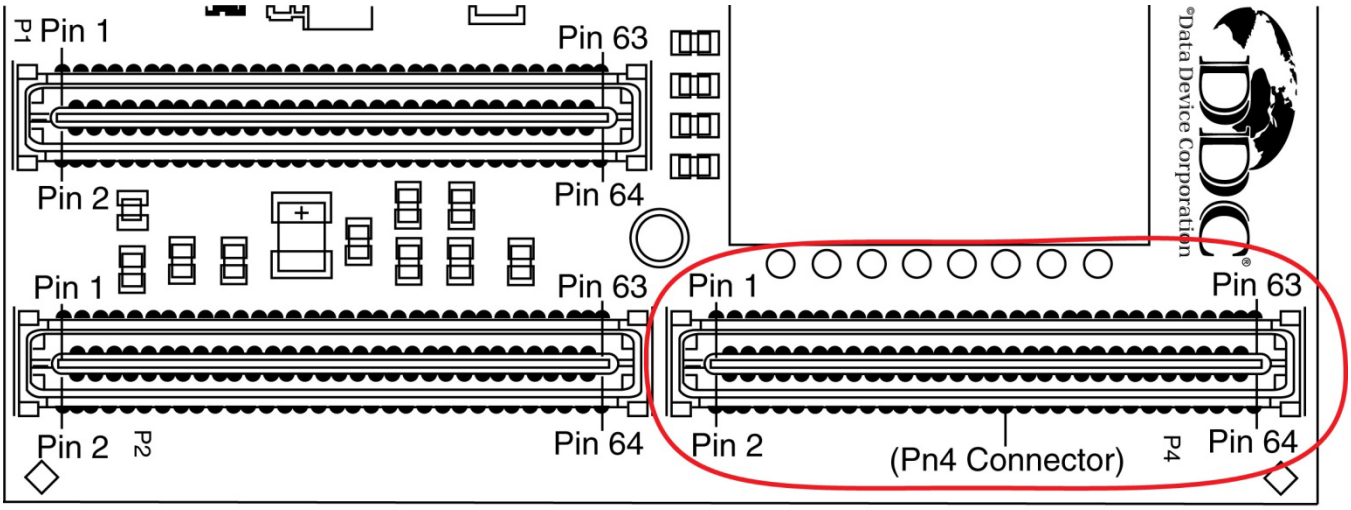


Figure 14. "Pn4" I/O Connector location/orientation

(Viewed from component side of card, typical card shown)

5.10.3 Front Panel Version (F)

5.10.3.1 Front Panel I/O Connector

The ***BU-67x10F/i/T*** models include a front-panel I/O, 68-contact, "SCSI-II" type connector. This connector (Soldered on the board) is a female 68-contact: TE Connectivity 5787170-7 or equivalent.

Pin numbering designations for the connector are as shown in Figure 15. The board-mounted connector comes with screw locks , allowing for positive retention of the mating cable/connector.

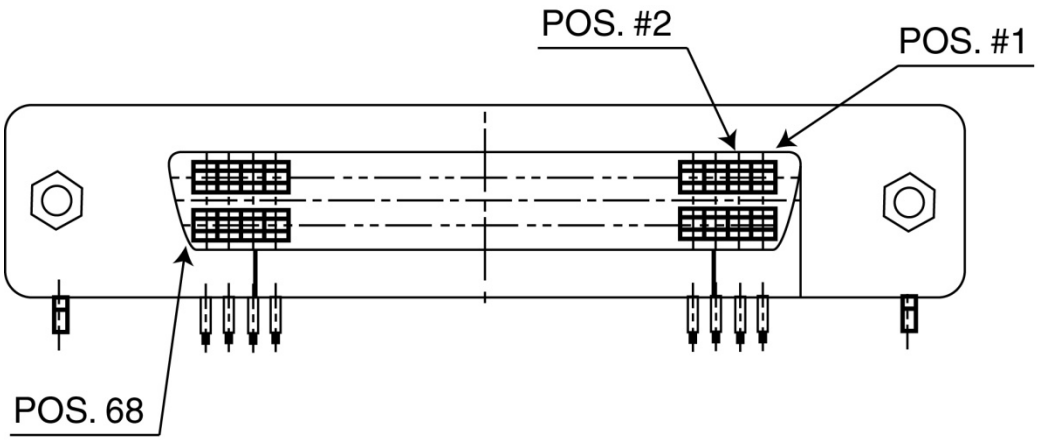


Figure 15. Front panel 68-Pin I/O Connector Pin Locations

(Viewed from Front panel of card)

5.10.3.2 Supplied I/O connector components

Front-panel versions of the card (***BU-67x10F, BU-67x10i*** and ***BU-67x10T***) are supplied with the mating I/O connector components as listed in Table 8. These components may be used to construct a cable to interface to the I/O on the card. A breakout cable (see Section 5.10.4) is also included with the ***BU-67X10i*** and ***BU-67x10T*** and can optionally be ordered for the ***BU-67x10F***.

Table 8. Supplied I/O Connector Components

Connector Description	Part Number
68-Position Male IDC type Connector Kit with Backshell	TE Connectivity 2053345-1 Contains TE 5750752-1 Contains TE 5750913-7

5.10.4 Interface Cables

The front panel version (***BU-67x10F***) of the interface card can be ordered with an optional cable assembly that interfaces directly to the PMC Card. The ***BU-67x10i*** and ***BU-67x10T*** always include this cable. This section describes these optional “breakout” type cable assemblies. DDC Part Numbers for the cable assembly are listed in Table 9. Details for the J1 connector of these assemblies are listed in Table 10.

Three versions of the cables are available for the different 1553 channel counts. Cables supporting 2, 4, and 8 1553 channels are available.

These cables are available in leaded or ROHS compliant versions.

Standard ***BU-67x10F*** versions with MIL-STD-1553 channels are built with isolation transformers that are designed for transformer coupling (long stub) to the actual 1553 bus. The transformer coupling of the bus to the ***BU-67x10F's*** stub is a reference to the need for an external transformer referred to as a "coupling transformer". In accordance with MIL-STD-1553B, the turns ratio of the coupling transformer is 1:1.4

The 1553 mating connector required on the customer supplied stub cable is a Trompeter PL75 or equivalent connector. Two are required per dual-redundant 1553 channel.

Table 9. Interface Cable Assemblies

Card Version	Cable Part Number
Leaded (L)	
BU-67x10F/i/T1L or BU-67x10F/i/T2L	DDC-75767-3
BU-67110F/i/T4L	DDC-75767-2
BU-67210F/i/T4L	DDC-75767-4
BU-67110F/i/T8L	DDC-75767-1
ROHS (R)	
BU-67x10F/i/T1R or BU-67x10F/i/T2R	DDC-75767-7
BU-67110F/i/T4R	DDC-75767-6
BU-67210F/i/T4R	DDC-75767-8
BU-67110F/i/T8R	DDC-75767-5
The cable can be ordered together with the PMC card, or as a separate line item at a later date.	

Table 10. J1 Cable Connector Details

Manufacturer PN	Type	Description
Positronic SD37F00000	Female Connector	J1
Positronic SD37MXXXXX	Male Connector	J1 Mate
AMP/TYCO 167296-1	Male Connector	Mating housing to J1
AMP/TYCO 166053-1	Male Pins (20-24AWG)	Inserted pins for Male housing
AMP/TYCO 166054-1	Male Pins (24-28AWG)	Inserted pins for Male housing

Please see Table 7 for definitions of the Signal Names below in Table 11.

Table 11. Cable Assembly DDC-75767-X J1 Pinout	
J1 Pin	**Signal Name**
J1-1	AV_DIS_I/O_7/CH1_RTAD4
J1-2	GND
J1-3	AV_DIS_I/O_8/CH1_RTADP
J1-4	(BU-67X10MX) AV_DIS_I/O_9 (All Other P/N's) DIS_I/O_1
J1-5	AV_DIS_I/O_5/CH1_RTAD2
J1-6	(BU-67X10MX) AV_DIS_I/O_11 /CH2_RTAD0 (All Other P/N's) DIS_I/O_3 /CH2_RTAD0
J1-7	AV_DIS_I/O_6/CH1_RTAD3
J1-8	(BU-67X10MX) AV_DIS_I/O_15 /CH2_RTAD4 (All Other P/N's) DIS_I/O_7 /CH2_RTAD4
J1-9	GND
J1-10	GND
J1-11	AV_DIS_I/O_1
J1-12	CLK_ENABLE_IN
J1-13	GND
J1-14	EXT_CLK_OUT
J1-15	AV_DIS_I/O_2
J1-16	GND
J1-17	GND
J1-18	GND
J1-19	AV_DIS_I/O_3/CH1_RTAD0
J1-20	(BU-67X10MX) AV_DIS_I/O_10 (All Other P/N's) DIS_I/O_2
J1-21	AV_DIS_I/O_4/CH1_RTAD1
J1-22	(BU-67X10MX) AV_DIS_I/O_12 /CH2_RTAD1 (All Other P/N's) DIS_I/O_4 /CH2_RTAD1
J1-23	GND

Table 11. Cable Assembly DDC-75767-X J1 Pinout	
J1 Pin	**Signal Name**
J1-24	(BU-67X10MX) AV_DIS_I/O_14 /CH2_RTAD3 (All Other P/N's) DIS_I/O_6 /CH2_RTAD3
J1-25	GND
J1-26	(BU-67X10MX) AV_DIS_I/O_16 /CH2_RTADP (All Other P/N's) DIS_I/O_8 /CH2_RTADP
J1-27	GND
J1-28	(BU-67X10MX) AV_DIS_I/O_13 /CH2_RTAD2 (All Other P/N's) DIS_I/O_5 /CH2_RTAD2
J1-29	GND
J1-30	IRIG_OUT
J1-31	GND
J1-32	GND
J1-33	EXT_CLK_IN
J1-34	IRIG_DIG
J1-35	IRIG_MOD
J1-36	GND
J1-37	NC

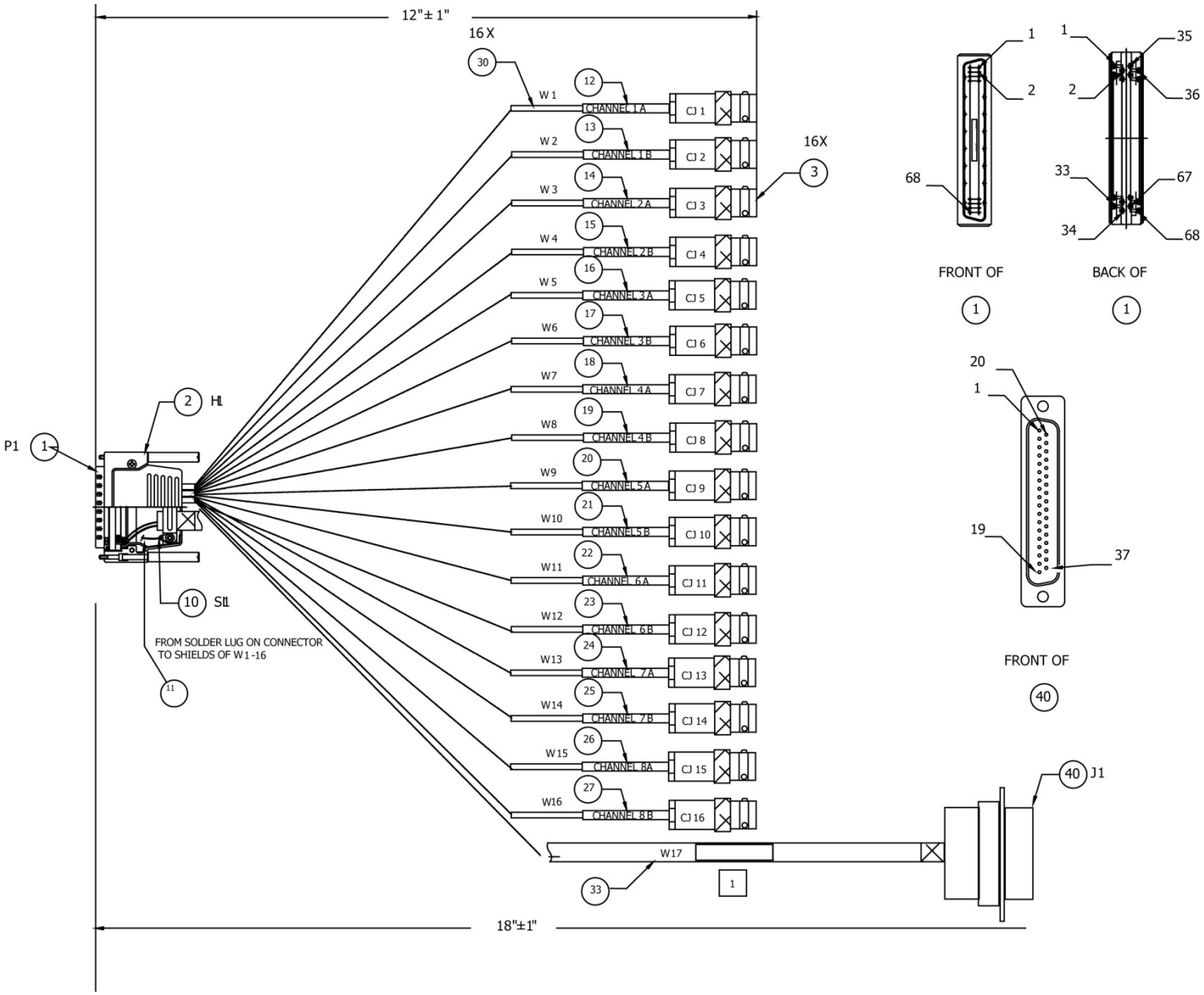


Figure 16. Eight 1553 channel Interface Cable Assembly DDC-75767-1 and DDC-75767-5

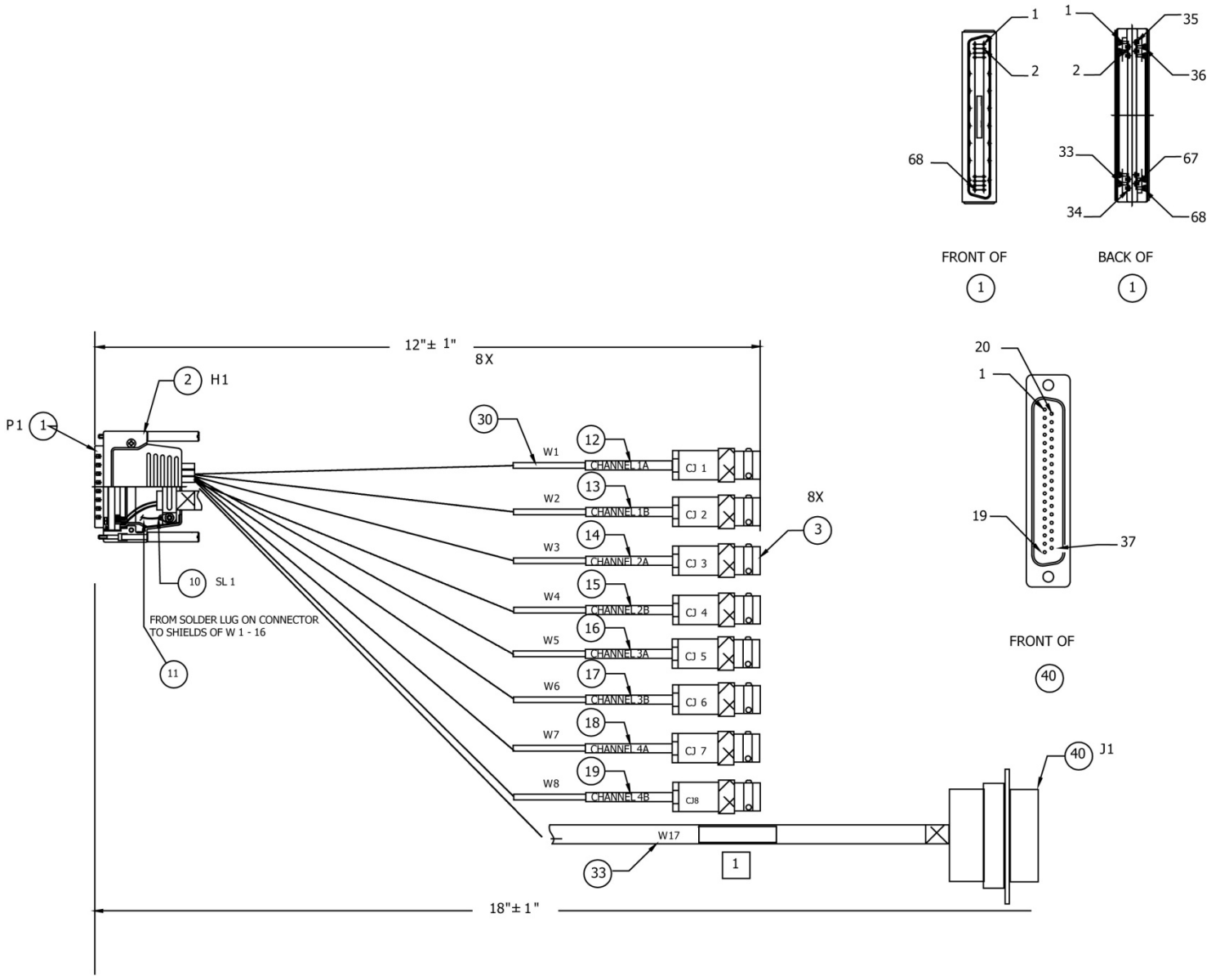


Figure 17. Four 1553 channel Interface Cable Assembly DDC-75767-2 DDC-75767-4 and DDC-75767-6 / DDC-75767-8

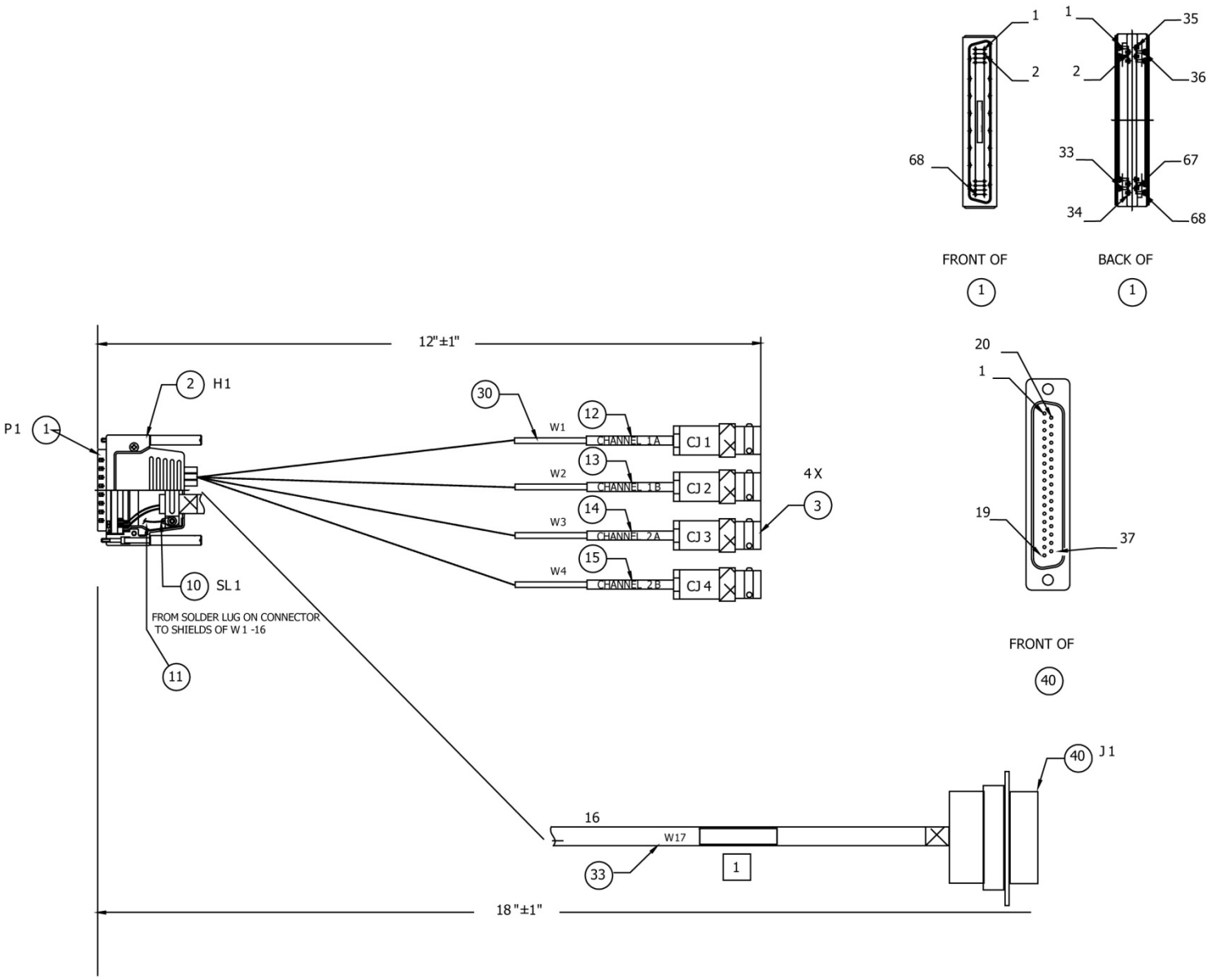


Figure 18. Two 1553 channel Interface Cable Assembly DDC-75767-3 and DDC-75767-7

6 ORDERING INFORMATION

BU-67X 10X XX0X-JL0 (PCI and 3U cPCI/PXI)

JL = 0°C to +55°C Card

R = RoHS

(See Note 1)

I/O Option	# of 1553 Channels	# of Avionics Discrete I/O	# of Digital Discrete I/O
10	1	8	8
20	2	8	8
40	4	8	8
80 note 1	8	8	8

I = PCI Card

T = 3U cPCI/PXI Card

BU-67X 10F XX0X-XX0X (Front I/O PMC)

N = Acrylic Conformal Coating

U = Polyurethane Conformal Coating

Blank = No Conformal Coating

2A = Rugged Air Cooled (-40°C to +85°C) note 4

3L = Air Cooled (0°C to +71°C)

(See Note 1)

L = Leaded

R = RoHS (only available with -3L option)

I/O Option	# of 1553 Channels	# of Avionics Discrete I/O	# of Digital Discrete I/O
10	1	8	8
20	2	8	8
40	4	8	8
80 note 1	8	8	8

BU-67X 10M XX0X-2X0X (Rear I/O PMC)

N = Acrylic Conformal Coating

U = Polyurethane Conformal Coating

Blank = No Conformal Coating

A = Rugged Air Cooled (-40°C to +85°C)

C = Rugged Conduction Cooled (-40°C to +85°C)

(See Note 1)

L = Leaded

I/O Option	# of 1553 Channels	# of Avionics Discrete I/O	# of Digital Discrete I/O
10	1	8	8
20	2	8	8
21	2	16	0
40	4	8	8
41	4	16	0
80 note 1	8	8	8

Notes:

1. 672 = AceXtreme Multi-Function (BC + Multi-RT + MT), not available with 8 MIL-STD-1553 Channels
   671 = AceXtreme Single-Function (BC/MT or Multi-RT/MT)
2. All Models include IRIG-B Input/Output
3. PCI and cPCI Models Include Cables
4. Only Available with Leaded Board

Included Accessories:

For the BU-67x10F/i/T versions:

- 1 Mating Connector and Backshell

For the BU-67x10i/T versions:

- 1 Breakout Cable

Included Software:

BU-69092SX- AceXtreme® C Software Development Kit (SDK)

Operating System:

0 = Windows 10/11
1 = Linux
2 = VxWorks

Optional Software:

BU-694X4DS-64VM- *dataSIMS* (Avionics Data Bus Test and Analysis Software)

BU-69066S0-XX0- BusTrACEr™ (Data Bus Analyzer and Monitor)

BU-69093S0-XX0- LabVIEW® Support Package

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Industry documents used to support DDC's certifications and Quality system are: AS9001 OEM Certification, MIL-STD-883, ANSI/NCSL Z540-1, IPC-A-610, MIL-STD-202, JESD-22, and J-STD-020.





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