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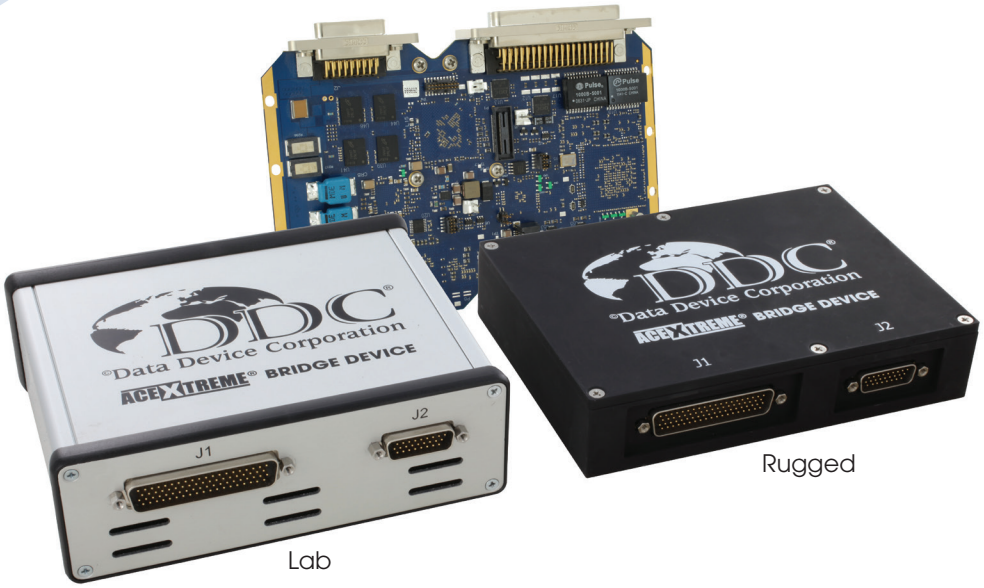
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# AceXtreme® Bridge Device

## Hardware Manual

**Model: BU-6711XWX**




MIL-STD-1553

ARINC 429

DISCRETE

ETHERNET

ACEXTREME®

DDC's AceXtreme Bridge Device can be used to bridge avionics messages in real time between Ethernet, MIL-STD-1553, and ARINC-429, in any direction, without the need for a host computer.

## Applications

- Upgrade & Retrofit
- Protocol Conversion
- Mission Computers
- Displays
- Test & Systems Integration
- Situational Awareness
- Simulators
- Data Loading
- Data Monitoring

**Custom Design Capability** - DDC can customize designs for all cards, ranging from simple modifications of standard products to fully customized solutions for commercial, military, aerospace, and industrial applications.

**For more information:** www.ddc-web.com/6711XWX

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# DDC's Data Networking Solutions

## MIL-STD-1553 | ARINC 429 | Fibre Channel

As the leading global supplier of data bus components, cards, and software solutions for the military, commercial, and aerospace markets, DDC's data bus networking solutions encompass the full range of data interface protocols from MIL-STD-1553 and ARINC 429 to USB, and Fibre Channel, for applications utilizing a spectrum of form-factors including PMC, PCI, Compact PCI, PC/104, ISA, and VME/VXI.

DDC has developed its line of high-speed Fibre Channel and Extended 1553 products to support the real-time processing of field-critical data networking netween sensors, compute notes, data storage displays, and weapons for air, sea, and ground military vehicles.

Whether employed in increased bandwidth, high-speed serial communications, or traditional avionics and ground support applications, DDC's data solutions fufill the expanse of military requirements including reliability, determinism, low CPU utilization, real-time performance, and ruggedness within harsh environments. Out use of in-house intellectual property ensures superior mutli-generational support, independent of the life cycles of commercial devices. Moreover, we maintain software compatibility between product generations to protect our customers' investments in software development, system testing, and end-product qualification.

### *MIL-STD-1553*

DDC provides an assortment of quality MIL-STD-1553 commercial, military, and COTS grade cards and components to meet your data conversion and data interface needs. DDC supplies MIL-STD-1553 board level products in a variety of form factors including AMC, USB, PCI, cPCI, PCI-104, PCMCIA, PMC, PC/104, PC/104-Plus, VME/VXI, and ISAbus cards. Our 1553 data bus board solutions are integral elements of military, aerospace, and industrial applications. Our extensive line of military and space grade components provide MIL-STD-1553 interface solutions for microprocessors, PCI buses, and simple systems. Our 1553 data bus solutions are designed into a global network of aircraft, helicopter, and missle programs.

### *ARINC 429*

DDC also has a wide assortment of quality ARINC-429 commercial, military, and COTS grade cards and components, which will meet your data conversion and data interface needs. DDC supplies ARINC-429 board level products in a variety of form factors including AMC, USB, PCI, PMC, PCI-104, PC/104 Plus, and PCMCIA boards. DDC's ARINC 429 components ensure the accurate and reliable transfer of flight-critical data. Our 429 interfaces support data bus development, validation, and the transfer of flight-critical data aboard commercial aerospace platforms.

### *Fibre Channel*

DDC has developed its line of high-speed Fibre Channel network access controllers and switches to support the real-time processing demands of field-critical data networking between sensors, computer nodes, data storage, displays, and weapons, for air, sea, and ground military vehicles. Fibre Channel's architecture is optimized to meet the performance,reliability, and demanding environmental requirements of embedded, real time, military applications, and designed to endure the multi-decade life cycle demands of military/aerospace programs.



# BU-67115W/BU-67116W/BU-67119W
# ACEXTREME BRIDGE DEVICE
# HARDWARE MANUAL

## MN-6711XWX-001

The information provided in this Manual is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise connection therewith.

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| Rev B | 6/2013 | 14 | Added Figure 7 |
| Rev C | 2/2014 | 3-5, 7-9, 11-23, 28, 31, 39-40, 43, 47, 49, 50-51, 53, 60-61 | Removed “Future” product and feature references. Updated Figure 1. Updated Tables 1, 3, 11, 12, and 14. Combined Tables 12 and 13. Removed Table 17. |
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# 1 PREFACE

This manual uses typographical conventions to assist the reader in understanding the content. This section will define the text formatting used in the rest of the manual.

## 1.1 Text Usage

- BOLD–indicates important information and table, figure, and chapter references.
- BOLD ITALIC–designates DDC Part Numbers.
- Courier New–indicates code examples.
- <…> - indicates user-entered text or commands.

## 1.2 Standard Definitions

**PCI** Peripheral Component Interconnect Express

## 1.3 Special Handling and Cautions

The ***BU-67115Wx*** and ***BU-67119Wx*** use state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.




*Warnings: For the* **BU-67119Wx** *(lab) version only, turn the unit off. For all versions, unplug the power adapter from the wall.*

*When handling the* ***BU-67116Wx*** *embedded board version, ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.*

*Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.*

## 1.4 Trademarks

All trademarks are the property of their respective owners.

## 1.5 What is included in this manual?

This manual contains a complete description of the AceXtreme Bridge Device's hardware installation and use.

## 1.6 Technical Support

In the event that problems arise beyond the scope of this manual, you can contact DDC by the following:

US Toll Free Technical Support:
1-800-DDC-5757, ext. 7771

Outside of the US Technical Support:
1-631-567-5600, ext. 7771

Fax:
1-631-567-5758 to the attention of DATA BUS Applications

DDC Website:
www.ddc-web.com/ContactUs/TechSupport.aspx

Please note that the latest revisions of Software and Documentation are available for download at DDC's Web Site, www.ddc-web.com.

# 2 OVERVIEW

The ***BU-67115Wx, BU-67116Wx*** and ***BU-67119Wx*** are different versions of DDC's AceXtreme Bridge Device (ABD). The ***BU-67119Wx*** non-ruggedized module is for lab and production test applications. The ***BU-67115Wx*** enclosed ruggedized module is for embedded applications, and the ***BU-67116Wx*** ruggedized board is also for embedded applications.

The ***BU-67119Wx*** operates over an ambient air temperature range of 0°C to +55° C, and includes an internal fan. The operating ambient air temperature range for the ***BU-67115Wx*** box is -40°C to +71°C. The operating case temperature range for the ***BU-67115Wx*** box, and the operating thermal rail temperature for the ***BU-67116Wx*** board is -40°C to +85°C.

The ABD is available in a variety of channel configurations. All configurations include two 10/100/1000 Ethernet channels. Further, there are ordering options for one or two dual redundant MIL-STD-1553 channels, and for six ARINC 429 channels. Additional ordering options include for leaded or RoHS, and for conformal coating (acrylic, urethane, or none).

The ABD's MIL-STD-1553 channels can operate as BC, combined BC and Monitor, single RT, Multi-RT (up to 32) and combined single or Multi-RT and Monitor. All ARINC 429 channels may be independently programmed for either transmit or receive operation. The ABD includes an IRIG-B time synchronization input, along with an option to configure the MIL-STD-1553 RT Address inputs to operate as up to 12 discrete digital I/Os.

The ABD offers a high degree of flexibility, and is therefore suitable for a wide range of embedded and lab applications. The ABD includes a Remote Access Mode, in addition to the Protocol Conversion Mode. For use in conjunction with Remote Access mode, DDC also offers multiple interactive GUI software programs.

In Protocol Conversion Mode, the ABD is configured to provide autonomous communication bridging from any input channel(s) to any other channel(s). To minimize setup time and provide turnkey operation, the ABD includes a high-level bridging API. Alternatively, users may develop their own bridging applications by means of DDC's AceXtreme MIL-STD-1553 and/or ARINC 429 APIs, along with Linux TCP/IP and UDP/IP socket interfaces for the ABD's two Ethernet channels.

In Remote Access Mode, users are able to develop applications running on a remote computer communicating over Ethernet to the ABD's MIL-STD-1553 and/or ARINC 429 channels. In the remote access configuration, the user is able to write applications running on a remote host invoking the AceXtreme MIL-STD-1553 and/or ARINC 429 APIs. As an alternative to developing application software, in Remote

Access Mode, the user is able to operate the ABD using any of DDC's GUI software programs. These include:

- **BusTrACEr**, a simple menu program for generating and monitoring MIL-STD-1553 messages. Further, BusTrACEr includes an option for the automatic generation of ANSI 'C' source code.
- ***dataSIMS*,** a software GUI tool for test and simulation applications. *dataSIMS* converts data to engineering units, allows the creation of graphical display formats, and may be used for either passive monitoring and/or simulation.
- **LabVIEW® Support**. The ***BU-69093S0-XX0*** software operates in conjunction with National Instruments' LabVIEW® system design software to provide a simple interface and easy programming of the ABD's MIL-STD-1553 and/or ARINC 429 interfaces. Users can either create their own custom interfaces "from scratch" or may modify the samples that are provided.
- **Commercial Avionics Utilities Software Package.** The ***DD-42999S0-XX0*** **Data Bus Analyzer and Data Loader GUI software** is for ARINC 429 data bus analysis and simulation. This GUI provides advanced filtering, message scheduling, and triggering. In addition, it includes a graphical ARINC 615 data loader, providing a software interface to load data to and from airborne computers.

## 2.1 Features

**General**

- Overall Configuration:
  - Two 10/100/1000 BASE-T Ethernet Channels
  - Options for One or Two MIL-STD-1553 Channels
  - Option for Six ARINC 429 Transmit or Receive Channels
  - Intel Atom E640T Processor
  - Embedded Linux Real Time Operating System
- Bridge Any Channel to Any Other Channel(s)
- Self-Contained Development Environment
- Lab and Rugged Versions
- Protocol Conversion Mode
  - Standalone "anything-to-anything" Bridge: Ethernet, 1553, ARINC 429
  - Bridging API for Turnkey Solutions
  - Ethernet Sockets, and 1553 and ARINC 429 APIs for added flexibility
  - Built-in Linux development environment
- Remote Access Mode

- Enables Communication Over Ethernet to/from 1553 and ARINC 429 Channels
- 1553 and ARINC 429 Software Drivers and/or GUIs Installed on Remote Host Computer

**MIL-STD-1553**

- One or Two Dual Redundant 1553 channels
  - Each 1553 channel can be independently programmed for BC, BC/MT, RT, Multi-RT, Monitor, RT/Monitor, or Multi-RT/Monitor operation.
  - Transformer-coupled 1553 bus connection (consult factory for direct-coupled).
- 2 MB RAM per 1553 Channel
- Each Dual Redundant MIL-STD-1553 Channel:
  - BC or Multi-RT with Concurrent Bus Monitor
  - Support of MIL-STD-1553 A/B, STANAG-3838, and MIL-STD-1760
  - 2 MB (64K x 36) Shared RAM
  - Transmit Inhibit Inputs for Monitor-only Applications
  - BC Disable Inputs for RT-only Applications
  - 48-bit/100ns Time Stamp
  - IRIG-106 Chapter 10 Monitor
- 1553 Bus Controller (BC)
  - Highly Autonomous Controller, with 32-Instruction Set
  - Streaming and Minor/Major Frame Scheduling of Messages
  - High and Low Priority Asynchronous Message Insertion
  - Modify Messages or Data While BC is running
- 1553 Remote Terminal (RT)
  - Emulate up to 31 RT Addresses Simultaneously
  - Multiple Buffering Techniques
  - Programmable Command Illegalization
  - Programmable Busy by Subaddress
  - Programmable Single Buffer, Double Buffer, Circular Buffer, or Global Circular Buffer by Subaddress
  - RT Auto-Boot for MIL-STD-1760
- 1553 Bus Monitor (MT)
  - IRIG-106 Chapter 10 Compatibility

  - Filter Based on RT Address, T/R bit, and Subaddress
  - 48-bit, 100 ns/LSB Time Stamping
  - Advanced Bit Level Error Detection to Isolate Bus Failures
- IRIG-B Clock
  - IRIG-B Digital Time Code Input Enables 1 Hz Synchronization
  - 48-bit resolution, with options of 64, 32, …1 µs/LSB; or 500, 250, or 100 ns/LSB
  - 100 ns/LSB resolution for IRIG 106 Chapter 10 Monitor
- Capability for Fast DMA Transfers between 1553 Channels' Shared RAM and Atom Processor Local Memory.
- API Compatible with **AceXtreme® SDK and Commercial Avionics SDK**

**ARINC 429**

- Six ARINC 429 channels programmable for Transmit or Receive operation
- Programmable High or Low Speed Operation for each ARINC 429 Channel
- Scheduled and FIFO ARINC 429 transmission
- FIFO and mailbox ARINC 429 reception

**Software**

- Linux Operating System and BSP
  - Ethernet Stacks, with UDP/IP and TCP/IP Sockets, Telnet, FTP, TFTP, SSH, and HCTP.
- DDC Protocol Bridging API, Providing Turnkey Bridging From Any Ethernet, 1553, or ARINC 429 Port to Any Other Port(s)
- DDC AceXtreme MIL-STD-1553 API, Including Sample Programs
- DDC ARINC 429 API, Including Sample Programs
- Built-in Editor, Allowing Editing and Saving Files Over Telnet
- Built-in 'C' Compiler

- Can transfer internal files to a host computer, edit remotely, and transfer files back to the ABD before compiling.

## 2.2 Top-Level Block Diagram

Figure 1 is the top-level functional block diagram of the AceXtreme Bridge Device (ABD). The ABD's CPU, an Intel E640T Atom processor, interfaces through four 1x PCI Express interfaces to the ABD's other major functional blocks.

One 1x PCIe interface services the ABD's MIL-STD-1553 and ARINC 429 channels, while a second PCIe link interfaces to the ABD's two 10/100/1000 Ethernet channels. A third PCI Express interface connects between the Atom processor and an Intel EG20T hub controller. The hub controller communicates with the ABD's solid state disk drive over a SATA interface. The processors' interface to on-board RAM is over a DDR2 interface.

The fourth PCIe interface enables the Atom to communicate with a card installed in the ABD's Mini-PCI Express expansion slot.

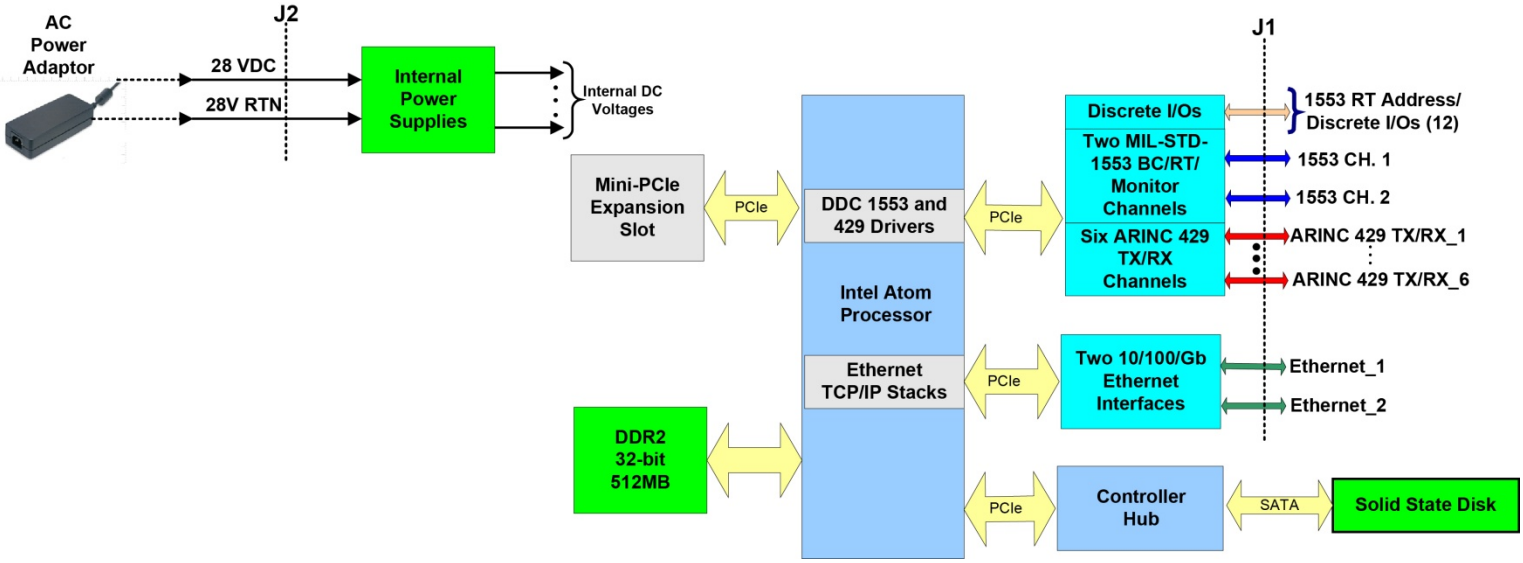



**Figure 1. AceXtreme Bridge Device Block Diagram**

## 2.3 System Requirements

### 2.3.1 System Requirements for Protocol Conversion Mode

- Remote computer with Ethernet interface and Telnet (only applicable for configuration mode).

### 2.3.2 System Requirements for Remote Access Mode

- Remote computer with Ethernet interface.
- Windows 2000/XP, Windows Vista 32/64-bit, Windows 7 32/64-bit, Linux, or VxWorks Operating System
    - Tornado software development environment for VxWorks platforms
- An appropriate compiler or development environment.
- Contact factory for additional operating systems

## 2.4 Applications

The ***BU-65119Wx*** lab module is a valuable tool for design and test teams involved with MIL-STD-1553 and/or ARINC 429 interfaces. The ***BU-67115Wx and BU-67116Wx*** devices' conduction cooling and ruggedized construction enabling operation over the industrial temperature range makes these ideal for use in mission computers, flight data recorders, ground vehicles, and other embedded systems that require a military grade module or card. The AceXtreme Bridge Device is the ideal solution for any application requiring an Ethernet-to-MIL-STD-1553 and/or ARINC 429 interface in a lab, production test, or embedded environment.

The design of the AceXtreme Bridge Device leverages the full capabilities of DDC's ***AceXtreme*** MIL-STD-1553 Architecture. Features include a highly autonomous BC with expanded instruction set, an RT or Multi-RT providing a wide variety of buffering options, a selective message monitor, IRIG-B time code input, and a 48-bit, 100 ns resolution Time Tag. Each ***AceXtreme*** channel contains 512K X 36 (2 MB) of RAM.

## 2.5 Configuration Options

- Generic P/N: BU-6711XWX00(L or R)
    - L = leaded; R = RoHS
- Mechanical/Environmental Options:
    - ***BU-67119Wx***: Lab box, RoHS only.
    - ***BU-67115Wx***: Embedded Box, with rugged connectors and either leaded or RoHS options.

- ***BU-67116Wx***: Embedded Board Only, with “D” connectors and either leaded or RoHS options.

- Channels Configuration:
  - W000 = 2 Ethernet, 6 ARINC 429
  - W100 = 2 Ethernet, 1 MIL-STD-1553
  - W200 = 2 Ethernet, 2 MIL-STD-1553
  - W300 = 2 Ethernet, 2 MIL-STD-1553, 6 ARINC 429

## 2.6 Mechanical Design and Qualification Testing

The ***BU-67115Wx*** chassis and ***BU-67116Wx*** card meets or exceeds vibration and shock requirements as specified by MIL-STD-810F. For vibration, the chassis and box are tested in accordance with MIL-STD-810F, Method 514.5, and Category 24. The minimum integrity test is in accordance with Figure 514.5C-17 for a duration of 60 minutes in each of the three orthogonal axes.

For shock, the chassis and box is tested in accordance with MIL-STD-810F, Table 516.5-1 and figure 516.5-8 “functional Test for Ground Equipment” for functional shock response spectrum (SRS) in each of three orthogonal axes.

The ***BU-67119Wx*** board (Figure 2 and Figure 3) is a non-ruggedized configuration intended for applications operating in a lab or other commercial environment.

The ***BU-67115Wx*** box and ***BU-67116Wx*** card (Figure 9) is designed to meet or exceed the humidity requirements of ANSI/VITA 47, and is tested to withstand 95% humidity as specified.




**Front view**




**Rear view**

**Figure 2. BU-67119Wx AceXtreme Bridge Device Lab Box**

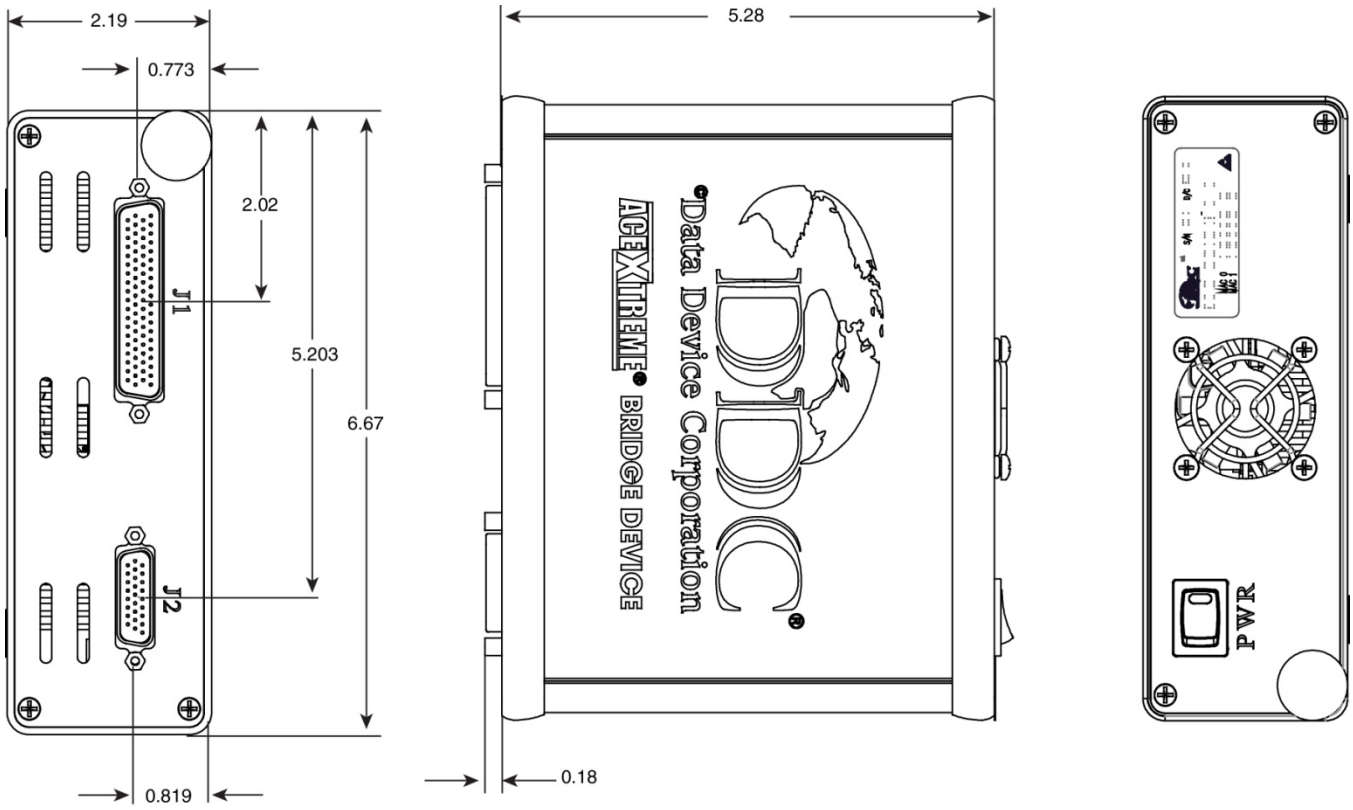



**Figure 3. BU-67119Wx Mechanical Outline**

Figure 5 is the outline drawing for the ***BU-67115Wx*** ruggedized box version of the ABD. As shown in Figure 6 and Figure 7, there is a mounting plate option for this. The mounting plate is available as DDC-78117.




**Figure 4. BU-67115Wx AceXtreme Bridge Device Rugged Box**

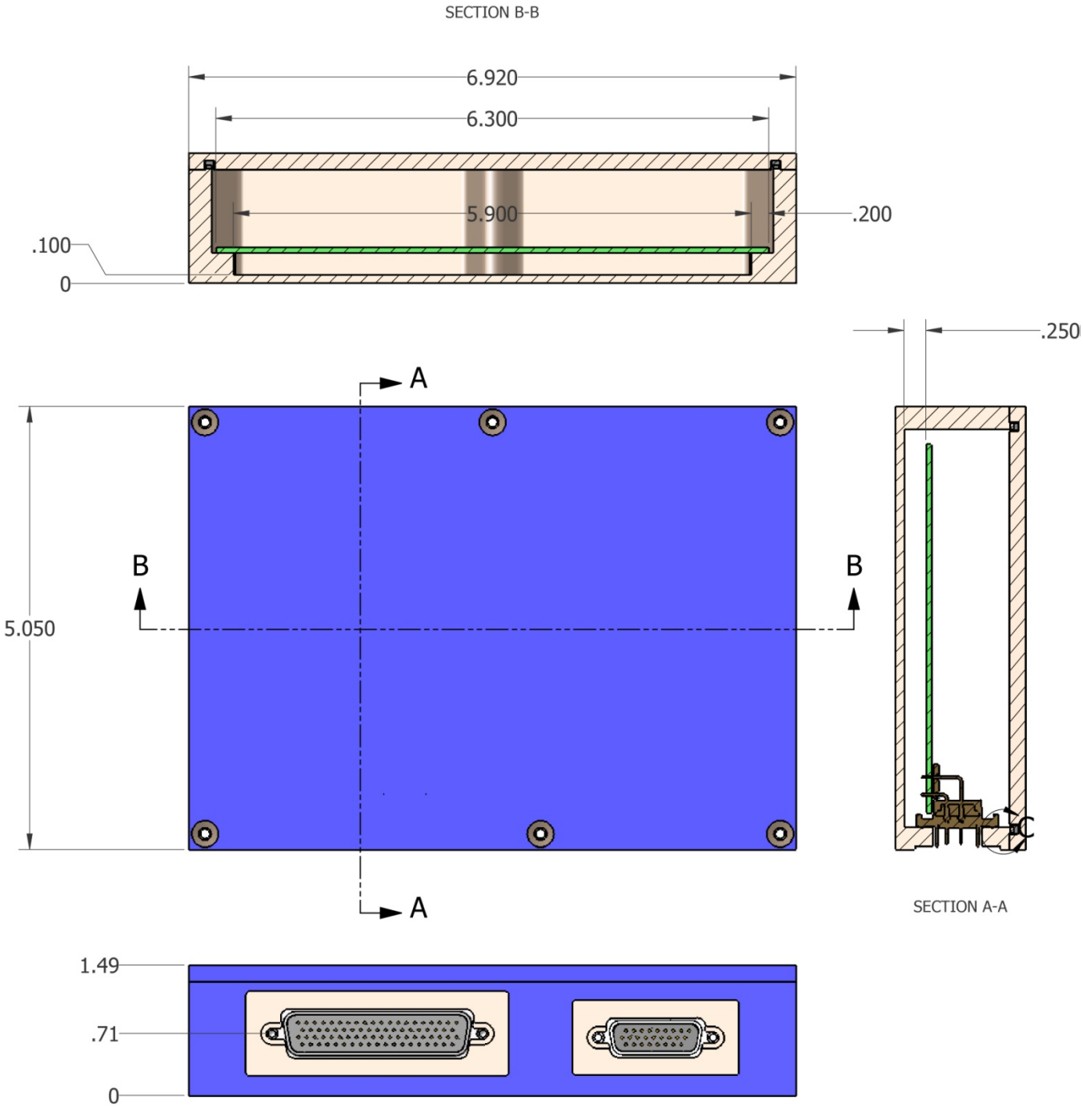



**Figure 5. BU-67115Wx Mechanical Outline**

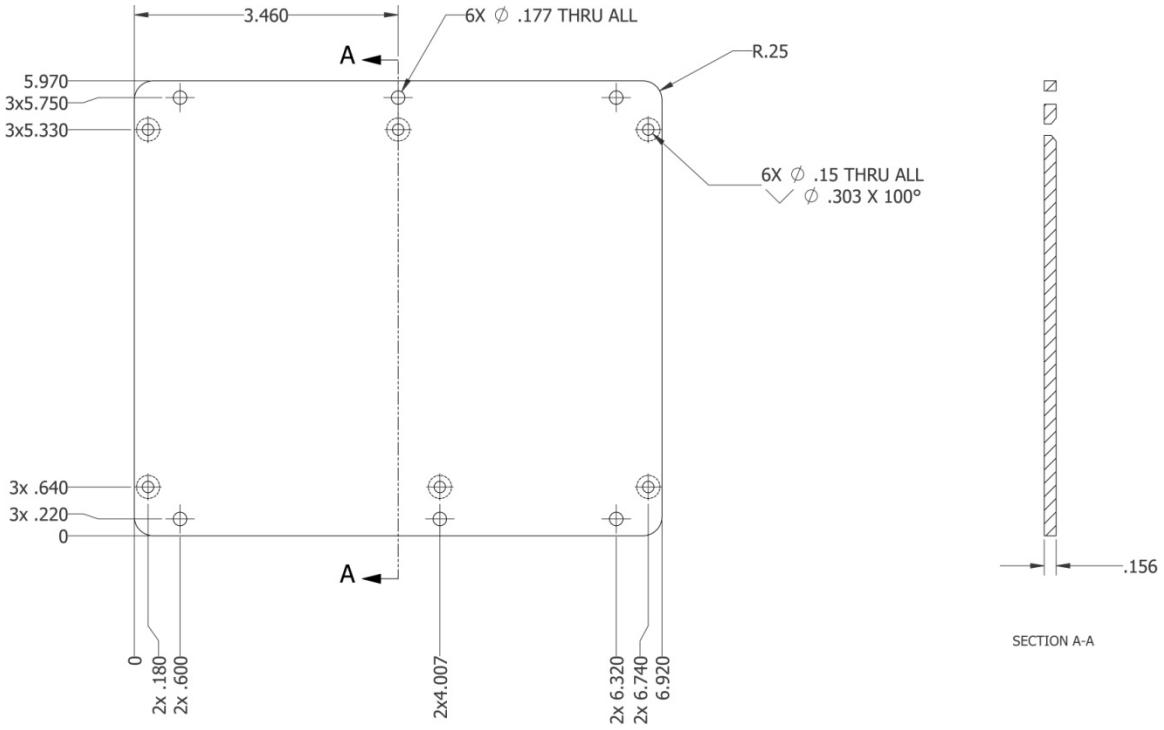



**Figure 6. BU-67115Wx Mounting Plate Mechanical Outline**

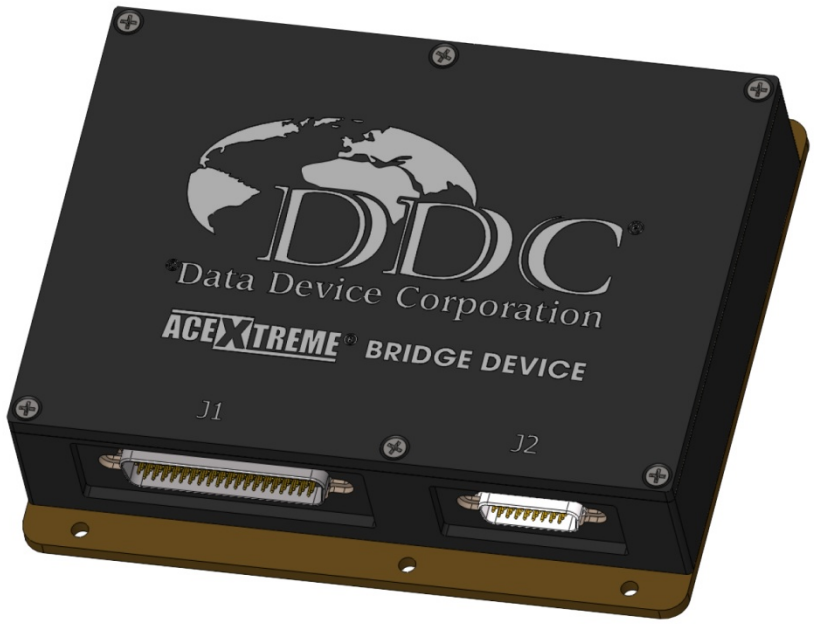



**Figure 7. BU-67115Wx Assembled on Mounting Plate**

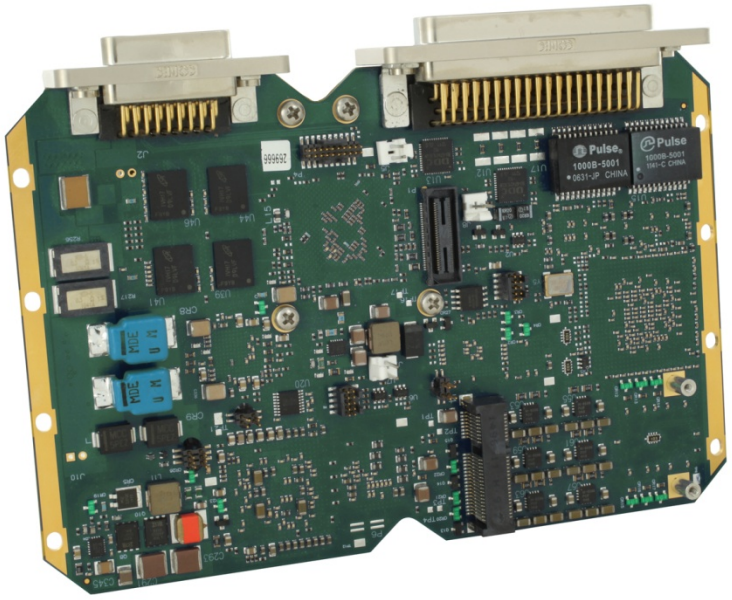


**Figure 8. BU-67116Wx AceXtreme Bridge Device Rugged Card**

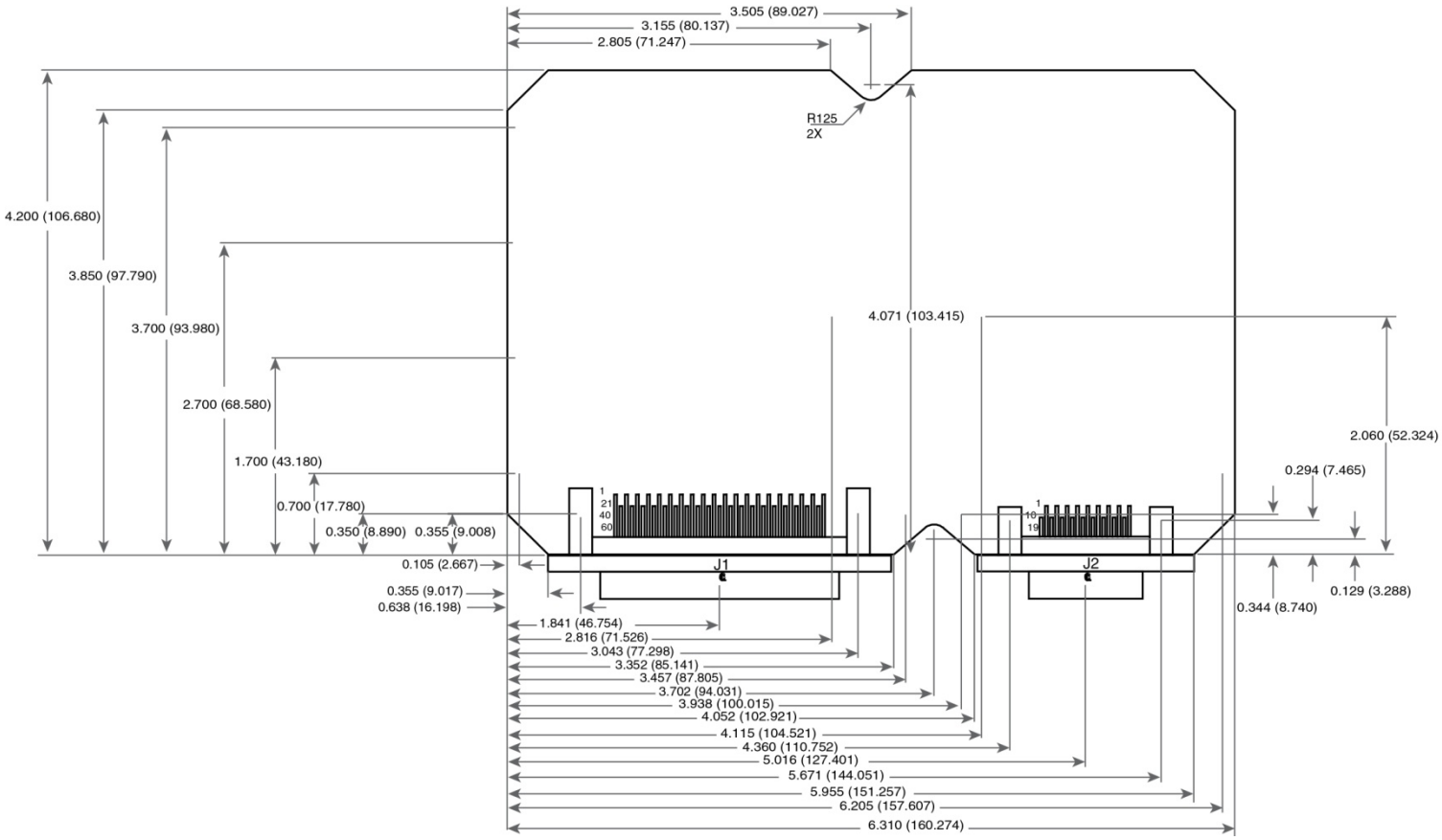



**Figure 9. BU-67116Wx Mechanical Outline**

## 2.7 Power Adaptor

The ***BU-67119WX*** lab version AceXtreme Bridge Device is powered by means of an MW GS120A24-R7B 115/230 VAC-to-28 VDC (5 Amp) power adaptor. This comes with separate line cords for operation in the US, UK, Europe, and Japan. The power adaptor may be ordered from DDC under part number DDC-78164-1.

The ***BU-67115Wx*** and ***BU-67116Wx*** embedded versions of the AceXtreme Bridge Device are normally powered by platform 28V power. However as an option, the power adaptor is also able to be ordered for use with the ***BU-67115Wx*** and ***BU-67116Wx***.

## 2.8 Specifications

**Table 1. BU-67115/6/9 Specification Table**

| PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|
| **ABSOLUTE MAXIMUM RATINGS** | | | | |
| AC Voltage Input | | | 264 | VAC |
| DC Power Input | 28 VDC nominal, per MIL-STD-704F and MIL-STD-1275D | | | |
| Logic Inputs | -0.5 | | 3.95 | V |
| **POWER SUPPLY REQUIREMENTS (NOTE 8)** | | | | |
| Using External AC Power Supply | | | | |
| • Voltage | 85 | | 264 | VAC |
| • Frequency | 47 | | 63 | Hz |
| • With no card in PCIe expansion slot: | | | | |
| - Current with 115 VAC input: | | | | |
| • Both1553 channels idle | | 115 | 136 | mA |
| • Both 1553 channels transmitting 100% duty cycle | | 152 | 178 | mA |
| - Current with 230 VAC input: | | | | |
| • Both1553 channels idle | | 58 | 68 | mA |
| • Both1553 channels 100% duty cycle | | 76 | 88 | mA |
| Using Direct DC Power Input | | | | |
| • Input Voltage<br>- Steady state range | 22 | | 33 | V |
| - Input spec compliance | Per MIL-STD-704F and MIL-STD-1275D | | | |
| • Current with no card PCIe expansion slot, VIN = 28V: | | | | |
| - Both1553 channels idle | | 429 | 500 | mA |
| - Both1553 channels transmitting 100% duty cycle | | 560 | 664 | mA |
| **INTERNAL POWER DISSIPATION (NOTE 8)** | | | | |
| Without card in PCIe expansion slot: | | | | |
| • Both 1553 channels idle | | 12 | 14 | W |
| • Both 1553 channels transmitting 100% duty cycle | | 12.96 | 14.96 | W |
| **ETHERNET PHYSICAL LAYER INTERFACE** | 10/100/1000BASE-T IEEE 802.3 compliant | | | |
| **MIL-STD-1553 RECEIVER** | | | | |
| Input Impedance, | | | | |
| • Transformer Coupled (Notes 1-3) | 1.00 | | | kΩ |
| Threshold Voltage, | | | | |
| • Transformer Coupled | 0.20 | | 0.86 | $V_{peak\text{-}to\text{-}peak}$ |
| Common-Mode Voltage (Note 4) | | | 10 | $V_{peak}$ |

| Table 1. BU-67115/6/9 Specification Table | | | | |
|---|---|---|---|---|
| **PARAMETER** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **MIL-STD-1553 TRANSMITTER** | | | | |
| Differential Output Voltage | 20 | 21.5 | 27 | $V_{P-P}$ |
| Output Offset Voltage, | | | | |
| • Transformer Coupled Across 70 Ohm | -250 | 150 | 250 | $mV_{peak}$ |
| Rise/Fall Time | 100 | 150 | 300 | ns |
| **ARINC 429 RECEIVER** | | | | |
| Differential Input Voltage (Notes 10 & 11) | | | | |
| • ONE | 6.5 | 10.0 | 13.0 | V |
| • ZERO | -13.0 | -10.0 | -6.5 | V |
| • NULL | -2.5 | 0.0 | 2.5 | V |
| **ARINC 429 TRANSMITTER** | | | | |
| Differential Output Voltage (Note 10) | | | | |
| • ONE | 9.0 | 10.0 | 11.0 | V |
| • ZERO | -11.0 | -10.0 | -9.0 | V |
| • NULL | -0.5 | 0.0 | 0.5 | V |
| **DIGITAL I/O** | | | | |
| $V_{IL}$ | -0.3 | | 0.8 | V |
| $V_{IH}$ | 1.7 | | 3.6 | V |
| $V_{OL}$ @ $I_{OL}$ = 4 mA out | | | 0.45 | V |
| $V_{OH}$ @ $I_{OH}$ = -4 mA out | 2.4 | | | V |
| **1553 MESSAGE TIMING** | | | | |
| BC Intermessage Gap (Note 5) | 10 to 10.5 | | 65536 | µs |
| BC/RT/MT Response Timeout (Note 6) | | | | |
| • Default | | 18.5 | | µs |
| • Programmable Range | 4.0 | | 511.5 | µs |
| RT Response Time | | | | |
| • (mid-parity to mid-sync)(Note 7) | 4 | | 7 | µs |
| Transmitter Watchdog Timeout | | 660 | | µs |
| **THERMAL** | | | | |
| BU-67119WX00(L/R)-JL0 (ambient temperature, includes internal fan) | 0 | | 55 | °C |
| BU-67115WX00(L/R)-CC0X (case temperature) | -40 | | 85 | °C |
| BU-67115WX00(L/R)-CC0X (ambient air temperature) | -40 | | 71 | °C |
| BU-67116WX00(L/R)-2C0X (board thermal interface temperature) | -40 | | 85 | °C |

| Table 1. BU-67115/6/9 Specification Table | | | | |
|---|---|---|---|---|
| **PARAMETER** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **MECHANICAL DESIGN (applicable to BU-67115 and BU-67116)** | | | | |
| Shock | | | | |
| • Tested for functional shock response spectrum (SRS) in each of three orthogonal axes | Tested in accordance with MIL-STD-810F, Table 516.5-1 and Figure 516.5-8 "Functional Test for Ground Equipment" | | | |
| Vibration | | | | |
| • Tested for a duration of 60 minutes in each of the three orthogonal axes | Tested in accordance with MIL-STD-810F, Method 514.5, and Category 24 | | | |
| Humidity (assumes conformal coating or the BU-67116) | In accordance with MIL-STD-810F Method 507.4: 5 humidity cycles (240 hours) | | | |
| Ingress Protection (applicable to BU-67115) | IPC-67; Def Stan 00-35 part 3, test CL27; CL25 Vel8.9m/s, 3Hrs;CH 4-04, Test CN4 Intermittent exposure, 3 24Hr cycles of 8 hr wetting and 16 hr draining at 55°C | | | |
| **PHYSICAL CHARACTERISTICS** | | | | |
| Size | | | | |
| • BU-67119Wx | 6.67 x 5.28 x 2.19 | | | in. |
| | 169.4 x 134.1 x 55.6 | | | mm. |
| • BU-67115Wx | 6.92 X 5.05 X 1.5 | | | in. |
| | 175.8 X 128.3 X 38.1 | | | mm. |
| • BU-67116Wx | 6.31x 4.20 | | | in. |
| | 160.3 x 106.7 | | | mm. |
| Weight | | | | |
| • BU-67119Wx | 26.0 (737) | | | oz. (g) |
| • BU-67115Wx | 35.3 (1000) | | | oz. (g) |
| • BU-67116Wx | 6.92 (197) | | | oz. (g) |

| Table 1. BU-67115/6/9 Specification Table | | | | |
|---|---|---|---|---|
| **PARAMETER** | **MIN** | **TYP** | **MAX** | **UNITS** |

**Notes For Table 1:**

(Notes 1 through 3 are applicable to the input Impedance specification)

1. The specifications are applicable for both unpowered and powered conditions.
2. The specifications assume a 2 Volt rms balanced, differential, sinusoidal input. The applicable frequency is 75 kHz to 1 MHz.
3. Minimum impedance is guaranteed over the operating range, but is not tested.
4. Assumes a common mode voltage within the frequency range of dc to 2 MHz, applied to pins of the isolation transformer on the stub side (transformer coupled), and referenced to signal.
5. Defined as the time between the mid-parity bit zero crossing of the last word of one message to the mid-sync zero crossing of the Command Word of the next message. The typical value for minimum BC intermessage gap time is 10 to 10.5 µS. Under software control, this may be lengthened to 65,535 µS, with a resolution of 1 µs.
6. Measured from mid-parity crossing of the last word transmitted by the BC or transmitting RT to the mid-sync crossing of the RT's Status Word. Includes RT-to-RT Timeout, measured from mid-parity of transmit Command Word to mid-sync of Transmitting RT Status Word. Default value is 18.5 µS, and may be software programmed from 4.0 µS to 511.5 µS, with a resolution of 0.5 µS.
7. Measured from mid-parity crossing of the last word received from the BC or transmitting RT to the mid-sync crossing of RT's Status Word.
8. For MIL-STD-1553 channels, the power dissipation specifications assume external dissipation (while transmitting) of 1.5 Watts total for 1553 bus isolation and termination resistors. Power dissipation specs do not include the dissipation of external AC-to-DC converter.
9. ARINC 429 I/O is not lightning protected per DO-160D
10. Absolute Maximum Input Voltage Rating at ARINC 429 receiver input pins is –29V to +29V
11. ARINC 429 Current Drain based on Max Load = 400Ω and 10,000 pF.

# 3 MODES AND OPERATION

The ABD includes basic modes of operation, Protocol Conversion Mode and Remote Access Mode.

## 3.1 Protocol Conversion Mode

Figure 10 shows an example of the AceXtreme Bridge Device operating in its Protocol Conversion Mode. In its Protocol Conversion Mode, the ABD may be configured to provide autonomous communication bridging between any channel and any other channel(s). To minimize setup time and provide more "turnkey" operation, the ABD includes a high-level bridging API. Alternatively, users may develop their own bridging applications invoking DDC's AceXtreme MIL-STD-1553 and/or ARINC 429 APIs, along with the Linux socket interfaces for the two Ethernet channels.

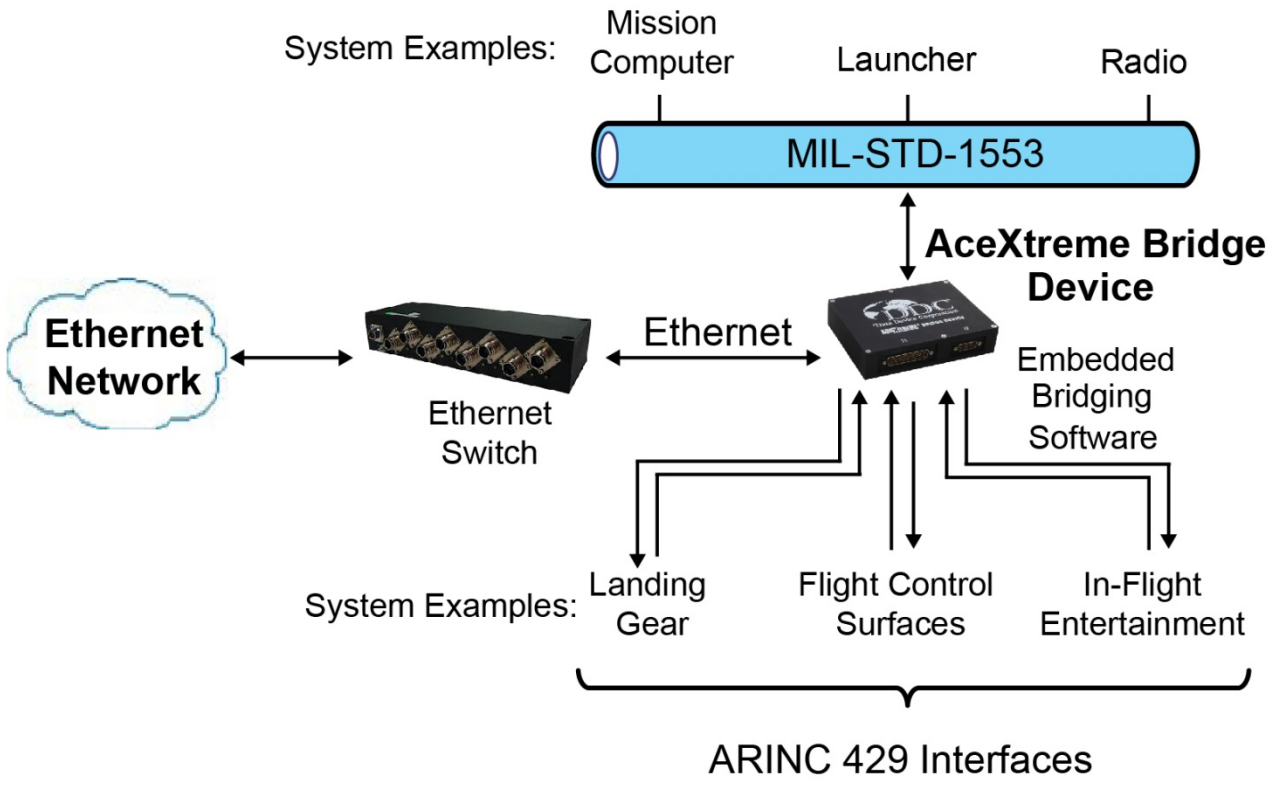



**Figure 10. Example of AceXtreme Bridge Device Used in Protocol Conversion Mode**

## 3.2 Remote Access Mode

Remote Access Mode is a capability of the AceXtreme Bridge Device. Figure 11 shows an example of the AceXtreme Bridge Device operating in Remote Access Mode. In Remote Access Mode, users are able to develop applications running on a remote computer that communicates over Ethernet to the ABD's MIL-STD-1553 and/or ARINC 429 channels. In the remote access configuration, the user is able to write applications running on a remote host that invoke the AceXtreme MIL-STD-1553 and/or ARINC 429 APIs. For use in Remote Access Mode, DDC offers AceXtreme software drivers for Windows 2000, XP, Vista, and 7; Linux kernel version 2.6.x; and Wind River VxWorks versions 6.x.

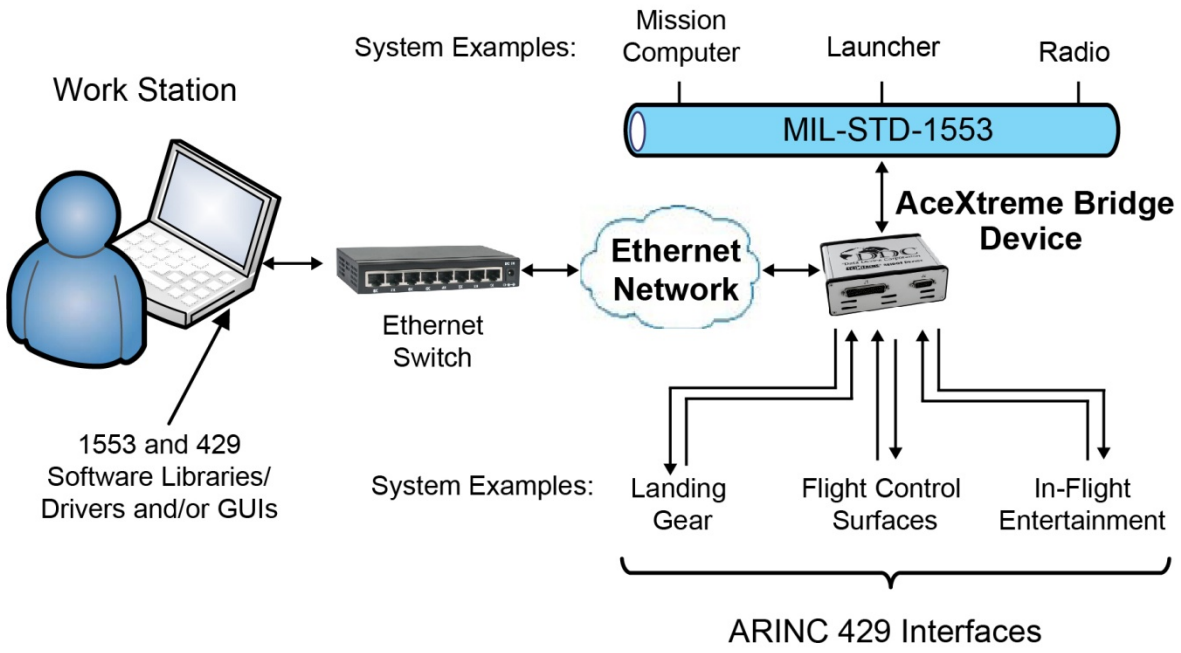



**Figure 11. Example of AceXtreme Bridge Device Used in Remote Access Mode**

### 3.2.1 Optional Software Tools – BusTrACEr, *dataSIMS*, etc.

For the Remote Access Mode, as an alternative to developing application software, the user may operate the ABD using any of DDC's GUI software programs. These include:

- **BusTrACEr.** The ***BU-69066S0-XX0*** BusTrACEr allows a user to generate and monitor MIL-STD-1553 messages. It allows rapid creation and setup of custom applications and includes an option for the automatic generation of ANSI 'C' source code.

- ***dataSIMS.*** The ***BU-694X4DS-64VM*** *dataSIMS* is a software GUI tool for accelerating software development for test and simulation applications. It includes capability to display data in a variety of graphical formats, and may be used for either passive monitoring, or both monitoring and simulation of real time systems with MIL-STD-1553 and/or ARINC 429 interfaces.
- **LabVIEW® Support**. The ***BU-69093S0-XX0*** software operates in conjunction with National Instruments' LabVIEW® system design software to provide a simple interface and easy programming of the ABD's MIL-STD-1553 and/or ARINC 429 interfaces. Users can either create their own custom interfaces "from scratch" or may modify the samples that are provided.
- **Commercial Avionics Utilities Software Package.** The ***DD-42999S0-XX0*** **Data Bus Analyzer and Data Loader GUI software** is for ARINC 429 data bus analysis and simulation. This GUI provides advanced filtering, message scheduling and triggering. In addition, it includes a graphical ARINC 615 data loader, providing a software interface to load data to and from airborne computers.

## 3.3 MIL-STD-1553 Channels

The AceXtreme Bridge Device provides up to two MIL-STD-1553 channels utilizing the DDC ***AceXtreme*** architecture. Each 1553 channel may be independently programmed for BC, RT, Monitor or RT/Monitor modes, and is configured with 2MB of onboard RAM per installed channel.

Each MIL-STD-1553 interface provides a transformer-coupled dual redundant bus interface (consult factory for direct-coupled).

### 3.3.1 Bus Controller Mode

The ***AceXtreme's*** MIL-STD-1553 Bus Controller (BC) is based on the 32-bit architecture of DDC's AceXtreme 1553 Bus Controller.

AceXtreme's BC architecture retains much of the previous generation (Enhanced Mini-ACE, Mini-ACE Mark 3, Micro-ACE (TE), and Total-ACE) 1553 Bus Controller architecture. However, it expands upon it in specific areas to provide improved capabilities.

The AceXtreme® BC architecture is based on a built-in command interpreter with a set of 32 instructions. The command interpreter is a message sequence control engine that provides a high degree of flexibility for implementing 1553 Message lists, including major and minor frame scheduling. It separates 1553 message data from control/status data for the purposes of implementing different data block handling schemes, performing bulk data transfers, and implementing automatic message retries. It also includes the capability for automatic bus switchover for failed

messages and reporting of various error and status conditions to the host processor by means of five user-defined interrupts and a general-purpose queue.

Two Asynchronous queues are also included, to improve the Bus Controller's efficiency and flexibility. The High Priority Queue (HPQ) enables the user to easily insert asynchronous messages into a running Message list, causing it to operate on the new message immediately. The Low Priority Queue (LPQ) enables the user to insert asynchronous messages which will only be processed when there's sufficient "dead-time" available on the bus at the end of a minor frame.

The AceXtreme's BC Engine implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis. Automatic retries and interrupt requests may be enabled or disabled for each individual message. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The BC No-Response timeout value is also programmable to enable operation over long buses or through repeaters.

### 3.3.2 Remote Terminal Operation

The AceXtreme RT architecture builds upon the single-RT architecture of Enhanced Mini-ACE, Mini-ACE

The AceXtreme architecture includes Multi-RT capability. That is, AceXtreme provides the capability to implement up to 31 independent Remote Terminals (up to 32 RTs if Broadcast is disabled).

The AceXtreme RT engine can also be configured to operate in a Single-RT mode of operation. Single RT operation supports hardware control of the RT address and RT automatic boot for each channel, allowing the AceXtreme to respond to commands with Status with its Busy bit set immediately following power turn-on prior to host configuration.

For RT (and/or Monitor) applications, where the possibility of BC operation must be absolutely prohibited, the ABD's two 1553 channels each include a BC_DISABLE input signal. In addition to single-RT and Multi-RT operation, the AceXtreme includes the following capabilities:

- Compliance with MIL-STD-1553A, MIL-STD-1553B, MIL-STD-1760, and STANAG 3838 standards.
    - Consult factory for McAir applications.
- Multiple Data Handling Modes:

  - Single Buffer Mode
  - Double Buffer Mode
  - Circular Buffer Mode
  - Global Circular Buffer
- Command Illegalization by Subaddress/Word Count, and Mode Codes
- Programmable Busy by Subaddress
- Flexible Interrupt Conditions, Including 50% and 100% Rollover Interrupts for Circular Buffers
- Interrupt Status Queue with Programmable Filtering
- Time Tagging Options for Synchronize Mode Codes
- Option for RT Auto-Boot with Busy bit Set

### 3.3.3 Monitor Mode Operation

The AceXtreme Monitor engine autonomously stores individual messages into contiguous memory packets formatted in compliance with IRIG 106 Chapter 10 Data Packets.

In addition to the IRIG 106 Chapter 10 Monitor, DDC's legacy Selective Monitor mode that's implemented in previous generations of DDC MIL-STD-1553 engines is emulated through DDC's software drivers. Using these, all information and functionality supported on the legacy Monitor engines may be extracted from stored messages.

IRIG 106 Chapter 10 provides standardization for such applications as test range telemetry, flight test instrumentation, mission recorders, video/data servers; surveillance and reconnaissance; health and usage monitoring; mission planning, debriefing, and training; and flight operations. IRIG 106 Chapter 10 defines a standardized file format, and within that, specific representations for several types of flight data, including MIL-STD-1553 buses, PCM, analog, computer-generated data, images, discretes, UARTs, IEEE 1394, parallel, IRIG time, video, and voice. Further, IRIG 106 Chapter 10 provides for standardized representation of time. This synchronized time stamping is applicable not only across multiple 1553 channels, but also across channels of other types of monitored data.

For MIL-STD-1553, IRIG 106 Chapter 10 defines packets encapsulating one or more 1553 messages. Within these packets, all messages are tagged with either a 48-bit relative or 64-bit absolute time stamp. For each message, there's also a block status word, which includes indications of bus channel and message validity, and identifies specific errors. The 1553 format also defines indications of RT response time(s), plus storage of all 1553 Command, Status, and Data Words, in the order received. For

supporting IRIG 106 Chapter 10, the AceXtreme Bridge Device includes DMA capability, which enables high-speed transfers of monitored data from the 1553 monitor shared RAM to the ABD's Atom processor host address space.

## 3.4 ARINC 429/575 Channels

The ABD includes an option for six ARINC 429/575 channels, with each channel software configurable as a transmitter or receiver. The powerful and efficient ARINC 429/575 engine supports full line transmission/reception on all channels. All channels comply with the ARINC 429 electrical specification.

Additional features include multiple speed options (high, low, 575), FIFO, scheduled or mailbox data transfer methods, message filtering, data handling, interrupts, internal/external loopback capability, and error control options.

## 3.5 Timers

For its MIL-STD-1553 BC, Multi-RT, and Monitor modes, the ABD stores time tags associated with all processed MIL-STD-1553 messages. The ABD provides two sources for the relative time tags: a local timer with hardware support for the 1553 Synchronize mode codes, along with an IRIG-B digital input. The IRIG-B input supports applications where accurate synchronization with other devices is required.

### 3.5.1 Local Timer

The Local Timer is a free-running 48-bit binary counter that's maintained locally within the ABD. Its value may be designated by host software or alternatively for RT mode, be programmed to automatically update in response to "Synchronize" and "Synchronize with data" messages received from the 1553 bus. In BC mode, "Synchronize with data" messages may be configured to transmit the lower 16 bits of the current value of the local time tag as the data word. Timer resolution and overflow frequency may also be programmed.

### 3.5.2 IRIG-B Timer

IRIG 200-04 time code standardization allows equipment to be synchronized to a known reference time. The ABD can accept a digital B006 time code input, although B004, B005, and B007 will work equally well. B000, B001, B002, and B003 time codes can also be used, but may result in a one day error due to the lack of leap year information. The digital IRIG data is read/updated once per second.

Refer to the "Using IRIG 200-04 Time Codes with DDC Data Bus Devices" (document AN/B-57) and "AceXtreme C SDK Software Manual" (document #MN-69092SX-002) for more information.

# 4 HARDWARE INSTALLAION

The ***BU-67115Wx*** and ***BU-67119WX*** are rugged and lab boxes respectively, while the ***BU-67116Wx*** is an embedded board assembly.

- When installing the ***BU-67116Wx*** board, the following should be observed:
- **NEVER** insert or remove the card with the power turned on.
- **ALWAYS** take proper precautions to guard against static damage.
- Use a wrist strap if available, or ensure proper static grounding by touching the power supply cover **WITH POWER OFF**.

## 4.1 Connector Pinouts

### 4.1.1 I/O Connectors

As shown in Figure 12, the ABD includes two front-panel I/O connectors, J1 and J2. J1 includes all the analog and digital I/O signals for the ABD's two MIL-STD-1553 channels, six ARINC 429 channels, two Ethernet channels, and 12 RT Address/Discrete I/O signals.

J1 also includes a pair of ABD configuration signals for selecting between a configuration mode and normal run mode, and for directing the ABD to re-load its internal operating system and library/driver software from its internal solid state disk.

J2 includes the pins for bringing 28V DC power into the ABD. In addition, J2 also provides connections to a Mini-PCI Express card that's plugged into the ABD's internal expansion socket.




**Figure 12. *BU-67119WX* J1 and J2 I/O Connectors**

#### 4.1.1.1 I/O Connectors

The connector and mating connector part numbers for the ABD are as follows:

- Main I/O connector J1: Conec 15-002231
- Mating connector for J1: Amphenol 17EHD-078S-AA0000 with Amphenol 17E-1728-1 backshell.
- Power and Mini-PCI Express expansion card connector J2: Conec 15-002201
- Mating connector for J2: Amphenol 17EHD-026S-AA0000 with Amphenol 17E-1725-1 backshell.

The ***BU-67119WX*** includes an ON/OFF switch on the back of the box.

### 4.1.2 Main I/O Connector Pinout (J1)

**Table 2. J1 Main I/O Connector Pinout**

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | E1 TXRX 1- | 21 | E1 TXRX 2- | 40 | E1 TXRX 3- | 60 | E1 TXRX 4- |
| 2 | E1 TXRX 1+ | 22 | E1 TXRX 2+ | 41 | E1 TXRX 3+ | 61 | E1 TXRX 4+ |
| 3 | ETHNT1_CT | 23 | ETHNT2_CT | 42 | ETHNT1_CT | 62 | ETHNT2_CT |
| 4 | E2 TXRX 2- | 24 | E2 TXRX 1- | 43 | E2 TXRX 3- | 63 | E2 TXRX 4- |
| 5 | E2 TXRX 2+ | 25 | E2 TXRX 1+ | 44 | E2 TXRX 3+ | 64 | E2 TXRX 4+ |
| 6 | GROUND | 26 | GROUND | 45 | GROUND | 65 | GROUND |
| 7 | RESTORE_EN_L | 27 | RT Chan#1 PAR/GP Discrete#0 and BC_TRG/ SSFLAG* Chan#1 | 46 | IRIG_DIG_1-2 | 66 | RT Chan#2 PAR/GP Discrete#6 and BC_TRG/ SSFLAG* Chan#2 |
| 8 | CONFIG_MODE_EN_L | 28 | RT Chan#1 0/GP Discrete #1 | 47 | BC_DISABLE_2 | 67 | RT Chan#2 0/GP Discrete #7 |
| 9 | GROUND | 29 | RT Chan#1 1/GP Discrete #2 | 48 | RTBOOT_L_2 | 68 | RT Chan#2 1/GP Discrete #8 |
| 10 | MIL_STD_1553_B1- | 30 | RT Chan#1 2/GP Discrete #3 | 49 | TX_INH_AB2 | 69 | RT Chan#2 2/GP Discrete #9 |
| 11 | MIL_STD_1553_B1+ | 31 | RT Chan#1 3/GP Discrete #4 | 50 | BC_DISABLE_1 | 70 | RT Chan#2 3/GP Discrete #10 |

| Table 2. J1 Main I/O Connector Pinout | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Pin** | **Signal** | **Pin** | **Signal** | **Pin** | **Signal** | **Pin** | **Signal** |
| 12 | GROUND | 32 | RT Chan#1 4/GP Discrete #5 | 51 | RTBOOT_L_1 | 71 | RT Chan#2 4/GP Discrete #11 |
| 13 | MIL_STD_1553_A1- | 33 | GROUND | 52 | TX_INH_AB1 | 72 | Shield |
| 14 | MIL_STD_1553_A1+ | 34 | ARINC_TXDIS_L_5 | 53 | GROUND | 73 | ARINC_TXDIS_L_2 |
| 15 | GROUND | 35 | ARINC 429 CH5+ | 54 | ARINC_TXDIS_L_3 | 74 | ARINC 429 CH2+ |
| 16 | MIL_STD_1553_B2- | 36 | ARINC 429 CH5- | 55 | ARINC 429 CH3+ | 75 | ARINC 429 CH2- |
| 17 | MIL_STD_1553_B2+ | 37 | ARINC_TXDIS_L_4 | 56 | ARINC 429 CH3- | 76 | ARINC_TXDIS_L_1 |
| 18 | GROUND | 38 | ARINC 429 CH4+ | 57 | ARINC_TXDIS_L_6 | 77 | ARINC 429 CH1+ |
| 19 | MIL_STD_1553_A2- | 39 | ARINC 429 CH4- | 58 | ARINC 429 CH6+ | 78 | ARINC 429 CH1- |
| 20 | MIL_STD_1553_A2+ | | | 59 | ARINC 429 CH6- | 79 | Shield |
| | | | | | | 80 | Shield |

### 4.1.3 Power and Mini-PCIe Expansion Slot I/O Connector Pinout (J2)

**Table 3. J2 Power Input and Expansion Bus Connector Pinout**

| J2 Pin | Expansion Bus Signal Name | J2 Pin | Expansion Bus Signal Name |
|---|---|---|---|
| 1 | EXP_BUS[7] | 15 | EXP_BUS[14] |
| 2 | EXP_BUS[5] | 16 | EXP_BUS[12] |
| 3 | EXP_BUS[4] | 17 | +28V RETURN |
| 4 | EXP_BUS[3] | 18 | +28 VDC |
| 5 | EXP_BUS[2] | 19 | EXP_BUS[8] |
| 6 | EXP_BUS[1] | 20 | EXP_BUS[9] |
| 7 | EXP_BUS[0] | 21 | EXP_BUS[10] |
| 8 | +28V RETURN | 22 | EXP_BUS[11] |
| 9 | +28V RETURN | 23 | EXP_BUS[15] |
| 10 | EXP_BUS[6] | 24 | EXP_BUS[13] |
| 11 | EXP_BUS[19] | 25 | +28 VDC |
| 12 | EXP_BUS[18] | 26 | +28 VDC |
| 13 | EXP_BUS[17] | 27 | Shield |
| 14 | EXP_BUS[16] | 28 | Shield |

## 4.2 Signal Descriptions by Functional Groups

### 4.2.1 J1 Main I/O Connector Signals

The descriptions of the signals for the ABD's main I/O connector J1 are indicated in Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, and Table 10. These signals include Ethernet; MIL-STD-1553 data bus, RT Address/Discrete I/O signals, and 1553 control inputs; ARINC 429 data bus and control inputs; the ABD's CONFIGURATION and RESTORE input signals, grounds and shields.

**Table 4. J1 Main I/O Connector: Ethernet**

| Signal Name | ABD J1 Pin | Connector Pin on DDC-78053-1 Breakout Cable | Description |
|---|---|---|---|
| E1 TXRX 1- | 1 | EJ1-2 | Channel 1 10/100/1000 BASE-T Ethernet interface. The ETHNT1_CT pin connects to an on-board Bob Smith termination network from the transformer center taps and may be connected to system chassis ground.<br><br>In Protocol Conversion Mode, the ABD's Channel 1 Ethernet interface (but not the Channel 2 Ethernet interface) may be used in CONFIGURATION_MODE for establishing a TELNET programming interface.<br><br>In Protocol Conversion Mode, it's possible to bridge between Ethernet Channel 1 and the ABD's 1553 and/or ARINC 429 channels. In addition in Protocol Conversion Mode, it's possible to communicate with the ABD over the Channel 1 Ethernet using Telnet.<br><br>In Remote Access Mode, the ABD's Channel 1 Ethernet interface (but not the Channel 2 Ethernet interface) is used for interfacing with a remote host computer.<br><br>The ETHNT1_CT pin connects to a Bob Smith termination network from the transformer center taps and may be connected to system chassis ground. |
| E1 TXRX 1+ | 2 | EJ1-1 | |
| E1 TXRX 2- | 21 | EJ1-6 | |
| E1 TXRX 2+ | 22 | EJ1-3 | |
| E1 TXRX 3- | 40 | EJ1-5 | |
| E1 TXRX 3+ | 41 | EJ1-4 | |
| E1 TXRX 4- | 60 | EJ1-8 | |
| E1 TXRX 4+ | 61 | EJ1-7 | |
| ETHNT1_CT | 3, 42 | N/C | |
| E2 TXRX 1- | 24 | EJ2-2 | Channel 2 10/100/1000 BASE-T Ethernet interface.<br><br>In either Protocol Conversion Mode, Ethernet Channel 2 may be bridged to the ABD's 1553 or ARINC 429 interfaces, or to Ethernet Channel 2.<br><br>In Remote Access Mode, it's possible to communicate between a remote host computer (over Ethernet Channel 1) to Ethernet Channel 2. |
| E2 TXRX 1+ | 25 | EJ2-1 | |
| E2 TXRX 2- | 4 | EJ2-6 | |
| E2 TXRX 2+ | 5 | EJ2-3 | |
| E2 TXRX 3- | 43 | EJ2-5 | |
| E2 TXRX 3+ | 44 | EJ2-4 | |
| E2 TXRX 4- | 63 | EJ2-8 | |

| Table 4. J1 Main I/O Connector: Ethernet | | | |
|---|---|---|---|
| **Signal Name** | **ABD J1 Pin** | **Connector Pin on DDC-78053-1 Breakout Cable** | **Description** |
| E2 TXRX 4+ | 64 | EJ2-7 | The ETHNT2_CT pin connects to a Bob Smith termination network from the transformer center taps and may be connected to system chassis ground. |
| ETHNT2_CT | 23, 62 | N/C | |

| Table 5. J1 Main I/O Connector: MIL-STD-1553 Data Bus | | | |
|---|---|---|---|
| **Signal Name** | **ABD J1 Pin** | **Connector Pin on DDC-78053-1 Breakout Cable** | **Description** |
| MIL-STD-1553_B1- | 10 | CJ2-OUTER | Channel 1 MIL-STD-1553 Transmit/Receive Input/Outputs. Connect directly to MIL-STD-1553 long (transformer-coupled) stub. |
| MIL-STD-1553_B1+ | 11 | CJ2-CENTER | |
| MIL-STD-1553_A1- | 13 | CJ1-OUTER | |
| MIL-STD-1553_A1+ | 14 | CJ1-CENTER | |
| MIL-STD-1553_B2- | 16 | CJ4-OUTER | Channel 2 MIL-STD-1553 Transmit/Receive Input/Outputs. Connect directly to MIL-STD-1553 long (transformer-coupled) stub. |
| MIL-STD-1553_B2+ | 17 | CJ4-CENTER | |
| MIL-STD-1553_A2- | 19 | CJ3-OUTER | |
| MIL-STD-1553_A2+ | 20 | CJ3-CENTER | |

| Table 6. J1 Main I/O Connector: MIL-STD-1553 RT Address, BC_TRIG/RT SSFLG*, and General Purpose Discrete I/Os | | | |
|---|---|---|---|
| **Signal Name** | **ABD J1 Pin** | **Connector Pin on DDC-78053-1 Breakout Cable** | **Description** |
| RT Chan#1 PAR/ BC_TRG/ SSFLAG* Chan#1/GP Discrete#0 | 27 | J1-5 | Referring to the table and notes below, these digital signals may be programmed to operate in either of three modes:<br>• As MIL-STD-1553 RT address inputs;<br>• As general purpose discrete I/O signals; or<br>• As BC_TRG/ SSFLAG* signals (J1 pins 27 and 6 only). |
| RT Chan#1 0/GP Discrete #1 | 28 | J1-6 | |
| RT Chan#1 1/GP Discrete #2 | 29 | J1-7 | |
| RT Chan#1 2/GP Discrete #3 | 30 | J1-8 | |
| RT Chan#1 3/GP Discrete #4 | 31 | J1-9 | |
| RT Chan#1 4/GP Discrete #5 | 32 | J1-10 | |
| RT Chan#2 PAR/ BC_TRG/ SSFLAG* Chan#2/GP Discrete#6 | 66 | J1-34 | |
| RT Chan#2 0/GP Discrete #7 | 67 | J1-35 | |
| RT Chan#2 1/GP Discrete #8 | 68 | J1-36 | |
| RT Chan#2 2/GP Discrete #9 | 69 | J1-37 | |
| RT Chan#2 3/GP Discrete #10 | 70 | J1-38 | |

| | | |
|---|---|---|
| RT Chan#2 4/GP Discrete #11 | 71 | J-39 |

| J1 Pin | Option #1 Function | Option #2 Function | Option #3 Function |
|---|---|---|---|
| 27 | RT Chan#1 PAR | GP Discrete#0 | BC_TRG/SSFLAG* Chan#1 |
| 28 | RT Chan#1 0 | GP Discrete #1 | N/A |
| 29 | RT Chan#1 1 | GP Discrete #2 | N/A |
| 30 | RT Chan#1 2 | GP Discrete #3 | N/A |
| 31 | RT Chan#1 3 | GP Discrete #4 | N/A |
| 32 | RT Chan#1 4 | GP Discrete #5 | N/A |
| 66 | RT Chan#2 PAR | GP Discrete#6 | BC_TRG/ SSFLAG* Chan#2 |
| 67 | RT Chan#2 0 | GP Discrete #7 | N/A |
| 68 | RT Chan#2 1 | GP Discrete #8 | N/A |
| 69 | RT Chan#2 2 | GP Discrete #9 | N/A |
| 70 | RT Chan#2 3 | GP Discrete #10 | N/A |
| 71 | RT Chan#2 4 | GP Discrete #11 | N/A |

**Notes:**

1. Option #1, RT Address inputs, is the default configuration. The two RT Addresses (including parity bits) are latched immediately following ABD power turn-on. The user software (running on the internal processor in Protocol Conversion Mode; or on a remote processor in Remote Access Mode) will then have two options:
   (1) As the default, leave these signals in a “tracking” mode, such that if the external values change, then the internal effective RT Address values change correspondingly.
   (2) By means of an API function call, the internal RT Address values are latched at their “power-up” values. In this case, the two RT addresses may later be changed via software, and the 12 signals assume different functions as indicated for “Option #2” or “Option #3” below.

2. For “Option #2”, there’s an API call to configure these 12 signals to operate as general purpose discrete I/O signals.

   For the 12 (or possibly 10) Discrete I/O signals, there’s an API function call to specify the data direction for each signal. The default values are to initialize as inputs.

   For discrete I/O signals programmed as either inputs or outputs, there’s an API function to read the signals’ logic values. For discrete I/O signals programmed as outputs, there’s a separate API function to program the signals’ logic values.

3. Option #3, which is only applicable to pins 27 and 66, is to configure these two signals to operate as BC_TRG (trigger inputs) in BC mode and SSFLAG* inputs in RT mode.

   If programmed to operate as BC_TRG/SSFLAG* inputs, pins 27 and/or 66 operate as follows:
   - In RT mode, if this input is asserted low, the Subsystem Flag bit will be set in the message’s RT Status Word.
   - In BC mode, during the execution of a Wait for External Trigger (WTG) instruction, the BC will wait for a low-to-high transition on BC_TRIG before proceeding to the next instruction.

| Table 6. J1 Main I/O Connector: MIL-STD-1553 RT Address, BC_TRIG/RT SSFLG*, and General Purpose Discrete I/Os | | | |
|---|---|---|---|
| **Signal Name** | **ABD J1 Pin** | **Connector Pin on DDC-78053-1 Breakout Cable** | **Description** |
| | | | |

| Table 7. J1 Main I/O Connector: MIL-STD-1553 Control Signals | | | |
|---|---|---|---|
| **Signal Name** | **ABD J1 Pin** | **Connector Pin on DDC-78053-1 Breakout Cable** | **Description** |
| BC_DISABLE_1 | 50 | J1-23 | When connected to '1', this configures the respective MIL-STD-1553 channel (1 or 2) such that it cannot operate in BC mode (i.e. BC operation is disabled).<br><br>When connected to '0', this configures the respective MIL-STD-1553 channel (1 or 2) such that it can operate in BC mode.<br><br>The BC_DISABLE signals include internal pull-up resistors. |
| BC_DISABLE_2 | 47 | J1-20 | |
| RTBOOT_L_1 | 51 | J1-24 | If RTBOOT_L_x is connected to logic "0", the respective MIL-STD-1553 channel (1 or 2) will initialize to RT mode with the Busy status word bit set following power turn-on.<br><br>If nRTBOOT is hardwired to logic "1", the respective MIL-STD-1553 channel (1 or 2) will initialize in Idle mode. From Idle mode, the channel may then be programmed to operate as a BC, RT, or Monitor.<br><br>The RTBOOT_L_x input signals include internal pull-up resistors. |
| RTBOOT_L_2 | 48 | J1-21 | |
| TX_INH_AB1 | 52 | J1-25 | For MIL-STD-1553 Channel 1 and Channel 2, the respective transmitter inhibit inputs may be used to inhibit the Channel A and Channel B 1553 transmitters. For normal operation, these inputs should be connected to logic '0'.<br><br>To force a shutdown of Channel 1's and/or Channel 2's transmitters, a value of logic '1' should be applied to the respective TX_INH input.<br><br>The TX_INH input signals include internal pull-up resistors. |
| TX_INH_AB2 | 49 | J1-22 | |
| IRIG_DIG_1-2 | 46 | J1-19 | IRIG_DIG_1-2 may be used to synchronize the time tags used by the MIL-STD-1553 Channel 1 and Channel 2 interfaces with external devices. The IRIG_DIG_1-2 digital input signal will receive and synchronize to a new time-code once per second. |

| Table 8. J1 Main I/O Connector: ARINC 429 | | | |
|---|---|---|---|
| **Signal Name** | **ABD J1 Pin** | **Connector Pin on DDC-78053-1 Breakout Cable** | **Description** |
| ARINC_TXDIS_L_1 | 76 | J1-43 | ARINC 429 Channel 1 differential pair, software programmable for either transmit or receive operation. If ARINC_TXDIS_L_1 is asserted low, transmission is disabled. ARINC_TXDIS_L_1 includes an internal pull-up resistor. |
| ARINC 429 CH1+ | 77 | J1-44 | |
| ARINC 429 CH1_ | 78 | J1-45 | |
| ARINC_TXDIS_L_2 | 73 | J1-40 | ARINC 429 Channel 2 differential pair, software programmable for either transmit or receive operation. If ARINC_TXDIS_L_2 is asserted low, transmission is disabled. ARINC_TXDIS_L_2 includes an internal pull-up resistor. |
| ARINC 429 CH2+ | 74 | J1-41 | |
| ARINC 429 CH2- | 75 | J1-42 | |
| ARINC_TXDIS_L_3 | 54 | J1-27 | ARINC 429 Channel 3 differential pair, software programmable for either transmit or receive operation. If ARINC_TXDIS_L_3 is asserted low, transmission is disabled. ARINC_TXDIS_L_3 includes an internal pull-up resistor. |
| ARINC 429 CH3+ | 55 | J1-28 | |
| ARINC 429 CH3- | 56 | J1-29 | |
| ARINC_TXDIS_L_4 | 37 | J1-15 | ARINC 429 Channel 4 differential pair, software programmable for either transmit or receive operation. If ARINC_TXDIS_L_4 is asserted low, transmission is disabled. ARINC_TXDIS_L_4 includes an internal pull-up resistor. |
| ARINC 429 CH4+ | 38 | J1-16 | |
| ARINC 429 CH4- | 39 | J1-17 | |
| ARINC_TXDIS_L_5 | 34 | J1-12 | ARINC 429 Channel 5 differential pair, software programmable for either transmit or receive operation. If ARINC_TXDIS_L_5 is asserted low, transmission is disabled. ARINC_TXDIS_L_5 includes an internal pull-up resistor. |
| ARINC 429 CH5+ | 35 | J1-13 | |
| ARINC 429 CH5- | 36 | J1-14 | |
| ARINC_TXDIS_L_6 | 57 | J1-30 | ARINC 429 Channel 6 differential pair, software programmable for either transmit or receive operation. If ARINC_TXDIS_L_6 is asserted low, transmission is disabled. ARINC_TXDIS_L_6 includes an internal pull-up resistor. |
| ARINC 429 CH6+ | 58 | J1-31 | |
| ARINC 429 CH6- | 59 | J1-32 | |

| Table 9. Main I/O Connector: Miscellaneous | | | |
|---|---|---|---|
| **Signal Name** | **J1 Pin** | **Connector Pin on DDC-78053-1 Breakout Cable** | **Description** |
| RESTORE_EN_L | 7 | J1-47 | RESTORE_EN_L should only be asserted low to cause the ABD to initialize in its backup mode. This operation is only intended to be used for situations where the embedded software has been irrevocably corrupted. The effects of asserting this signal low include:<br>• Loading a back-up copy of the Linux operating system.<br>• Automatically restores the IP Address to a fixed value.<br>• Restores the default configuration parameters to factory default values.<br>RESTORE_EN_L is sampled continuously, allowing the ABD to be initialized in its backup mode at any time.<br><br>RESTORE_EN_L includes an on-board 10 KΩ pull-up resistor. |
| CONFIG_MODE_EN_L | 8 | J2 | Asserting this signal low selects CONFIGURATION_MODE, while leaving this signal open or asserting it high selects RUNNING_MODE.<br>In CONFIGURATION_MODE, the following may be set or changed over the ABD's Ethernet channel 1 interface:<br>• IP Address (fixed or DHCP)<br>• Update the operating system.<br>• Update the FPGA Build (into main FPGA location)<br>• Update the DDC Libraries.<br>• Load Custom applications.<br>CONFIG_MODE_EN_L is sampled continuously, allowing the ABD to be put into or taken out of CONFIGURATION_MODE at any time.<br><br>CONFIG_MODE_EN_L includes an on-board 10 KΩ pull-up resistor. |

| Table 10. Main I/O Connector: Grounds and Shields | | | |
|---|---|---|---|
| **Signal Name** | **ABD J1 Pins** | **Connector Pins on DDC-78053-1 Breakout Cable** | **Description** |
| Ground | 6, 9, 12, 15, 18, 26, 33, 45, 53, 65 | J1-1, J1-2, J1-3, J1-4, J1-11, J1-18, J1-26, J1-33, J1-46, J1-49 | Signal ground. |
| Shield | 72, 79, 80 | N/C | Shield connections, connect to ABD chassis ground. |

## 4.3 J2 Power and Expansion Bus Signals

The descriptions for the power and expansion bus signals from ABD connector J2 are included in Table 11,and Table 12.

**Table 11. J2 Expansion Bus Signals: Power, Grounds, and Shield Connections**

| Expansion Bus Signal Name | MIL-STD-1553 Mini-PCIe Card Signal | ABD J2 Pins | Connector Pin(s) on DDC-78055-1 Breakout Cable | Description |
|---|---|---|---|---|
| N/A | +28V | 18, 25, 26 | J1-1, J1-4 | 28 VDC per MIL-STD-704F and MIL-STD-1275D |
| N/A | +28V RETURN | 8, 9, 17 | J1-2, J1-3 | 28 VDC return |
| N/A | ABD Chassis Ground Shield | 27, 28 | N/C | Shield connections, connect to ABD chassis ground. |

**Table 12. J2 Expansion Bus Signals**

| Expansion Bus Signal Name | ABD J2 Pin | Connector Pin(s) on DDC-78055-1 Breakout Cable |
|---|---|---|
| EXP_BUS[0] | 7 | J3-11 |
| EXP_BUS[1] | 6 | J3-10 |
| EXP_BUS[2] | 5 | N/C |
| EXP_BUS[3] | 4 | J3-20 |
| EXP_BUS[4] | 3 | J3-19 |
| EXP_BUS[5] | 2 | J2-1 |
| EXP_BUS[6] | 10 | J3-4 |
| EXP_BUS[7] | 1 | J3-3 |
| EXP_BUS[8] | 19 | J2-2 |
| EXP_BUS[9] | 20 | J3-2 |
| EXP_BUS[10] | 21 | J3-1 |
| EXP_BUS[11] | 22 | J2-3 |
| EXP_BUS[12] | 16 | J2-4 |
| EXP_BUS[13] | 24 | J2-5 |
| EXP_BUS[14] | 15 | J2-6 |
| EXP_BUS[15] | 23 | J2-7 |
| EXP_BUS[16] | 14 | J2-8 |
| EXP_BUS[17] | 13 | J2-9 |
| EXP_BUS[18] | 12 | J2-10 |
| EXP_BUS[19] | 11 | J2-11 |

## 4.4 Cable Assemblies

The ***BU-67119WX*** lab version of the ABD comes with the three cable assemblies shown in Figure 13, Figure 14, Figure 16, and Figure 18. The ***BU-67119WX*** lab ABD is also supplied with 3 mating connectors and backshells for the breakout cables, along with a 115/230 VAC-to-28 VDC power adaptor.




**Figure 13. BU-67119Wx Lab ABD and Cable Assemblies**

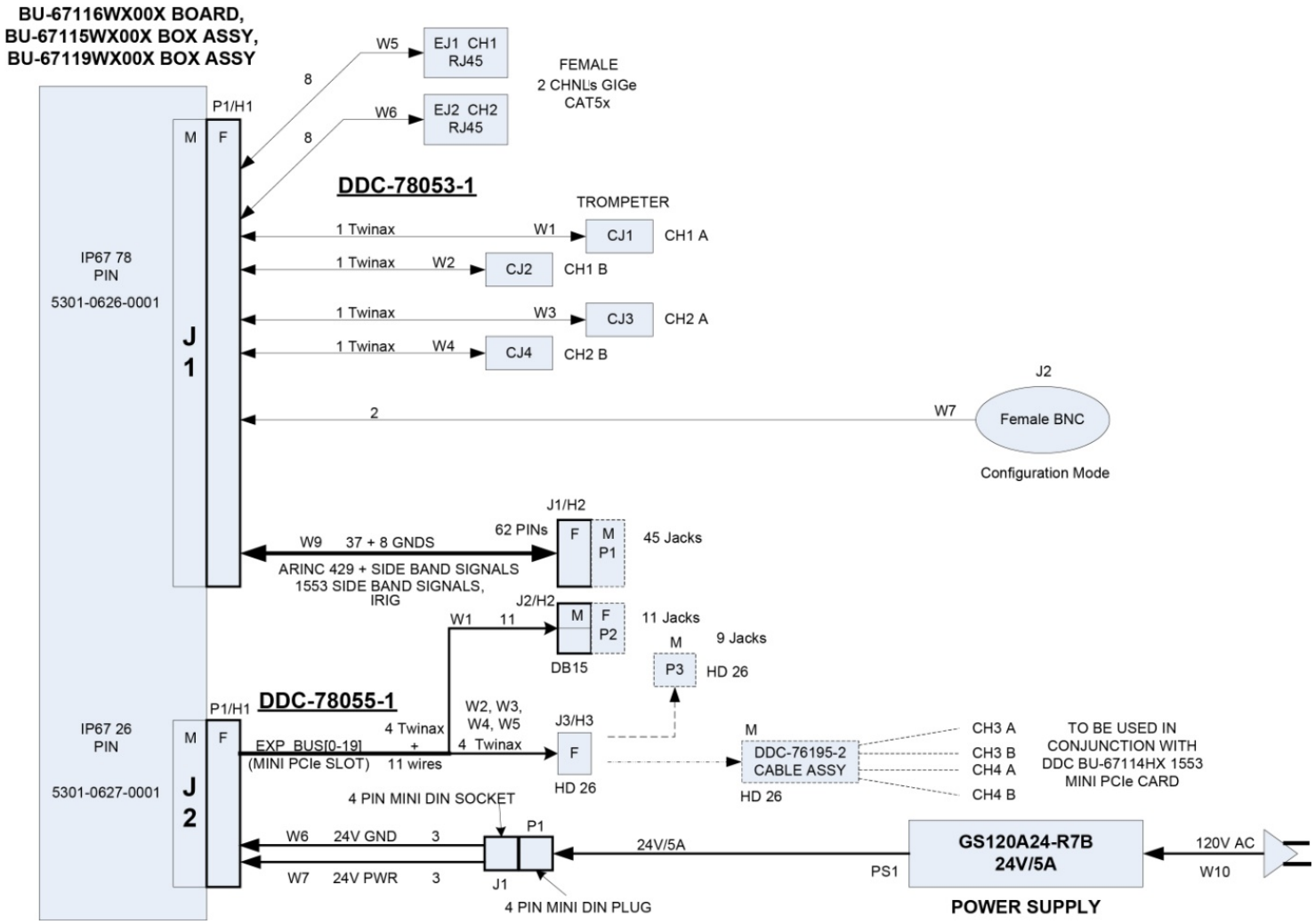



**Figure 14. ABD Top-Level Cable Assemblies Interconnect Diagram**

The cable assemblies, mating connectors, and power adaptor that are provided with the different versions of ABD are shown in Table 13.

**Table 13. ABD Cable Assemblies, Mating Connectors, and Power Adapter**

| Cable Assemblies, Mating Connectors, etc. | BU-67115 (rugged box) or BU-67116 (rugged board) | BU-67119 (lab box) |
|---|---|---|
| **DDC-78053-1** main I/O breakout cable assembly, mates to the ABD J1. | Option | Included |
| Mating connector to ABD J1, 78-pin 'D' connector H1 (Amphenol 17E-1728-1, may also be ordered as DDC P/Ns 5301-0641-0001, 5301-0641-0002, and 5301-0639-0001) – alternative to using DDC-78053-1 breakout cable. | Included | Option |
| **DDC-75594-1** accessory kit -- mating connector, etc. to DDC-78053-1 J1 | Option (comes with DDC-78053-1) | Included |
| Shorting cap (Pomona 5085) for DDC-78053-1 J2, for ABD CONFIG_MODE_EN_L signal. May also be ordered as DDC P/N 5301-0663-0001. | Option (comes with DDC-78053-1) | Included |
| **DDC-78055-1** power and expansion card breakout cable, mates to ABD power/expansion card connector J2. | Option | Included |
| Mating connector to ABD J2 -- 26-pin 'D-SUB' connector P1 (Amphenol 17EHD-026S-AA00), with backshell (Amphenol 17E-1725-1) – alternative to using DDC-78055-1 breakout cable. | Included | Option |
| Mating connector for DDC-78055-1 J2, 15-position female connector P2 (TE Connectivity 5-747909-7, may also be ordered as DDC P/N 5301-0637-0001), with cable clamp kit (TE Connectivity 207470-1) | Option (comes with DDC-78055-1) | Included |
| **DDC-78164-1**/Mean Well GS120A24-R7B 115/230 VAC-to-28V power adaptor, with multiple with multiple international power cables/plugs. | Option | Included |
| Mating connector to DDC-78055-1 J1, P1, 4-pin Mini DIN DC power connector (Kycon KPPX-4P) – alternative to using DDC-78164-1/Mean Well power adaptor. This connector may be purchased as DDC P/N 5301-0645-0001. | Option | Option |

The breakout cable assemblies supplied with the ***BU-67119WX*** lab box are explained in the following paragraphs.

### 4.4.1 DDC-78053-1 Cable Assembly for ABD Main I/O

#### 4.4.1.1 Connector J1

The DDC-78053-1 breakout cable mates to the ABD's main I/O connector J1 (Conec 15-002231). The mating connector to J1 is a 78-pin 'D' connector H1 (Amphenol 17E-1728-1, may also be ordered as DDC P/Ns 5301-0641-0001, 5301-0641-0002, and 5301-0639-0001). The pinout for ABD J1 is shown in Table 2. The breakout cables are terminated as follows:

- The breakout cable with the ARINC 429 channels, 1553 RT Address/discrete signals, the MIL-STD-1553 control inputs, and the CONFIGURATION and RESTORE ABD control inputs. This cable is terminated with 62-position 'D' type receptacle connector J1 (Amphenol 1658684-1). The pinout for DDC-78053-1 J1 is shown in Table 14.
- The two Ethernet cables are terminated with molded female RJ45 jacks EJ1 and EJ2 (Computer Cable C5E-MF-UTP-03-BL).
- The four cables for MIL-STD-1553 Channels 1 and 2 are terminated with twinax connectors CJ1, CJ2, CJ3, and CJ4 (Trompeter CJ70-47).
- The CONFIG_MODE_EN_L and a GROUND connection are terminated in female BNC connector J2 (Pomona 4969). The DDC-78053-1 cable assembly also includes a shorting cap for this connector (Pomona 5085, may also be ordered as DDC P/N 5301-0663-0001). To enable Configuration mode, the shorting cap must be plugged into the female BNC connector. For normal operation, the shorting cap must be removed from the BNC connector.
- This cable assembly also comes with an accessory kit, DDC-75594-1. This includes:
  - The mating connector to J1, which is a 62-position, 'D' type connector J1 (Amp/Tyco 1658673-1).
  - Pins (62) for P1 (Amp/Tyco 1658670-4).
  - Latching block for P1 (Amp/Tyco 208101-8).



Figure 15. ABD J1 Harness Assembly DDC-78053-1

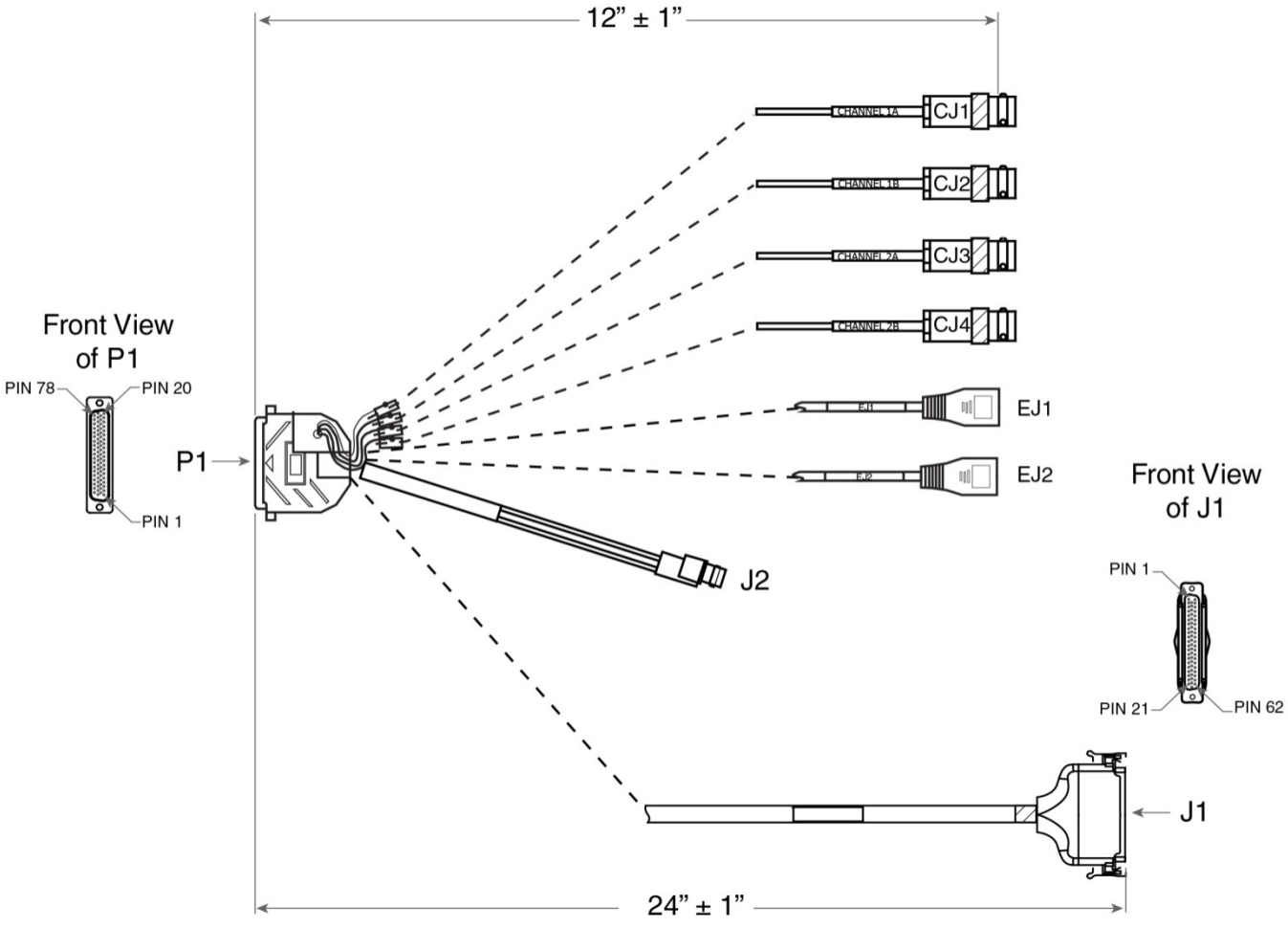



Figure 16. ABD J1 Harness Assembly DDC-78053-1Outline

Connector Pinout for DDC-78053-1 Cable Connector J1, with MIL-STD-1553 RT Address/Discrete IO and Control Input Signals, and ARINC 429 Signals

**Table 14. Pinout for DDC-78053-1 Cable Connector J1**

| Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|
| 1 | GROUND | 22 | TX_INH_AB2 | 43 | ARINC_TXDIS_L_1 |
| 2 | GROUND | 23 | BC_DISABLE_1 | 44 | ARINC 429 CH1+ |
| 3 | GROUND | 24 | RTBOOT_L_1 | 45 | ARINC 429 CH1- |
| 4 | GROUND | 25 | TX_INH_AB1 | 46 | GROUND |
| 5 | RT Chan#1 PAR/ BC_TRG/ SSFLAG* Chan#1/GP Discrete#0 | 26 | GROUND | 47 | RESTORE_EN_L |
| 6 | RT Chan#1 0/GP Discrete #1 | 27 | ARINC_TXDIS_L_3 | 48 | CONFIG_MODE_L |
| 7 | RT Chan#1 1/GP Discrete #2 | 28 | ARINC 429 CH3+ | 49 | GROUND |
| 8 | RT Chan#1 2/GP Discrete #3 | 29 | ARINC 429 CH3- | 50 | N/C |
| 9 | RT Chan#1 3/GP Discrete #4 | 30 | ARINC_TXDIS_L_6 | 51 | N/C |
| 10 | RT Chan#1 4/GP Discrete #5 | 31 | ARINC 429 CH6+ | 52 | N/C |
| 11 | GROUND | 32 | ARINC 429 CH6- | 53 | N/C |
| 12 | ARINC_TXDIS_L_5 | 33 | RT Chan#2 PAR/GP Discrete#6 and BC_TRG/ SSFLAG* Chan#2 | 54 | N/C |
| 13 | ARINC 429 CH5+ | 34 | RT Chan#2 0/GP Discrete #7 | 55 | N/C |
| 14 | ARINC 429 CH5- | 35 | RT Chan#2 1/GP Discrete #8 | 56 | N/C |
| 15 | ARINC_TXDIS_L_4 | 36 | RT Chan#2 2/GP Discrete #9 | 57 | N/C |
| 16 | ARINC 429 CH4+ | 37 | RT Chan#2 3/GP Discrete #10 | 58 | N/C |
| 17 | ARINC 429 CH4- | 38 | RT Chan#2 4/GP Discrete #11 | 59 | N/C |
| 18 | GROUND | 39 | Shield | 60 | N/C |
| 19 | IRIG_DIG_1-2 | 40 | ARINC_TXDIS_L_2 | 61 | N/C |
| 20 | BC_DISABLE_2 | 41 | ARINC 429 CH2+ | 62 | N/C |
| 21 | RTBOOT_L_2 | 42 | ARINC 429 CH2- | | |

### 4.4.2 DDC-78055-1 Cable Assembly for ABD Power and Expansion Signals Connector J2

The DDC-78055-1 breakout cable mates to the ABD's power/expansion signals connector J2 (Conec 15-002201). The pinout for ABD J2 is shown in Table 3. The mating connector to J2 is a 26-pin 'D-SUB' connector P1 (Amphenol 17EHD-026S-AA00), with a backshell (Amphenol 17E-1725-1). These may also be ordered as DDC P/Ns 5301-0640-0001, 5301-0640-0002, and 5301-0638-0001. The breakout cables are terminated as follows:

- A breakout cable for the MIL-STD-1553 control signal inputs, grounds and shields. This terminates in a 15-position solder cup male connector J2 (TE Connectivity 5-747908-2). The mating connector for this is P2, which is supplied, a 15-position female connector (TE Connectivity 5-747909-7), with a cable clamp kit (TE Connectivity 207470-1). The pinout for DDC-78055-1 J2 is shown in Table 15.
- A six-wire breakout cable for 28V power, which includes three wires for 28 VDC and three wires for 28V RETURN. This cable is terminated by socket connector J1 (Kycon KPJX-CM-4S). This connector (J1) can mate to the ABD's 115/230 VAC-to-28 VDC power adaptor, Mean Well GS120A24-R7B. The power adaptor may be ordered from DDC under part number DDC-78164-1. Alternatively, the mating connector to J1 is P1, a 4-pin Mini DIN DC power connector (Kycon KPPX-4P). The pinout for DDC-78053-1 J1 is shown in Table 16.



**Figure 17. ABD J2 Harness Assembly DDC-78055-1**

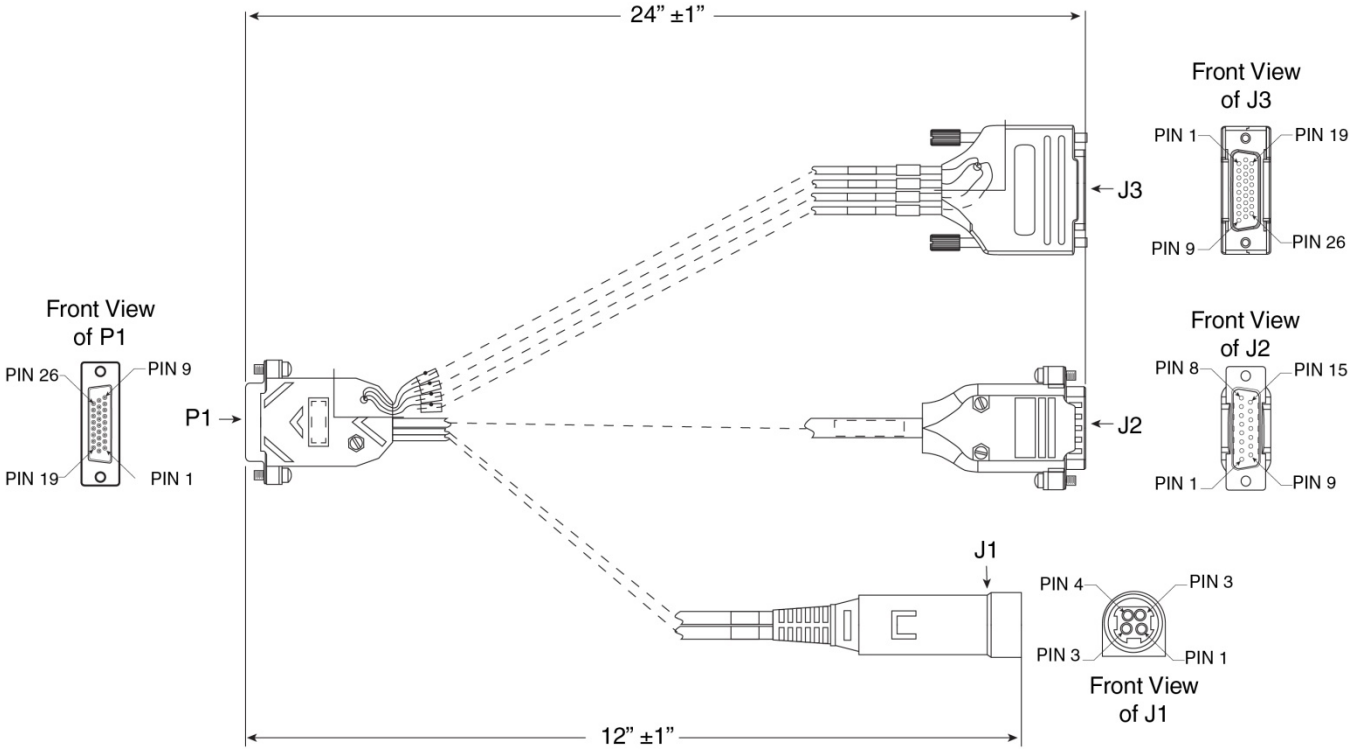



**Figure 18. ABD J2 Harness Assembly DDC-78055-1 Outline**

| Table 15. Pinout for DDC-78055-1 Cable Connector J2 (1553 control signals) | | | | | |
|---|---|---|---|---|---|
| **J2 Pin** | **Signal** | **J2 Pin** | **Signal** | **J2 Pin** | **Signal** |
| 1 | Looped System Shield | 6 | MIL-STD-1553 CH. 3 BC EXT_TRIG/RT SSFLAG* | 11 | System Shield/Board Digital Ground |
| 2 | Looped System Shield | 7 | IRIG_DIG_3-4 | 12 | N/C |
| 3 | Looped System Shield | 8 | MIL-STD-1553 CH. 4 TX_INH | 13 | N/C |
| 4 | MIL-STD-1553 CH. 3 TX_INH | 9 | MIL-STD-1553 CH. 4 BC_DISABLE | 14 | N/C |
| 5 | MIL-STD-1553 CH. 3 BC_DISABLE | 10 | MIL-STD-1553 CH. 4 BC EXT_TRIG/RT SSFLAG* | 15 | N/C |

| Table 16. Pinout for DDC-78055-1 Cable Connector J1 (28V power) | |
|---|---|
| **J1 Pin** | **Signal** |
| 1 | 28V Power In |
| 2 | 28V RETURN |
| 3 | 28V RETURN |
| 4 | 28V Power In |

## 4.5 External Power Supply

The ***BU-67119WX*** lab version of the ABD comes with an AC-to-DC power adaptor, Mean Well GS120A24-R7B, along with the four international AC line cords listed below. As an option, the kit consisting of the power adaptor and AC line cords may also be ordered separately for use with the ***BU-67115Wx*** and ***BU-67116Wx*** ruggedized versions of the ABD. The adaptor converts 115 or 230 VAC to 28 VDC for the ABD's use.

The power adaptor comes with the following US and international AC line cord attachments:

- For the US: Qualtek 212004-01 (90 in.)
- For the UK: Qualtek 370001-E01 (2.5 meters = 98.4 in.)
- For Europe: Qualtek 3640002-D01 (2.5 meters = 98.4 in.)
- For Japan: Qualtek 397002-01 (2.5 meters = 98.4 in.)

The power adaptor, along with the four AC line cords, may be purchased from DDC as part number DDC-78164-1.

# 5 DETAILED ARCHITECTURE

## 5.1 Ethernet Interfaces

The ABD includes two Ethernet interfaces. Both Ethernet interfaces are capable of operating over 10 BASE-T, 100 BASE-T, or 1000 BASE-T physical layers, with auto-negotiation capability. The Linux stack running on the ABD's Atom processor supports TCP/IP and UDP/IP protocols.

## 5.2 MIL-STD-1553 Interfaces

The ABD is available in versions including either one or two MIL-STD-1553 interfaces.

The ABD's 1553 interfaces are based on DDC's ***AceXtreme*** MIL-STD-1553 BC/RT/Multi-RT/Monitor architecture. Each channel provides complete multi-protocol support of MIL-STD-1553A/B and STANAG 3838.

### 5.2.1 1553 Transceivers

Each AceXtreme 1553 channel includes a 3.3V transceiver. To enable use in MIL-STD-1760 applications, transmitters are trimmed to meet the MIL-STD-1760 requirement of a minimum amplitude of 20 volts peak-to-peak, transformer coupled.

### 5.2.2 RT Address Selection and Discrete I/O signals

The RT addresses for the ABD's two 1553 channels may be configured by either hardware or software.

The 12 RT Address pins (5 RT Address pins and RT Address Parity for each channel) for the ABD's two MIL-STD-1553 channels may be programmed to operate in either of three modes:

1. As MIL-STD-1553 RT address inputs;
2. As general purpose discrete I/O signals; or
3. As BC_TRG/ SSFLAG* signals (J1 pins 27 and 6 only).

#### 5.2.2.1 Option #1: RT Address Inputs (default)

The default configuration for these 12 signals is to operate as the RT Address inputs for 1553 Channels 1 and 2. The two RT Addresses are latched immediately following ABD power turn-on. The user software (running on the internal processor in Protocol Conversion Mode; or on a remote processor in Remote Access Mode) will then have two options:

1. As the default, allow these signals to remain in a "tracking" mode, such that if the external values change, then the internal effective RT Address values change correspondingly.
2. By means of an API function call, the internal RT Address values are latched at their "power-up" values. In this case, the two RT addresses may later be changed via software, and the 12 signals assume different functions as indicated for "Option #2" or "Option #3" in the table.

#### 5.2.2.2 Option #2: General Purpose I/O Signals

For "Option #2", there's an API call to configure the 12 RT Address signals to operate as general purpose discrete I/O signals.

For the 12 (or possibly 10) Discrete I/O signals, there's an API function call to specify the data direction for each signal. The default values are to initialize as inputs.

For discrete I/O signals programmed as either inputs or outputs, there's an API function to read the signals' logic values. For discrete I/O signals programmed as outputs, there's a separate API function to program the signals' logic values.

#### 5.2.2.3 Option #3: BC_TRIG/SSFLAG Input Signals

Option #3, which is only applicable to pins 27 (RT Chann #1 Parity/GP Discrete#0) and 66 (RT Chann #2 Parity/GP Discrete#6), is to configure these two signals to operate as BC_TRG (trigger inputs) in BC mode or SSFLAG* inputs in RT mode.

If programmed to operate as BC_TRG/SSFLAG* inputs, pins 27 and/or 66 will operate as follows:

- In RT mode, if this input is asserted low, the Subsystem Flag bit will be set in the message's RT Status Word.
- In BC mode, during the execution of a Wait for External Trigger (WTG) instruction, the BC will wait for a low-to-high transition on BC_TRIG before proceeding to the next instruction.

***Note:*** *Refer to the BU-69094SX AceXtreme Bridge Device SDK Software User's Manual and the AceXtreme SDK Software Manual for additional information.*

### 5.2.3 MIL-STD-1553 Time Tag

The AceXtreme MIL-STD-1553 architecture includes an internal MIL-STD-1553 read/write Time Tag Register. This register is a host read/write 48-bit counter with a resolution of 100 ns. Another option allows software-controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register. For each message processed, the value of the Time Tag Register is loaded into the second location of the respective descriptor stack entry (“TIME TAG 48-bit WORD”) for both the BC and RT modes.

The functionality involving the Time Tag Register includes the capability to issue an interrupt request and set a bit in the Interrupt Status Register when the Time Tag Register rolls over from 0xFFFFFFFFFFFF to 0x000000000000; for RT mode, the capability to automatically clear the Time Tag Register following reception of a Synchronize (without data) mode command, or to load the Time Tag Register following a Synchronize (with data) mode command.

Additional time tag features supported by the ABD include the capability for the BC to transmit the contents of the Time Tag Register (lower 16-bits only) as the data word for a Synchronize (with data) mode command; the capability for the RT to “filter” the data word for the Synchronize with data mode command, by only loading the Time Tag Register if the LSB of the received data word is “0”; an instruction enabling the BC Message Sequence Control engine to autonomously load the Time Tag Register; and an instruction enabling the BC Message Sequence Control engine to write the value of the Time Tag Register to the General Purpose Queue.

### 5.2.4 MIL-STD-1553 Interrupt Handling

The software API library allows the user to implement custom Interrupt Service routines, which are operated on by the driver using a callback function. This allows for a high-level of scalability while maintaining the ease-of-use, which the API library affords.

The ABD’s MIL-STD-1553 interfaces are capable of generating interrupts on numerous events. The specific conditions available to generate interrupts can be found in the AceXtreme SDK software manual. This manual can be found on the DDC website at www.ddc-web.com.

In either Protocol Conversion Mode or Remote Access Mode, interrupt requests are issued to the ABD’s Atom processor. Further, for the case of Remote Access mode, the occurrence of an interrupt will result in a data packet being transmitted across Ethernet to the remote host computer, and the API on the remote host computer will be notified after this packet has been received.

### 5.2.5 DMA Architecture

DMA is supported for the ABD's MIL-STD-1553 channels. The 1553 channels' DMA engines are host initiated via the AceXtreme SDK. The AceXtreme SDK (ABD processor or remote Host) initiates a DMA transfer by writing to the respective 1553 channel's PCI controller. The channel will issue an interrupt once a read or write DMA transfer between the respective channel's shared memory and the ABD's Atom processor address space has been completed. The AceXtreme SDK will implement a round robin scheduling mechanism in order arbitrate between the ABD's two MIL-STD-1553 DMA channels.

In Remote Access Mode, an interrupt event will result in the ABD transferring a data packet across Ethernet to the remote host computer. For the case of DMA completion, this packet will include all of the data that was transferred via DMA from the 1553 or ARINC 429 shared RAM to Atom processor local RAM. The API on the remote host computer will then be notified after this packet has been received.

## 5.3 ARINC 429 Controller Architecture

Each of the ABD's six ARINC 429 channels may be programmed by software for either transmit or receive operation, and also for low-speed or high-speed operation. In addition, the ABD's six ARINC 429 controllers are each capable of operating in ARINC 429 or ARINC 575 mode. Each ARINC channel is independently programmable to operate in either mode of operation.

### 5.3.1 ARINC 429 Receive Mode

The ABD allows the programmer access to the following card features in a simple, easy to understand format:

- "Mailbox" type reception
- FIFO type reception
- Filtering of received data
- Time stamping of received data

Each receive channel has a receive hardware FIFO that is 32 bits wide by 32 words long. When combined with the 32 bit, 32k word software FIFO for each channel, the ABD provides excellent data transfer reliability. The transmission speed of the receive channels can be programmed in pairs. Receivers can be independently designated high or low speed. A 1024-word mailbox (software enhanced) on each channel stores the most recently received data value for any of the label/SDI (Source Destination Indicator) combinations. Data may be stored in the Mailbox only, FIFO only, or both the Mailbox and Receive FIFO.

The software API library supports two modes of reception: Mailbox and FIFO. Mailbox reception allows the user to retrieve the "latest" copy of data received on a particular label/SDI combination. This mode would be used when the user is only interested in the most recently received data. FIFO reception allows the user to dequeue words in the same sequence as they were received on the channel. This mode is useful when the user wants to see the exact order and timing of events on the data bus.

Data from each receive channel may by filtered prior to storing in the FIFO or Mailbox. A filter table, which is defined under program control, allows the user to specify which label/SDI combinations should be stored. This filtering allows the user to reduce the data being stored on the hard disk and displayed on the screen to only that data which is needed. A separate filter table is maintained for each receiver channel.

### 5.3.2 ARINC 429 Transmit Mode

The ABD allows the programmer access to the following card features in a simple, easy to understand format:

- FIFO Queued transmissions
- Scheduled data transmissions

For transmission, each channel includes a hardware FIFO that is 32 bits wide by 32 words long. When combined with the 32 bit, 32k word software FIFO for each channel, the cards offer excellent data transfer reliability.

Each transmit FIFO allows the host PC to reliably transfer blocks of data to the card for transmission. Use of this FIFO prevents the host PC from becoming I/O bound, and allows for other activities to proceed in the PC when not transferring data to the card.

Data contained in the FIFO is transmitted on command from the host system. The transmit channels may be configured as either high or low speed, and are independent of the receiver speed settings. The library supports two modes of transmission: Scheduled and FIFO. Scheduled transmission allows the user to configure the host to automatically transmit labels at regular intervals (e.g. every 20 ms). Data values can be changed or updated without stopping the scheduled transmission once it has been started.

FIFO transmission allows the user to transmit a series of words in sequence. FIFO and Scheduled transmissions can be intermixed on the same transmit channel.

When a transmitter is set up for both FIFO and scheduled transmissions, the scheduled data will take priority over the FIFO data. FIFO data is transmitted on the first available gap between scheduled data transmissions without altering the schedule.

### 5.3.3 ARINC 429 Time Tag

The ARINC 429 channels provide time stamping capability. Each received data word will be time stamped if the user specifies to do so in the EnableTimeStamp() API library routine of the ARINC 429 API Library. The time stamping of each data word has a resolution of 1 µs.

### 5.3.4 ARINC 429 Interrupt Handling

The ABD ARINC 429 Controllers are capable of generating interrupts to the host computer. Using the supplied ARINC 429 SDK, the host is capable of configuring the ARINC controllers to generate interrupts based on numerous events. Each channel may be configured independently of each other.

Using the **SetIntCondition()** function within the SDK allows the user to define interrupts conditions per interface. The interrupt conditions are:

1. An ARINC Protocol word is received
2. A Fail warning is received
3. An ARINC Function test command is received.
4. An ARINC solo command word is received.
5. An ARINC transmit start command is issued.
6. No data Received
7. End of transmission
8. Normal operation mode received
9. Data Pattern match
10. Word type match
11. Receiver buffer is full
12. Received FIFO rollover

## 5.4 Configuration Mode Enable Input

The ABD's CONFIG_MODE_EN_L input signal allows users to be able to select between CONFIGURATION_MODE and normal RUNNING_MODE. CONFIG_MODE_EN_L is brought out on pin 8 of the ABD's main I/O connector J1.

In addition, the CONFIG_MODE_EN_L signal and a GROUND connection are terminated by female BNC connector J2 (Pomona 4969). The DDC-78053-1 cable assembly also includes a shorting cap for this connector (Pomona 5085 , may also be ordered as 5301-0663-0001).

Asserting this signal low, which may be done by installing the shorting cap over J2, selects CONFIGURATION_MODE, while leaving this signal open or asserting it high selects RUNNING_MODE. To select normal RUNNING_MODE, the shorting cap must *not* be installed over J2.

In CONFIGURATION_MODE, the following may be set or changed over the ABD's Ethernet channel 1 interface:

- IP Address (fixed or DHCP)
- Update the operating system.
- Update the FPGA Build (into main FPGA location)
- Update the DDC Libraries.
- Load Custom applications.

CONFIG_MODE_EN_L is sampled continuously, allowing the ABD to be put into or taken out of CONFIGURATION_MODE at any time. This signal includes an on-board 10 kΩ pull-up resistor.

## 5.5 Restore Enable Input

The RESTORE_EN_L input signal is brought out on pin 7 of the ABD's main I/O connector J1.

This signal, which includes an on-board 10 kΩ pull-up resistor, should only be asserted low to cause the ABD to initialize in its backup mode. This operation is only intended to be used for situations where the embedded software has been irrevocably corrupted. The effects of asserting this signal include:

- Loading a back-up copy of the Linux operating system.
- Automatically restores the IP Address to a fixed value.
- Restores the default configuration parameters to factory default values.
- RESTORE_EN_L is sampled continuously, allowing the ABD to be put into its backup mode at any time.

# 6 SOFTWARE INSTALLATION

For information about ABD software, refer to the BU-69094SX AceXtreme Bridge Device SDK Software User's Manual and the AceXtreme SDK Software Manual.

# 7 ORDERING INFORMATION



| Model Number | Ethernet Ch. | 1553 Ch. | 429 Ch. | RoHS |
|---|---|---|---|---|
| BU-67119W000R-JL0 | 2 | 0 | 6 | ✓ |
| BU-67119W100R-JL0 | 2 | 1 | 0 | ✓ |
| BU-67119W200R-JL0 | 2 | 2 | 0 | ✓ |
| BU-67119W300R-JL0 | 2 | 2 | 6 | ✓ |

Temperature Range is 0°C to +55°C for all ***BU-67119WX*** models.



| Model Number | Ethernet Ch. | 1553 Ch. | 429 Ch. | RoHS |
|---|---|---|---|---|
| BU-67115W000L-CC0 | 2 | 0 | 6 | |
| BU-67115W100L-CC0 | 2 | 1 | 0 | |
| BU-67115W200L-CC0 | 2 | 2 | 0 | |
| BU-67115W300L-CC0 | 2 | 2 | 6 | |

Temperature Range is -40°C to +71°C for all ***BU-67115Wx*** models.



| Model Number | Ethernet Ch. | 1553 Ch. | 429 Ch. | RoHS |
|---|---|---|---|---|
| BU-67116W000L-2C0 | 2 | 0 | 6 | |
| BU-67116W100L-2C0 | 2 | 1 | 0 | |
| BU-67116W200L-2C0 | 2 | 2 | 0 | |
| BU-67116W300L-2C0 | 2 | 2 | 6 | |

Temperature Range is -40°C to +85°C for all ***BU-67116Wx*** models.

***Note:*** *1. For the* **BU-67116Wx** *board series, conformal coat is available.*
*2. Add "N" to end of the part number for Acrylic Conformal Coat or "U" for Polyurethane Conformal Coat.*

## Included Accessories:

**For the 119W version:**

- Breakout cable to main I/O connector J1: DDC-78053-1
- Breakout cable to power/expansion connector J2: DDC-78055-1
- Accessory kit: DDC-75594-1 mating connector, etc. to DDC-78053-1 cable
- Shorting cap for DDC-78053-1 J2 (for enabling Configuration mode): Pomona 5085, may also be ordered as DDC P/N 5301-0663-0001.
- Mating connector for DDC-78055-1 J2: TE Connectivity 5-747909-7, may also be ordered as DDC P/N 5301-0637-0001. Also, Cable clamp kit, TE Connectivity 207470-1.
- 115/230 VAC-to-28 VDC power adaptor: Mean Well GS120A24-R7B, along with the following AC line cords: Qualtek 212004-01 (US), 370001-E01 (UK), 3640002-D01 (Europe), and 397002-01 (Japan). A kit consisting of the power adaptor and the AC line cords may be ordered from DDC as P/N DDC-78164-1.

**For the 115W and 116W versions:**

- Mating connector to J1: Amphenol 17E-1728-1
- Mating connector to J2: Amphenol 17EHD-026S-AA00, with backshell Amphenol 17E-1725-1

## Optional Accessories:

- Mating connector to DDC-78055-1 J1 (power input), Kycon KPPX-4P, may be ordered as DDC P/N 5301-0645-0001.
- Included accessories for the ***BU-67115/6Wx*** may be optionally ordered for ***BU-67119WX***.
- Included accessories for ***BU-67119WX*** may be optionally ordered for the ***BU-67115/6Wx***.

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