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REPLACING BUS-65517II

# IBM® AT COMPATIBLE MIL-STD-1553 SIMULATOR AND TESTER CARD

## DESCRIPTION

DDC's BUS-65518 is a versatile, half-size 16-bit ISA Bus printed circuit card designed for the test and simulation of MIL-STD-1553 systems. It provides full, intelligent interfacing between the serial dual redundant MIL-STD-1553 data bus and the IBM PC. User-friendly software allows the BUS-65518 to simultaneously simulate a Bus Controller (BC), multiple Remote Terminal Units (RTUs), and/or a selectable, triggerable Bus Monitor (MT). The BUS-65518 may be either direct or transformer coupled to an external 1553 bus for use with user-provided 1553 devices.

The BC and RTUs evaluate each 1553 message in real time, determining if any format errors have occurred. Separate registers are maintained for the last command word and the last status word of each emulated RTU. In addition, the user may inject errors into any 1553 message issued by the emulated BC or RTUs. These errors include word count, bit count, zero crossing, parity, and, in the case of emulated RTUs, response errors.

The intelligent MT captures the 1553 bus traffic. The user can define when MT operation is to begin and which messages (based on the RTU address, T/$\overline{R}$ bit, and subaddress) are to be captured. Monitored information is displayed on a message by message basis.

Both DOS and MS Windows® Menus are provided and optional software is available to allow the BUS-65518 RTUs to respond within the timing constraints of MIL-STD-1553A. An optional driver allows the user to control the operation of the BUS-65518. These features make the BUS-65518 an excellent choice for dynamic simulation of MIL-STD-1553B systems.

## *FEATURES*

- ***Simulation and Test of MIL-STD-1553 Systems***
- ***Half-Size 16-Bit ISA Bus Card***
- ***128K Bytes of Shared RAM***
- ***Simultaneous Emulation of BC, Up to 31 RTUs, and MT***
- ***Selective Message Monitor***
- ***Most Comprehensive Error Injection and Detection Capability in the Industry***
- ***32-Bit Time Tag***
- ***User-Friendly Menu Software for DOS and Windows***
- ***Optional Runtime Libraries for DOS and Windows***
- ***Optional Software for RT Validation and Production Testing***

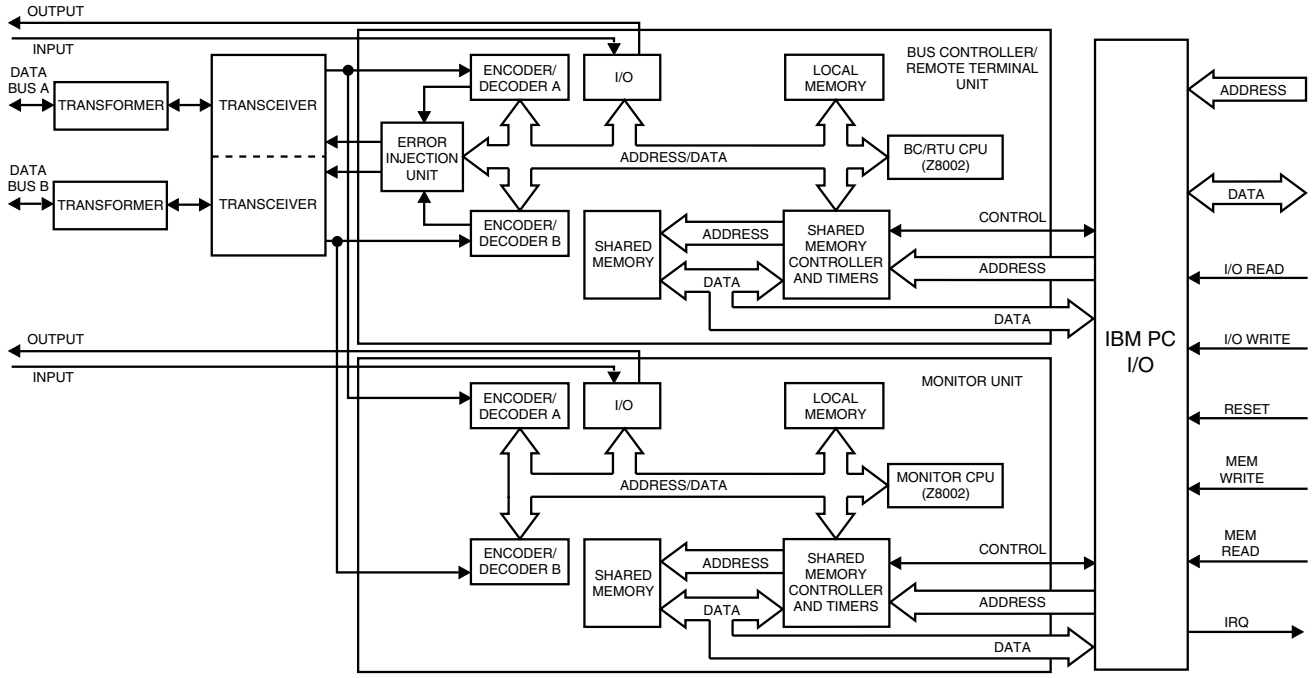



**FIGURE 1. BUS-65518 BLOCK DIAGRAM**

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® MS Windows is a registered trademark of Microsoft Corporation.

| TABLE 1. BUS-65518 REQUIREMENTS AND CAPABILITIES |
|---|
| **HARDWARE REQUIREMENTS**<br>80x86 computer with 16-Bit ISA Slot<br>DDC's BUS-65518 MIL-STD-1553 Simulator and Tester Card |
| **SOFTWARE REQUIREMENTS**<br>PC DOS 3.1 or higher<br>DDC's BUS-65518 Software diskettes |
| **AVAILABLE OPERATIONS**<br>- Tests and simulates MIL-STD-1553 BC and up to 31 RTUs.<br>- Provides independent MT mode operation.<br>- Error injection and detection capabilities. |

| TABLE 2. BUS-65518 HARDWARE SPECIFICATIONS | | | |
|---|---|---|---|
| **PARAMETER** | **UNITS** | **VALUE** | |
| **POWER SUPPLIES** | | **Idle** | **Max*** |
| +5 V Supply Current Drain | A | 1.7 | 1.8 |
| +12 V Supply Current Drain | mA | 15 | 400 |
| -12 V Supply Current Drain | mA | 55 | 55 |
| **TEMPERATURE RANGE** | | | |
| Operating (Case) | °C | 0 to 50 | |
| Storage | °C | -65 to 150 | |
| **PHYSICAL CHARACTERISTICS** | | | |
| Half-size card; requires one 16-bit slot. | in (mm) | 4.81 x 6.75 (122.2 x 171.5) | |

*(100% Duty Cycle at MAX Transmit Amplitude [28 $V_{PP}$] )

## GENERAL

The BUS-65518 (IDEA Card) allows a PC to simultaneously simulate a MIL-STD-1553 BC, multiple (up to 31) RTUs, and an intelligent MT. The BUS-65518 may be either direct or transformer coupled to a dual redundant external 1553 bus, for operation with user-provided 1553 devices.

The BUS-65518's operation as BC, RT, and Monitor is implemented through the use of two Z8002 embedded processors. One processor operates as a combined BC/RT while the other processor operates as a bus monitor. Each Z8002 processor communicates with the PC via independent shared memories residing on the BUS-65518 card and through a common interrupt request line on the ISA backplane.

The 64K x 16 of static RAM is shared by the PC host and the two Z8002 processors with memory arbitration handled automatically by the BUS-65518. The shared RAM interface to the BUS-65518 consists of eight 8K x 16 pages; at any given time, one page is used by the BC/RT and the other by the MT. As such, the BUS-65518 requires only 32K (a half segment) within the PC's address space. A maximum wait of 1 μsec can occur. The BUS-65518 will withhold the I/O channel ready signal on the ISA backplane while a word is being transferred to or from the RAM by one of the Z8002 processors.

The BUS-65518 contains a DIP switch which is used to specify the I/O mapped base address of four 8-bit control registers. The base address of the 32K bytes of shared RAM and the hardware interrupt level are software programmable via the BUS-65518's I/O mapped control registers.

Full error detection features are provided in all modes of operation. In addition, user specified errors – including bit count, Manchester II errors – may be injected in both BC and any of the emulated RTU modes.

Operation of the BUS-65518 is controlled through the use of DOS or Windows based user-friendly IDEA menus. The IDEA for DOS menu provides a fast text based user interface while the IDEA for Windows menu provides a flexible graphical multitasking interface. Both versions of the menu provide an interactive software interface which allows for full control of the features and functionality of the BUS-65518.

## BUS CONTROLLER MODE

The BUS-65518 Bus Controller supports all MIL-STD-1553B message formats. Up to 250 unique receive, transmit, mode code, and RT to RT messages may be defined at one time. Programmable attributes within a message are time to next message, bus (channel A or channel B), intermessage routines, and injected error. The time to next message defines the time from the start of the present message to the start of the next message. The time to next message is programmable up to 65,535 μsec in 1 μsec increments.

### *MINOR AND MAJOR FRAMES*

The execution of messages is controlled by a message list referred to as a frame. The frame specifies the contents and timing of complete communication runs by the BC. Each entry in the frame is either a reference to a message or a special symbol. The entire frame is referred to as a major frame. The major frame is divided into minor frames of equal time duration.

The major frame time is based on a programmable 32-bit counter with 2 μsec resolution. The BUS-65518 supports major frames of up to 1000 messages for single buffered mode or up to 100 messages for double buffered mode, and the period is up to 143 minutes.

### *BC ERROR INJECTION*

Error conditions may be injected on a message by message basis. The BUS-65518 supports three categories of injected BC errors: length errors, encoding errors, and gap errors. Length errors include both word count errors and bit count errors. Word counts of -32 to +1 words may be programmed. Bit counts of +3, +2, +1, -3, -2, or -1 bit may be programmed on any word within the message.

Encoding errors are implemented though the use of two simple yet powerful mechanisms for modifying the output of the BUS-65518's Manchester encoder. The two modifying functions are glitch and inverse. A glitch will force the output of the encoder to an idle bus condition for the specified period of time. An inverse will invert the output of the encoder for the specified period of time. The placement of the error is specified by the word number, starting time, and width. The error may be placed in any word within the message. The starting time is programmed in 500 ns increments from the beginning of the specified word. The width of the error is specified in 50 ns increments up to 3 μsec. This error injection scheme lends itself to generating a host of errors

including invalid sync patterns, parity errors, and Manchester biphase errors.

A gap of 3, 4, or 5 μsec (measured mid-parity crossing to mid-sync crossing) may be inserted between any two words in a message. This allows for a "dead time" gap between words of 1, 2, or 3 μsec.

### *INSERTING ASYNCHRONOUS MESSAGES*

The BUS-65518 allows an asynchronous message to be inserted while the card is running. This inserted message will be executed upon completion of the current message.

### *BC INTERMESSAGE ROUTINES*

Upon completion of a BC message, the BUS-65518's on-board processor executes 2 intermessage routines. These routines are contained within the firmware for the on-board Z8002 processor. The firmware is downloaded to the processor when the card is reset. Intermessage routines are used to implement automatic retries on failed messages as well as other “end of message” functions. TABLE 3 provides a summary of the BUS-65518's intermessage routines.

### *RESPONSE TIMEOUT*

The BUS-65518 BC RTU’s and MT support programmable response timeout values of 14, 15, 18, and 20 μsec.

## RT MODE

The BUS-65518 can simultaneously simulate the operation of 31 unique remote terminals (RTs) plus a broadcast address. The BUS-65518 maintains 31 independent "last status" and "last command" words allowing for full support of transmit last command and transmit status mode commands. The BUS-65518 supports full RT command illegalization for each transmit or receive message based on RT address AND subaddress. In addition, individual mode commands may be illegalized.

### *RT ERROR INJECTION*

Error conditions may be injected on an individual RT basis. The BUS-65518 supports five categories of injected RT errors: length errors, encoding errors, gap errors, status address errors, and response errors. Length errors include both word count errors and bit count errors. Word counts of -32 to +1 words may be programmed. Bit counts of +3, +2, +1, -3, -2, or -1 bit may be programmed on any word within the message.

Encoding errors are implemented though the use of two simple yet powerful mechanisms for modifying the output of the BUS-65518's Manchester encoder. The two modifying functions are glitch and inverse. A glitch will force the output of the encoder to an idle bus condition for the specified period of time. An inverse will invert the output of the encoder for the specified period of time. The placement of the error is specified by the word number, starting time, and width. The error may be placed in any word within the message. The starting time is programmed in 500 ns increments from the beginning of the specified word. The width of the error is specified in 50 ns increments up to 3 μsec. This error injection scheme lends itself to generating a host of errors

**TABLE 3. BC/RT INTERMESSAGE ROUTINES**

| |
|---|
| NO OPERATION |
| RETRY CURRENT MESSAGE ON ALTERNATE BUS |
| RETRY CURRENT MESSAGE AND REMAIN ON ALTERNATE BUS |
| RETRY ON SAME BUS |
| INTERRUPT ON END OF MESSAGE |
| INTERRUPT ON FRAME SYMBOL |
| SET SERVICE REQUEST BIT IN STATUS |
| RESET SERVICE REQUEST BIT IN STATUS |
| INTERRUPT AFTER ACCESSING TX/RX DATA TABLE |
| INTERRUPT AFTER MODE COMMAND |
| INTERRUPT AFTER TX/RX COMMAND TEMPLATE MATCH |
| INTERRUPT AFTER MODE COMMAND TEMPLATE MATCH |
| TIME-TAG (STORE RTC IN A CIRCULAR QUEUE) |
| RETRY ON SAME BUS AND THEN ON ALTERNATE BUS |
| SET OUTPUT TRIGGER |
| RESET OUTPUT TRIGGER |
| WAIT FOR INPUT TRIGGER |
| NO RESPONSE ON BOTH BUSES |
| SET BUSY BIT IN STATUS |
| RESET BUSY BIT IN STATUS |
| SKIP NEXT MESSAGE |
| SKIP NEXT MESSAGE ONCE |
| BLOCK_DATA_BC |
| BLOCK_DATA_RT |

including invalid sync patterns, parity errors, and Manchester biphase errors.

A gap of 3, 4, or 5 μsec (measured mid parity crossing to mid-sync crossing) may be inserted between any two words in message. This allows for a "dead time" gap between words of 1, 2, or 3 μsec. A status address error may be injected in which the RT responds with a status word containing an RT address which does not match the terminal's RT address. The RT may be programmed to respond with any value from zero to 31 in its status response.

The BUS-65518 supports three types of response errors: no response, a late response, or a response on the wrong bus. No response errors may be programmed for a single channel (Bus A or Bus B) or for both buses. Injecting a no response error on one bus provides a simple mechanism for testing bus controller retry conditions. A late response may be programmed in the range of 12 to 30 μsec in 1 μsec increments.

### *RT INTERMESSAGE ROUTINES*

The RT section of the BUS-65518 also supports intermessage routines. Upon completion of an RT message the BUS-65518's on-board processor executes two intermessage routines. These routines are contained within the firmware for the on-board Z8002 processor which is downloaded when the card is reset.

The intermessage routine is specified by the data table that was used by the RT for a given message. Refer to TABLE 3 for a summary of the BUS-65518's intermessage routines.

## BC/RT DATA TABLES

The BUS-65518 maintains 250 data tables within the shared RAM on the card. Each data table may be up to 32 words in length. These data tables are common to both BC and RT. Internal lookup tables map each RT address, T/$\overline{R}$, subaddress combination (RT mode) and message number (BC mode) to a given data table. Data tables may be read or written to in real time (note: requires the BUS-65518's optional runtime libraries). Data tables may be either single or double buffered. Double buffering can be used to avoid contention when the PC's application and the 1553 bus access data tables simultaneously.

The BUS-65518 provides a block data mode in which the data table number associated with a given BC or RT message is incremented after completion of the message. The block data mode is implemented as a circular data structure. Each BC message and RT command (RT address, T/$\overline{R}$, and subaddress) has three data table numbers associated with it: first, last, and current. The current data table number will be incremented after completion of message until the value of last is reached, at which point the current table number will rollover to the value of first. The incrementing of the current data table is accomplished through the use of an intermessage routine.

## MONITOR MODE

The BUS-65518 contains an independent message monitor with the ability to filter messages in real time. Monitor selection or filtering is performed through the use of a lookup tabled based on the RT address, T/$\overline{R}$, and subaddress of command words. Monitored messages are stored into a 6K word circular buffer located in the shared RAM on the BUS-65518. Each entry in the monitor buffer contains an eight word header followed by a variable number of data words. Contained with the message header are the receive/transmit command(s), receive/transmit status(es), message format, Bus (A or B), a capture flag, word count (actual number of words in the message), a detected error field, and a 32-bit time tag (2 μsec resolution).

The transfer of the messages from the card's circular buffer to the host memory/disk is determined by the capture flag which is set upon detection of a predefined event. Capture events include immediately, command template match, exception, or trigger. The command template event is based on a 16-bit command word with a 16-bit mask. Exception events may be programmed for any exception: invalid command, invalid data, invalid status, gap preceding data, response time error, wrong RT address error, status set condition or an illegal command. The trigger event uses one of the eight monitor input pins on the 25-pin D-type connector as a trigger input.

### *INTERRUPTS*

Interrupts to the PC are requested by both the BC/RT and the Monitor on a common output. The hardware interrupt level used by the BUS-65518 is software programmable via an I/O mapped register on the card. The interrupt level may be programmed for any level from three thru seven, or nine thru 15.

### *BC INTERRUPT GENERATION*

BC interrupts may be enabled by a global interrupt mask for successful messages, communication errors, status set conditions, or on selected frame symbols (skip, break point, major frame, and minor frame symbols). The criteria for a status set condition is programmed globally through the use of a status mask. The status mask allows any of the 16 bits within an RT status word to be ignored. The status mask affects the generation of interrupts as well as the detected error field which is stored in the message structure.

BC interrupts are issued by intermessage routines associated with messages allowing for selective interrupt generation on a message by message basis. Each interrupt request is accompanied by a two word vector pushed onto a circular queue which is transparent to the user. The queue can hold up to 64 interrupt vectors; thus, the host computer is not required to immediately acknowledge the interrupt request.

### *RT INTERRUPT GENERATION*

RT interrupts may be enabled by a global interrupt mask for transmit/receive messages with no message error, mode commands with no message error, transmit/receive messages with the message error bit set, or mode commands with the message error bit set.

RT interrupts are issued by intermessage routines associated with data tables allowing for selective interrupt generation on a message by message basis. Each interrupt request is accompanied by a two word vector pushed onto a circular queue which is transparent to the user. The queue can hold up to 64 interrupt vectors; thus, the host computer is not required to immediately acknowledge the interrupt request.

### *MONITOR INTERRUPTS*

Monitor interrupts may be generated after each message is received or after one third of the monitor's circular buffer has been filled (approximately 2K words). This allows for either real-time analysis or mass collection/storage of monitored data.

## IDEA FOR DOS MENU

FIGURE 2 illustrates the menu options for the IDEA software.

### *SETUP MODE*

The SETUP menus define the BUS-65518 as a BC, one or more RTUs, and a selectable triggerable MT. No real-time activity is performed in this mode. Through menu screens, the user specifies what errors (if any) are to be injected into the messages issued by the BC, or within the response(s) (data or status words) of the emulated RTUs.

### *BUS CONTROLLER MODE*

The BC mode is programmed through a series of hierarchal menus. Up to 250 different messages may be defined at one time. The user defines these messages by overriding the default values in the SETUP/BC/MESSAGE menu (shown in FIGURE 3).

Error conditions may be injected into any of the messages. Once an error has been selected, menus prompt for additional information regarding the error (number of bits, length of error, position of error, etc.).

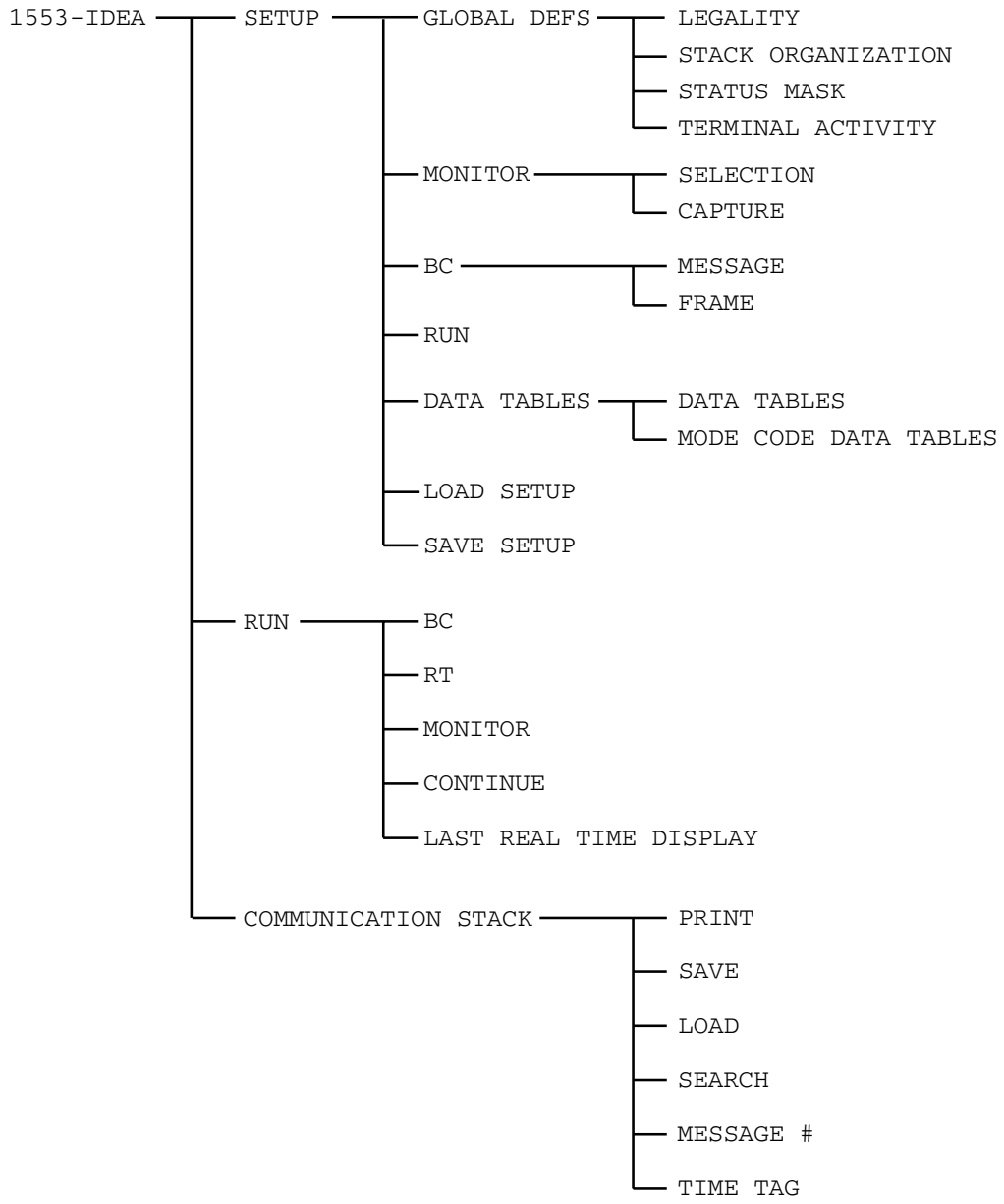



**FIGURE 2. BUS-65518 MENU TREE**

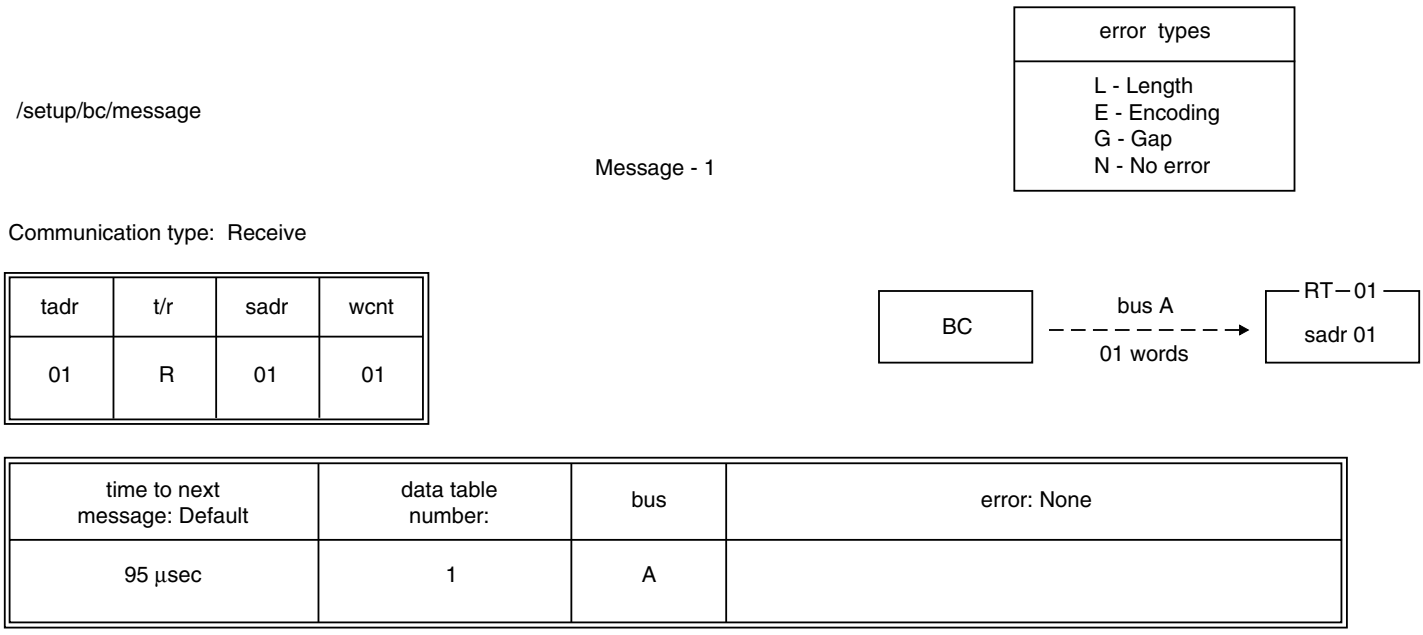



**FIGURE 3. SETUP/BC/MESSAGE MENU**

### *REMOTE TERMINAL MODE*

The BUS-65518 can be programmed to emulate up to 31 unique RTU addresses. The SETUP/RT menu is shown in FIGURE 4. The BUS-65518 dynamically examines each message and determines the appropriate response for each emulated RTU (clear response, suppress status word and set message error bit, etc.). Additionally the user can force any bit of a particular RTU's status word to be set to logic 1. All errors available in the BC mode can be injected along with the following response errors:

1) No response on Bus A, Bus B, or both buses
2) Late response (12 to 30µs)
3) Respond on the alternate bus

Each RTU can be programmed to accept bus control after a user defined delay.

### *BUS MONITOR MODE*

The BUS-65518 contains an independent MT which reconstructs monitored bus traffic and flags detected errors for user analysis. FIGURE 5, Communications Stack, illustrates how this information is displayed.

The BUS-65518 MT mode performs three stages of MT operation. The **first stage monitors** all messages received from the bus. The **second stage stores** the selected messages in an on-card circular buffer. The **third stage transfers** the contents of the circular buffer to the Communication Stack located in the PC'S system RAM. By default, the BUS-65518 software will use all available RAM (including expanded memory) for the Communication Stack; if desired, the stack size may be limited.

The first stage listens to both buses until a command is detected. It then receives, exclusively, from the active bus until the message is completed or invalidated. The second and third stages are programmed by the two MT menu options, SELECTION and CAPTURE.

### Selection

By default, the BUS-65518 monitors all 1553 bus traffic. If desired, the user can select which messages are to be stored in the Communication Stack. Messages may be selected on the basis of RT Address, $T/\overline{R}$ type, and subaddress.

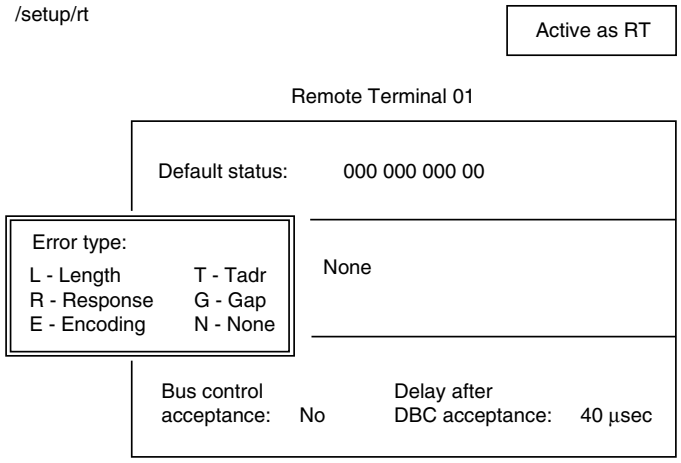



**FIGURE 4. SETUP/RT MENU**

### Capture

By default, the BUS-65518 begins storing the selected bus traffic as soon as the user issues the RUN command. If desired, the BUS-65518 can begin storage only after a specific command is seen on the bus, after any exception, (invalid word, invalid response, flagged bit in status word, etc.) is detected, after a specific exception, or upon receipt of an external trigger via the BUS-65518's D type connector. The CAPTURE condition is defined via the CAPTURE MENU.

After executing a RUN command, the 1553 traffic may be displayed by calling on the DISPLAY COMMUNICATION STACK screen (refer to FIGURE 5).

### *SETUP GLOBAL DEFINITIONS*

Global definitions are conditions common to BC, RTU, and MT. They include:

***1.Transmit Amplitude:*** The transmitter amplitude of the BC and RTUs can be varied in 0.1 V (max) steps from 0.1 V to at least 28Vpp as measured across a 77 ohm load attached to the BUS-65518 BNC connector. The amplitude is specified by entering a number between 0 and 255.

***2. Response Time:*** This option defines the maximum time (14, 16, 18, or 20 µs) allowed for an RTU response. If a status word is not received within the allowed time, the BC and MT will detect a No Response error.

| Print | saVe | Load | Search | Message_# | Time_tag |
|---|---|---|---|---|---|
| 1. Capture | TIME = 0 µsec<br>Cmd 0823 01-R-01-03<br>Cmd 1423 02-T-01-03<br>Exception No response | | BUS A | RT–01 ← bus A (00 words) RT–02 sadr 01 | |
| 2. | TIME = 2,044 µsec<br>Cmd 0823 01-R-01-03<br>Cmd 1423 02-T-01-03<br>Exception No response | | BUS A | RT–01 ← bus A (00 words) RT–02 sadr 01 | |
| 3. | TIME = 214 µsec<br>Cmd 1025 02-R-01-05<br>Data FB00 2301 2381<br>Exception Bad data Manchester encoding | | BUS A | BC → bus A (03 words) RT–02 sadr 01 | |
| 4. Capture | TIME = 0 µsec<br>Cmd 0A62 01-R-19-02<br>Data 043F AC4A<br>Stat 0C00<br>ME<br>Exception Bit in status | | BUS A | BC → bus A (03 words) RT–01 sadr 19 | |

End of Tables

**FIGURE 5. COMMUNICATION STACK**

/run/bc

REAL TIME DISPLAY

BC RT MON running halted

invalid commands = 65504

total commands = 0,000,000592

| tadr | invalid data | invalid status | delayed data | resp. timing | wrong tadr | bit in status | illegal mode/cmd | total messages |
|---|---|---|---|---|---|---|---|---|
| 00 | 00000 | 00000 | 00000 | 00001 | 00000 | 00001 | 00000 | 0,000,000,002 |
| 01 | 00000 | 00000 | 00000 | 00001 | 00000 | 00001 | 00005 | 0,000,000,032 |
| 02 | 00099 | 00000 | 00000 | 00012 | 00000 | 00000 | 00000 | 0,000,000,099 |
| 03 | 00000 | 00022 | 00000 | 00000 | 00000 | 00000 | 00000 | 0,000,000,022 |
| 04 | 00000 | 00000 | 00044 | 00000 | 00032 | 00000 | 00000 | 0,000,000,109 |
| 05 | 00000 | 00000 | 00000 | 00000 | 00000 | 00000 | 00000 | 0,000,000,333 |

**FIGURE 6. REAL-TIME DISPLAY**

### *RUN MODE*

In RUN mode the BUS-65518 communicates over the 1553 bus and message status statistics are displayed is real time. This includes both internal emulated 1553 devices as well as traffic to and from external, user-provided 1553 devices. A sample real-time display is shown in FIGURE 6.

## IDEA FOR WINDOWS

The IDEA for Windows program provides a user-friendly GUI (Graphical User Interface) for controlling the operation of the BUS-65518 card. IDEA for Windows, consisting of three independent programs: Setup Editor, Run, and Stack View, provides several enhancements over the IDEA for DOS program. These enhancements include real-time disk storage of 1553 traffic, support for Intermessage Routines in BC and RT modes, support for multiple cards, and comprehensive online help.

The Setup Editor contains a series of pull-down menus and dialog boxes used to create a file containing all the information needed to program the BUS-65518 card for BC, RT, and Monitor modes. This setup file may be stored to and retrieved from the disk. An additional utility is provided to convert the setup file from its native binary format to a readable text format and vice versa. Refer to FIGURE 7 for a sample BC message edit window.

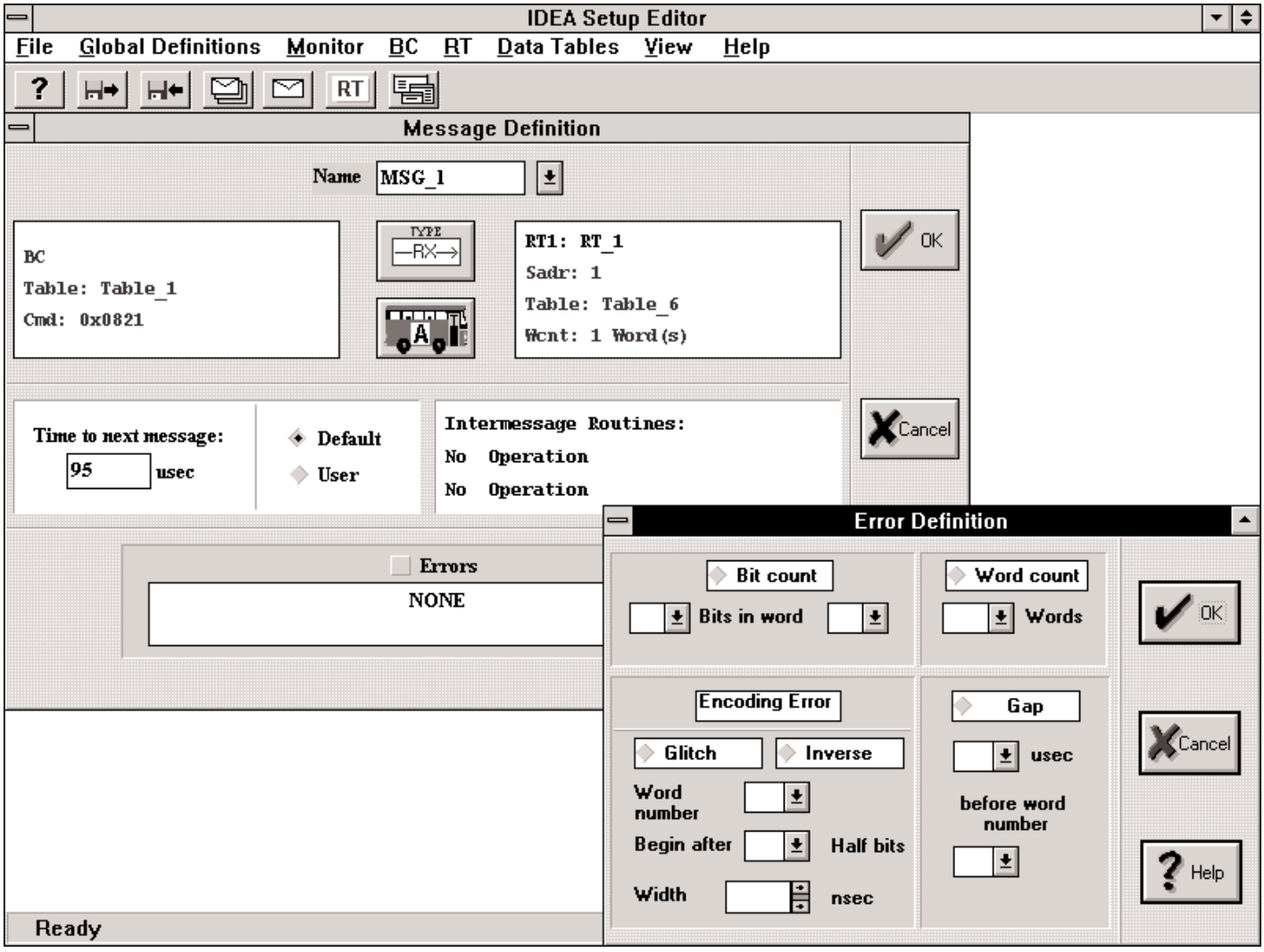



**FIGURE 7. BC MESSAGE/ERROR WINDOW IN SETUP EDITOR**

The Run program executes the scenario created using the setup editor. The Run program supports up to eight BUS-65518 cards running either individually or simultaneously. The communication stack output from the run program is stored into a user specified file on the hard disk. An option for cyclic real-time disk storage allows data storage to alternate between two files; when one of the files is full, the storage is redirected to the alternate file. A runtime display screen provides a real-time status of 1553 message traffic including number of messages as well as detected errors. FIGURE 8 illustrates a sample runtime display.

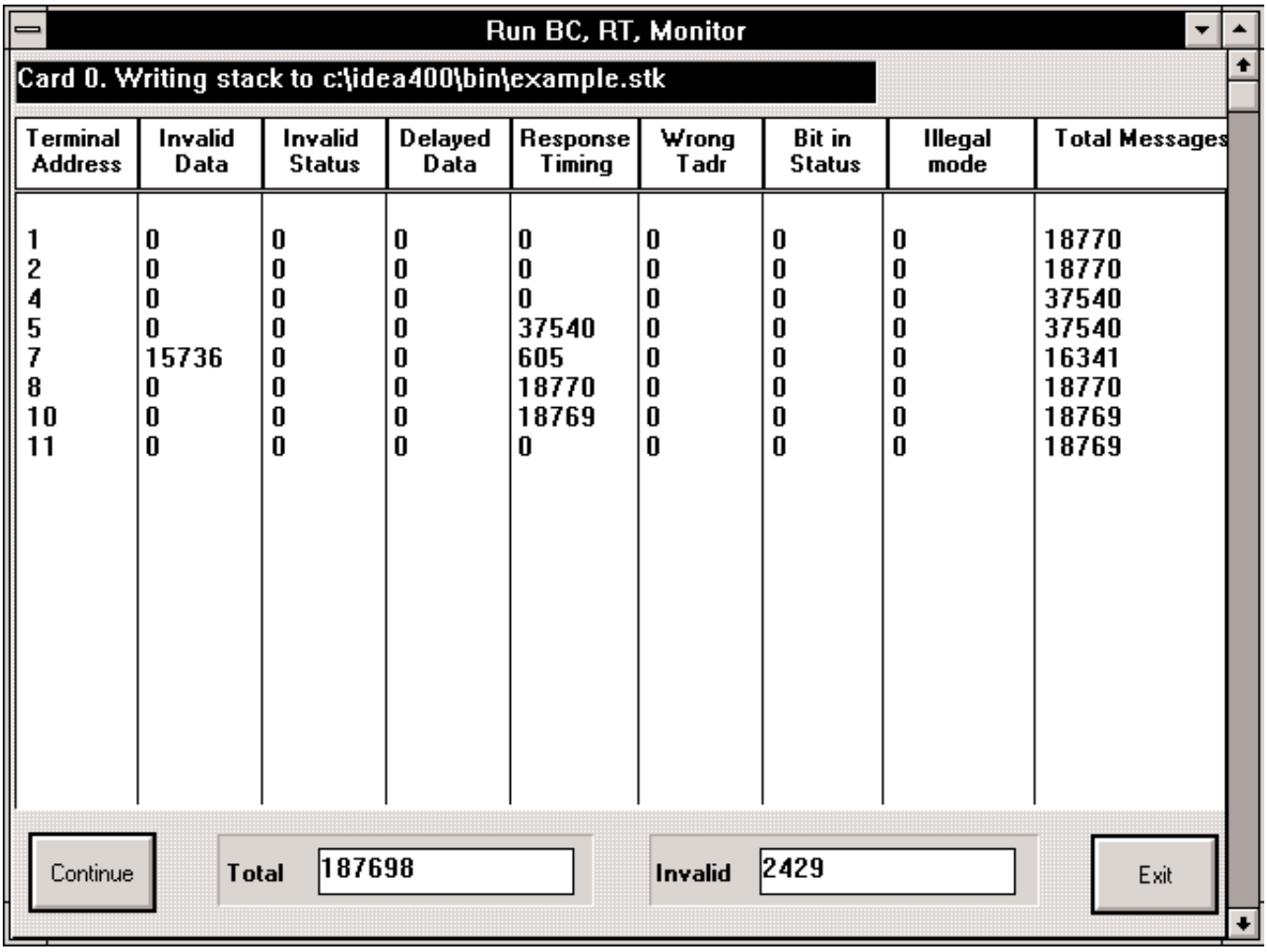



**FIGURE 8. RUNTIME DISPLAY**

Analysis of monitored 1553 traffic is accomplished through the use of the Stack View program. Stack View combines powerful search and filter capabilities with a 1553 bus traffic display. Stack files may be viewed in a scrolling window, stored to a text file or printed. A monitor stack file may be searched based on a command template, a status template, a data template, a time stamp, or an error condition. FIGURE 9 illustrates a sample communication stack display.

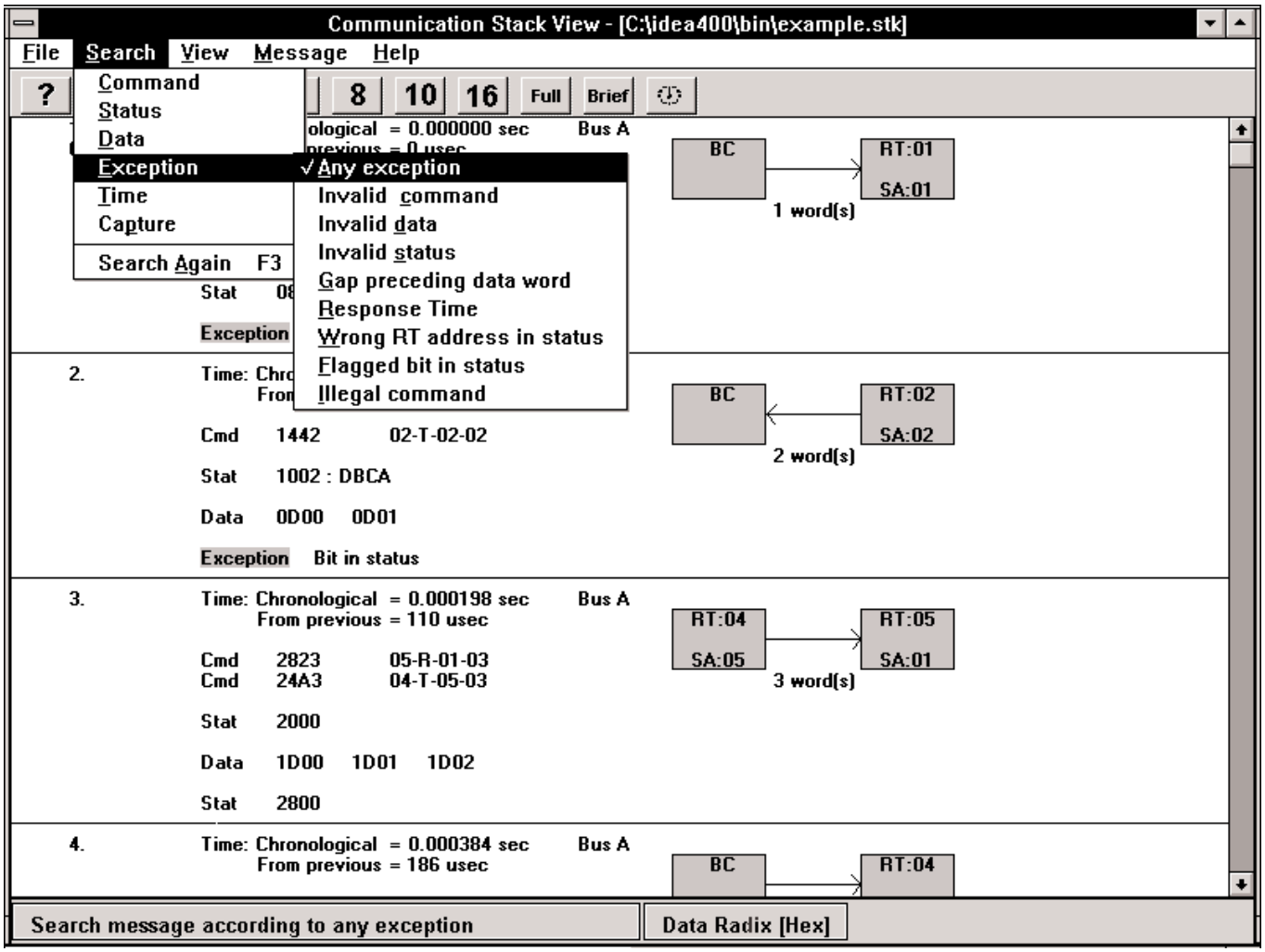



**FIGURE 9. COMMUNICATION STACK DISPLAY**

## INTERFACE TO A MIL-STD-1553 BUS

The BUS-65518 provides options for both direct and transformer coupling to a MIL-STD-1553 bus. FIGURE 10 illustrates the interface from the IDEA Card to a MIL-STD-1553 bus. Connections for both transformer (long stub) and direct (short stub) coupling are indicated. Transformer coupling is implemented using the triax connectors while direct coupling can be implemented using the D-type connector or Triax connectors. In accordance with MIL-STD-1553, a transformer coupled connection to a 1553 bus requires the use of a bus coupler. In addition, the 1553 bus must be properly terminated. A bus coupler contains an impedance matching transformer as well as a pair of fault isolation resistors.

The transmitter output voltage of the BUS-65518 may be varied in 256 steps from 0.1 V to at least 28 Vpp, measured across a 77 ohm resistor attached to the stub (triax connector).

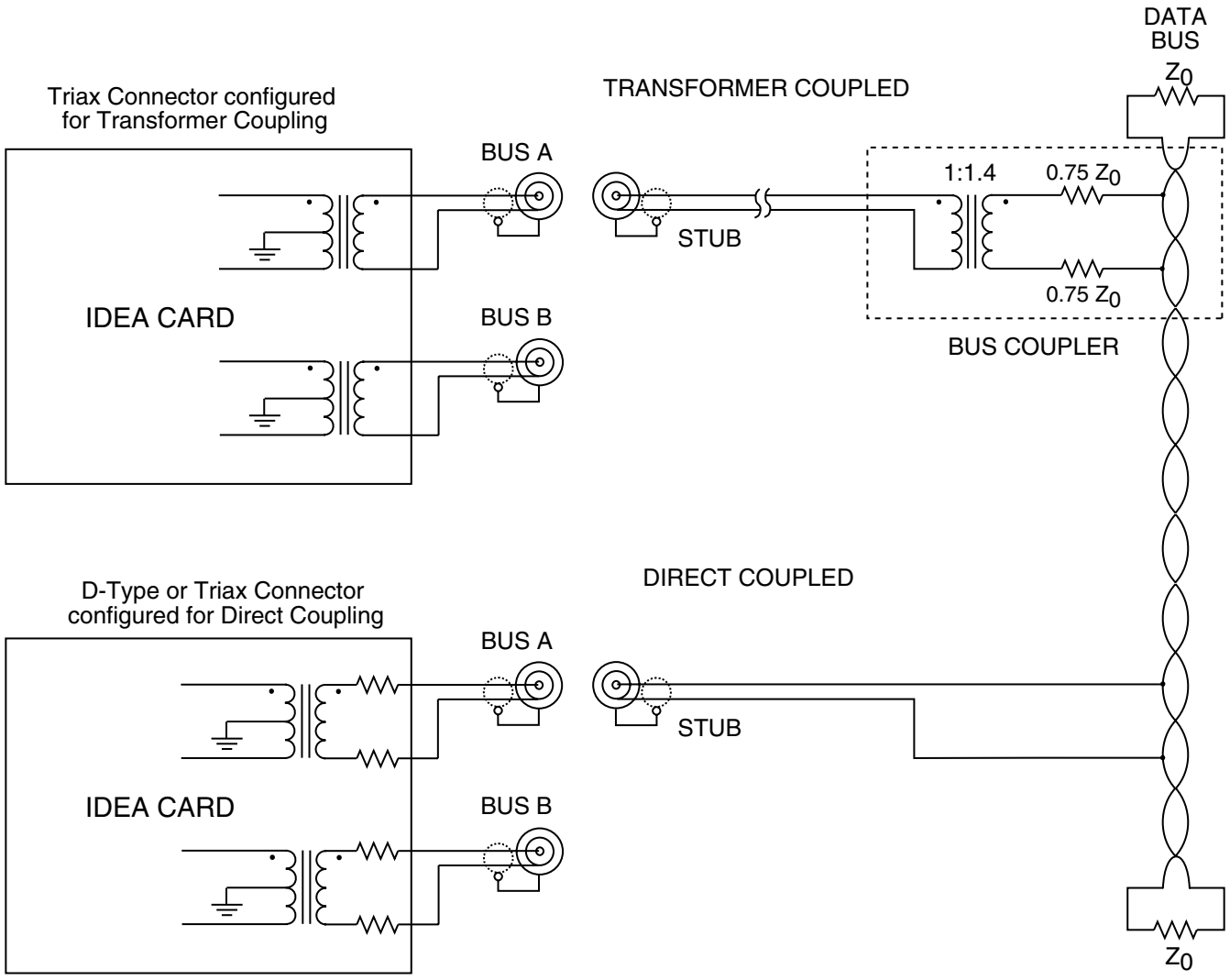



**FIGURE 10. BUS-65518 INTERFACE TO A MIL-STD-1553 BUS**

## CE MARK CERTIFICATION

This product carries the CE MARK signifying conformance to the requirements of COUNCIL DIRECTIVE 89/336 EEC. The supporting test (report) is on file at DDC, New York, USA and is available for on-site review.

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### DECLARATION OF CONFORMITY

We Data Device Corporation
105 Wilbur Place
Bohemia, NY 11716-2482

declare under our sole responsibility that the product(s)

**BUS-65518**

to which this declaration relates is in conformity with the following standard(s) or other normative document(s):

| | |
|---|---|
| EN 55022-1: 1998 | CLASS B; Conducted Emissions (150kHz to 30MHz) |
| | CLASS B; Radiated Emissions (30MHz to 1GHz) |
| EN 50082-1: 1997 | EN 61000-4-2:1995; Electrostatic Discharge |
| | EN 61000-4-3:1997; Radiation Immunity |
| | ENV 50204:1994; Radiated Immunity, Pulsed |
| | EN 61000-4-4:1995; EFT/Burst, Power and I/O Leads |
| | EN 61000-4-5:1995; Surge Immunity, Power Leads |
| | EN 61000-4-6:1996; Conducted Immunity, Power and I/O Leads |
| | EN 61000-4-11:1994; Voltage Dips and Interrupts |

following the provisions of COUNCIL DIRECTIVE 89/336 EEC

Place Bohemia, NY USA

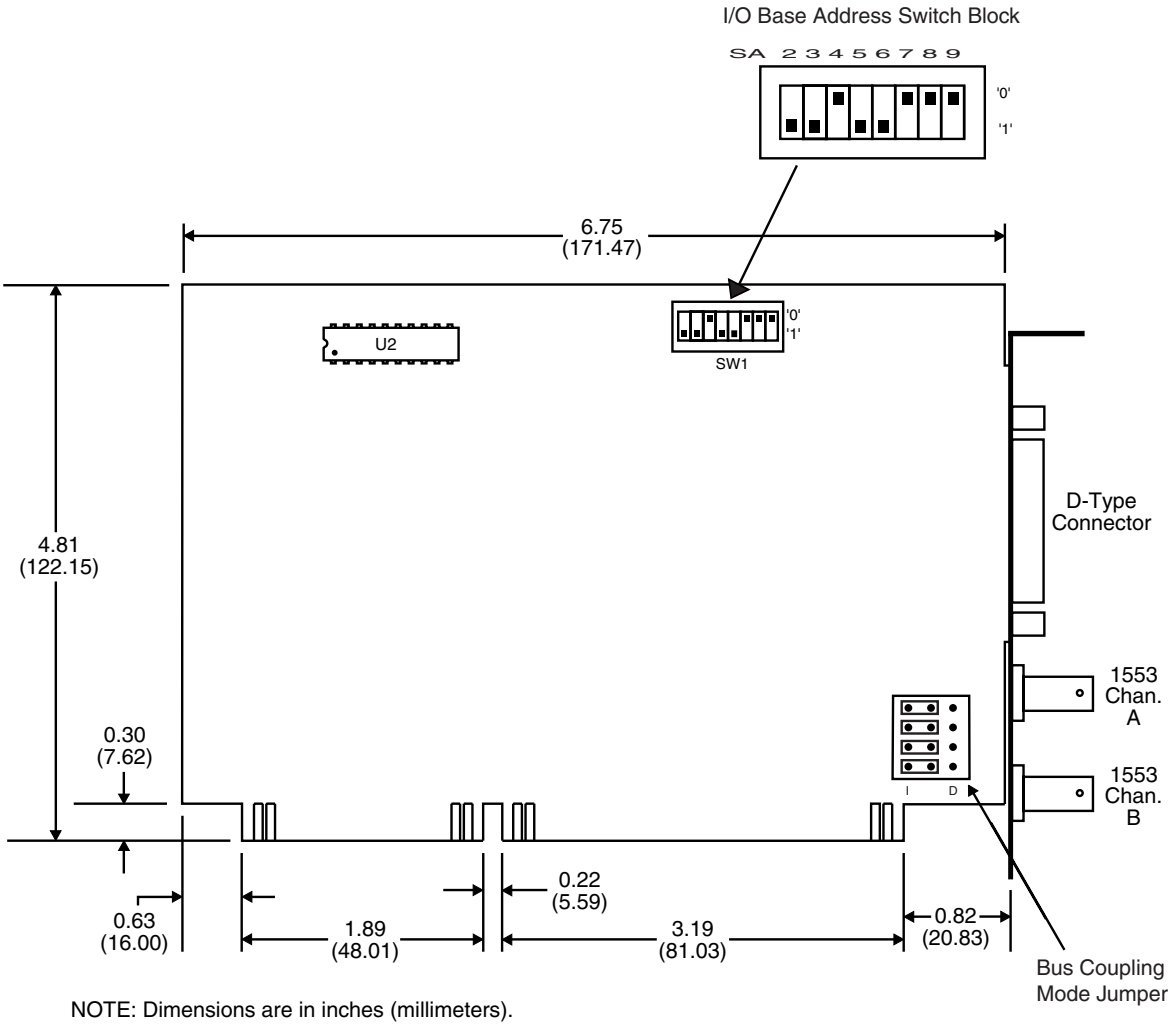
(Signature)

Date May 2, 2000

Joseph Saber
(Full Name)

Director, Product Assurance
(Position)

DDC-PAF-830A
04/05/2000




NOTE: Dimensions are in inches (millimeters).

**FIGURE 11. BUS-65518 MECHANICAL OUTLINE**

## ORDERING INFORMATION

BUS-65518 MIL-STD-1553 Simulator and Tester (IDEA) Card.

BUS-69XXX

**Software Upgrades:**

123 = Production Test Plan, plus 690135 components
124 = Validation Test Plan, Production Test Plan, plus 69135 components,
135 = Reconstructor, Parameter Monitor, “C” libraries (RTL) and Menu for DOS, Windows 3.1X, 95 and NT, support for MIL-STD-1553 A and B, (see Note 3 )

These products contain tin-lead solder finish as applicable to solder dip requirements.

Notes:

1. Above configurations are supported by Rev. E, U2 PAL.
2. The following part numbers are superceded by BUS-69135:
   BUS-69125, BUS-69128 and BUS-69129
3. A copy the BUS-69135 software is included with the purchase of a BUS-65518 card.

# NOTES

# NOTES

The information in this data sheet is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith.
Specifications are subject to change without notice.

Please visit our web site at **www.ddc-web.com** for the latest information.


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