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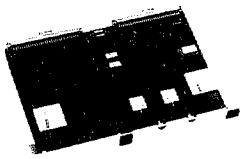
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DDC
ILC DATA DEVICE CORPORATION

BUS-65522 AND BUS-65523



MIL-STD-1553B BC/RTU/MT VME/VXI INTERFACE UNIT

FEATURES

- *VMEbus/VXIbus INTERFACE WITH INTELLIGENT 1553 BC/RT/MT*
- *STANDARD DOUBLE EUROCARD SIZE*
- *SUPPORTS ALL 1553B DUAL REDUNDANT MESSAGE FORMATS AND MODE CODES*
- *8K X 16 ON-BOARD DUAL ACCESS RAM*
- *D08(E0), D16 DATA TRANSFERS*
- *A16/24, A16/32 JUMPER SELECTABLE*
- *ON-BOARD TIME TAG COUNTER*
- *DYNAMIC WRAP-AROUND BUILT-IN-TEST (BIT)*
- *ON-BOARD MEMORY MANAGEMENT*

DESCRIPTION

The BUS-65522 provides full, intelligent interfacing between the serial dual redundant MIL-STD-1553B Data Bus and the parallel VMEbus and VXIbus. Software controls the BUS-65522's operation as either a 1553 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT).

The VME/VXI board is packaged on one double eurocard size printed circuit card. Its on-board 8K x 16 dual access RAM is double buffered, preventing partially updated data from being read by the CPU or transmitted to the 1553 Data Bus. The CPU can access any part of the shared RAM as needed.

All MIL-STD-1553 functions: address recognition, Manchester coding validation, bit count and mode code response are provided without subsystem intervention. The BUS-65522 contains eleven VMEbus/VXIbus and 1553 command registers which allow the subsystem to configure its operation under software control.

The BUS-65522 supports four groups of vectored interrupts. One custom interrupt can be programmed by the on-board PROM. The interrupts can be software controlled as to enable/disable, priority level and 8 bit vector.

Additional features include a dynamic wrap-around Built-In-Test (BIT), on-board Time Tag counter, and software loaded board base address and BUS-65522 RT address. The BUS-65522 supports all dual redundant mode codes and message formats. Its full compliance with MIL-STD-1553B makes it an excellent choice for dynamic real time applications.

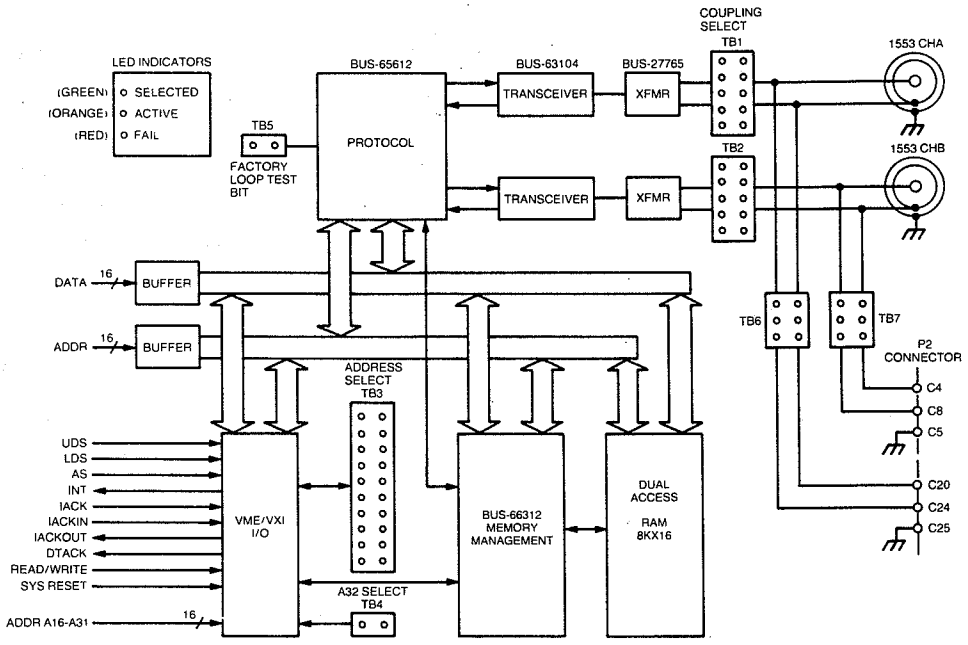


FIGURE 1. BUS-65522 BLOCK DIAGRAM

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TABLE 1. BUS-65522 & 65523 SPECIFICATIONS

PARAMETER	VALUE	UNITS
Power Supplies		
+ 5V (+/−10%)	1.00	Amps, max.
+ 12V-15V (+/−10%)	0.21 (100% DC)	Amps, max.
	0.06 (IDLE)	Amps, max.
− 12V-15V (+/−10%)	0.26 (100% DC)	Amps, max.
	0.13 (IDLE)	Amps. max.
Temperature Range		
Operating	0 TO +70	Degrees C
Storage	−65 TO +150	Degrees C
Size		
Double Eurocard	6.3" x 9.2" x 0.6"	Inches
	16 x 23.4 x 1.1	CM

GENERAL

The BUS-65522 provides a user friendly interface between the serial MIL-STD-1553B Bus and the VME/VXI Bus. The operating modes of the BUS-65522 are controlled through the use of eleven on-board registers. 1553 message traffic is stored and retrieved using the dedicated, memory mapped, on-board 8K words of RAM. The 1553 internal registers control and operate the BUS-65522. They include the Configuration Register, Start/Reset Register, 1553 Time Tag Register, Interrupt Select Register, and RTU Address Register. The Configuration Register defines the operating mode. The Start/Reset Register generates the start and reset signals. The Interrupt Mask Register enables desired interrupts, with the interrupt priority level being software programmable by the user. The RTU Address Register is used to program the RTU address. The 1553 Time Tag Register is used to time tag messages or act as a word counter in the out mode. The VME/VXI functions are controlled by the other six registers which include the Identification Register, Device Type, STATUS Control, offset, vector/enable/level and Device Type Extension Register.

The BUS-65522's 8K x 16 high speed static RAM is shared by the CPU and the 1553 Bus with memory arbitration handled automatically by the BUS-65522.

The BUS-65522 will withhold the $\overline{\text{DTACK}}$ signal to the CPU while a word is being transferred to or from the 1553 Bus. Since the memory arbitration is handled by simply stretching the handshake cycle, the wait state is transparent to the CPU's software. A maximum wait of 1.90 μs may occur.

The RAM implements the Stacks and Look-Up Tables required for the different modes of operation, as well as for storing the 1553 messages. A double buffering architecture is available to prevent partially updated information from being transferred to or from the 1553 Bus. A Descriptor Stack is used in both BC and RTU modes. This stack records the status of each message, the time the message was transmitted or received, and contains either the received 1553 command, (in RTU mode), or the actual address of the data block containing the 1553 message (in BC mode). In the RTU mode, a Look-Up Table is implemented to store the address of the data blocks to be used when receiving or transmitting messages for a particular subaddress.

The BUS-65522 may also be used as a passive MT: in this mode all messages transferred across 1553 Bus A or Bus B are captured. The BUS-65522 generates an Identification Word for each word, indicating its sync type (command or data), the 1553 channel it was received on, (A or B), whether it contained an error, (parity, incorrect bit count, etc.) and whether it was preceded by a gap of more than 2.5 μs. If the gap was more than 2.5 μs, the length of the gap, (in 0.5 μs units) using 8 bit resolution is given.

ADDRESSING THE BUS-65522 WITH A MICROPROCESSOR

The BUS-65522 contains DDC's BUS-66312 II to manage its on-board 8K x 16 RAM.

All pointers used by the BUS-66312 are assumed to be word addresses. For example, to begin Descriptor Stack B at location 1000, the user initializes Descriptor Stack Pointer B to word location 0800 (1000 divided by two).

INDICATORS:

Green front panel led indicates that the BUS-65522 offset register has been initialized.

Orange front panel led indicates when the board is active on the MIL-STD-1553 Bus.

Red front panel led indicates when the BUS-65522 has failed the internal self BIT test.

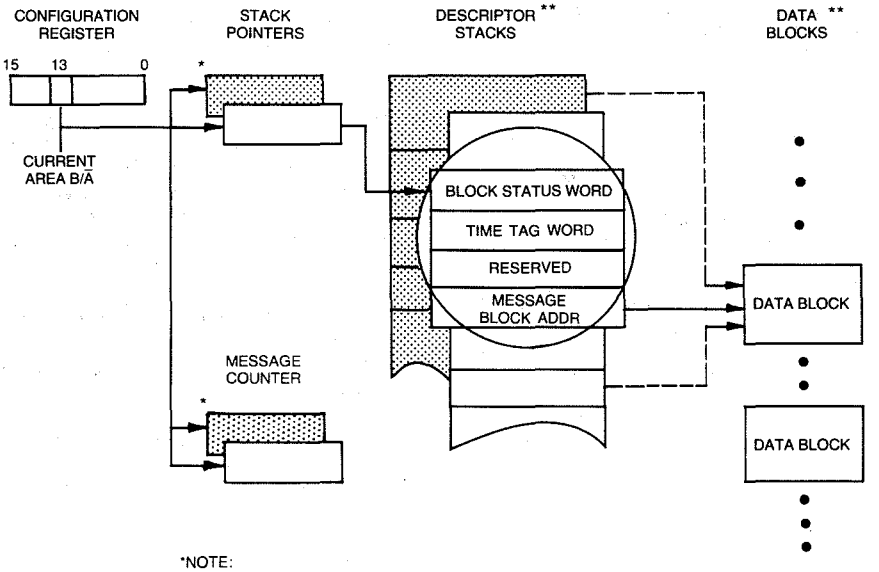
IMPLEMENTATION OF THE DESCRIPTOR STACK

The BUS-65522 uses a Descriptor Stack in BC and RTU modes which may reside anywhere in the non-fixed area of RAM (see figures 2 and 3). The Stack Pointer is 16 bits and resides in a fixed area of RAM. The 8 LSBs of the Stack Pointer are loaded into an internal counter which the BUS-65522 increments by four after each 1553 message has been processed. The results are loaded back into the Stack Pointer location in RAM. Any carry generated by the counter is ignored. As a result, the stack occupies 256 contiguous words of memory, and the 256th word is automatically followed by the first word in the Stack (see figure 4). The 8 MSBs are used as a base address.

The Descriptor Stack is divided into four word descriptor blocks. The first word is the Block Status Word. The second word contains the time tag, and the third is reserved for system use. The contents of the fourth word depend on the operating mode of the BUS-65522. In BC mode it contains the address of the 1553 message. In RTU mode it contains the received 1553 command word. See the description of the particular operating mode for more information.

BLOCK STATUS WORD. The Start-of-Message (SOM) bit is set by the BUS-65522 when it begins processing the message associated with that particular Descriptor Block. The End-of-Message (EOM) bit is set and the SOM reset upon completion of the message. MESSAGE STATUS and ERROR bits are also set at that time. See figure 5 and table 2.

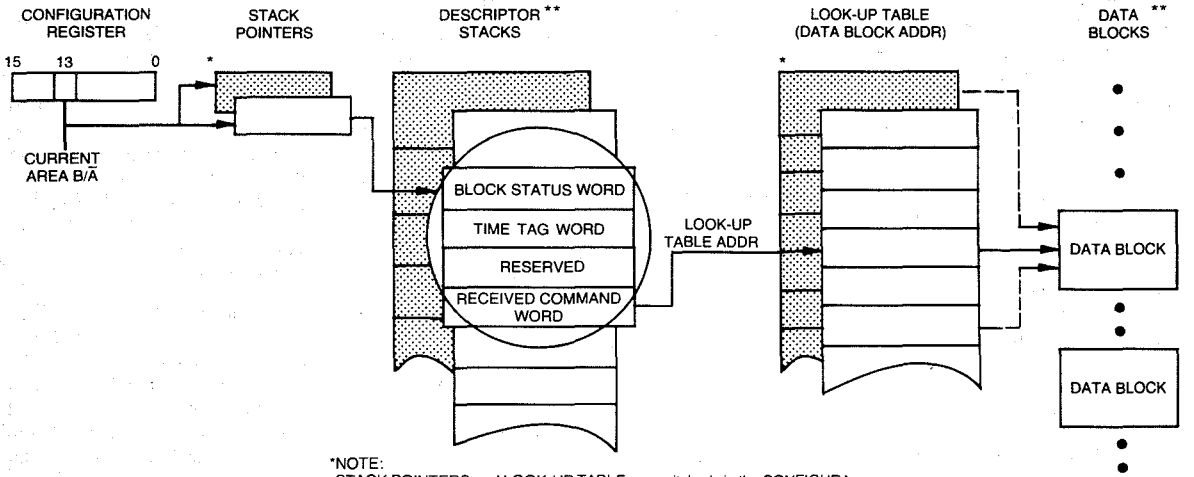
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*NOTE:
STACK POINTERS and MESSAGE COUNTERS are switched via the CONFIGURATION REGISTER under external CPU control.

**NOTE:
DESCRIPTOR STACKS and DATA BLOCKS have 256 word boundaries which should be observed.

FIGURE 2. USE OF DESCRIPTOR STACK – BC MODE

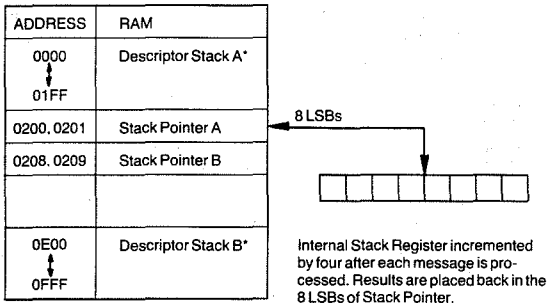


*NOTE:
STACK POINTERS and LOOK-UP TABLE are switched via the CONFIGURATION REGISTER under external CPU control.

**NOTE:
DESCRIPTOR STACKS and DATA BLOCKS have 256 word boundaries which should be observed.

FIGURE 3. USE OF DESCRIPTOR STACK – RTU MODE

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*The address space listed is an example.

FIGURE 4. IMPLEMENTATION OF DESCRIPTOR STACK

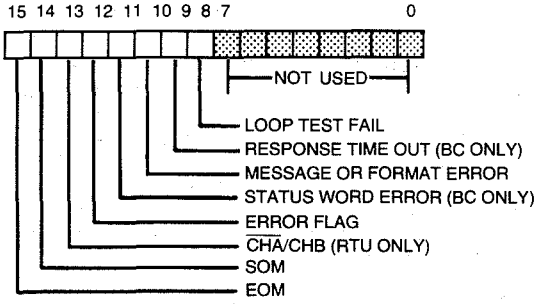


FIGURE 5. BLOCK STATUS WORD

TABLE 2. BLOCK STATUS WORD BIT DEFINITIONS

NAME	DEFINITION
EOM	End Of Message. Set at the completion of a message transfer, regardless of whether or not any errors were detected.
SOM	Start Of Message. Set at the beginning of a message transfer and reset upon completion of the message, regardless of whether or not any errors were detected.
$\overline{\text{CHA}}$/CHB	Channel A/B. Set in RTU mode to indicate whether the message was received on 1553 bus A or B. Set to 0 in BC mode regardless of which bus is used for the message.
ERROR FLAG	Indicates an error was detected during the processing of the particular message. The particular error can be determined by examining bits 0 to 3.
STATUS SET	Set in BC mode to indicate that the received RTU status word had a status bit set or that the wrong RTU responded to the command.
FORMAT ERROR	Set when the MESSAGE ERROR flag is set in the returning RTU's status word or if any word received off the bus violated 1553B specifications (incorrect parity or Manchester sync field, incorrect number of bits, etc.). Also set in RTU mode when the BUS-65522 is acting as the receiving RTU in an RTU-RTU message transfer to indicate that the wrong RTU responded as the transmitting RTU.
RESPONSE TIMEOUT	Set in BC mode if the addressed RTU did not respond within 14 μs of receiving a Transmit command or the last data word in a Receive command. Also set in RTU mode when the BUS-65522 is acting as the receiving RTU in a RT-RT message transfer to indicate that the transmitting RTU did not respond in time.
LOOP TEST FAIL	Set to indicate that the BUS-65522 did not pass its continuous on-line self test.

TIME TAG: In BC and RTU modes the contents of the 1553 Time Tag Counter is loaded into this location at the beginning of each message and updated at the end. Each of the 16 bits represent 1 μs. See 1553 time tag/word counter register description.

ADDRESS MODIFIERS

The address modifiers are programmed in a PAL, with the following response's:

ADDRESS MODE	MODIFIERS
A16	29, 2D
A24	3D, 3E, 39, 3A
A32	0D, 0E, 09, 0A

INTERRUPT PROCESSING

The BUS-65522 generates an interrupt to the processor, upon receiving an interrupt acknowledge from the processor. The board will place the interrupt vector on the data bus and remove the interrupt request. Further interrupts are inhibited until the Status / Control register is read. A 1553 reset mode command or power-on condition will inhibit further interrupts. The interrupts will be enabled after the processor initiates a Status / Control register read command.

INTERRUPT SPECIFICATION

The BUS-65522 generates four types of interrupts. These types can be individually enabled or disabled by the software with the VECTOR/ENABLE/LEVEL REGISTER. The interrupt vector, priority level, and interrupt type enable are loaded into this register. The four interrupt types are:

1553
PROM/WORD COUNT
BIT FAIL
BUFFER FLIP

1553 interrupt-is generated for an error condition or end of message (EOM). The error could occur for either a format error, status bit set or no response as shown in the 1553 section.

PROM/WORD COUNT INTERRUPT-is used in the RT mode by programming a illegalization PROM to meet the system requirement. Parameters monitored by the PROM are subaddress, T/R bit, Word Count and valid messages. In the monitor mode of operation this interrupt is generated whenever the time tag counter crosses the internal memory 256 word boundary, indicating 256 (data & tag) words have been placed in memory.

BIT FAIL. This is generated whenever the internal Wraparound self-test fails.

BUFFER FLIP. This indicates that the requested Buffer Flip (memory swap) has been completed. This flip occurs after the 1553 message activity has ceased. See Figure 8, Bit 8.

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ILLEGALIZING PROM

The BUS-65522 has a socket for a 4K x 4 PROM (U42, PN 27341) that is used in the RT mode to illegalize commands, resetting the time tag counter, generating a custom selected interrupt and a custom selected trigger. The PROM mapping should be setup as follows:

ADDRESS		OUTPUT	
A0	WORD COUNT 0	00	$\overline{\text{ILLEGAL}}$
A1	WORD COUNT 1	01	$\overline{\text{TIME TAG RESET}}$
A2	WORD COUNT 2	02	$\overline{\text{CUSTOM INTERRUPT}}$
A3	WORD COUNT 3	03	NOT USED
A4	WORD COUNT 4		
A5	SUB ADDRESS 0		
A6	SUB ADDRESS 1		
A7	SUB ADDRESS 2		
A8	SUB ADDRESS 3		
A9	SUB ADDRESS 4		
A10	T/$\overline{\text{R}}$		
A11	$\overline{\text{BROADCAST}}$		

NOTES:
Maximum access time (address to data valid) is 250ns.

For further information refer to User's Manual.

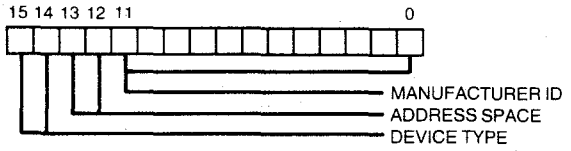
BUS-65522 Register Specification

TABLE 3. BUS-65522 REGISTERS

WORD ADDRESS	BYTE	ADDRESS	DESCRIPTION
00	00	01	IDENTIFICATION
02	02	03	DEVICE TYPE
04	04	05	STATUS / CONTROL
06	06	07	OFFSET (BASE ADDRESS OF RAM)
08	08	09	VECTOR / ENABLE / LEVEL
0A	0A	0B	DEVICE TYPE EXTENSION
0C	X	0D	1553 RT ADDRESS
0E	0E	0F	1553 BC-RT TIME TAG / MT WORD COUNT
10	X	11	1553 INTERRUPT SELECT
12	12	X	1553 CONFIGURATION
14	X	X	1553 NOT USED
16	X	17	1553 START / RESET

DEFINITIONS:

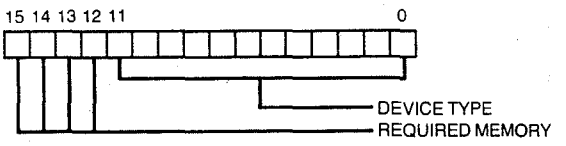
IDENTIFICATION REGISTER. A 16 bit read only register used to convey the device class, address space and manufacturer identification per VXI requirement. The bit definitions:



NAME	DEFINITION
DEVICE TYPE	"11" = Register
ADDRESS SPACE	00 (TB3 open A16/A24 mode selected) 01 (TB3 closed A16/A32 mode selected)
MANUFACTURER ID	1111 1110 1000 (HEX FE8) = DDC'S

FIGURE 6. IDENTIFICATION REGISTER

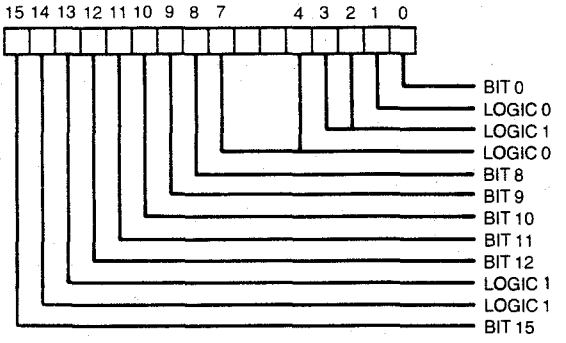
DEVICE TYPE REGISTER. A 16 bit read only register used to convey the required memory and device type per VXI requirement. The bit definitions:



NAME	DEFINITION
REQUIRED MEMORY	1001 (TB3 open A16/A24 mode selected) 1111 (TB3 closed A16/A32 mode selected)
DEVICE TYPE	0110 0101 0000 (HEX 620) = BUS-65522 0110 0011 0000 (HEX 630) = BUS-65523

FIGURE 7. DEVICE TYPE REGISTER

STATUS / CONTROL REGISTER. A 16 bit register. Bit 15 is a read/write bit that defines the status of the offset register. When this bit is a "1" the software has previously initialized the offset register and memory read/write are allowed. When this bit is reset, memory read/writes are not executed and the $\overline{\text{DTACK}}$ is not returned to the CPU. Bits 14 to 1 are read only status bits and contain the parity check on the selected RT address and the interrupts status. Bit 0 is write only reset bit equivalent to a power on reset. The bit definitions:



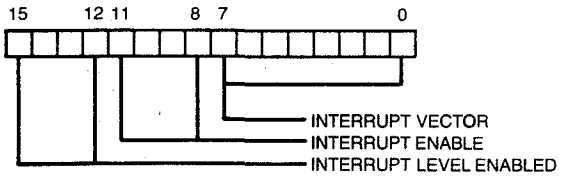
NAME	DEFINITION
BIT 15	RAM ENABLE Enables access to RAM. Writing a "1" enables access to RAM. this bit is reset upon power up or with bit 0 of the STATUS/CONTROL.
BIT 12	1553 address has odd parity
BIT 11	1553 interrupt
BIT 10	Custom interrupt
BIT 9	Loop error interrupt
BIT 8	Buffer flip interrupt
BIT 0	Don't care read. A write "1" causes a reset, same as power on reset of board.

FIGURE 8. STATUS/CONTROL REGISTER

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OFFSET REGISTER. This is a 16 bit read/write register which defines the on board memory base address. In the A16/23 mode the upper 8 bits of the register are not used. Bits 15-0 equals the memory base address. Note: User must set Bit 15 to a logic "1" to access RAM.

VECTOR/ENABLE/LEVEL REGISTER. This is a 16 bit read/write register which defines the value of the interrupt vector, enable/disables the four interrupts and defines the interrupt priority level to 4, 5, 6, and 7. The bits are defined as:



NAME	DEFINITION
INTERRUPT LEVEL ENABLE	Bit 15 = "1" level 7 enabled Bit 14 = "1" level 6 enabled Bit 13 = "1" level 5 enabled Bit 12 = "1" level 4 enabled
INTERRUPT ENABLE	Bit 11 = "1" enables 1553 interrupt Bit 10 = "1" enables custom interrupt Bit 9 = "1" enables BIT interrupt Bit 8 = "1" enables buffer flip interrupt
INTERRUPT VECTOR	Bit 7 = MSB (user defined) Bit 0 = LSB

FIGURE 9. VECTOR/ENABLE/LEVEL REGISTER

DEVICE TYPE EXTENSION REGISTER. This is a 16 bit read only register that completes the device type model code. For a standard BUS-65522/23 this register is defined to be (hex 0000) 0000 0000 0000 0000. For earlier SN's the register will read:

BUS-65522 = 0010 0010 0000 0000 (HEX2200)
BUS-65523 = 0010 0011 0000 0000 (HEX2300)

1553 TIME TAG / WORD COUNT REGISTER. This 16 bit read/write register is used in two different modes. In the BC or RT mode it performs as a time tag counter, that is incremented every microsecond. In the MT mode it is a word counter that increments every time a 1553 word and its identification words are placed in memory. (i.e., Every time a word pair occurs the register increments 1.)

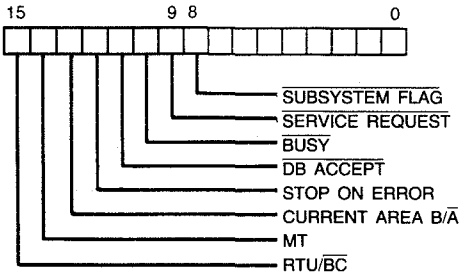
The time tag counter is reset by any of the following:

1. Write operation clears register.
2. Power on reset
3. Status control reset
4. 1553 reset, (start/reset register)
5. As programmed in the RT illegalization PROM in the RT mode of operation. ex: mode code reset.

The time tag/word counter register bit definition is as follows:

Bit 15-0
- Time tag (RT/BC) mode
  LSB = 1 microsecond
- Word count (MT) mode
  LSB = 2 words in memory (data & tag word).

1553 CONFIGURATION REGISTER. An 8 bit read/write register. The four MSB's define the mode of operation; the four LSB's control the RT status bits in the 1553 status word. Activating the $\overline{\text{SUBSYSTEM FLAG}}$, $\overline{\text{SERVICE REQUEST}}$, $\overline{\text{BUSY}}$, and $\overline{\text{DB ACCEPT}}$ bits to logic "0" causes the BUS-65522 to set these bits in the 1553 status word. If $\overline{\text{BUSY}}$ is set, the status word only will be transmitted upon receipt of a transmit command, but data associated with a receive command will be placed in the RAM, see figure 10. The bits are defined as follows:



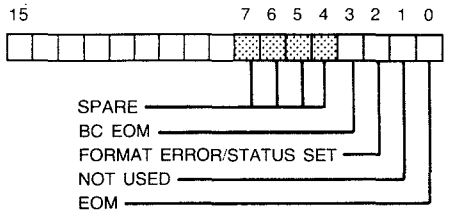
NAME	DEFINITION		
$\overline{\text{SUBSYSTEM FLAG}}$	1553 Status Word bit.		
$\overline{\text{SERVICE REQUEST}}$	1553 Status Word bit.		
$\overline{\text{BUSY}}$	1553 Status Word bit.		
$\overline{\text{DB ACCEPT}}$	1553 Status Word bit.		
STOP ON ERROR	Causes BC to stop at end of current data block if an error is detected.		
CURRENT AREA B/$\overline{\text{A}}$	Used for Double Buffering; see description.		
RTU/$\overline{\text{BC}}$, MT	Operating Mode	Bit 15	Bit 14
	BC	0	0
	MT	0	1
	RTU	1	0
	ILLEGAL	1	1
Note: A "0" in bits 9-11 activates the corresponding bit in the 1553 Status Word.			

FIGURE 10. 1553 CONFIGURATION REGISTER

1553 INTERRUPT SELECT REGISTER. An 8 bit read/write register used to enable interrupt conditions. All interrupts are enabled with a logic "1". In the BC and RT modes the BUS-65522 generates an IRQ (interrupt request) for an EOM or error set condition. An IRQ is generated in the BC mode for a BC EOM indicating that all requested transfers by the BC are completed. Refer to the VECTOR/ENABLE/LEVEL REGISTER for setting

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the interrupt priority level, see figure 9. The bits are defined as follows:

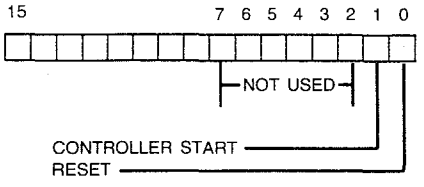


NOTE:
Spare Bits 4-7 = CPU can read or write.

INTERRUPT	DEFINITION
EOM	End of message. Set by BUS-66300 II (during BC or RTU mode) every time a 1553 message is transferred (regardless of validity).
FORMAT ERROR/ STATUS SET	Set by BUS-66300 II for these conditions: **Loop Test Failure:** Last transmitted word did not match received word. **Message Error:** Received message contained an address error, one of eight 1553 status bits set, or 1553 specification violated (parity error, Manchester error, etc.). **Time-Out:** Expected transmission was not received during allotted time. **Status Set:** Received status word contained status bit(s) set or address error.
BC EOM	Bus Controller End of Message. Set by BUS-66300 II (in BC mode) when all messages have been transferred.

FIGURE 11. 1553 INTERRUPT SELECT REGISTER

1553 START/RESET REGISTER. A write only two bit register used to enable or reset the terminal, see figure 12. The bits are defined as:

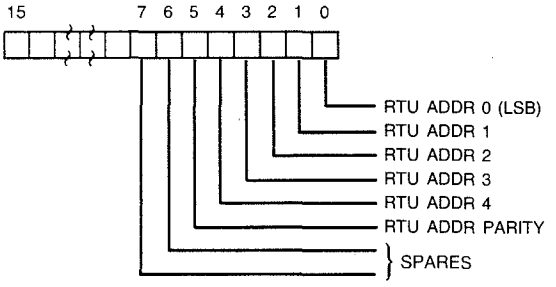


Bits 2-15 Don't Care

NAME	DEFINITION
RESET	Places BUS-65522 in the power-up condition; Configuration, Start/Reset Register, and Interrupt Mask registers are reset to "0". Does not affect RTU Address Register or the contents of RAM. It is recommended that this command be issued prior to changing the operating mode (RT-BC, BC-MT, etc.).
CONTROLLER START	Used in BC mode to begin transmission of the designated number of messages. The message count must have been previously loaded into the current area message count, using 1's complement notation. Also used in MT mode to begin reception of 1553 message traffic. (Yellow LED = in use.)

FIGURE 12. 1553 START/RESET REGISTER

1553 RT ADDRESS REGISTER. An internal 8 bit read/write register used to set the RT address and to enable the BUS-65522 to receive information transferred over the 1553 bus, see figure 13. The bit definitions are as follows:



NAME	DEFINITION
RTU ADDR PARITY	Odd parity bit associated with five RTU address bits. BUS-65522 will not respond to 1553 commands if the parity is incorrectly set. Set to a logic "1" if RTU Address is 0, 3, 5, or 6.
RTU ADDR 0-4	RTU address bits.

FIGURE 13. 1553 RTU ADDRESS REGISTER

BC MODE

The BC mode is selected by setting the two MSBs of the Configuration Register to logic "0". The BUS-65522 defaults to BC mode upon power up and after receipt of a Reset signal from the CPU.

BC INITIALIZATION. For BC operation, the user initializes the RAM, Stack Pointers, Descriptor Stack Entries, and Message Blocks. See table 4 for a sample memory map and follow the steps in figure 14 (A), (B), and (C).

The BUS-65522 uses an indirect addressing architecture to determine which messages to send over the 1553 bus. The Stack Pointer indicates which entry in the Descriptor Stack to use, while the fourth word in the Descriptor Block indicates the location of the 1553 message (see figure 2).

Two Stack Pointers and two Descriptor Stacks are provided to allow the user to double buffer the RAM. All transfers to/from the 1553 bus are made using the "current" Descriptor Stack and Stack Pointer, as defined by the user through bit 13 of the Configuration Register.

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The Descriptor Stack in BC mode occupies 256 contiguous words. It may be located anywhere in the non-fixed area of RAM as long as it begins on a 256 word boundary (i. e., HEX 0000, 0700, 1000, XX00, etc.). Each Descriptor Block is four words long; the fourth word of each block is loaded by the user with the address of the message to be transferred onto the 1553 bus.

Each data block should be formatted as shown in figure15. The first word of the message is the Control Word (see figure 16). The BUS-65522 uses an 8 bit counter for the lower byte of the internal Address Counter. As a result, the data block may be stored anywhere in the non-fixed area of RAM, so long as the individual data block does not cross a 256 word boundary. For example, a data block should not begin at word location 04FE if the user plans on storing more than two words in the block. The first word will be stored at 04FE, the second at 04FF, and a third word would be stored at 0400 as a result of the lower byte Address Counter overflowing.

The number of messages to be transferred must be stored in the current area Message Counter location of the RAM in 1's complement (XXFE = 1 message). The user instructs the BUS-65522 to begin transferring the messages by setting bit 1 of the Start/Reset Register to logic "1". The BUS-65522 will then begin transferring the messages in the order in which their starting addresses were placed in the Descriptor Stack (see figure17).

The BUS-65522 can be instructed to end 1553 bus transactions if any message does not transfer successfully. This is done by setting the STOP-ON-ERROR bit in the Configuration Register. An ERROR interrupt will be generated at that time if enabled by the user.

If desired, a BCEOM interrupt can be generated to notify the CPU that the BUS-65522 has completed the transfer of the requested number of messages. The CPU can also request that an EOM interrupt be generated upon completion of each individual message.

While the current group of messages is being processed, the CPU may read or write to the non-current area of RAM in order to set up the next group of messages, or to examine the results of the previous bus transfers.

Once a block of messages has been completed, the user may swap the current and non-current areas and instruct the BUS-65522 to execute the next group of messages. This is done by toggling bit 13 of the Configuration Register and issuing a new BCSTART command.

BC SOM SEQUENCE. After setting the CONTROLLER START bit in the Start/Reset Register, the BUS-65522 takes the following actions:

1. Uses Stack Pointer to get the address of the current Descriptor Stack Entry.
2. Sets SOM flag in the Block Status Word to indicate a transfer operation in progress.
3. Stores the Time Tag.
4. Reads the Data Block Address from the fourth location of the Descriptor Stack and transfers the Data Block Address into an internal Address Register.
5. Begins transmission of the message onto the 1553 bus.

Note that data words are transferred to and from memory using the internal Address Register.

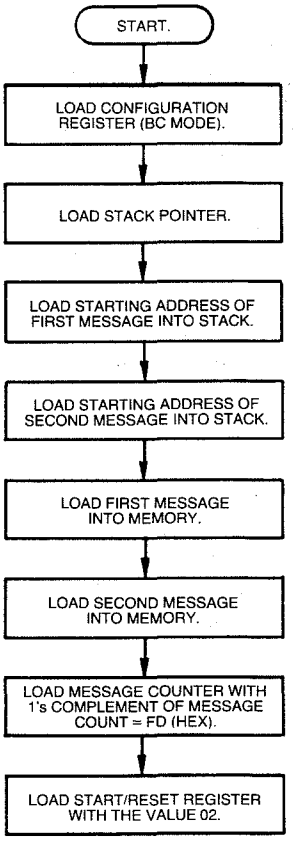


FIGURE 14A.
BC SET-UP EXAMPLE FOR
TWO MESSAGE TRANSFER

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BC EOM SEQUENCE. Upon completion of a 1553 message, the BUS-65522 takes the following action:

1. Reads the Stack Pointer to get the address of the current Descriptor Stack Entry.
2. Updates the Block Status Word by resetting the SOM and setting EOM and any error bits.
3. Updates the Time Tag.
4. Increments the contents of the Stack Pointer by four and increments the Message Counter by one.
5. Additional messages are transmitted.
6. Generates a BCEOM interrupt if enabled and no further messages are to be transmitted.

Note that if an error is received and STOP ON ERROR is set, the BUS-65522 stops issuing commands over the 1553 bus. The Stack Pointer will point to the next message to be transmitted.

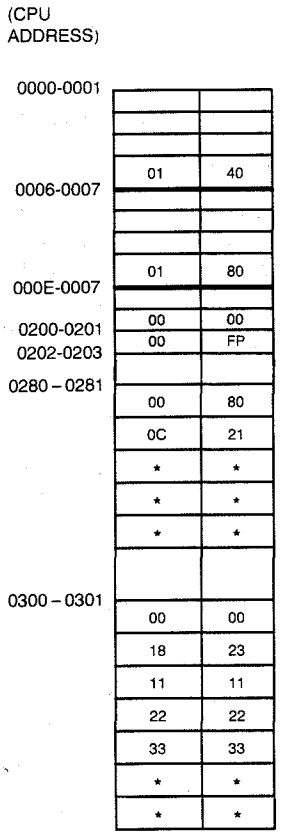
GIVEN:

All values are in HEX.

1. Stack area A is used and is located from address 0000 to address 01FF.
2. Message number 1 is located at address 0280.
3. Message number 2 is located at address 0300.

BYTE ADDRESS		CONTENTS
—12	Initialize Configuration Register.	
0200	Initialize Stack Pointer.	WORD 0000
0006	Load address of message number 1 into Stack.	WORD 0140
000E	Load address of message number 2 into Stack.	WORD 0180
0280	Load Control Word.	WORD 0080
0282	Load Command.	WORD 0C21
0300	Load Control Word.	WORD 0000
0302	Load Command.	WORD 1823
0304	Load Data Word number 1.	WORD 1111
0306	Load Data Word number 2.	WORD 2222
0308	Load Data Word number 3.	WORD 3333
0202	Load Message Counter.	WORD 00FD
—17	Start Transfer.	BYTE 02

FIGURE 14B. BC SET-UP WRITTEN IN BASIC



*Left empty for RTU's response & LOOP WORD.

FIGURE 14C.
BC SET-UP MEMORY MAP

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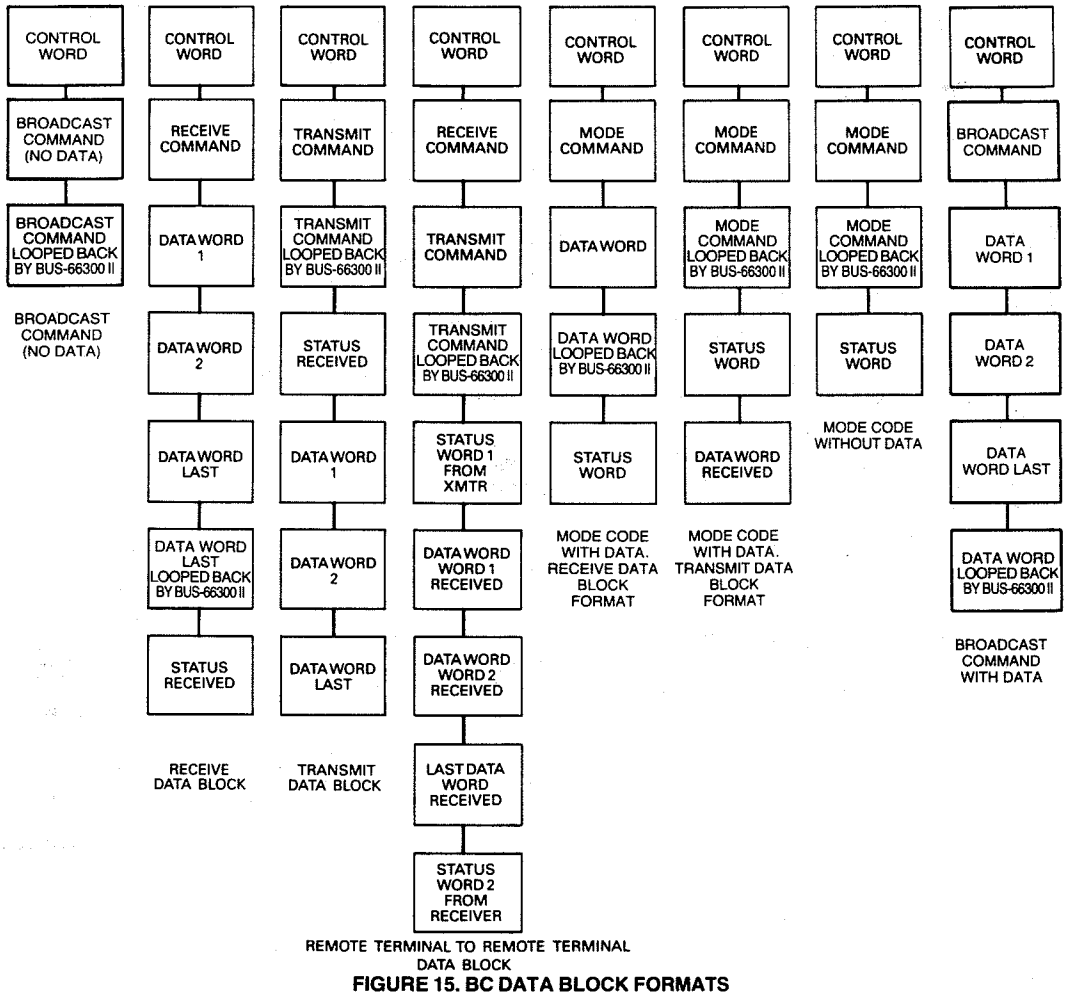
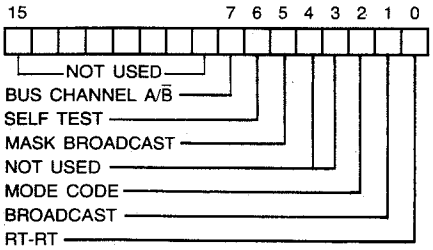


FIGURE 15. BC DATA BLOCK FORMATS



Note:
1. MASK BROADCAST XOR BROADCAST BIT in Status Word = STATUS SET ERROR.
2. When the BC expects the BROADCAST bit set in the Status Word, a logic 1 will mask the Status Interrupt Error flag.

FIGURE 16. BC CONTROL WORD

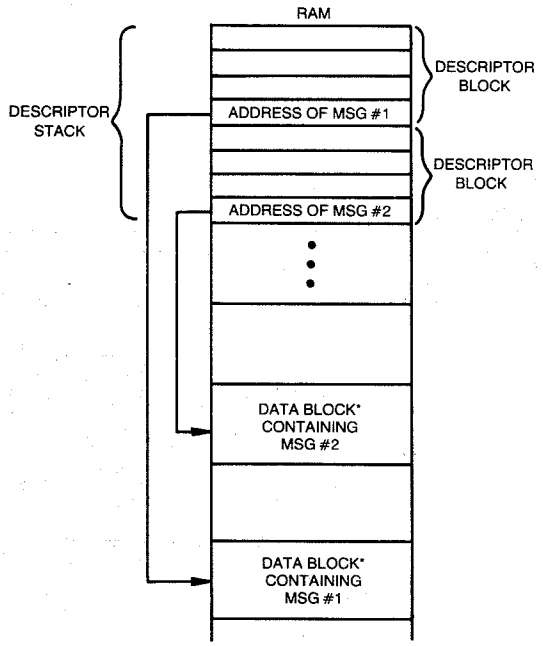
BIT NAME	DEFINITION
BUS CHANNEL A/B̄	Determines whether the message will be transmitted on 1553 Bus A or Bus B. Logic 1 = A, logic 0 = B.
INITIATE OFF-LINE SELF TEST	Logic 1 performs internal off-line transmit/receive test. The last word of the message is looped back through the decoder and placed in RAM. See Self Test paragraph.
MASK BROADCAST (1)	When logic 1, prevents Broadcast RCVD bit of the 1553 Status Word response from signalling a status error as a result of a Broadcast command. (A FORMAT error will be generated if the BROADCAST bit is not set on the RTU's Status Word.)
MODE CODE	When logic 1, the message is treated as a Mode Code. (The Command Word – Word Count field indicates Mode Code type.)
BROADCAST	When logic 1, indicates that the message is a Broadcast Command. (No Status Word is expected.)
RT-RT	When logic 1, the message is treated as an RT-RT transfer. (The next two words are Command Words.) Both Status Word responses are validated.

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TABLE 4. TYPICAL RAM ALLOCATION IN BC MODE

ADDRESS	USE	DESCRIPTION
0000-0001 • • 01FE-01FF	Descriptor Stack A	256 Words
0200-0201 0202-0203 0204-0205 0206-0207 0208-0209 020A-020B 020C-020D 020E-020F	Stack Pointer A Message Counter A* Reserved Reserved Stack Pointer B Message Counter B* Reserved Reserved	Fixed Area of RAM
0210-0211 • 027E-027F		Not used in this example.
0280-0281 0300-0301 0380-0381 0400-0401 0480-0481 • • • 1D80-1D81	Data Block 1 Data Block 2 Data Block 3 Data Block 4 Data Block 5 Data Block 55	64 Words each in this example.
3E00-3E01 • 3FFE-3FFF	Descriptor Stack B	256 Words

*Message Counters A and B are one byte each.



*DATA BLOCKS NEED NOT BE CONTINUOUS AND MAY BE OF WHATEVER LENGTH IS SUFFICIENT TO HOLD THE PARTICULAR MESSAGE

FIGURE 17. ORDERING MESSAGES IN BC MODE

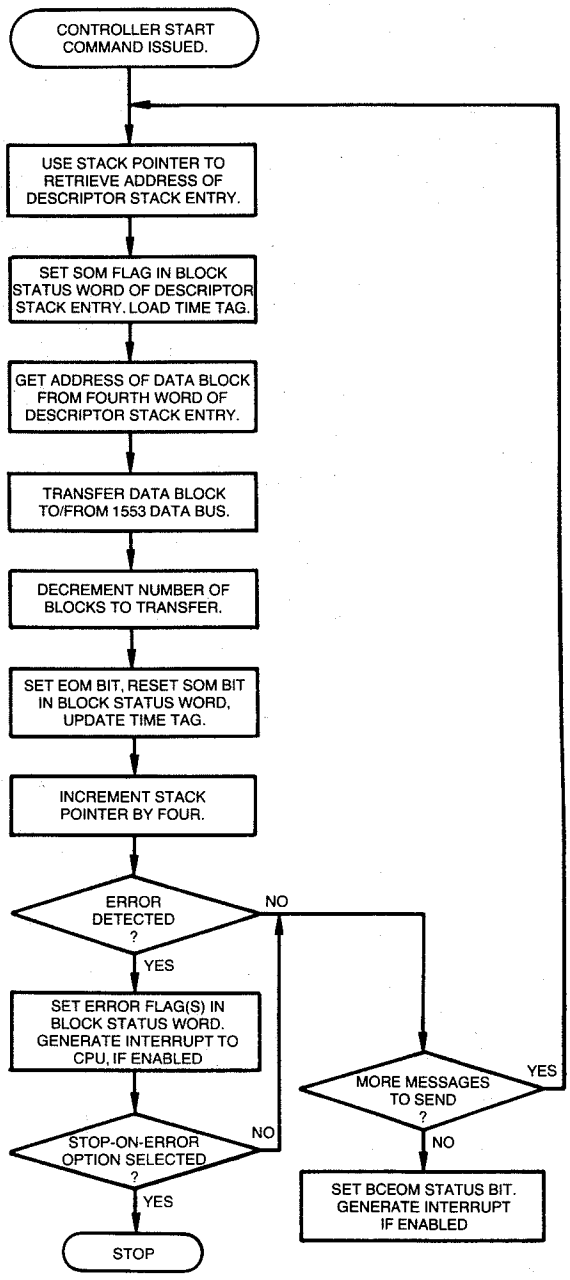


FIGURE 18. BC SEQUENCE OF OPERATION (UNDER BUS-65522 CONTROL)

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RTU MODE

The RTU mode is selected by issuing a RESET command and setting bits 15 and 14 of the 1553 Configuration Register to logic "1" and "0", respectively. The RTU Address of the BUS-65522 is defined by loading the desired value into the RTU Address Register. Note that bit 5 of the RTU Address Register must be programmed to implement odd parity.

RTU INITIALIZATION. For RTU operation, the user initializes the RAM, Stack Pointer, Look-Up Tables, and data to be transmitted to the BC. Table 5 lists a sample memory map for the RTU mode. The user follows the steps shown in Figure 19, RTU Initialization.

The BUS-65522 uses an indirect addressing architecture to determine where to store or retrieve the data required to service the commands received from the BC. The Stack Pointer indicates which block in the Descriptor Stack to use. The fourth word of the Descriptor Stack is used to store the received command word.

The T/$\overline{R}$ bit and the subaddress field of the command word will then be used to generate a pointer into the Look-Up Table, which contains the starting address of the data block to be used for transmitting or receiving information for the particular subaddress.

Two Stack Pointers, two Descriptor Stacks, and two Look-Up Tables are provided to allow the user to double buffer the RAM. All transfers to and from the 1553 Bus are made using the current Stack and Look-Up Tables as defined by the user through bit 13 of the Configuration Register.

The Stack Pointer should be initialized by the CPU with the starting address of the Descriptor Stack. This pointer must contain a word address (i.e., if the Stack is to begin at HEX (0400), the Stack Pointer should be initialized to 0200).

In the RTU mode, the Descriptor Stack occupies 256 contiguous words. It may be located anywhere in the non-fixed area of RAM, beginning a 256 word boundary (i.e., HEX 0000, 0700, 1000, XX00, etc.).

The Look-Up Table is loaded by the user with the addresses of the data blocks to be used for receiving or transmitting data from the particular subaddress. The first 32 words of each Look-Up Table should contain the word address of the data blocks to be used when receiving data. The next 32 words should contain the address to be used when transmitting data from the various subaddresses.

The Look-Up Table is sequentially ordered so that the first location refers to T/$\overline{R}$ = 0, Subaddress = 00000. The second location refers to T/$\overline{R}$ = 0 and Subaddress = 00001. The last location within the Look-Up Table refers to T/$\overline{R}$ = 1 and Subaddress = 11111 (see figures 20 and 21).

RTU SOM SEQUENCE. When a 1553 command is received, the BUS-65522 saves the command received in an internal register. Figure 22 illustrates the RTU Sequence of Operation once a 1553 command word is received. Once the command word is received, the BUS-65522 performs the following steps:

1. Reads the Stack Pointer to get the address of the current Descriptor Stack Entry.
2. Stores an SOM flag in the Block Status Word to indicate a transfer operation in progress.
3. Stores the Time Tag.
4. Stores the Command Word received.
5. Reads a Block address from the Look-Up Table using the T/$\overline{R}$ bit and the subaddress from the Command Word; transfers the Block address into an internal address register.

RTU EOM SEQUENCE. At the end of a 1553 message (valid or invalid), the BUS-65522 performs the following steps:

1. Updates the Block Status Word by resetting the SOM and setting the EOM and any error bits.
2. Updates the Time Tag.
3. Increments the Stack Pointer by four.
4. Generates an Interrupt if enabled.

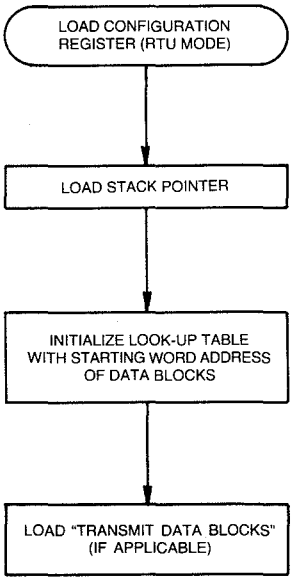


FIGURE 19. RTU INITIALIZATION (UNDER USER CONTROL)

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TABLE 5. TYPICAL RAM ALLOCATION IN RTU MODE

WORD ADDRESS	USE	DESCRIPTION
0000-0001 • • 01FE-01FF	Descriptor Stack A	256 Words
0200-0201 0202-0203 0204-0205 0206-0207 0208-0209 020A-020B 020C-020D 020E-020F	Stack Pointer A Reserved Reserved Reserved Stack Pointer B Reserved Reserved Reserved	Fixed Area of RAM
0210-0211 • 027E-027F		Unused in this example.
0280-0281 • • 02FE-02FF	Look-Up Table A	Fixed Area of RAM

TABLE 5. TYPICAL RAM ALLOCATION IN RTU MODE (Cont'd)

WORD ADDRESS	USE	DESCRIPTION
0300-0301 03FE-033F 0340-0341 037E-037F	Data Block 1 Data Block 2	32 Words in this example.
0380-0381 • • 03FE-03FF	Look-Up Table B	Fixed Area of RAM
0400-0401 • • • 1EC0-1EC1 1EE0-1EEF	Data Block 3 • • • Data Block 97	
2F00-2F01 • • 2FFE-2FFF	Descriptor Stack B	256 Words

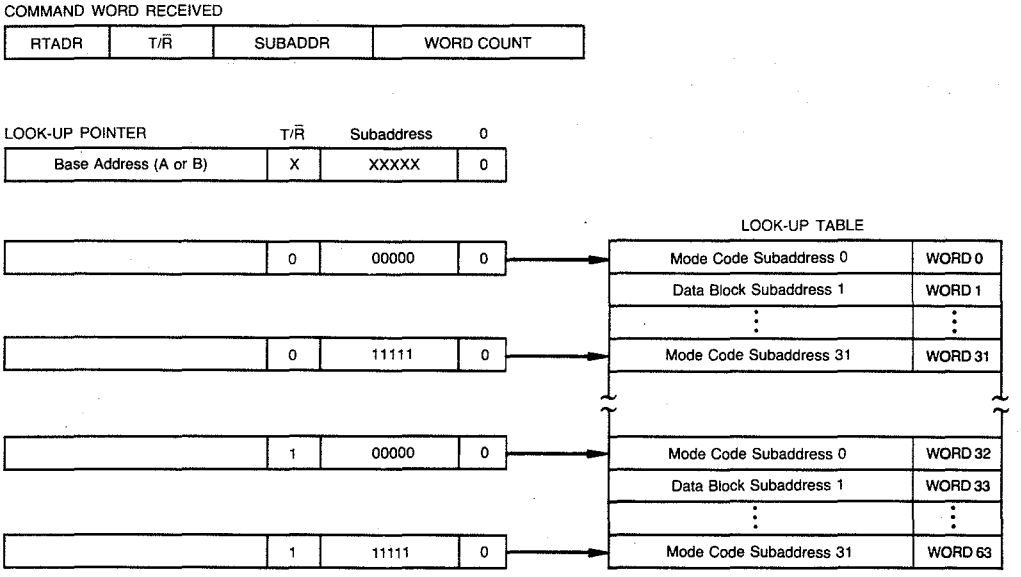


FIGURE 20. LOOK-UP TABLE SET-UP

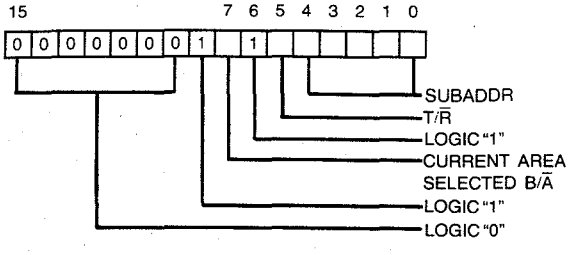


FIGURE 21. LOOK-UP TABLE POINTER

MT MODE

The MT mode is selected by setting bit 15 of the Configuration Register to logic "0" and bit 14 to a logic "1".

MT INITIALIZATION. For MT operation, the user initializes the RAM as shown in table 6 and follows the steps shown in figure 23, MT Initialization.

The entire RAM is used as the MT stack. The user instructs the BUS-65522 where to store the first Identification Word by loading the starting word address in word 100 HEX of RAM.

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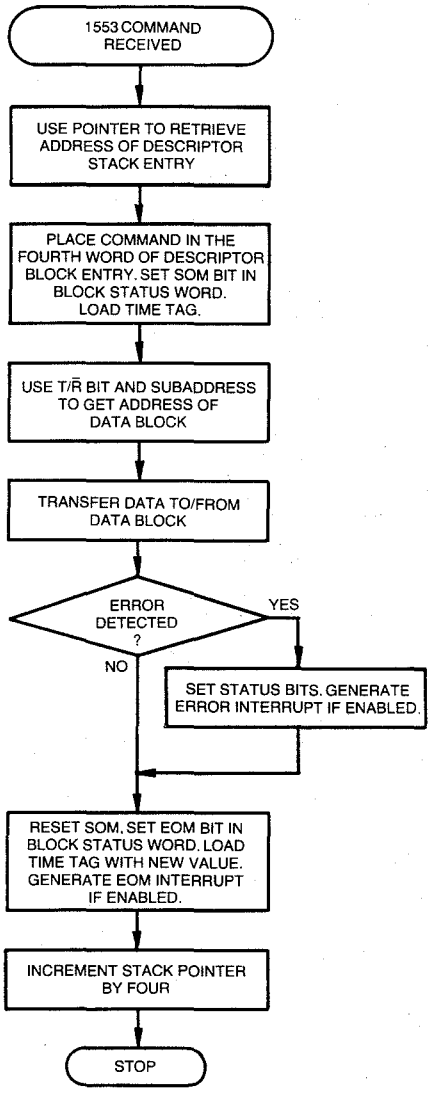


FIGURE 22. RTU SEQUENCE OF OPERATION (UNDER BUS-65522 CONTROL)

To initiate reception of the 1553 bus traffic, the user issues a CONTROLLER START command by setting bit 1 of the Start/Reset Register to a logic "1". This causes the BUS-65522 to load the contents of either Stack Pointer A or B (as selected by the Configuration Register) into an internal address register. Once a word is received from the 1553 bus, the BUS-65522 stores this word at the address indicated by the internal address register. The contents of this register are then incremented by two to point to the next word in RAM.

The BUS-65522 generates an Identification Word for the received word and stores it in the RAM location indicated by the internal address register. The Address Register is again incremented, in preparation for storing the next 1553 word. The RAM automatically wraps around from 2FFE-2FFF.

The Identification Word is generated by the BUS-65522 in order to provide the CPU with additional information regarding the received 1553 word (see figure 24).

The CPU can read the 1553 time tag/word count register to determine the number of data words and identification words received.

TABLE 6. TYPICAL RAM ALLOCATION IN MT MODE

WORD ADDRESS	DESCRIPTION
0000-0001	First Received 1553 Word
0002-0003	First Identification
0004-0005	Second Received Word
0006-0007	Second Identification
•	
•	
3FFE-3FFF	Word stored at 3FFE-3FFF followed by word stored at 0000.
•	
•	
•	
0200-0201	Stack Pointer* A (Fixed area of RAM)
0208-0209	Stack Pointer* B (Fixed area of RAM)

*Stack Pointers are read by the BUS-65522 upon executing a BCSTART command. It is overwritten by data in the course of acting as a MT.

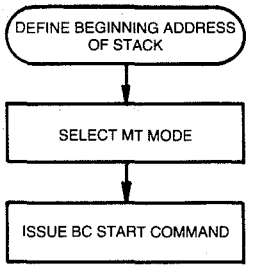
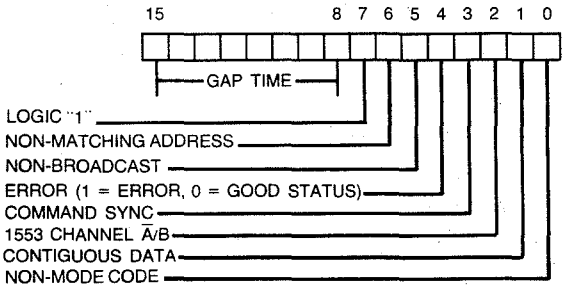


FIGURE 23. MT INITIALIZATION (UNDER USER CONTROL)



Note: Each bit of the GAP TIME field represents 0.5 μs.

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NAME	DEFINITIONS
BIT 0	Non-Mode Code – Set to logic 1 if preceding 1553 word was a valid word, contained a command sync, and the subaddress field was any value other than 00000 or 11111. Set to '0' otherwise.
BIT 1	Contiguous Data – Logic "1" indicates that data received is contiguous and therefore associated with a message being received. Logic "0" = gap.
BIT 2	1553 Channel $\overline{A}$/B – indicates which Bus the data was received on.
BIT 3	Command Sync – this will differentiate data from that of Command/Status sync types. Logic "1" = Command Sync.; "0" = Data Sync.
BIT 4	ERROR – this bit will be a logic 1 for an Error or 0 for a valid word received.
BIT 5	Non-Broadcast – Set to logic '1' if associated 1553 word was a valid word, contained a command sync, and the 5 MSB's (the RTU address) was any value other than 11111. Set to '0' otherwise.
BIT 6	$\overline{\text{THIS RT}}$ – Set to a logic '0' if the associated 1553 word was a valid word, received with a command sync and the 5 MSB's (the RTU address) match the RTU address defined for the device.
BIT 7	logic '1'
BIT 8-15	Gap time – Bit 15 (MSB) indicates the amount of gap time should Bit 1 indicate non contiguous data. Resolution is 0.5μs per LSB.

FIGURE 24. MT IDENTIFICATION WORD

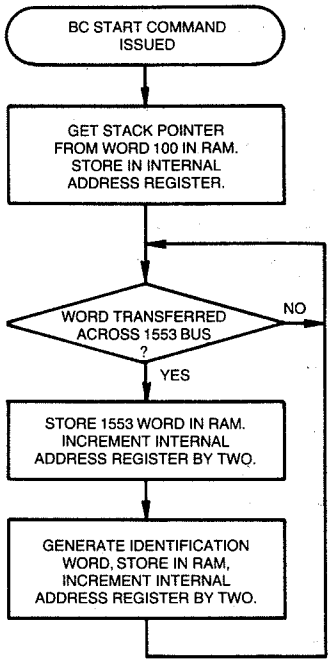


FIGURE 25. MT SEQUENCE OF OPERATION (UNDER BUS-65522 CONTROL)

MODE CODES

The BUS-65522 supports all 1553B mode codes for dual redundant systems. Note that a Reset mode code command does not have the same effect as issuing a RESET command (setting bit 1 of the Start/Reset Register). A mode code Reset command will override the Inhibit TF Flag, override the Transmitter Shutdown condition, and reset the Time Tag Register if instructed to do so through the user programmable PROM.

A mode code with an associated data word and a T/$\overline{R}$ bit set to "0" is handled the same as a receive operation. In the RTU mode, the T/$\overline{R}$ bit and the subaddress field are used as pointers into the Look-Up Table. Thus, the 1st and 31st entries of the Look-Up Table should contain the address of the word in RAM to be used for receiving data associated with the Synchronize with Data mode code command. Note that these entries correspond to a T/$\overline{R}$ bit equal to "0" and a subaddress field of 00000 or 11111.

The mode code command Transmit Vector word is handled in a similar manner. Look-Up Table entries 32 and 63 (T/$\overline{R}$ bit = 1 and a subaddress field of 00000 or 11111) should point to the location in RAM containing the user defined Vector Word.

The BUS-65522 maintains separate registers containing the last received Command Word and Status Word, along with the BIT Word. It will automatically transmit these words to the BC when it receives a mode code command instructing it to do so.

The BUS-65522 responds to reserved or illegalized mode code commands if implemented by setting the Message Error bit in its 1553 Status Word. If the command had been issued as a non-broadcast command, the Status Word will be transmitted to the BC. For a complete description of the BUS-65522's response to various mode code commands, see tables 7 and 8.

TABLE 7. MODE CODE FUNCTIONS

T/R BIT	MODE CODE	FUNCTION	DATA WORD	BROAD-CAST
1	00000	Dynamic Bus Control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	Yes
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag	No	Yes
1	00111	Override Inhibit Terminal Flag	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	10000	Transmit Vector Word	From Memory	No
0	10001	Synchronize with Data	To Memory	Yes
1	10010	Transmit Last Command	From Internal Register	No
1	10011	Transmit Bit Word	From Internal Register	No

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TABLE 8. MODE CODES

DYNAMIC BUS CONTROL (00000)

MESSAGE SEQUENCE = DBC ⋆ STATUS

The BUS-65522 responds with status. If the subsystem wants control of the bus, it must set DBACC within 2.5μs after $\overline{\text{NBGRT}}$.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, *T/R Error (BIT Word).*
5. ***Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

SYNCHRONIZE WITHOUT DATA WORD (00001)

MESSAGE SEQUENCE = SYNC ⋆ STATUS

The BUS-65522 responds with status. If sent as a broadcast, the broadcast receive bit will be set and status response suppressed.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, *T/R Error (BIT Word).*

TRANSMIT STATUS WORD (00010)

MESSAGE SEQUENCE = TRANSMIT STATUS ⋆ STATUS

The status and BIT word registers are not altered by this command and contain the resulting status from the previous command.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, *T/R Error (BIT Word).*
5. ***Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

INITIATE SELF-TEST (00011)

MESSAGE SEQUENCE = SELF-TEST ⋆ STATUS

The BUS-65522 responds with a status word. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Short-loop test is initiated on the status word transmitted. If the test fails, an RT fail flag is generated.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).
5. ***Faulty Test.*** Bits set: terminal flag (SW), A/$\overline{B}$ Loop Test Fail, Current 1553 Bus (A or B) Loop Test Fail (BIT Word).

TRANSMITTER SHUTDOWN (00100)

MESSAGE SEQUENCE = SHUTDOWN ⋆ STATUS

This command is only used with dual redundant bus systems. The BUS-65522 responds with status. At the end of the status transmission, the BUS-65522 inhibits any further transmission from the dual redundant channel. Once shutdown, the transmitter can only be reactivated by Override Transmitter Shutdown or RESET RT commands.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, *T/R Error (BIT Word).*

⋆ = Status response time

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TABLE 8. MODE CODES (CONT'D)

OVERRIDE TRANSMITTER SHUTDOWN (00101)

MESSAGE SEQUENCE = OVERRIDE SHUTDOWN ⋆ STATUS

This command is only used with dual redundant bus systems. The BUS-65522 responds with status. At the end of the status transmission, the BUS-65522 re-enables the transmitter of the redundant bus. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, *T/R Error (BIT Word).*

INHIBIT TERMINAL FLAG BIT (00110)

MESSAGE SEQUENCE = INHIBIT TERMINAL FLAG ⋆ STATUS

The BUS-65522 responds with status and inhibits further internal or external setting of the terminal flag bit in the status register. Once the terminal flag has been inhibited, it can only be reactivated by an Override Inhibit Terminal Flag or Reset RT command. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

OVERRIDE INHIBIT TERMINAL FLAG BIT (00111)

MESSAGE SEQUENCE = OVERRIDE INHIBIT TERMINAL FLAG ⋆ STATUS

The RTU responds with status and reactivates the terminal flag bit in the status register. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

RESET REMOTE TERMINAL (01000)

MESSAGE SEQUENCE = RESET REMOTE TERMINAL ⋆ STATUS

The BUS-65522 responds with status and internally resets. Transmitter shutdown, BIT word, mode commands, and inhibit terminal flag commands will be reset. If the command was broadcast, the broadcast received bit is set and the status word is suppressed.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

RESERVED MODE CODES (01001-01111)

MESSAGE SEQUENCE = RESERVED MODE CODES ⋆ STATUS

The BUS-65522 responds with status. If the command is illegalized through an optional PROM, the message error bit is set and only the status word is transmitted.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), Illegal Mode Code (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code *(BIT Word).*

⋆ = Status response time

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TABLE 8. MODE CODES (CONT'D)

TRANSMIT VECTOR WORD (10000)

MESSAGE SEQUENCE = TRANSMIT VECTOR WORD ⋆ STATUS VECTOR WORD

The BUS-65522 transmits a status word followed by a vector word. The contents of the vector word (from the subsystem) are enabled onto DB0-DB15 with $\overline{BUSREQ}$ after the command transfer (same as data word in a normal transmit command).

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, *T/R Error, Low Word Count (BIT Word).*
5. ***Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, (BIT Word).

SYNCHRONIZE WITH DATA WORD (10001)

MESSAGE SEQUENCE = SYNCHRONIZE DATA WORD ⋆ STATUS

The data word received following the command word is transferred to the subsystem. The status register is then enabled and its contents transferred onto the data bus and transmitted. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Not Followed by Data Word.*** No status response. Bits set: message error (SW), Low Word Count (BIT Word).
3. ***Command Followed by too many Data Words.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
4. ***Command T/$\overline{R}$ bit Set to One.*** No status response. Bits set: message error (SW), T/R Error, High Word Count (BIT Word).
5. ***Command T/$\overline{R}$ bit Set to One and Broadcast Address.*** No status response. Bits set: message error, broadcast received *(SW), High Word Count, T/R Error (BIT Word).*

TRANSMIT LAST COMMAND (10010)

MESSAGE SEQUENCE = TRANSMIT LAST COMMAND ⋆ STATUS LAST COMMAND

The status and BIT word registers are not altered by this command. The SW contains the status from the previous command. The data word transmitted contains the previous valid command (providing it was not another TRANSMIT LAST COMMAND).

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error (SW), Illegal Mode Code, T/R Error (BIT Word).
5. ***Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

TRANSMIT BIT WORD (10011)

MESSAGE SEQUENCE = TRANSMIT BIT WORD ⋆ STATUS BIT WORD

The BUS-65522 responds with status followed by the BIT word. When activated, $\overline{BITEN}$ allows the subsystem to latch the BIT word on the parallel data bus. The BIT word is not altered by this command; however, the next SW will reflect errors in this transmission.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bit set: message error (SW).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error (SW), Illegal Mode Code, T/R Error, Low *Word Count (BIT Word).*
5. ***Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

⋆ = Status response time

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TABLE 8. MODE CODES (CONT'D)

SELECTED TRANSMITTER SHUTDOWN (10100)

MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN DATA ⋆ STATUS

The data word received is transferred to the subsystem and status is transmitted. No other action is taken by the BUS-65522. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Intended for use with RTs with more than one dual redundant channel.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Not Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code *(BIT Word).*
3. ***Command Followed by too many Data Words.*** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code *(BIT Word).*
4. ***Command T/$\overline{R}$ bit Set to One.*** No status response. Bits set: message error (SW), Illegal Mode Code, High Word Count (BIT Word).
5. ***Command T/$\overline{R}$ bit Set to One and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), *Illegal Mode Code, High Word Count (BIT Word).*

OVERRIDE SELECTED TRANSMITTER SHUTDOWN (10101)

MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN DATA ⋆ STATUS

The data word received after the command word is transferred to the subsystem. No other action is taken by the BUS-65522. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Not Followed by Data Word.*** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code *(BIT Word).*
3. ***Command Followed by too many Data Words.*** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code *(BIT Word).*
4. ***Command T/$\overline{R}$ bit Set to One.*** No status response. Bits set: message error (SW), Illegal Mode Code, High Word Count (BIT Word).
5. ***Command T/$\overline{R}$ bit Set to One and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), *Illegal Mode Code, High Word Count, T/R Error (BIT Word).*

RESERVED MODE CODES

MESSAGE SEQUENCE = RESERVED MODE CODE (T/R = 1) ⋆ STATUS
RESERVED MODE CODE (T/R = 0) ⋆ STATUS

The BUS-65522 responds with status. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.

ERROR CONDITIONS (T/R = 1)

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code *(BIT Word).*

ERROR CONDITIONS (T/R = 0)

1. ***Invalid Command.*** No response, command ignored.
2. ***Command not Followed by Contiguous Data Word.*** No status response. Bits set: message error (SW), Low Word Count, *Illegal Mode Code (BIT Word).*
3. ***Command Followed by too many Data Words.*** No status response. Bits set: message error (SW), High Word Count, Illegal *Mode Code (BIT Word).*

⋆ = Status response time

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SELF TEST

The BUS-65522 performs an automatic self test each time a 1553 message is processed. The last word transferred onto the 1553 bus for each message is "looped back" from the transmitter to receiver. An on-line comparison of the transmitted word and the received looped back word is then performed. If a discrepancy is detected, the Error bit in the Block Status Word is set, the Terminal Flag bit is set in the 1553 Status Word, and an error interrupt is generated to the CPU, if enabled.

In the BC mode, the looped back word is placed in the next sequential location of the message block in the on-board RAM, where it is available for the CPU to inspect. See the data formats in figure 15 for specific 1553 message types.

The BUS-65522 maintains a separate BIT (Built-In-Test) register which contains information regarding the last message transfer (see figure 26). In RTU mode, the contents of this register are automatically passed to the BC in response to a Transmit BIT Word mode code command.

The Initiated [off-line] self-test can be executed only when the BUS-65522 is configured as a Bus Controller. Set the Wrap-Around Test bit within the BC Control Word (logic '1') and initiate any standard message transfer. This inhibits the 1553 transceivers and initiates the wrap-around test (i.e., internal 1553 encoder output is fed back into the decoder – the word is then written into memory). See BC Operation and Figure 14, BC Control Word for more detail.

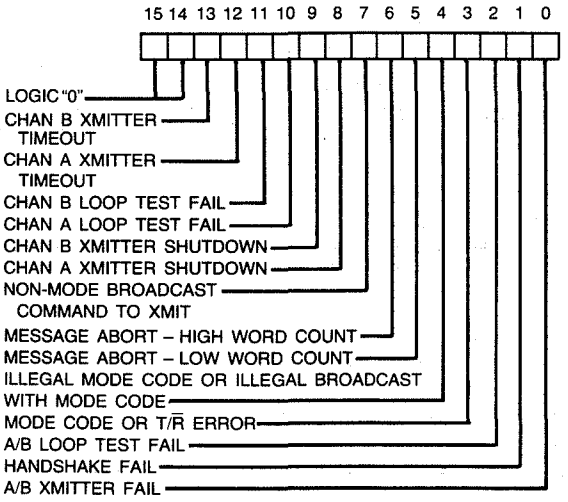


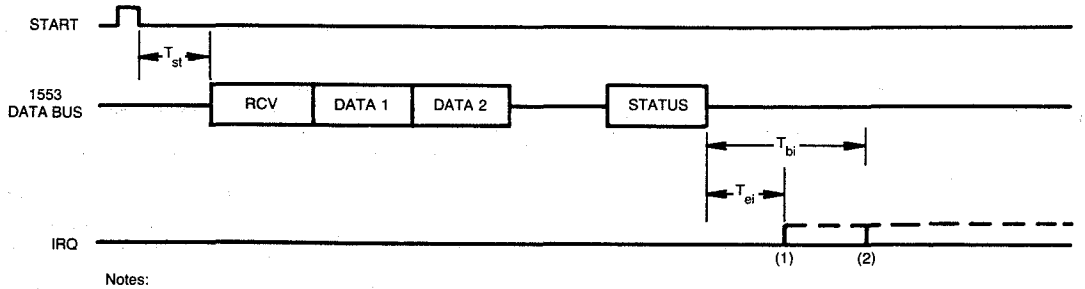
FIGURE 26. BUILT-IN-TEST (BIT) WORD

BUS-65515 BC AND RTU MODE TIMING

Table 9 defines the times and lists the units for the following 11 timing diagrams.

TABLE 9. 1553 I/O TIMING DEFINITIONS

TIME	DEFINITION	MIN	MAX	UNITS
T_{st}	Start timing (start to data on 1553)	3	4	μs
T_{ei}	EOM/Error Interrupt	5	7	μs
T_{bi}	BC EOM Interrupt	10	12	μs
T_{ebo}	EOM/Error Timeout Interrupt	19	21	μs
T_{gp}	Intermessage Gap (Mid parity to mid sync)	12	12	μs
T_{gpto}	Intermessage Gap (Timeout) (Mid parity to mid sync)	24	26	μs
T_{rsp}	Response Time (Mid parity to mid sync)	10	12.5	μs
T_{ero}	RT/RT Timeout Interrupt	19.5	20.5	μs



Notes:
(1) Error
(2)No Error

FIGURE 27. BC MODE – RECEIVE COMMAND

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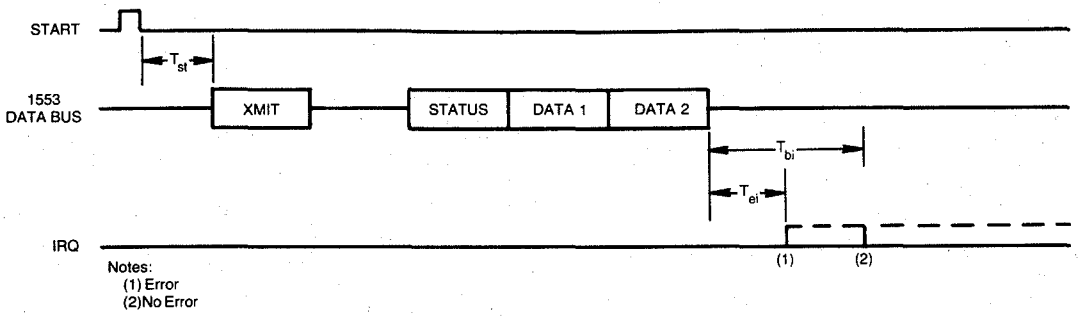


FIGURE 28. BC MODE – TRANSMIT COMMAND

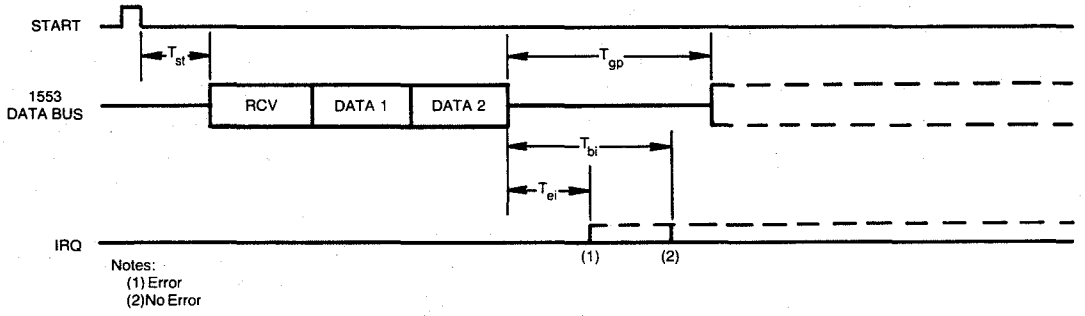


FIGURE 29. BC MODE – BROADCAST

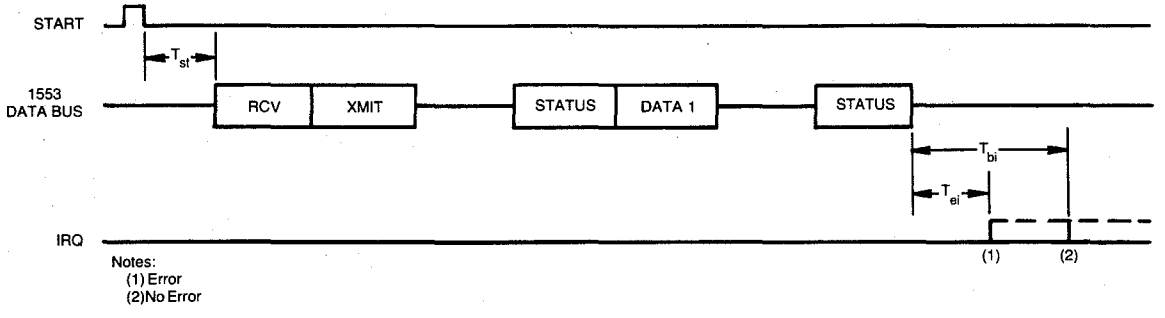


FIGURE 30. BC MODE – RTU TO RTU TRANSFER

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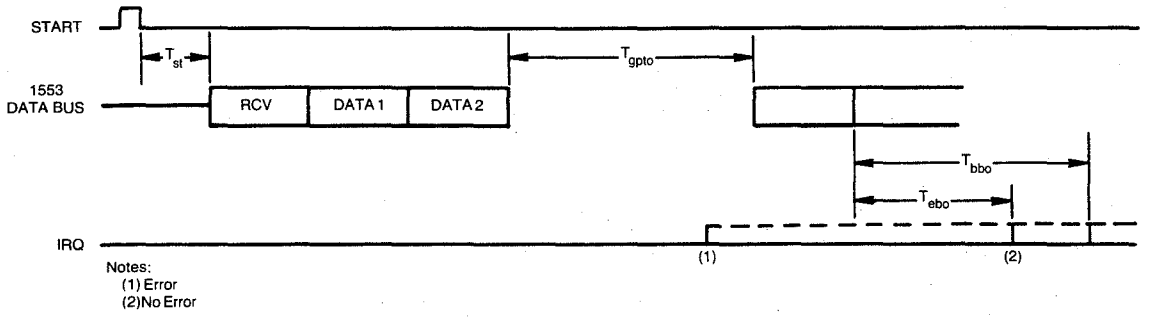


FIGURE 31. BC MODE – TIMEOUT

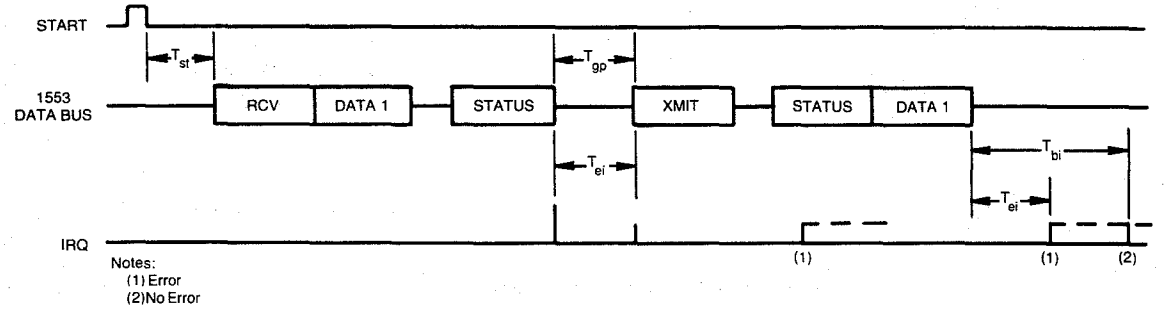


FIGURE 32. BC MODE – TWO COMMANDS

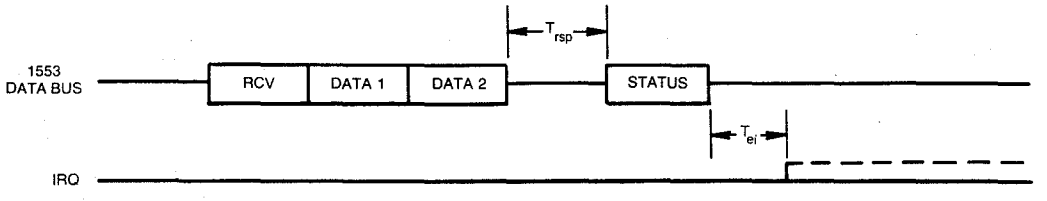


FIGURE 33. RTU MODE – RECEIVE COMMAND

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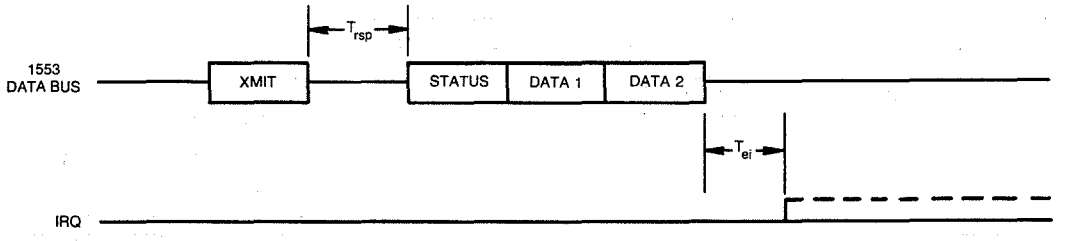


FIGURE 34. RTU MODE – TRANSMIT COMMAND

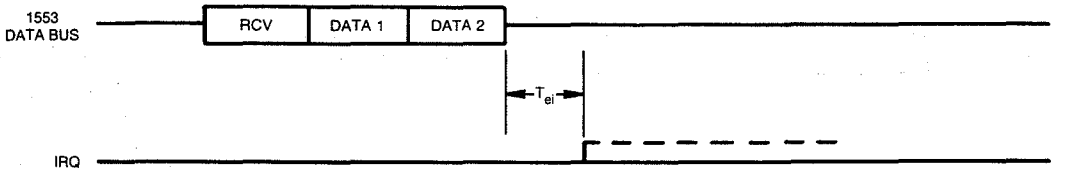


FIGURE 35. RTU MODE – BROADCAST COMMAND

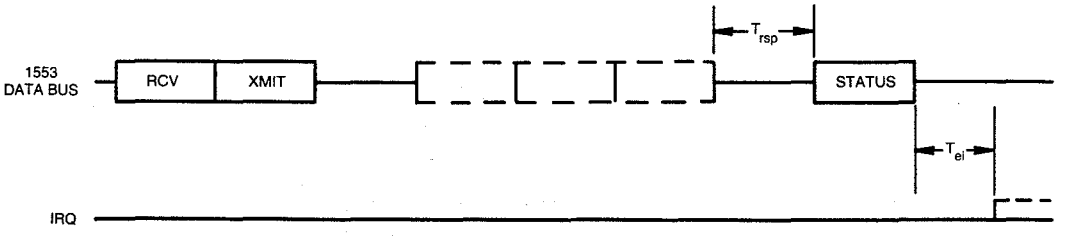


FIGURE 36. RTU MODE – RT/RT RECEIVE

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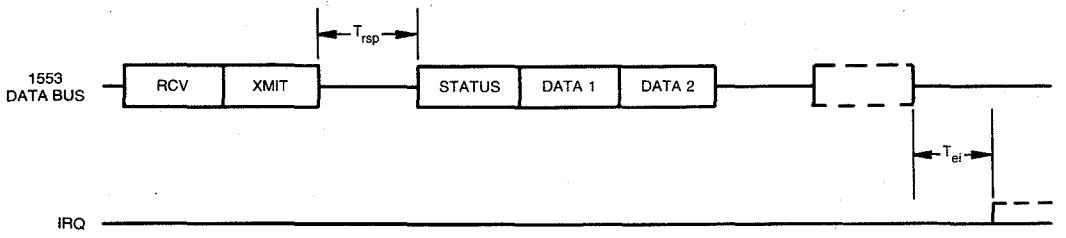


FIGURE 37. RTU MODE-RT/RT TRANSMIT

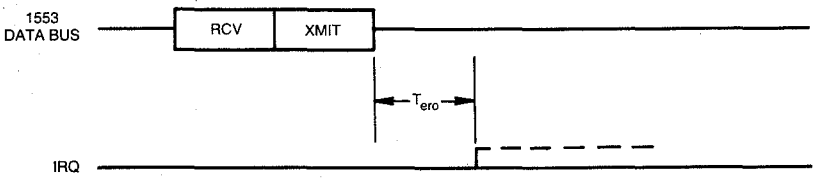


FIGURE 38. RTU MODE – RT/RT TIMEOUT

INSTALLATION

1553 COUPLING. The BUS-65522 can be direct coupled or transformer coupled to the 1553 bus. The user selects the type of coupling desired through the on-board jumper groups TB1 and TB2. The BUS-65522 comes equipped with two Bulkhead (front panel) connectors, Trompeter part no. BJ77 and mating connector Trompeter Cable Plug, part no. PL-75N.

Transformer coupled connections are also possible on the P2 connector, see TB6 and TB7 jumpers.

TB1 JUMPER CONFIGURATION

1553 CHANNEL A. Connections selected by jumpers at TB1 BUS-65522 shipped with:

(1) Transformer coupling selected.
(2) Frame floating.

TB1-1	DC COUPLED +
TB1-2	XFM COUPLED +
TB1-3	XFM COUPLED –
TB1-4	DC COUPLED –
TB1-5	FRAME TO GROUND

TB2 JUMPER CONFIGURATION

1553 CHANNEL B. Connections selected by jumpers at TB2 BUS-65522 shipped with:

(1) Transformer coupling selected.
(2) Frame floating.

TB2-1	DC COUPLED +
TB2-2	XFM COUPLED +
TB2-3	XFM COUPLED –
TB2-4	DC COUPLED –
TB2-5	FRAME TO GROUND

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TB3 JUMPER CONFIGURATION

BUS-65522 REGISTER ADDRESSES. The user may select the upper bits, (A6-A15) of the starting address of the BUS-65522 through the on-board jumper group TB3. (Adding a jumper sets the selected address bit to a logic "0".) BUS-65522 shipped with address 00 selected.

TB3-1	ADDRESS A6
TB3-2	ADDRESS A7
TB3-3	ADDRESS A8
TB3-4	ADDRESS A9
TB3-5	ADDRESS A10
TB3-6	ADDRESS A11
TB3-7	ADDRESS A12
TB3-8	ADDRESS A13
TB3-9	ADDRESS A14
TB3-10	ADDRESS A15

TB4 JUMPER CONFIGURATION

32 ADDRESS SPACE SELECTION. Adding a jumper to TB4 selects 32 Bit address bus. Removing the jumper selects 24 Bit address bus.

TB5 FACTORY LOOP TEST BIT

No Jumper = Normal operation
With Jumper = Factory loop test enabled

TB6 (P2) OPTIONAL 1553 P2 COUPLING (CHANNEL B)

TB6-1	BUS B + P2 (C4)
TB6-2	BUS B – P2 (C8)
TB6-3	SHIELD P2 (C5)

TB7 (P2) OPTIONAL 1553 P2 COUPLING (CHANNEL A)

TB7-1	BUS A + P2 (C24)
TB7-2	BUS A – P2 (C20)
TB7-3	SHIELD P2 (C25)

BUS-65522/23 PINOUTS P1 CONNECTOR

PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
A1	D0	B1		C1	D8
A2	D1	B2		C2	D9
A3	D2	B3		C3	D10
A4	D3	B4		C4	D11
A5	D4	B5		C5	D12
A6	D5	B6		C6	D13
A7	D6	B7		C7	D14
A8	D7	B8		C8	D15
A9	GND	B9		C9	GND
A10		B10		C10	
A11	GND	B11		C11	
A12	$\overline{DS1}$	B12		C12	$\overline{SYSRST}$
A13	$\overline{DS0}$	B13		C13	
A14	$\overline{WRITE}$	B14		C14	AM5
A15	GND	B15		C15	A23
A16	$\overline{DTACK}$	B16	AM0	C16	A22
A17	GND	B17	AM1	C17	A21
A18	$\overline{AS}$	B18	AM2	C18	A20
A19	GND	B19	AM3	C19	A19
A20	$\overline{IACK}$	B20	GND	C20	A18
A21	$\overline{IACKIN}$	B21		C21	A17
A22	$\overline{IACKOUT}$	B22		C22	A16
A23	AM4	B23	GND	C23	A15
A24	A7	B24	$\overline{IRQ7}$	C24	A14
A25	A6	B25	$\overline{IRQ6}$	C25	A13
A26	A5	B26	$\overline{IRQ5}$	C26	A12
A27	A4	B27	$\overline{IRQ4}$	C27	A11
A28	A3	B28		C28	A10
A29	A2	B29		C29	A9
A30	A1	B30		C30	A8
A31	–12V	B31		C31	+12V
A32	+5V	B32	+5V	C32	+5V

BUS-65522/23 PINOUTS P2 CONNECTOR

PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
A1		B1	+5V	C1	
A2		B2	GND	C2	
A3		B3		C3	
A4		B4	A24	C4	BUS B POS
A5		B5	A25	C5	BUS B SHIELD
A6		B6	A26	C6	
A7		B7	A27	C7	
A8		B8	A28	C8	BUS B NEG
A9		B9	A29	C9	
A10		B10	A30	C10	
A11		B11	A31	C11	
A12		B12	GND	C12	
A13		B13	+5V	C13	
A14		B14		C14	
A15		B15		C15	
A16		B16		C16	
A17		B17		C17	
A18		B18		C18	
A19		B19		C19	

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BUS-65522/23 PINOUTS (CONT) P2 CONNECTOR					
PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
A20		B20		C20	BUS A NEG
A21		B21		C21	
A22		B22		C22	
A23		B23		C23	
A24		B24		C24	BUS A POS
A25		B25		C25	BUS A SHIELD
A26		B26		C26	
A27		B27		C27	
A28		B28		C28	
A29		B29		C29	
A30		B30		C30	
A31		B31	GND	C31	
A32		B32	+5V	C32	

1553 FRONT PANEL CONNECTORS (Trompeter BJ77 mates with PL75-Bayonet) reference J1 & J2 connectors.

J1
Center Conductor – BUS A POS
Ring – BUS A NEG
Frame – Shield

J2
Same as J1 for 1553 Bus B Channel 1.

ORDERING INFORMATION

BUS-65522
- Power Supply Option:
  - 2 = ± 12V to ± 15V 1553B
  - 3 = ± 12V to ± 15V supplies (MACAIR)

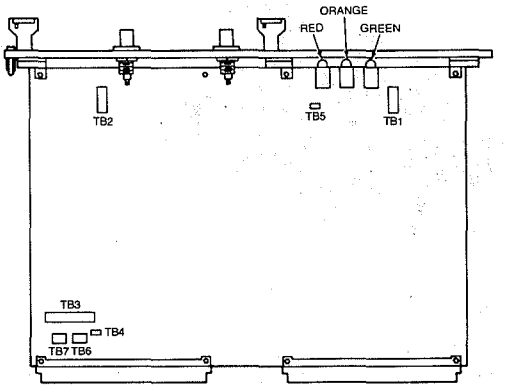


FIGURE 39. JUMPER CONNECTIONS

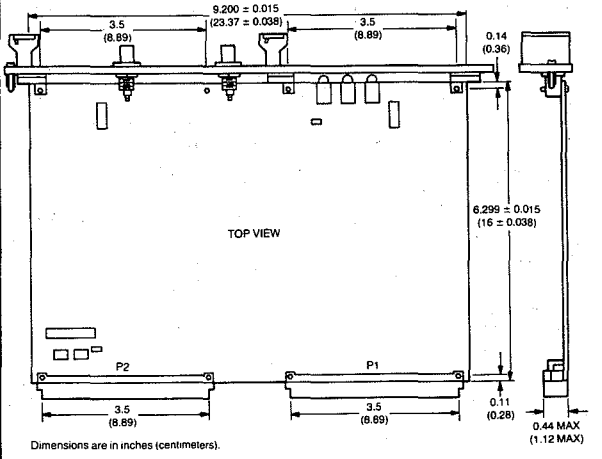


FIGURE 40. MECHANICAL OUTLINE

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