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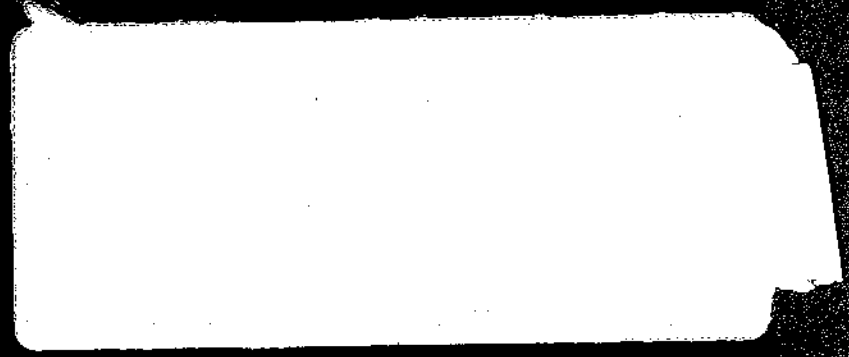
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INSTRUCTION MANUAL
FOR
BUS-68005 DATA BUS EXERCISER

June 1988

ILC DATA DEVICE CORPORATION
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SECTION 1

GENERAL DESCRIPTION

1.1 SCOPE

This instruction manual provides installation, operating, and maintenance instructions for the Model BUS-68005 MIL-STD-1553 Data Bus Exerciser, hereafter referred to as the Exerciser. The Exceriser is exclusively designed and manufactured by ILC Data Device Corporation, Bohemia, New York.

1.2 PURPOSE OF EQUIPMENT

The Exerciser is an instrument designed to assist in the development, test, and maintenance of RTs, BCs and bus monitors configured for use in systems meeting Aircraft Internal Time Division Command/Response Multiplex Data Bus MIL-STD-1553 requirements.

The Exerciser is packaged in a 3.47 in. x 14.5 in. x 17.0 in. full rack enclosure with a handle that can be used as a tilt-stand. It operates from either 115 VAC or 230 VAC 47-63 Hz power. With its flexible manual or remote programmability and its error generation and detection, the Exerciser is ideal for simulation of BCs or RTs for bench, field, or factory test applications.

For manual operation, the instrument is equipped with a 24-button keyboard and display consisting of a 10-character alphanumeric readout and 12 LED indicators. The display indicates:

1) Programmed and received message data on a word-by-word basis.
2) The unit's present programmed status.
3) Real-time information including indications of bus activity and fault conditions such as message error, response and transmitter timeouts.

For operation under the control of a host computer, the instrument is equipped with an 8-bit tri-state parallel I/O port as well as RS-232 and IEEE-488 (GPIB) ports. The unit is fully controllable through any of these interfaces. The IEEE-488 interface incorporates DMA capability.

When configured in the BC mode, the unit may be programmed to process up to eight messages of up to 49 words each at a given time. Intermessage gap time may be selected from 7 to 2047 us, in 1 us steps. The Exerciser evaluates the response to each command, and flags and displays errors such as response time, continuity, Manchester encoding, sync, parity, and high or low bit count or word count. Each message has independent programmable parameters, including format, word count, response time and intermessage gap time. The Exerciser implements BC-to-RT, RT-to-BC, and RT-to-RT message transfer formats, as well as broadcast and mode code commands. Furthermore, the Exerciser can be configured to simulate both the BC and either of the RTs for an RT-to-RT transfer. Commands and responses are stored in the Exerciser internal RAM, and may be viewed on a word-by-word basis by means of a

10-character front panel alphanumeric display or any of the remote I/O ports. These formats are useful for exercising and testing RT devices. As a BC, a large number of error conditions may be generated and detected. Induced error conditions include word errors, such as Manchester encoding error in any bit position, parity error, sync type, sync encoding, bit count, zero-crossing, mid-word and inter-word gap errors, as well as message errors such as incorrect word count, response and transmitter timeout and various format errors.

Two Exercisers may be used to perform the Bus Switching test for dual redundant RTs, as required by the SAE ASD-1 (formerly AE-9A) Production Test Plan. By means of a simple 3-wire interface, it is possible to synchronize the start of bus activity for the two instruments. Under either keyboard or remote I/O control, the delay time interval between the start of bus activity on the two redundant buses may be programmed to be anywhere in the range from 0 to 2040 us, in 1 us steps. It is also possible to perform the bus switching test using a single Exerciser in conjunction with a BUS-68015 Noise Tester, under control of the IEEE-488 (GPIB) interface.

As an RT simulator, the Exerciser receives, validates, and stores data bus commands containing any of its programmed addresses. Up to eight RTs can be simulated at one time. Each simulated RT address may be mapped to one or more Exerciser memory blocks, allowing the Exerciser to transmit or receive multiple messages for the same RT in real time. It responds to commands with status and data, as appropriate. Response time may be programmed from 6 to 31 us, in 1 us steps. Up to eight messages of 49 words each may be stored at one time in the Exerciser's internal RAM. These messages may be accessed via the keyboard for viewing on the front panel alphanumeric display. The selectable formats are similar to the formats for the BC mode, with the instrument capable of simulating either or both the transmitting and receiving RTs for RT-to-RT transfers. This feature enables the unit to perform full characterization and testing of BCs. In the RT mode, as in the BC mode, the Exerciser can generate and detect a similar repertoire of word, message, and timing errors.

The Exerciser also includes a real-time monitor output port. In addition to providing a 16-bit parallel representation of each word on the 1553 bus as it is transmitted or received in real time, this port also provides indications of sync type, data direction, word errors, RT trigger word flag, Exerciser message block number, and many other signals that may be used in various testing applications. The real-time monitor output port may be utilized as either a passive monitor interface or as a high-speed parallel window to the bus when the Exerciser is in either BC or RT mode.

Another feature included to support real-time operation is direct memory access (DMA) capability for the IEEE-488 (GPIB) interface. This provides a direct, high-speed parallel link between a host computer and the Exerciser's message and trigger RAMs, and control registers.

In either mode, the Exerciser is programmable for either single frame (one to eight) messages or continuous operation. Also, the number of active message blocks as BC, or the number of enabled RTs, is programmable from one to eight. As BC, the frame (repetition) time is also a programmable parameter.

Other features of the Exerciser include relay-selectable 2-channel bus operation with a choice of direct or stub coupling from the front and rear panels,

respectively. Additional features include sync outputs for oscilloscope viewing, transmitted waveform amplitude variable via keyboard or host computer I/O control (from 0 to 9.75 Vpp direct coupled) and a fully internal self-test routine performed at power turn-on or following user command which exercises ROM, RAM, and most of the Exerciser front end components. The instrument also allows for selecting 120/240 VAC, (50/60 Hz) operation.

1.3 FEATURES

The most significant Exerciser capabilities are summarized as follows:

1) Full implementation of the protocol portion of the SAE ASD-1 (AE-9A) Production Test Plan for MIL-STD-1553 RTs. For testing of dual redundant RTs, two Exercisers, or one Exerciser and one BUS-68015 Noise Tester may be used.

2) Ability to handle up to eight message blocks as BC or simulate up to eight RTs.

3) Inclusion of a real-time monitor output port. This interface, which provides a broadside parallel window to the activity on the 1553 bus, may be used either as a passive background monitor or in conjunction with the Exerciser's BC or RT modes.

4) Timing requirements for MIL-STD-1553A as well as MIL-STD-1553B are supported. These include programmable response times of 5 to 31 us (BC mode), 6 to 31 us (RT mode) and a BC intermessage gap programmable from 7 to 2047 us. For the Exceriser, the response time-out value for an external RT is programmable over the range of 5 to 32 us (per the MIL-STD-1553B definition). In addition, a timer detects violations of the minimum response time specification (4 us per MIL-STD-1553B, 2 us for MIL-STD-1553A).

5) For RT mode, capability to transmit or receive multiple blocks of data from or to the same RT address in real time.

6) Trigger input and output signals, allowing two Exercisers to be synchronized for testing of dual redundant RT operation.

7) Variable transmission amplitude via keyboard or remote I/O control.

8) Quasi dual redundancy, with channel A/B selection via keyboard or remote I/O control.

9) The transmitter amplitude level, programmable via either keyboard or host I/O control, is selectable from 0 to approximately 9.75 Vpp peak-to-peak (direct coupled across 35 ohms).

10) Induced word error capability: Manchester, parity, bit count, sync, mid-word gap, interword gap, and zero-crossing deviation errors. Halt-on-error capability.

11) Manual operation via a 24-button keyboard and a 10-character display.

12) Eight-bit tri-state parallel I/O, RS-232 and IEEE-488 (GPIB) interface ports provide communication to an ATE host computer. The IEEE-488 interface includes DMA capability to support high-speed testing.

13) User-friendly interactive CRT terminal operation via the RS-232 interface port.

14) Sync output provided for oscilloscope viewing.

15) Comprehensive built-in self-test capability exercises internal microcomputer and 1553 components. Includes diagnostics for failure of a 1553 bus wraparound test.

16) Configured with a carry handle which doubles as a tilt stand for bench use. In addition, brackets are provided for full-rack, 19-inch mounting.

17) Switch-selectable 115/230 VAC (50/60 Hz) operation.

1.4 OPTIONS

The Exerciser is available in a single configuration:
Equipped with an 8-bit tri-state parallel port, as well as IEEE-488 (GPIB) and RS-232 interface ports.

1.5 EQUIPMENT SUPPLIED

Each Exerciser is supplied with two triaxial connectors for the 1553 bus I/O, a mating connector for Real Time Monitor/Trigger I/O port J15, a line cord, and two full-rack mounting brackets and screws. Refer to paragraph 2.3.

1.6 PHYSICAL DESCRIPTION

The Exerciser instrument is a full-rack, lightweight instrument. Figure 1-1 illustrates the instrument with its carry-handle/tilt-stand, as supplied. By removing the handle and installing the two provided brackets, the instrument is easily installed in a standard 19 inch NEMA rack. (Refer to Figure 2-1(d).).

The ten 7-segment LED displays, along with 12 individual LED indicators, RUN and HALT pushbuttons, and two 12-position keyboards, are mounted on a PC board, which is situated behind the front panel. Figure 1-2 provides front and rear panel views of the display board assembly. Other front panel features include a POWER on/off switch, two triaxial connectors for the 1553 bus I/O, and a BNC connector for the Sync output.

Internally, the instrument embodies two main PC boards in addition to the front panel display board. The two main boards connect to each other by means of the display board and to the front and rear panels via four separate harness assemblies. (Refer to Figure 4-3.)

The top PC board may be accessed by removal of the instrument's top cover. (See Figure 1-3.) The top board contains all the circuitry used to interface with the 1553 bus. This includes two isolating pulse transformers, a variable-amplitude transceiver, an error-generating encoder, and an error-detecting decoder. The transceiver is encased in a 24-pin hybrid package. The encoder and decoder are each packaged in separate replaceable modules. All modules and integrated circuits are mounted on sockets for ease of maintainability. Other circuits mounted on the top board perform the functions of message memory, clock generation, buffering, timing sequence control and real-time monitor interface. Removal of the bottom cover

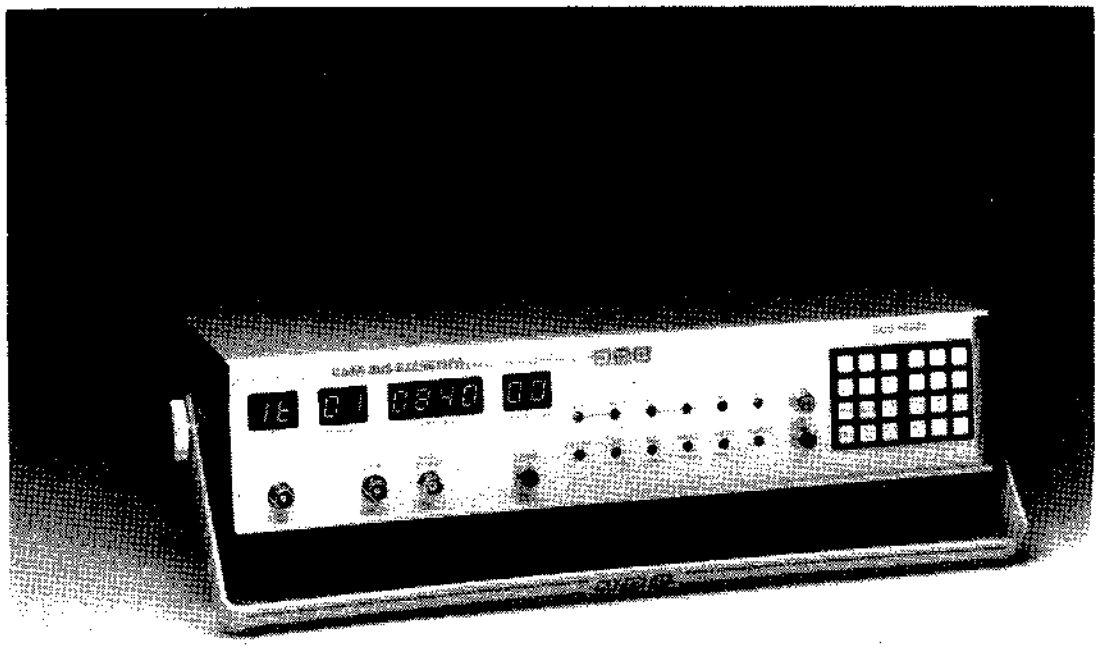
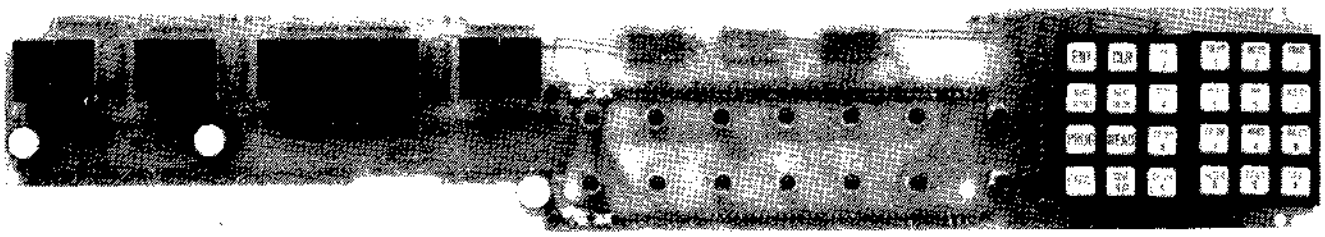
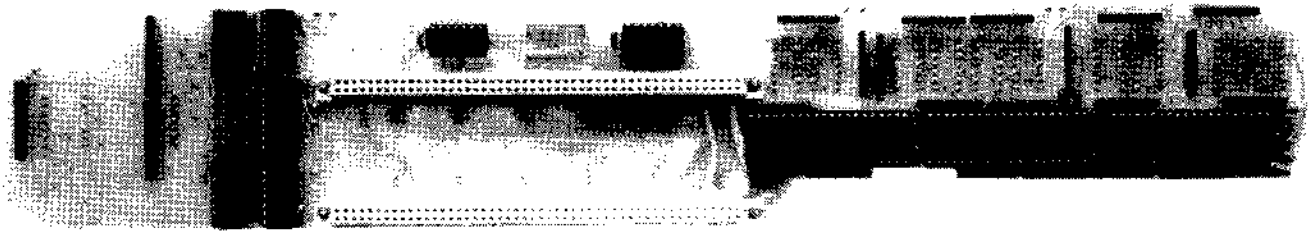


Figure 1-1. BUS-68005, Front View



(a)



(b)

Figure 1-2. Display Board (a) Front View, (b) Rear View

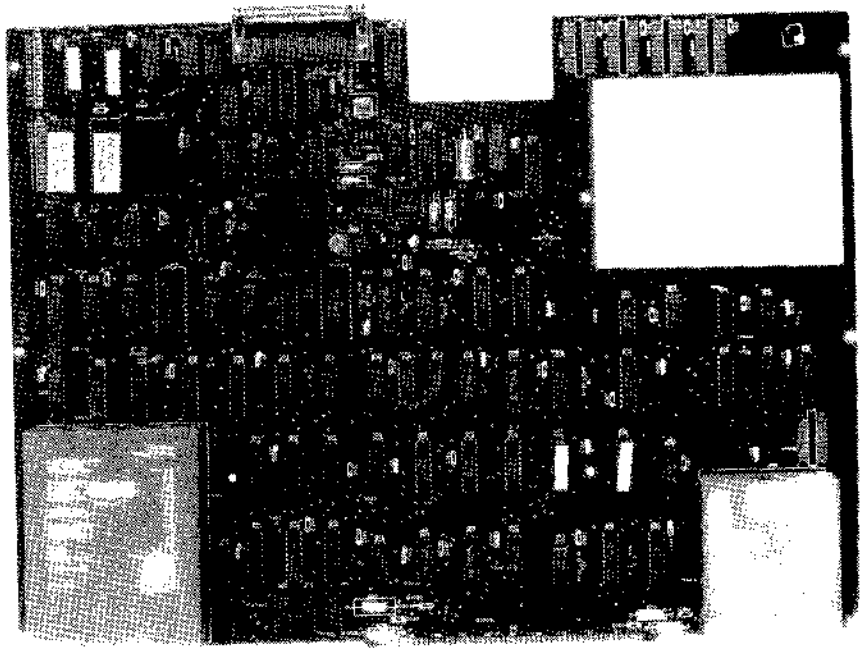


Figure 1-3. Top Board

exposes the solder side of the board. Access to the component side of the bottom board (see Figure 1-4) is achieved via the following procedure:

1) Remove the top and bottom covers.
2) Remove the front panel and display board.
3) Remove the top board.

The bottom board contains the power supply, microprocessor and interface sections. The power supply provides +24V, +5V, +15V, and -15V to the rest of the instrument. The microprocessor section, which includes program and scratchpad memory, services the manual and remote I/Os, and controls the operation of the 1553 interface. Circuitry for the five I/O sections are on the bottom board as follows:

1) Keyboard Interface
2) Display Interface
3) 8-Bit Tri-State Parallel I/O
4) IEEE-488 (GPIB) with DMA controller I/O
5) RS-232 I/O

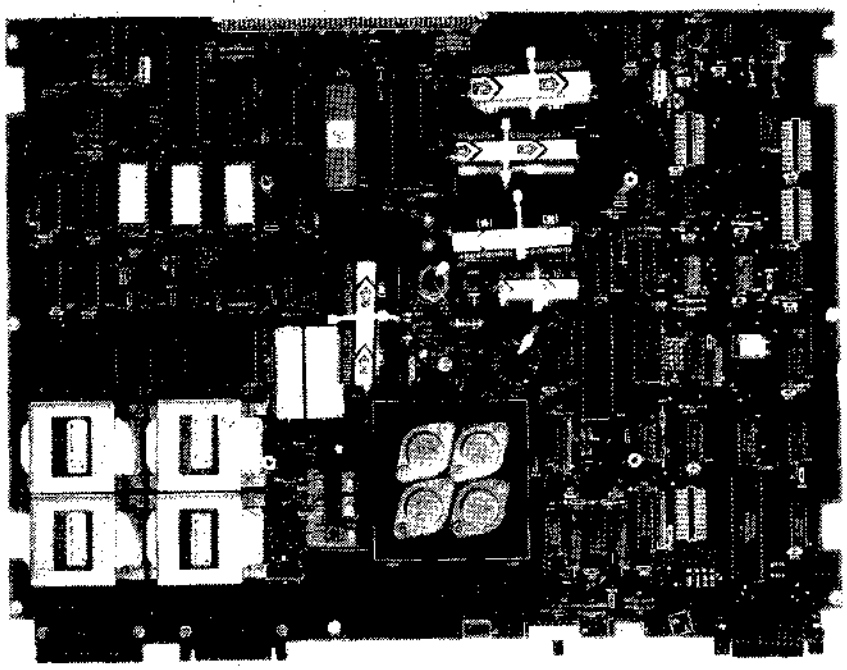


Figure 1-4. Bottom Board

The rear panel, shown in Figure 1-5, contains the following connectors: POWER connector (J1), 8-BIT PRL TRS I/O connector (J2), RS-232 connector (J3), GPIB connector (J4), REAL TIME MONITOR/TRIGGER connector (J15), bus output BNC connectors CH.A on and CH.B (J13) and SYNC OUTPUT connector (J14). In addition, included on the rear panel are the following switches: GPIB ADDRESS switch (S9), I/O SELECT switch (S8), and VOLTAGE SELECT switch (S2). A pressurizing fan with a guard and mesh filter are also mounted on the rear panel.

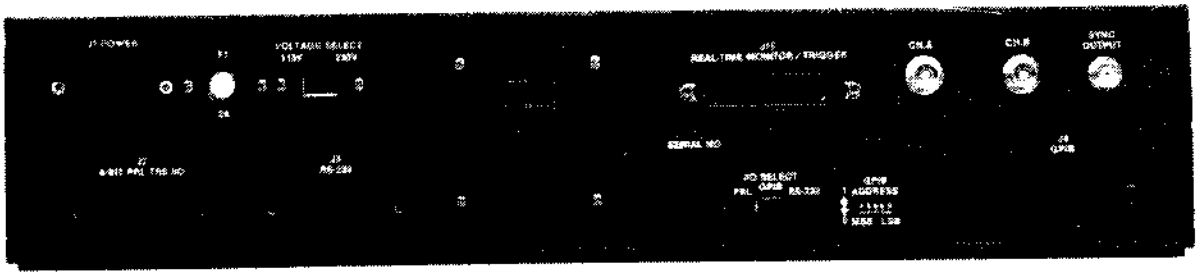


Figure 1-5. Rear Panel View

1.7 TECHNICAL SPECIFICATIONS

Refer to the table below for the technical specifications for the Exerciser.

Table 1-1. Exerciser Characteristics

PARAMETER	VALUE
DATA BUS INTERFACE	
Channels	2 (user selectable)
Coupling	Direct (front panel) or stub (rear panel)
Transmitter	
Output Voltage	Programmable: 0 to 9.75 Vpp nominal with 1 part in 255 resolution
Rise/Fall Time	200 +/- 20 ns
Output Noise	10 mv peak-to-peak max (differential)
Receiver	
Input Voltage	40 Vpp max (differential)
Input Impedance	4K min (differential)
Threshold Level	1 Vpp typ (direct coupled)
CMRR	40 dB min
BUS CONTROLLER MODE	
Message Formats (NOTE 1)	RT-to-BC, BC-to-RT, RT-to-RT including any combination of Mode Code and Broadcast
Message Repetition	Single, Repeat, or Halt after a programmable number (1 to 99) of Errors
Messages Per Frame	Programmable 1 to 8
Words Per Message	Programmable 1 to 49
Intermessage Gap	Programmable 7 to 2047 us
Frame Time	Programmable 2 to 500 ms

NOTE:

(1) In BC mode, unit can simulate BC only, or BC and either RT, for RT-to-RT transfer.

Table 1-1. Exerciser Characteristics - cont.

PARAMETER	VALUE
RT MODE	
Message Formats (NOTE 2)	RT-to-BC, BC-to-RT, RT-to-RT including any combination of Mode Code and Broadcast
Message Repetition	Single (1 to 8 messages) or Continuous
Simulated RTs	Programmable 1 to 8
Response Time	Programmable 6 to 31 us
RT Address	Programmable 0 to 31 transmitting or receiving; independent address for each message block
Message RAM blocks per RT address	Programmable 1 to 8
SELF-TEST	
Occurrence	Power turn-on or following user command
Circuitry Tested	Microprocessor RAM, ROM; Message RAM, Remote Terminal Trigger RAM, MIL-STD-1553 Front-End (Encoder/Decoder)
Indication	Pass, or Fail with fail code, plus diagnostics in case of MIL-STD-1553 wraparound test failure
Lamp Test	Blanks and illuminates all front panel LEDs
MANUAL INPUT OPERATION	
Type	Keyboard
Functions	Hex Data Entry 0 through F, Enter, Clear, Next Word, Next Block, Program, Read, Self-Test, Local, Single/Repeat, Mode, Format, RT Address, Response Time, Intermessage Gap Time, Word Count, Error Bit Position, Frame Time, Print, Message Count, Channel Select, Internal/External Trigger Select, Transmit Amplitude, Response Timeout, Halt-on-Error, Run, Halt
LED Display (7-Segment Displays)	Block Number, Direction Indicator, Word Number, 16-Bit hex Data, 8-Bit hex Error Code
LED Indicators	Local, Remote, Bus Controller, RT, Single, Repeat, On-Line, Line Active, Bus Fault, Reply Timeout, Transmitter Timeout

NOTE:

(2) In RT mode, unit can simulate either or both RTs, for RT-to-RT transfer.

Table 1-1. Exerciser Characteristics - cont.

PARAMETER	VALUE
REMOTE INTERFACES	
Types	8-Bit Tri-State Parallel, RS-232 and IEEE-488 (GPIB) with DMA
PARALLEL I/O	
Number of Lines	8 Bidirectional TTL Data Lines, T0 ~ T7; $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ TTL Request inputs; Transfer Acknowledge ($\overline{\text{TACK}}$), Read Acknowledge ($\overline{\text{RACK}}$), and Write Acknowledge ($\overline{\text{WACK}}$) open collector handshake outputs; $\overline{\text{SERVICE REQUEST}}$ open collector output.
Loading	
Input	1 TTL load for T0 ~ T7, READ, WRITE
Output	4 TTL loads for T0 ~ T7; 10 TTL loads for $\overline{\text{TACK}}$, $\overline{\text{RACK}}$, WACK and $\overline{\text{SERVICE REQUEST}}$
IEEE-488 INTERFACE	The following subset of the IEEE-488-1978 standard is implemented : SH1, AH1, T6, L4, SR1, RL1, DC1, DT1, C0.
RS-232 INTERFACE	
Word Length	1 Start Bit (Mark), 8 Data Bits (No Parity), 1 Stop Bit (Mark)
Received Parity	Ignored
Baud Rate	Factory configured for 9600 baud; selectable from among 134.5,150,600,900,1200,1800,2400,4800, 7200,9600
REAL-TIME MONITOR PORT	
Interface Bus Width	8,16,32-bit selectable
Outputs	16-bit Data Receive/$\overline{\text{Transmit}}$ Data/Command Sync Type $\overline{\text{Valid Word}}$ Word Errors (5) Block Address (3) $\overline{\text{RT Trigger Word}}$ Message Fault Indicators (3) Real-Time Signals (6)
Inputs	$\overline{\text{Tri-State Enables}}$ (5)

Table 1-1. Exerciser Characteristics - cont.

PARAMETER	VALUE
ERRORS GENERATED	
Manchester Error	Any bit position
Parity Error	Any word
High or Low Bit Count	Any word, -1, +1, +2 bits
Sync Type Error	Command or Data Word
Sync Field Error	Incorrect first, third, fourth, or sixth 500 ns time window
Word Gap Error	1 us gap between 8th and 9th data bits
Message Gap Error	2 us gap between end of current word to start of next word
Zero-Crossing Deviation Error	Start of bit time to mid-bit zero-crossing selectable from 312.5, 375, 625, 687.5 ns, any (single) data bit position
High or Low Word Count	Any message
Response Time Error	Any message
Format Error	Incorrect T/R bit any message
ERRORS DETECTED	
Manchester Error	
Parity Error	
Bit Count Error	
Word Count Error	
Sync Type Error	
Response Timeout	Programmable, 5 to 32 us (per MIL-STD-1553B)
Minimum Response Time Error	Less than 4 us (per MIL-STD-1553B)
Transmitter Timeout	Greater than 800 us
AC POWER INPUT	
Voltage	115V/230V +/- 10% (switch-selectable)
Power	60VA max
Frequency	47-63 Hz
OPERATING TEMPERATURE RANGE	32^{0} F to 158^{0} F (0^{0} C to $+70^{0}$ C)

Table 1-1. Exerciser Characteristics - cont.

PARAMETER	VALUE
MECHANICAL	
Outline	3.47 in. x 14.5 in. 5 x 17 in. (9 cm x 37 cm x 43.2 cm)
Mounting	Bench or full-rack, standard
WEIGHT	18 lbs (8.2 kg)

SECTION 2

INSTALLATION AND OPERATION

2.1 INTRODUCTION

This section provides all necessary background information and detailed procedures for installing and operating the Exerciser. All input and output connectors are identified and a full discussion of the operation of the instruments by means of the keyboard/display and the four remote interfaces is included. Background information regarding the instrument's 1553 BC and RT simulation capabilities is imbedded in this discussion.

2.2 PREPARATION FOR USE

The Exerciser is operational in all respects as shipped from the factory. Carefully remove instrument from packing material and inspect front and rear panels for damage. Unless otherwise specified, the instrument is set at the factory for 115 VAC operation. This should be verified by checking the position of the VOLTAGE SELECT switch on the rear panel. Should the instrument show any signs of damage, notify the nearest ILC DATA DEVICE CORPORATION field representative immediately.

2.3 INSTALLATION

No special installation procedures are required for the instrument if it is used with the carry handle/tilt stand as shipped. For full rack mounting (19 in. rack), remove the handle and install the two rack adapters with the screws provided. Instrument mounting dimensions are shown in Figure 2-1.

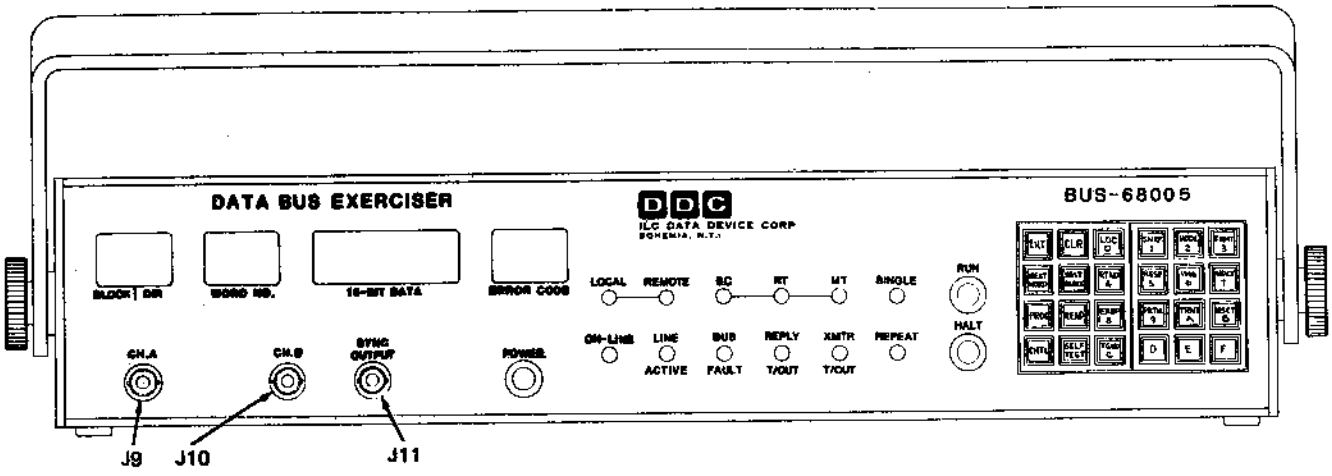
2.4 CONNECTIONS

The mechanical outline drawing (Figure 2-1) also shows location of all instrument panel switches, indicators and I/O connectors.

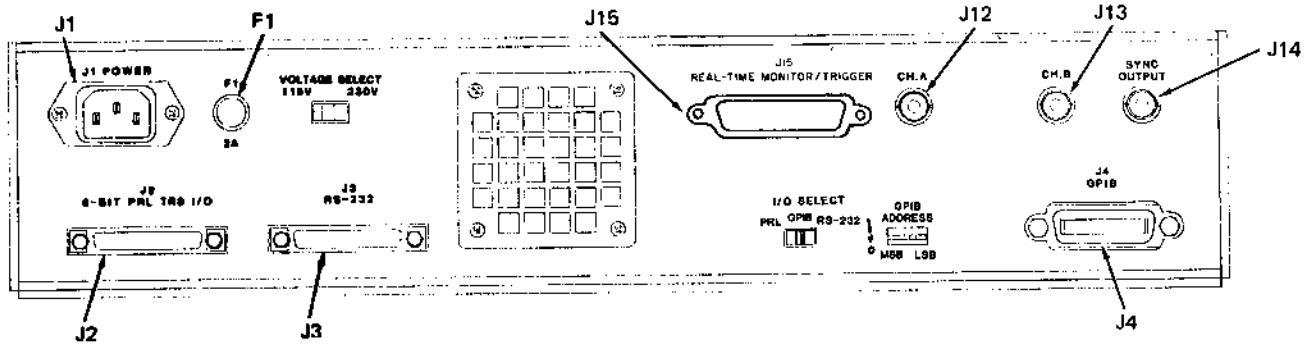
The Exerciser is supplied with a power line cord, Belden 40250; two 1553 bus mating connectors for the front and rear panel Channel A and B (J9, J10, J12 and J13), Trompeter PL75-47; and a mating connector for REAL TIME MONITOR/TRIGGER connector (J15), Amphenol 17-10500-1-390.

Also required but not supplied are mating connectors for:

- 8-Bit parallel tri-state I/O port (8-BIT PRL TRS I/O connector J2); TRW DB25S using backshell SDH-25BFCS.
- RS-232 port (connector J3); TRW DB25S using backshell SDH-25BFCS.
- IEEE-488 (GPIB) port; GPIB connector J4 (used to connect to IEEE-488 bus); appropriate "GPIB" type 24-pin connector.



(a) FRONT VIEW



(b) REAR VIEW

Figure 2-1. Outline Drawing (Sheet 1 of 2)

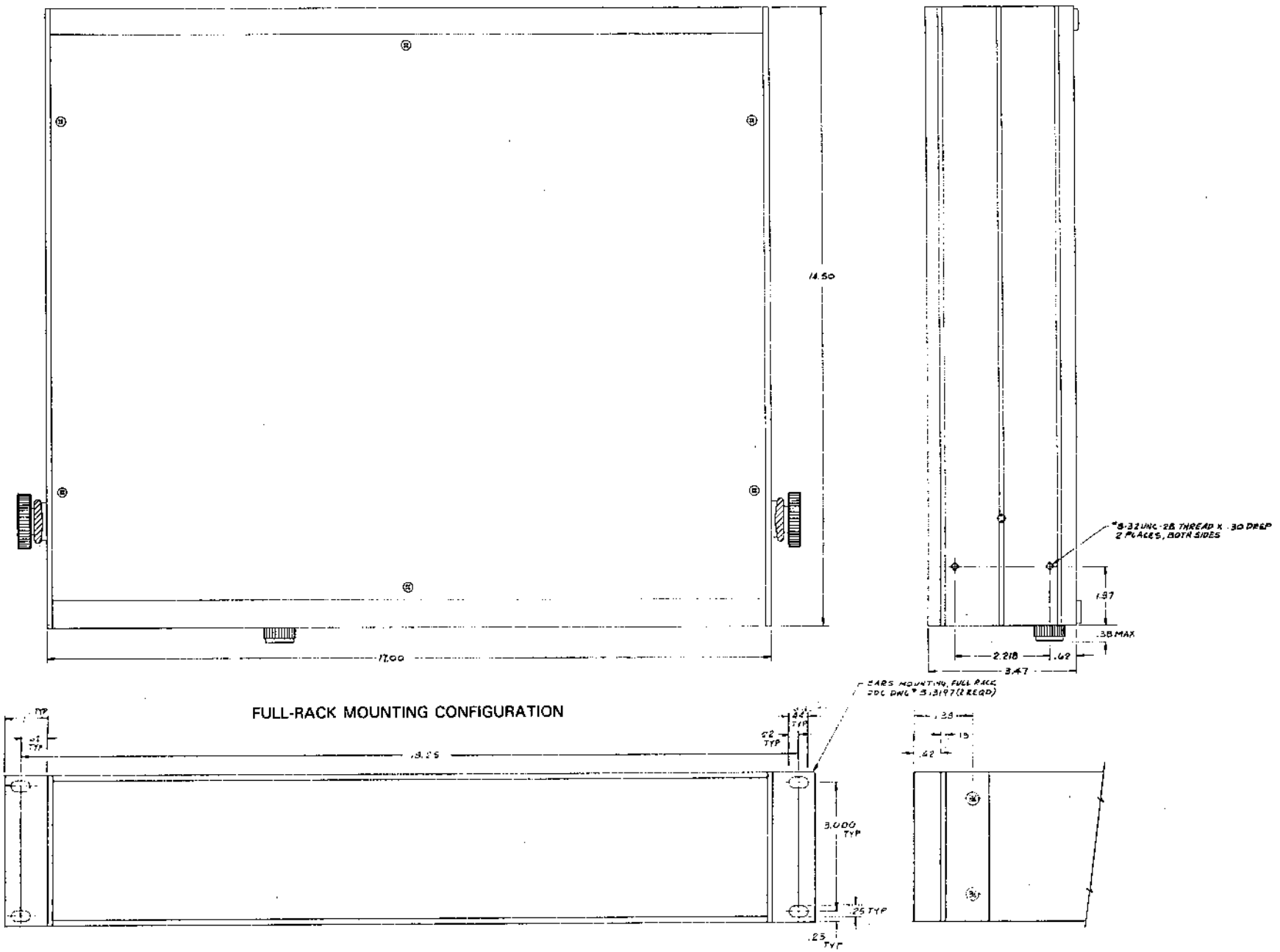


Figure 2-1. Outline Drawing (Sheet 2 of 2)

- Male BNC type cable connectors may be used to connect to CH. A, CH. B and SYNC output connectors (J11 and J14).

The internal and external schematic for the 1553 bus hook-up is shown in Figure 2-2. The following points should be taken into account when connecting the Exerciser to the 1553 bus:

1) The instrument contains all necessary circuitry for direct or stub coupling connection to a 1553 bus. However, it does not contain an internal termination. This must be constructed external to the Exerciser, as indicated in Figure 2-2.

2) To comply with MIL-STD-1553, the bus cabling should be comprised of twisted, shielded, jacketed cable with a characteristic impedance in the range of 70 to 85 ohms at 1 MHz. Trompeter 14949 cable is an example of such a cable. The bus should be terminated with 70 ohm resistors at both ends as shown to minimize reflections.

3) The instrument is configured as a quasi dual-redundant BC or Multi-RT simulator by means of an internal relay. This relay selects the active bus from between CH. A (front panel connector J9, or rear panel connector J12) and CH. B (front panel connector J10, or rear panel connector J13).

4) Front panel CH. A and CH. B ports (connectors J9 and J10, respectively) provide a direct coupled connection to the 1553 bus. It should be noted that MIL-STD-1553 allows for a maximum of 12 inches between a direct coupled device and the 1553 bus.

5) For "non-system" type testing (e.g., lab bench) of individual BC or RT devices, there is a more convenient hookup scheme which may be utilized. This is illustrated in Figure 2-3.

   The 35 ohm resistor simulates a properly terminated 70 ohm bus (as shown in Figure 2-2). Although this configuration does not conform strictly to MIL-STD-1553, it does allow for a simplified hookup scheme as compared to that shown in Figure 2-2 without compromising the quality of the data bus waveform.

   When using the configuration indicated in Figure 2-3, the monitoring oscilloscope must be configured as follows:

   - Connect DATA to channel A.
   - Connect $\overline{\text{DATA}}$ to channel B.
   - The oscilloscope must be configured for add mode, with the channel B input inverted. Select either 1 or 2 volts per vertical division.
   - Connect Exerciser SYNC OUTPUT to the oscilloscope external trigger input. Trigger from the positive slope of this signal.
   - For best oscilloscope viewing, the 1553 bus shield wire must be connected to chassis ground at both the Exerciser and device under test. This minimizes the amount of 50/60 Hz common mode pickup on the DATA and DATA lines. Although this pickup will not impair operation of the Exerciser or device-under-test, it will tend to make oscilloscope viewing difficult.

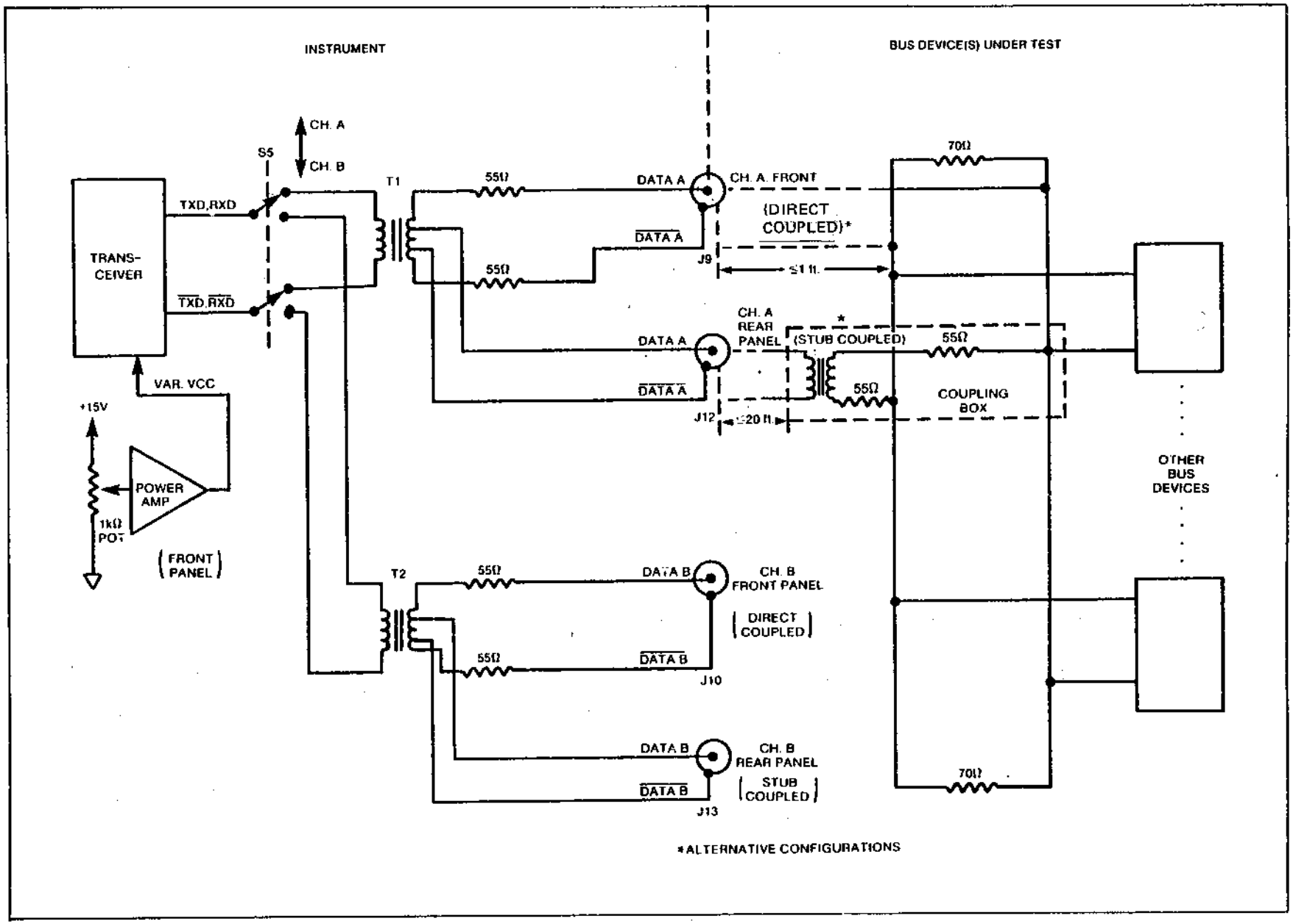


Figure 2-2. Electrical Hookup to Bus

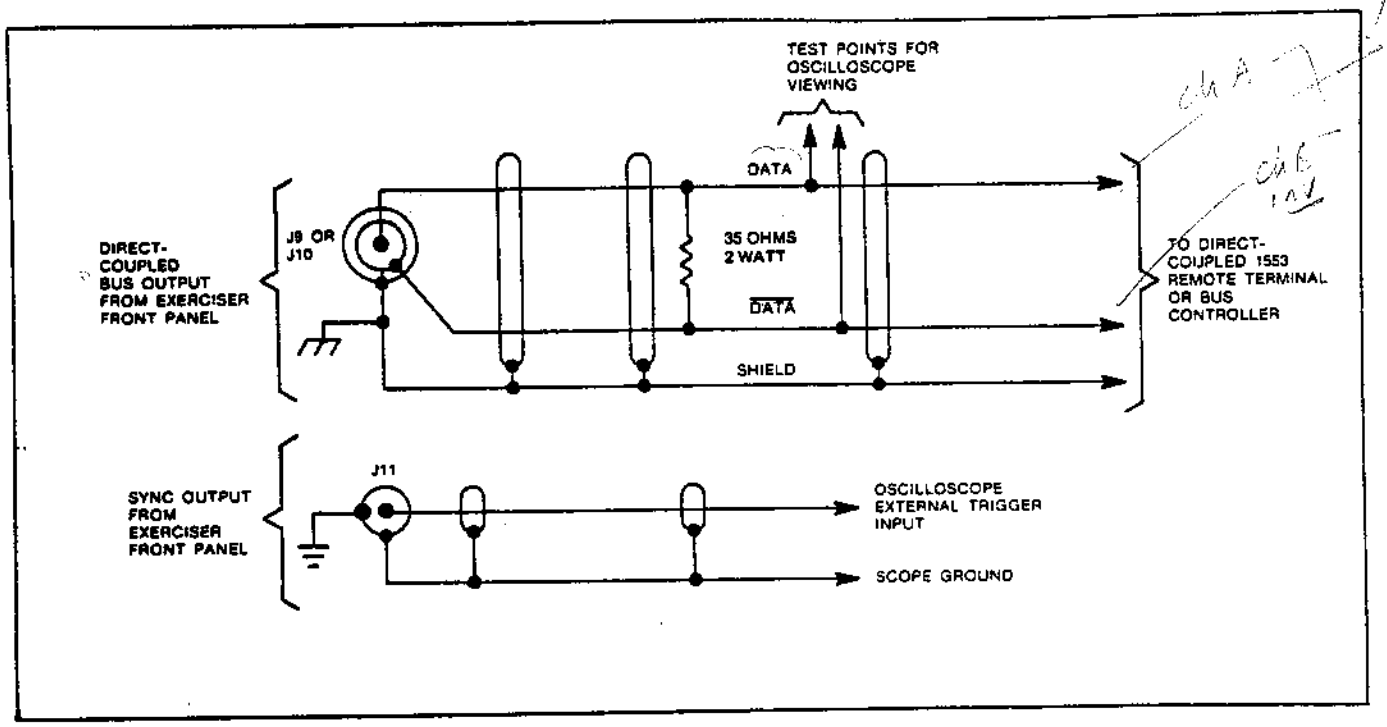


Figure 2-3. Suggested Lab Bench Connection Diagram

6) Rear panel CH. A and CH. B ports (connectors J10 and J13, respectively) provide for a stub, or transformer coupled connection to the 1553 bus. A stub coupled device may be connected through a distance of up to 20 feet (suggested maximum per MIL-STD-1553) and must be connected into the bus by means of a coupling box, comprised of a transformer and two 55 ohm resistors, as shown in Figure 2-3.

7) Front panel SYNC OUTPUT port (connector J11) and rear panel SYNC OUTPUT port (connector J14) provide a TTL sync output to assist in oscilloscope viewing of the 1553 bus waveform. In BC mode, the rising edge of the sync output precedes the start of a frame's transmission by approximately the time specified for the intermessage gap time (about 5 us minimum) for message 1. In RT mode, this edge occurs about 22 us after the start of a command word directed to one of the Exerciser's simulated RTs.

Pinout connections at the rear panel for the 8-bit tri-state parallel I/O port (8-BIT PRL TRS I/O connector J2), RS-232 port (RS-232 connector J3), IEEE-488 port (GPIB connector J4) and REAL TIME MONITOR/TRIGGER connector J15 are given in Tables 2-1, 2-2, 2-3, and 2-4, respectively.

Table 2-1. 8-Bit Parallel I/O Connector J2 Pinout

J2 PIN	FUNCTION	DESCRIPTION
1	T7 (MSB)	
2	T6	8-Bit
3	T5	bidirectional parallel
4	T4	tri-state
5	T3	I/O lines
6	T2	
7	T1	
8	T0 (LSB)	
9	$\overline{\text{READ}}$	Read Command Input
10	$\overline{\text{WRITE}}$	Write Command Input
11	$\overline{\text{TACK}}$	Transfer Acknowledge Output
12	$\overline{\text{SERVICE REQUEST}}$	Service Request Output
13	SIG. GND	Signal Ground
14	$\overline{\text{RACK}}$	Read Acknowledge Output
15	$\overline{\text{WACK}}$	Write Acknowledge Output
16	CHASS. GND	Chassis Ground

Table 2-2. RS-232 Connector J3 Pinout

J3 PIN	FUNCTION	DESCRIPTION
1	PROTECTIVE GROUND	Chassis Ground
2	TxD	Transmit Data
3	RxD	Receive Data
4	RTS	Request to Send
5	CTS	Clear to Send
7	SIGNAL GROUND	Ground
8	DCD	Data Carrier Detect

Table 2-3. GPIB Connector J4 Pinout

J3 PIN	FUNCTION	DESCRIPTION
1	$\overline{\text{DIO1}}$ (LSB)	Lower 4 data bits of GPIB Bus
2	$\overline{\text{DIO2}}$	
3	$\overline{\text{DIO3}}$	
4	$\overline{\text{DIO4}}$	
5	$\overline{\text{EOI}}$	End or Identify
6	$\overline{\text{DAV}}$	Data Available
7	RFD	Not Ready for Data
8	DAC	Not Data Accepted
9	$\overline{\text{IFC}}$	Interface Clear
10	$\overline{\text{SRQ}}$	Service Request
11	$\overline{\text{ATN}}$	Attention
12	CHASSIS GROUND	Chassis Ground
13	$\overline{\text{DIO5}}$	Upper 4 data bits of GPIB Bus
14	$\overline{\text{DIO6}}$	
15	$\overline{\text{DIO7}}$	
16	$\overline{\text{DIO8}}$ (MSB)	
17	$\overline{\text{REN}}$	Remote Enable
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground

Table 2-4. REAL TIME MONITOR/TRIGGER Connector J15 Pinout

J15 PIN	FUNCTION	DESCRIPTION
1	MON.TRANSMITTER TIMEOUT	Indicates bus activity greater than 800 us
2	$\overline{\text{MON.FAULT ENABLE}}$	Enables tri-state outputs for pins 1, 31, 32, 33 when low
3	$\overline{\text{RT TRIGGER WORD}}$	Indicates Exerciser's RT Address in command word when low
4	BLOCK ADDRESS 2 (MSB)	Exerciser block address, 0 through 7 indicating message blocks 1 through 8, respectively
5	BLOCK ADDRESS 1	
6	$\overline{\text{BLOCK ADDRESS 0 (LSB)}}$	
7	$\overline{\text{MON.BLOCK ADDRESS ENABLE}}$	Enables tri-state outputs for connector pins 3, 4, 5, 6 when low
8	MON.FRAME ENABLE	Indicates Exerciser on-line for BC or RT operation
9	MONITOR BUS CYCLE ACTIVE	Indicates that a message is being processed in BC or RT mode
10	MONITOR LINE ACTIVE	Indicates activity on the 1553 bus
11	MONITOR ENCODER CLOCK	2 MHz encoder clock - low when not transmitting
12	$\overline{\text{TRIGGER OUTPUT}}$	Used to synchronize another Exerciser BC transmission
13	$\overline{\text{TRIGGER INPUT}}$	Enables start of BC transmission in external trigger mode
14	MON.START-OF-MESSAGE	125 ns pulse indicates start of a message
15	MON.END-OF-MESSAGE	125 ns pulse indicates end of a message
16	GROUND	Ground
17	GROUND	Ground
18	MON.D2	3 LSBs of last transmitted or received word (LSB)
19	MON.D1	
20	$\overline{\text{MON.D0 (LSB)}}$	
21	$\overline{\text{MON.DATA LO ENABLE}}$	Enables tri-state outputs for pins 18-20, 46-50 when low
22	RECEIVE/$\overline{\text{TRANSMIT}}$	Indicates current word in buffer was transmitted by Exerciser when low
23	MON.$\overline{\text{VALID}}$/INVALID WORD	Indicates current word in buffer is valid when low
24	MON.DATA/$\overline{\text{CMD}}$ SYNC	Indicates command/status sync type for current word in buffer when low
25	MON.SYNC TYPE ERROR	Indicates incorrect sync type for current word if high
26	MON.PARITY ERROR	Indicates parity error for word in buffer if high
27	MON.MANCHESTER ERROR	Indicates Manchester encoding error for word in buffer if high
28	MON.LO BIT COUNT ERROR	Indicates low bit count error for word in buffer if high

Table 2-4. REAL TIME MONITOR/TRIGGER Connector J15 Pinout - cont.

J15 PIN	FUNCTION	DESCRIPTION
29	MON.HI BIT COUNT ERROR	Indicates high bit count error for word in buffer if high
30	MON.ERROR ENABLE	Enables tri-state outputs for pins 22 thru 29 when low
31	MON. WORD FLAG	Always high (when enabled by pin 2 low)
32	MON. BUS FAULT	Indicates word or word count error in current frame (BC mode) or current message (RT mode)
33	MON.REPLY TIMEOUT	Indicates that an RT external to the Exerciser has not responded in time
34	GROUND	Ground
35	GROUND	Ground
36	LOAD PULSE	125 ns negative pulse latches new data into output buffer on falling edge
37	MON.D15 (MSB)	(MSB)
38	MON.D14	8 MSBs of last transmitted or received word
39	MON.D13	
40	MON.D12	
41	MON.D11	
42	MON.D10	
43	MON.D9	
44	MON.D8	
45	MON.DATA HI ENABLE	Enables tri-state outputs for pins 37 thru 44
46	MON.D7	Part of last transmitted or received word
47	MON.D6	
48	MON.D5	
49	MON.D4	
50	MON.D3	

2.5 OPERATING CONTROLS AND INDICATORS

The controls and indicators used in the operation of the Exerciser are shown in Figure 2-1 and described in Table 2-5.

Table 2-5. Operating Controls and Indicators

ITEM	FUNCTION
FRONT PANEL	
POWER Pushbutton	Alternatively applies and removes AC power to the instrument.
RUN Pushbutton	Starts operation of the Exerciser's 1553 bus processor. If the instrument is in BC mode, it will start processing of a single message or multi-message frame. If the instrument is configured in BC single mode, the frame is processed one time only before the 1553 processor halts. If the instrument is configured in BC repeat mode, the frame of messages will repeat continuously until the HALT pushbutton is pressed, or, if running in Halt-On-Error "Repeat" BC mode, until the specified number of erroneous message frames has been processed. If the instrument is configured for single RT operation, it will respond in recognition to any one of its specified RT addresses and halt following the processing of the number of messages specified by the "Blocks per Frame" or "Message Count" parameter. If an insufficient number of such commands are received, the instrument may be taken off-line by pressing the HALT pushbutton. In the "Repeat" RT operation, the instrument will continue to respond to commands containing any of its programmed addresses until commanded to go off-line by pressing the HALT pushbutton.
HALT Pushbutton	Causes the 1553 processor to halt operation. (Refer to discussion on RUN pushbutton.)

Table 2-5. Operating Controls and Indicators - cont.

ITEM	FUNCTION
24-Button Keyboard	Provides for full manual control of instrument operation. It enables hex data entry and/or review of all command, status and data words as well as decimal or hex (as appropriate) entry of all parameters (e.g., timing, formatting, modes, etc.) relating to instrument operation. It should be noted that the sixteen (16) hex data entry keys (denoted 0 through F) are dual function keys. The upper case functions are marked in red, while the hex data values are marked in blue. In order to activate one of the upper case functions, it is necessary to first press the red CNTL key; then, while still pressing CNTL, the function key must be pressed. A detailed description of the various key functions and associated displays is given in Table 2-14.
10-CHARACTER LED DISPLAY	
BLOCK Digit	Displays number of message block currently being programmed or reviewed.
DIR Indication	This character indicates data direction for currently displayed word. It will indicate either "T", "P", "R", or "-", as follows: T: Transmit Word R: Received Word P: Pending Received Word; that is, either a word that is anticipated being received prior to the processing of a message, or a word that should have been received in a particular position within a message block, but was missing. -: The displayed word position is not used for the current combination of Exerciser mode (BC or RT) and the current block's format and word count.

Table 2-5. Operating Controls and Indicators - cont.

ITEM	FUNCTION
WORD NO.	This indicates the position of the current word within current message block. "WORD NO" will be a decimal number between 1 and 49.
16-BIT DATA	This 4-character field is used to display a 4-digit hex representation of the 16 bit positions for all transmitted or received command, status and data words. In addition, it is used to display other numeric parameter information such as format, programmed times, RT addresses, error positions, etc. For a detailed discussion, refer to Table 2-10.
ERROR CODE	This field displays the hex encoded error information for currently displayed word. Refer to Table 2-6 for error-coding for transmitted and received words.
INDIVIDUAL LED INDICATORS	
LOCAL	Indicates that the instrument is in local (keyboard) mode of control.
REMOTE	Indicates that the instrument is under control of one of the three remote I/O's. The active I/O port is determined by the setting of the I/O SELECT switch on rear panel.
BC	Indicates that the instrument is in the BC mode of operation.
RT	Indicates that the instrument is in the RT mode of operation.
MT	Indicates that the instrument is in monitor terminal mode of operation. This mode is not implemented in present the configuration of Exerciser.
SINGLE	Indicates that the instrument is in single mode of operation. That is, single frame for BC mode, or single group of from 1 to 8 messages for RT mode.

Table 2-5. Operating Controls and Indicators - cont.

ITEM	FUNCTION
REPEAT	Indicates that instrument is in repeat, or continuous mode of operation. That is, it will stay on-line until a halt command is received.
ON-LINE	A real-time display indicating that a 1553 bus message sequence is being processed by the instrument.
LINE ACTIVE	A real-time display indicating that there is activity on the 1553 bus; the activity may be originating from the Exerciser or from an external device on the bus.
BUS FAULT	Indicates that either a message error has occurred (instrument busy in repeat mode) or has occurred in the received portion of a message (instrument halted). The LED will clear only after the message frame sequence has been processed correctly, or following a Self-Test or Initialization command.
REPLY T/OUT	Indicates that an RT device external to the Exerciser has not responded within time specified by timeout parameter. Timeout is programmable from 5 to 32 us, per MIL-STD-1553B. An external RT that responds in less than 4 us (per MIL-STD-1553) will also cause the REPLY T/OUT LED to illuminate. Similar to the BUS FAULT LED, this indicator will clear only after the fault has been corrected, or following re-initialization.
XMTR T/OUT	Indicates that either the Exerciser or an external bus device has transmitted on the bus for longer than 800 us. The XMTR T/OUT LED will clear after the problem has been corrected or following re-initialization.

Table 2-5. Operating Controls and Indicators - cont.

ITEM	FUNCTION
REAR PANEL	
VOLTAGE SELECT Switch 115V/250V	Selects either 115 VAC or 250 VAC operation. The position of this switch should be verified before applying AC power to instrument.
I/O SELECT Switch PRL/GPIB/RS-232 ...	Selects active remote interface from among the 8-bit parallel (PRL) I/O, IEEE-488 (GPIB) and RS-232 interfaces. It should be noted that: 1. This switch position should only be changed when Exerciser power is off. 2. Commands addressed to a non-selected interface are ignored. 3. A print command (output) will be transmitted via the RS-232 port even if the RS-232 I/O is not the currently selected interface.
GPIB ADDRESS Switch	Designates unit's 5-bit device address for selection over the IEEE-488 (GPIB) bus. The bit positions (MSB-LSB) and logic sense (1-0) are panel marked.

2.6 POWER TURN-ON DISPLAY SEQUENCE

AC power is supplied to the Exerciser via the external line cord to rear panel POWER connector J1.

WARNING: Before applying AC power, it must be verified that the 115/230 VOLTAGE SELECT switch (S2) on the rear panel, is set to the appropriate house voltage.

Power is applied to the instrument by pressing POWER pushbutton (S1) on the front panel. After power is applied, front panel LED displays should indicate the following test sequence: (Each step in the sequence is displayed for approximately 1-2 seconds.)

1) All horizontal LEDs illuminate.
2) All LEDs turn off (blanking test).
3) All LEDs illuminate (lamp test).

4) Assuming self-test passes, pass will display in 16-BIT DATA field.

5) Eight dashes, followed by a 2-digit number representing the current software revision level, will be displayed.

6) IT 01 0840 00 will be displayed in the BLOCK, DIR, WORD NO., 16-BIT DATA and ERROR CODE fields, respectively. In addition, the LOC, BC and SINGLE individual LEDs will illuminate.

The self-test is a comprehensive software-controlled sequence that exercises several key internal portions of the instrument. The self-test is comprised of five parts:

1) Checkerboard and reverse checkerboard test of the microcomputer scratchpad RAM.

2) Checksum test of the three EPROM devices that store the microprocessor program.

3) Checkerboard test of the 1553 processor message RAM.

4) Checkerboard test of the RT address recognition (trigger) RAM.

5) An internal wraparound test of the 1553 front end. In this test, 47 test words, including erroneous words, are internally transmitted from the encoder to the decoder (but **not** on the external 1553 bus). The received words are then verified against the known correct patterns.

As noted above, the word PASS will displayed in the 16-BIT DATA display, provided that all parts of the self-test pass. Should one or more portions of the self-test fail, the word FAIL will be indiated in the 16-BIT DATA field and a 2-digit hex fail code will be displayed in the ERROR CODE field. The self-test fail byte is encoded as follows:

BIT WEIGHT (HEX)	80	40	20	10	08	04	02	01
BIT DESCRIP-TION	NOT USED (Always 0)	1553 Front End Wrap-around Test Failed	RT Trigger RAM Test Failed	Message RAM Test Failed	EPROM U21 Check-sum Failed	EPROM U23 Check-sum Failed	EPROM U24 Check-sum Failed	EPROM U22 Check-sum Failed

In the event of self-test failure, the display will continue to display the word FAIL and the appropriate fail code indefinitely. However, the Exerciser can still be forced to proceed to the next state, where it will display IT 01 0840 00, by pressing the CLR key. The Exerciser may then be operated with the knowledge that an internal fault condition exits.

If the self-test failure was due to a fault in the 1553 processor front end wraparound test (fail code of 40), it is possible to perform diagnostics. This is done by repeatedly pressing a combination of the CNTL and READ keys. By so doing, it is possible to get an indication of which test words failed and the received incorrect patterns. This procedure is discussed in the troubleshooting section of this manual in paragraph 4.4.

After self-test passes (or fails, and having pressed CLR), the front panel display will indicate:

1	T
BLOCK	DIR.

0	1
WORD NO.	

0	8	4	0
16-BIT DATA			

0	0
ERROR CODE	

The BLOCK field indicates that the displayed word is in message block 1. This field will always display a number between 1 and 8 when a 1553 message word is being displayed. That is, as BC, the Exerciser processes from 1 to 8 message blocks. In RT mode, the Exerciser can simulate from one to eight RTs. When the display is indicating a parameter other than a 1553 word, the BLOCK display may or may not be used. Refer to Table 2-6.

The DIR field indicates the direction of data flow over the 1553 bus for the current word. In this case, the "T" indicates that the word currently displayed will be transmitted by the Exerciser. In other instances, the DIR field may indicate R (received word), P (pending received word) or - (unused position in message RAM). Refer to Table 2-5.

The "01" in the WORD NO. field indicates that the currently displayed word is the first word of the message for the current message block (in this case block 1). In BC mode, the first word of any message is always a command word to be transmitted by the Exerciser.

The "0840" in the 16-BIT DATA field gives a 4-digit hex representation of the current word. By extracting the appropriate fields for a 1553 bus command word, it is seen that this is a receive command to RT 1, subaddress 2, requesting it to receive 32 data words. This is explained in detail in paragraph 2.10.1.

The "00" in the ERROR CODE field is a 2-digit hex indication, with the individual binary bit positions associated with unique word error types (i.e., Manchester encoding error, parity error, etc.). The display of 00 indicates that a valid word (no errors) is to be transmitted. This is discussed in detail in paragraph 2.9.1.7.

It was also noted that the LOC, BC and SINGLE LEDs are illuminated following self-test at power turn-on. BC indicates that the Exerciser is in BC mode. SINGLE indicates that the Exerciser is in single frame operation mode. LOC indicates that the instrument is in local, or manual mode of control. At this time, the user may proceed to control all instrument functions by means of the front panel keyboard. The Exerciser will remain in local control mode until it is given a command from the selected remote I/O source. The selected I/O source is determined from among the 8-bit tri-state parallel I/O, IEEE-488 (GPIB) and RS-232 ports by the setting of rear panel I/O SELECT switch (S8). The Exerciser will then remain in remote control mode until either:

1) The remote enable handshake line is disasserted or a go-to-local (GTL) command is received (IEEE-488 (GPIB) port only), or,

2) The user enters a CNTL-LOC command via the keyboard. It should be noted that CNTL-LOC will be ignored if either a Local Lockout (LLO) or, possibly, a Device Clear (DCL) command has been received from the IEEE-488 interface.

2.7 MESSAGE RAM ORGANIZATION

The message memory of the Exerciser consists of a 16K bit RAM that is shared between the user interface (microprocessor) and the 1553 bus processor portions of the Exerciser. The message RAM is configured as a dual port memory. That is, it is addressable as a 2K x 8 memory from the microprocessor side and as a 1K x 16 memory by the 1553 interface.

Figure 2-4 illustrates the organization map of the Exerciser message RAM. As shown in the map, word 1 of block 1 and all other 1553 message words each occupy four 8-bit bytes of RAM. It is also seen that the shared RAM is divided into eight partitions or blocks. Each block is 256 (100 hex) bytes deep. That is, the transmitted and/or received words for each message to be processed (BC mode), or each RT message to be simulated (RT mode) are stored in separate, contiguous blocks of memory locations.

It may also be seen that the first 4-byte word of each block is designated as the control word for that block. The control word, which logically is designated as word 0 for the block, contains the control parameter information for the BC message to be processed or RT message to be simulated. These block parameters include format, word count, response time, intermessage gap time (BC mode) and "linked to" block number (RT mode). Although these parameters are all user programmable via the keyboard and remote I/Os, the control word per se is accessible only by means of the high speed and DMA remote I/O commands discussed in paragraphs 2.11.4 and 2.11.5.

The 1553 message words are stored in word positions 1 through 49 of each message block. Word positions 50 through 63 (byte addresses 1XC8 through 1XFF) are unused for blocks 1 through 8.

The command, status and data words to be transmitted or received by the Exerciser are stored in separate contiguous memory blocks for each 1553 message, starting at word position 1 for each respective block. For example, in the case of the Exerciser acting as BC for an RT-to-BC transfer of two data words, the words of the message will be as follows: word 1 will be the command word; word 2 will be the received RT status word and words 3 and 4 will be the data words transmitted by the RT. As shown in the memory map, the two upper bytes for each 1553 word comprise the actual 16-bit word data. The third byte contains information relating to the various word error conditions that may be induced for transmitted words or detected for received words. The fourth byte contains positioning data for Manchester encoding, zero-crossing deviation or sync field errors for transmitted words. For received words, the fourth byte indicates whether a pending received word was actually received, as well as its sync type. The four-byte representation of all command, status and data words to be transmitted or received by the Exerciser is defined in Table 2-6.

With reference to Table 2-6, the following should be noted:

1) When the Exerciser is displaying current word on its front panel display, the contents of bytes 1 and 2 are displayed in the 16-BIT DATA display field. The contents of byte 3 are displayed in the ERROR CODE display. The contents of byte 4 are displayed in the 16-BIT DATA field when an Error Position command is entered. It should be noted that the "80" bits for both third and fourth bytes are masked to zero for the 16-BIT DATA display, but are indicated in decoded form (T, R, P,-) in the DIR field of the display.

ADDRESS (HEX)	DATA	
1000	Block 1, Word 0: Byte 1 (Word Count)	CONTROL WORD
1001	Block 1, Word 0: Byte 2 (Format)	
1002	Block 1, Word 0: Byte 3 (Response/IMG Time)	
1003	Block 1, Word 0: Byte 4 (IMG TIME/"Line" Block)	
1004	Block 1, Word 1: Byte 1 (Upper Data)	
1005	Block 1, Word 1: Byte 2 (Lower Data)	
1006	Block 1, Word 1: Byte 3 (Error Byte)	
1007	Block 1, Word 1: Byte 4 (Error Position Byte)	
1008 o o o 10C7	BLOCK 1: WORDS 2 THRU 49	
10C8 o o o 10FF	UNUSED	
1100 o o o 11C7	MESSAGE BLOCK 2	
11C8 o o o 11FF	UNUSED	
1200 o o o 17C7	MESSAGE BLOCKS 3 THRU 8	
17C8 o o o 17FF	UNUSED	

Figure 2-4. Exerciser Message RAM Map

Table 2-6. 4-Byte Representation of 1553 Words (Keyboard/Low-Speed I/O)

BYTE NO.	BYTE DESCRIPTION	BIT VALUE (HEX) 80	40	20	10	08	04	02	01
1 (T,R)	Command Word: Upper 8 Bits	5-BIT RT Address (MSB)				(LSB)	Transmit/ Receive	5-BIT Subaddress/ Mode (MSB)	
2 (T,R)	Command Word: Lower 8 Bits	5-BIT Subaddress/Mode		(LSB)	(MSB)	5-BIT Data Word Count/Mode Code			(LSB)
1 (T,R)	Status Word: Upper 8 Bits	5-BIT RT Address (MSB)				(LSB)	Message Error	Instrumentation	Service Request
2 (T,R)	Status Word: Lower 8 Bits	Reserved			Broadcast Command Received	Busy	Subsystem Flag	Dynamic Bus Control Acceptance	Terminal Flag
1 (T,R)	Data Word: Upper 8 Bits	BIT 1 (MSB)	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8
2 (T,R)	Data Word: Lower 8 Bits	BIT 9	BIT 10	BIT 1	BIT 12	BIT 13	BIT 14	BIT 15	BIT 16 (LSB)
3 (T)	Transmit Word: Generated Errors	Pending-Receive/Transmit (0)	Incorrect Sync Type Error	Parity Manchester Error	Sync Field Error	Parity Error	Manchester Encoding or Zero-Crossing Deviation Error	Low Bit Count or Message Gap Error	High Bit Count or Word Gap Error
4 (T)	Transmit Word: Generated Sync/Manchester Error Pos.	Transmit-Receive/Pending (1)	Error Type Select (See Table 2.9)	Sync/Zero Crossing Error Position 1	Sync/Zero-Crossing Error Position 0 or High Bit Count Select	Manchester/ Zero Crossing Bit Position 3	Manchester/ Zero Crossing Bit Position 2	Manchester/ Zero Crossing Bit Position 1	Manchester/ Zero Crossing Bit Position 0
3 (R)	Receive Word: Detected Error	Pending-Receive/Transmit (1)	Incorrect Sync Type	Early Response Error	Message Error	Parity Error	Manchester Encoding Error	Low Bit Count Error	High Bit Count Error
4 (R)	Receive Word: Receive Verification/Sync Type	Transmit Receive/Pending-(0:P, 1:R)	Date/Command-Status Sync Type	Not Used (Always 0)					

2) Bytes 1 and 2 are defined the same for both transmit and receive words. Bytes 3 and 4 are defined the same for command, status and data words.

3) The meanings of the bits for the error and error modifier bytes (3 and 4) are discussed in paragraph 2.9.1.7 and delineated in Table 2-7.

4) It is permissible to program single or multiple errors in any or all transmitted words. Similarly, it is possible to detect multiple errors in received words.

5) The "Message Error" bit, the "10" bit of the received word/detected error byte is set if a word error (i.e. Manchester encoding parity, etc.) occurs in a received word, or if one or more extra data words are received (high word count). The "Message Error" bit will remain set for all subsequent received words of the current message frame (BC mode) or current message (RT mode).

6) The "80" bits (MSBs) of the third and fourth bytes, designated as pending-Received/Transmit and Transmit-Received/Pending, respectively, are decoded as follows:

Table 2-7. Decoded Meaning of "80" Bits

"80" Bit of Third (Detected Error) Byte: Pending-Received/Transmit	"80" Bit for Fourth (Receive Verification/ Sync Type) Byte: Transmit-Received/ Pending	Word Type	Indication in DIR Display Field	Meaning
0	0	Unused	-	Location in message block not currently used
0	1	Transmit	T	Word transmitted by Exerciser
1	0	Pending Received	P	Word pending to be received by Exerciser
1	1	Received	R	Word received by Exerciser

2.8 POWER TURN-ON/INITIALIZATION STATE

The Exerciser will assume the following state following either power turn-on, a Self-Test command or an Initialize command from one of the three remote ports:

1) Two pointers, designated as Current Block and Current Word, are maintained in the Exerciser scratchpad memory. These pointers specify which word (or error byte) may be currently displayed on the front panel, programmed, or interrogated via a remote port. Block parameters such as response time, format, word count, etc. may be updated only for the block specified by the Current Block pointer. The Current Block and Current Word pointers both initialize to one (1).

2) The instrument is initialized for Local control, BC mode, Single Frame operation.

3) The 1553 message processor will be in the "Halt" state (not processing messages).

4) Blocks per frame, or Message Count is initialized to 1 (block 1 only).

5) Frame time is initialized to 10 ms.

6) For blocks 1 through 8, word 1 is specified as a T (transmit) word with 16-bit data of 0840 (a receive command word to RT 1, subaddress 2, to receive 32 words). Words 2 through 33 are initialized as transmit words to 0000, 0001, 0002, ... 001E, 001F. Word 34 is initialized as a P (pending received) word. Words 32 through 49 are initialized as - (unused), to 0000. The displayed error byte is initialized to 00 for words 1 to 49. The displayed error position byte is initialized to 00 for word 1 of each block and to 08 for words 2 through 49 of each block.

7) Format for blocks 1 through 8 is initialized to 00 (BC-to-RT transfer). In addition, word count is initialized to 32, intermessage gap time is initialized to 7 us and response time to 8 us for blocks 1 through 8.

8) The RT address is initialized to D (disabled) for all eight message blocks.

9) Channel A is initialized as the active bus channel.

10) Relative Transmitter Amplitude is initialized to 171, or approximately 6.5 Vpp, direct coupled.

11) Halt-on-Error is initialized with a value of 00, or disabled.

12) Response Timeout is initialized to 15 us.

13) Exerciser Trigger Mode is initialized to "Internal".

2.9 DISCUSSION OF EXERCISER OPERATION

2.9.1 BACKGROUND INFORMATION

2.9.1.1 LOCAL/REMOTE CONTROL SOURCE

The Exerciser is controlled by one of four sources:

1) Front Panel Keyboard
2) Eight-bit Tri-State Parallel I/O Interface
3) IEEE-488 (GPIB) Interface
4) RS-232 Interface

As mentioned previously, the instrument is under control of the keyboard (local control source) following power turn-on. The instrument remains in local control mode until a command is received by the selected I/O source as described in paragraph 2.6.

The Exerciser is fully controllable by means of any of the four sources. Therefore, the remainder of the discussion in this paragraph (2.9) applies equally for all four sources.

2.9.1.2 EXERCISER MODES

The Exerciser functions in two principal modes of operation: BC and Multi-RT simulator.

As BC, the Exerciser can store and process up to eight independently programmed messages at a given time. As RT, it can simulate up to eight terminal units. The eight terminals may each have separate addresses. Alternatively, the same RT address/T-R bit combination may be programmed to reside in any number (up to eight) of separate Exerciser memory blocks, by means of the block linking feature.

An auxiliary mode of operation involves self-test. In addition to the built-in-self-test software routine, there is a self-test format that is supported in the BC mode. Using this format, the instrument may be programmed to perform a continuous internal wraparound test of its 1553 front end components. This mode is useful for troubleshooting of the Exerciser.

2.9.1.3 SINGLE/REPEAT/HALT-ON-ERROR OPERATION

The user may select from among single and repeat (continuous) modes of Exerciser operation. For BC mode, there is the added option of repeat mode with halt-on-error capability.

In both single and repeat modes, the Exerciser starts transmitting (BC mode), or goes on-line (RT mode), following reception of a GO command.

In single BC mode, the Exerciser processes the programmed frame (from one to eight messages) one time and then halts (goes off-line).

In Repeat BC mode without Halt-On-Error, the instrument repeats the programmed frame of messages until it receives a Halt command. At this time, it will complete the current frame before going off-line.

In the Halt-On-Error Repeat BC mode, the Exerciser will continuously process the programmed frame of messages until a specified number of erroneous frames has occurred. A message frame is considered erroneous if one or more of the following error conditions has occurred:

1) A reply timeout: this indicates that an external RT device has not responded in the specified time, programmable from 5 to 32 us. An external RT response time of less than 4 us (MIL-STD-1553B definition) will also result in a reply timeout error condition.

2) A message error condition has occurred: this indicates either an erroneous word has been received (Manchester, parity, bit count or sync error), a word count error or a format error.

3) A transmitter timeout condition has occurred: this indicates that there was continuous bus activity for longer than 800 us.

Halt-On-Error is a programmable parameter that assumes a value in the range from 0 to 99. The default value of zero (0) directs the Exerciser, when in Repeat BC mode, to run continuously regardless of the number of errors that occur. Programming a number between 1 and 99 configures the Exerciser to halt following processing of the specified number of erroneous frames.

In single RT mode, the Exerciser stays on-line until it processes the specified number of messages containing command words with any of its programmed RT addresses. Similar to BC mode, the number of messages is programmable by means of the Message Count, or Blocks per Frame parameter. It will respond as programmed to each such message and then halt (go off-line). The Exerciser can still be forced to go off-line by means of a halt command, if the specified number of command words containing any of the programmed addresses is not recognized.

In repeat RT mode, the Exerciser stays on-line indefinitely until the reception of a halt command. During this time, it will respond to any and all commands that incorporate any of its programmed RT addresses.

It should be noted that for both the BC and RT Repeat modes, the individual memory blocks of the message RAM are continually overwritten each time a message is repeated. That is, when the block is read following the message processing, only the results from the **last** time that data was received for the particular block will be resident in memory.

2.9.1.4 MESSAGE BLOCKS

As discussed in paragraph 2.7, the Exerciser message RAM is divided into eight blocks.

In BC mode, each message block is used to store the transmitted and received words for an individual message. In this mode, the number of active blocks is specified by the Blocks per Frame, or Message Count parameter. The active blocks will be blocks 1, 2,...N where N is the currently programmed value of message count.

That is, when the instrument is in the Go (execute) state, message 1 will be processed first, followed by message 2, 3 . . ., etc.

In RT mode, the value of the message count parameter has no bearing on the order that message blocks are processed. Instead, each block may be programmed to simulate a separate RT unit. The first digit of the RT address parameter is programmed as either E or d for each of blocks 1 through 8 (see paragraph 2.9.3.1). d indicates that the respective block is disabled as an RT; that is, no data transfers will be transacted between locations in this block and the 1553 bus, regardless of the RT address in the received command word. E indicates that the particular block is enabled as an RT. L indicates that the current block has been linked to from another block. In either case (E or L), the last four digits of the RT Address parameter indicate:

1) Whether the block is configured as a Transmitting (T) or Receiving (R) terminal,

2) The 2-digit decimal (between 0 and 31) address of the simulated terminal. It should be noted that when two or more message blocks are programmed as enabled for the same combination of T/R bit and address, the Exerciser firmware will default such that the RT in question will be simulated by the **lowest** numbered block in the group.

3) The last digit of the RT address represents the "link" parameter. That is, it indicates which of the eight data blocks will be used to transfer data to (or from) the **next** time that the respective RT address/T-R bit combination is addressed following the processing of the current message block. The value of the "linked to" field may be specified to be the same block number (default), a different block number, or disabled. See paragraph 2.9.3 for a further explanation of RT block linking.

2.9.1.5 FORMAT AND DATA WORD COUNT

Structure of a 1553 bus message is specified by two parameters: format and data word count. Format specifies which devices transmit and receive words over the bus, the sequence of such transfers and their timing relationships. Data word count specifies the number of data words to be transferred in the specified direction.

The various message formats are defined in paragraph 4.3.3.6 of MIL-STD-1553B. These formats include BC-to-RT transfer, RT-to-BC transfer, RT-to-RT transfer, mode code and broadcast. There are also messages taking the form of RT-to-RTs broadcast transfers.

In addition to all of the legal transfer formats by the standard, the Exerciser also supports an erroneous format designated as "T/R bit reversal" as well as a self-test format, used for internal diagnostics. With the exception of the self-test format which applies to BC mode only, all of the possible formats are implemented for both BC and RT modes. The BC formats are delineated in detail in paragraph 2.9.2.2. The RT formats are discussed in paragraph 2.9.3.4.

The value of the format parameter is a 2-digit hex byte. As discussed further in paragraphs 2.9.2 and 2.9.3, this byte is encoded slightly differently for

the high-speed and DMA remote I/O commands than it is for the keyboard and low-speed remote operations. The format byte is defined in Table 2-8 as follows:

Table 2-8. Format Byte Definition

BIT VALUE (HEX)	80 40	20	10	08	04	02	01
Bit Meaning	Not Used	Self-Test	*** T/$\overline{R}$ Reversal Error Bit	Broadcast	Mode Code	Information Transfer Format (See Below)	

"01" bit	"02" bit	Format for BC Mode	Format for RT Mode
0	0	BC-to-RT or RT-to-BC transfer*	BC-to-RT or RT-to-BC transfer**
0	1	RT-to-RT tranfer; Exerciser simulates BC only	RT-to-RT transfer; Exerciser simulates transmitting RT only
1	0	RT-to-RT transfer; Exerciser simulates BC and transmitting RT	RT-to-RT transfer; Exerciser simulates both transmitting RT and receiving RT
1	1	RT-to-RT transfer; Exerciser simulates BC and receiving RT	RT-to-RT transfer; Exerciser simulates receiving RT only

*BC-to-RT transfer for T/$\overline{R}$ bit of command word = 0
RT-to-BC transfer for T/$\overline{R}$ bit of command word = 1

**BC-to-RT transfer for T/$\overline{R}$ bit of RT address = R(0)
RT-to-BC transfer for T/$\overline{R}$ bit of RT address = T(1)

***When specifying format by means of a high-speed or DMA input command (via the control word mechanism per paragraph 2.11.4), the 10 bit of the format byte is defined as the T/$\overline{R}$ bit rather than as the T/$\overline{R}$ reversal bit, as it is defined for keyboard and low-speed remote I/O operation.

Please note:

1) The T/R-Bit reversal format (10 bit for keyboard/low-speed operation) is defined as follows: if this bit is set, for BC mode, a message containing a transmit command word assumes the erroneous format of a BC-to-RT transfer. Likewise, a message containing a receive command would assume the erroneous format of an RT-to-BC transfer. The situation is similar for a "10" format in RT mode, with the difference being that the T/$\overline{R}$ bit is decoded from the 5-digit RT Address parameter rather than from the programmed command word.

2) The self-test, or 20 format is relevant only for message block 1 in BC mode. In this format, which is employed in the instrument self-test routine, the Exerciser operates in an internal wraparound mode. That is, the transmitter is inhibited and the decoder input is switched to the output of the encoder, rather than to the receiver. No response from an external device is anticipated and the last transmitted word received by the decoder is stored in the next word location in the memory block. An example of how to use the self-test format is as follows: program word 1 of block 1 to 0821 (RT 1 receive 1 data word). Program any arbitrary test word as word 2. Process the message. The received (decoded) version of the test word will appear in the word 3 position of block 1.

The value of the Word Count parameter (number of data words) for each of the eight message blocks is initialized to 32 at power turn-on or following either a Self-Test or a remote Initialization command. It is updated as follows:

1) By means of a Word Count command.

2) A change in either word 1 of the block (the first command word) or the format byte will cause the word count for the respective block to be updated per the following definition:

If the mode code bit, the 04 bit of the format byte is not set, then the word count updates to the normal word count equal to the number between 1 and 32 indicated by the lower five bits of word 1 of the block (word count/mode code field), with binary 00000 taken to denote a word count of 32. If the 04 (mode code) bit of the format byte is set, then the word count updates to either 0 or 1 per the "10" bit of the second byte (fifth LSB) of word 1 of the block. It should be noted that this definition of word count is fully in agreement with MIL-STD-1533B. If the Exerciser is used in a MIL-STD-1553A application, the Exerciser's normal word count for some mode codes will have to be overridden by means of a Word Count command to comply with MIL-STD-1553A.

It should also be noted that for BC mode, the normal word count may always be changed to an erroneous value by means of the WORD COUNT command. In addition, for RT mode, word count must be specified. If it is not, it will default to its previously defined value. It should also be noted that for RT mode, word count should always be specified **after** both the Format and RT Address parameters have been programmed for the respective message block. If this sequence is not followed, an erroneous data word count, corresponding to the word count field of the command word in location 1 of the block, may possibly result.

2.9.1.6 TIMERS: FRAME, RESPONSE, INTERMESSAGE GAP AND FAIL-SAFE

2.9.1.6.1 FRAME TIME

This parameter is relevant for Repeat BC mode only. It defines the overall repetition time for the frame of messages being processed. That is, it defines the overall time window between consecutive start-of-transmission times for message 1. See Figure 2-7.

Frame Time is programmable from 2 to 500 ms in 1 ms steps with a power turn-on value of 10 ms. It should be noted that if the programmed Message Count is greater than two, the actual frame time implemented by the Exerciser will never fall below

1 ms per message block. For example, if message count is programmed to five and frame time is programmed to 2 ms, the frame time in response to an interrogation will indicate 2 ms, even though the implemented time will be 5 ms.

It should also be noted that when processing a message frame sequence in external trigger repeat BC mode, the implemented frame time will, in general, be greater than the programmed frame time. The additional time is required to allow the Exerciser to synchronize with its external trigger input signal.

2.9.1.6.2 RESPONSE TIME

There are three response timers in the Exerciser.

One timer verifies that the response time of an external RT device is less than the user-specified value of response timeout, as programmed by the Timeout parameter. Timeout is programmable over the range from 5 to 32 us, as defined by MIL-STD-1553B. This definition is shown in Figure 2-5.

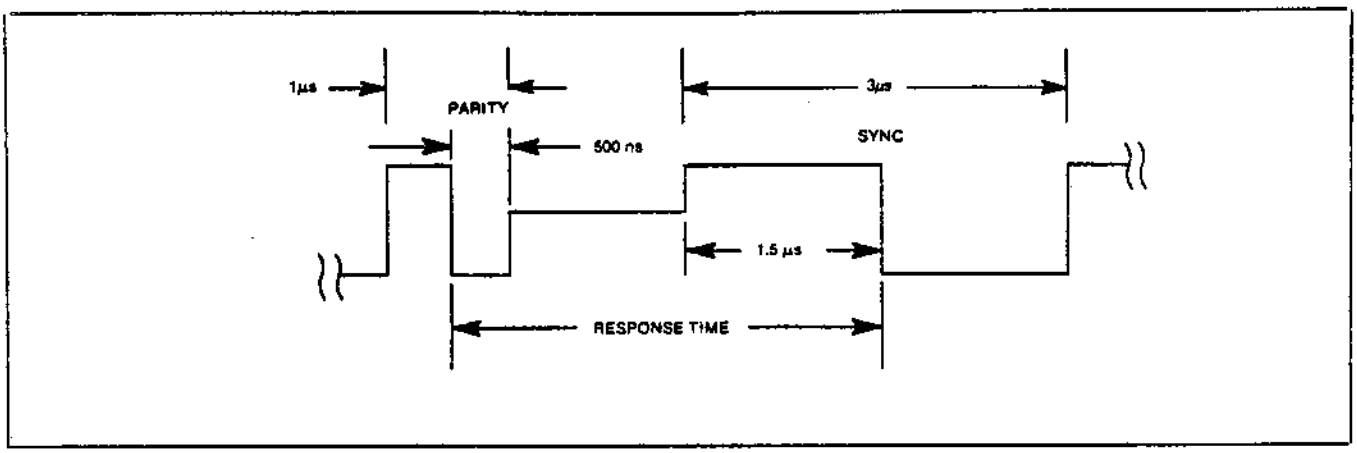


Figure 2-5. Response Time Definition (MIL-STD-1553B)

As indicated, response time per MIL-STD-1553B is defined as the time between the mid-parity zero crossing of the last word transmitted by one device (usually the BC) and the mid-sync zero crossing for the status word of the responding RT.

For MIL-STD-1553A applications, response time is defined as the true gap in transmission, resulting in a response time 2 us less than the corresponding time for MIL-STD-1553B applications. For MIL-STD-1553A applications, the effective range for timeout is therefore 3 to 29 us.

If an external RT responds later than the programmed value of timeout or does not respond, the Exerciser no response timer will timeout, resulting in:

1) The REPLY T/OUT LED on the instrument front panel illuminating, and,
2) The "Direction" digit of the anticipated RT status word (and subsequent data words, if any) will indicate P (pending received), rather than R (received).

The power turn-on value for Timeout is 15 us.

In addition, there is another timer that checks for early response errors. This timer verifies that the response time for an external RT is greater than the minimum allowable time of 4 us (per MIL-STD-1553B), or 2 us (MIL-STD-1553A definition). An Early Response error is flagged with a hex word error code of 20 for received words via either the front panel or any of the remote interfaces. Also, for an early response error, the REPLY T/OUT LED on the front panel illuminates.

The third response timer is used to vary the programmed response time for situations where the Exerciser is simulating an RT device. The response time is independently programmable for each of the eight message blocks with a range of 5 to 31 us for BC mode or 6 to 31 us for RT mode, in 1 us steps, with a power turn-on value of 5 us. It should be noted that the maximum allowable response time per MIL-STD-1553B is 12 us. Programmable RT response time is applicable for BC formats 2, 3 and A as well as for RT mode.

2.9.1.6.3 INTERMESSAGE GAP TIME

Like frame time, intermessage gap time is relevant for BC mode only.

Similar to response time, intermessage gap time is defined per MIL-STD-1553B as being the time between the zero crossing of the parity bit of the last word of one message to the mid-sync zero crossing of the (first) command word of the next message. (See Figure 2-5.) It should be noted that for the Exerciser, intermessage gap time for a particular message block (each block has its own independently programmable intermessage gap) refers to the time delay **preceding** the start of the block. For example, the intermessage gap for block 2 is the mid-parity to mid-sync time between message 1 and message 2, in microseconds.

Intermessage gap is programmable from 7 to 2047 us per MIL-STD-1553B in 1 us steps with a power turn-on value of 7 us. The wide range for intermessage gap time allows the channel A to channel B delay time to be swept over a large range for performing the Bus Switching test for dual redundancy.

2.9.1.6.4 TRANSMITTER TIMEOUT

This timer provides an indication, via the XMTR T/OUT LED that there is activity on the bus for a period of 800 us or longer. Bus activity is continuously monitored by this timer or by determining whenever the LINE ACTIVE output of the Exerciser decoder is asserted continuous for a time interval of 800 us or more (800 us is the FAILSAFE time interval specified by MIL-STD-1553B). It should be noted that the bus activity causing this fault may originate from either the Exerciser or an external bus device on the bus.

2.9.1.7 WORD AND MESSAGE ERRORS

The Exerciser is capable of generating and detecting a wide repertoire of word errors and message errors.

The possible word errors that may be induced are: Manchester encoding error in any data bit position and/or the parity bit, parity logic sense error, high bit count, low bit count, sync field errors, incorrect sync type, word gap, message gap and zero-crossing deviation.

The generated errors for transmitted words are specified by the programming of the Error and Error Position bytes for each respective word. These are expanded in Table 2-9, indicating the precise bit assignments for all of the possible induced word error conditions.

By setting the appropriate bit(s) in the error and error modifier bytes, it is possible to program none, any or various combinations of induced error types for any transmitted word in any message. Specifying an error byte of 00 will result in a correct word being transmitted.

It is possible to program word errors for any number of transmitted words in a message. It should be noted that the 80 bits of both the error and error modifier bytes cannot be user programmed via the keyboard and are masked to 0 for purposes of front panel viewing. These bits, which are used to distinguish between transmitted, pending and received words, are accessible by means of the remote I/O commands as discussed in paragraph 2.11. Refer to Table 2-7.

Examples of the various errors for transmitted words are shown in Figure 2-6.

Programming of a Manchester encoding error results in the bit pulse for the specified bit position to take the form of a 1 us logic 0 pulse on the bus, if the bit is specified as a logic 0. The normal Manchester representation for a logic 0 is a 500 ns low level followed by a 500 ns logic high level pulse. Likewise, a Manchester encoding error specified for a bit that is programmed as a logic 1 will result in a 1 us high level pulse on the bus.

By means of the Manchester or zero-crossing error position bits, M/ZCEP3 (MSB) through M/ZCEP0 (LSB) of the error modifier byte, a Manchester encoding error may be selected to occur in any of the 16 bit positions. As shown in Figure 2-6, bit 1 is taken to be the first bit transmitted,. . . bit 16 is taken to be the last data bit transmitted, followed by the parity bit. Assuming that the Manchester encoding error bit (04 bit) of the error byte is set to logic 1 and the error type select bit (40 bit) of the error modifier byte is set to zero, the bit position of the encoding error (1 through 16) will be one (1) **plus** the hex number (0 to 15) defined by M/ZCEP3 through M/ZCEP0. For example, if M/ZCEP3 through M/ZCEP0 = 0101 (binary) = 5, the encoding error will occur in the sixth bit position.

A Manchester encoding error may be caused to occur in the parity bit position by setting the PARITY MANCHESTER ENCODING ERROR bit (20 bit) of the error byte.

Programming a HIGH BIT COUNT ERROR (error byte 01 with error modifier byte 00) results in one extra bit pulse (with logic sense 1) to be transmited at the end of the word. Programming an error byte of 01 with an error modifier byte of 10 results in a word with two additional logic 1 bit pulses.

Programming a LOW BIT COUNT ERROR (error byte 02 with error modifier byte 00) results in one bit position, the parity bit, to be missing.

Programming a parity error (08 bit) results in the parity bit, which normally yields odd parity for the word, to be transmitted with its logic sense inverted.

The SYNC ERROR bit (10 bit) of the error byte works in conjunction with the sync error position bits (20, 10) of the error modifier byte to induce various sync field errors, as shown in Table 2-9 and Figure 2-6.

Table 2-9. Transmitted Word Induced Error Encoding

INDUCED WORD ERROR CONDITION	ERROR BYTE (HEX)							ERROR MODIFIER BYTE (HEX)						
	40	20	10	08	04	02	01	40	20	10	08	04	02	01
Normal Word (No Errors)	0	0	0	0	0	0	0	x	x	x	x	x	x	x
Long Word: 1 extra bit	0	0	0	0	0	0	1	0	x	0	x	x	x	x
Long Word: 2 extra bits	0	0	0	0	0	0	1	0	x	1	x	x	x	x
Short Word: 1 missing bit	0	0	0	0	0	1	0	0	x	x	x	x	x	x
Manchester encoding error in specified data bit position	0	0	0	0	1	0	0	0	x	x	(MEP-1)*			
Parity Error 0	0	0	1	0	0	0	x	x	x	x	x	x	x	
Sync Error: 110000 (C); 001111 (D)	0	0	1	0	0	0	0	x	0	0	x	x	x	x
Sync Error: 111100 (C); 000011 (D)	0	0	1	0	0	0	0	x	0	1	x	x	x	x
Sync Error: 011000 (C); 000110 (D)	0	0	1	0	0	0	0	x	1	0	x	x	x	x
Sync Error: 111001 (C); 100111 (D)	0	1	0	0	0	0	0	x	1	1	x	x	x	x
Manchester encoding error in parity bit position	0	1	0	0	0	0	0	x	x	x	x	x	x	x
Inverted sync type error	1	0	0	0	0	0	0	x	x	x	x	x	x	x
Word gap error: 1 us gap between 8th and 9th data bits	0	0	0	0	0	0	1	1	x	x	x	x	x	x
Message gap error: 2 us gap between current word and next word	0	0	0	0	0	1	0	1	x	x	x	x	x	x
Zero-crossing Deviation 187.5 ns Early	0	0	0	0	1	0	0	1	0	0	(ZCDEP-1)*			
Error in First half 125 ns Early	0	0	0	0	1	0	0	1	0	1				
Of specified Bit Time 125 ns Late	0	0	0	0	1	0	0	1	1	0				
187.5 ns Late	0	0	0	0	1	0	0	1	1	1				

Notes: (1) * Indicates that the Manchester encoding error or zero-crossing deviation error will occur in the data bit position (1-16) as one **greater** than the number indicated by the sum of the 08, 04, 02, 01 bits (0-15) of the Error Modifier byte.

(2) X indicates don't care.

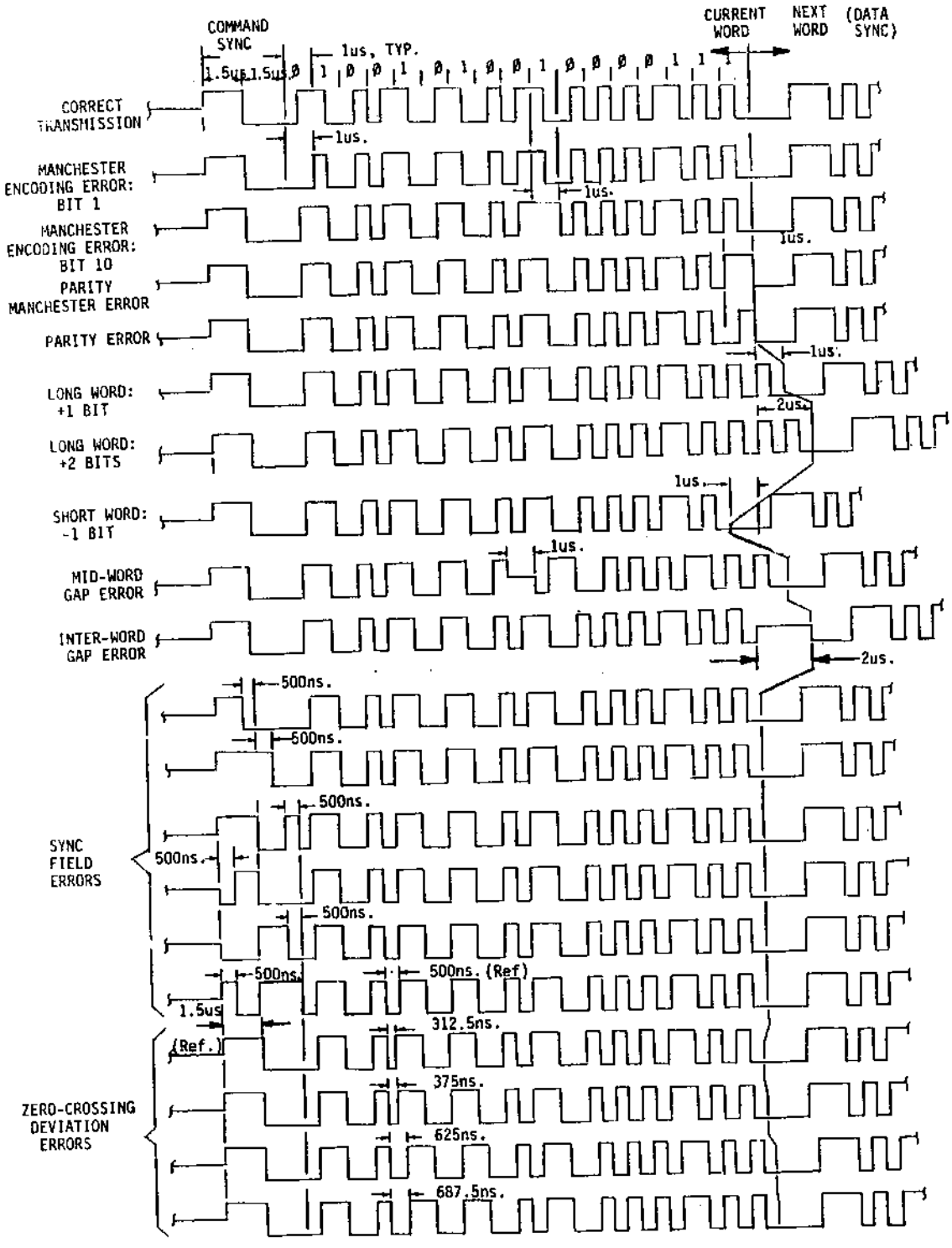


Figure 2-6. Induced Word Error Conditions

The Incorrect Sync Type bit causes a reversal in the logic sense of the sync pulse. That is, if the position of the word in the message dictates that it contain a command/status type of sync, the word will contain a data sync. Likewise, if the word is in a data word position of a message, it will contain a command/status sync pulse.

A Word Gap error inserts a 1 us gap (bus dead time) between the eighth and ninth data bits of the respective word.

An Message Gap error inserts a 2 us gap (bus dead time) between the end of the current word and the start of the next word to be transmitted.

Zero-Crossing Deviation errors are implemented as follows: the time interval from the start of the data bit time to the mid-bit zero-crossing, which is specified to be 500 +/- 25 ns (per MIL-STD-1553B), may be varied to be 312.5, 375, 625 or 687.5 ns. By means of the Manchester/Zero-Crossing Deviation bit position bits of the error modifier (fourth) byte, the Zero-Crossing error may be programmed to occur in any of the 16 data bit positions. The coding for the zero-crossing error bit positioning is identical to that for Manchester encoding errors.

The Exerciser can detect a similar repertoire of errors for received words. The detected error and receive verification/sync type bytes for keyboard and low speed I/O operations are found in Table 2-6.

As with transmitted words, the 80 bits of these bytes are encoded to distinguish between transmitted, pending and received words.

The four word encoding error bits of the detected error byte: Parity Error, Manchester Encoding Error, Low and High Bit Count errors often occur in combination with each other for erroneous received words. This is due to the action of the error-detecting decoder. The decoder response to erroneous words is dependent on the previous word as well as the logic sense of sync and data bits. For example, in response to a low bit count error, it is conceivable for both the Low Bit Count Error and Parity Error bits to be set.

The Message Error bit (10 bit) of the detected error byte is set under either of two conditions:

1) A word error has occurred in the present or any previous received word of a message frame.

2) A high or low received word count condition has been detected. The Message Error bit will be set for the first extra word (for a high word count) and for all subsequent words of the current message frame (BC mode) or current message (RT mode).

The Incorrect Sync Type error is similar to that for transmitted words. It indicates that a data sync was detected for a command or status word, or vice versa.

A received word with an error in the sync field, such as a shifted zero crossing, will generally be ignored by the Exerciser.

In addition to word errors, the Exerciser is capable of generating a number of message type errors. For example, it is possible to induce either a long or short message length by altering the data word count by means of a word count command. Word count is variable from 0 to 45 data words. If the transmitted word count is greater than 40, a fail-safe fault will occur, causing the XMTR T/OUT LED on the front panel to illuminate.

Other examples of programmable message errors include:

1) Invoking a "10" format. This results in an erroneous message whose format is reversed from what the T/R bit in the command word (BC mode) or RT address (RT mode) indicates.
2) Programming an RT response time of greater than 12 us (per MIL-STD-1553B) in either BC mode (formats 02, 03, 0A) or RT mode.
3) Disabling the appropriate RT address in RT mode will result in a no response error.
4) An incorrect sync type word error may also be considered a format error.
5) An RT status word may be programmed to contain an incorrect RT address.

The Exerciser can also detect message or format type errors. A few examples of these are:

1) A no response, late response, or early response condition will result in the REPLY T/OUT LED illuminating. In addition, for the case of non-received words, the "Direction" (DIR) indication for the anticipated received status word will be "P" rather than "R". All words received following a gap of less than 4 us (per MIL-STD-1553B) will be flagged with a hex error code of 20.
2) A low word count condition will result in the BUS FAULT LED illuminating and a "P" direction indication for the missing words.
3) A high word count condition will result in the BUS FAULT LED illuminating and the Message Error bit (10 bit) to be set for the extra words and subsequent words in the message frame. In addition, if the Exerciser senses continuous bus activity for greater than 800 us, the XMTR T/OUT LED will illuminate.
4) The BUS FAULT LED will illuminate in response to any word error in the received portion of a message, or a high received word count.

2.9.1.8 TRANSMISSION AMPLITUDE ADJUSTMENT

Transmitter amplitude is programmable by means of either the front panel keyboard or any of the three remote I/O ports. Relative transmitter amplitude is programmable via an internal 8-bit D/A converter. Its value may be specified to be in the range from 0 to 255, corresponding to an approximate range of zero to 9.75 Vpp direct coupled across 35 ohms, or 0 to 30 Vpp transformer coupled (open-circuit).

2.9.1.9 ACTIVE CHANNEL SELECTION

Internally, the Exerciser is a single channel instrument. The selection of Channel A or Channel B as the active bus channel provides for quasi-dual redundancy. This is implemented by means of an internal 2-pole relay, illustrated in Figure 2-2. The active channel selection may be made by means of either the front panel keyboard or any of the three remote I/O ports.

2.9.2 BUS CONTROLLER

2.9.2.1 OVERALL TIMING

Figure 2-7 illustrates the typical timing for the Exerciser's BC mode of operation.

As indicated in the diagram, the frame time is the overall repetition time between the individual starting times for message 1. It is also shown that the intermessage gap time, defined by MIL-STD-1553B as being the mid-parity to mid-sync time between the end of message 1 and the start of message 2 is the gap time programmed for message block 2, rather than message block 1.

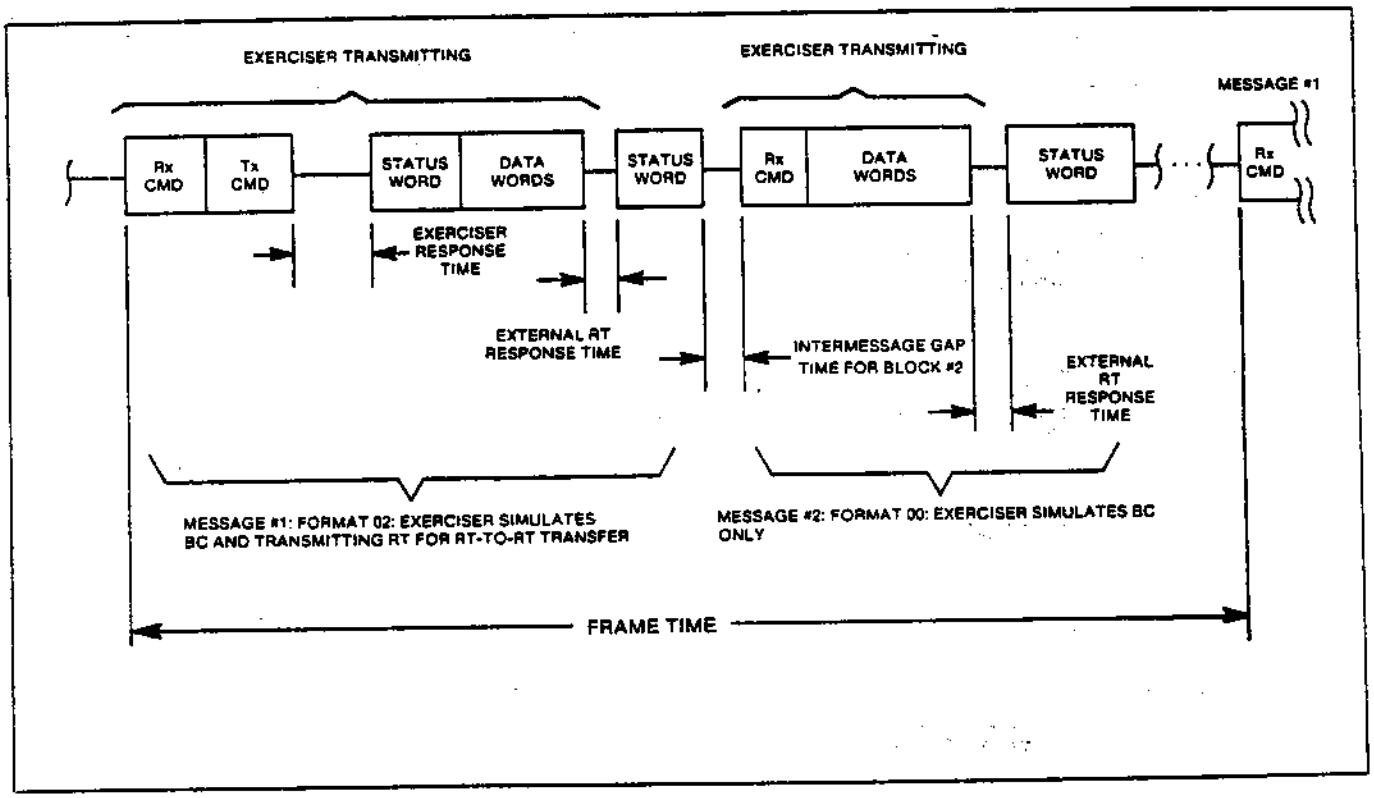


Figure 2-7. Timing Diagram for Exerciser BC Operation

In addition, it should be noted that the response time preceding the transmitting RT's status word for message 1 is the delay period specified by the **Exerciser's** programmed response time for block 1. This is because for RT-to-RT transfer format 02, the Exerciser simulates the activity of the transmitting RT as well as the BC. The two other response times indicated on the diagram arise from external RTs. The Exerciser verifies that these times are greater than 4 us (per MIL-STD-1553B) and less than the programmed value of response Timeout.

2.9.2.2 BC FORMATS

Paragraph 2.9.1.5 discussed a general overview of the Exerciser message formats. Table 2-10 illustrates in detail the Exerciser formats for BC operation. For the format diagrams, N refers to the data word count discussed in paragraph 2.9.1.5. As noted in Table 2-10, for some of the formats, the parameter designation varies between the keyboard low-speed and the high-speed/DMA remote I/O operations.

Table 2-10. BC Formats

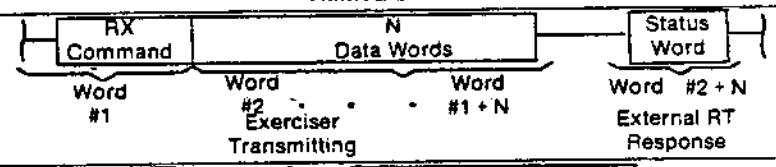
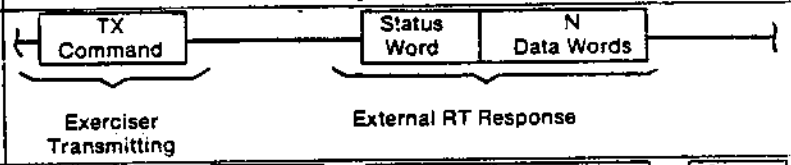
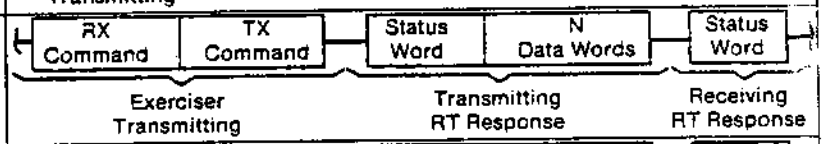
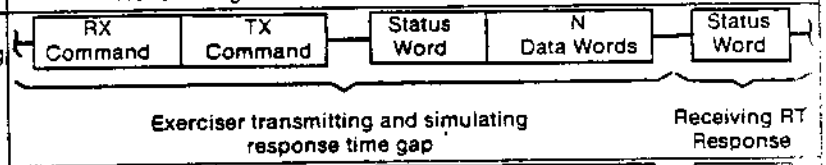
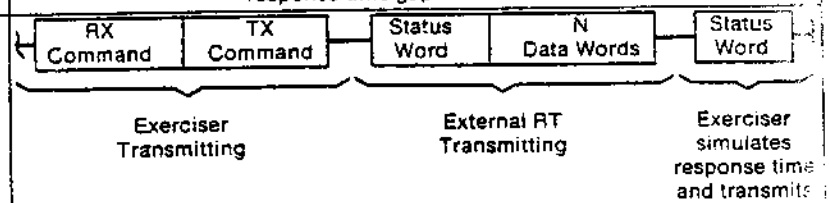
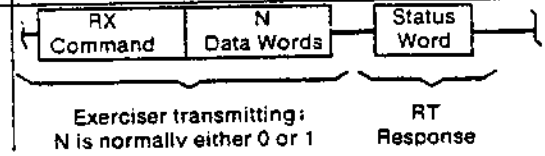
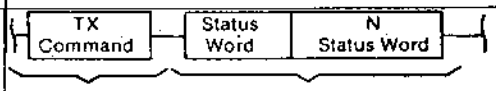
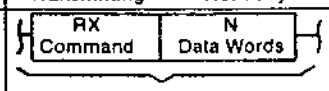
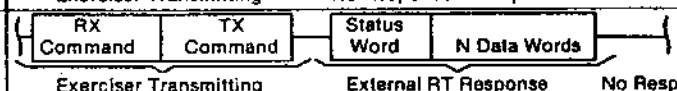
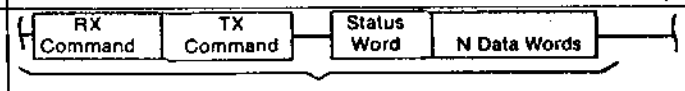
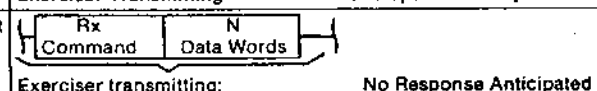
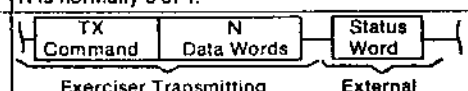
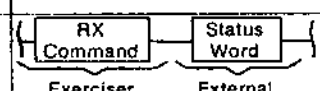
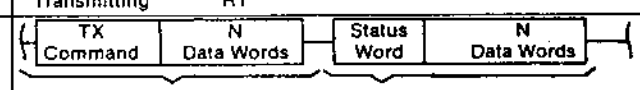
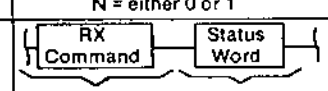
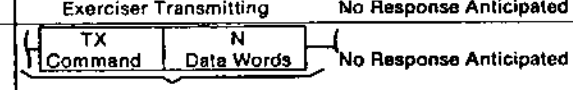
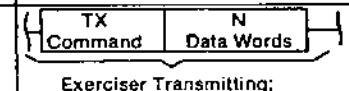
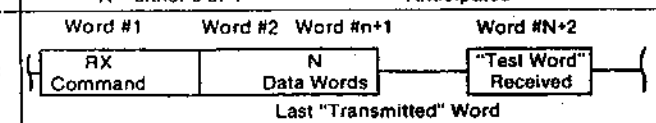
KEYBOARD LOW-SPEED I/O FORMAT	HIGH-SPEED/ DMA REMOTE I/O FORMAT	DESCRIPTION	TIMING DIAGRAM
00, and T/R bit in Command Word = 0	00	**BC-to-RT Transfer**	
00, and T/R bit in Command Word = 1	10	**RT-to-BC Transfer**	
01	01	**RT-to-RT Transfer; Exerciser simulates BC only**	
02	02	**RT-to-RT Transfer; Exerciser simulated BC and transmitting RT**	
03	03	**RT-to-RT Transfer, Exerciser simulates both BC and receiving RT**	
04 T/R Bit of Command Word = 0	04	**"Receive" Mode Code Command**	

Table 2-10. BC Formats - cont.

KEYBOARD LOW-SPEED I/O FORMAT	HIGH-SPEED/ DMA REMOTE I/O FORMAT	DESCRIPTION	TIMING DIAGRAM
04; T/R Bit of Command Word = 1	14	"Transmit" Mode Code Command	
"08"; T/R Bit of Command Word = 0	08	Broadcast Receive Command	
09, 0B	09, 0B	Broadcast RT-to-RT, Simulating BC only	
0A	0A	Broadcast RT-to-RT, Simulating BC and Transmitting RT	
08 T/R Bit of Command Word = 1	18	"Transmit" Broadcast Command (Erroneous)	
0C	0C	Broadcast/Mode Code Format	
10; T/R Bit of Command Word = 1	00	"T/R Reversal" Format Error; Transmit Command	
10; T/R Bit of Command Word = 0	10	"T/R Rversal" Format error; Receive Command	
14; T/R Bit of Mode Code Command Word = 1	04	Mode Code Command with "T/R Reversal" formal error; Transmit Command	
14; T/R Bit of Mode Code Command Word = 0	14	Mode Code Command with "T/R Reversal" format error; Receive command	
18; T/R Bit of Command Word = 0	18	"T/R Reversal" Error: Receive Broadcast Command	
18; T/R Bit of Word = 1	08	"T/R Reversal" Error: Transmit Broadcast Command	
1C	1C	Broadcast/Mode Code Command with "T/R Reversal" Error.	
20	20	Self-Test "Wraparound" Format. This format is applicable for message block #1 only.	 In the "Self-Test" format, the Exerciser does not transmit on the -1553 bus, but rather enables the encoder to send directly to the decoder. The last "transmitted" word is received and stored in location "N+2" of the message block.

2.9.2.3 DEFAULT RT STATUS WORD FOR BC MODE

As a means of minimizing number of keystrokes or host computer software coding required to program the Exerciser, the instrument's internal firmware assigns a default value to RT status words, wherever possible.

The default value for the assigned status words is Clear Status. That is, the status words will be comprised of the respective (programmed) terminal address for bit positions 1 through 5, with bit position 6 through 16 (message error, instrumentation, service request, etc.) assigned the value 0.

For BC mode, the default value of Clear Status is assigned for the "Extended" RT-to-RT transfer message formats; that is, for those situations where the Exerciser simulates the action of an RT as well as the BC.

The pre-assigned (default) status word may be overwritten via user command. The user-programmed status word may be valid or may be programmed to contain induced word errors.

For BC mode, the default status word is assigned for formats 02, 03 and 0A as follows:

Table 2-11. Assigned RT Status Words (BC Mode)

FORMAT (LOW-SPEED DESIGNATION)	STATUS WORD RT ADDRESS TAKEN FROM COMMAND WORD ADDRESS FIELD FROM WORD NUMBER:	POSITION IN MESSAGE BLOCK (WORD NUMBER) OF STATUS WORD TO BE ASSIGNED
02	2	3
03	1	4 + N
0A	2	3

N indicates the Word Count parameter for the respective message block.

For BC mode, the status word for the respective message block defaults to its Clear Status default value under the following circumstances:

1) Exerciser operating mode is switched from RT to BC.
2) Whenever the Format parameter for the current message block is updated via keyboard or low-speed command.
3) Whenever the Word Count parameter for the current message block is updated via keyboard or low-speed command.
4) Whenever word 2 for formats 02 and 0A or word 1 for format 03 is updated via keyboard or low-speed command.

2.9.3 RT OPERATION

As discussed above, the Exerciser is capable of simulating up to eight RTs in its RT mode. When the instrument is on-line "BUSY" in the RT mode, it will respond to any and all valid command words containing any of its programmed combinations of RT Address and T/R bit.

2.9.3.1 RT ADDRESS

In RT mode, there is an RT Address parameter associated with each of the eight message blocks. The RT address parameter is comprised of four parts. These are:

1) The first digit either enables (E), disables (D) or links (L) the block in question as an active RT. Unlike BC operation, where contiguous blocks starting with block 1 (i.e. blocks 1,2 ... N) must be activated, any random combination of message blocks may be utilized to simulate RTs. For example, blocks 2, 5 and 7 may be designated as active blocks.

2) The second digit selects either "transmit" (T) or "receive" (R) RT operation for an "enabled" or "linked to" message block. For front panel keyboard operation, 1 (for T) or 0 (for R) must be entered for this digit.

   The designated T/R bit specifies the transmit/receive type of the anticipated, or "trigger" command word for the particular message block. It usually, but not always, indicates that the Exerciser will simulate the action of a transmitting RT if T is specified or a receiving RT if R is specified. This is clarified in the disucssion of RT mode formats in paragraph 2.9.3.4.

3) The third and fourth digits specify the 2-digit (decimal) address of the simulated RT. This must always be entered as two decimal digits with value in the range from 00 to 31. Three additional points to keep in mind when specifying RT address are:

   (i) In order for the Exerciser to respond as an RT, it must recognize the following in the appropriate command word:

   Specified RT Address,
   Specified T/R Bit,
   Command Sync Type,
   Valid word (Sync, Manchester, Parity, Bit Count).

   (ii) It is possible to designate one group of message blocks to simulate a given RT as a transmitter and designate a second group of blocks to simulate the same RT (address) as a receiver.

   (iii) It is also possible to enable (E) two separate blocks to have the identical combination of address and T/R bit. In this situation, the **lower** numbered block becomes the active enabled block. For example, if both block 2 and block 6 are specified (enabled) as RT 27, receiving message data to RT 27 will be stored in memory block 2, but will not be stored in block 6.

4) The fifth digit of RT address represents the value of the "linked to" block. The function of this field is described in detail in paragraph 2.9.3.2.

2.9.3.2 MULTIPLE DATA BLOCKS PER RT ADDRESS VIA RT BLOCK ADDRESS LINKING

The Exerciser's RT mode features a "block linking" capability. This feature allows multiple data blocks to be transmitted or received for the same T/R bit/terminal address combination. Block linking is described as follows:

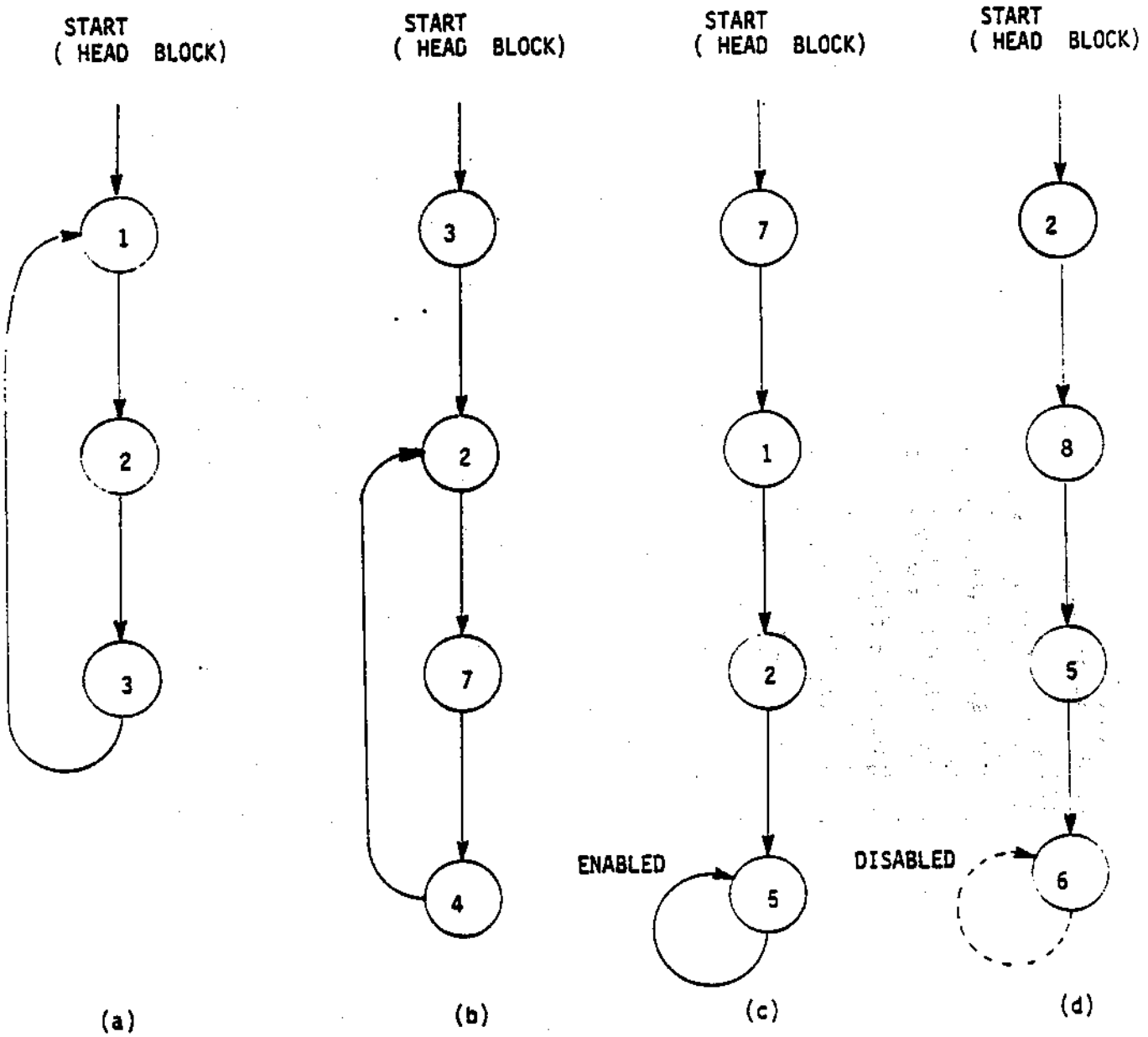
1) Block linking, which is applicable for BC testing and system simulation, provides the capability to receive and store a series of messages directed to a specific RT address in a specified sequence of data blocks. Likewise, it enables the Exerciser to transmit varying blocks of data from the same simulated terminal without keyboard or I/O intervention. The specific sequence of Exerciser block numbers that simulate a given address/T-R bit combination is completely user programmable.

2) For RT mode of the Exerciser, each message block may be specified as either disabled (d), or enabled (E) for a specific address. A third possibility is to be able to (indirectly) specify the block to be "linked" (L). That is, when the "RT Address" parameter for a given block is programmed as Edaa (with d specifying direction (T or R) and aa specifying RT address (0 to 31)), the internal Exerciser firmware designates the enabled (E) block as the "head" block of the chain. In addition, the user has the option of specifying an optional fourth parameter, yielding "Edaan". The "n" field specifies the number of the message block that will be processed the **second** time that a message (command word) is directed to the respective RT address/T-R bit combination. If "n" is not specified, it defaults to the number of the current message block, implying that data will be transmitted from/received to the same memory block each time the respective RT is addressed.

3) The "RT Address" parameter for the "linked to" message block, specified by n, is then automatically updated via the Exerciser firmware to assume the value "Ldaan," where the "daa" field matches that of the linked from block, and n is, initially, the number of the "linked to" block. Also at this time, the RT status word for the linked to block is assigned the value "Clear Status."

4) Similarly, the second "linked" block in the chain may be linked to a third, the third to a fourth, etc. (up to eight) by appending "n" to the respective RT address, yielding Ldaan. By referring to the sequences illustrated in Figure 2-8, it may be seen that it is possible to link any block in the chain to: (1) the first block in the chain, which has address Edaan (Figure 2-8 (a)). This results in a continuous loop. (2) Any arbitrary link in the chain (Figure 2-8 (b)), (3) Itself-enabled (Figure 2-8 (c)), or (4) Itself-disabled (Figure 2-8 (d)). This last feature allows a given RT to respond only a specified number of times (up to eight), before going off-line but still allowing other RTs simulated by the Exerciser to stay on-line. It is implemented by specifying a value of "d" as the "linked to" block field of the "RT Address" parameter.

5) Figure 2-9 indicates an example of RT linking. The three simulated RT addresses are RT 1 (receiving), RT 1 (transmitting), and RT 2 (receiving). The timing diagram at the bottom of the figure illustrates a working example of the RT linking mechanism.



POSSIBLE R.T. LINKING SEQUENCES: (a) Link from last block back to first block: continuous looping; (b) Link from last block to an arbitrary block in link chain ; (c) Link from last block in chain to itself (Enabled); (d) Link from last block in chain to itself (Disabled).

Figure 2-8. Possible RT Linking Sequences

MESSAGE RAM MAP

BLK #	R.T. ADDRESS
1	R.T. #1, RECEIVING
2	R.T. #1, TRANSMITTING
3	R.T. #2, RECEIVING
4	R.T. #1, RECEIVING
5	R.T. #1, RECEIVING
6	R.T. #1, TRANSMITTING
7	NOT USED
8	NOT USED

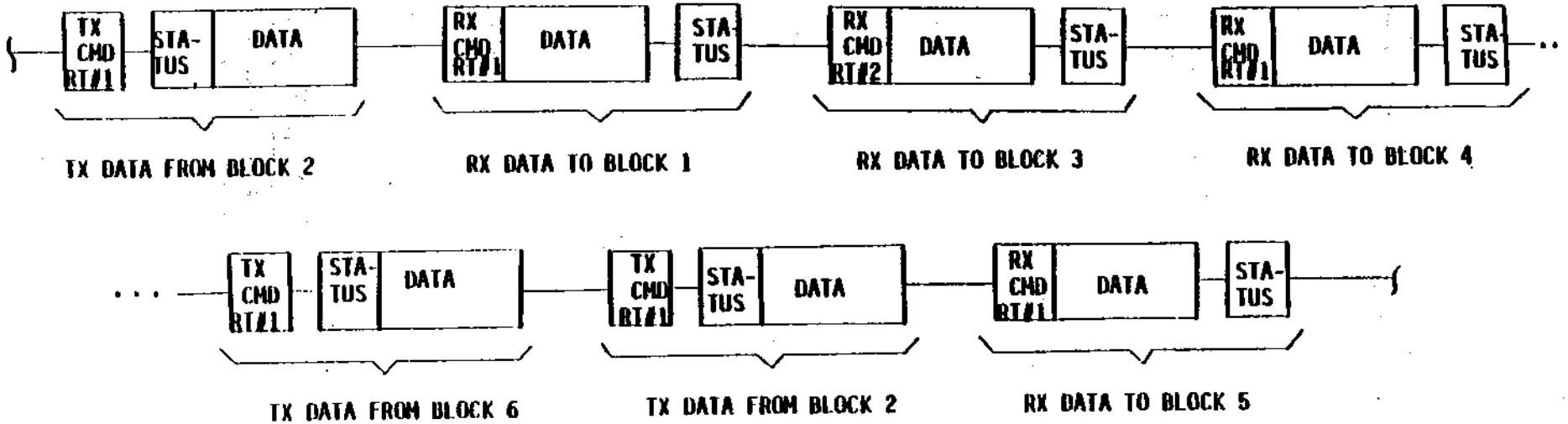


Figure 2-9. Multiple Message RAM Blocks for Emulated RTs (Example)

2.9.3.3 RESPONSE TIME

As described in paragraph 2.9.1.6, the RT response time is programmable from 6 to 31 us in 1 us steps. The response times for each of the eight simulated RTs are independently programmable.

2.9.3.4 WORD COUNT

As discussed in paragraph 2.9.1.5, the data word count is programmable from 1 to 45 for each message block. The maximum word count per the standard is 32.

Unlike the BC mode, there is no "default" or "correct" word count (per command word/format) for the RT mode. Therefore, the number of data words anticipated to be received or transmitted must be specified by the Word Count parameter for each block. If it is not specified, the Word Count will revert back to the previous value resident in memory.

If the Word Count for a particular RT is incorrectly specified, the result will be either a response timeout, a bus crash, an incorrect number of words being transmitted, status and/or data words transmitted at the wrong times, or a combination of these fault conditions. However, word count errors may be intentionally introduced as part of the characterization or acceptance testing of a BC.

As discussed in paragraph 2.9.1.5, Word Count must be specified **after** both format and RT address have been specified for a particular message block in RT mode.

2.9.3.5 RT FORMATS

The RT mode formats are generally similar to the BC mode formats. They are illustrated in detail in Table 2-12. For the diagrams, "N" refers to the word data count, and (*) refers to the position of the RT "trigger" word. The trigger word is the command word containing the RT's programmed address and T/R bit. Similar to the BC mode formats, the parameter designations for "keyboard/low-speed remote I/O" and "high-speed/DMA remote I/O" operations vary for some of the RT mode formats.

2.9.3.6 DEFAULT RT STATUS WORDS

As a means of minimizing the number of user keystrokes and/or software coding required to program the Exerciser, the Exerciser's internal software assigns a default value to all RT Status words, wherever possible.

The default value for the assigned Status words is "Clear Status". That is, the status words will be comprised of the respective (programmed) terminal address for bit positions 1 through 5, with bit positions 6 through 16 (Message Error, Instrumentation, Service Request, etc.) assigned the value 0.

Table 2-12. RT Mode Formats

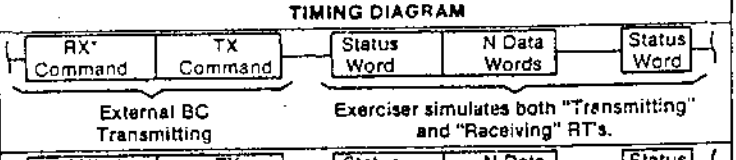
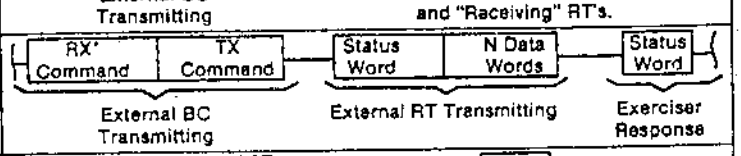
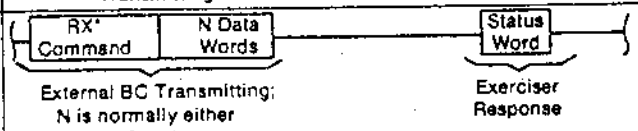
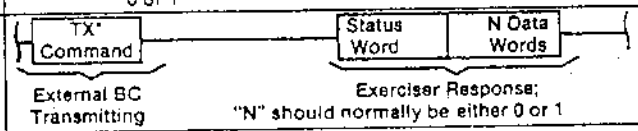
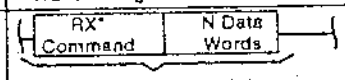
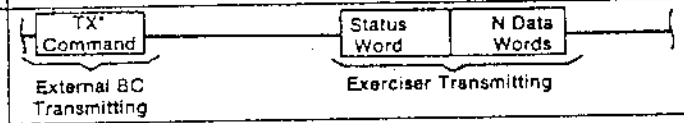
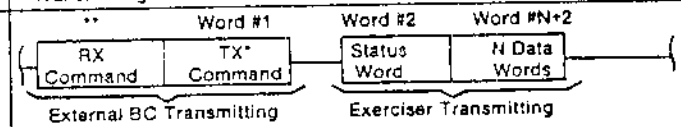
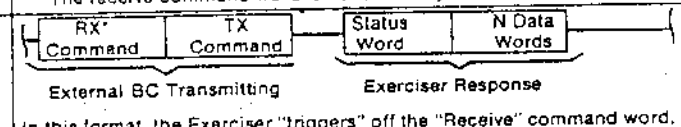
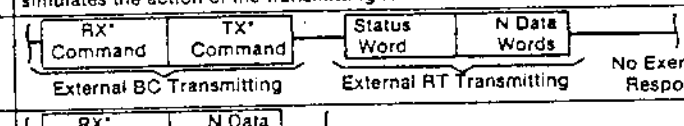
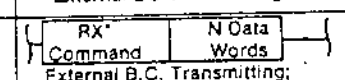
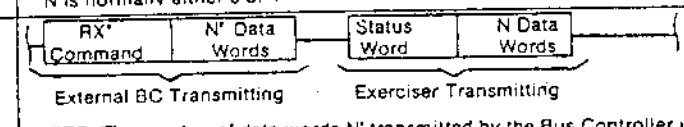
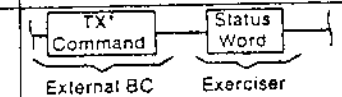
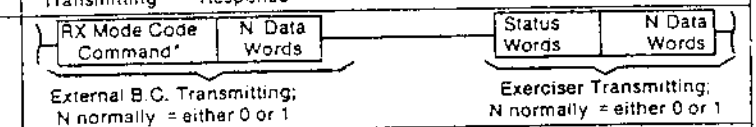
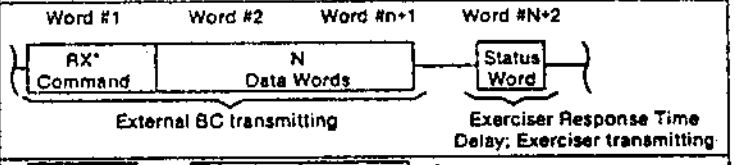
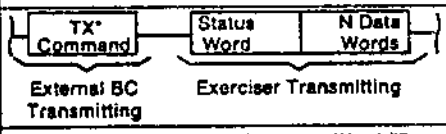
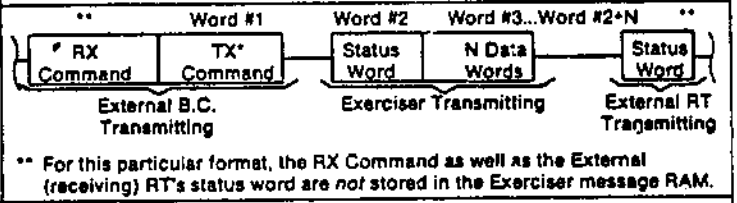
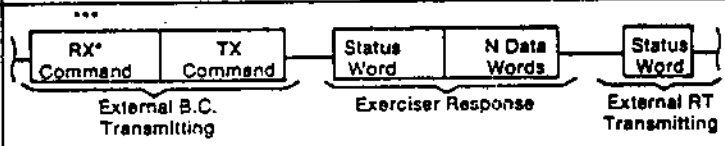
KEYBOARD LOW-SPEED I/O FORMAT	HIGH-SPEED/ DMA REMOTE I/O FORMAT	DESCRIPTION	TIMING DIAGRAM
02	02	RT-to-RT Transfer; Exerciser simulates both transmitting and receiving RT's	
03	03	RT-to-RT Transfer; Exerciser simulates receiving RT only	
04; T/R Bit in "RT Address" = 0	04	"Receive" Mode Code Command	
04; T/R Bit in "RT Address" = 1	14	"Transmit" Mode Code Command	
08; T/R Bit of "RT Address" = 0	08	Broadcast: "Receive" Command	
08; T/R Bit in "RT Address" = 1	18	"Transmit" Broadcast Command (Erroneous)	
08; T/R Bit in "RT Address" = 1	10	"Broadcast RT-to-RT's" Transfer Format; simulating transmitting RT	 ** The receive command word is not stored by the Exerciser for this format.
09, 0A	09, 0A	RT-to-RT's Broadcast; simulating transmitting RT	 In this format, the Exerciser "triggers" off the "Receive" command word, but simulates the action of the transmitting RT.
0B	0B	RT-to-RT's Broadcast; Exerciser simulates (one) Receiving RT	
0C	0C	Broadcast/Mode Code Format	
10; T/R Bit in "RT Address" = 0	10	"T/R Reversal" Error: Receive Command	 NOTE: The number of data words N' transmitted by the Bus Controller is not necessarily the same as the number of words, N, transmitted by the Exerciser
10; T/R Bit in "RT Address" = 1	00	"T/R Reversal" Error: Transmit Command	
14; T/R Bit in "RT Address "=0	14	"T/R Reversal" Error: Mode Code Format	
20	20	Self-Test Format	Not applicable in RT mode

Table 2-12. RT Mode Formats - cont.

*Indicates Exerciser R.T. "Trigger" Word

KEYBOARD LOW-SPEED I/O FORMAT	HIGH-SPEED/ DMA REMOTE I/O FORMAT	DESCRIPTION	TIMING DIAGRAM
00; and T/R Bit in "RT Address = 0	00	BC-to-RT Transfer	
00; and T/R Bit in "RT Address" = 1	10	RT-to-BC Transfer	
00; and T/R Bit in "RT Address" = 1	10	RT-to-RT Transfer	 ** For this particular format, the RX Command as well as the External (receiving) RT's status word are *not* stored in the Exerciser message RAM.
01	01	RT-to-RT Transfer, Exerciser simulates transmitting RT only	 ***Note—In this format, the Exerciser "triggers" off the "Receive" command word, but simulates the action of the "Transmitting" R.T.

Similar to BC mode, the pre-assigned Status word may be overwritten via user command. The user-assigned Status word may be valid or may contain encoding errors, as programmed.

For RT mode, the "default" RT Status word is updated under the following circumstances:

1) Exerciser operating mode is switched from BC to RT.
2) Whenever the format for the current message block is updated via keyboard or Low Speed remote I/O command.
3) Whenever the "RT Address" parameter is updated for the current message block, or whenever a particular RT message block is linked to by means of the programming of the "linked from" block's RT Address parameter. (Refer to Table 2-13.)

Table 2-13. Assigned RT Status Words (RT Mode)

FORMAT ("LOW-SPEED" DESIGNATION)	"T/R" BIT IN RT ADDRESS PARAMETER	POSITION OF STATUS WORD TO BE UPDATED
0	R (0)	2 + N
0	T (1)	2
2	R (0)	4 + N
3	R (0)	4 + N
4	R (0)	2 + N
4	T (1)	2
8	T (1)	2
10	R (0)	2 + N
10	T (1)	2
14	R (0)	2 + N
14	T (1)	2

"N" indicates the value of the Word Count parameter for the respective message block.

For RT mode, the default status word is assigned for both "enabled" (E) and "linked to" message blocks.

2.9.4 REAL-TIME MONITOR OUTPUT PORT

Another added feature for the Exerciser is the Real-Time Monitor/Trigger output port. This port provides a real-time parallel interface between the serial bus, via the BUS-1553 decoder, and an external memory.

The real-time monitor, which may be utilized either as a passive background monitor, or in conjunction with the Exerciser's BC or RT modes, presents a full parallel representation of all words that are either transmitted or received over the 1553 bus. In addition to providing a 16-bit representation of each word as it is decoded off the serial bus, the port also provides indications of sync type, data direction, word errors, RT "trigger" word flag, Exerciser message block number and many other signals that may be used in various testing and diagnostic applications.

Referring to block diagram Figure 2-10, it is seen that the Real-Time Monitor/Trigger output is configured with five tri-state enable inputs for individual 8-bit (or less) groups of output signals. This allows the monitor port to easily interface to either 8-, 16- or 32-bit system buses.

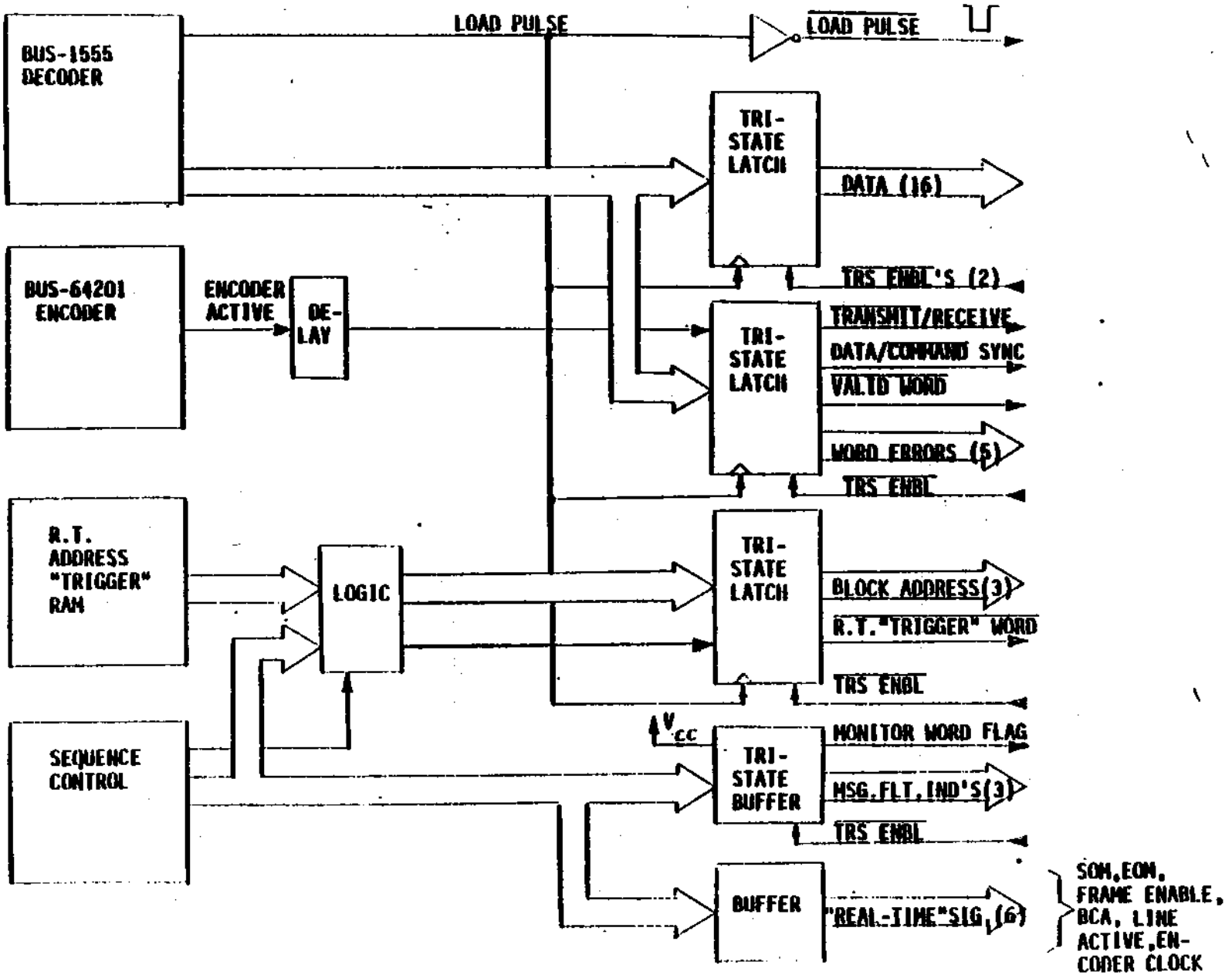


Figure 2-10. Real-Time Monitor Output Port Block Diagram

2.9.4.1 SIGNAL DESCRIPTIONS

$\overline{\text{LOAD PULSE}}$: The occurrence of this 125 ns negative pulse indicates that a new word has been latched into the monitor port's output buffer. The new word data becomes valid 30 ns MAX after the falling edge of LOAD PULSE.

D15 (MSB) through D8: Upper eight bits of the last received, decoded word from the serial bus.

$\overline{\text{DATA HIGH ENABLE}}$: When asserted low, this input activates the tri-state outputs for D15 through D8.

D7 through D0 (LSB): Lower eight bits of the last received, decoded word from the serial bus.

$\overline{\text{DATA LOW ENABLE}}$: When asserted low, this input activates the tri-state outputs for D7 through D0.

$\overline{\text{TRANSMIT}}$/RECEIVE: A low on this output indicates that the current word in the monitor output buffer was transmitted by the Exerciser. A high indicates that the word was transmitted by an external bus device.

DATA/$\overline{\text{COMMAND}}$ SYNC: A high indicates Data sync type for the current word in the buffer. A low indicates Command/Status sync.

$\overline{\text{VALID WORD}}$: A low on this output indicates that the current word has passed the MIL-STD-1553 validation criterion: Valid sync, Manchester encoding, bit count and parity. A high indicates one or more error conditions were detected for the current word.

SYNC TYPE ERROR: This output, which is valid for received words only, indicates (when high) that the decoded sync type for the current word varied from the anticipated sync type for the format and word count of the message being received.

PARITY ERROR: This output high indicates that odd parity was not decoded for the current word.

MANCHESTER ERROR: This output high indicates a Manchester II encoding error in the current word.

LOW BIT COUNT: This output high indicates that less than 17 bits were decoded for the current word.

HIGH BIT COUNT: This output high indicates that more than 17 bits were decoded for the current word.

$\overline{\text{ERROR ENABLE}}$: When asserted low, this input activates the tri-state outputs for $\overline{\text{TRANSMIT}}$/RECEIVE, DATA/$\overline{\text{COMMAND}}$ SYNC, VALID WORD, SYNC TYPE ERROR, PARITY ERROR, MANCHESTER ERROR, LOW BIT COUNT and HIGH BIT COUNT.

BLOCK ADDRESS 2 (MSB), 1 and 0 (LSB): These three bits indicate one less (0-7) than the number of the current Exerciser message block (1-8) when the instrument is operating in either BC or RT mode.

$\overline{\text{RT TRIGGER WORD}}$: This output is applicable for RT mode only. When it is low, it indicates that the current word is a received command word containing one of the Exerciser's programmed "RT Address/T-R bit" combinations.

$\overline{\text{BLOCK ADDRESS ENABLE}}$: When asserted low, this input activates the tri-state outputs for BLOCK ADDRESS 2, 1 and 0, and RT TRIGGER WORD.

WORD FLAG: This output is high for all words. It may be used to set a flag bit in an external memory that had been previously cleared by the external system. It may then be used to distinguish between used and unused memory locations.

BUS FAULT: This output high indicates that a word, word count or format error has occurred in the current frame (BC mode) or current message (RT mode).

REPLY TIMEOUT: This output high indicates that an external RT has responded later than the programmed value for response timeout, or earlier than 4 us (per MIL-STD-1553B).

TRANSMITTER TIMEOUT: This output high indicates that there has been continuous activity on the BUS for longer than 800 us.

$\overline{\text{FAULT ENABLE}}$: When asserted low, this input activates the tri-state outputs for WORD FLAG, BUS FAULT, REPLY TIMEOUT and TRANSMITTER TIMEOUT.

The remaining six outputs are real time signals that may be used in various testing applications. They are TTL positive-true outputs (not tri-states).

START-OF-MESSAGE: This 125 ns positive pulse marks the start of the Intermessage Gap delay time for BC mode, or the reception of a command word containing one of the Exerciser's programmed RT address/T-R bit combinations for RT mode.

END-OF-MESSAGE: This 125 ns positive pulse occurs after the last transmitted or received word has been transferred from (to) the Exerciser message RAM for the current message in BC or RT mode, or after a reply timeout condition has occurred.

FRAME ENABLE: This signal high indicates that the Exerciser is currently processing a frame of messages in BC mode, or is on-line and either processing or anticipating to process a message, in RT mode.

BUS CYCLE ACTIVE: This output high indicates that the Exerciser is presently processing a message in BC or RT mode. BUS CYCLE ACTIVE is the signal used for the Exerciser's front and rear panel SYNC OUTPUT connectors.

LINE ACTIVE: This positive-true output indicates that there is currently activity on the serial bus.

ENCODER CLOCK: When this output is a continuous low level, it indicates that the Exerciser is not transmitting on the serial bus. When the Exerciser is transmitting, this signal will be a 2 MHz clock output with each rising edge shifting the sync/data/parity bits through the encoder. For induced zero-crossing deviation errors, the period of this clock changes to 312.5, 375, 625 or 687.5 ns for a single cycle.

2.9.4.2 REAL-TIME MONITOR TIMING

The timing diagrams of Figures 2-11 (BC mode) and 2-12 (RT mode) illustrate the operation of the Real-Time Monitor/Trigger Interface. Figure 2-13 indicates the real-time monitor/trigger output for various message error conditions (shown for BC mode).

2.9.5 EXTERNAL TRIGGERING AND BUS SWITCHING TEST FOR DUAL REDUNDANT RTs

The SAE ASD-1 production test plan for MIL-STD-1553 RTs includes a requirement for testing of dual redundant RT operation. In order to perform this test, it is necessary to transmit on two 1553 buses simultaneously.

As shown in Figure 2-14, it is possible to implement the bus switching test by using two Exercisers. The sequence for the test is as follows:

1) Send a transmit command word requesting 32 data words on either of the RT's dual redundant channels (channel A in the example shown). Verify for either no response, clear status, or truncated response from this RT channel.
2) Following a programmed delay of at least 4 us, send a similar command word to the RT's alternate channel. Verify for a response of Clear Status and 32 data words from this channel.
3) Send a valid transmit status mode code command to the first channel of the RT. Assuming this mode code is implemented by the RT, verify for Clear Status response.

For dual redundant RTs, the bus switching test must be performed for both channels.

2.9.5.1 INTERNAL/EXTERNAL TRIGGER SELECT

For most test scenarios, the start of BC transmission is initiated directly by either pressing the front panel RUN pushbutton or by entering either a low-speed go command or a high-speed "!" command from one of the three remote interfaces.

The Exerciser offers the choice of "external" triggering as an alternative to the normal "internal" triggering. "External" triggering is required for performing the Bus Switching test and may be used in other applications where it is required to synchronize the start of Exerciser transmission to an external event.

In order to initiate BC transmission in "External" trigger mode, two events must occur:

1) The RUN pushbutton must be pressed, or a low-speed GO command or high-speed("!")command issued, or the BC may be started via the IEEE-488 (GPIB) interface using DMA. (Refer to paragraph 2.11.5.11.)
2) The $\overline{\text{TRIGGER INPUT}}$ signal to J15-13 must be asserted as a logic zero level.

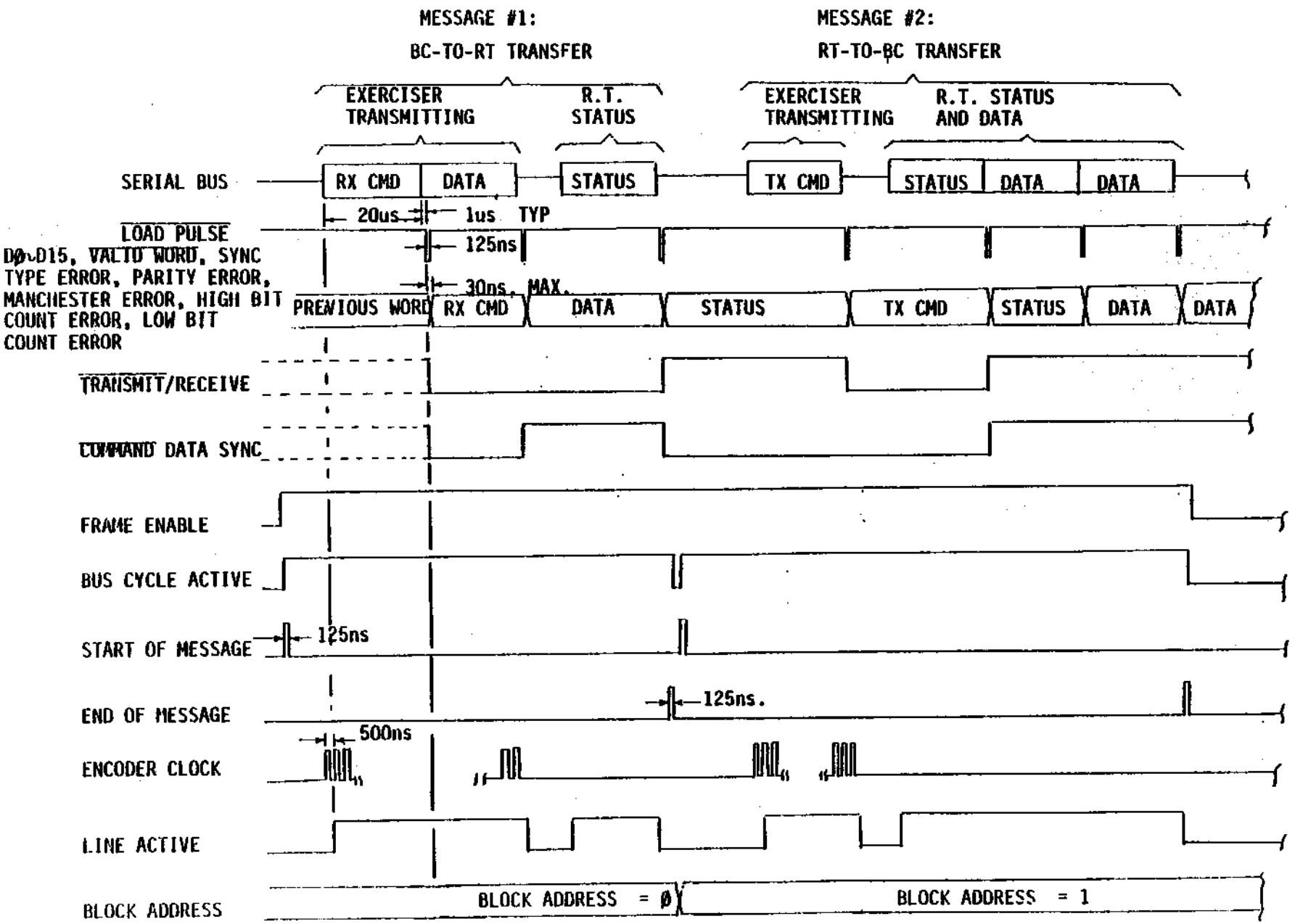


Figure 2-11. Real-Time Monitor/Trigger Timing for BC Mode

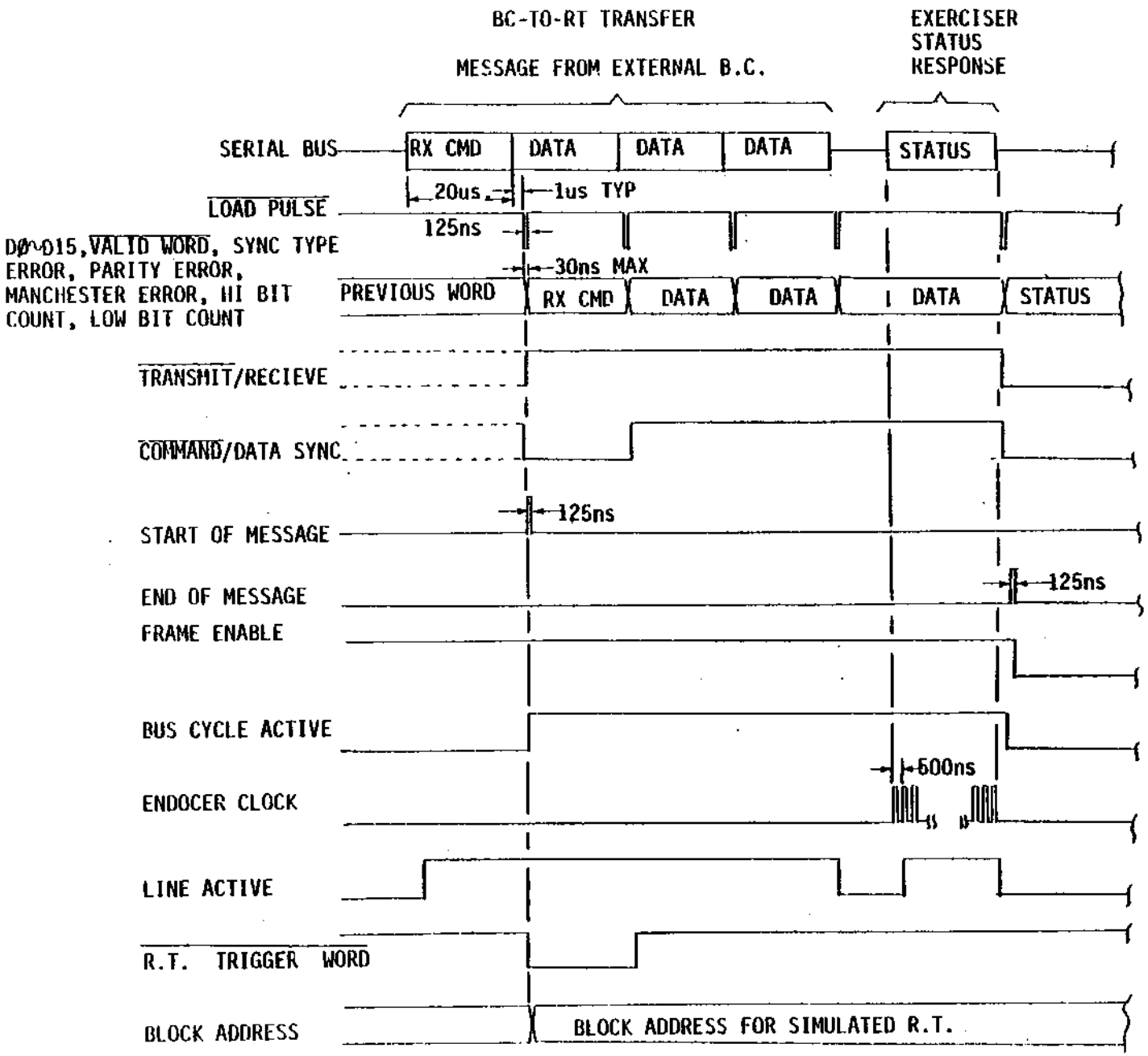


Figure 2-12. Real-Time Monitor/Trigger Timing for RT Mode

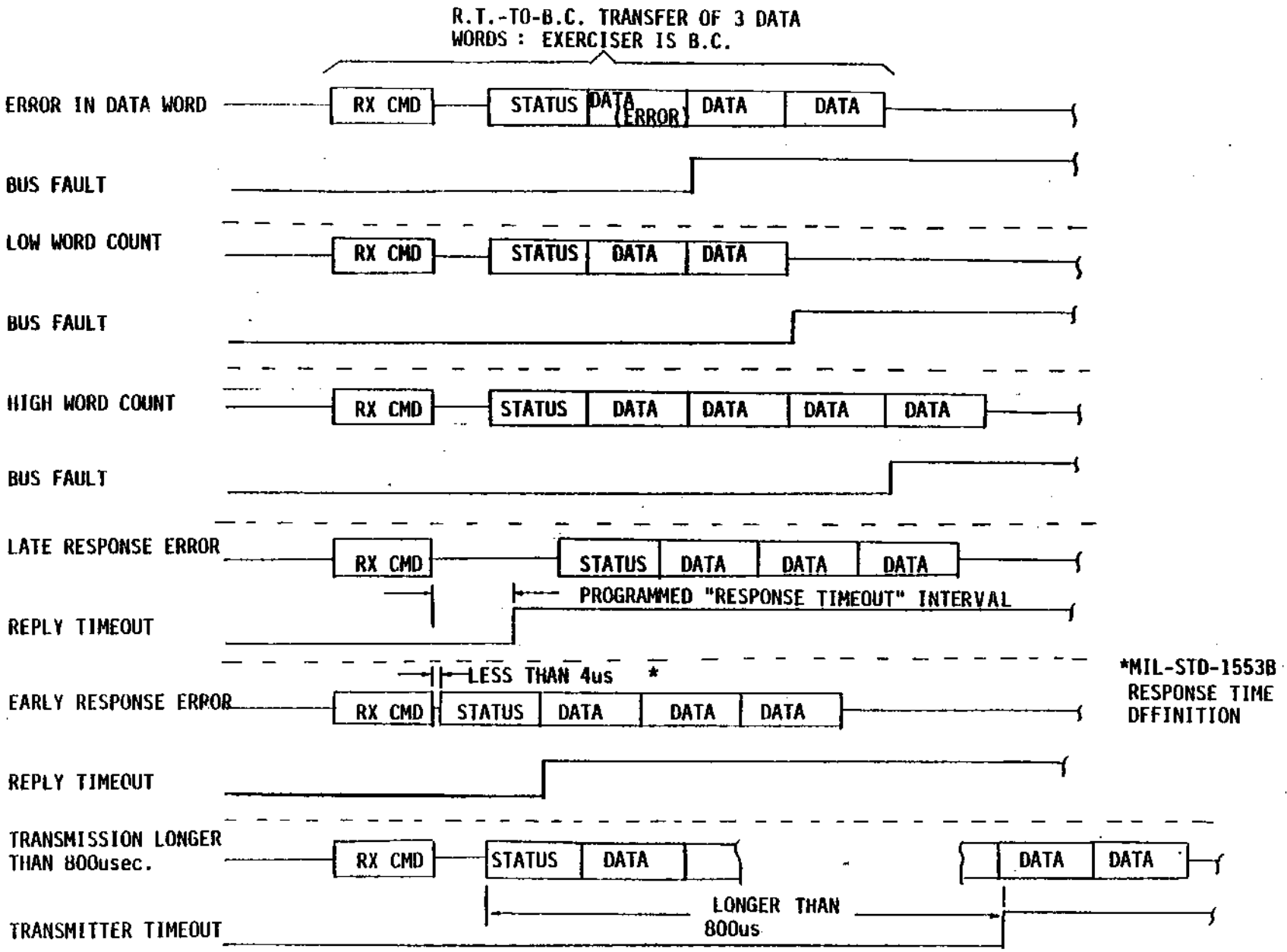


Figure 2-13. Real-Time Monitor/Trigger Timing for Message Error Condition (BC Mode)

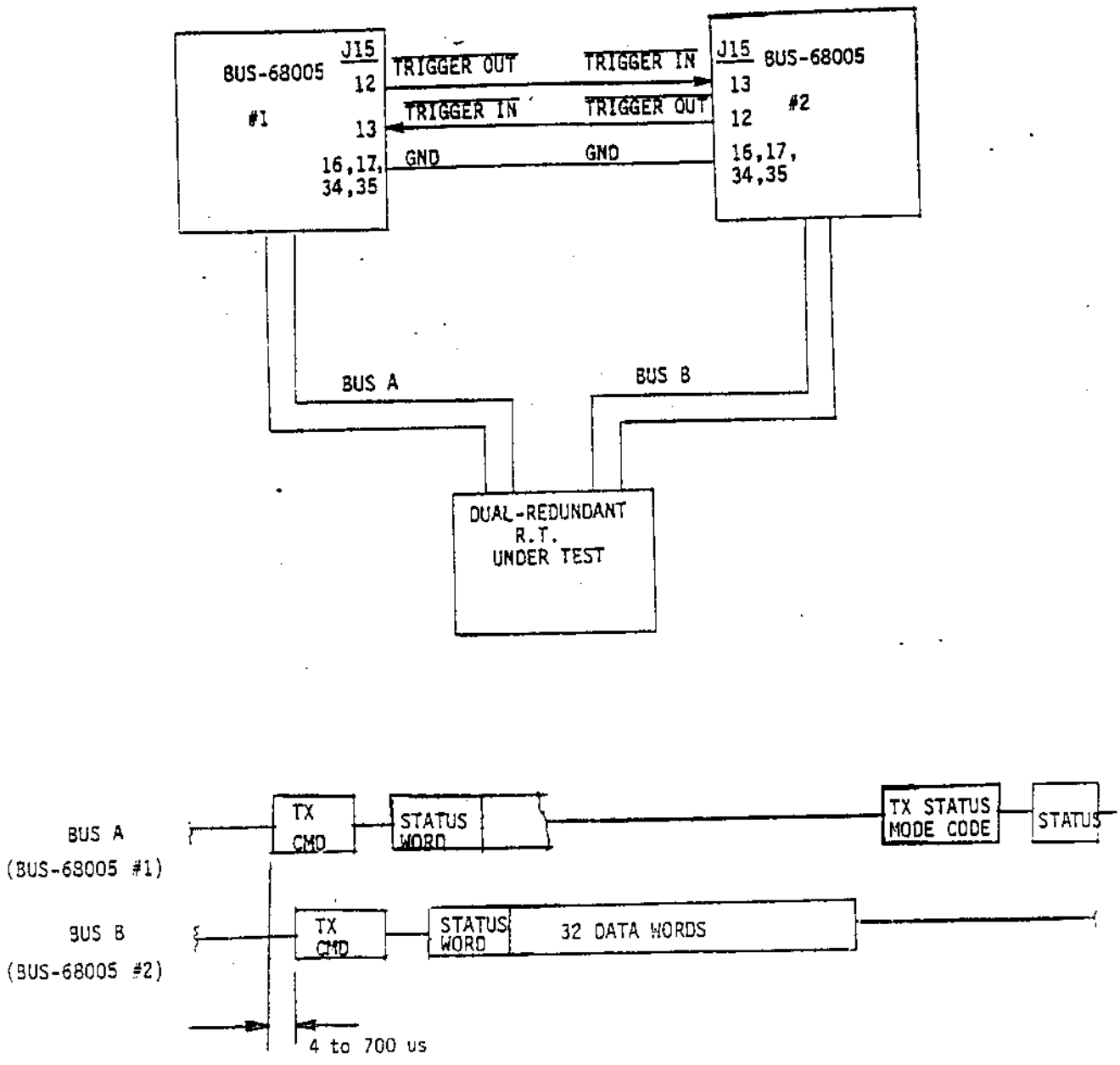


Figure 2-14. Bus Switching Test Using Two Exercisers

The possible timing sequences for "External" triggering are illustrated in Figure 2-15. The start of BC transmission will only occur after **both** of these events occur. In effect, if the Go command (or equivalent) is executed after a $\overline{\text{TRIGGER INPUT}}$ pulse has been received, the Exerciser will initiate transmission following a delay corresponding to the programmed Intermessage Gap Time (IMG) for message block 1. If the Go command is executed first, the start of transmission will occur after the programmed intermessage gap time has elapsed after the $\overline{\text{TRIGGER INPUT}}$ has been asserted low. If a Go command is executed and no $\overline{\text{TRIGGER INPUT}}$ pulse is received before a subsequent Halt I/O command (or HALT pushbutton) is processed, the Exerciser will switch to its off-line (halted) state without processing any messages.

2.9.5.2 TRIGGER OUTPUT

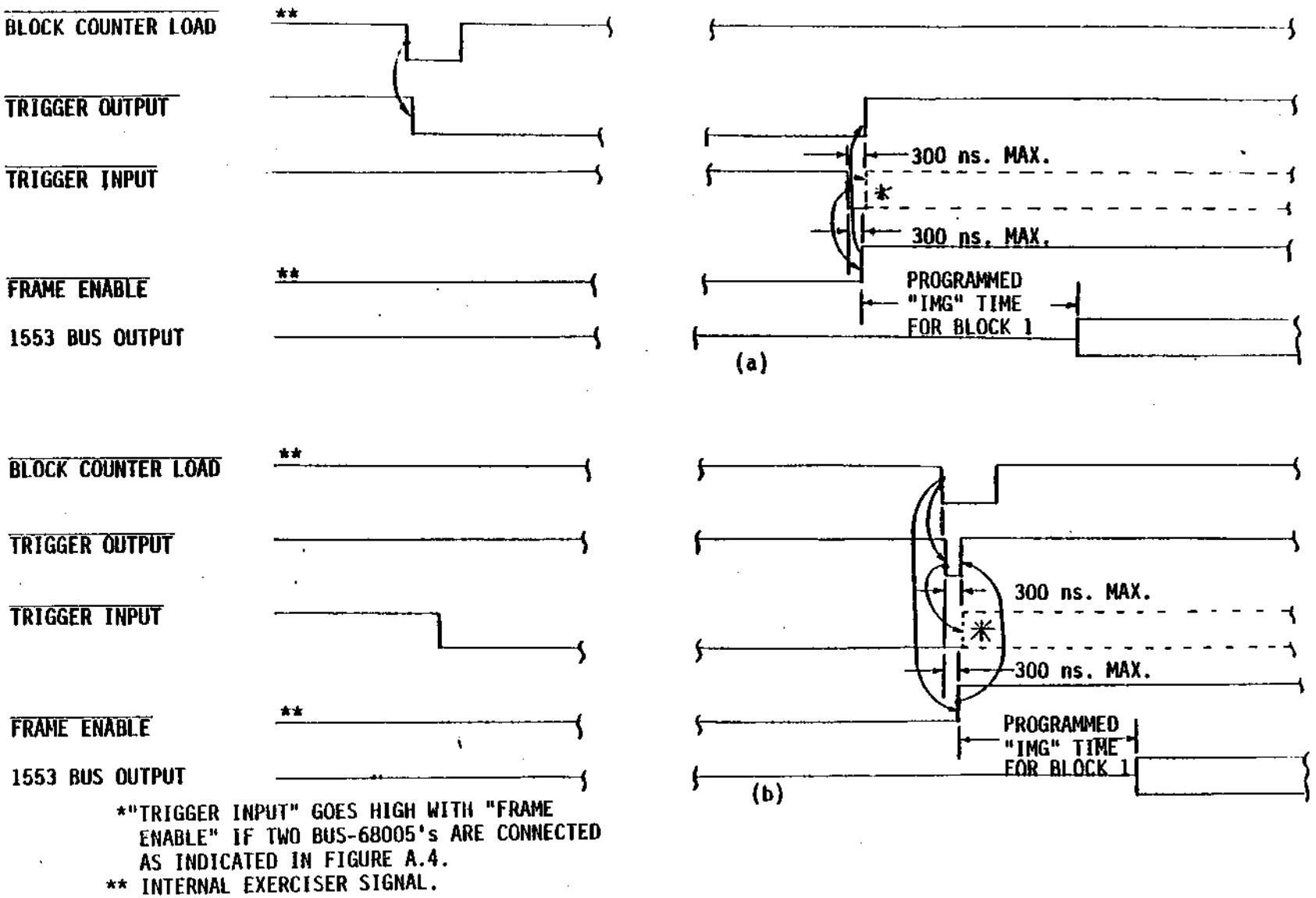
In addition to the $\overline{\text{TRIGGER INPUT}}$ signal, there is also a $\overline{\text{TRIGGER OUTPUT}}$ signal (J15-12) associated with the external trigger mode. As shown in Figures 2-14 and 2-15, $\overline{\text{TRIGGER OUTPUT}}$ is used for synchronizing two Exercisers. $\overline{\text{TRIGGER OUTPUT}}$ is asserted low from the time that the Go command (or equivalent) is executed until the time that the Exerciser actually starts processing messages. If $\overline{\text{TRIGGER INPUT}}$ was a low prior to the Go command, $\overline{\text{TRIGGER OUTPUT}}$ will be low for 125 ns (typical), 300 ns maximum. If the Go command is processed prior to $\overline{\text{TRIGGER INPUT}}$ being asserted low, $\overline{\text{TRIGGER OUTPUT}}$ will go low and remain low until the time that the frame is started by bringing TRIGGER INPUT low. As shown in Figure 2-14, the $\overline{\text{TRIGGER INPUT}}$ and $\overline{\text{TRIGGER OUTPUT}}$ signals are crosscoupled between the two Exercisers in order to synchronize the two instruments. No external delay timing is required.

External trigger is applicable for both single and repeat BC operation. Following power turn-on, the value of the trigger parameter defaults to Internal.

2.9.5.3 BUS SWITCHING TEST IMPLEMENTATION USING TWO EXERCISERS

In order to configure two Exercisers to execute the test sequence indicated in Figure 2-14, the instruments must be configured and programmed as follows:

1) Connect the $\overline{\text{TRIGGER INPUT}}$, $\overline{\text{TRIGGER OUTPUT}}$ and ground signals as indicated.
2) Program both instruments for External Trigger BC mode (TGE via I/O command).
3) Program an intermessage gap time of 7 us for message block 1 of Exerciser 1. Program an intermessage gap time of (7 + (desired delay time interval)) us for message block 1 of Exerciser 2.
4) Program the desired message formats, command words and data words for the two messages for Exerciser 1 and the single message for Exerciser 2.
5) Specify Single or Repeat BC operation for the two instruments, as desired.
6) Initiate the test sequence by either pressing the two RUN pushbuttons or by implementing a GO or (!) I/O command, or by sending the appropriate data via the IEEE-488 GPIB DMA interfaces to both instruments. (Refer to paragraph 2.11.5.11.)



*"TRIGGER INPUT" GOES HIGH WITH "FRAME ENABLE" IF TWO BUS-68005's ARE CONNECTED AS INDICATED IN FIGURE A.4.

** INTERNAL EXERCISER SIGNAL.

Figure 2-15. External Trigger Timing

2.9.5.4 BUS SWITCHING USING EXERCISER AND A BUS-68015 NOISE TESTER

The Bus Switching test implementation using one Exerciser and a BUS-68015 Noise Tester is accomplished as follows:

1) Connect the equipment as shown in Figure 2-16.

2) By referring to the timing diagram of Figure 2-17, it may be seen that the BC transmission from the BUS-68015 Noise Tester will occur exactly 1000 us (1 ms) after its $\overline{\text{SYNC}}$ output is first asserted low. By connecting the $\overline{\text{SYNC}}$ output of the BUS-68015 Noise Tester to the $\overline{\text{TRIGGER INPUT}}$ (J15-13) of the Exerciser, the start of transmission for the Exerciser may be synchronized to occur over the range from -993 us to +1047 us with respect to the BUS-68015 Noise Tester's transmission. This variation is provided by the programming of the intermessage gap time parameter for the message to be transmitted by the Exerciser.

3) By means of the IEEE-488 (GPIB) interface, configure the Exerciser to process a single transmit command to the RT under test. The Exerciser must be programmed for "external" trigger mode, with a transmit command to the appropriate RT address/subaddress, directing it to transmit its maximum number of data words (usually 32). In addition, the intermessage gap time parameter must be specified to correspond to the desired delay time with respect to the BUS-68015 Noise Tester's transmission and, finally, a GO command (either low-speed or high-speed) must be issued. This prepares the Exerciser to transmit after it receives the $\overline{\text{TRIGGER INPUT}}$ (sync) pulse from the BUS-68015 Noise Tester.

   An example of such an Exerciser command string is as follows:

   TGE;IMxxxx;PG0C20;GO carriage return

   Note that xxxx assumes the value of 1000 + (delay time) for the case of the BUS-68015 Noise Tester transmitting prior to the Exerciser, or 1000 - (delay time) for the case of the Exerciser transmitting prior to the BUS-68015 Noise Tester. It should also be noted that the command word 0C20 directs RT 1, subaddress 1 to transmit 32 data words.

4) By means of the IEEE-488 (GPIB) interface, configure the BUS-68015 Noise Tester to send a similar transmit command to the RT under test. The BUS-68015 Noise Tester must also be programmed for the appropriate transmitter amplitude and to be initially in its halt state with its noise output disabled.

The following sample BUS-68015 Noise Tester command string sequence is representative of what is required:

(i) SL117;HA;NF;

This sets the transmitter amplitude to approximately 3.0 Vpp, direct coupled across 35 ohms (per the SAE AE-9A Production Test Plan). It also puts the instrument into its halt state with its noise output disabled.

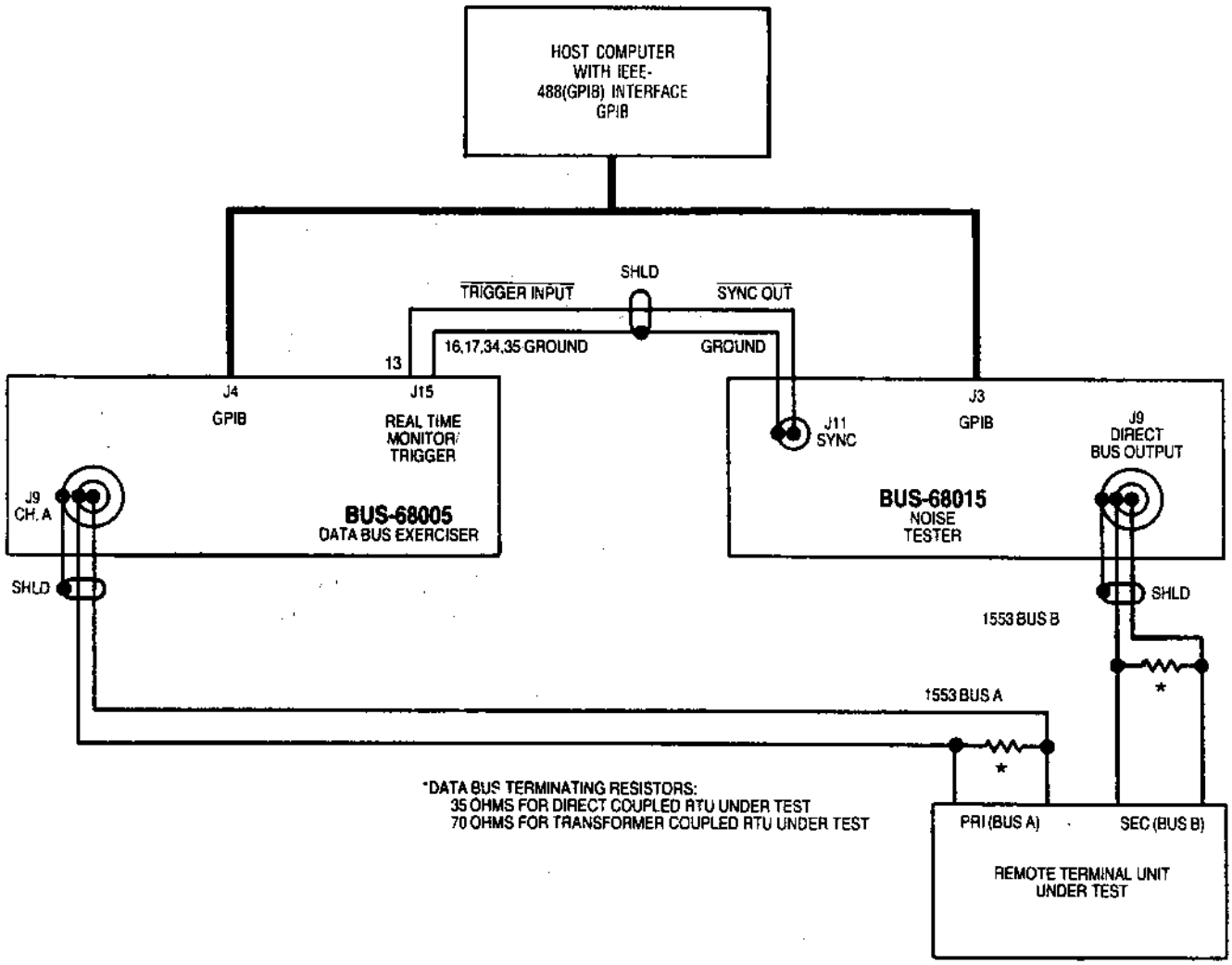


Figure 2-16. Bus Switching Test Using an Exerciser and a BUS-68015 Noise Tester

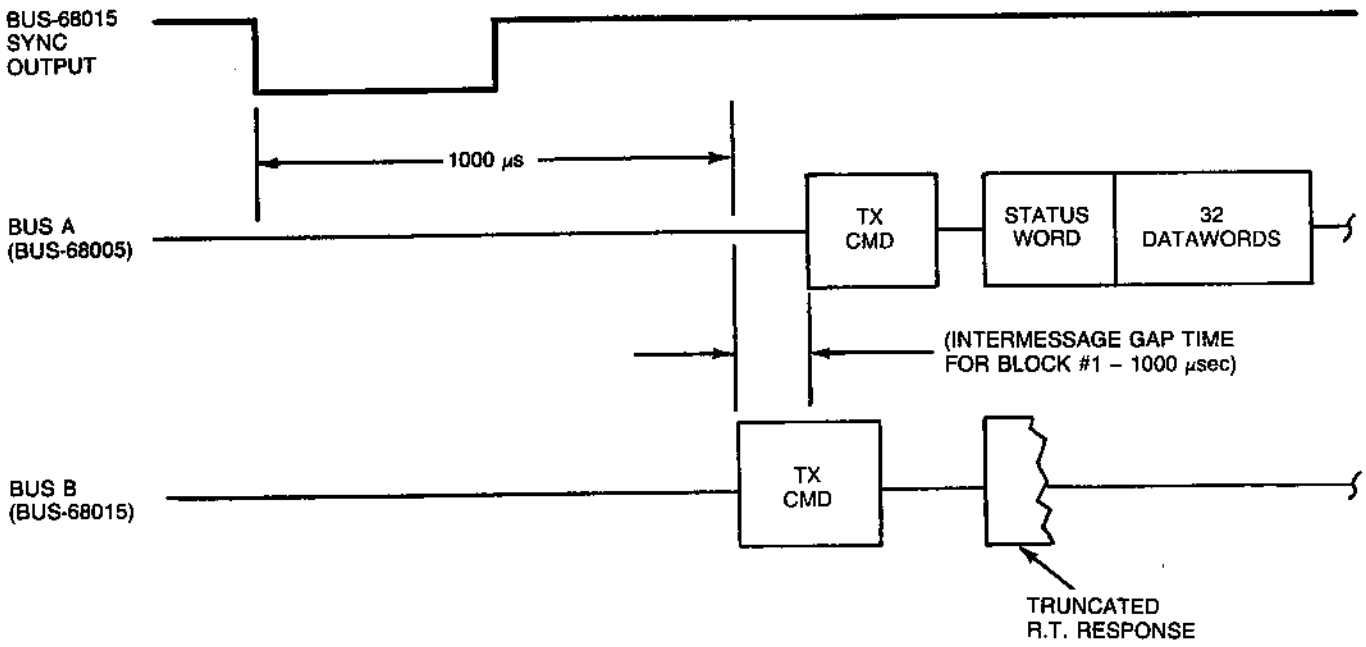


Figure 2-17. Bus Switching Test Timing Diagram for Exerciser/BUS-68015 Noise Tester

(ii)) 03 81 0C 20

This "high-speed" input command configures the BUS-68015 Noise Tester to process a message containing a transmit command word for RT address 1, subaddress 1 to transmit 32 data words --- identical to the command word to be issued by the Exerciser. Note that the first hex byte contains control bits, the second and third bytes contain 16-bit data. Refer to the BUS-68015 Noise Tester Instruction Manual for an explanation of the control bits.

(iii) The "high-speed" Go (!) command to the BUS-68015 Noise Tester initiates the BC message transmission for both the BUS-68015 Noise Tester and the Exerciser.

5) After the message sequences have been processed, the Exerciser should be interrogated to determine the response from the RT under test to the bus switching test message. This is done by means of a Send Block command:

SB carriage return

The reply string will (for example) be 0C20,0080;0800,8080;0000,80C0;0001, 80C0; 001F,80C0;

Refer to paragraph 2.11 for further information regarding the format of the reply string to the Send Block command.

6) To interrogate for the reply string for the BUS-68015 Noise Tester message, a high-speed output command must be sent as follows (to the BUS-68015 Noise Tester):

(63

This directs the BUS-68015 Noise Tester to return a reply string of 63 (hex) (99 decimal) bytes --- three bytes representing the RT status word and each of the 32 data words. The first byte representing each word contains flag bits, the second and third bytes contain the 16-bit data.

A typical BUS-68015 Noise Tester reply string is formatted as follows:

87 08 00 85 00 00 85 00 01 .... 85 00 1F

Refer to the BUS-68015 Noise Tester Instruction Manual for bit coding of the flag byte and additional information regarding the reply string.

2.10 EXERCISER OPTION VIA FRONT PANEL KEYBOARD

As previously mentioned, the Exerciser is fully controllable by means of the front panel keyboard. As shown in Figure 2-18, the keyboard is comprised of a total of 24 pushbuttons. In addition, there are two pushbuttons for run/halt control.

The sixteen keys in the four righthand columns of the keyboard enable manual entry of both decimal and hexidecimal (hex) types of data. On each of these keys, the hex data values are marked in blue. All these keys are dual function keys. That is, in addition to the hex data values, they contain upper case functions, labeled in red.

RUN ○

HALT ○

ENT	CLR	LOC 0	SN RP 1	MODE 2	FRMT 3
NEXT WORD	NEXT BLOCK	RTAD 4	RESP 5	IMG 6	WD CT 7
PROG	READ	ER BP 8	FR TM 9	PRNT A	MS CT B
CNTL	SELF TEST	TA CH C	HLTER D	T/OUT E	TRIG F

Figure 2-18. Front Panel Keyboard Layout

The sixteen keys in the four righthand columns of the keyboard enable manual entry of both decimal and hexidecimal (hex) types of data. On each of these keys, the hex data vlaues are marked in blue. All of these keys are dual function keys. That is, in addition to the hex data values, they contain uppper case functions, labeled in red.

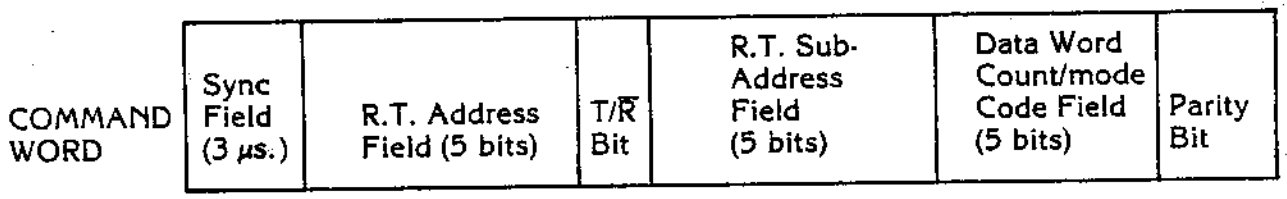
Although all message data is entered, verified and reviewed in hex, most of the instrument parameters (e.g., word and message counts, response time, etc.) must be entered in decimal format.

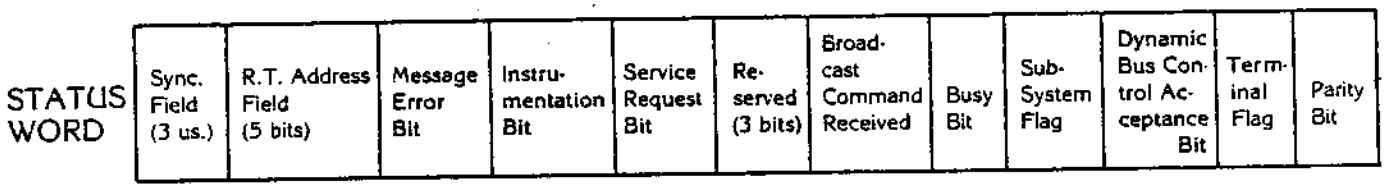
The eight keys in the two lefthand columns of the keyboard are used for entering instrument commands such as Enter, Clear, Program, Read, etc. The "CNTL", or control key in the lower left corner is always used in conjunction with one of the thirteen dual-function keys in order to enter instrument parameters. For example, in order to update the value of the response time parameter, it is necessary to first press the "CNTL" key, then press the "RESP" key while still holding down the CNTL key. The parameter may then be updated by entering one or two digits followed by "ENT".

2.10.1 4-DIGIT HEX PRESENTATION OF MIL-STD-1553 COMMAND AND STATUS WORDS

When using the keyboard "PROG" command to program words to be transmitted to the Exerciser, or using the "READ" command to review received words, it must be noted that all command, status and data words are represented by four hex digits. Similarly, when the instrument is operated over one of the remote interfaces, the 4-digit hex (or 16-bit binary for the "high-speed" or DMA commands) representation is also used.

The formats for MIL-STD-1553 command and status words are as shown below:





The conversion from the command word 4-field representation to the 4-digit hex representation takes place as follows:

- The first hex digit is comprised of the upper four bits of the RT address field.
- The second hex digit is comprised of the LSB of the address field, the T/R bit and the upper two bits of the subaddress field.
- The third hex digit is comprised of the three lower bits of the subaddress field and the MSB of the word count/mode code field.
- The fourth hex digit is comprised of the lower four bits of the word count/mode code field.

This is illustrated as follows:

R.T. ADDRESS FIELD				T/$\overline{R}$ BIT				R.T. SUBADDRESS FIELD				WORD COUNT /MODE CODE FIELD			
A4	A3	A2	A1	AØ	T/$\overline{R}$	S4	S3	S2	S1	SØ	C4	C3	C2	C1	CØ
First Hex Digit				Second Hex Digit				Third Hex Digit				Fourth Hex Digit			

Similarly, for an RT status word, the hex digits are defined as follows:

R.T. Address Field					Message error Bit	Instrument-ation Bit	Service Request Bit	Reserved (3 bits)	Broad-cast Command Received	Busy Bit	Sub-system Flag	Dynamic Bus Control Acceptance	Terminal Flag
A4	A3	A2	A1	A0									
First Hex Digit					Second Hex Digit			Third Hex Digit		Fourth Hex Digit			

To illustrate by example: First consider a transmit Command word to RT 17 (Decimal), subaddress 6 to transmit 25 data words.

Address Field = 17					T/R bit = 1	Subaddress Field = 6					Data Word Count = 25				
1	0	0	0	1	1	0	0	1	1	0	1	1	0	0	1
8					C	D						9			

The hex representation of this Command word is thus 8C09.

As a second example, consider an RT Status word as follows: Terminal Address 23, with the Message Error bit and all other Status word bits cleared (0).

R.T. Address Field = 23					Message Error Bit	Other Status Bits							
1	0	1	1	1	0	0	0	0	0	0	0	0	0
B					8	0				0			

The 4-digit hex representation of this Status word is therefore B800.

2.10.2 KEYBOARD COMMAND TABLE

The operation of the Exerciser's keyboard and display is summarized in Table 2-14.

Figure 2-19 illustrates the generalized flow diagram for manual programming of the Exerciser for both the BC and RT modes. It should be noted that a number of the parameter entries are optional and do not have to be user-specified. These parameters are frame time, error bit position, response time and intermessage gap time. These parameters assume their power turn-on values or previously assigned values, if left unprogrammed.

Table 2-14. Exerciser Keyboard and Display Functions

KEY SEQUENCE	FUNCTION	DISPLAY/INDICATION
CNTL + LOC 0	Selects local mode of exerciser control	LOCAL Indicator lights up
CNTL + MODE 2	Selects (alternatively) Bus controller or Remote Terminal operation	BC or RT Indicator Indicator lights up
CNTL + SNRP 1	Selects (alternatively) Single or Repeat (continuous) mode of operation	SINGLE or REPEAT Indicator lights up
CNTL + FRMT 3; One or Two Hex Digits: DIGIT, DIGIT; (Right Justified) ENT	Information transfer format the current block is selected. See discussion of format in Paragraph 2.9.1.5	The 4-digit (HEX) display will indicate the one or two-digit format

Table 2-14. Exerciser Keyboard and Display Functions - cont.

CNTL RESP 5 One or Two Decimal Digits (Right Justified) { DIGIT, DIGIT } ENT	Simulated Remote Terminal Response Time is entered as 2 decimal digits. The allowable range for response time is from 5 to 32 (us.) for B.C. mode and from 6 to 32 (us.) for R.T. mode.	The 4-digit (HEX) data display will indicate the one or two-digit response time, in microseconds.
CNTL IMG 6 Two or Three Decimal Digits (Right Justified) { DIGIT, DIGIT, DIGIT } ENT	The Intermessage Gap time preceding a given message block for Bus Controller mode is specified. Allowable range is from 7 to 2047 us. See Figure 2-7.	The 4-digit (HEX) data display will indicate the two or three-digit intermessage gap time, in microseconds.
CNTL WDCT 7 One or Two Decimal Digits (Right Justified) { DIGIT, DIGIT } ENT	The data word count for a given message block is specified. For R.T. mode, this parameter must be programmed. For B.C. mode, word count defaults to the correct value if unspecified. Allowable range for word count is from 0 to 45 words.	The 4-digit (HEX) data display will indicate the one or two-digit data word count.
CNTL ER BP 8 One or Two Hex Digits (Right Justified) { DIGIT, DIGIT } ENT	The sync and/or Manchester error position for the current word is specified. See paragraph 2.09.1.7	The block and word number are displayed in their normal positions. The one or two-digit (HEX) error position code will appear in the four-digit (HEX) data section of of the display.
CNTL FR TM 9 One, Two, or Three Decimal Digits (Right Justified) { DIGIT, DIGIT, DIGIT } ENT	The "frame time", or overall repetition time for a series of messages to be executed in Bus Controller mode is programmed. The allowable range for frame time is from 2 to 500 ms. See Figure 2-7.	The 4-digit (HEX) Data Section of the display will show the entered data.
CNTL PRNT A	A user-friendly message that can be displayed on a CRT terminal or printer, conveying all information about the current message block, is outputted via the instrument's RS-232 port. See Figure 2-23.	No change from previous indication
CNTL MS CT B One Decimal Digit { DIGIT } ENT	The number of messages (blocks) to be executed in Bus Controller mode is specified. The allowable range for message count is from 1 to 8.	The 4-digit (HEX) Data Section will show the entered message count information
CLR	Clear function. Terminates data or parameter entry. Also used to enable instrument operation in the event of self-test failure at power turn-on.	The display reverts back to its state prior to the start of entry of the last command
NEXT WORD	The current word number pointer (within the current block) is incremented by one. If the current word is the last word in the block, the "next word" becomes the first word of the block. "NEXT WORD" is also used in conjunction with "PROG" (see below).	The next (or first) word in the message block is displayed in the block, T/R, word number, data and error fields.

Table 2-14. Exerciser Keyboard and Display Functions - cont.

NEXT BLOCK	The block pointer is incremented to the next highest block, or to block 1 if the current block number is 8. The word pointer then points to the first word of the new current block.	The first word of the new current block is displayed in the block, T/R, word number, data and error fields.
PROG One to Six Hex Digits Per Word: DIGIT … DIGIT NEXT WORD DIGIT … DIGIT ENT From one to a full message block full of words may be programmed by the one "PROG" Command.	The data contents and error codes of the current word, or successive words within a message block are programmed. Multiple words are separated by a "NEXT WORD" entry. "ENT" terminates entry of the string of words. If the entry string for a given word is four HEX digits or less, the string represents right-justified data only, with the "error" field defaulting to 00. If programmed, the fifth and sixth HEX digits represent the (right justified) error field for the word. See Paragraph 2.09.1.7 for encoding of the error field for "TRANSMIT" words.	The block number, T/R bit, word number, data and error fields for each word will be displayed as entered.
READ Three Decimal Digits: DIGIT DIGIT DIGIT ENT	The "READ" command positions the word pointer to a specific block and word for review. The block number is specified by the first digit entered. The word number within the block is specified by the second and third digits. Refer to table 2.5 for decoding of the error fields for "TRANSMIT and "RECEIVE" words	The appropriate word is displayed in the block number, T/R bit, word number, data and error fields. The "T/R" field is decoded as follows: T: Transmit Word R: Received Word P: Word Pending Reception; that is, either the message has not yet been executed; or it has been executed and the anticipated "RECEIVE" word was not received -: Word location is not used for the particular mode/format/word count of the message block
CNTL SELF TEST	Causes the instrument to perform its internal self-test. This test exercises PROM, "Message" and "R.T. Trigger" RAMS, and a "wrap-around" test of the -1553 encoder/decoder circuitry. Following self-test, the instrument reinitializes to its power turn-on state:Bus Controller mode, local, single frame, single block, etc.	In sequence: (1) All L.E.D.'s Blank (1 second) (2) All L.E.D.'s illuminate (1 second) (3) "PASS" or "FAIL" is displayed in the 4-digit (HEX) data display. If "FAIL" is displayed, a two-digit "fail-code" is displayed in the error field. See Paragraph 2.6 for interpretation of the "Fail Codes".
SELF TEST	Test L.E.D.'s.	In sequence: (1) All L.E.D.'s blank (1 second) (2) All L.E.D.'s illuminate (1 second) (3) The display reverts back to its previous state.
CNTL READ	This command may only be invoked following failure of the -1553 "Wrap-around" test at power turn-on. It may be used to review the individual "failed" word patterns.	"E" is displayed in the "Block" field. "D" for data, or "E" for Error is displayed in the "Direction" field. The self-test word number (from 1 to 36) is displayed in the word number field. The erroneous data or error word that failed appears in the "sixteen-bit data" field. See Paragraph 4.4 for a more detailed discussion of this diagnostic function.

Table 2-14. Exerciser Keyboard and Display Functions - cont.

KEY SEQUENCE	FUNCTION	DISPLAY/INDICATION
CNTL TA CH DIGIT DIGIT DIGIT ENT ENT	Relative transmitter is programmable in the range from 0 to 255, corresponding to approximately 0 to 9.75Vpp,direct-coupled across 35 Ohms.	"TA" will be displayed in the "BLOCK/DIRECTION" field. The 4-digit (HEX) data section for the "16-BIT DATA" field will indicate the 1,2,or 3-digit relative transmitter amplitude as entered.
CNTL TA CH ENT A or B ENT	The active BUS channel is selected as either Channel A or Channel B.	"CH" will be displayed in the "BLOCK/DIR" field. "-A" or "-B" will be displayed in the "WORD NO." field, as programmed.
CNTL HLTER DIGIT DIGIT ENT	The "HALT-ON-ERROR" parameter is entered as a 1 or 2-digit decimal number from 0 to 99. An entry of 0 specifies continuous operation without halt on-error. An entry of 1 to 99 indicates to halt following the occurrence of the specified number of erroneous message frames (BC mode only).	"HE" will be displayed in the "BLOCK/DIR" field. The 4-digit (HEX) data section for the" 16-BIT DATA" field will display the entered data.
CNTL T/OUT DIGIT DIGIT ENT	The RT response time-out interval (MIL-STD-1553B definition) is programmable over the range from 5 to 32 microseconds, in 1 microsecond steps.	"TO" will be displayed in the "BLOCK/DIR" field. The 4 digit (HEX) data section for the "16-BIT DATA" field will display the entered data.

Table 2-14. Exerciser Keyboard and Display Functions - cont.

KEY SEQUENCE	FUNCTION	DISPLAY/INDICATION
CNTL TRIG 1 or E ENT	In order to enable "External" triggering (usually from another BUS-68005) of the Exerciser to synchronize the start of BC transmission, specify "E". To enable normal "internal" triggering, specify "1".	"TG" will be displayed in the "BLOCK/DIR" field. "1" or "E", as programmed, will be displayed as the last digit of the "16-BIT DATA" field.
CNTL RTAD E 0 or 1 DIGIT DIGIT ENT ,or, CNTL RTAD E 0 or 1 DIGIT DIGIT DIGIT ENT	The "R.T.Address/T-R bit" combination for the current block is enabled as a transmitting or receiving R.T. at the specified address. Since the "linked" field is not specified, it defaults to the current block (no link). Similar to the entry described above, except that the third digit entered specifies the "linked to" block number, or the data block to be processed the second time that the R.T. is addressed. The third digit may also be specified as the current block number ("no link", similar to the default) or as "d", specifying that the simulated R.T. is to go "off-line" after it has processed one message.	The current block will be displayed in the "ERROR"(denoting "links to itself") as well as the "BLOCK" display fields. E, followed by r (for 0),or T(for 1), followed by the two-digit terminal address, will be displayed in the "16-BIT DATA" field. Similar to above,except that the third digit (or "d") entered is displayed in the "ERROR CODE" field, denoting the number of the "linked to" block.

Table 2-14. Exerciser Keyboard and Display Functions - cont.

KEY SEQUENCE	FUNCTION	DISPLAY/INDICATION
,or, CNTL RTAD, d or c ENT	An entry of "d" disables the current block and,effectively, any blocks that were "linked to" from this block. An entry of "d" to a "linked to" block specifies that the simulated R.T. will go "off-line" after the current block processes one message. An entry of "c" disables ALL EIGHT message blocks.	The current block will be displayed in the "BLOCK" field The letter "d" or "c", as programmed, will appear in the "16-BIT DATA" field for previously "enabled" blocks. For previously "linked to" blocks, "d" will appear in the "ERROR CODE" field.
,or, CNTL RTAD DIGIT ENT	The digit specifies the "linked to" block for the current block, if the block has been previously "enabled" or "linked to".	The current block will be displayed in the "BLOCK" field. E or L, followed by r or t,followed by the two-digit R. T. Address will be displayed in the "16-BIT DATA" field. The entered "linked to" digit will be displayed in the "ERROR CODE" field. (examples: Lr01 2, Lt08 1)
,or, CNTL RTAD ENT	The "R.T. Address" parameter is interrogated.	The block number will be displayed in the "BLOCK" field. Either "E" (Enabled as head link of chain), "L" ("linked to" block) or d (disabled) is displayed as the first digit of the "16-BIT DATA" field. If appropriate ("E" or "L"), the following three digits display the transmit/receive and R.T. Address information and the "ERROR CODE" field displays the "linked to" block number.
HALT ◯	Pressing the "HALT" button terminates message processing by the Exerciser. In the B.C. "HALT-ON-ERROR" mode, the Exerciser will halt automatically after the specified number of erroneous frames has occurred.	"HALT" will be displayed in the "16-BIT DATA" field. The number of erroneous message frames that occurred will appear in the "ERROR CODE" field. If "HALT-ON-ERROR" is disabled ("HALT-ON-ERROR" = 0) or no errors have occurred, this field will indicate zero (00).

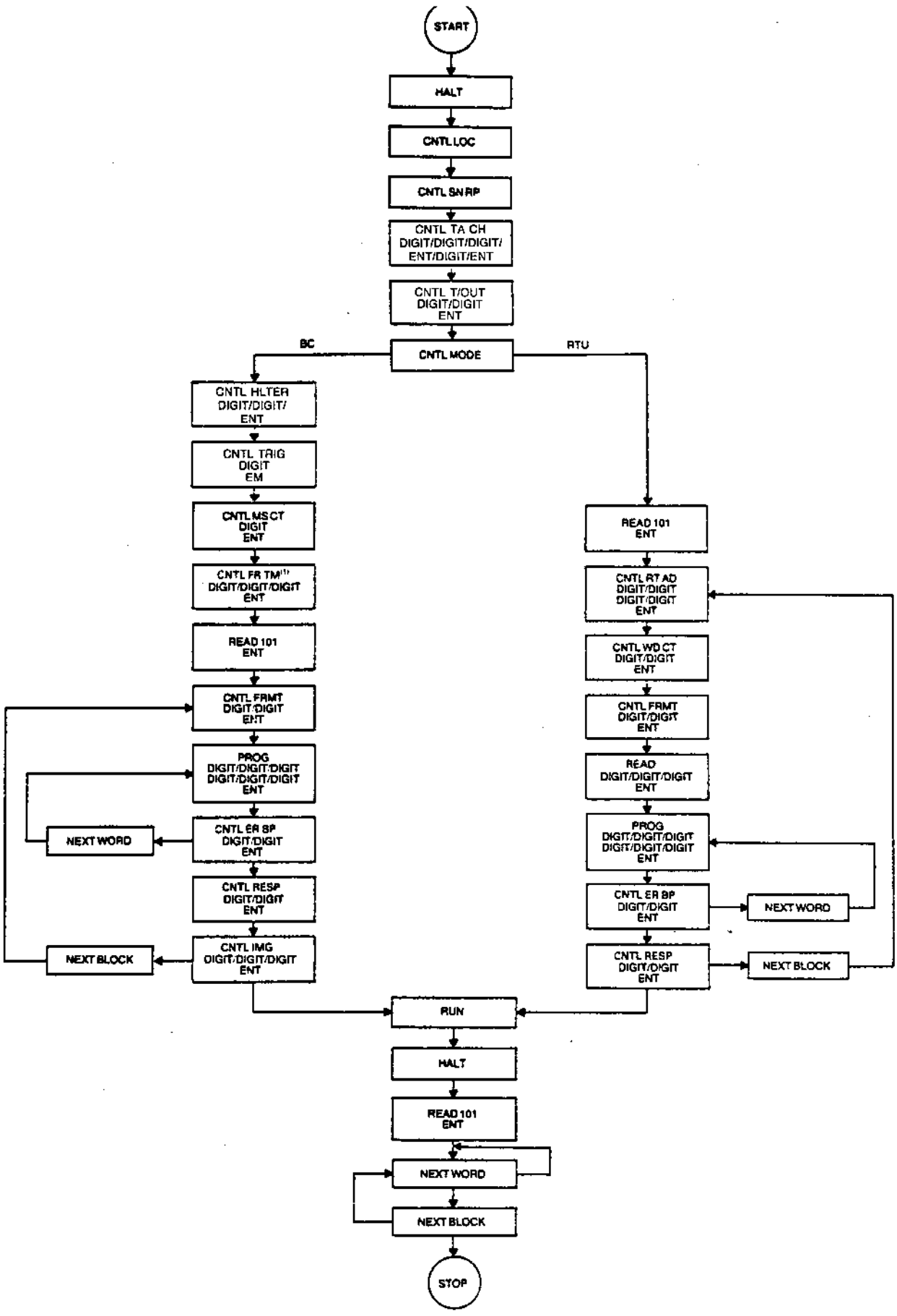


Figure 2-19. Keyboard Programming Flowchart

2.10.3 EXAMPLE OF EXERCISER OPERATION VIA FRONT PANEL KEYBOARD CONTROL

The following example illustrates the use of the front panel keyboard to program a typical set of 1553 message sequences.

The example begins by discussing the power turn-on sequence. It then illustrates Exerciser operation in BC mode for a BC-to-RT transfer message, an RT-to-RT transfer message and for a bus switching test sequence, involving the synchronizing of two Exercisers.

In the second part of the example, the Exerciser is programmed as an RT simulator. In this portion, block linking, multiple RT simulation, and induced error programming are included.

The final portion of the example illustrates the required steps necessary to switch between local and remote control modes.

For the first part of the example, it is assumed that the instrument's channel B bus connector is connected to a set of 1553 RTs over a properly terminated bus. In addition, it is assumed that the Exerciser power switch is initially in the off position.

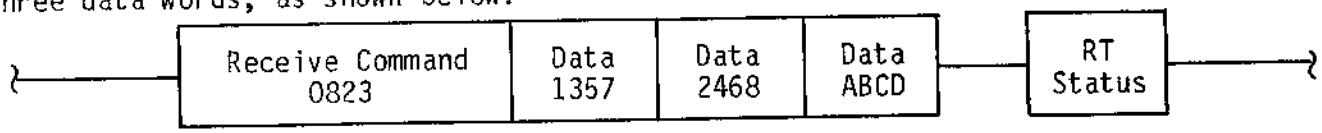
Before programming the message specific commands for BC operation, power is turned on and the user specifies a 5 ms frame time, a relative transmitter amplitude of 125 (approximately 4 Vpp, direct coupled), Channel B as the active bus channel, and an RT response timeout value of 14 us. It should be noted that following power turn-on, the Exerciser defaults to single BC mode, with Channel A the active bus channel, with a relative transmitter amplitude of 6.5 Vpp, a frame time of 10 ms, and a programmed response timeout of 15 us.

The power turn-on and initializing key sequences are performed as follows:

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
Power Switch On In Sequence	In sequence: All horizontal LEDs illuminate (all displays off) 88 -- 1T	88 -- 01	8888 PASS ---- 0840	88 09 00	Power turn-on Blank displays Lamp test display Self-test PASS indication Current software revision Default command word for message block 1
CNTL FR TM 9 5 ENT			5		BC frame time is programmed to 5 ms.
CNTL TA CH C 1 2 5 ENT	TA		125		Relative transmitter amplitude is programmed to 125, corresponding to about 4 Vpp, direct coupled across 35 ohms.
B ENT	CH		b		Channel B is designated as the active BUS channel.

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
CNTL T/OUT E 1 4 ENT	TO	14			RT response timeout is specified for a value of 14 us.

The first message to be processed in BC mode will be a BC-to-RT transfer of three data words, as shown below:



The programming for this message is as follows:

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
PROG 0 8 2 3	1T	01	0823	00	Following power turn-on, the Exerciser's word/ block pointer defaults to word 1 of block 1. The hex command 0823 is a receive command of three data words to RT address 1, subaddress 1.

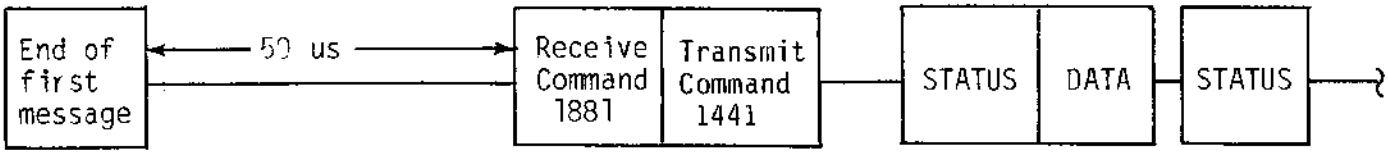
KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
NEXT WORD 1 3 5 7	1T	02	1357	00	The first data word is specified as 1357, with no induced errors (by default).
NEXT WORD 2 4 6 8	1T	03	2468	00	The second data word is 2468.
NEXT WORD A B C D	1T	04	ABCD	00	The third data word is ABCD.

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
ENT	1T	04	ABCD	00	The first four words of message block 1 (command word plus three data words) are loaded into the Exerciser Message RAM.
NEXT WORD	1P	05	0003	00	Note that the next (fifth) word in Block 1 has a direction indication of "P" (pending received), indicating that it is the location of the anticipated RT Status word.

Next, the programmed message is processed once (single BC mode), as follows:

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
RUN ○	BUSY (momentarily) HALT				The single-message frame is processed a single time.
READ 1 0 5 ENT	1R	05	0800	00	It is verified that the Exerciser received an RT Status word response of 0800 -- clear status for RT Address 1, with no word errors detected.

The next message sequence, shown below, is comprised of the BC-to-RT message described above plus an RT-to-RT transfer message. For the RT-to-RT transfer message, the Exerciser simulates the BC only, directing RT address 2, subaddress 2 to send a single data word to RT address 3, subaddress 4. The second message is formatted as follows:



The two messages are to be separated by a programmed intermessage gap time of 50 us, as indicated above. The 2-message frame is to be processed in Repeat, Halt-On-Error mode until the first error is detected.

The key sequence is as follows:

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
CNTL, SN RP 1, ENT	1R	05	0800	00	The Exerciser is configured for "Repeat" BC mode.
	(SINGLE LED turns off. REPEAT LED illuminates.)				
CNTL, MS CT B, 2, ENT			2		The message count (blocks per frame) is specified as 2.
CNTL, HLTER D, 1, ENT	HE		1		The Exerciser is configured to halt repeat BC operation following the first erroneous message frame.

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
NEXT BLOCK	2T	01	0840	00	The Exerciser's block/ word pointer is incremented to the first word of block 2. This word displays its default value of 0840.
CNTL, IMG 6, 5, 0, ENT	2		50		The intermessage gap time for block 2, defined as the gap between message 1 and message 2, is specified as 50 us.
CNTL, FRMT 3, 0, 1, ENT	2		01		The format for message 2 is programmed as 01. This specifies an RT-to-RT transfer message, with the Exerciser simulating the BC only.
PROG, 1, 8, 8, 1	2T	01	1881	00	The first command word for block 2 is programmed as 1881, a receive command for RT address 3, subaddress 4, to receive one data word.

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
NEXT WORD 1 4 4 1 ENT	2T	02	1441	00	The second command word for block 2 is programmed as 1441, a transmit command for RT 2, subaddress 2, to transmit one data word. The ENT key closure causes the two command words to be loaded into Exerciser message RAM.
RUN ○	After a period of time (could be seconds, minutes, or hours)		BUSY o o o o o o HALT	 01	The Exerciser repeats the two-message frame sequence every 5 ms until the first error is detected. At this time, the Exerciser halts transmission and displays HALT 01.

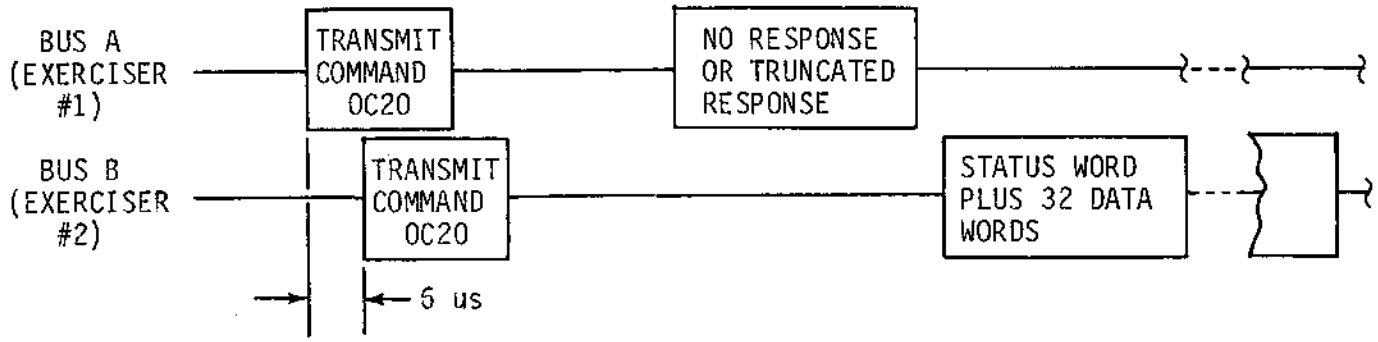
The following key sequence may then be entered to determine the error that was detected:

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
READ 1 0 5 ENT	1R	05	0800	00	A Clear Status response of 0800, with no detected errors having been received for Block 1.
READ 2 0 3 ENT	2R	03	1000	00	A "Clear Status" response with no errors is detected from transmitting RT Address 2.
NEXT WORD	2R	04	7777	00	A data word of 7777 with no errors is detected from the transmitting RT.
NEXT WORD	2R	05	1800	18	The status word response from receiving the RT. Address 3 indicates "Clear Status," but with the Message Error (10) and Parity Error (08) bits set; therefore, the received parity error caused the Exerciser to halt.

Before proceeding with the final portion of the BC example, the Bus Switching test, the Exerciser is reinitialized to its power turn-on default state by invoking a Self-Test command as follows:

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
CNTL SELF TEST	In sequence: (all displays off)				LEDs blank LED lamp test Self-test indication At this time, the Exerciser is in its power turn-on (default) state.
	88	88	8888 PASS	88	

In the Bus Switching test, the starts of BC transmission for the two Exercisers are synchronized to occur with a pre-programmed delay time between the two instruments. The two Exerciser bus outputs are connected to alternate dual redundant buses. In order to perform the synchronization, it is necessary to connect the $\overline{\text{TRIGGER OUTPUT}}$ signal (J15-12) from each Exerciser to the $\overline{\text{TRIGGER INPUT}}$ signal (J15-13) of the alternate instrument. The timing for the bus switching test to be programmed is as follows:



The necessary programming to configure Exerciser 1 to perform this test is as follows:

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
CNTL, TRIG F, E, ENT	TG		E		The Exerciser is configured for External Trigger mode for the Bus Switching test.
CNTL, IMG 6, 1, 0, ENT	1		10		The intermessage gap time for block 1 for Exerciser 1, the time from the start of frame triggering to the start of transmission, is specified as 10 us.
PROG, C, 2, 0, ENT	1T	01	0C20	00	The first word of block 1 is programmed as a transmit command to RT address 1, subaddress 1 to transmit 32 words.

In order to configure Exerciser 2 to start its command word transmission 6 us after Exerciser 1's transmission, this Exerciser should be programmed identically to Exerciser 1, except that the intermessage gap time should be programmed for 16 us instead of 10 us, to provide for the desired 6 us delay time.

After both Exercisers have been programmed, the test sequence may then be initiated by pressing the RUN pushbuttons for both instruments. The order and exact timing of the two RUN pushbuttons closures is **not** critical. The two instruments will then synchronize with each other, resulting in the desired timing.

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
RUN ○	BUSY-momentarily o o o HALT				The Exercisers have BOTH completed the programmed bus switching test sequence.

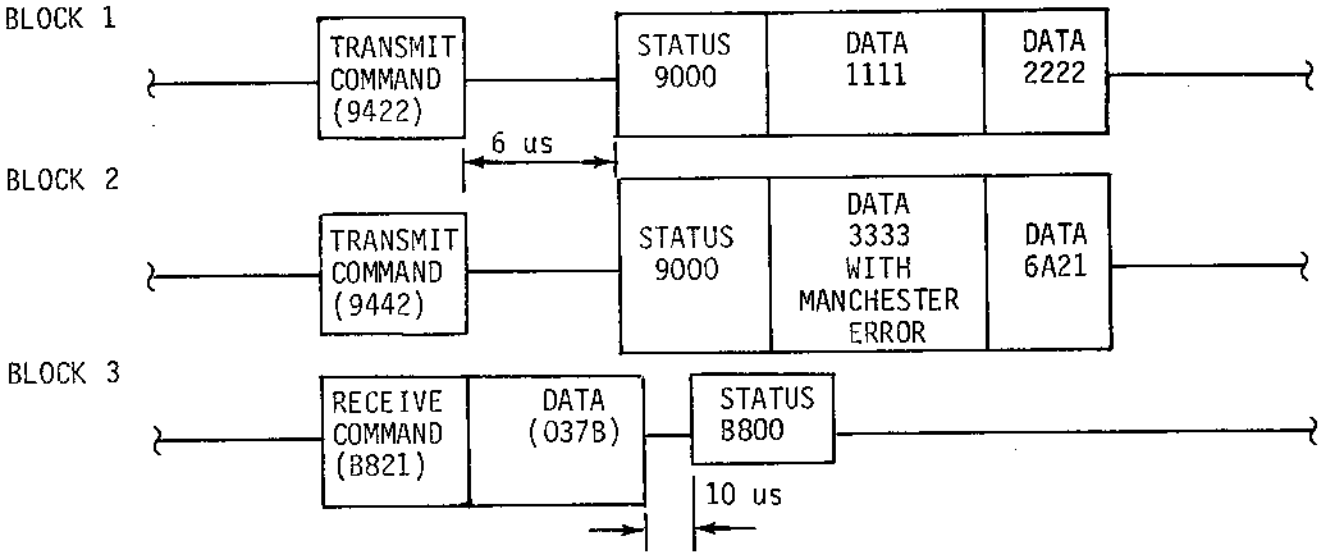
At this time, both Exercisers may be interrogated by means of READ key sequences (NEXT WORD, etc.) to determine the response of the dual redundant RT under test.

The next part of the example illustrates the Exerciser operating in its multi-RT simulator mode. Before performing the detailed key sequence for configuring the simulated terminals, the Exerciser is first reinitialized and switched to its RT mode by invoking the following steps:

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
[CNTL] [SELF TEST]	In sequence...(all displays off) 88	88	8888 PASS	88	LEDs blank LED lamp test Self-test indication At this time, the Exerciser is in its power turn-on, or default state (BC mode).
[CNTL] [MODE 2]	"BC" LED Turns Off "RT" LED Illuminates				The Exerciser switches from BC to RT mode.

In this example, Message Blocks 1, 2, and 3 are programmed to simulate two RTs. Blocks 1 and 2 are configured to simulate RT address 18, transmitting two data words. This illustrates the Exerciser's block linking capability. The first data word transmitted in block 2 will be programmed to contain a Manchester encoding error in its sixth data bit position. Block 3 is programmed to simulate RT address 23, receiving one data word. The response time for this RT is programmed to be 10 us. For the RT responses associated with blocks 1 and 2, the response time assumes the default value for RT mode of 6 us.

The messages for the three message blocks are formatted as follows:



The key sequence to enable these data blocks to be processed in repeat RT mode is as follows:

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
CNTL, SN RP 1	PASS ("SINGLE" LED Turns Off; "REPEAT" LED Illuminates)				Exerciser switches from "Single" to "Repeat" RT mode.

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
CNTL RT AD 4 E 1 1 8 2 ENT	1		Et18	2	Block 1 is programmed to simulate RT address 18, transmitting. The "link" field of 2 indicates that block 2 will simulate RT address 18 (transmitting), the **second** time that it is addressed, after the Exerciser goes on-line.
CNTL WD CT 7 2 ENT	1		2		The transmit word count for block 1's RT is specified as 2.
READ 1 0 2 ENT	1T	02	9000	00	Word 2 has assumed the value 9000, or "Clear Status," for RT address 18.
NEXT WORD	1T	03	0001	00	The default value of word 3 is 0001.

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
PROG 1 1 1 1	1T	03	1111	00	The first data word is programmed as 1111.
NEXT WORD 2 2 2 2 ENT	1T	04	2222	00	The second data word is programmed as 2222. Both data words are stored in the Exerciser Message RAM.
NEXT BLOCK	2P	01	Lt18	2	Second block.
CNTL + RT AD 4	2		Lt18	2	The RT Address parameter for block 2 assumes the same value as that of its "linked from" block (block 1): RT address 18 (transmitting). The default value of its "link" field is 2, meaning block 2 links to itself.

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
1 ENT	2		Lt18	1	The link field is updated from 2 to 1. This means that the third, fifth, seventh, ... etc., times that RT Address 18 (transmitting) is addressed, block 1 will be referenced. Block 2 will be referenced the second, fourth, sixth, ... etc., times that RT address 18 (transmitting) is addressed.
CNTL WD CT 7 2 ENT	2		2		The transmit data word count is specified as 2.
READ 2 0 3 ENT	2T	03	0001	00	The word pointer is positioned to word 3 of block 2.

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
PROG 3 3 3 3 0 4 ENT	2T	03	3333	04	The first data word for block 2 is programmed as 3333, with an error code of 04. This error code is used to induce a Manchester encoding error in the data word.
CNTL + ER BP 8 0 5 ENT	2	03	05		The programmed Error Position, or Error Modifier byte of 05 specifies that the Manchester encoding error will occur in the sixth data bit position.
NEXT WORD PROG 6 A 2 1 ENT	2T	04	6A21	00	The second data word for block 2 is programmed as 6A21.

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
NEXT BLOCK	3P	01	0840	00	The block/word pointer is positioned to the first word of block 3.
CNTL, RTAD 4, E, 0, 2, 3, ENT	3		Er23	3	The RT Address simulated by Block 3 is programmed as Address 23, receiving. Note that the "linked to" block number is not specified and defaults to the block's own number (3). Therefore, block 3 will simulate RT Address 23 (receiving) **every** time that it is addressed to receive data.
CNTL, WD CT 7, 1, ENT	3		1		The receive word count for block 3 is specified as 1.
CNTL, RESP 5, 1, 0, ENT	3		10		The RT response time for block 3 is programmed as 10 us.

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
NEXT WORD NEXT WORD	3T	03	B800	00	The status word for block 3 assumes the Clear Status value for RT Address 23 of B800.
RUN ○			BUSY		The two simulated RTs (three blocks) are put on-line to respond to any and all commands addressed to them.
HALT			HALT		The two simulated RTs (three blocks) are taken off-line.
READ 1 0 1 ENT	1R	01	9422	00	The transmit command word received in block 1 (RT address 18, subaddress 1, transmit two words) is reviewed.
NEXT BLOCK	2R	01	9442	00	The transmit command word received in block 2 (RT address 18, subaddress 2, transmit two words) is reviewed.

KEYBOARD ENTRY	DISPLAY				EFFECT
	BLOCK/ DIR.	WORD NO.	16-BIT DATA	ERROR CODE	
[NEXT BLOCK]	3R	01	B821	00	The "receive" command word received in block 3 (RT address 23, subaddress 1, receive one word) is reviewed.
[NEXT WORD]	3R	02	037B	00	The received data word, 037B, is reviewed.
Instrument is issued a command from its **selected** (via "I/O SELECT" switch S9) host computer interface.	"LOCAL" LED Turns Off "REMOTE" LED Illuminates				The Exerciser switches from Local (keyboard) to Remote (host computer interface) control mode. Subsequent keyboard entries (except for [CNTL] [LOC 0]) will have no effect.
[CNTL] [LOC 0]	"REMOTE" LED Turns Off "LOCAL" LED Illuminates				The instrument switches back to local control mode. Subsequent key entries made will now take effect.

2.11 EXERCISER OPERATION VIA REMOTE INTERFACES

2.11.1 OVERVIEW:

The Exerciser 8-bit bidirectional parallel I/O port, IEEE-488 (GPIB) interface and RS-232 port support three categories of I/O commands, which are:

1) Low-Speed
2) High-Speed
3) DMA (IEEE-488 interface only)

The instrument accepts input commands and data from only one of the ports at a given time. The enabled port is determined by the setting of rear panel I/O SELECT switch S8. Any attempts to input commands to the instrument via a non-selected port are ignored. Setting of the I/O SELECT switch must be changed when Exerciser power is off. If this setting is changed with power on, operation of the interface select logic will be unpredictable.

At power turn-on, the Exerciser initializes to local control mode; i.e. under control of the front panel keyboard. The instrument will switch to remote control mode when either: (1) It receives a command from the parallel port (if selected), (2) it receives a character from its RS-232 port (if selected), or (3) the Remote Enable (REN) line on the IEEE-488 (GPIB) bus is asserted and the instrument is addressed, if the GPIB is the selected interface.

The Exerciser may be switched back to local control mode by means of the keyboard by entering a CNTL-LOC command as per Table 2-14. It should be noted that CNTL-LOC will not take effect if a Local Lockout (LLO) command has been issued to the Exerciser via its IEEE-488 (GPIB) port. It should also be noted that the instrument may be switched from Remote to Local by either issuing a go to local (GTL) command or by clearing REN on the GPIB.

The I/O command lexicon is divided into three major subgroupings:

1) A set of 36 low-speed commands, formatted entirely of 2-letter ASCII mnemonics plus ASCII data. This set of commands essentially duplicates the functions of the front-panel keyboard. It is possible to fully control the Exerciser by means of the low-speed commands only. The low-speed commands allow for user-friendly interactive operation by connecting the Exerciser to an external CRT terminal via the RS-232 interface. The low-speed commands may also be used in conjunction with the high-speed and DMA commands, for purpose of initial set-ups.
2) A set of four high-speed commands, consisting of a single character ASCII mnemonic followed by (in two cases) parameters and data formatted in pure binary bytes. The high-speed commands are used, essentially, for the purpose of transferring blocks of message data between the Exerciser and a host controlling device. In addition to transferring message data, the high speed input command may also be used for entering the control word for a particular message block.

The control word contains the format, word count, timing and block linking (RT mode) information for any given message. Using the high speed commands, it is possible to input 46 words to the Exerciser, process a message and output 46 words in about 26 ms, using a high-speed GPIB controller. The 26 ms is broken down into about 16 ms of general overhead time plus approximately 140 us of transfer time for each word in each direction (a word consists of four binary bytes). This is many times faster than it would take to process the same sequence by means of the low speed commands only. Details of the high speed remote operation are discussed in paragraph 2.11.4.

3) For use with the IEEE-488 (GPIB) interface only, a set of two DMA commands allows the host computer to directly access all memories and registers in the Exerciser's 1553 processor. By means of the DMA mechanism, it is possible to read and write message and control data to memory and to the various Exerciser registers that control the 1553 processor.

2.11.2 CHARACTERISTICS OF THE THREE REMOTE PORTS

2.11.2.1 8-BIT TRI-STATE PARALLEL PORT

This interface is comprised of eight bidirectional tri-state data lines T0 (LSB) through T7 (MSB), two TTL control input lines $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$, and four open-collector handshake output lines $\overline{\text{RACK}}$, $\overline{\text{WACK}}$, $\overline{\text{TACK}}$ and $\overline{\text{SERVICE REQUEST}}$. This interface may be used to communicate with computers and parallel printers.

By referring to timing diagram Figure 2-20, it is seen that the data lines are driven by the instrument only during a read operation. The rest of the time these lines are either in the high impedance state, or are being driven by a controlling device during a write operation.

A read operation is initiated by bringing the $\overline{\text{READ}}$ line to a logic 0. The instrument will then respond by putting the ASCII character to be read on the 8-bit parallel data bus, T0 through T7. Following a minimum delay of 100 ns after the data becomes valid, the handshake outputs $\overline{\text{RACK}}$ (read acknowledge) and $\overline{\text{TACK}}$ (composite transfer acknowledge) are asserted as logic 0. The data stays valid with $\overline{\text{RACK}}$ and $\overline{\text{TACK}}$ held low until $\overline{\text{READ}}$ is returned to logic 1.

In order to write data to the instrument, valid input data must be presented on T0 through T7 for a minimum of 40 ns set-up time prior to bringing the $\overline{\text{WRITE}}$ input line to a logic 0. Although the instrument's input buffer latches the input data on the falling edge of $\overline{\text{WRITE}}$, the character is not read by the Exerciser's internal microprocessor until some time later. At this time, the handshake outputs WACK (write acknowledge) and $\overline{\text{TACK}}$ are dropped to logic 0. When $\overline{\text{WRITE}}$ is brought to logic 1, $\overline{\text{WACK}}$ and $\overline{\text{TACK}}$ will then go high. At this time, the interface is ready for the next byte transfer cycle.

It may be noted from the above discussion that the user has the option of employing either a 3-wire handshake, ($\overline{\text{READ}}$, $\overline{\text{WRITE}}$ and $\overline{\text{TACK}}$) or a 4-wire handshake ($\overline{\text{READ}}$, $\overline{\text{WRITE}}$, RACK and $\overline{\text{WACK}}$). TACK is the logical product of WACK ANDED with $\overline{\text{RACK}}$.

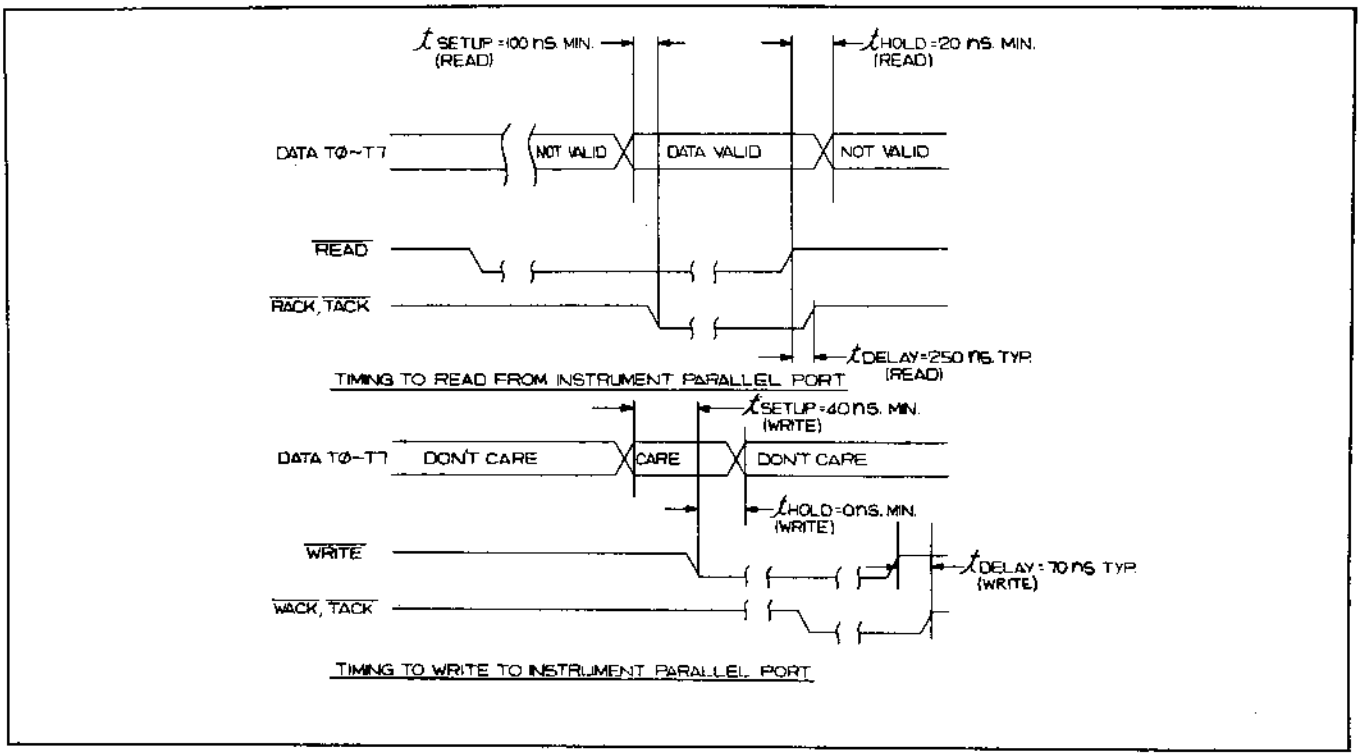


Figure 2-20. Parallel Interface Timing Diagram

The $\overline{\text{SERVICE REQUEST}}$ open-collector output is used to denote a change in instrument status. It will be asserted low under the following conditions:

1) Input Buffer (Queue) is full -- no more characters may be loaded. If an attempt to write additional characters is made when the queue is full, the handshake will continue to operate, but the characters will be ignored. The operation of the command queue is discussed in detail in paragraph 2.11.3.2.
2) Following detection of an error in the input character string.
3) Following completion of a message sequence by the Exerciser's 1553 processor.

$\overline{\text{SERVICE REQUEST}}$ returns to logic 1 after the next character has been read from the instrument via the parallel interface.

2.11.2.2 IEEE-488 INTERFACE (GPIB)

The subset of the IEEE-STD-488-1978 standard that is supported by the Exerciser is indicated in Table 2-15.

Table 2-15. Implemented Subset of GPIB Standard

SH1	Full Source Handshake Capability
AH1	Full Acceptor Handshake Capability
T6	Basic Talk capabilities with Serial Poll and Untalk if My Listen Address
L4	Basic Listen Capabilities with Unlisten if My Talk Address
SR1	Full Service Request Capability
RL1	Full Remote Local Capability including Lockout
DC1	Full Device Clear Capability
DT1	Full Device Trigger Capability
C0	No Controller Capability

The 5-bit GPIB address for the Exerciser is user-selectable by means of the GPIB ADDRESS switch on the rear panel. The MSB and LSB bit positions, as well as the logic sense for the switch, are panel marked. Since the setting of this switch is read by the instrument only at power turn-on, the GPIB address selection must only be changed when the Exerciser power is off.

The serial poll status byte for the Exerciser is defined as follows:

	BIT VALUE (HEX)							
	80	40	20	10	08	04	02	01
BIT MEANING	Input Buffer (Queue) Full	RQS *	RS-232 Error **	DMA Timeout	High-Speed I/O Error	Self-Test Failure	Error In Input Command String	1553 Message Sequence Complete

*USED ONLY IN REPLY TO A GPIB "SERIAL POLL" (SPE) COMMAND. THE "40" BIT OF THE STATUS BYTE WHICH APPEARS AT THE END OF THE "STATUS" REPLY STRING (OVER ANY INTERFACE, SEE PARAGRAPH 2.11.3.1) WILL ALWAYS BE MASKED TO ZERO

**RS-232 ERROR INDICATES ONE OR MORE OF THE FOLLOWING CONDITIONS:

(i) FRAMING ERROR

(ii) RECEIVER OVERRUN

(iii) DCD LOSS

The conditions that result in a GPIB Service Request are identical to those causing a Service Request for the parallel interface:

1) Input Buffer (Queue) full.
2) Error in Input Command String.
3) DMA Timeout
4) 1553 Message Sequence Complete.

Per the IEEE-488 (GPIB) standard, the Service Request (SRQ) is cleared following a read of the GPIB Serial Poll Status Byte by means of a Serial Poll Enable (SPE) command.

2.11.2.3 RS-232 INTERFACE

As indicated in Table 2-2, only seven of the 25 pins on RS-232 connector J3 are used. It should be noted that although the handshake protocol for the signals RTS, CTS and DCD (pins 4, 5 and 8) is supported, the Exerciser's RS-232 interface may be operated as a simple 4-wire connection as shown in Figure 2-21a, when operating interactively using a CRT terminal.

For use with a host computer, especially at baud rates above 300, the hook-up configuration of Figure 2-21b should be used. The use of the RTS and CTS handshake lines on a character-by-character basis serves to prevent a character overflow condition in the Exerciser's RS-232 receiver. If the handshake lines are not used, the host computer can make use of either of two other handshaking mechanisms: (1) Observe XON/XOFF (CRTL/S - CLTL/Q) protocol, or (2) observe the echo back for each low speed command character transmitted to the Exerciser.

The characters transmitted from the instrument's RS-232 port contain 1 start bit, 8 data bits with no parity and 1 stop bit. The parity on all received characters is ignored by the Exerciser.

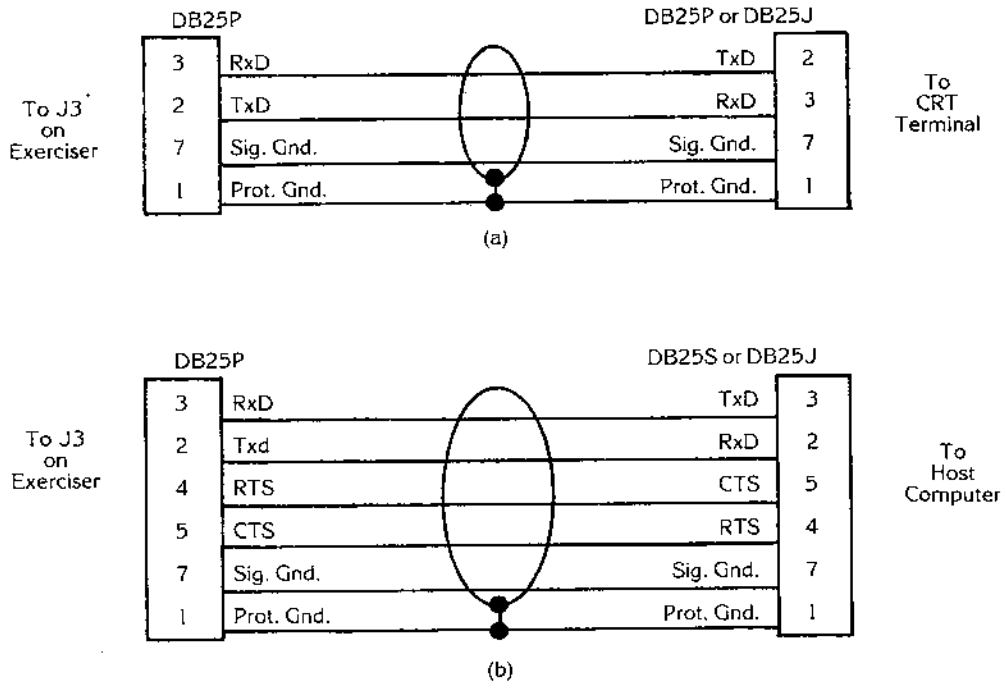


Figure 2-21. RS-232 Connections

a. 4-Wire Connection for CRT Terminal Interactive Operation

b. 6-Wire Connection Including Handshake Lines for Use with Host Computer

When operating interactively by means of a CRT terminal, the terminal should be configured for remote echo. This is because the instrument will handshake by echoing back all correctly formatted low-speed command and data characters received by the RS-232 port. Incorrectly formatted input strings (as well as command queue full, or 1553 sequence complete) result in a service request condition. The Exerciser informs of a service request condition by responding with a "Bell" character (ASCII 07), if RS-232 is the selected interface.

When operating from an ATE host computer via RS-232, a problem that must be avoided is receiver overrun for the Exerciser's RS-232 receiver. There are several ways of avoiding this problem:

1) Operate with the Exerciser's RS-232 echo function enabled and wait for each transmitted character to echo back to the host before transmitting the next character. It should be noted that the Exerciser's RS-232 echo-back function is operational for the low speed commands only. There is no echo-back for the high-speed commands.

2) A preferred method to (1) is to use the RTS and CTS hardware handshake lines, as indicated in figure 2-21(b). In order to attain the fastest, attainable I/O speed over the RS-232 interface using the handshake lines, the echo-back function should be disabled. This is done by sending an echo disable command: ED (CR). Following the (CR), there will be no echo-back for subsequent received characters. By observing the RTS/CTS handshake on a character-by-character basis, the host computer will avoid the problem of transmitting a subsequent character when the Exerciser's RS-232 one-byte input buffer is full, thus avoiding an overrun. Using the handshake lines with the echo disabled will result in higher I/O speed than observing the character echo.

3) Observe the XON/XOFF protocol on a character-by-character basis. The ASCII character XON (CRTL/Q) requests further transmission, while XOFF (CRTL/S) requests for a pause in transmission.

4) Another method that may be used to prevent both receiver overrun as well as queue overflow (refer to paragraph 2.11.3.2) is to terminate each command string with either (CR) or (;) and observe the Exerciser's reply string (refer to paragraph 2.11.3.1) before loading the next command.

5) Configure the Exerciser and host computer for a slower baud rate.

When the Exerciser is sending long reply strings via the RS-232 port, the transmissions may be interrupted and resumed by means of the XON/XOFF protocol: CRTL/S to create a pause in the transmission, CRTL/Q to resume transmission. This is particularly useful when the instrument is sending data to a CRT terminal in response to a PRINT command.

As shipped from the factory, the Exerciser is configured for a baud rate of 9600 bits/second. The baud rate may be field altered by soldering jumper wires on the dip side of the bottom PC board. This is accessible by removing the bottom cover of the instrument. Indications for tie-points E19 through E26 are visibly etched on the solder side of the board. Their locations are as indicated in Figure 2-22. To configure the RS-232 interface for baud rates other than 9600, install jumpers where indicated by X in Table 2-16. The baud rate jumpers should be installed and removed only after AC power is removed from the unit.

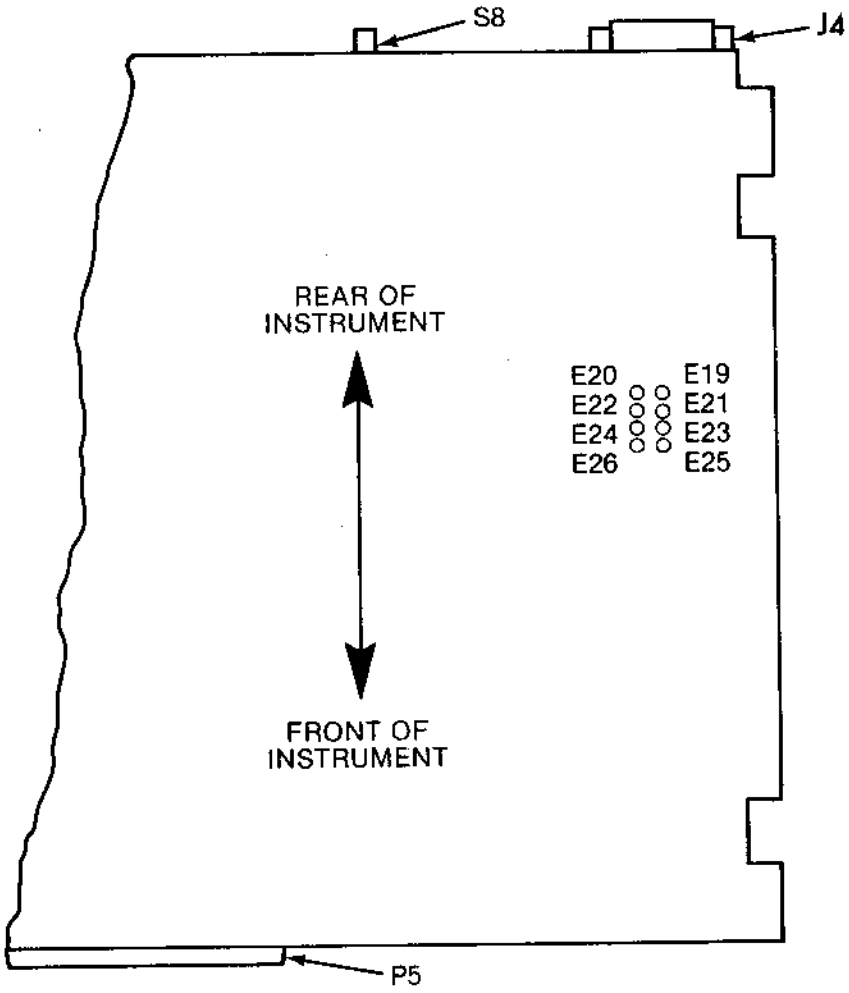


Figure 2-22. Partial View, Bottom PC Board Assembly Dip Side, Indicating Location of Tie Points E19 through E26

Table 2-16. Jumpers Required for RS-232 Baud Rates

Baud Rate (Bits/second)	X = Jumper Required			
	E19 to E20	E21 to E22	E23 to E24	E25 to E26
134.5	X		X	X
150	X		X	
300	X			X
600	X			
900		X	X	X
1200		X	X	
1800		X		X
2400		X		
3600			X	X
4800			X	
7200				X
9600*				

*Factory Setting

2.11.3 LOW-SPEED REMOTE OPERATION

The Exerciser is fully controllable by means of the set of low speed commands discussed in this section. This set of commands, which very closely duplicates the operation of the front panel keyboard, comprises a highly user-friendly mechanism for controlling the instrument.

The low-speed commands serve a number of purposes. These include:

1) They facilitate communication to a host computer, allowing for processing of stored test sequences in situations where timing is not critical.

2) The two-letter command mnemonics with their associated reply strings enable the user to operate the instrument from an RS-232 CRT terminal.

3) The low-speed commands may be used in conjunction with the high-speed and DMA commands discussed in paragraphs 2.11.4 and 2.11.5, respectively. That is, message set-up parameters may be programmed using low-speed commands, while the high-speed and DMA commands are used for block data transfer and go/halt control.

2.11.3.1 COMMAND AND REPLY STRINGS

As mentioned above, the low-speed remote commands are made up of multi-character ASCII strings. As shown in Table 2-17, the first two letters of each command string comprise the identifying mnemonic for the particular command. It may be seen that for 21 of the commands, there are no associated parameters to be loaded into the Exerciser. For the other 10 commands, there are parameters that may be appended.

The input parameters are comprised of either hex or decimal data, depending on the particular command. It should be noted from Table 2-17 that a semicolon is used as a separator following all commands that include data. The exception to this rule involves the case where the command/parameter is the last command in an input string. In this situation, the command should be followed by (CR) or (CR) (LF) instead of the semicolon. The next input character following the semicolon is then assumed to be the start of the next command. Input commands that do not contain data must **not** be separated by semicolons. It should also be noted from the table that commas are used to denote the separation between words for the PG (program) command only.

The right-most column of Table 2-17 indicates the ASCII reply string associated with each of the respective command strings. In order to read the reply string for a particular command string, the following sequence must be implemented:

1) The command whose string is the desired reply must be the **last** command in the loaded string. As shown in Table 2-17, it is possible to interrogate the Exerciser for the value of an instrument parameter by sending the mnemonic only, without data, for the parameter in question. For example, to determine the programmed response time for the current message block, input the string RE, rather then RE10 (for example), as the last command. The exerciser will then respond with the reply string for response time.

2) The input string must be terminated by either a semicolon (;) or (CR) (LF). For the case of the IEEE-488 interface, the EOI handshake line must be asserted with the terminating linefeed (LF) character. A CR (carriage return) or a semicolon (;) may also be used to reinitialize the Exerciser's command parser, in the event of an error in the input command string. Carriage return or semicolon should be transmitted to the instrument immediately after power turn-on to ensure proper initialization.

3) For the parallel port, the reply string will be output from the Exerciser starting with the first character read after LF is written. For the IEEE-488 interface, the reply string will be the instrument's response when it is put into its Talker Active State (TACS). For the RS-232 I/O, the reply string will be sent immediately following the processing of the last loaded command and either (CR) or (;).

   An exception to (1), (2) and (3) above involves the Print (PR) command. This reply (always sent over the RS-232 port) occurs **immediately** following receipt of the PR command in the input string.

4) The appropriate command string from Table 2-17 will then be transmitted. When operating over the RS-232 interface with echo enabled, a leading line feed (LF) character will precede all reply strings. This allows for interactive operation using a CRT terminal. (Refer to paragraph 2.11.3.3.) For any of the interfaces, the reply string will be terminated with a following linefeed (LF) character. When using the IEEE-488 (GPIB) I/O, the EOI handshake line will be asserted when the terminating (LF) is sent.

   This sequence is illustrated by the following example:

   Input (command) string:
   FR02; WC21; SW (CR) (LF)

   Reply String:
   ((LF), if RS-232 with echo enabled) 1T03080000 (LF)

In this example, the format is designated as 02, word count is specified as 21 and the word indicated by the current position of the block/word pointer (word 3 of block 1) is interrogated. The reply string represents this word.

Table 2-17 indicates the command and reply strings for the 36 "low-speed" commands.

Table 2-17. Remote I/O Low-Speed Command Table

COMMAND NAME/ DESCRIPTION	COMMAND STRING SYNTAX	REPLY STRING SYNTAX
Mode Select: causes the instrument to toggle between Bus Controller (BC) and Remote Terminal (RT) modes.	MO	Status Information
Bus Controller: Selects BC Mode.	BC	Status Information
Remote Terminal: Selects RT Mode.	RT	Status Information
Single/Repeat Operation Select: Causes instrument to toggle between "Single" and "Repeat" operation.	SR	Status Information
"Single" operation selection.	SN	Status Information
"Repeat" operation selection.	RP	Status Information

Table 2-17. Remote I/O Low-Speed Command Table - cont.

COMMAND NAME/ DESCRIPTION	COMMAND STRING SYNTAX	REPLY STRING SYNTAX
"Blocks per frame" selection.	BF n; n = number of blocks per frame or BF (to interrogate only)	(7 spaces) n n = number of message blocks per frame. Range is from 1 to 8.
"Frame Time" selection.	FT fff; fff = frame time, 1 to 3-digit decimal (right-justified in ms.) or FT (to interrogate only)	(5 Spaces) fff fff = Frame time in ms. Range is from 2 to 500 ms.
"Next Block" causes the word pointer to point to the first word of the next message block	NB	Word representation of first word of next message block
"Format" selection	FR ff; ff = format byte (HEX) for current block or FR (to interrogate only)	b (5 spaces) fff b = block number fff = message format for current block (see Paragraph 2.09.1.5)
"Word Count" selection. Range is from 0 to 45 data words.	WC nn; nn = one or two-digit decimal word count (right-justified) or WC (to interrogate only)	b (3 spaces) 00nn b = block number nn = block word count

Table 2-17. Remote I/O Low-Speed Command Table - cont.

COMMAND NAME/ DESCRIPTION	COMMAND STRING SYNTAX	REPLY STRING SYNTAX
"Error Position" One or two-digit HEX entry specifies the positioning of sync zero-crossing and/or Manchester encoding errors for the current word. This command may also be used to inquire for the "fourth byte" for received words Refer to Table 2-5.	EP pp; └─2 digit HEX error position code; or, EP (to interrogate only)	b (1 space) nn (2 spaces) pp └─Error-position byte. (Transmit word, or "Fourth byte" for received/ pending received words. └─current word number within current block └─current block number
"GO" command initiates processing of message sequence. To avoid possible I/O timing problems following execution of a "GO" command in "single" B.C. mode, it is recommended that a delay greater than the programmed "Frame Time" be inserted in the host computer program, before sending the next command (e.g., SW, SB,*)	GO. (Alternatively, a "Group Executive Trigger" (GET) command may be used, via the IEEE-488 Bus in place of "GO". The instrument must be "listen addressed" prior to the GET in order for it to take effect).	(4 spaces BUSY: If on-line continuous mode; or HALT following: execution of a single frame (B.C. mode) or message (R.T. mode) if in "Single" mode.
HALT command. Halt causes the Exerciser to terminate -1553 message processing. The Halt reply string for BUS-68005 is expanded to include the error frame count information.	HA	HALT nn └─This indicates the number of erroneous message frames that have occurred for repeat BC mode. If HALT-ON-ERROR is disabled (HE0) or no errors have occurred, this field will indicate zero (00). Indicates that the Exerciser has stopped processing -1553 messages.

Table 2-17. Remote I/O Low-Speed Command Table - cont.

COMMAND NAME/ DESCRIPTION	COMMAND STRING SYNTAX	REPLY STRING SYNTAX
Remote Terminal Address Selection. Each message block may be either disabled, or enabled for a specified t or R direction at a specified address (0 to 31). In order to support the RT Block Linking function, the command and reply strings for RT Address command may assume several formats, as indicated	RAEdaa; 2 digit (decimal) RT Address Designates Transmit (T or 1) or, Receive (R or 0) command as trigger word. Enables the block as a transmitting or receiving RT at the specified address. This block becomes the head block of the chain if a linked to parameter is appended. or, RADdaan; designates linked to block. The linked to block may be specified either as a number between 1 and 8, or as d, indicating that the simulated RT will go off-line following the first time it processes a message. Note that, since the first parameter character for this block's RT address is E, it is designated as the head block of the chain. The head block of the chain is processed first after the instrument goes on line. See syntax above	b (3 spaces) Edaa (space) b linked to block (defaults to current block number). See command string syntax. Current message block number b (3 spaces) Edaa (space) n linked to block number See syntax above

Table 2-17. Remote I/O Low-Speed Command Table - cont.

COMMAND NAME/ DESCRIPTION	COMMAND STRING SYNTAX	REPLY STRING SYNTAX
	or, RAx; x may be specified as either d, c or the number of the linked to block for the current message block. If the current block has been previously enabled (E), an entry of d will cause the current block and, effectively, any linked to blocks, to become disabled. If the current block is presently a linked to block, it will remain linked to, but its link field will become disabled, causing the RT to go off-line after the first time that the block processes a message. If c is entered, ALL EIGHT message blocks become disabled. If a number between one and eight is entered, it becomes the value of the linked to field for the current block. or, RA (to interrogate reply string only)	b (3 spaces) d Indicates current block disabled or, b (3 spaces) Edaa (space) n Same syntax as above; indicates Enabled message block with linked to parameter or, b (3 spaces) L daa (space) n number of linked to block Same syntax as above Indicates block is linked to from another block Current message block number

Table 2-17. Remote I/O Low-Speed Command Table - cont.

COMMAND NAME/ DESCRIPTION	COMMAND STRING SYNTAX	REPLY STRING SYNTAX
"Response Time" specification. Programmable range is from 5 to 31 us. for Bus Controller mode and from 6 to 31 us. for Remote Terminal mode	RE rr; └response time for current message block in us. (one or 2-digit decimal, right-justified); or RE (to interrogate only)	b (3 spaces) rr └response time for current block in us. └block number
"Intermessage Gap" time. This specifies the time delay preceding the start of transmission for a given message block in B.C. mode. The range is from 7 to 2047 us.	IM iii └Intermessage gap time in us. for current block; 2 or 3-digit decimal, right-justified), or, IM (to interrogate only)	b (3 spaces) Oiii └Programmed intermessage gap time in us. └current block number
"Read" command allows for interrogating the data and error code for any transmitted, received or pending received word. The "Read" command may also be used to position the Exerciser's "Block #/ Word #" pointer. Inputting a "Read" command without parameter will position the pointer to word #1 or block #1.	RD bnn; └word number within block └block number or, RD; (positions word pointer to word #1 of block #1).	Representation of Specified Word.

Table 2-17. Remote I/O Low-Speed Command Table - cont.

COMMAND NAME / DESCRIPTION	COMMAND STRING SYNTAX	REPLY STRING SYNTAX
"Next Word" command. Increments word pointer and returns new current word.	NW	Representation of new current word.
"Program" command allows for the programming of one or more transmitted command, status or data words within a message block. Substrings for specifying individual words may be from one to six hex digits. If the word substring is 4 digits or less, it represents right-justified word data. If a fifth, or fifth and sixth hex digits are specified, they represent the right-justified error code for the word. See Para-2.10.1 for the HEX representation of MIL-STD-1553 command and status words	PG dddd; or PG dddd, dddd; or PG dddddee, dd ... d; ... d └ comma separates word entries └ 2-digit HEX error code. (See paragraph 2.09.1.7) └ 4-digit HEX word data or PG (to interrogate only)	Word representation of last programmed word.

Table 2-17. Remote I/O Low-Speed Command Table - cont.

COMMAND NAME / DESCRIPTION	COMMAND STRING SYNTAX	REPLY STRING SYNTAX
"Send Status" command	SS	Status Information
"Send Word" causes the current word to be returned.	SW	Representation of current word
"Send block" command causes all information regarding transmitted, received and pending words in the current block to be returned.	SB	dddd, eepp; dddd, ...dddd, eepp — Semicolon separates words. Only the implemented "R" or "P" words) from the current message block are sent — HEX representation of "error-position" (T words) or "fourth byte" (R words) as per Table 2.5. — HEX representation of word error byte As per Table 2.5. — comma separates data and error fields — HEX representation of 16-bit word data
"Initialize" command configures the instrument to its "power turn-on" state. Refer to Paragraph 2.8.	IN	Representation of word #1 of block #1.
"Self-Test" causes instrument to exercise and verify	ST	None. Instrument reverts back to "Local" control mode. When put in Remote mode

Table 2-17. Remote I/O Low-Speed Command Table - cont.

COMMAND NAME / DESCRIPTION	COMMAND STRING SYNTAX	REPLY STRING SYNTAX
PROMS, "Message" and "R.T. Trigger" RAMS and the 1533 "front-end" circuitry (encoder-decoder). Following self-test, the instrument reverts to its "power turn-on" state. Refer to Paragraph 2.8.		directed to "Talk", the Status Information will be the reply string.
Echo disable. This eliminates the byte (character) handshake echo for the RS-232 port. It may be used to speed up communication between the instrument and a host computer "Echo disable" also eliminates the "leading" (LF) from the RS-232 reply strings.	ED	None.
Echo enable. This configures the instrument's RS-232 port to echo back all bytes (characters) that are received. It is used for interactive operation with an RS-232 CRT terminal. The power turn-on (default) condition for the RS-232 echo is enabled. "Echo enabled" also causes the instrument to transmit a "leading" (LF) for all RS-232 reply strings.	EE	None.
"Lamp-Test" causes the front panel display to "blank" for about 1.5 seconds, then illuminate all L.E.D.'s for about 1.5 seconds.	LT	Word representation of current word
"Print" causes the "user-friendly" formatted print-out of block information to be output via the RS-232 port. Refer to Figure 2-23.	PR	None

Table 2-17. Remote I/O Low-Speed Command Table - cont.

COMMAND NAME / DESCRIPTION	COMMAND STRING SYNTAX	REPLY STRING SYNTAX
"Display Disable" will cause the instrument to stop updating the 10-character front panel display. The 10-character display, as well as the "LOC", "BC" and "RT" L.E.D's will blank while the "REMOTE" L.E.D. will illuminate if the "DD" command is the last command in the input string. The display is automtically re-enabled if the Exerciser is put back in "Local" control mode. Disabling the display eliminates the software overhead time required for display updating when the Exerciser is being controlled from a remote source.	DD	None
"Display Enable" causes the 10-character display to display the current word and allows the display to be updated as required.	DE	Word representation of current word.

Table 2-17. Remote I/O Low-Speed Command Table - cont.

COMMAND NAME / DESCRIPTION	COMMAND STRING SYNTAX	REPLY STRING SYNTAX
Transmitter Amplitude level. The relative transmitter level may be programmed from 0 to 255, corresponding to approximately 0 to 9.75 volts peak-to-peak direct coupled across 35 Ohms. The default value is 171 (about 6.5 VPP).	TAaaa. aaa — Relative transmitter level, 0 to 225 or, TA (to interrogate only)	TA (3 spaces) aaa aaa — Programmed Transmitter Amplitude
Channel Select. The active BUS channel is designated as either Channel A or Channel B. The default value is Channel A.	CHc; c — Active Channel selection (A or B) or, CH (to interrogate only)	CHc; c — Active BUS Channel (A or B)
Internal/External Trigger designation. External triggering (initiating BC transmission) is utilized for the dual redundant bus switching test in order to synchronize two BUS-68005s. Internal triggering is used in all other situations. The default value is internal triggering.	TGt; t — Internal (I) or External (E) triggering is specified, or, TG (to interrogate only)	TGt; t — Internal (I) or External (E) trigger designation
Response Timeout. The timer to determine a no response condition for an external remote terminal is programmable over the range from 5 to 32 usec (Per MIL-STD-1553B) in 1 usec steps. The default value is 15 usec.	TOtt; tt — Response timeout in us, or, TO (to interrogate only)	TO (4 spaces) tt tt — Response timeout value, in microseconds
Halt-on-Error. For Repeat Bus controller mode, the Exerciser may be configured to process message sequences until a programmed number of errors (word, format or reply timeout) has occurred. The number of errors is programmable from 1 to 99. If the parameter is programmed as 0 (default), the Exerciser will run continuously, without halt-on-error.	HEhh; hh — 0 for no halt-on-error. For 1 to 99, halt after the specified number of erroneous message frames. or HE (to interrogate only)	HE (4 spaces) hh hh — Halt-on Error value

Two strings that comprise the reply to a large number of the remote I/O commands are the status information, and the 1553 word representation.

The status information reply string, which constitutes the reply string for the MO, BC, RT, SR, SN, RP, SS, IN, ST and DE commands, is formatted as follows:

mm, r, <3 spaces> n, <1 space> fff, x, c, aaa, tt, ss

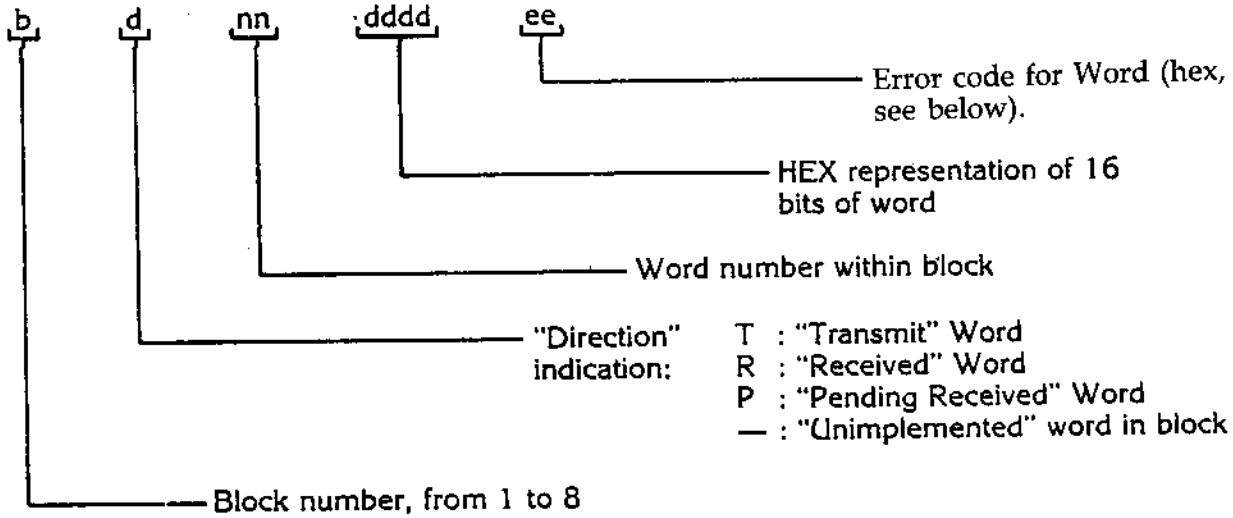
Reply String Parameters:

mm	:	Bus Controller (BC) or Remote Terminal (RT) mode
r	:	Single (S) or continuous (C) Exerciser operation
n	:	Message blocks per frame (decimal); 1 <= <n <= 8
fff	:	Frame time in ms. (decimal); 2 <= fff <= 500
x	:	"Triggering" mode: Internal (I) or External (E)
c	:	Active BUS channel: A or B
aaa	:	Relative transmitter amplitude 000 = aaa = 255
tt	:	Instrument Self-test byte (hex)
ss	:	Serial poll status byte (hex)*

*In the status reply string, the "40" (hex) bit of the status byte is masked to zero.

It is recommended that a Send Status (SS) command be invoked immediately following power turn-on. At this time, it is possible that one or more of the bits or the serial poll status byte will be set. Since this byte is subsequently cleared as a result of performing the SS command, it will reply as 00 the next time it is invoked.

The representation of a 1553 command, status or data word (transmit or receive) in response to the NB, RD, NW, PG, SW and LT commands is as follows:



The error code field in the reply string for these commands for transmitted and received words is identical to the representation indicated in Table 2-5, except that the 80 (hex) bit (pending-received/transmit) is masked to zero. Therefore, the encoding of this error byte is as follows:

Bit Value (HEX)	80	40	20	10	08	04	02	01
For Transmit Words	Always 0	Incorrect Sync Type Error	Parity Manchester Encoding Error	Sync Field Error	Parity Error	Manchester Encoding Error or Zero-Crossing Deviation Error	Low Bit Count Error or Message Gap Error	High Bit Count Error or Word Gap Error
For Receive Words	Always 0	Incorrect Sync Type Error	Early Response Error	Message Error	Parity Error	Manchester Encoding Error	Low Bit Count Error	High Bit Count Error

The third and fourth ASCII hex bytes transmitted in response to a Send Block (SB) command are formatted as indicated in Table 2-5.

2.11.3.2 COMMAND QUEUE:

When a string of commands is loaded to the Exerciser, the individual commands are **not** processed immediately before the next command in the string is accepted. Instead, as a means of minimizing the I/O bus overhead time for the host computer (particularly when operating over the IEEE-488 interface), the commands are stored in a buffer, or command queue section of memory. The command queue serves as a first-in/first-out buffer that may be loaded in minimum time for future processing.

The essential caution that must be heeded in loading command strings to the Exerciser is that the command queue is of finite size: 560 bytes deep. For many applications, this presents no problem. However, for situations where a number of long messages are to be loaded via "PG" commands, the 560 byte (character) queue capacity may be exceeded.

As discussed in paragraph 2.11.2.1, Queue Overflow is one of the Exerciser's "Service Request" conditions. The service request for input buffer full will actually occur when there are ten vacant locations in the queue. At this time, it is imperative that the host device provide for a time delay before inputting additional characters. If attempts to input characters are made with the buffer full, the handshaking for the selected I/O bus will continue to occur, but the characters will be ignored.

There are three methods for handling the problem of finite queue size. It is strongly recommended that methods (1) and (2) below be utilized, since they serve to avoid the complications involved with queue overflow.

1) Limit the length of the input command strings to less than 500 characters and terminate the strings with (CR) (LF). After the terminator, configure the Exerciser to output its reply string. This is done by putting the instrument in its Talker Active State (TACS) for the IEEE-488 (GPIB) interface, or by asserting the READ line low for the parallel interface.

For the RS-232 interface, the Exerciser will output the reply string at the appropriate time, assuming that the RTS/CTS handshake is not used. For any of the interfaces, the Exerciser will return its reply string corresponding to the last command in the input string after it has processed **all** of the commands in the string. At this time, the queue is empty and ready to receive additional command characters.

2) When dealing with long strings of input data, it is better to use the "high-speed" input command (&) or IEEE-488 DMA input command (>) rather than the low-speed program (PG) command. The use of the high-speed and DMA input commands, which are discussed in paragraphs 2.11.4 and 2.11.5, has two advantages:

   (i) The queue buffer is bypassed, eliminating the possibility of the overflow condition.

   (ii) The overall operating speed of the Exerciser will be greatly increased, by a factor of ten or more.

3) Command strings of more than 500 characters may also be loaded by executing the following sequence:

   (i) Load characters until a "Service Request" is issued.

   (ii) Determine that queue overflow is the cause of the Service Request and clear the SRQ flag. This is done by performing a Send Status (SS) command for the parallel or RS-232 interfaces, or a Serial Poll Enable (SPE) command for the IEEE-488 (GPIB) interface. A Serial Poll Status byte of C0 indicates Queue Overflow.

   (iii) Delay for about 20 ms to allow the Exerciser to execute a portion of the commands in the queue.

   (iv) Continue to input characters until Service Request is reasserted. Then return to step (ii).

2.11.3.3 INTERACTIVE OPERATION

Operation of the Exerciser by means of an RS-232 CRT terminal provides for an alternative form of manual control.

Any of the commands listed in Table 2-17 may be entered from such a terminal. As a means of handshake, each character received by the Exerciser is echoed back to the CRT.

The user-friendly printout feature (Figure 2-23) is a particularly useful device available for the interactive operation. It is a powerful tool in that it can be used for reviewing message block data for both set-up as well as verification purposes; i.e., for both prior to and after execution of 1553 message sequences.

The following notes are relevant for the interactive operation:

1) The terminal should be connected to the Exerciser as shown in Figure 2-21a (4-wire connection).

2) The transmit and receive baud rates of the CRT terminal must match the instrument's setting. Refer to paragraph 2.11.2.3.

3) The Exerciser must be configured with its RS-232 echo enabled. This may be done by means of an "Echo Enable" (EE) command, or as the result of power turn-on or following self-test.

4) The terminal should be configured for 1 start bit, 8 data bits, 1 stop bit (mark parity), remote echo.

5) If the user inputs an error in the command string (e.g., a typing error), the Exerciser may be "re-initialized" to accept the next character (start of a new command) by first entering Carriage Return (CR).

```
BLOCK NUMBER:    1                                  RESPONSE TIME:    1Ø
I.M.G. TIME  :   10                                 WORD COUNT    :   5
FORMAT       :   ØØ                                 RT TRIGGER    :   ETØ8


WORD #      T/R        DATA        ERROR        SYNC        ERROR DECODE

  1          T         Ø825        ØØØØ
  2          T         Ø123        ØØØØ                      PE      ME
  •          •          •           •
  •          •          •           •
  •          •          •           •
  6          T         ABCD        ØØØØ
  7          R         Ø8ØØ        ØØØØ          CS
```

WORD NUMBER IN BLOCK

T: Transmit Word
R: Received Word
P: Pending Received Word

HEX representation of 16-bit data

Transmit or Receive Error BYTE and error position byte (for transmitted words) or Fourth Received byte (for Received Words). The values of the Pending-Receive/Transmit" bit (800 HEX) and the Transmit-Receive/Pending bit (ØØ8Ø HEX) are masked to zero in this representation.

Denotes Sync type for Received Words: CS= Command/Status Sync; DS= Data Sync

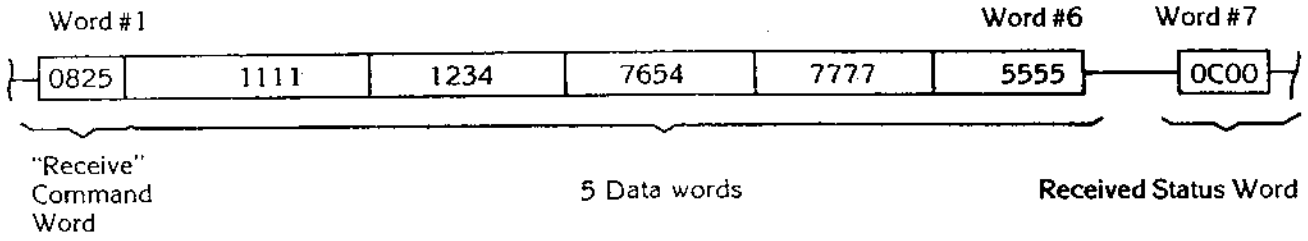
Errors encoded in 2-letter mnemonics as follows: for Transmit words:
LW (Long Word),
SW (Short Word),
ME (Manchester Encoding Error),
PE (Parity Error,
SE (Sync Error),
IS (Incorrected Sync Type),
PM (Parity Manchester Error).
WG (Word Gap Error)
MG (Message Gap Error)
ZC (Zero-Crossing Deviation Error)
For Received Words:
LW, SW, ME, PE, IS, IM (incorrect message: i.e., either an error in the current or previous received word in a message, or a high word count).

Figure 2-23. Example of User-Friendly Printout Via RS-232, as a Result of a Print Command

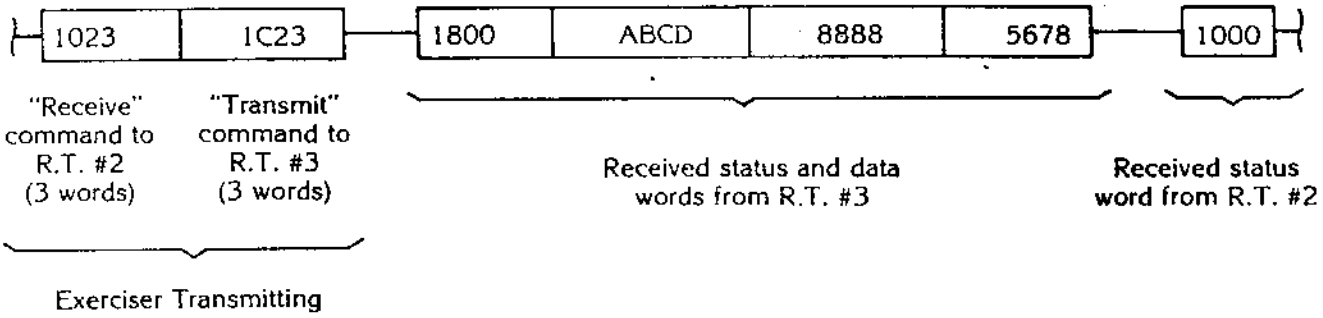
2.11.3.4. EXAMPLE OF EXERCISER OPERATION VIA REMOTE INTERFACE

The operation of the instrument using the "low-speed" remote I/O commands is illustrated by the following example. In this example, the Exerciser will process a frame of two message blocks in "Single" mode as BC.

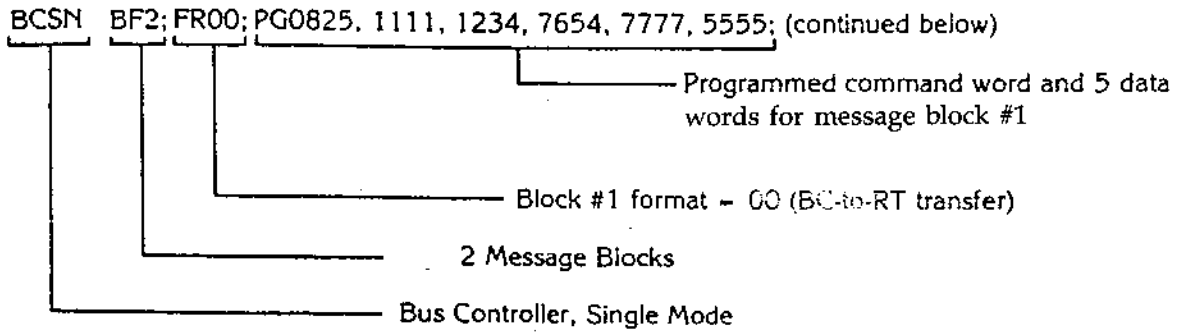
The first message will be a receive command; that is, for RT 1 to receive five words.

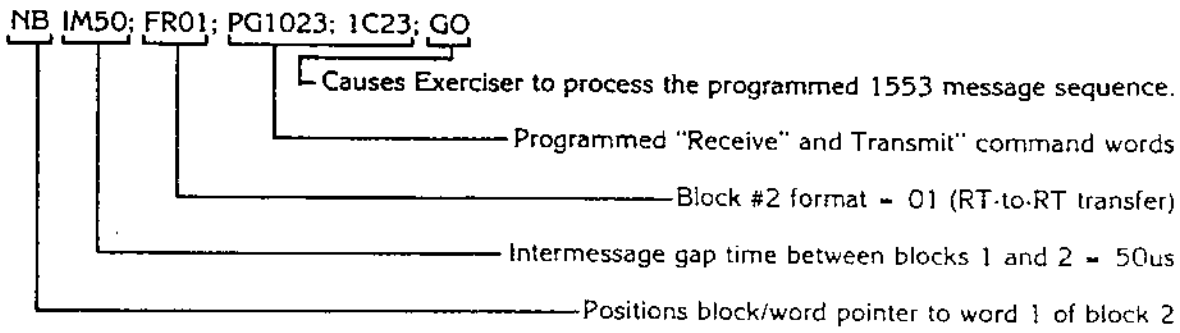


The second message will have a programmed intermessage gap time of 50 us (time between message blocks 1 and 2). The second message will be a format 1 message. That is, the message will be an RT-to-RT transfer with the Exerciser simulating the BC only:

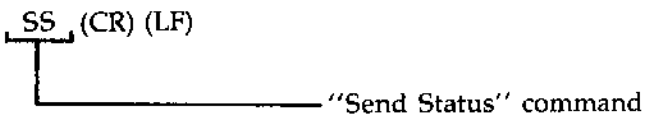


The input command string to cause the instrument to process this sequence is as follows:





After the message sequence has been processed once (single mode), the Exerciser will assert its Service Request flag. To determine what caused the SRQ, a send status command is performed as follows:

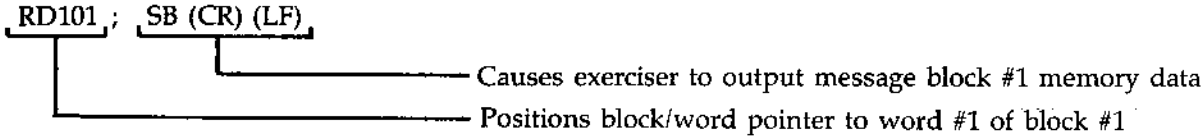


The instrument will reply with:

((LF), if RS-232 interface with echo enabled) BC,S,___2,__10,I,A,171,00,01 (LF)

Serial Poll Status byte = 01 indicates that the 1553 message sequence is complete.

To read the result of message block 1, a Send Block (SB) command is executed as follows:



The instrument will respond to the send block command as follows:

((LF), if RS-232 interface with echo enabled) 0825,0080;1111,0088;1234,0088; 7654,0088;7777,0088;5555,0088;0C00,8080 (LF)

To read the results of message block 2, perform a Next Block (NB) and a Send Block (SB):

NBSB (CR) (LF)

The reply string will be:

((LF), if RS-232 interface with echo enabled) 1023,0080;1C23,0088;1800,8080; ABCD,80C0;8888,80C0;5678;80C0;1000,8080(LF)

If the command sequence is processed using the IEEE-488 (GPIB) interface, the EOI handshake line will be asserted with the terminating linefeed (LF) character for each reply string.

2.11.4 HIGH-SPEED REMOTE I/O COMMANDS

As discussed in Paragraph 2.11.3, the low-speed remote commands mimic the action of the front panel keyboard. This set of commands allows the Exerciser to be controlled by a host computer in applications where throughput rate is not critical.

The primary purpose of the high-speed commands is to provide a mechanism that may be used to quickly transfer blocks of 1553 command, status and data words between a host computer and the Exerciser's message RAM. A secondary function is to provide a faster means of updating message parameters (format, word count, response and intermessage gap times and block linking information) than is possible via the low-speed commands.

In most applications, the low-speed and high-speed commands are used in conjunction with each other. The low-speed commands must be used to specify set-up parameters such as BC/RT mode, single/repeat operation, blocks per frame, frame time and RT address. Message parameters such as format, data word count, response and intermessage gap times, as well as the programming of command words (BC mode) may be specified using either high-speed or low-speed commands. If these parameters are to be changed in real time (up to about 70 Hz), they must be updated using the high-speed input command. In situations where speed is not a factor, it is more convenient to enter these variables using the low-speed commands, since they may be specified in their user friendly formats using this set of commands. For example, to specify an intermessage gap of 20 us in low-speed mode, simply program IM20. To specify the same thing using the high-speed input command requires that the lower 11 bits of the block control word be designated as 111 11101010, the binary representation of 2034 (2034 = 2054 - 20; refer to paragraph 2.11.4.3).

The important differences between the low-speed and high-speed commands are as follows:

(1) Whereas the low-speed commands and associated data are stored in the queue buffer memory before being processed the high-speed input and output commands (roughly equivalent to the low-speed PG and SB commands) cause data to be transferred directly between the selected I/O port and the Exerciser's message RAM. That is, by programming the host computer to transfer packed binary bytes as opposed to hex or decimal ASCII data, it is possible to bypass the command queue and eliminate the time required to perform the necessary code conversion and arithmetic. Since the high-speed I/O transfers are essentially burst transfers, care must be taken in

the specifying of the burst sizes to avoid hanging the bus, particularly when the IEEE-488 bus is the selected interface.

(2) The high-speed representation of all 1553 command, status and data words is four binary bytes, as opposed to a maximum of seven ASCII characters (including separators) for a low-speed Program (PG) command, or ten ASCII characters (including separators) for a low-speed Send Block (SB) command. There is also a difference in the placement of the Message Error bit. This is discussed in paragraph 2.11.4.2.

(3) Using the high-speed commands, there is full flexibility to load or review any contiguous block of control, command, status or data words in Exerciser message RAM.

(4) Using the high-speed input command, the user has direct access to the control word or word 0 for any given message block. The block control word, which is loaded into the control register of the Exerciser's 1553 processor prior to the processing of messages, contains format, word count, response, intermessage gap time and block linking information. The capability to update the control word on the fly significantly enhances the Exerciser's performance as a real time bus tester. The format parameter that is programmed as part of the control word is defined slightly differently from the format that is specified via the keyboard or the low-speed FR command. This difference is discussed in paragraphs 2.9.1.5, 2.9.2.2 and 2.9.3.4.

(5) When operating by means of the low-speed commands, including GO and HA, a certain amount of structuring of messages and words takes place that does **not** occur when the high-speed commands are used:

(i) In low-speed mode, the control words for the individual message blocks are updated automatically according to the programmed values of format, word count, response and intermessage gap times and block linking parameters.

(ii) Also in low-speed mode, the format and word count portions of the block control word are automatically updated whenever the block's command word (BC mode) is programmed. (Refer to paragraph 2.9.1.5.) The control word is **not** automatically updated when the command word is specified by a high-speed input command. One way around this situation is to program both control parameters and command words via low-speed commands, using the high-speed commands for transfers of data words and go/halt control.

(iii) When the low-speed go command is used, the MSBs of the third and fourth bytes of the 1553 words are used to distinguish between transmitted, received and pending received words. Refer to paragraph 2.7, Table 2-6. When the high-speed go command (!) is used, the encoding of these bits must be performed by the host computer. Alternatively, the user may choose not to specify these bits, in which case their values should be ignored when the message data is reviewed.

2.11.4.1 HIGH-SPEED COMMANDS

There are four high-speed commands. They are data input, data output, go and halt. The high-speed commands and their associated reply strings are indicated in Table 2-18.

Table 2-18. Remote I/O High-Speed Command Table

COMMAND NAME DESCRIPTION	COMMAND STRING SYNTAX	REPLY STRING SYNTAX
High-Speed Data Input	& (Block #) (Starting Word #) (Byte Count (N)) (Byte #1) (Byte #2)...(Byte #N)* The three parameters following the ampersand (&) are formatted in binary. They denote the block number, starting word number within the block and the total number of binary bytes to be transferred from the selected port to message RAM. The starting word number must be in the range from 0 to 49. The word in position 0 is the block control word. There are four binary bytes per word. See Paragraph 2.10 for the hex representation of MIL-STD-1553 Command and Status words.	None
High-Speed Data Output	*(Block #) (Starting Word #) (Byte Count (N)) Similar to the high-speed data input command. The parameters block number, starting word number and byte count are designated in binary.	(Byte #1) (Byte #2)··· (Byte #N)(LF)* N Binary bytes are transferred from message RAM to the selected port. The representation of all control, command, status and data words is comprised of four binary bytes.
High-Speed GO	! Causes the exerciser to execute the programmed 1553 message sequence.	(4 Spaces) Busy
High-Speed Halt	● Causes the exerciser to halt execution following execution of the current frame (B.C. Mode) or current message (R.T. mode)	(4 Spaces) Halt

*When operating over the IEEE—488 interface, the "EOI" handshake line is asserted with the last data byte of the "high-speed" input command string and with the terminating "linefeed" at the end of the "high-speed" output reply string.

2.11.4.2 PROGRAMMING AND TIMING CONSIDERATIONS

For the low-speed remote commands, the 1553 Command, Status and Data words are represented by strings of either six or eight ASCII-coded hex digits. Eight digits are used for the full representation, which includes the fourth (error position) byte. This expanded ASCII hex format, while being more user convenient, is by necessity slower for doing block transfers than is a packed binary format.

For the high-speed input and output commands, the 1553 words are represented by four binary bytes. Referring to Table 2-19, it is seen that the four-byte representation of 1553 words for the high-speed I/O commands is identical to that for the low-speed commands, with the following two exceptions:

1) As denoted by (*), the "Message Error" bit, indicating either a word error or a high word count error, appears in the bit 5 position of the fourth received byte rather than the bit 4 position of the third received byte. The bit 4 position of the third (received word - detected error) byte will always return a 0.

2) The pending-receive/$\overline{\text{transmit}}$ and transmit-receive/$\overline{\text{pending}}$ bits, the MSBs (bit 7) for the third and fourth bytes respectively (denoted by (**)), are positioned the same as in the low-speed representation. However, it should be noted that when the user employs the low-speed go command, as opposed to the high-speed(!) command, the values for these two bits are pre-assigned prior to the processing of the message sequence as follows:

	BYTE 3 "D7" BIT (Pending-receive/$\overline{\text{transmit}}$)	BYTE 4 "D7" BIT (Transmit-receive/$\overline{\text{pending}}$)
For "TRANSMIT" words	0	1
For "PENDING" words	1	0

When using the low-speed go command, this pre-assigning is done by the Exerciser's internal firmware. The action of the instrument's 1553 processor (following either go or !), will be to set both of these bits to logic 1 for all received words only. The bit values do not change for transmitted words.

Since the high-speed GO (!) and HALT(.) commands greatly reduce the amount of instrument firmware overhead time, they will generally be used in conjunction with the Input (&) and Output (*) commands. The user has two options for handling the MSBs of the third and fourth bytes in high-speed mode:

1) Mimic the instrument software by presetting the two bits to their proper values prior to message processing by means of the high-speed input command. This must be done for pending received as well as for transmit words.

2) Ignore the values of these bits following message processing. This introduces the problem of not being able to make a simple determination of received word count. In many applications involving system type testing, this may be acceptable.

Table 2-19. 4-Byte Representation of 1553 Words for High-Speed and DMA (GPIB) Input and Output Commands

BYTE		BIT POSITION							
		D7	D6	D5	D4	D3	D2	D1	D0
1(T-R)	Upper 8 Bits of Data (shown for Data Word)	BIT 1 (MSB)	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8
2(T-R)	Lower 8 Bits of Data (shown for Data Word)	BIT 9	BIT 10	BIT 11	BIT 12	BIT 13	BIT 14	BIT 15	BIT 16 (LSB)
3(T)	Transmit Word: Induced Errors	** Pending-Receive/$\overline{\text{Transmit}}$ (Ø)	Incorrect Sync Type Error	Parity Manchester Error	Sync Zero Crossing Error	Parity Error	Manchester Encoding or Zero - Crossing Deviation Error	Low Bit Count or Message Gap Error	High Bit Count or Word Gap Error
4(T)	Transmit Word: Receive/ Induced Sync/ Manchester Error Position	** Transmit Received/ $\overline{\text{Pending}}$ (1)	Error Type Select (see Table 2.9)	Sync/Zero Crossing Error Position 1	Sync/Zero Crossing Bit Position 0 or High Bit Count Select	Manchester/ Zero - Crossing Bit Position 3	Manchester/ Zero - Crossing Bit Position 2	Manchester/ Zero - Crossing Bit Position 1	Manchester/ Zero - Crossing Bit Position 0
3(R)	Received Word: Detected Errors	** Pending Receive/$\overline{\text{Transmit}}$ (1)	Incorrect Sync Type Error	Early Response Error	Message Error	Parity Error	Manchester Encoding Error	Low Bit Count Error	High Bit Count Error
4(R)	Receive Word: Receive Verification/ Sync Type/ Message Error	** Transmit-Receive/ $\overline{\text{Pending}}$ (1)	Data/$\overline{\text{Command}}$ Status Sync Type	Message Error	NOT USED (ALWAYS 0)				

In order to achieve the fastest Exerciser throughput using the high-speed commands, the following guidelines should be adhered to:

1) Disable the updating of the front-panel display by invoking a low-speed Display Disable (DD) command before implementing any of the high-speed commands. There is considerable firmware overhead time to be saved by freezing (or blanking) the display.

2) The fastest instrument operation will result from not mixing any of the low-speed PG, SB, GO or HA commands with the high-speed (&), (*), (!) and (.) commands. Use the low-speed commands for set-up purposes only. When a string contains both low-speed and high-speed commands, the two sub-strings must be separated by the terminator (CR) (LF); i.e., (low-speed command string) (CR) (LF) (high-speed command string).

3) The high-speed (!) and (.) commands may be used in either Single or Repeat operation. In order to minimize the instrument firmware time delays in situations where data is to be output from the Exerciser following a message sequence, it is best to concatenate the output command (*) and its parameters immediately following the (!) command (for single mode), or the . command (for repeat mode).

   The alternative method, which is a bit slower, but will not momentarily hang the bus when operating over the IEEE-488 (GPIB) interface, is to wait for the Service Request indication following the completion of the Exerciser message sequence. The Serial Poll Status byte may then be read (via an SPE command (GPIB only), or an SS command) and verified to have a value of 01 hex (41 hex, when using the GPIB with the possibility that other Status byte bits may also be set), indicating that the Exerciser's 1553 message sequence has been completed. The controlling device should then proceed with whatever high-speed input or output commands are required.

   These sequences are indicated in Figure 2-24 and illustrated in the examples given in paragraph 2.11.4.4.

4) When the controlling device sends a high-speed output (*) command and associated parameters, it must **immediately** configure the instrument to start sending its reply string. When the IEEE-488 (GPIB) port is the selected interface, this is done by putting the instrument in its Talker Active State (TACS). This is done by sending a My Talk Address (MTA) command (an MTA command automatically unlistens the Exerciser), and then configuring the GPIB handshake to allow the Exerciser to start sending its reply string. When the 8-bit parallel port is the selected interface, the Exerciser will send the first reply character when the $\overline{\text{READ}}$ request input is brought to logic 0. For the RS-232 interface, the reply string will be sent immediately after the output command (and parameters) is received, assuming that the handshake lines are not used. For any of the interfaces, if the Exerciser is not configured to respond within about 1 ms after it is ready for reply to a high-speed output command, the instrument's reply string may become invalid. The reason for this is that there is a fail-safe timing mechanism implemented in the Exerciser firmware. When this timer times out, the instrument assumes there is a problem with the controlling device (or bus) and exits the high-speed mode. When this occurs, the reply string will correspond to the last command loaded to the command queue rather than to the * command.

2.11.4.3 UPDATING MESSAGE CONTROL PARAMETERS VIA THE HIGH-SPEED INPUT COMMAND

As shown in Figure 2-3, the first word of each of the memory blocks dedicated to a particular -1553 message is designated as the block control word.

The Exerciser representation of the control word, like the 1553 Command, Status and Data words, is comprised of four 8-bit bytes. Since the first 1553 bus word (command word) is designated as word 1 of the block, the control word, which precedes it, is designated as word 0.

The control word contains the word count, format, intermessage gap time (BC mode), response time and block linking (RT mode) information that is transferred from the message RAM to the control register of the Exerciser's 1553 processor prior to the processing of the particular message.

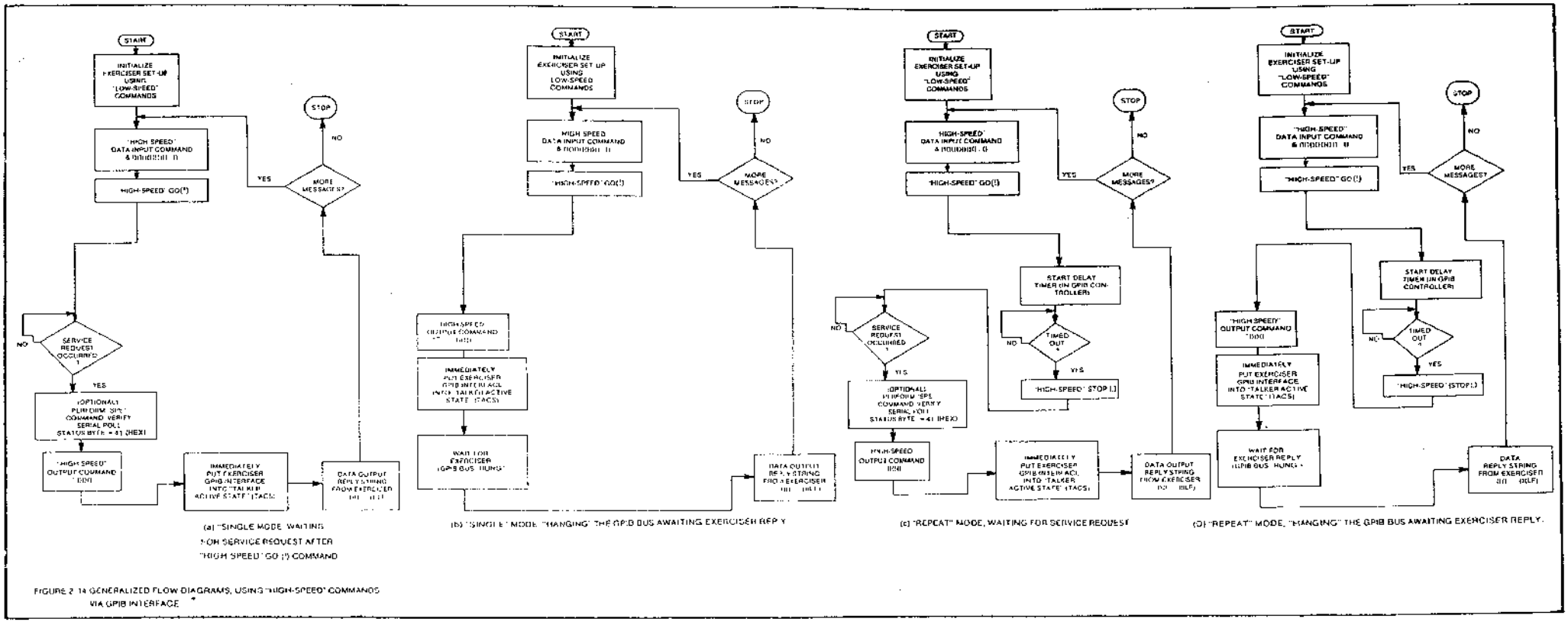


FIGURE 2-14 GENERALIZED FLOW DIAGRAMS, USING "HIGH-SPEED" COMMANDS VIA GPIB INTERFACE

Figure 2-24. Generalized Flow Diagrams, Using High-Speed Commands Via GPIB Interface

When the low-speed commands to update these various parameters are issued to the instrument via the keyboard or a remote interface, a number of internal firmware routines are invoked. These processes include filling and emptying the command queue, parsing the command string and performing the necessary code conversions, arithmetic, etc., to implement the particular command. These routines use up relatively large amounts of time. For test applications where the same message or message frame is repeated a large number of times with no parameter changes (but usually involving block data transfers), applying the low-speed commands once prior to the start of the test sequence for initialization purposes does not pose a severe timing problem. However, for other applications where (for example) formats and word counts are updated prior to each message frame, this might present an intolerable situation. Even though the word count and format information are partially implicit in the message command word (BC mode) or RT address parameter (RT mode), it must be noted that the 1553 processor derives its word count and format information from the **control word, not** the **command word.** Therefore, when using the high-speed input command, it is generally necessary to update **both** words, if either format or word count is changed. This is an important distinction from low-speed mode. The critical difference is that the control word format and word count fields are automatically updated by the Exerciser software when the command word is entered via a low-speed PG command (refer to paragraph 2.9.1.5).

The high-speed input command (&) provides a mechanism for updating the message control parameters in real time.

The Exerciser control word, word 0 for each message block in both BC and RT modes, is defined as follows (Refer to Table 2-20):

Table 2-20. Control Bit Word Assignments

	BIT							
BYTE #	D7	D6	D5	D4	D3	D2	D1	D0
1. (B.C.&R.T.)	NOT USED		(MSB)	WORD COUNT				(LSB)
2. (B.C.&R.T.)	NOT USED		(MSB)	FORMAT				(LSB)
3. (B.C. Mode)	(MSB) "RESPONSE TIME"				(LSB)	(MSB) INTERMESSAGE GAP TIME		
3. (R.T. Mode)	(MSB) "RESPONSE TIME"				(LSB)	NOT USED		
4. (B.C. Mode)	"INTERMESSAGE GAP TIME"							(LSB)
4. (R.T. Mode)	NOT USED				Link Enable/ Disable	(MSB) "Link To" Block		(LSB)

TABLE A.10. "CONTROL WORD" BIT ASSIGNMENTS

BYTE 1: Data Word Count, in binary, as defined in paragraph 2.9.1.5.

BYTE 2: Message Format, in binary, per the High-Speed/DMA Remote I/O formats listed in Tables 2.10 and 2.12.

BYTE 3: Upper five bits (bits 7-3): Response Time: Assuming bit 7 (MSB) to have a bit weight of 128 and bit 3 (LSB of Response Time field) to have a bit weight of 8, the value of these 5 bits should be:

For BC mode: 8*(36-response time), with 5 < = response time < = 31 (us)
For RT mode: 8*(37-response time), with 6 < = response time < = 31 (us).

Note that for RT format 02, the minimum allowable response time is 7 us. It is 6 us for all other message formats in RT mode.

BYTE 3: (Lower 3 bits (bits 2-0)), and

BYTE 4: For BC mode, the three LSBs of byte 3 are part of the Intermessage Gap Time field. For RT mode, these three bits are not used (set to 0).

For BC mode, the three LSBs of the third control byte (D2 is MSB) assume the weights 1024, 512 and 256, while the eight bits of byte 4 are assigned bit weights of 128 (bit 7), 64 (bit 6), ...1 (bit 0). The value of the 11 bits is defined to be: 2054 - intermessage gap time, with 7 < = intermessage gap time < = 2047 (us).

Exerciser intermessage gap time is defined as the time interval from the end of the previous message to the start of the particular message; i.e., the time interval **preceding** the processing of the particular message.

BYTE 4: (Bits 3-0): "Linked to Block" field (RT mode only): If the "linked to" message block is to be enabled either to the same or a different block number, the fourth RT control byte assumes the value of one **less** (0-7) than the number of the "linked to" message block (1-8). If it is desired to specify the "linked to" field as "disabled," the fourth RT control byte should be programmed for a value of eight (8).

The upper four bits of the fourth control byte (bits 7-4) are not used (set to 0) for RT mode.

The control word may be loaded by means of either a high-speed input (&) command or a DMA input command (>).

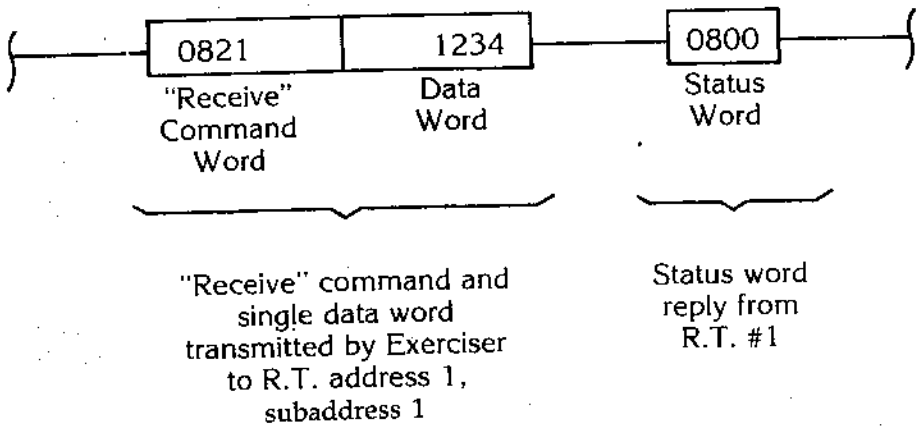
The format byte that is loaded via the high-speed input command is encoded slightly differently than the format that is inputted via a low-speed FR command. The difference is as follows: for the low-speed FR command, the "10" (hex) bit is defined as the T/R reversal error bit. For the format byte in the Exerciser control word that is loaded via a high-speed input command (&), the "10" bit is defined simply as the T/R bit. That is, in general, the 10 bit that should be programmed using the high-speed input command must match the T/R bit from the command word (in BC mode) or the block's RT Address parameter (in RT mode). The exception to this rule is the situation where it is desired to induce a T/R bit reversal error; that is, to send a transmit command word plus data words, or transmit a receive command without data words (BC mode). For this case, the 10 bit of the format byte should be programmed to be the opposite of the T/R bit of the command word or RT address. When the low-speed FR and PG commands are used, this XOR operation is performed internally by the Exerciser firmware.

The differences between the encoding for the low-speed and high-speed format bytes are illustrated in Tables 2-10 and 2-12.

2.11.4.4 EXAMPLE OF EXERCISER OPERATION VIA HIGH-SPEED REMOTE I/O COMMANDS

The operation of the instrument using the high-speed I/O commands is illustrated by the following example.

In the example shown, the Exerciser is controlled by a host computer via its IEEE-488 (GPIB) interface to produce the single-message sequence shown below:



Before invoking the sequence of high-speed commands listed below, the Exerciser must be initialized to Repeat, BC mode with a message count of 1 and a frame time of 2 ms. As an additional means of enhancing speed, the front panel display is disabled and blanked. Using the IEEE-488 interface, the low-speed command string for this configuration is as follows:

(MLA (with ATN)) BCRPBF1;FT2;DD(CR)(LF with EOI) (UNL (with ATN))

As a means of minimizing the amount of Exerciser software overhead time, the parameters for the message to be processed will be loaded via the high-speed input command rather than as a series of low-speed commands. That is, the format, word count, intermessage gap and response time information will be imbedded in the control word, or word 0, which is sent as the first word in the high-speed input command string.

The control word parameters will be as follows. The response and intermessage gap times are not relevant for a single BC-to-RT transfer in BC mode, but are shown for purpose of illustration.

Data Word Count = 1 = 0000 0001 (binary)

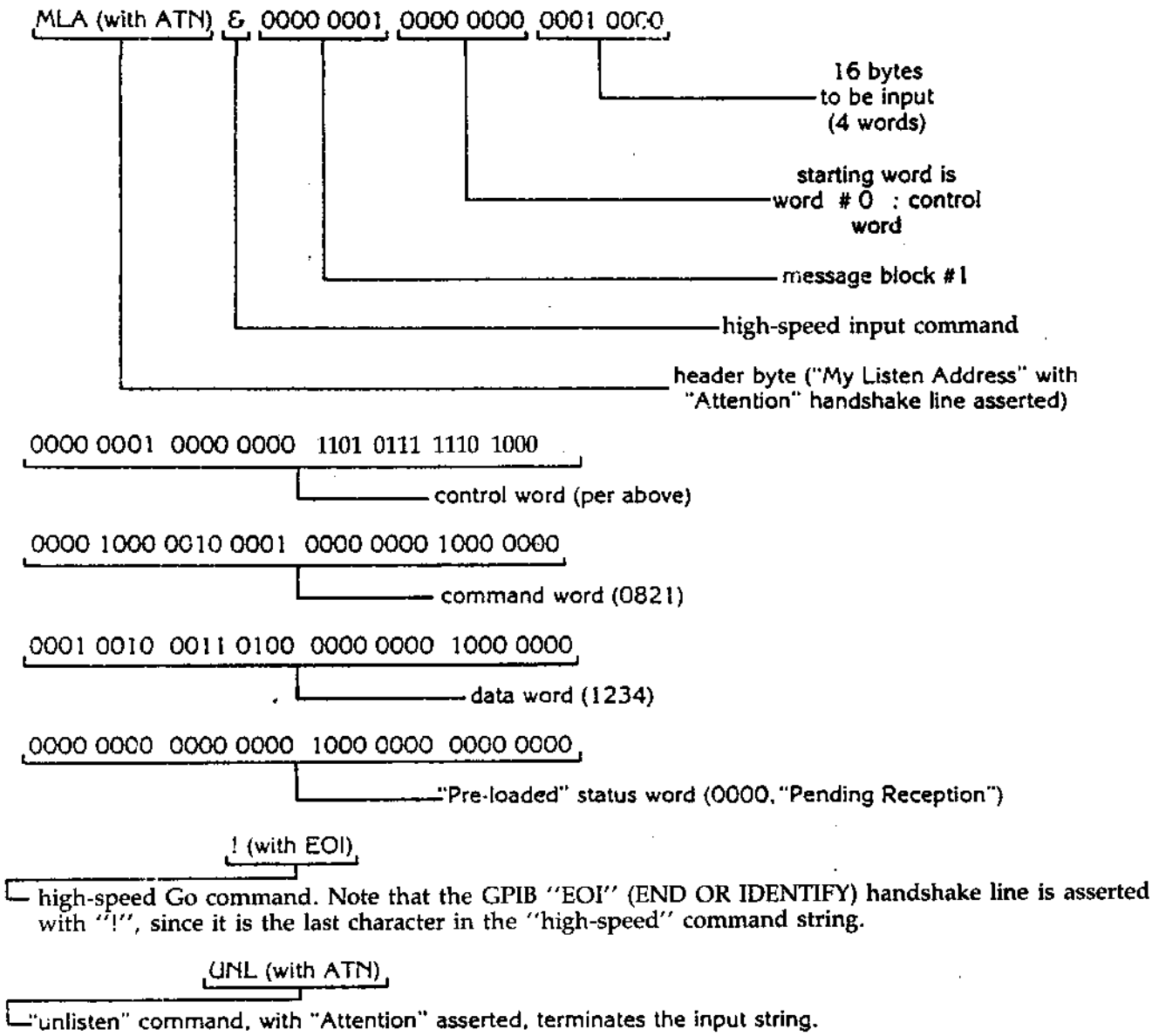
Message Format (per Table 2.8) = 0 = 0000 0000

Response Time = 10 us; therefore, load 8 * (36 - 10) = 208 = 1101 0---

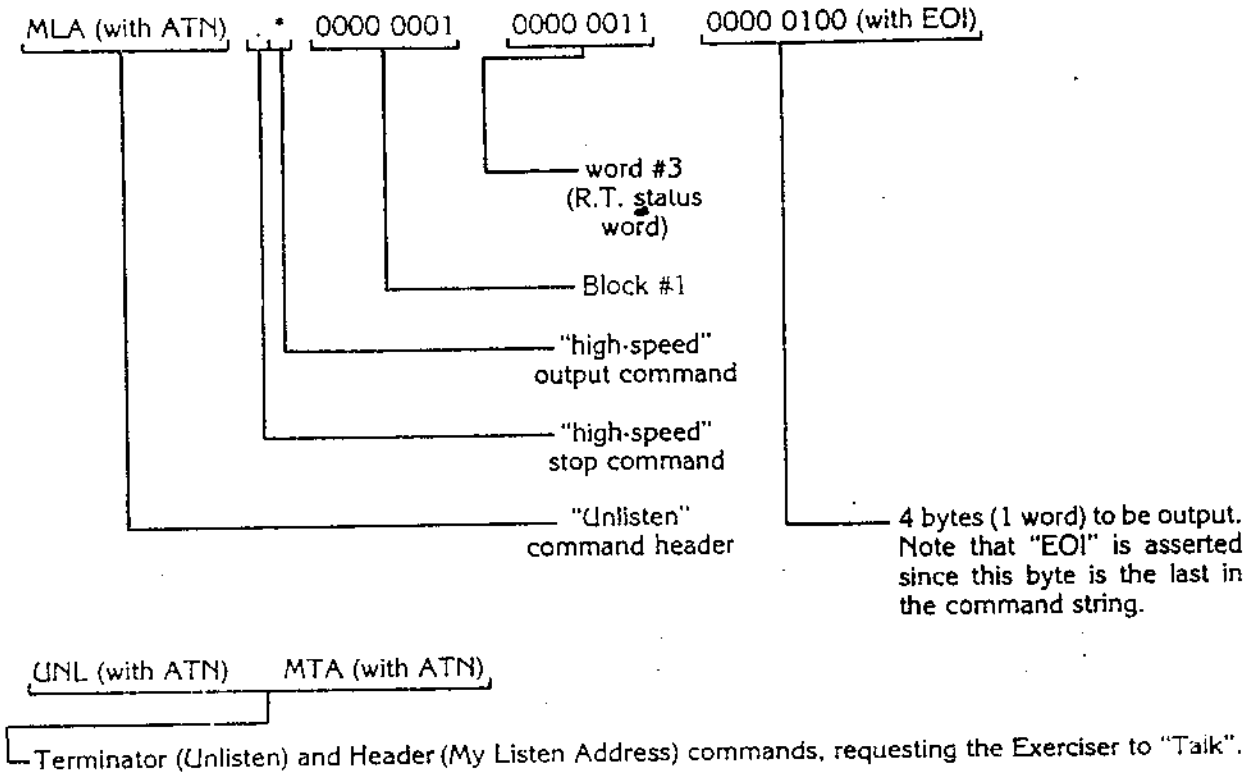
Intermessage Gap Time = 30 us; therefore, load 2054 - 30 = 2024 = ---- -111 1110 1000

Therefore, byte 3 of the control word should be specified as 1101 0111 and byte 4 should be 1110 1000.

The high-speed command string necessary to load the control, command, data and (preloaded) status words and to initiate the BC transmission is as follows:

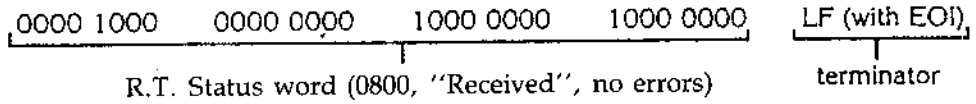


After a suitable delay (20 ms) to allow the Exerciser to repeatedly execute the message sequence, a high-speed stop command followed by a high-speed output command are used to terminate the 1553 transmission and to interrogate the Exerciser for the received RT Status word.



At this time, the GPIB handshake lines must be configured immediately (within 1 ms to avoid a timeout condition) for the Exerciser to talk (reply).

The Exerciser high-speed reply string will be as follows:



2.11.5 IEEE-488 DMA INTERFACE

2.11.5.1 OVERVIEW

As a means of providing a standard, high-speed interface to an ATE host computer, the IEEE-488 (GPIB) interface for the Exerciser incorporates direct memory access (DMA) capability. The design of the GPIB interface for the Exerciser allows the host computer to directly access all memories and registers in the Exerciser's 1553 processor, completely bypassing the instrument's internal microprocessor. The only portion of a DMA input or output command string that the Exerciser handles as programmed I/O is the first five (5) bytes, used for configuring the DMA controller.

By means of the DMA mechanism, it is possible to read and write message and control data to memory and to the various Exerciser registers that control the 1553 processor. This includes:

1) All transmitted and received Command, Status and Data words.

2) All control words to the Exerciser message RAM. As discussed in paragraph 2.11.4, control words are used to program all parameters for individual messages, including format, word count, response time, intermessage gap time and RT "linked to" block address.

3) The RT trigger RAM used for mapping the RT Address/T-R bit combinations for received command words to individual message blocks.

4) Full real time control over BC/RT mode selection and start/stop functions.

5) Additional functions such as message count, transmitter amplitude, response timeout, Channel A/B select, internal/external trigger select and message error indications.

The Exerciser DMA operations are implemented as halt burst transfers. That is, the user specifies the DMA starting address and the number of bytes to be transferred to/from Exerciser memory (or registers). The specified number of bytes are then sequentially written to or read from the Exerciser 64K address space. It should be noted that certain portions of the Exerciser address space have been made inaccessible to the DMA interface to prevent the user from inadvertently "crashing" the instrument microprocessor. The inaccessible address locations include the microprocessor PROM, scratchpad RAM and I/O ports.

The total time required for a DMA burst (either in or out) is approximately 1.2 ms of overhead "set-up" time plus slightly under 10 us per byte transferred. The Exerciser GPIB handshake timing for DMA transfers is shown for reference in Figure 2-27.

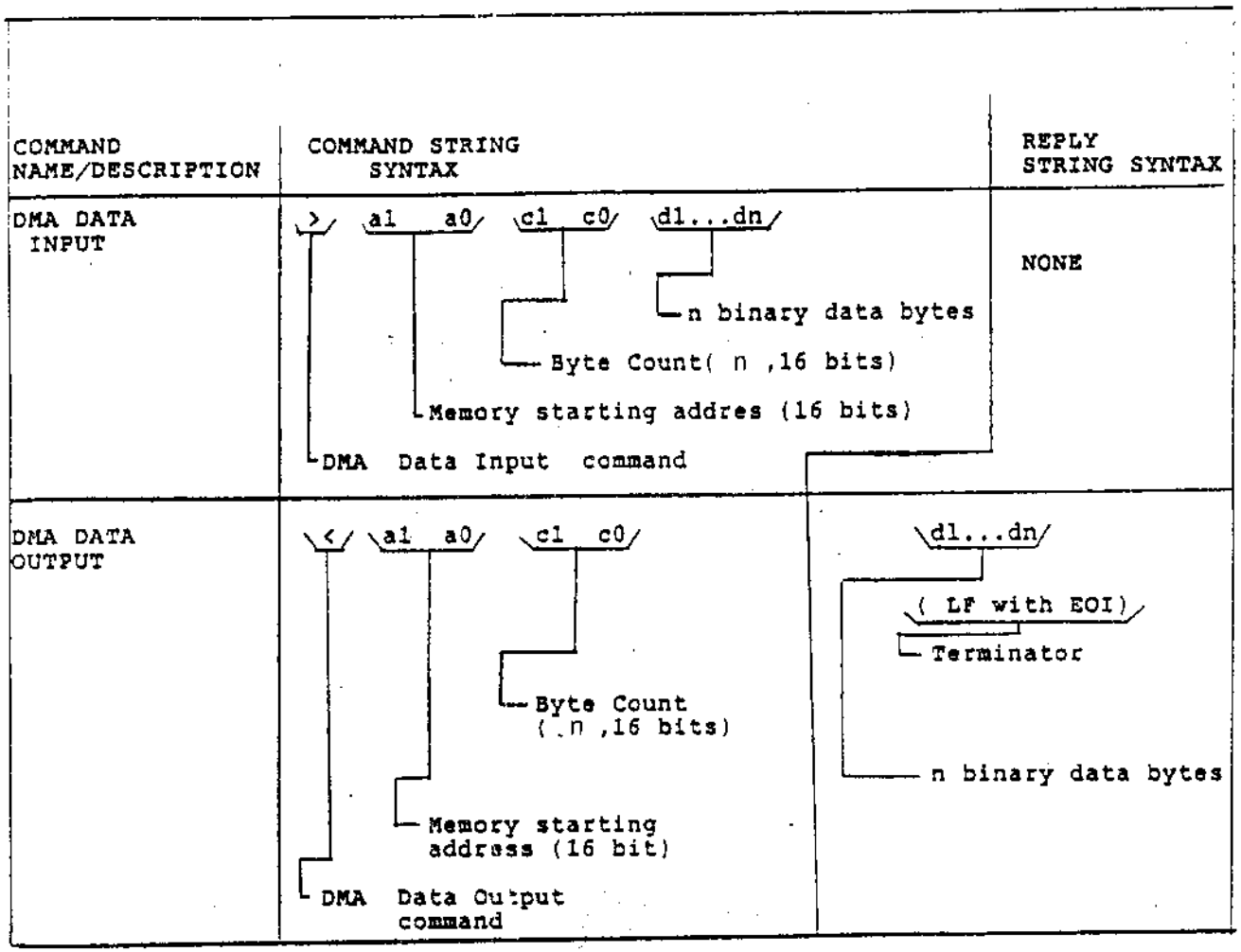
There is also a DMA "failsafe" timeout. This timer, which prevents the Exerciser from "locking up" in the event of a problem in the host computer or the GPIB handshaking circuitry, flags a fault condition if there is an excessive time interval between byte transfers. This time, which is user selectable, is factory configured for its minimum setting of 427 ms. A DMA timeout fault results in a GPIB Service Request and sets a bit in the Serial Poll Status byte.

2.11.5.2 DMA COMMANDS

There are two (2) DMA commands: DMA input and DMA output. Both commands are comprised of a single ASCII command character (byte), followed by four (4) parameter bytes specifying the 16-bit (binary) starting address in the Exerciser address space and the 16-bit (binary) byte count indicating the length of the burst to be transferred.

The two DMA commands are listed in Table 2-21.

Table 2-21. DMA Commands



2.11.5.3 DMA ADDRESS AND BIT MAPPING FOR EXERCISER MEMORY AND REGISTERS

Table 2-22 lists locations of the Exerciser memory address space that are accessible via the GPIB DMA:

Table 2-22. Exerciser Memory Address Locations

ADDRESS/RANGE (HEX)	DESCRIPTION	READ/WRITE
1000-17FF	Message RAM	R/W
1800-18FF (Lower 4 Data bits only)	R.T. Address "Trigger" RAM	R/W
3802	Mode Set-up Register	R,R/W
1C00	Message Count Register	W
6000	Transmitter Amplitude Register	W
6200	Channel Select/Internal-External Trigger Select/ Response Timeout Register	W
3C00	Error Status Register	R

2.11.5.4 MESSAGE RAM ORGANIZATION (HEX ADDRESS 1000-17FF, R/W)

The message RAM, which stores all message block control words, as well as all command, status and data words to be transmitted or received, is organized as shown below. All locations of the message RAM are read/writable.

ADDRESS (HEX)	BYTE	DESCRIPTION
1000	Message Block #1:	Control Word byte #1
1001	Message Block #1:	Control Word byte #2
1002	Message Block #1:	Control Word byte #3
1003	Message Block #1:	Control word byte #4
1004	Message Block #1:	Word #1, byte #1
1005	Message Block #1:	Word #1, byte #2
1006	Message Block #1:	Word #1, byte #3
1007	Message Block #1:	Word #1, byte #4
1008	Message Block #1:	Word #2, byte #1
.	.	
.	.	
.	.	
10C7	Message Block #1:	Word #49, byte #4
.	.	
.	.	
1100	Message block #2:	Control Word, Byte #1
.	.	
.	.	
.	.	
11C7	Message block #2:	Word #49, byte #4
.	.	
.	.	
.	.	
1200	Message block #3:	Control word, byte #1
.	.	
.	.	
.	.	
1700	Message block #8:	Control Word, byte #1
.	.	
.	.	
.	.	
17C7	Message block #8:	Word #49, byte #4

It should be noted that the last 56 bytes of each message block, locations 10C8-10FF, 11C8-11FF,...17C8-17FF are NOT used by the Exerciser.

2.11.5.5 RT TRIGGER RAM ORGANIZATION (HEX ADDRESS 1800-18FF, R/W)

The RT trigger RAM is a 256 X 4 dual-ported RAM that acts as a mapping mechanism from the RT address and T/R bit fields of valid received command words that are decoded from the 1553 bus. When the Exerciser is in RT mode, the RAM outputs the upper three bits of the message RAM address, which comprise the Exerciser block address. In addition, the RT trigger RAM, which is fully read/writable, has a fourth output signal, VU-L, which, when asserted low, indicates that the RT address and T/R bit fields of the command word map to one of the Enabled Exerciser message RAM blocks (i.e., the particular address/T/R bit combination is simulated by the instrument). The block diagram of Figure 2-25 indicates a schematic representation of the trigger RAM circuitry.

The address bit mapping of the trigger RAM is as follows:

A7: Data/$\overline{\text{Command-Status Sync}}$ (must be 0)
A6: $\overline{\text{Valid Word}}$ (must be 0)
A5: Command Word T/$\overline{\text{R}}$ BIT
A4: Command Word RT Address 4 (MSB)
A3: Command Word RT Address 3
A2: Command Word RT Address 2
A1: Command Word RT Address 1
A0: Command Word RT Address 0 (LSB)

The data bit mapping of the trigger RAM is as follows:

D7, D6, D5, D4 : NOT USED (RAM is 256X4)
D3 : VU-L: when low indicates that the RT address - T/$\overline{\text{R}}$ bit combination of the received command word is simulated by the Exerciser (RT Enabled).
D2 : EXERCISER MESSAGE BLOCK ADDRESS 2 (MSB)
D1 : EXERCISER MESSAGE BLOCK ADDRESS 1
D0 : EXERCISER MESSAGE BLOCK ADDRESS 0 (LSB)

To disable all eight message blocks, write 8 to all 256 locations of the trigger RAM.

When enabling a specific Exerciser message block to simulate a given "RT address/T-R bit" combination, it should be kept in mind that, in general, the specified data will be accessed only the **FIRST** time that a command word is directed to the respective RT address/T-R bit combination. When the simulated RT is addressed subsequently, it is possible that the contents of the trigger RAM may have been overwritten by means of the "RT Block Linking" mechanism. The exact sequence of message blocks (after the first "enabled" or "head" block) that simulates a given RT is under control of the **control** words in the message RAM, **not** the **trigger** RAM.

Therefore, in order to enable a given block to simulate a given RT address/T-R bit combination the **FIRST** time that the appropriate command is received, write the data defined as (Exerciser block number -1) to the address location defined by (1800(hex)) + (RT address) + (0 for receive, 32 for transmit)).

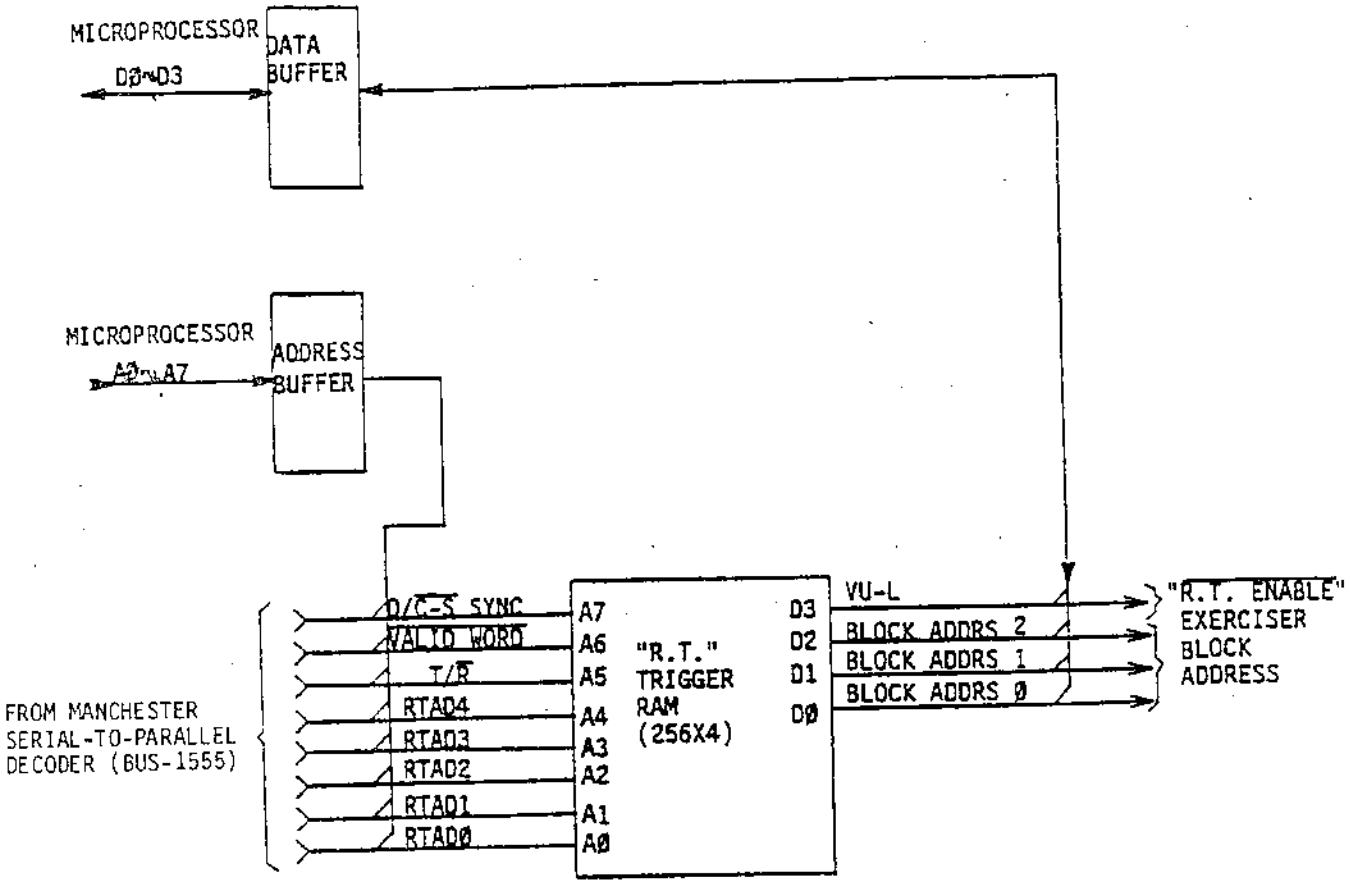


Figure 2-25. RT Trigger RAM Block Diagram

To disable a previously enabled block, write 8 to the address location defined above. It should be noted that whenever the RT address or TR bit for a given block is changed, it is necessary to first disable the currently programmed (Enabled) address, before enabling the new RT address/T-R bit combination for the respective message block.

2.11.5.6 MODE SET-UP REGISTER (HEX ADDRESS 3802; BITS 7,6,4,3,2,1 AND 0 ARE READ/WRITE; BIT 5 IS READ ONLY)

This register is used for configuring the Exerciser for its various operating modes. It is also used in conjunction with the Message Count register (paragraph 2.11.5.7) for start/stop control. The set-up/start/stop sequences for the various Exerciser operating modes are discussed in paragraph 2.11.5.11. The bit mapping for the mode/set-up register is as follows:

BIT	DESCRIPTION	
7 (MSB)	RT-MON/$\overline{BC}$	(R/W)
6	ON-LINE	(R/W)
5	FRAME ENABLE	(READ ONLY)
4	$\overline{\text{REPEAT RT MODE}}$	(R/W)
3	BC-MON/$\overline{RT}$	(R/W)
2	SELF-TEST	(R/W)
1	NOT USED	(R/W)
0 (LSB)	NOT USED	(R/W)

2.11.5.6.1 RT-MODE/$\overline{BC}$(R/W) AND BC-MON/$\overline{RT}$(R/W)

These two bits select the Exerciser mode of operation as follows:

MODE	RT-MODE/$\overline{BC}$(Bit 7)	BC-MON/RT(Bit 3)
BC	0	1
RT	1	0
Monitor (Not implemented)	1	1
Invalid Combination	0	0

2.11.5.6.2 ON-LINE (R/W)

This bit should be set high to enable BC or "Single" mode RT operation to start after the Message Count register has been written to. To enable "Repeat" RT MODE operation, this bit should be kept high with $\overline{\text{REPEAT RT MODE}}$ (bit 4) held low. ON-LINE should be held low at all other times when the Exerciser is not operating in BC or RT mode.

2.11.5.6.3 FRAME ENABLE (READ ONLY)

Frame enable is a read only bit that indicates, when high, that the Exerciser is currently either processing a single frame of up to eight messages in either BC or RT mode or is "on-line" for continuous RT operation.

2.11.5.6.4 REPEAT RT MODE (R/W)

For repeat (continuous) RT operation, this bit should be held low with ON-LINE set high. REPEAT RT MODE should be kept high at all other times.

2.11.5.6.5 SELF-TEST (R/W)

This bit should be set high when performing an internal encoder/decoder wraparound self-test, utilizing BC format 20. SELF-TEST, which has the effect of inhibiting the transmitter (preventing traffic on the external serial bus) and routing the encoder serial outputs directly to the decoder inputs, should be set low at all other times.

2.11.5.7 MESSAGE COUNT REGISTER (HEX ADDRESS 1C00, WRITE ONLY)

The bit definitions for the message count register are as follows:

BIT	DESCRIPTION
7 (MSB)	NOT USED
.	.
.	.
.	.
3	NOT USED
2	MESSAGE COUNT 2
1	MESSAGE COUNT 1
0	MESSAGE COUNT 0

This register is used for controlling the processing of a single frame of from 1 to 8 messages in single BC or RT modes. It is not used in repeat RT mode. Writing to the message count register has two effects:

1) The number one **LESS** (0 to 7) than the actual number of messages to be processed (1 to 8) is specified directly by the lower three bits.

2) When configured for Internal trigger, writing to the MESSAGE COUNT register has the effect of bringing the "FRAME ENABLE" signal in the Exerciser's 1553 processor high. When configured for External trigger, frame enable goes high after: (1) the message count register has been written to, **and** (2) the TRIGGER INPUT signal has been asserted low. When FRAME ENABLE goes high in BC mode, the Exerciser initiates its frame sequence (1 to 8 messages). For single RT mode, FRAME ENABLE going high puts the Exerciser on-line. For both BC and single RT modes, frame enable goes low, and the Exerciser goes off-line after the number of messages specified by the MESSAGE COUNT register has been processed.

2.11.5.8 TRANSMITTER AMPLITUDE (HEX ADDRESS 6000, WRITE ONLY)

Writing to this register has the effect of controlling the relative transmitter amplitude. The register contents (range 0 to 255) relate directly to the transmitter amplitude level, which varies from 0 to approximately 9.75 volts peak-to-peak direct-coupled across 35 ohms, or 0 to 30 Vpp transformer-coupled, open-circuited. The relationship between the contents of the Transmitter Amplitude register and the peak-to-peak amplitude is approximately linear for register contents above 15.

2.11.5.9 CHANNEL SELECT/INTERNAL-EXTERNAL TRIGGER SELECT/RESPONSE TIMEOUT REGISTER (HEX ADDRESS 6200; WRITE ONLY)

The bit definitions for this register are as follows:

BIT	DEFINITION
7 (MSB)	CHANNEL $\overline{A}$/B SELECT
6	$\overline{\text{INTERNAL}}$/EXTERNAL TRIGGER SELECT
5	NOT USED
4	RESPONSE TIMEOUT 4 (MSB)
3	RESPONSE TIMEOUT 3
2	RESPONSE TIMEOUT 2
1	RESPONSE TIMEOUT 1
0	RESPONSE TIMEOUT 0 (LSB)

2.11.5.9.1 CHANNEL A/B SELECT

Setting this bit low specifies Channel A as the active bus channel for the front and rear panel 1553 bus connectors. Setting this bit high specifies Channel B as the active channel.

2.11.5.9.2 INTERNAL/EXTERNAL TRIGGER SELECT

Setting this bit low specifies normal Internal triggering to initiate a BC frame sequence. Setting this bit high specifies External triggering, which is used for the bus switching test for dual redundant RTs. Use of the External trigger feature is discussed in detail in paragraph 2.9.5.

2.11.5.9.3 RESPONSE TIMEOUT 4 (MSB) THROUGH RESPONSE TIMEOUT 0 (LSB)

These 5 bits are used to specify the response timeout time for external RTs. The value of these 5 bits corresponds directly to the response timeout value, in microseconds, per the MIL-STD-1553B definition of response time. The allowable range for response timeout is 5 to 32 us., in 1 us steps. Programming the RESPONSE TIMEOUT bits to zero (0) results in a timeout value of 32 us.

2.11.5.10 ERROR STATUS REGISTER (HEX ADDRESS 3C00; READ ONLY)

The bit definitions for this register are as follows:

BIT	DEFINITION
7 (MSB)	NOT USED
6	NOT USED
5	NOT USED
4	NOT USED
3	NOT USED
2	BUS FAULT
1	REPLY TIMEOUT
0 (LSB)	TRANSMITTER TIMEOUT

2.11.5.10.1 BUS FAULT

When this bit is high, it indicates that a word, word count or format error has occurred in the current or last completed message frame for BC mode or in the current or last completed message for RT mode. The BUS FAULT bit is cleared at the start of a message frame in BC and RT modes and at the start of each message involving an RT simulated by the Exerciser for RT mode.

2.11.5.10.2 REPLY TIMEOUT

When this bit is high, it indicates that an external RT has responded later than the programmed value for response timeout, or earlier than 4 us (per MIL-STD-1553B). The REPLY TIMEOUT bit is cleared at the start of each message frame for BC and RT modes and at the start of each message involving an RT simulated by the Exerciser for RT mode.

2.11.5.10.3 TRANSMITTER TIMEOUT

This output high indicates that there has been continuous activity on the bus for longer than 800 us. The TRANSMITTER TIMEOUT bit is reset at the start of each message frame for BC or RT modes.

2.11.5.11 CONTROL/START/STOP SEQUENCES VIA DMA

It is possible to fully control the Exerciser's 1553 processor by performing sequences of DMA input and output commands using the IEEE-488 interface. The DMA commands provide the fastest means of moving blocks of data into and out of the Exerciser's message RAM.

It is also possible to control the actual starting and stopping of the 1553 processor via DMA commands. For example, it is possible to initiate a BC frame sequence by writing a single byte to the message count register. In other situations that do not require the fastest throughput rate, it may prove more convenient to make use of the high-speed go (!) and halt (.) commands discussed in paragraph 2.11.4. The advantages of using the high-speed go and halt commands are:

1) When the Exerciser completes a 1553 message sequence that was initiated by a high speed GO (!) command, it will provide a Service Request indication to the GPIB controller. If the start/stop sequence is controlled by DMA commands, it becomes necessary for the controller to poll the FRAME ENABLE bit (bit 5) of the MODE SET-UP register via a DMA output command. This entails a high level of overhead for the controller.

2) For "Repeat" BC operation, the functions of frame timing and frame re-starting are handled by the internal Exerciser software. If the same control functions are done by DMA commands, the amount of controller overhead is increased.

3) For BC mode tests involving the "External Trigger" function, it is not possible in some instances to determine whether or not a message frame has been processed using the DMA commands only. Therefore, it is strongly recommended that the high-speed GO (!) and halt (.) commands be used when in "External Trigger" mode.

The flowchart of Figure 2-26 illustrates the general sequences for controlling the Exerciser 1553 processor by means of DMA Input and Output commands. The DMA and high-speed command sequences required to configure, start and stop the 1553 processor for the various operating modes are indicated in Table 2-23.

2.11.5.12 DMA TIMEOUT

The DMA interface is configured with a timeout circuit. The timeout circuit monitors each DMA transfer burst in order to detect a fault in the Exerciser IEEE-488 interface, the GPIB BUS or the GPIB controller hardware or software. It will detect low byte count errors as well as hard failures in the IEEE-488 interface.

The operation of the timeout circuit is as follows:

1) The timer is reset at the start of each DMA transfer burst.

2) The timer is reset on each trailing (electrically rising) edge of the "Data Valid" (DAV) GPIB handshake signal. This edge markes the end of each byte transfer cycle, since it indicates that the "Talker" device has acknowledged that the "Listener" device has accepted the last data byte.

3) If there is no trailing edge of DAV within the allotted timeout period (indicating no byte has been transferred during this timeout interval), the timer times out. This results in the following action being taken by the Exerciser:

   (i) The DMA transfer burst is aborted.

   (ii) The GPIB Service Request output (SRQ) is asserted low.

   (iii) The GPIB Serial Poll Status byte will indicate a hex value of 50 in response to a Serial Poll Enable (SPE) command. Bit 4 ("10" bit) of the serial Poll Status byte for the Exerciser is defined as DMA TIMEOUT.

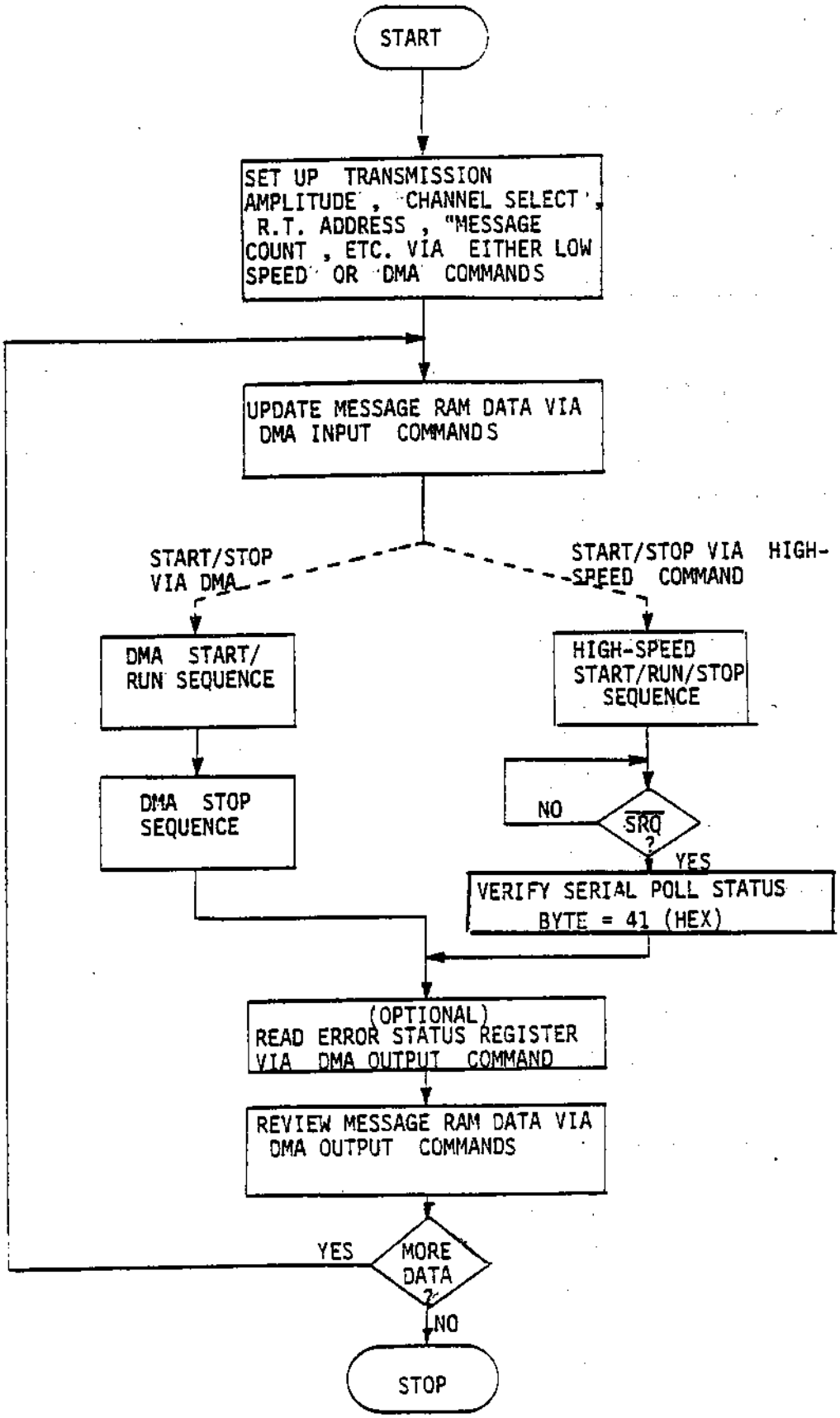


Figure 2-26. DMA Start/Stop Flowchart

Table 2-23. Configure/Start/Stop High-Speed and DMA Command Sequences

OPERATING MODE	"CONFIGURE/START" SEQUENCE	"STOP" SEQUENCE
BUS CONTROLLER		
Single-frame, Internal Trigger (High-Speed)	High-Speed Go(!)	Wait for SRQ
Single Frame, Internal Trigger, Not Self-Test, (DMA)	Write 58 (hex) to Mode Set-up Register. Write to MESSAGE COUNT REGISTER	Poll Frame Enable bit (bit 5) of MODE SET-UP REGISTER until it is low. Write 18 (hex) to MODE SET-UP REGISTER.
Single Frame, Internal Trigger, Self-Test (DMA)	Write 5C (hex) to Mode Set-up Register. Write (Message Count-1) to MESSAGE COUNT REGISTER	Poll Frame Eanble bit (bits 5) of MODE SET-UP REGISTER until it is low. Write 18 (hex) to MODE SET-UP REGISTER.
Single Frame, External Trigger (High-Speed)	High-Speed GO(!)	Wait for SRQ. If there is no SRQ within an appropriate time period, send a High-Speed HALT(.)
Repeat Operation, Internal Trigger (High-Speed).	High-Speed GO(!) Wait	High-Speed HALT(.) Wait for SRQ.
Repeat Operation, Internal Trigger, Not Self-Test (DMA)	(1) Write 58 (hex) to MODE SET-UP REGISTER. (2) Write to MESSAGE COUNT REGISTER. (3) Delay for desired Frame Time. (4) (Optional) Poll FRAME ENABLE bit (bit 5) of MODE SET-UP REGISTER until it is low. (5) Repeat steps (2), (3)&(4).	Following step (3), poll Frame Enable bit (bit 5) of MODE SET-UP REGISTER until it is low. Write 18 (hex) to Mode Set-up Register.

Table 2-23. Configure/Start/Stop High-Speed and DMA Command Sequences - cont.

OPERATING MODE	"CONFIGURE/START" SEQUENCE	"STOP" SEQUENCE
Repeat Operation, Internal Trigger, Self-Test (DMA)	Same sequence as above except write 5C instead of 58 to MODE SET-UP REGISTER in step (1)	Same sequence as above.
Repeat Operation, External Trigger (High-Speed)	High-Speed GO(!) Wait	High-speed HALT(.) Wait for SRQ
REMOTE TERMINAL		
Single Frame (High-Speed)	High-Speed GO(!)	Wait for SRQ. If there is no SRQ within an appropriate time period, send a High-Speed HALT (.) and wait for SRQ.
Single Frame (DMA)	Write D0 (hex) to MODE SET-UP REGISTER. Write to MESSAGE COUNT REGISTER.	Poll FRAME ENABLE bit (bit 5) of MODE SET-UP REGISTER until low or until an appropriate time has elapsed. Write 90 (hex) to MODE SET-UP REGISTER.
Repeat Operation (High-Speed)	High-Speed GO(!)	High-speed HALT(.) Wait for SRQ.
Repeat Operation (DMA)	Write C0 (hex) to MODE SET-UP REGISTER.	Writer 90 (HEX) to MODE SET-UP REGISTER.

The value of the DMA timeout time interval is user-selectable. By means of the jumpers used to select the baud rate for the Exerciser's RS-232 interface (paragraph 2.11.2.3), the DMA "inter-byte" timeout value may be selected to be in the range from 427 ms (factory setting) to about 30 seconds. A long time interval for DMA timeout is useful in situations when the IEEE-488 bus traffic is being monitored by a GPIB analyzer. Table 2-24 lists the possible DMA timeout values and corresponding RS-232 baud rates with the required bottom board jumpers for each. Refer to Figure 2-22 for the locations of the jumper points on the bottom board.

Table 2-24. DMA Timeout Value Jumpers

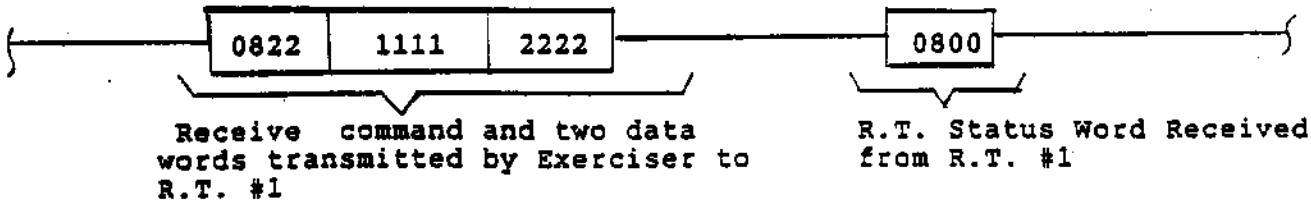
DMA Inter-byte Timeout(Seconds)	RS-232 Baud Rate(Bits/second)	X= Jumper Required			
		E19 to E20	E21 to E22	E23 to E24	E25 to E26
30.454	134.5	X		X	X
27.307	150	X		X	
13.653	300	X			X
6.827	600	X			
4.551	900		X	X	
3.413	1200		X	X	
2.276	1800		X		X
1.707	2400		X		
1.138	3600			X	X
.853	4800			X	
.569	7200				X
.427*	9600*				

*Factory Setting

2.11.5.13 EXAMPLES OF EXERCISER OPERATION VIA DMA COMMANDS

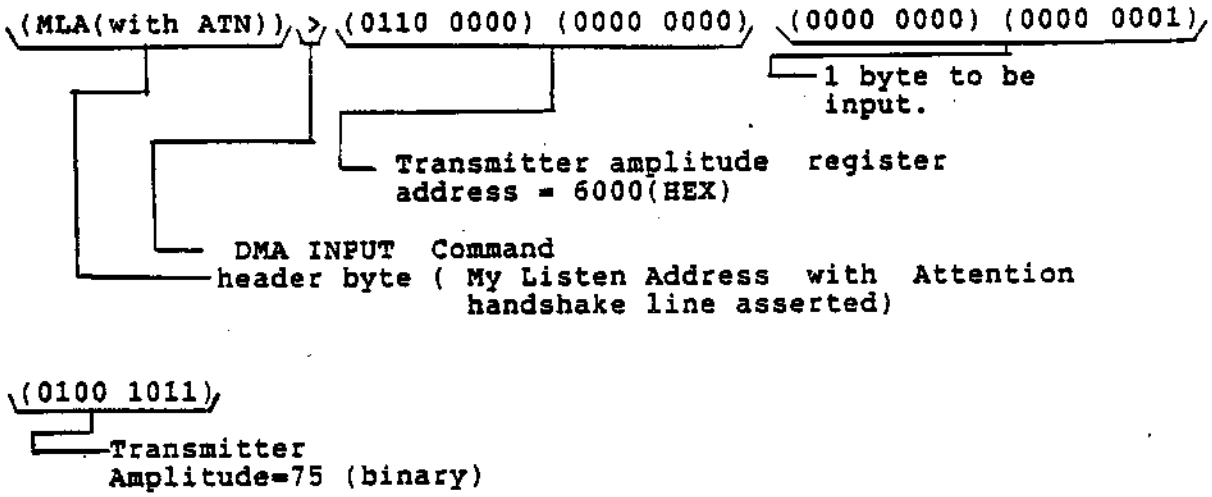
The operation of the Exerciser using the DMA commands is illustrated by the following two examples.

In the first example, the Exerciser is configured for BC mode. By means of DMA and high-speed commands over the IEEE-488 (GPIB) interface, the instrument processes the following single-message sequence:



It is assumed, for this example, that the Exerciser has been previously configured for "Single" BC mode.

To program the Exerciser for a transmission amplitude of approximately 3 Vpp, a level of 75 is specified via the DMA as follows:



Similar to the example of instrument operation using high-speed commands outlined in paragraph 2.11.4.4, the message parameters will be loaded by means of the message control word, via the DMA. The response time and intermessage gap time parameters are included in the example for purposes of illustration.

The control word parameters will be as follows:

Data word count = 2 = 0000 0010 (binary)
Message format = 0 = 0000 0000 (binary)

Response time = 9 us and intermessage gap time = 20 us

By referring to paragraph 2.11.4.3, it is seen that the third byte becomes

8 * (36 - 9) + 7

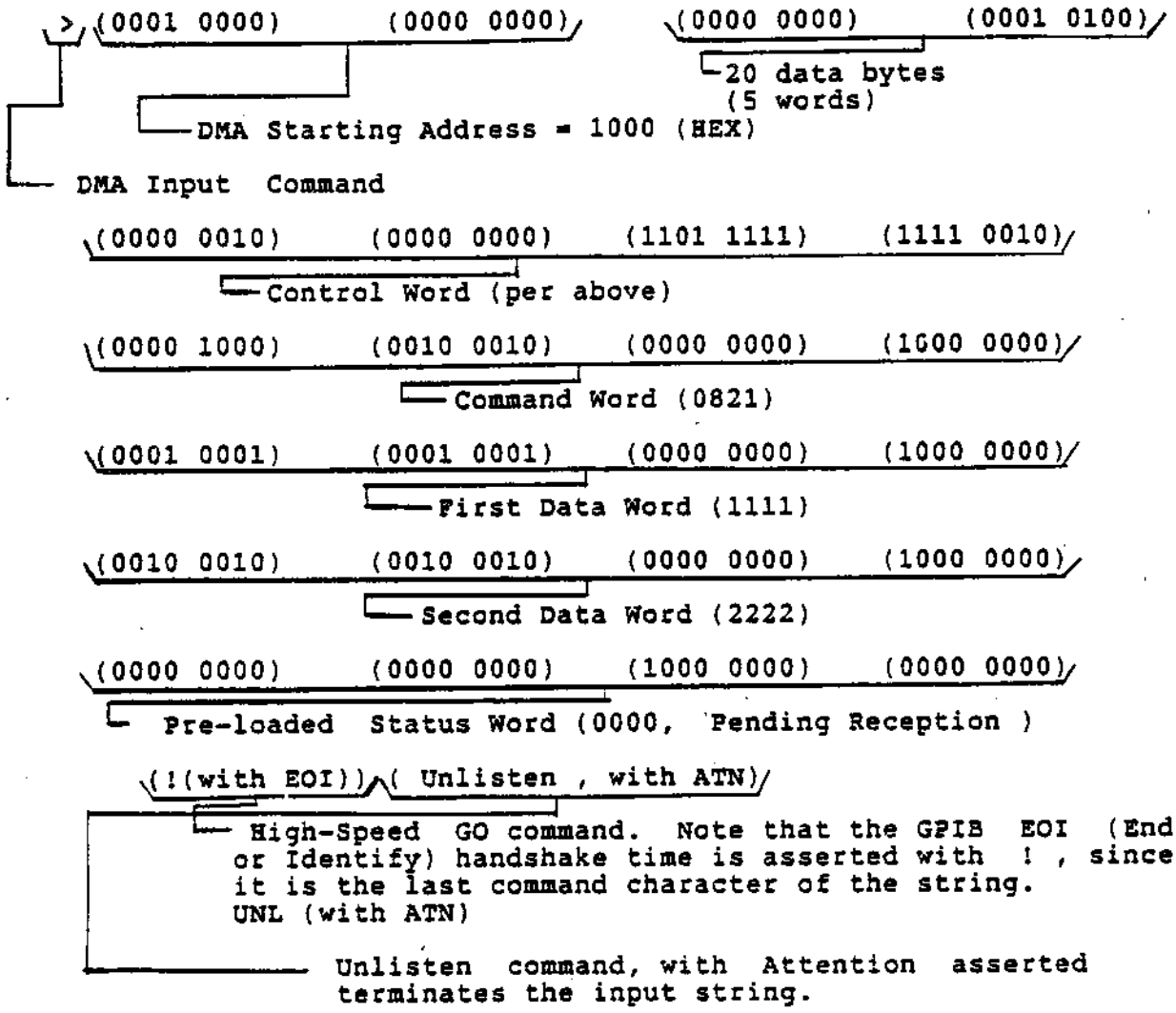
= 223 = 1101 1111 (binary), and

the fourth byte becomes

242 = 1111 0010 (binary)

The third and fourth bytes specify a response time (not applicable, shown for purpose of example only) of 9 us and an intermessage gap time of 20 us.

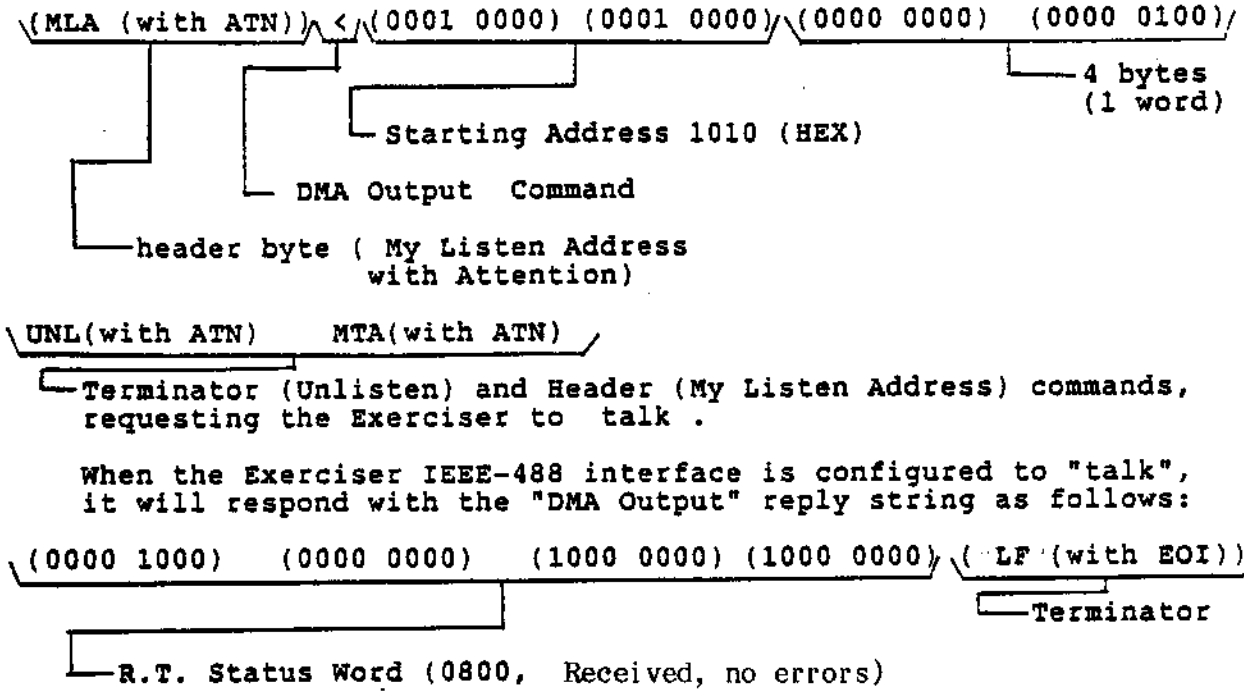
The DMA input string necessary to load the control word, Command word, two Data words and preloaded (pending received) Status word into the first five word positions (starting at position 0) of message block 1 is as follows:



Since the Exerciser is in "Single" BC mode, is will process the programmed single-frame message sequence once, and then assert its GPIB Service Request (SRQ) output.

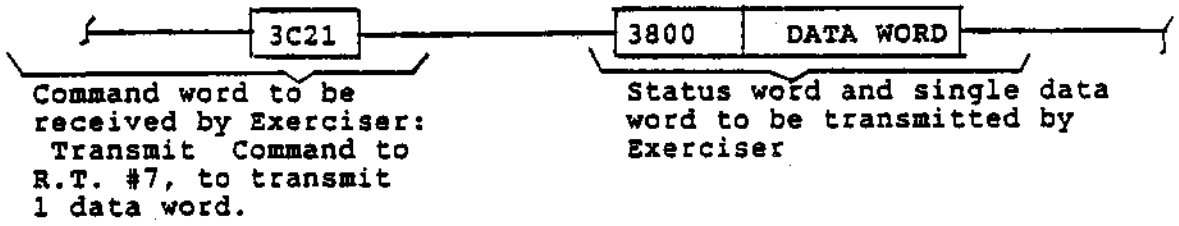
The GPIB controller may then determine that the cause of the SRQ is a "1553 Message Sequence Complete" condition in the Exerciser. This is done by performing a serial Poll Enable (SPE) sequence and verifying for a Serial Poll Status byte of 41 (hex) from the Exerciser.

The GPIB controller may then invoke a DMA Output command to verify the RT status word. This is performed as follows:



The second example of Exerciser operation using the DMA commands involves configuring the instrument for RT mode.

For this example, the Exerciser will simulate RT Address 7 for two messages. It will respond by transmitting status and one data word for each message. The two messages will be formatted as shown:

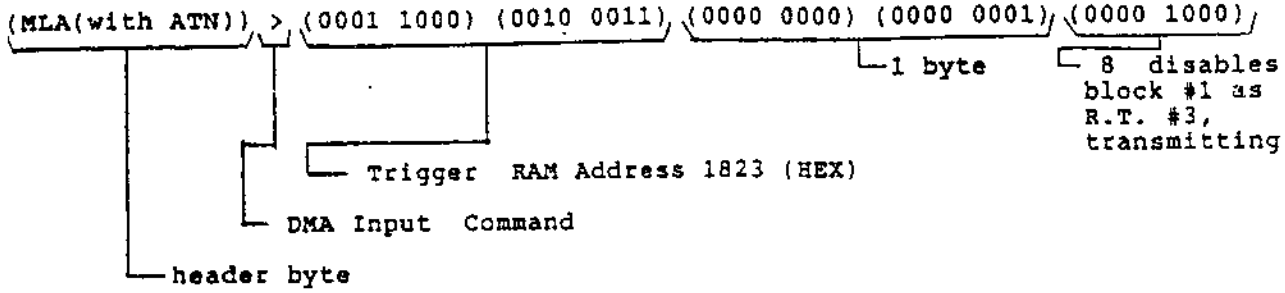


In this example, the Exerciser makes use of the RT "Block Linking" feature. That is, it will respond with a different data word for the two messages: the data word for the first message will be 1357, the data word for the second message will be 2468.

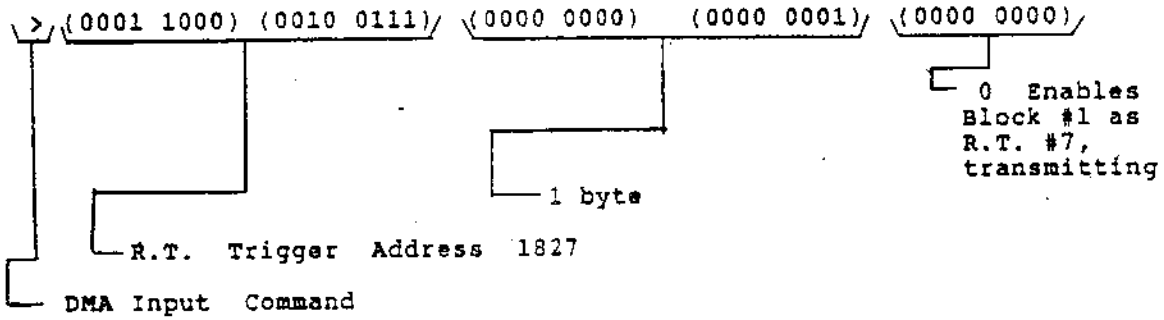
Since, for this example, **all** I/O is being done via DMA, it should be understood that two functions normally done by the instrument internal firmware must be performed by means of the DMA interface. These two functions are: (1) Loading the trigger RAM (for RT address mapping), and (2) Loading the RT Status reply word.

It is assumed that the Exerciser has been previously configured for RT mode with message block 1 simulating RT 3 transmitting, with the other seven message blocks disabled.

The first DMA command to be loaded must disable block 1 from simulating RT 3. This is done by loading an 8 into memory location 1823 (hex), as follows (reference paragraph 2.11.5.5.):



Similarly, to enable message block #1 to simulate R.T. #7 transmitting, 0 (1-1) must be stored in Trigger RAM location 1827 (hex) as follows:



Next, it is necessary to program the first two message RAM blocks for the control words and (preloaded) Command words, as well as for the Status and Data words to be transmitted.

The control word parameters for message blocks 1 and 2 are as follows:

Data Word Count = 1 = 0000 0001 (binary)

Format = 10 (hex) (per Table 2-9)
= 0001 0000 (binary)

For RT mode, the upper 5 bits of the third control byte specify response time; the lower 3 bits of the third byte are not used (default to 0). Assigning an RT response time of 10 us, the value of byte 3 should be:

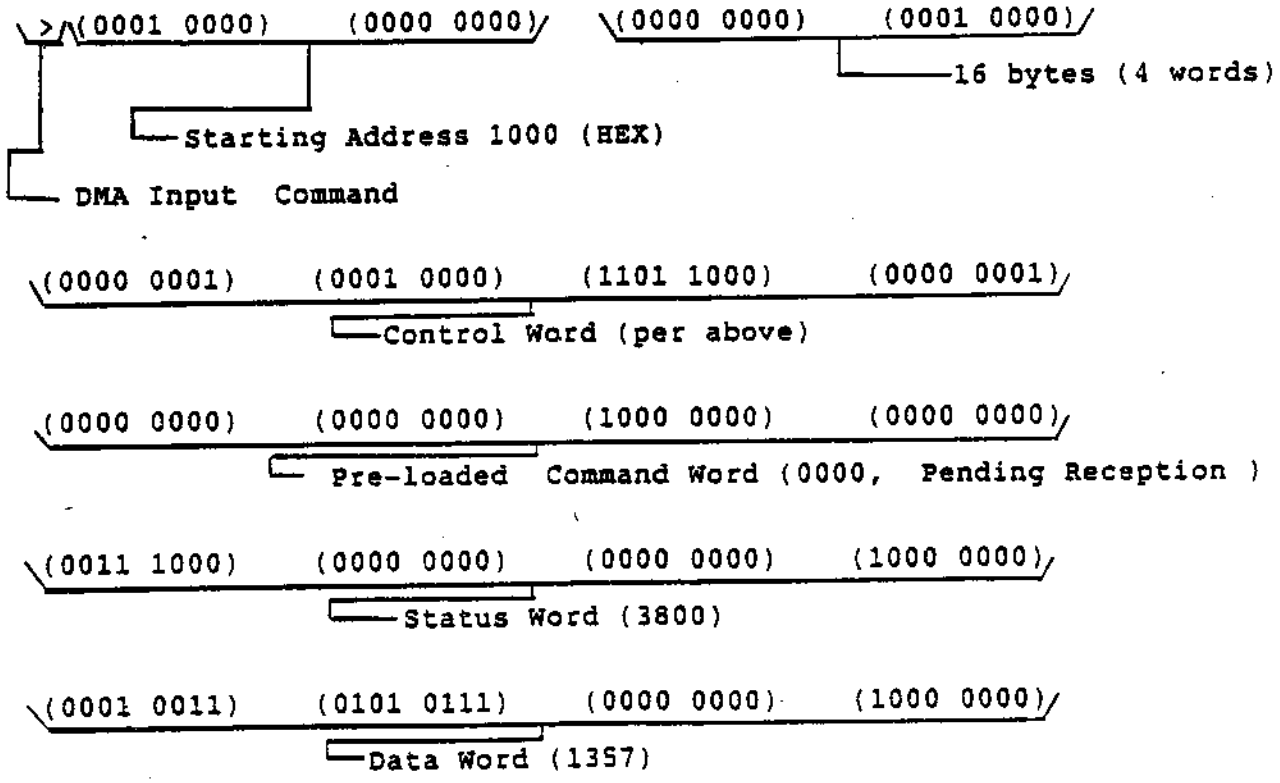
8 * (37 - 10) = 216 = 1101 1000 (binary)

The fourth control byte for RT mode is used to store the "linked to block" parameter in the lower 4 bits; the upper 4 bits are not used and default to 0.

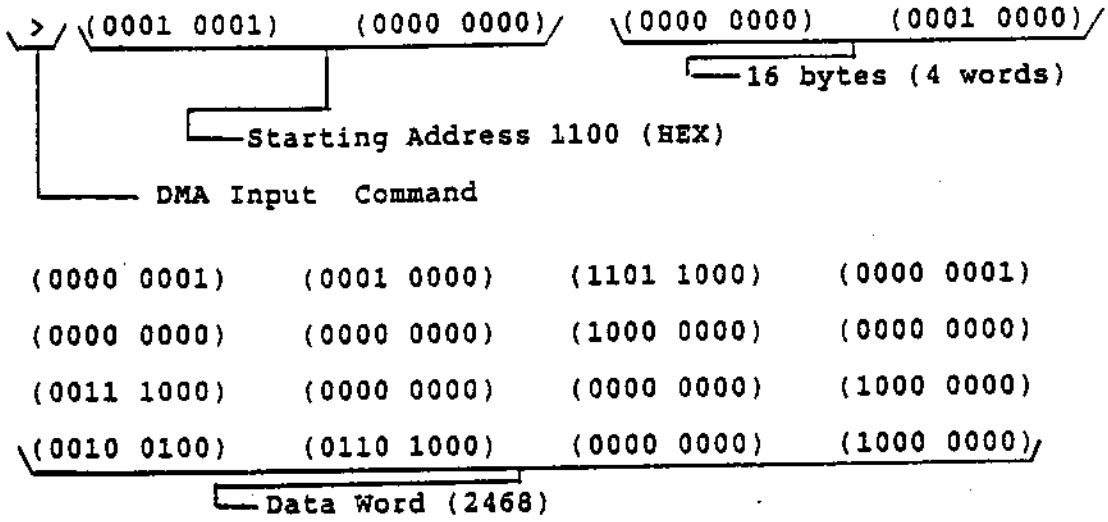
In order to link block 1 to block 2 (so that the Exerciser will respond with the data from block 2 the **second** time RT 7 is addressed to transmit), it is necessary to specify a value of 1 (2-1) as the fourth byte of block 1's control word.

Since the Exerciser will be programmed to switch off-line after it has processed the message for block 2 (second message), the fourth control byte for block 2 may be arbitrarily assigned. By loading a 1 to this location, RT 2 will link to itself. If the instrument was programmed using keyboard or low-speed I/O commands, this would be the effective result.

The DMA Input command to load data to message block 1 is:



Likewise, for block 2,



Now that the message and RT trigger RAMs are loaded, the Exerciser may be put on-line to process the two-message sequence. Using the DMA commands, this is done as follows:

By referring to Table 2-23, it is seen that two DMA Input commands are required to enable the Exerciser for "Single Frame" RT mode.

The first step is to load D0 (hex) to the Mode Set-Up Register, address 3802 (hex), as follows:

(0011 1000) (0000 0010) (0000 0000) (0000 0001) (1101 0000)

The second step is to load one less than the desired number of messages to be processed, 1 (2-1) to the message count register, address 1C00 (hex), as follows:

(0001 1100) (0000 0000) (0000 0000) (0000 0001) (0000 0001)
(UNL (with ATN))

This puts the Exerciser's 1553 processor "on-line." It will now respond to the first two messages (commands) directed to RT 7 to transmit, and then go "off-line."

To use the DMA mechanism to determine if the Exerciser has completed the programmed 2-message sequence, the MODE SET-UP register may be polled as follows:

(MLA (with ATN)) (0011 1000) (0000 0010) (0000 0000) (0000 0001)
(UNL (with ATN)) (MTA(with ATN))

The Exerciser will reply with:

(11(FE)1 0000) (LF with EOI),

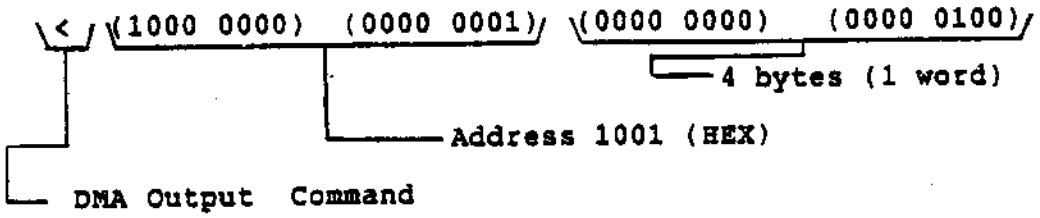
where FE indicates the read only binary value of the FRAME ENABLE output bit FRAME ENABLE will remain high until such time that the Exerciser has processed the programmed 2-message sequence.

The GPIB controller must continually poll FRAME ENABLE, as illustrated above until it reads a 0, indicating that the 2-message sequence has been completed.

When frame enable does return a 0 (or, if it doesn't in a suitable amount of time), the Exerciser should be taken off-line by loading 90 (hex) to the MODE SET-UP REGISTER, as follows:

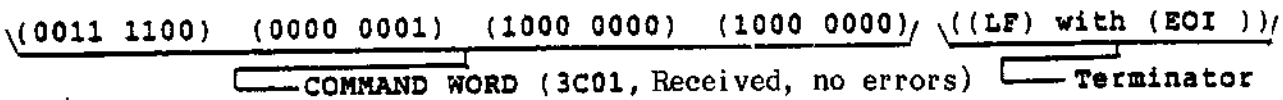
(UNT (with ATN)) (MLA (with ATN)) > (0011 1000) (0000 0010)
(0000 0000) (0000 0001) (1001 0000)

The received command word for block 1 may be verified by sending a DMA Output command as follows:



(UNL(with ATN)) (MTA (with ATN))

The Exerciser reply should be:



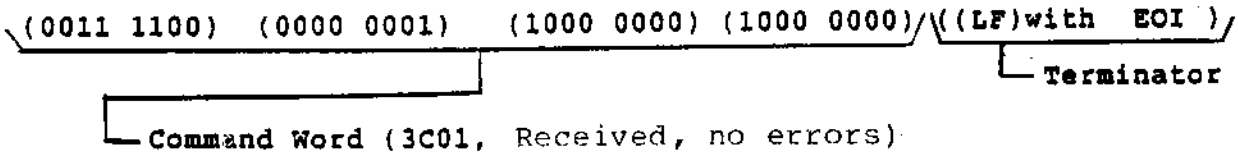
Similarly, the received command word for block 2 may be verified:

(UNT (with ATN)) (MLA (with ATN))

(1000 1000) (0000 0001) (0000 0000) (0000 0100)

(UNT (with ATN)) (MTA (with ATN))

Similar to block 1, the reply string should be:



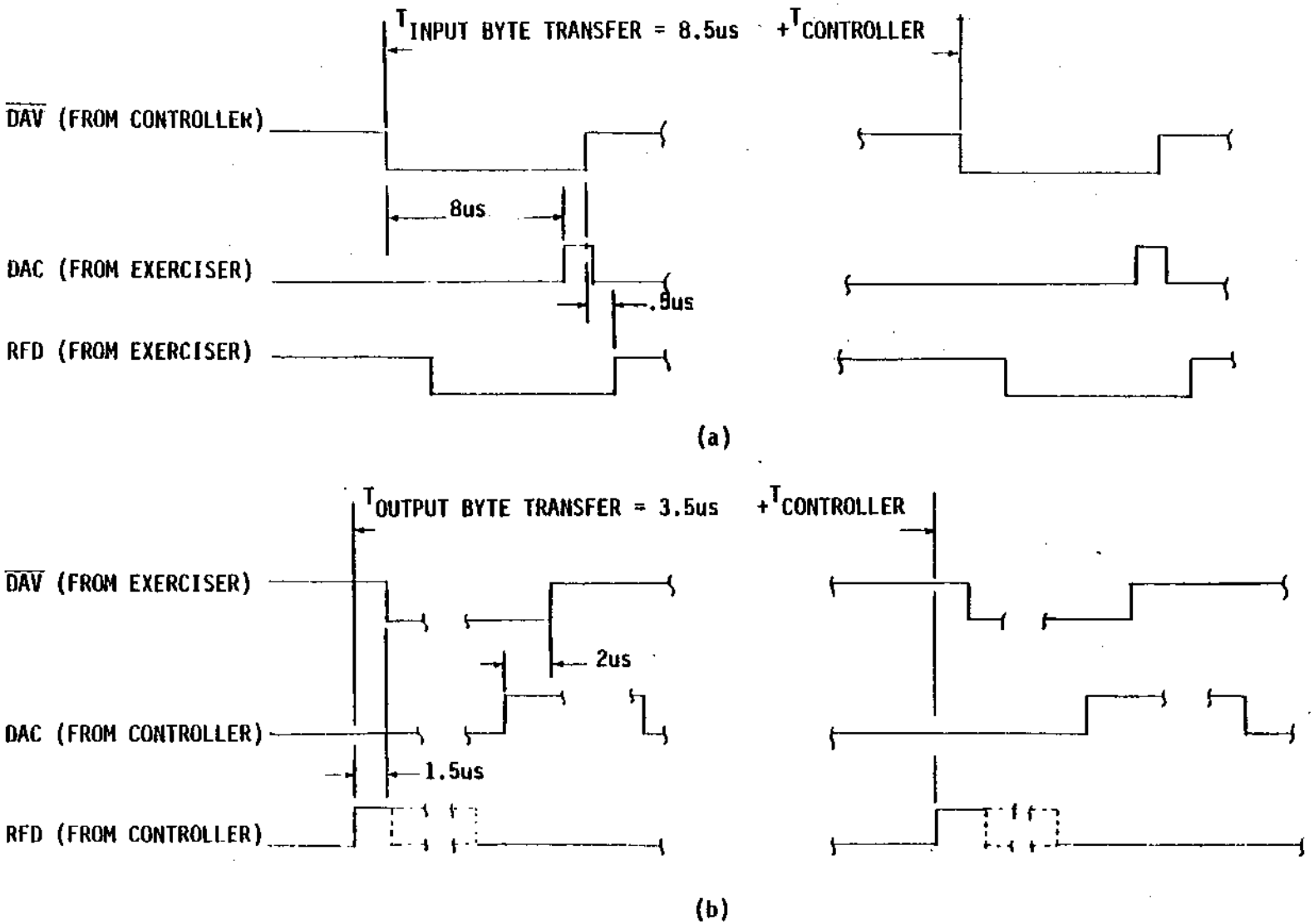


Figure 2-27. GPIB Handshake Timing for DMA Transfers

(a) EXERCISER IS LISTENER (DMA INPUT); (b) EXERCISER AS TALKER (DMA OUTPUT). TYPICAL TIMING VALUES ARE INDICATED

SECTION 3

PRINCIPLES OF OPERATION

3.1 INTRODUCTION

This section describes operation of the Exerciser in terms of block and simplified diagrams (Figures 3-1 through 3-13) and the interconnection and schematic diagrams of Section 4. With the exception of the proprietary portion of the top PCB assembly, sufficient information is provided to support equipment maintenance down to the component level.

3.2 OVERALL DESCRIPTION (Reference Block Diagram Figure 4-2)

Referring to the block diagram, the Exerciser is comprised of five main sections. These are:

1) The microcomputer section, including the microprocessor, RAM and ROM memory, and address decoding.
2) The keyboard and display is the manual section and the 8-bit tri-state parallel I/O, IEEE-488 and RS-232 interfaces is the remote interface section.
3) The 1553 message and trigger RAMs and associated buffering, timing, and sequence control circuitry. This manual contains no schematic diagram or detailed technical information pertaining to this section, since it is considered proprietary by DDC.
4) The 1553 front end section. This is comprised of an error-generating encoder and error-detecting decoder, a variable-level transceiver, and two bus pulse transformers.
5) The internal power supply, which delivers +5V, +24V, +15V, and -15V to the rest of the instrument.

Essentially, data flow through the instrument takes the following path: with the exception of the high speed remote I/O commands (discussed in paragraph 2.11.4), commands and data which are input via either the keyboard or one of the remote I/O ports are queued in the microcomputer scratchpad RAM. When the microprocessor is not servicing one of the I/O ports, it parses the command string and executes the individual commands. One of the important tasks performed by the processor is to translate the data from ASCII hex, as it appears on the I/O ports, to binary, as it is stored in the message RAM. Some of the other functions of the microprocessor include the loading of data to the RT trigger RAM to enable the Exerciser to recognize its own RT address(es), as well as the loading of various registers in the 1553 processor associated with mode selection, message count, frame time, and run/halt control.

The message RAM is a 16K-bit memory that is dual-ported to enable access from both the microprocessor as well as the -1553 encoder and decoder. It is configured with an 8-bit port to the microprocessor and 16-bit port on the 1553 side. Data

transfers between this memory and the encoder/decoder buffers take place in sets of two 16-bit transfer cycles.

The 1556 error-generating encoder converts 16-bit parallel data (plus error and control inputs) to bi-phase TTL Manchester II encoded serial data. The serial output will either be valid or will include induced encoding errors, depending on the programming of the various error lines.

Similarly, the 1555 bus error-detecting decoder converts bi-phase TTL Manchester II serial data to a 16-bit parallel output. Additional output lines indicate sync type, error conditions, and bus activity.

The 8559 transceiver contains waveshaping and power amplifier circuitry to drive the 1553 bus to the required voltage amplitude. This amplitude may be varied according to the level of the DC voltage delivered to the transceiver from a power amplifier, as determined by the setting of the front panel potentiometer. Two pulse transformers interface between the transceiver and the channel A and channel B buses to provide the appropriate voltages and impedances for either direct or transformer coupling.

The proprietary portion of the top board includes timers for generating response, intermessage gap, and frame times, as well as for monitoring of response and transmitter time-out conditions. In addition, the top board includes the sequence control and strobe generation logic necessary to format 1553 messages and to control data transfers between the message RAM and the encoder/decoder buffers.

All instrument timing is derived from the 16 MHz clock generated in the decoder module. This clock is divided down into 8, 4, and 2 MHz clocks which are used for various functions within the Exerciser.

3.3 MICROCOMPUTER CIRCUITS: MICROPROCESSOR/CLOCK/RAM/ROM/ADDRESS DECODING (Reference Block Diagram 3-1 and Bottom Board Schematic Figure 4-4)

The output of differential line receiver U50 provides the 4 MHz clock input to microprocessor U55 (Motorola 6809). The 4 MHz input to U50 comes from the top board.

Output pin 18 of buffer U57 provides a $\overline{\text{RESET}}$ pulse at power turn-on to the microprocessor, as well as to ACIA U15, PIAs U16 and U40, and GPIA U2 (bottom board), and to encoder U50, decoder U55, and timer U29 (top board).

Following the power-up $\overline{\text{RESET}}$ pulse to U55-37, the microprocessor begins running its program. Instructions are fetched from 8K x 8 EPROMs U22, U23, and U24. The microprocessor executes its instructions by reading and writing data to the 2K x 8 scratchpad RAM, comprised of U31, U32, U34, and U35 (individual 1K x 4 RAMs), and to various I/O ports and the 1553 message RAM on the top board.

Address decoder U41 is used to select the memory or I/O device currently reading or writing data. The timing diagram of Figure 3-2 illustrates the timing relationship of the microprocessor quadrature clocks Q and E and the memory and I/O chip select strobes.

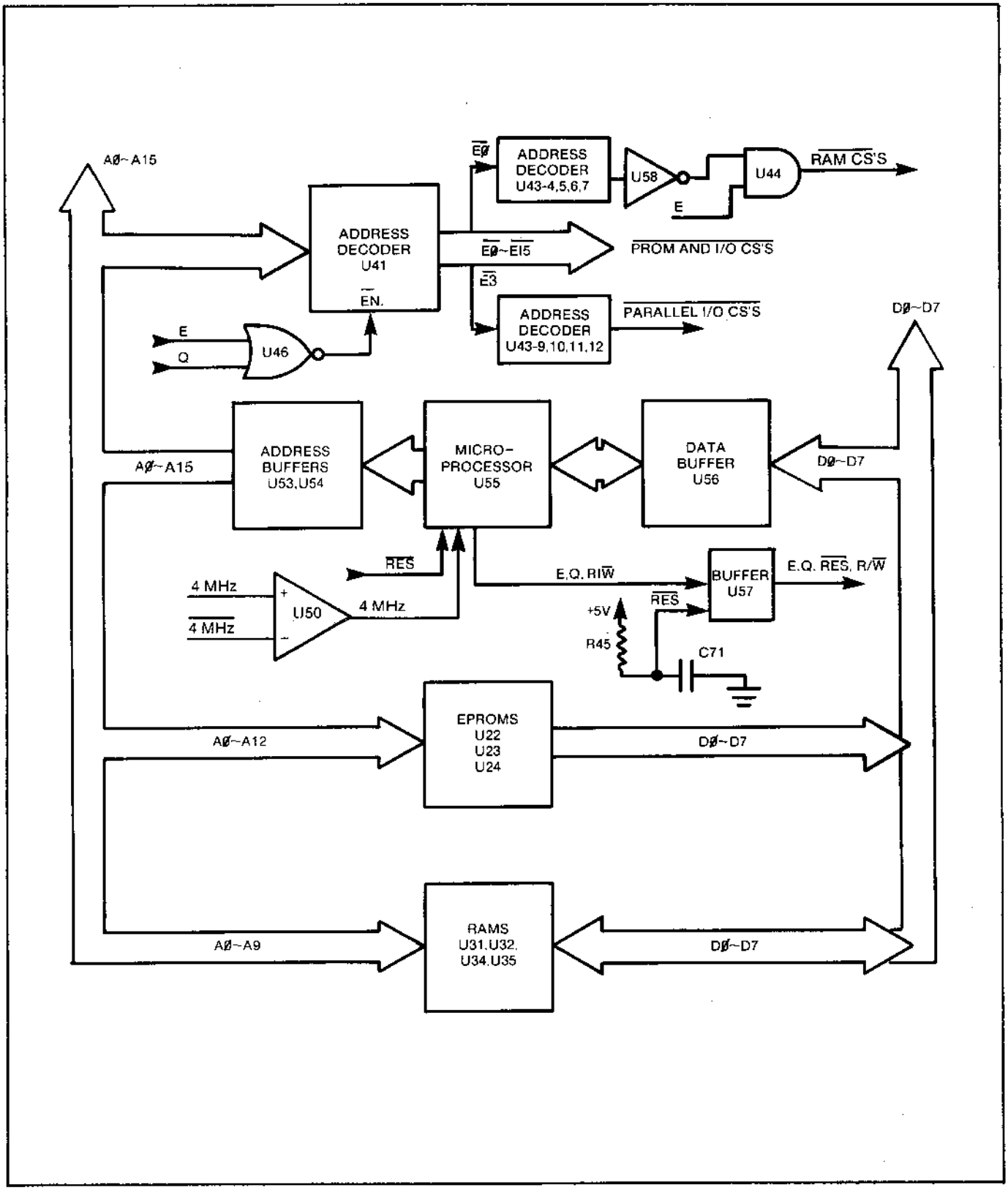


Figure 3-1. Microcomputer Circuits Block Diagram

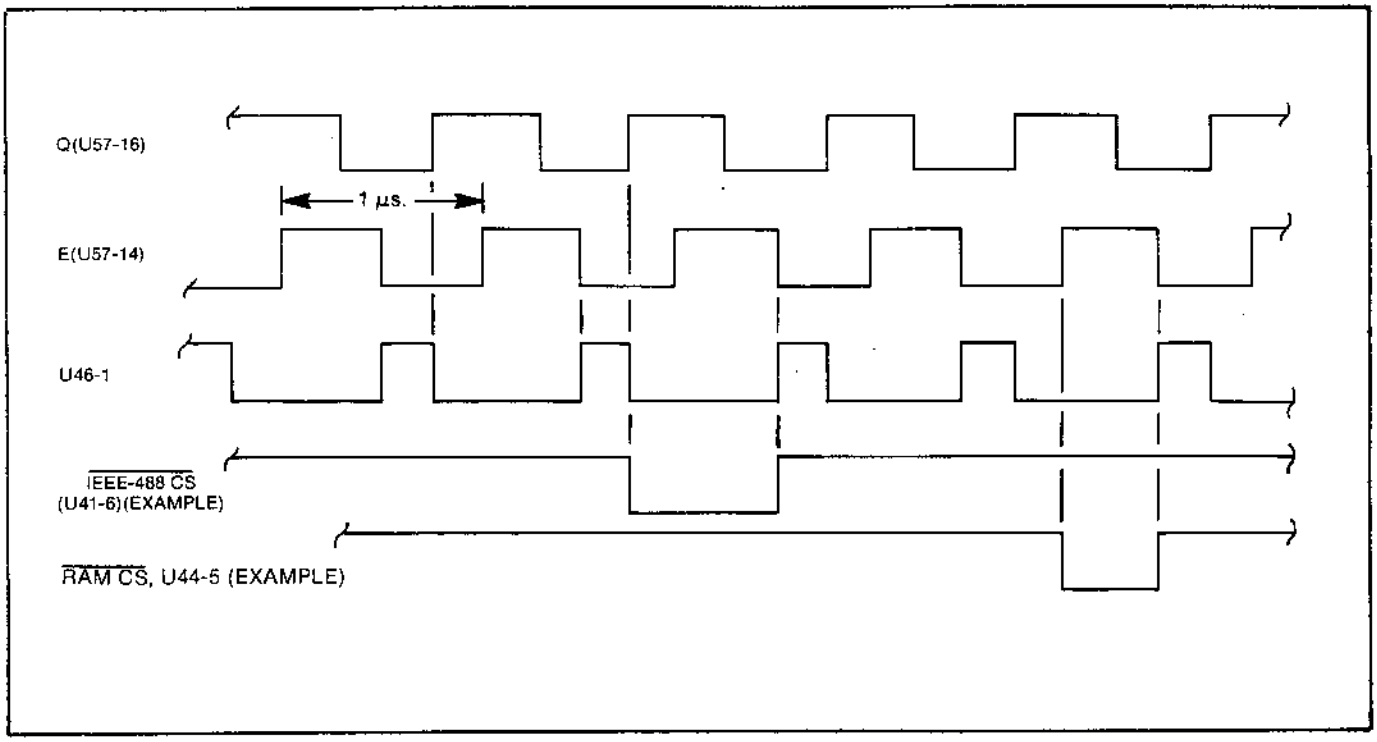


Figure 3-2. Sample Chip-Select Timing

In the timing diagram, the 1 MHz clock Q leads clock E by 90 degrees. The signal at U46-1 enables the address decoder with 750 ns negative pulses. The address decoder outputs are derived from these pulses in order to access RAM, ROM, keyboard, display, and the three remote interfaces. Note that the pulse width of the RAM chip select lines is 500 ns, as compared to 750 ns for the other devices. This is due to the fact that the $\overline{\text{RAM CS}}$ signals are gated by the E clock (via gates of U58, U44) to prevent erroneous memory WRITE cycles following the falling edge of E.

There is buffering on all the microprocessor signals, allowing them to drive all the devices on the bottom board, as well as to the message and trigger RAMs (and other devices) on the top board. Data lines D0 through D7 are buffered by transceiver U56, with READ/WRITE providing the direction control to U56. Address lines A0 ~ A15 are buffered by drivers U53 and U54. Clock and control signals Q, E, R/W, and RESET are buffered by driver U57.

There are three interrupt pins on U55: $\overline{\text{NMI}}$ (Pin 2), $\overline{\text{IRQ}}$ (Pin 3) and $\overline{\text{FIRQ}}$ (Pin 4). Non-maskable interrupt $\overline{\text{NMI}}$ is not used. Interrupt request IRQ may be asserted low by either a request from the 8-bit tri-state parallel I/O port (U26-4), the IEEE-488 interface (U2-40), or the timer (U29-9 on the top board) that is used to time frame time and transmitter time-out intervals. Fast interrupt request $\overline{\text{FIRQ}}$ may be driven low by either the keyboard interface circuitry (U26-2) or the RS-232 interface (U15-7). When any of these interrupts occurs, the microprocessor program is diverted to one of its interrupt service routines, where it determines the source of the interrupt, clears the appropriate interrupt request line, and takes appropriate action, as required.

3.4 INTERFACE CIRCUITS

3.4.1 KEYBOARD INTERFACE (Reference Block Diagram Figure 3-3 and Timing Diagram Figure 3-4)

As shown in the block diagram, the keyboards and a portion of their interface circuitry are located on the display board. The remainder of the interface circuitry is located on the bottom board.

The manual interface to the Exerciser is comprised of keyboards KB1 and KB2, as well as RUN and HALT switches S3 and S4. The closure of any of the 24 individual keys results in the assertion of an active low on one of the individual output lines from KB1 and KB2. The combined logic of priority encoders U1, U2, and U3 and AND gates U5 and U6 presents a unique 5-bit code at U4-14, 17, 18, 8, 13 for each of the 23 keys (the CNTL key is not decoded). A logic low at pins 3, 4 or 7 of U4 indicates a closure of the RUN (S3), HALT (S4), or CNTL (KB1-10) keys, respectively (display board).

When any keyboard switch other than CNTL (without another key) is pressed, the KEY DEPRESSED output (U13-15) of the cascaded priority encoders is asserted high, forcing U39-11 high. When either RUN pushbutton (S3) or HALT push button (S4) is pressed, U44-8 and U39-11 will go high.

At this time, the keyboard de-bounce/data input timing sequence proceeds as follows (refer to Figure 3-4):

1) The first rising edge (there are generally multiple edges due to switch closure bounce) from U44-8 is gated and delayed by U39-11, C61, and U45-11 to U47-9 and U47-2. The incidence of the rising edge at U47-2 results in a 250 ms (approximate) positive pulse at single-shot output U47-13 (bottom board).
2) This 250 ms pulse clears flip-flop U43-9, 8, dropping the interrupt line FIRQ (U26-2) low and asserting KEYBOARD STATUS (U43-8) high.
3) Note that as a result of the first falling edge of U13-15 (due to key bounce), there is a 370 ms (approximate) negative pulse initiated at U47-12. By means of U45-12, 13, 11, this precludes any additional positive pulses at U47-13.
   It may be noted that the rising edge of the KEYBOARD LATCH signal (U47-13) is routed to block pin 11 of latch U44 on the display board. This edge, which occurs about 100 ns after the first rising edge of KEY DEPRESSED, due to the action of C61, latches the encoded data, identifying the depressed key(s). The 100 ns compensates for delays through the encoding circuitry, insuring sufficient setup time for U4.
4) In response to the interrupt, the microprocessor performs a polling sequence in its FIRQ service routine to determine the cause of the interrupt. To determine if the keyboard is the cause of the interrupt, it reads the KEYBOARD STATUS line by strobing U20-1, 19 with a 750 ns negative pulse. A high for KEYBOARD STATUS will then appear on the D7 data line.
5) The processor reads the data from keyboard latch U4 (display board) by routing a 750 ns KEYBOARD CS pulse to U4-1 (display board) and U43-4 (bottom board). This pulse has the effect of presetting flip-flop U43, disasserting FIRQ (U26-2) high, and dropping KEYBOARD STATUS (U20-17) low.

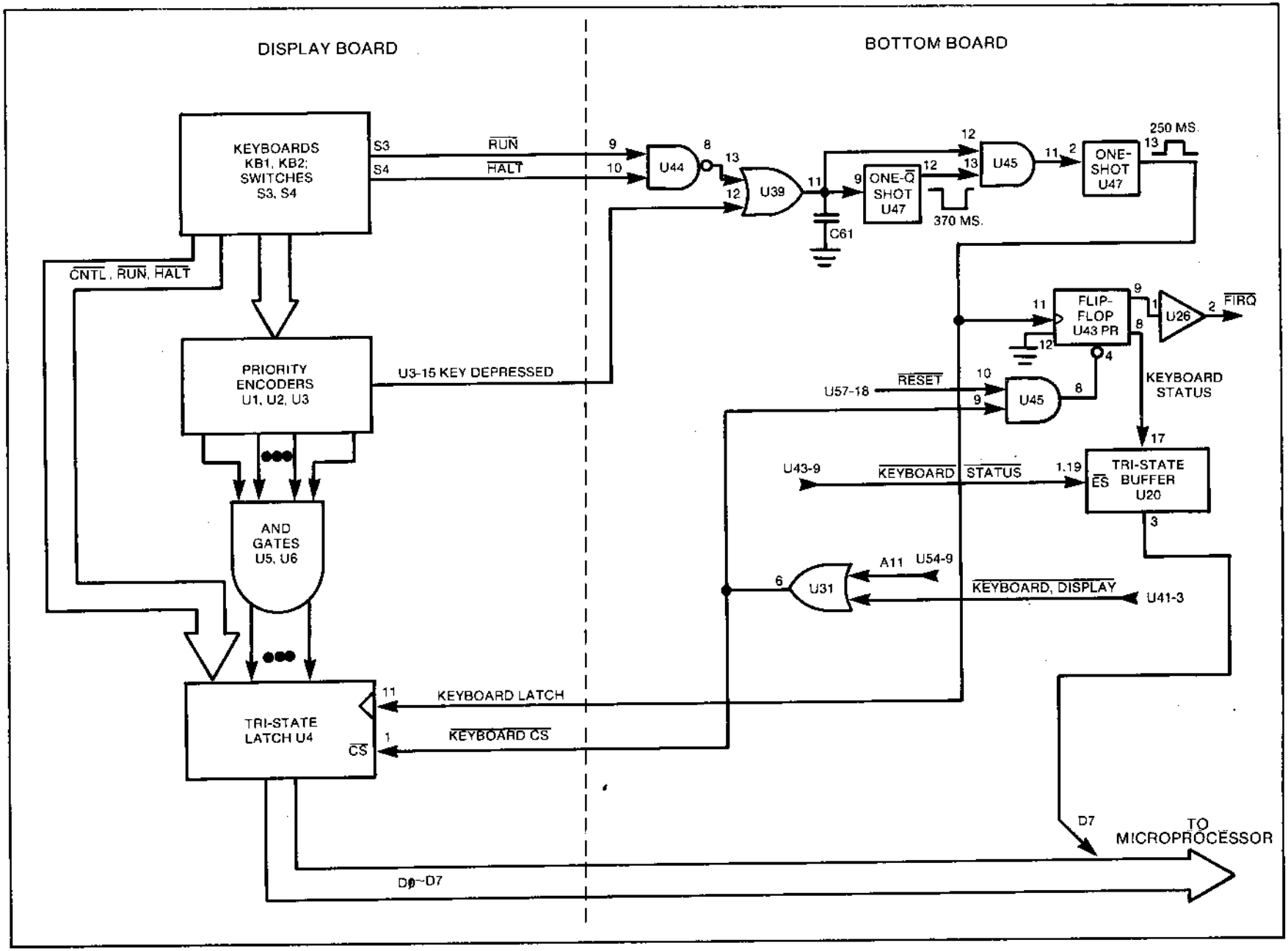


Figure 3-3. Keyboard Interface Circuit Block Diagram

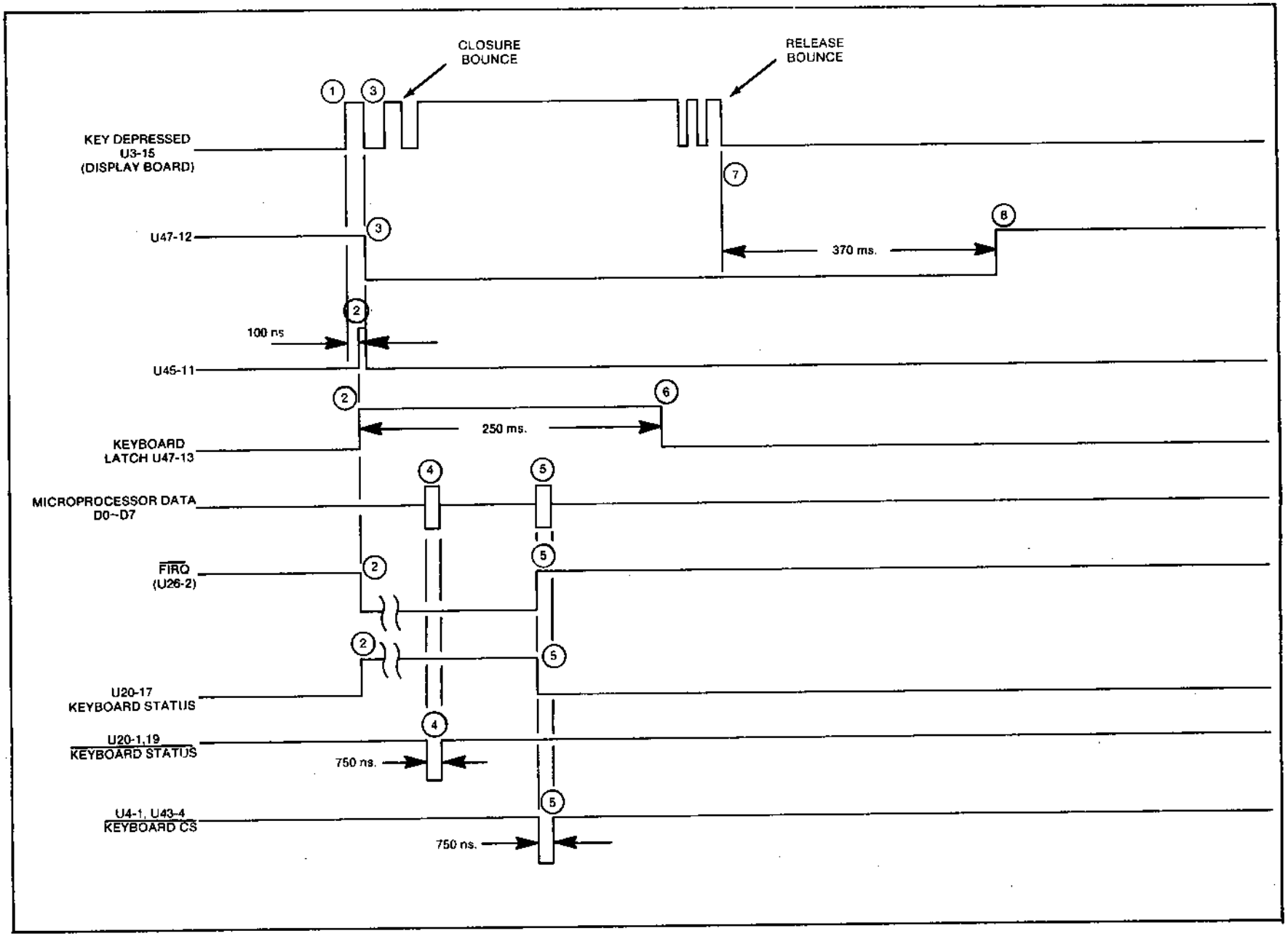


Figure 3-4. Timing Sequence for Keyboard Data Entry

6) Single shot output U47-13 drops after 250 ms.
7) When the key is released, the falling edges of KEY DEPRESSED (U3-15) cause retriggerable one-shot U47-12 to remain low for approximately 370 ms after the last release bounce. By means of AND gate U45-11, this eliminates the possibility of undesired additional pulses at U47-13 after key release.
8) After about 370 ms, U47-12 returns to high, enabling the de-bounce data input circuitry to respond to the next key closure.

3.4.2 DISPLAY CIRCUITS (Reference Block Diagram Figure 3-5 and Timing Diagram Figure 3-6)

The Exerciser front panel display is comprised of ten (10) 7-segment LED displays DS1 through DS10, and individual indicator LEDs DS11 through DS22 (display board). DS1 through DS15, and DS22 are driven by segment drivers U9, U10, and U11 under microprocessor control by means of PIA U40 (bottom board). LEDs DS17 (ON-LINE) and DS21 (XMITR/OUT) are also under microprocessor control, via PIA U16 and buffer U29 (bottom board) and NOR drivers U7 and U8 (display board). During normal Exerciser operation, real time LEDs DS18 (LINE ACTIVE), DS19 (BUS FAULT), and DS20 (REPLY T/OUT) are controlled by the proprietary portion of the top board circuitry. These three indicators may also be lamp tested under microprocessor control (via PIA U40-19 and U27-2, bottom board) by means of NOR drivers U7 and U8.

Display segment drivers U9, U10, and U11 may be configured to illuminate any possible combination of segments, thus providing for full numeric and partial alpha capability for the 10-character display comprised of DS1 through DS10.

Display data is communicated from PIA U40 (bottom board) to drivers U9, U10, U11 (display board) by means of the timing sequence illustrated in Figure 3-6. The data is transmitted from PIA U40-9 in serial NRZ format to U9-22, U10-22, U11-22. The data is shifted into the input registers in the individual drivers on the rising edge of the respective DISPLAY CLOCK (U40-17, etc.) when the DATA ENABLE signal (U40-13, etc.) to the respective driver is held low. The timing sequence is as follows:

1) The first clock pulse (labeled 1 on the timing diagram) after the respective DISPLAY ENABLE goes low does not contain any display data, but rather is used to initialize the driver circuitry. It is always a logic 1.
2) The next thirty-four (34) data pulses, 2 through 35, contain the actual display data. On the rising edge of the thirty-fifth pulse, the driver input shift register becomes full. At this time, the driver will update its output circuitry, causing the respective displays to change. The microprocessor will then proceed to provide fresh data to the next driver. Potentiometers R1, R2, and R3 are used to adjust the display intensity. They are factory-adjusted to provide a 13.3 ma drive current for each of the segments of DS1 through DS10. This corresponds to a voltage drop of 2.0V across TP1 to TP2 (RA18-8 to 7); TP3 to TP4 (RA21-8 to 7); and TP5 to TP6 (RA23-7 to 8).

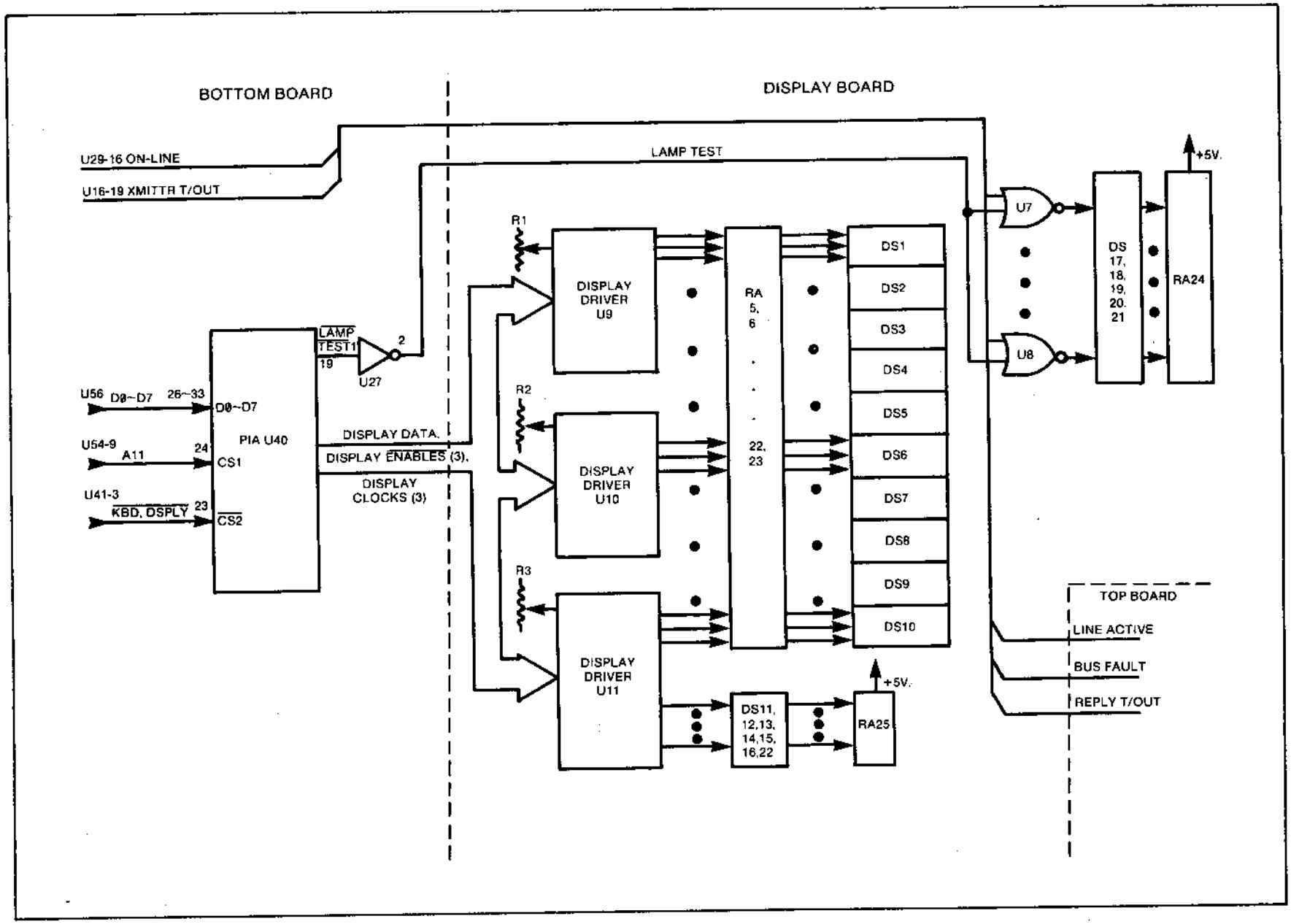


Figure 3-5. Display Circuits Block Diagram

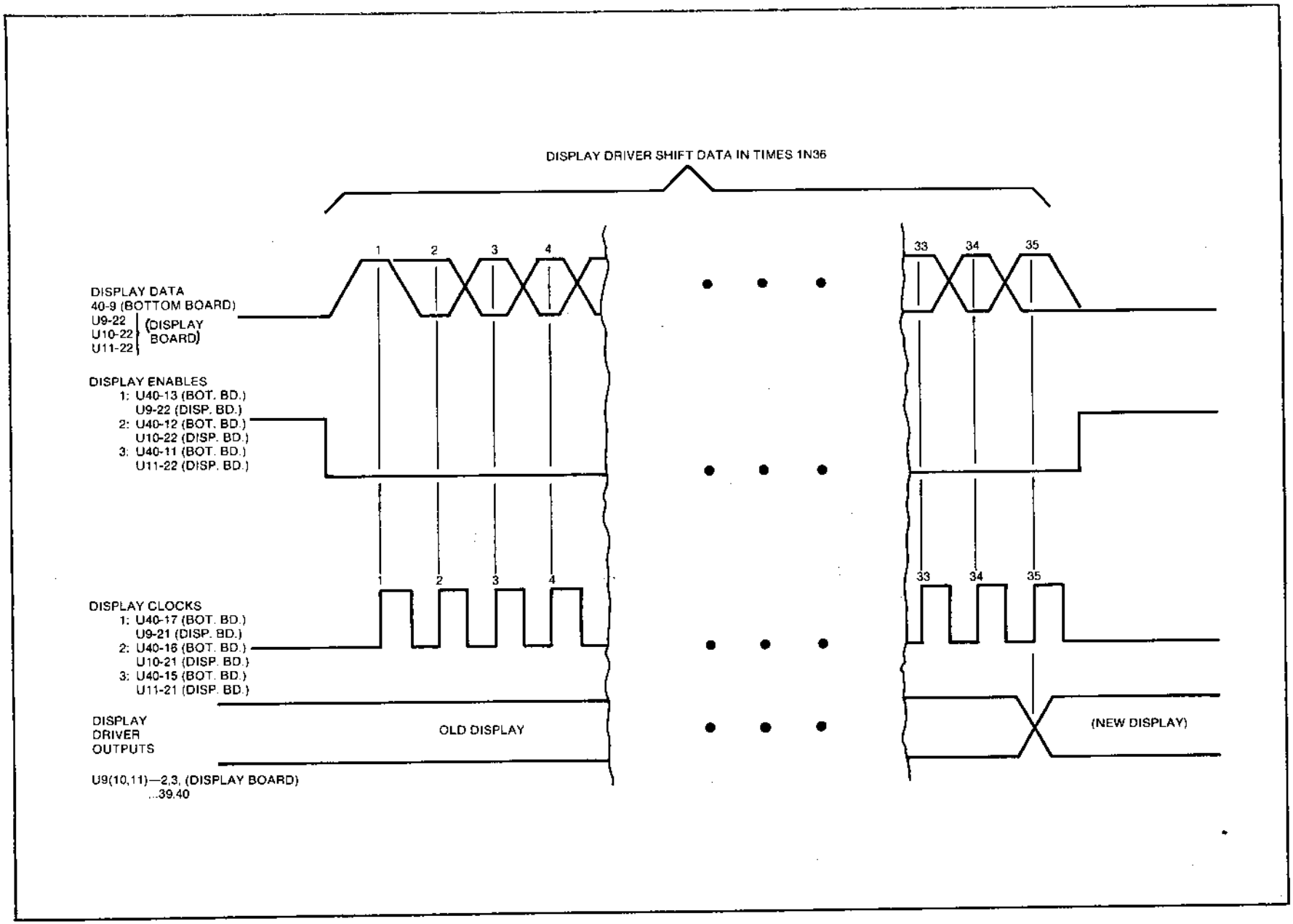


Figure 3-6. Timing Diagram for Display Drivers U9, U10, U11 (Display Board)

3.4.3 PARALLEL INTERFACE CIRCUITRY (Reference Block Diagram 3-7 and Timing Diagram 3-8 and 3-9)

All of the circuitry for the parallel interface is located on the bottom board. The parallel interface circuitry performs three functions:

1) Allows a host computer to write 8-bit ASCII and binary commands and data to the Exerciser.
2) Allows the host computer to read ASCII and binary data from the Exerciser.
3) Provides a service request output to alert the host of a change in instrument status (error, sequence complete, etc.).

The interface is comprised of bus transceivers U5 and U12; input latch U17; output PIA U16; open collector buffer U26; address decoder U43; tri-state buffer U28; flip-flops U36, U38, U25, U36; and various gates of U27, U37, U39, U49, U45, and U46.

Operation of the 8-bit tri-state parallel interface is best explained by the following descriptions of the READ and WRITE timing sequences.

The READ sequence takes place as follows: (Refer to Figure 3-7.)

1) To read a character from the Exerciser 8-bit tri-state parallel port, the controlling device must assert the $\overline{\text{READ}}$ line low (J2-9, U27-11). This results in the PARALLEL I/O line (U38-6 to tri-state buffer U28-2) and READ line (U27-10 to U28-4) going high. At the same time, interrupt line IRQ (U26-4) will assert low as a result of flip-flop U38-5 being cleared by the rising edge from U39-3, gated via U49-1, 2, 3. In addition, the rising edge of READ (U27-10) has the effect of setting flip-flop output U38-8, clearing (bringing high) the SERVICE REQUEST output (U26-8, J2-12).
2) As a result of the $\overline{\text{IRQ}}$, the microprocessor polls the status of the parallel I/O port by routing a 750 ns negative chip select pulse from U43-12 to U28-1, 19. After the processor verifies three of the status bit positions, it proceeds with the parallel READ transfer. The three conditions are:

   (i) Parallel I/O bit (U28-2...D7) high
   (ii) Parallel I/O read bit (U28-6...D5) high
   (iii) 8-bit tri-state parallel I/O port active (S8-1, U28-17...D0) low

3) The microprocessor writes the output data to PIA U16 by means of a chip select strobe from U43-10 to U16-23.
4) The PIA internal strobe to write data to the channel A data register is reconstructed by various gates of U49, U46, U37, U27 to derive $\overline{\text{PIA-A-WRITE}}$ U27-12. This pulse sets flip-flop output U36-5 DRIVER ENABLE, enabling transceivers U5 and U12 to drive the external parallel bus T0 ~ T7.
5) The rising edge at the end of the $\overline{\text{PIA-A-WRITE}}$ pulse clears flip-flop output U36-9 and sets output U36-8. This edge is synchronous with the falling edge of the E clock.
6) The output data on T0 ~ T7 becomes valid 1.04 us (maximum) after the rising edge of $\overline{\text{PIA-A-WRITE}}$.

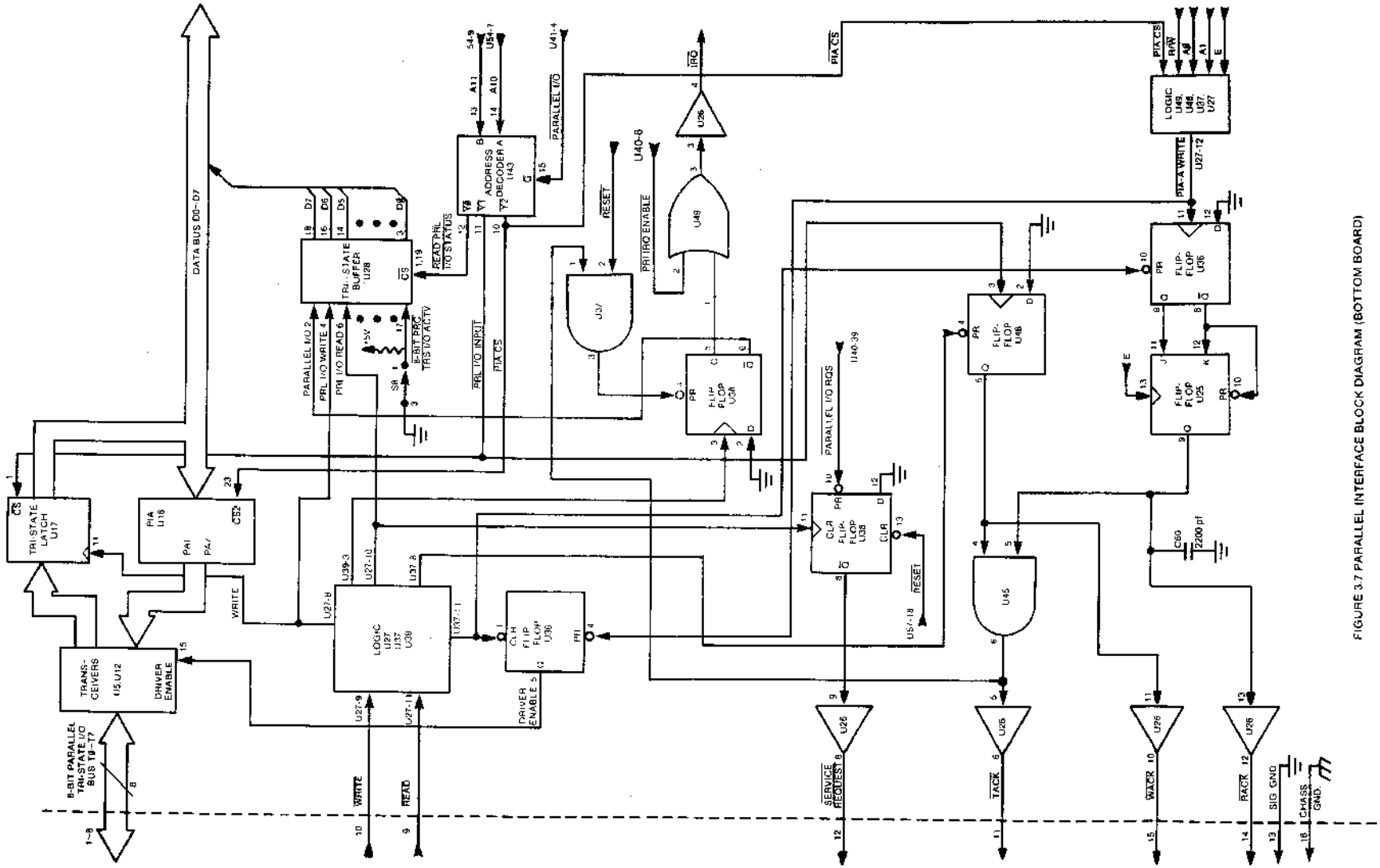


FIGURE 3.7 PARALLEL INTERFACE BLOCK DIAGRAM (BOTTOM BOARD)

Figure 3-7. Parallel Interface Block Diagram (Bottom Board)

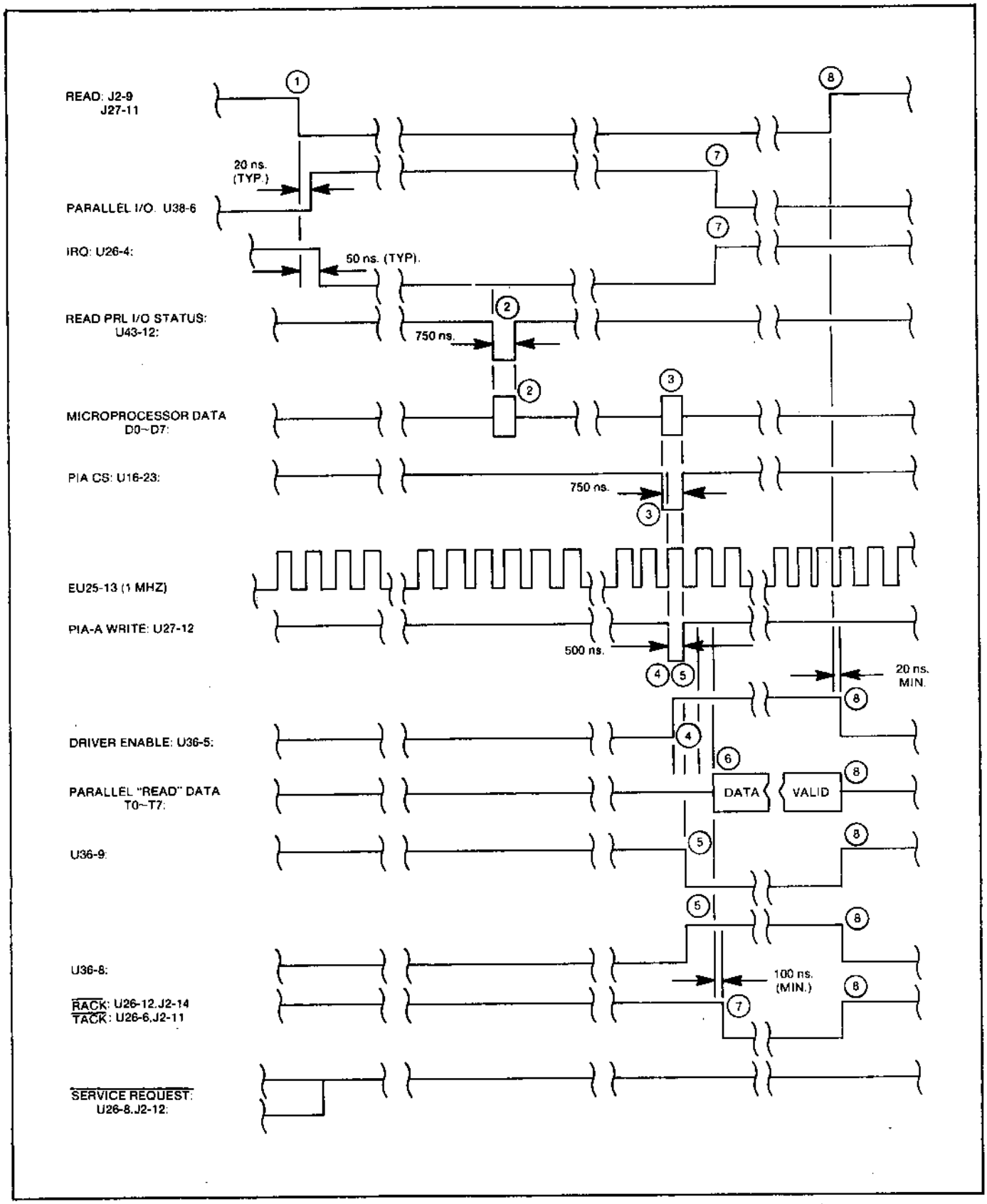


Figure 3-8. Parallel Interface Read Timing Diagram

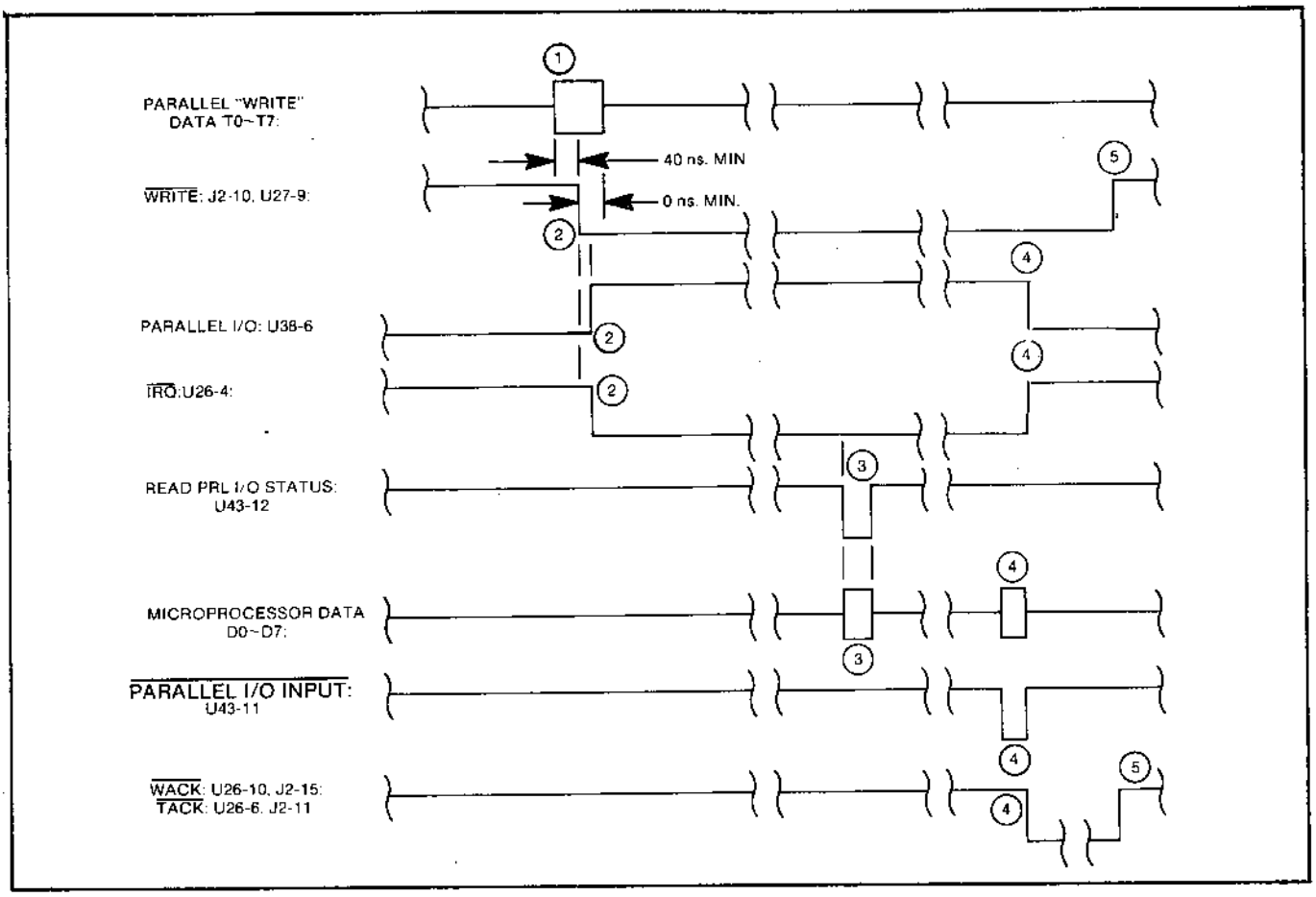


Figure 3-9. Parallel Interface Write Timing Diagram

7) The next falling edge of E after PIA-A-WRITE has the effect of clearing flip-flop output U25-9. Capacitor C60 provides a 200 ns (approximate) delay to insure T0 ~ T7 is settled before open-collector handshake outputs TACK (J2-11, U26-6) and RACK (J2-14, U23-12) are asserted low. The handshake outputs inform the host computer that the output data on T0 ~ T7 is valid. The unbuffered TACK signal (U45-6) also has the effect of presetting flip-flop U38-5, 6, clearing IRQ high and PARALLEL I/O low.
8) The READ sequence terminates when the host device dis-asserts the READ line by bringing it high. This has the following effects:

   (i) READ is brought low.
   (ii) DRIVER ENABLE is brought low, disabling the transmitters in U5 and U12, putting the T0~T7 bus in its high impedance state.
   (iii) Flip-flop outputs U36-9 and U25-9 are set, negating (bringing high) handshake outputs TACK and RACK.

The WRITE sequence takes place as follows (refer to Figure 3-9):

1) The host device initiates the WRITE sequence by presenting valid parallel input data on T0~T7.
2) After providing a minimum set-up time of 40 ns for T0 ~ T7, the host causes the input data to be latched into buffer U17 by asserting WRITE low. Asserting WRITE also has the effect of bringing PARALLEL I/O (U38-6)

and WRITE (U27-8) high and asserting IRQ (U26-4) low (via U49-3) by clearing flip-flop U38-5.

3) The microprocessor determines the status of the parallel interface by strobing U28-1, 19 low. In order to proceed with the data input sequence, the processor must verify:

   (i) Parallel I/O (U28-2...D7) is high
   (ii) Parallel I/O write (U28-4...D6) is high
   (iii) 8-bit tri-state parallel I/O active (S8-1, U28-17...D0) is low.

4) The microprocessor reads the input data by routing a 750 ns chip select pulse to U17-1. The rising edge of this pulse clears flip-flop U48-5, causing open-collector handshake outputs TACK and WACK (J2-15, U26-10) to assert low. This informs the host that the Exerciser has accepted the input character. At this time, the signal from U45-6 presets flip-flop U38-5, 6, clearing IRQ high and PARALLEL I/O low.

5) The Write sequence terminates when the user brings $\overline{\text{WRITE}}$ high. This brings WRITE low and clears WACK and $\overline{\text{TACK}}$ by presetting flip-flop U48-5 to bring them high.

The $\overline{\text{SERVICE REQUEST}}$ Output (J2-12, U26-8) is asserted low by clearing flip-flop output U28 with a software-derived pulse from PIA U40-39 to U38-10 following a change in instrument status (Error, Sequence Complete, etc.). $\overline{\text{SERVICE REQUEST}}$ becomes negated (high) when a character is read from the port by setting flip-flop output U38-8 by the rising edge of $\overline{\text{READ}}$ (U37-11 to U38-11).

3.4.4 IEEE-488 (GPIB) INTERFACE CIRCUITRY (Bottom Board: Reference Block Diagram Figure 3-10)

The IEEE-488 (GPIB) interface consists of four bus transceivers U1, U3, U9, U10; general purpose interface adapter (GPIA) U2; tri-state buffer U4; address switch S9; and half of hex inverter U27. Transceiver U1, U3, U9, and U10 serve as the interface between the IEEE-488 (GPIB) parallel bus and the bus protocol controller U2. Transceivers U10 and U3 are used for bus management and handshake signals; U9 and U1 accommodate the eight data lines. Logic levels applied to the four transmit/receive inputs of each quad transceiver from controller U2 determine the direction of data flow for each associated bus line. The T/R bit for $\overline{\text{SRQ}}$ (Service Request) is hardwired high (always transmit), while those for $\overline{\text{REN}}$ (Remote Enable), IFC (Interface Clear) and $\overline{\text{ATN}}$ (Attention) are hardwired low (always receive). The T/R lines for the remaining control and handshake signals $\overline{\text{EOI}}$ (End or Identify), DAC (Not Data Accepted), RFD (Not Ready For Data) and $\overline{\text{DAV}}$ (Data Available), as well as the eight bidirectional data lines $\overline{\text{D101}}$ through $\overline{\text{D108}}$, are controlled by U2. The bus transceiver outputs meet all requirements of IEEE STD 488-1978.

Under the direction of microprocessor U55, interface controller U2 mediates the transfer of data between the microprocessor data bus D0 ~ D7 and the GPIB. Controller U2 contains all necessary logic to decode messages from the IEEE-488 bus, control the GPIB and handshaking sequences, and supervise data transfer to and from the internal data bus. It should be noted, that although the GPIB signals follow negative logic convention, positive logic is used within the -488 interface. The GPIA controller is equipped with internal registers which are selected by register select lines RS0, RS1, and RS2, and chip select $\overline{\text{CS}}$ (from pin 6 of address decoder U41). The registers accommodate functions such as address, data-in, data-out, interrupt status, etc.

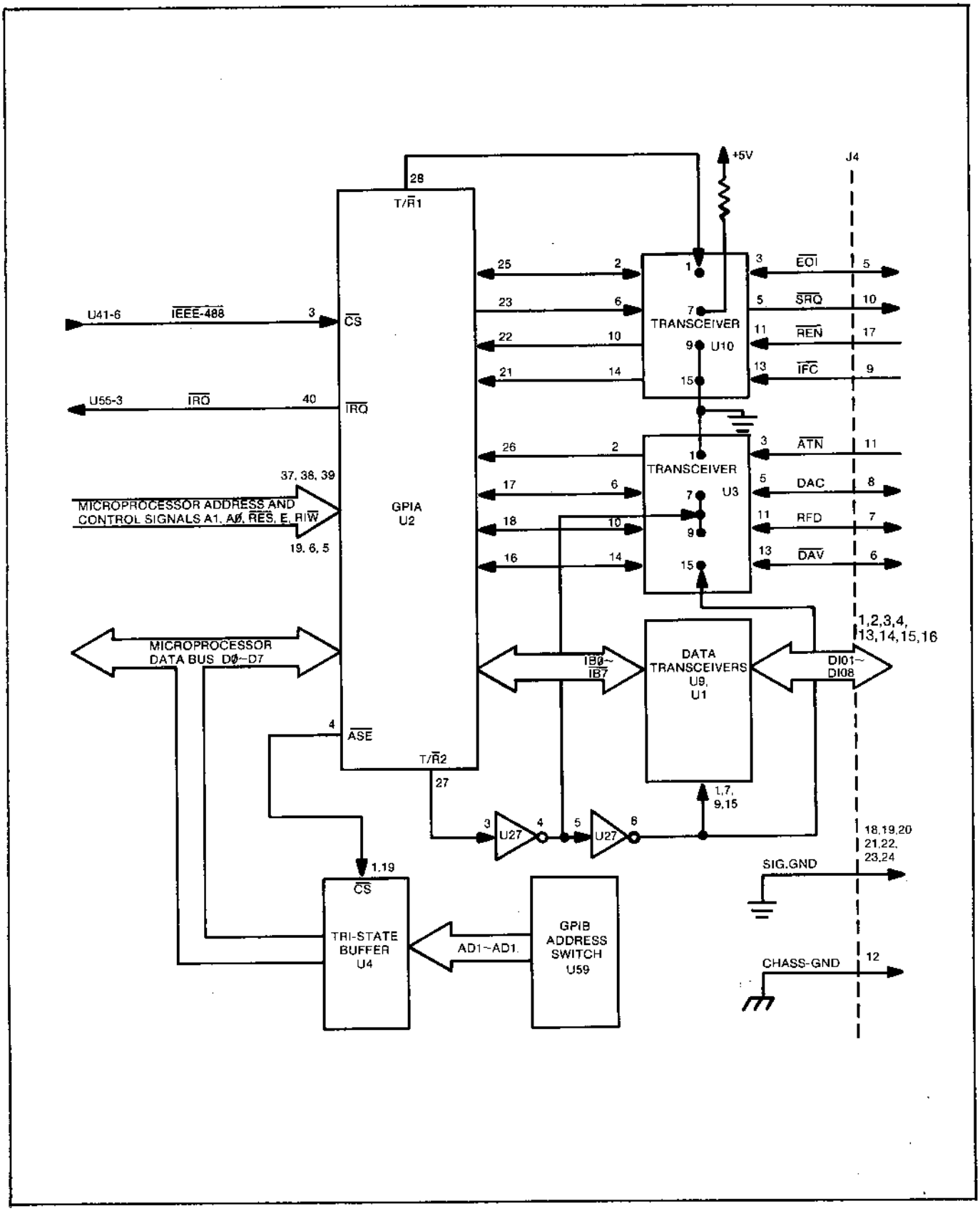


Figure 3-10. IEEE-488 (GPIB) Interface Block Diagram (Bottom Board)

The transfer of data between GPIA U2 and microprocessor U55 is directed by chip select $\overline{\text{IEEE-488}}$ (from U41-6), address lines A0, A1, and A2, and control lines $\overline{\text{RES}}$, E, and R/W. The GPIA alerts the processor of various conditions (input register full, output register empty, etc.) by means of interrupt line $\overline{\text{IRQ}}$ to U55-3.

The 5-bit GPIB address is user-selectable via rear panel switch S9. The setting of S9 is transferred to an internal register in U2 by the microprocessor at power turn-on over the D0 ~ D4 data bus lines when the ASE output line (address $\overline{\text{switch enable}}$ U2-4 to U4-1, 19) is asserted low.

The detailed operation of the GPIB is specified in IEEE STD 488-1978. The standard defines a negative logic format as follows:

Logic 0 = False = High (2.0V)

Logic 1 = True = Low (0.8V)

A summary of the GPIB signals is as follows:

$\overline{\text{EOI}}$ (End or Identify): True level on this bus management control line indicates end of a multiple byte transfer. When used with $\overline{\text{ATN}}$, performs parallel polling sequence.

$\overline{\text{SRQ}}$ (Service Request): Device sets this output line true when it requires service from the interface controller.

$\overline{\text{REN}}$ (Remote Enable): This controller-driven line is used with other messages to select source of device programming data (i.e., front panel or GPIB control).

$\overline{\text{IFC}}$ (Interface Clear): This controller driven line is set true to put all bus-controlled interfaces in their idle states.

$\overline{\text{ATN}}$ (Attention): This control line specifies how data on the data lines are to be interpreted and what devices must respond to the data. When $\overline{\text{ATN}}$ is true, the D101 ~ D108 lines carry addresses or commands. When $\overline{\text{ATN}}$ is false, the data lines carry data.

NDAC (Not Data Accepted): When set false by a device, this handshake line indicates that the device is ready to accept data.

NRFD (Not Ready For Data): When set false by a device, this handshake line indicates that the device is ready to accept data.

$\overline{\text{DAV}}$ (Data Available): When set true, this handshake line indicates that valid data has been presented on data lines D101 ~ D108.

$\overline{\text{D101}}$ (LSB) ~ $\overline{\text{D108}}$ (LSB) (Data Input-Output): These lines carry data in bit-parallel, byte-serial form. Information of these lines represents either address/commands or data, depending on the logic state of the attention line.

3.4.5 RS-232 INTERFACE CIRCUITRY (Bottom Board: Reference Block Diagram Figure 3-11)

The Exerciser RS-232 interface is comprised of ACIA U15 (asynchronous communication interface adapter); driver U6; receiver U11; baud rate generator U14; oscillator U13; and half of J-K flip-flop U25.

The oscillator circuit, consisting of crystal Y1 and oscillator U13, outputs a 1.8432 MHz square wave from U13-8 to U25-1. J-K flip-flop U25 divides this frequency by two, outputting a 921.6 kHz square wave from U25-5 to U14-5. Baud rate generator U14 is a variable frequency divider. By configuring the baud rate select inputs by means of the appropriate jumper wires between E-19-E20...E25-E26 (refer to paragraph 2.11.2.3), the baud rate generator will output a square wave at a frequency of sixteen times the selected baud rate to U15-3, 4 (RxCLK, TxCLK). The 4-bit code for the output frequency is latched into U14 by a negative pulse from U16-39 to U14-13 following power turn-on. For example, if the desired baud rate is 9600 (factory setting, all jumpers open), the output at U14-3 will be 16 x 9600 = 153.6 KHz.

Driver U6 serves as a buffer between ACIA U15 and the RS-232 serial bus. It inverts and level-shifts the serial digital data to TxD (Transmit Data) and levels to RTS (Request To Send) to the appropriate voltage, impedance, and rise/fall times required to drive the RS-232 I/O lines. The ± 15V power inputs to U6 are derived from the instrument's ± 15V lines by means of resistors R4 and R5 and zener diodes CR2 and CR3. Receiver U11 downshifts the serial data from RxD (Receive Data) and levels from DCD (Data Carrier Detect) and CTS (Clear To Send) to 5V logic inputs to ACIA U15.

ACIA U15 contains four internal 8-bit registers. The four registers are data output, data input, control (write only), and status (read only). Data transfers between the various registers and microprocessor U55 take place over data bus lines D0 D7, under the control of chip select RS-232 (from U41-5), address lines A0 (RS, register select), R/$\overline{W}$ and E. The ACIA informs the microprocessor of a change in status, such as input register full, output register empty, or error condition, by asserting interrupt line $\overline{FIRQ}$ low (U15-7 to U55-4).

The primary function of ACIA U15 is to convert 8-bit parallel ASCII data characters from microprocessor U55 to 10-bit NRZ serial data at TxD (U15-6 to U6-2), and to convert 10-bit serial TTL data (RxD, U11-3 to U15-2) to 8-bit parallel ASCII characters to be transferred to the microprocessor. The baud rate (bit data rate) of the serial data will be one sixteenth of the frequency of the TxD and RxD clock input frequency (U14-3 to U15-3, 4). A secondary function of the ACIA is to control handshake lines RTS, DCD, and CTS. RTS is asserted low prior to the start of transmission. When CTS is asserted high by the receiving device, the ACIA will initiate its transmission. When the RS-232 I/O is connected to a modem, DCD indicates the presence of received carrier. It may be noted that DCD and CTS are pulled high by means of resistors R7 and R6. This enables the RS-232 I/O to be operated as a three-wire interface consisting of TxD (J3-2), RxD (J3-3), and Signal Ground (J3-7). This is the normal configuration used for connecting to CRT terminals.

It may also be noted that the Exerciser's RS-232 port is configured to echo back all received characters. In addition to serving as a handshake mechanism, the echo feature facilitates troubleshooting of the RS-232 circuitry.

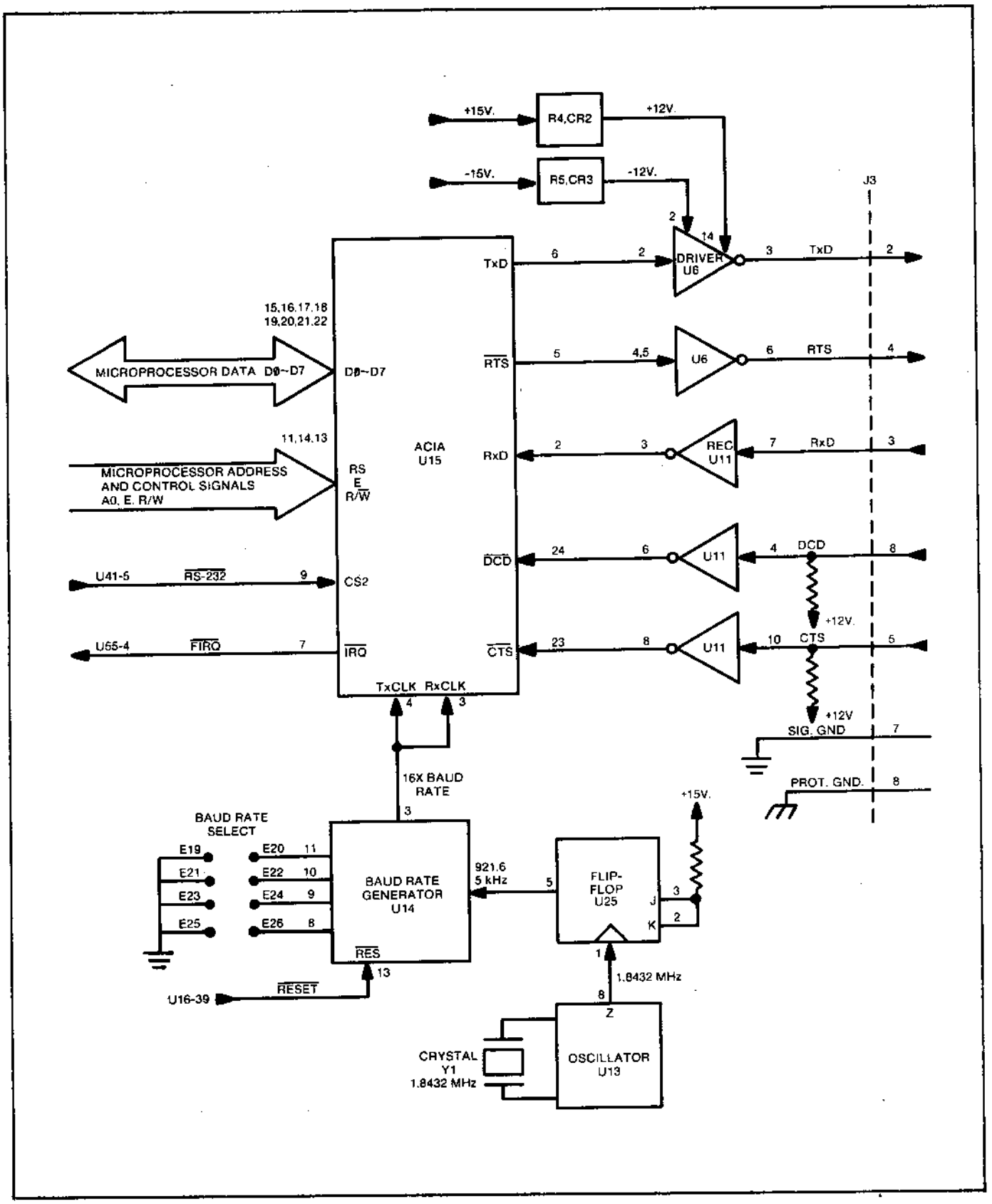


Figure 3-11. RS-232 Interface Block Diagram (Bottom Board)

3.5 1553 FRONT END CIRCUITRY
(Top Board: Reference Block Diagram Figure 3-12 and Timing Diagram Figure 4-1)

The 1553 front end circuitry is comprised of 1556 error-generating encoder U50 and encoder buffer latches U39, U60, U38, and U62; 1555 decoder U59 and decoder buffer latches U46, U67, U44, and U65; multiplexer U27; transceiver U28; pulse transformers T1 and T2; and potentiometer R1 and switch S5 on the front panel.

Words to be transmitted by the Exerciser are transferred from the message RAM in two 16-bit words over the internal memory data bus MD0 ~ MD15. A negative pulse on T-LOAD-L transfers the 16-bit message word data to buffer latches U39 and U60. This is followed by a negative pulse on E-LOAD-L, which transfers sync type and error control information to buffers U38 and U62.

The encoder transmission will begin approximately 2.5-3.0 us after ENCODE ENABLE is brought high. On the falling edge of the 750 ns T-LOAD pulse, data from the buffers is latched into the encoder, initiating the transmission of the first word. The 1556 error-generating encoder converts 16-bit parallel data (plus error and control inputs) to bi-phase TTL Manchester II encoded serial data. The serial data will either be valid or will include induced encoding errors, depending on the programming of the various error lines (refer to paragraph 2.9.1.7).

The bi-phase serial outputs TxD are routed to the input of 8559 transceiver U28. Part of U28 is comprised of a 1553 transmitter whose output amplitude is determined by the setting of four-turn potentiometer R1 on the front panel. This level, between 0 and 15 VDC, is amplified by power amplifier U20 to provide the VCC supply voltage to the transmitter output stage.

The transmitter in U28 contains waveshaping and power amplifier circuitry to drive the 1553 to the required voltage amplitude. By means of front panel switch S5, the user may direct the bus output to either channel A (CH. A front panel, connector J12 on rear panel) or channel B (CH. B front panel, connector J13 on rear panel). The bus signal is coupled by means of either pulse transformers T1 or T2. The two transformers provide the appropriate voltages and impedances for either direct coupling (front panel) or transformer coupling (rear panel). The other portion of transceiver U28 contains the necessary filtering, comparison, and level-shifting circuitry to convert the voltage levels from the 1553 to bi-phase TTL Manchester II serial data. For normal Exerciser operation, this serial data is routed to the input of 1553 decoder U59 by means of multiplexer U27. For self-test mode, the TEST line from P6-A36 is set high, inhibiting the transmitter in U28 and routing the encoder output to the decoder input via U27.

The 1555 error-detecting decoder converts the bi-phase TTL Manchester II serial data to a 16-bit parallel output. Additional output lines indicate sync type, error conditions, and bus activity.

At the end of each received word, the decoder outputs a positive 125 ns LOAD PULSE. The rising edge of this pulse latches the decoder parallel data and error inputs into buffers U46, U67, U44, and U65. The contents of these buffers are then transferred over the memory data bus MD0 ~ MD15 to message RAM as two 16-bit words. The first word, containing 16-bit message word data, is enabled from the outputs of latches U46 and U67 by a negative pulse on R-ENABLE-L. The second word, containing

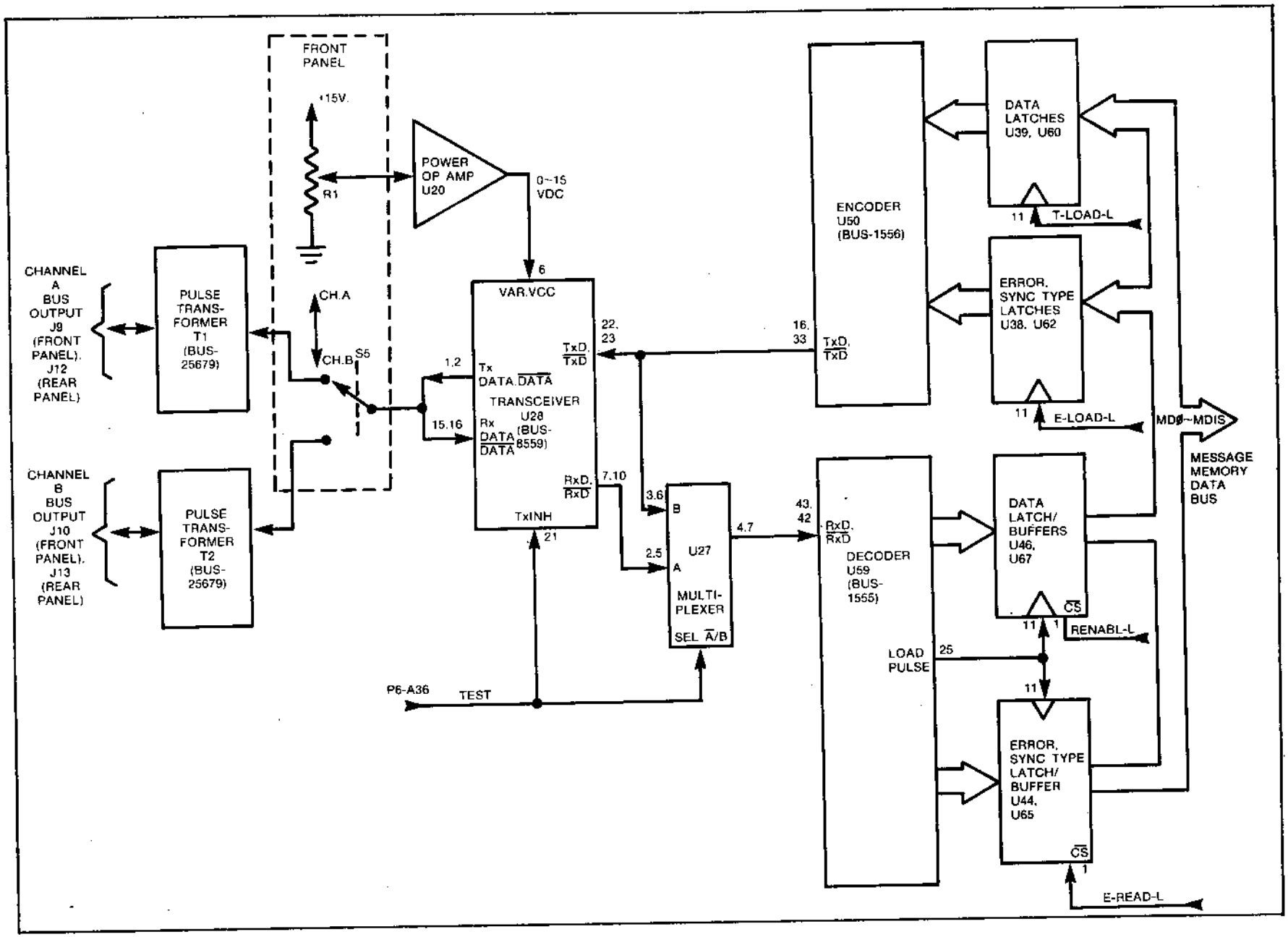


Figure 3-12. 1553 Front End Circuitry Block Diagram (Top Board)

sync type and error information, is enabled from latches U44 and U65 by a negative pulse on E-READ-L.

Paragraph 4.4 contains a timing diagram and detailed discussion illustrating the 1553 front end timing sequence.

3.6 POWER SUPPLY CIRCUITS (Bottom Board: Reference Figure 3-13)

The Exerciser DC power supply is comprised of two sections:

(i) A +5V Supply
(ii) A ±15V Supply

AC power is provided to the Exerciser via J1 POWER connector on the rear panel. Power is fused by F1 (rear panel) and switched by front panel POWER switch (S1). Rear panel VOLTAGE SELECT switch (S2) selects between parallel and series connections to the primaries of power transformers T1 through T4 for 115V and 230V operation, respectively.

3.6.1 +5V POWER SUPPLY

The secondaries of transformers T2, T3, and T4 are connected in series, resulting in approximately 19 VAC from T2-5, 7 to T3-6, 8 under normal instrument loading of the +5 VDC supply. This voltage is full wave rectified and filtered to approximately +24 VDC by the combination of rectifiers CRA1, CRA2, resistor R12, and capacitors C80 and C67. The +24V unregulated voltage is used to energize the power amplifier on the top board.

The +24V is regulated down to +18V by the circuit of R23, CR7, and Q2, providing the VCC to switching regulator U18. The output of U18 (pin 10) performs voltage regulation by pulse-width modulating (duty cycle modulation), the base drive to Darlington power transistor Q1. The waveform on the collector (case) of Q1 will normally be a rectangular pulse train with an amplitude of approximately 24V and positive duty cycle of about 20 to 40 percent. The output current pulses pass through toroidal current transformer CT1. The secondary voltage of CT1 is attenuated by current-limit potentiometer R31, providing current feedback (AC rectified by CR6) to U18-8.

The pulsating voltage is then filtered by the combination of inductor L1 and capacitor C49 to provide the low-ripple, regulated 5 VDC output.

Shottky diode CR1 allows the current to continue flowing through L1 during the off portion of the Q1 duty cycle.

Overvoltage protector VS1 clamps the output voltage to +6.3V in case of a regulator malfunction.

The network of resistors R34 and R36 and potentiometer R33 provides adjustment capability and voltage feedback to switching regulator U18-6.

Resistor R22 provides a path to ground for the pulsating switched current from Q1.

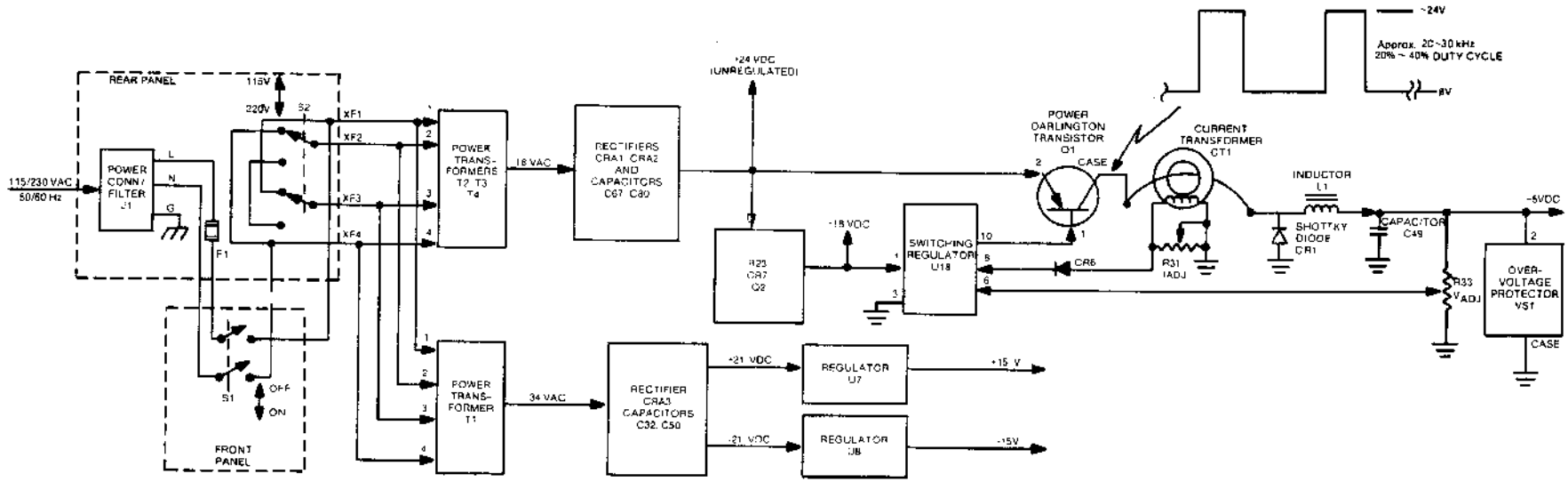


Figure 3-13. Power Supply Circuits Block Diagram

The network of R17, R18, C24, and C26 provides frequency compensation to the switching regulator.

3.6.2 ±15V POWER SUPPLY

The secondary of power transformer T1 delivers approximately 30 VAC from T1-5 to T1-8. This voltage is rectified and filtered by rectifier CRA3 and capacitors C32 and C50 to approximately +21V and -21V at TP9 and TP18, respectively.

The +15V regulated DC output is derived from the +21V line by means of series regulator U7. Likewise, the -15V output is derived from the -21V line by means of series regulator U8.

SECTION 4

MAINTENANCE

4.1 GENERAL

This section contains procedures and data that will help ensure continuity of service of the instrument. Troubleshooting and calibration procedures are included, as well as schematic diagrams and parts location diagrams of the equipment. It should be pointed out that a portion of the top PCB assembly is considered a proprietary design by DDC. There are no references to this block of circuitry included in the troubleshooting discussion. If a failure should occur in this portion of the instrument, the unit must be returned to the nearest ILC DATA DEVICE CORPORATION field office for servicing.

4.2 PREVENTIVE MAINTENANCE

At six month intervals (or more frequently, if the instrument is used in a very dusty environment), clean the exterior of the unit with a soft brush or cloth. In addition, it may sometimes be necessary to clean the mesh filter that is located behind the fan in the rear panel. This may be done by removing the filter and running water through it. No other preventive maintenance is required.

4.3 TROUBLESHOOTING

Table 4-1 provides troubleshooting hints which should prove useful when troubleshooting in the field is required. Use this data in conjunction with the schematic diagrams and parts location diagrams to isolate problems. All ICs, as well as the encoder and decoder modules, and the transceiver hybrid, are socketed to facilitate replacement. Parts identification data appears in Section 5.

Table 4-1. Troubleshooting Guide

SYMPTOM	POSSIBLE CAUSE/CORRECTIVE ACTION
Display is blank.	1. POWER connector/Filter J1. 2. Fuse F1. 3. POWER switch (S1). 4. VOLTAGE SELECT switch (S2). 5. +5V Power Supply. Verify +5V ± 1V from J12-6 to J12-2 (or TP26, ground). If this voltage is 5V ± 2V, adjust potentiometer R33 for +5, ± 0.1 VDC. Also, verify that current limit potentiometer R31 is appropriately adjusted (not fully CCW). If

	there is no voltage or low voltage (<3 VDC) at J12-6, verify the unregulated voltage at J12-3 to be +24 ± 5 VDC. At this point, it should be possible to isolate the power supply fault into one of two groups of components: (bottom board). (i) Unregulated +24V Supply: T2, T3, T4, CRA1, CRA2, R12, C80, C67. (ii) Regulated +5V Supply: Q2, CR7, U18, Q1, CT2, L1, C49, VS1, R31, R33, and associated passive components. 6. PIA U40 (bottom board). 7. Display drivers U9, U10, U11 (display board).
Fan is not taking in air.	1. Check if fan blade is free to turn. 2. 110/220 voltage select switch S2. 3. Resistor R53, capacitors C82, C83 (bottom board). 4. Mesh filter clogged.
Display is random/non-operational.	1. Verify 4 MHz clock input to microprocessor U55 (bottom board). If not present, verify operation of line receiver U50 (bottom board). If no input, check for 16 MHz output at U59-13 on top board. If present, check for 4 MHz clock at pin 4 of counter U34. Check for 4 MHz at input pins 10, 12, and output pins 13 (+) and 11 (-) of line driver U51 (top board). 2. If clock is present, verify operation of microprocessor U55 and associated components of the bottom board: (i) Check 1 MHz clocks E and Q at U55-34, U57-14 and U55-35, and U57-16, respectively (bottom board). (ii) Check for High on $\overline{\text{RESET}}$ input U55-37. (iii) Check READ/$\overline{\text{WRITE}}$ output at U55-8, U57-12. (iv) Check for data lines D0 ~ D7 going high and low and verify operation of data buffer U56.

(v) Check for address lines A0 ~ A15 going high and low and verify operation of address buffers U53, U54.

(vi) Check for 750 ns negative-going pulses at address decoder outputs U41-1,2...17 and gate outputs U42-6, 8, 11.

(vii) Check for Read operation of EPROMs U22, U23, U24; RAMs U31, U32, U34, U34; associated address decoder U43; and gates of U44 and U58. A failure in RAMs U31, U32, U34, U35 will cause the instrument display to freeze before attempting to execute the Blank Display portion of the power turn-on sequence.

(viii) Check $\overline{IRQ}$ and $\overline{FIRQ}$ interrupt signals at pins 3 and 4 of U55, respectively. If $\overline{IRQ}$ is held low, check circuitry driving U26-4 in the parallel I/O handshake circuitry (U38, U39, etc.), U2-40 in the IEEE-488 interface section and timer interrupt output U29-9 (top board). If $\overline{FIRQ}$ is held low, check circuitry controlling U26-2 from keyboard interface (U43, U47, U39, U44, U45 on bottom board) and the interrupt output pin 7 of ACIA U15 in the RS-232 interface (bottom board).

3. Check outputs of U40 (bottom board), pins 9, 11, 12, 13, 15, 16, 17, providing pulses to update display.

4. If display data, clock, and enable outputs from bottom board are present, check for updating of display driver outputs at U9, U10, U11 - 2, 3, 4 ... 18, 26, 27, ... 40. (display board).

5. Also verify for correct adjustment of potentiometers R1, R2, and R3. These control the display intensities of DS1, DS2, ... DS10, DS11, ... DS16.

   R1 should be adjusted for 2 ± 0.1 VDC across TP2(+) to TP1(-). Likewise, R2 should be adjusted for 2 ± 0.1 VDC across TP4(+) to TP3(-), while R3 should be adjusted for 2 ± 0.1 VDC across TP6(+) to TP5(-).

Some displays are faulty.	1. Check for segment currents (approximately 13.3 ma per segment) at 7-segment displays DS1 through DS10 and individual LEDs DS11 through DS18 and DS22. During Lamp Test (or at various times during Exerciser operation), the individual LEDs DS17, DS18 ... DS21 will be driven by approximately 10 ma of current. 2. Fault isolate between driving circuitry and display LEDs. 3. If the Real Time LEDs DS17 (ON-LINE), DS18 (LINE ACTIVE), DS19 (BUS FAULT), DS20 (REPLY T/OUT) and DS21 (XMTR T/OUT) fail to illuminate during lamp test following power turn-on and during operation, troubleshoot to various individual OR gates of U7, U8 (display board).
There are failures of internal self-test.	1. If the Exerciser fails any portion of its internal self-test following power turn-on, the word FAIL will be displayed in the 16-BIT DATA display field and a two-digit HEX failure mode code will be displayed in the ERROR display field. 2. The indicated hex failure code will be the sum of the bit codes for the individual fault conditions as follows: 01, 02: EPROM Checksum Fault 04: Message RAM Fault 08: RT Trigger RAM Fault 10: Encoder/Decoder Wraparound Test Fault 3. Troubleshooting for the individual fault modes should proceed as follows: (i) EPROM Checksum Fault (01, 02, 03): for this condition, the error code will indicate either 1, 2, or 3. The number indicates the actual number of individual EPROM devices that failed their checksum verification tests. The EPROMs are ICs U22, U23, and U24 on the bottom board. The individual programmed devices are designated by their DDC 12-digit part numbers as follows: U22: 4663-1002-0042 U23: 4663-1002-0022 U24: 4663-1002-0032

If the checksum fault still persists after replacing all three EPROMs, the problem must be isolated from among the address decoding circuitry U41 and U42, address buffers U53 and U54, and data buffer U56.

(ii) Message RAM Fault (04): The most probable cause of this failure will be a fault of RAM ICs U52, U53, U54, and U55 on the top board. Otherwise, the problem must be isolated from among data buffers U45 and U66, address buffers U56 and U21, and address decoding PAL U57 along with AND gate U58 (top board).

(iii) Trigger RAM Fault (08): The primary cause of this failure will be a fault in RAM U49 on the top board. A secondary cause of this failure may arise from data buffer U30, address buffer U48, address decoding PAL U22, latch U47, inverter U3, and PAL U1, all on the top board.

(iv) 1553 Encoder/Decoder Wraparound Self-Test Failure (10): A failure of this test indicates there is a probable fault in the 1553 front end circuitry. The principal components in this section of the top board are encoder U50 (1556) and decoder U59 (1555). Other components that could cause a failure of this test are encoder buffers U38, U59, U60, U62; decoder buffers U44, U46, U65, U67; multiplexer U27; latch U11; and OR gate U12. In addition, the failure may also arise from a fault in sequencer U5; PALs U1, U2; and latches U37, U40 or counters U36, U63, U64. Applicable to the failure of this test, there is a diagnostic software routine that may be used. The use of this diagnostic feature is discussed in paragraph 4.4.

There is no response to keyboard entry.	1. Check for negative going $\overline{\text{FIRQ}}$ pulses from U26-2 following the closure of any key (except CNTL). If pulses are present, then troubleshoot as follows: (i) Check for negative-going select pulses at U20-1, 19, and a high level at U20-17. This circuit informs the microprocessor that the keyboard is the cause of the interrupt (bottom board). (ii) If the CHIP-SELECT pulses are absent from U20, troubleshoot the address decoding path from U41-4 to U43-15 to U43-9 to U20-1, 19. (iii) If the CHIP-SELECT pulses are present at U20, verify that the microprocessor is reading a high level on the D7 line (bottom board). (iv) If the microprocessor is reading a high level from U20-3, verify a 250 ms (approximately) positive pulse from U47-13 (bottom board) to U4-11 (display board). If this pulse is not present at U4-11, troubleshoot to one-shot U47-13 (bottom board) and connectors P5 (bottom board) and J15 (display board). If the pulse is present, verify for 750 ns negative-going CHIP-SELECT pulses at U4-1 (display board). If this pulse is absent, troubleshoot address decoding path from U41-3 and U54-9 to OR gate U31-6 and P5 (bottom board), via J15 (display board). (v) If the LATCH and CHIP SELECT pulses are present at U4-11 and U4-1, respectively, the problem must be troubleshot from among keyboards KB1 and KB2; RUN and HALT switches S3 and S4; priority encoders U1, U2, and U3; AND gates U5 and U6; and latch U4 (display board). In conjunction with pull-up resistor arrays RA1, RA2, and RA3, the individual pushbuttons pull the respective lines low going into U1, U2, and U3. Pressing any of the 23 keys (excluding CNTL) produces a unique 5-bit code

	at pins 14, 17, 18, 8, and 13 of U4. The signals at U4-8, 13 identify which priority encoder (U1, U2, U3) has the active input, while the levels at U4-14, 17, 18 provide a negative-true representation indicating which input line is pulled low (0 ~ 7) to the designated encoder. The input signals at pins U4-3, 4, and 7 are pulled low when the RUN, HALT, and CNTRL buttons, respectively, are pressed. The signals present on the microprocessor data bus D0 ~ D7 during the CHIP-SELECT (U4-1) should correspond to the code presented to U4-3, 4...13 at the rising edge of the pulse at U4-11. 2. If a negative-going signal is not present at U26-2 ($\overline{\text{FIRQ}}$) following a key closure, troubleshoot as follows: (i) Verify a positive level at U39-11 (bottom board) when a key is pressed. If this level is not present, troubleshoot from U3-15 (display board) to 39-12 (bottom board), or from S3, S4 (display board) to U44-10, 9, 8 (bottom board), if RUN or HALT is pressed. (ii) If a high level is present at U39-11, verify for a 250 ms positive pulse at U47-13 when a key is pressed and a 370 ms negative pulse at U47-12 when either a key is released or a key bounces after a closure. Verify that U43-9 goes low with U43-8 going high following each key closure.
There is no output on 1553 (either Channel A or B).	1. Verify a variable DC voltage at pin 6 of transceiver U28 (top board). This voltage should vary smoothly from 0 to 15 VDC as the front panel potentiometer is rotated clockwise. 2. If the voltage is correct at U28-6, verify for positive pulses at TC DATA (U28-1, 15) and TC DATA (U28-2, 16). If these are present, troubleshoot from among front panel CHANNEL SELECT switch S5 and pulse transformers T1 and T2; isolation resistors R1,

	R2, R3, R4 (top board); connectors J9, J10 (front panel) and J12, J13 (rear panel); and associated cabling. 3. Check for +15 VDC and -15 VDC at pins 13 and 19 of U28, respectively. If not present, troubleshoot ±15 VDC Power Supply on the bottom board as follows: (i) Verify 15 ± 5 VAC at T1-5 and T1-8. (ii) Verify +21 ± 4 VDC at TP-9 and -21 ± 4 VDC at TP-18. (iii) Isolate fault from among T1, CRA3, C32, and C50 and voltage regulators U7 and U8. 4. Verify bi-phase TTL Manchester II encoded serial data at pins 22 (TxD) and 23 (TxD) of transceiver U28. 5. If TTL Manchester II encoded serial data is not present at TxD and TxD, verify for logic 1 pulses at pin 7 (ENCODER ENABLE) of encoder module U50. If ENCODER ENABLE is high, the 2 MHz clock is present at U50-26, and the encoder module is not outputting TTL Manchester II serial data, encoder module U50 is faulty. 6. If the 2 MHz clock signal is not present at U50-26, the fault lies in counter 34. 7. If the Exerciser fails to go ON-LINE to the 1553 after pressing RUN, verify for the correct levels, depending on operating mode, at U29-7, 9, 12, 16, 18 on the bottom board. If these are not present, troubleshoot between PIA U16 and buffer U29. 8. If there are no positive pulses at ENCODER ENABLE (U50-7) and no negative pulses at ENABLE-L (U4-1), the fault lies in the proprietary section of the top board. In this case, the unit must be returned to the nearest DDC field representative for servicing.
There is no sync output at J11 (front panel), J13 (rear panel).	1. Check for positive pulses at U19-3 (top board). If present, the fault lies in connectors J11, J13, or interconnection cabling. 2. Verify BCA signal at U19-2. If not present, the fault is in the proprietary portion of the top board and the unit must be returned to DDC for servicing.

There are 1553 message formatting, timing, or protocol errors.	1. A large number or problems are symptomatic of faults in the proprietary (1553) portion of the top PCB assembly. A partial listing of these symptoms follows: (i) Incorrect message formatting. (ii) No remote terminal response. (iii) Incorrect transmitted word count. (iv) Response, intermessage gap and/or frame times not agreeing with programmed values. (v) Intermittent transmission. (vi) Incorrect data transmitted. (vii) Failure to correctly store received data. (viii) Failure to detect errors in received portions of messages. If the unit displays any of these failure modes, it must be returned to the nearest DDC field office for servicing.
Parallel interface is not accepting WRITE data.	1. Verify low pulse at U26-4 ($\overline{IRQ}$) following $\overline{WRITE}$ (J2-10) being asserted low. If not present, troubleshoot signal path from J2-10 to U26-4 via U27-8, U39-3, U38-5, U49-3. 2. If $\overline{IRQ}$ is pulling low, verify for a 750 ns negative-going pulse at U28-1, 19. If this pulse is absent, troubleshoot address decoding path from U41-4 via U43-12 to U28-1, 19. 3. If the pulse is present at U28-1, 19, verify for a logic one at U28-18 (D7) and U28-16 (D6) and a logic zero at U28-3 (D0) during this pulse. If these three levels are not present, troubleshoot from among buffer U28, switch S8, and resistor R3. 4. If the data from U28 is being read properly, verify for 750 ns negative pulses at pin 1 of latch U17. If this pulse is not present, troubleshoot address decoding path from U41-4 to U43-11 to U17-1. 5. If pulses are present at U17-1, verify that the data on D7 ~ D0 (U17-2, 5, ... 19) is identical to the data presented at T7 ~ T0 (J2-1, 2, ... 8) at the time of the falling edge of WRITE. If the data

	does not match, fault isolate from among U12, U5, U17, and RA1. 6. If the instrument is not providing $\overline{\text{WACK}}$ and $\overline{\text{TACK}}$ handshake outputs (active low) following each $\overline{\text{WRITE}}$ cycle, troubleshoot signal path from address decoder U43-11 to latch U48-5, gate U45-6, and open collector buffers U26-6 and U26-10. In addition, it should be verified that U37-8 goes high during a WRITE operation and stays low otherwise.
Parallel interface is not outputting READ data.	1. Verify for a low pulse at U26-4 ($\overline{\text{IRQ}}$) following $\overline{\text{READ}}$ being asserted low (J2-9). If not present, troubleshoot signal path from J2-10 to U26-4 via U27-8, U39-3, U38-5, U49-3. 2. If $\overline{\text{IRQ}}$ is pulling low, verify for a 750 ns negative-going pulse at U28-1, 19. If this pulse is absent, troubleshoot address decoding path from U41-4, via U43-12 to U28-1, 19. 3. If the pulse is present at U28-1, 19, verify for a logic one at U28-18 (D7) and U28-14 (D5) and a logic zero at U28-3 (D0) during the time of the pulse. 4. If the data from U28 is being read properly, verify for a 750 ns negative-going CHIP-SELECT pulse at U16-23. If this pulse is absent, troubleshoot address decoding path from U41-4 to U43-10 to U16-23. 5. If the pulse is present at U16-23, verify that the correct 8-bit ASCII character is present at U16-9, 8...2 (PA7, PA6...PA0). 6. If the correct ASCII byte is present at U16-9, 8 ... 2, verify for a high level at U12-15 and U5-15. If this signal is low, verify for 500 ns negative pulses for each $\overline{\text{WRITE}}$ command at U27-12. If this pulse is absent, troubleshoot address decoding path from U43-10, U49-11 (also A0, A1 to U49-8) to U46-10, U37-6 to U27-12. If this pulse is present with U12-5 and U5-15 stuck low, the fault lies in flip-flop U36-5. 7. If U12-5 and U5-15 are high, with correct data at U16-9, 8 ... 2, the fault lies in transceivers U12 and/or U5.

	8. If the Exerciser is not providing $\overline{\text{RACK}}$ and $\overline{\text{TACK}}$ handshake outputs following an otherwise correct READ operation, the problem must be isolated from among U36-8, 9, U25-9, U45-6, and open-collector buffers U26-6 and U26-12. In addition, it should be verified that U37-11 goes high during a READ operation, and low otherwise.
Parallel interface SERVICE REQUEST output is not working.	1. Verify for a 10 us (approximate) negative pulse at U40-39 following the completion of a 1553 message sequence by the Exerciser. If this pulse is absent, the fault lies in PIA U40. Otherwise, the problem must be isolated between flip-flop U38-8 and open-collector buffer U26-8. 2. If the $\overline{\text{SERVICE REQUEST}}$ line fails to go high following a READ operation, troubleshoot from among inverter U27-10, flip-flop U38-8, and buffer U26-8.
RS-232 interface is not functioning.	1. Verify for correct output of baud rate generator at U14-3. The signal at this node should be a TTL square wave of frequency 16 times the programmed baud rate. The correct baud rate is determined by the installation of jumpers at E19-E20 ... E-25-E26, as discussed in paragraph 2.11.2.3. 2. If the correct frequency square wave is not present at U14-5, fault isolate as follows: (i) A 921.6 kHz square wave should appear at U25-5. (ii) A 1.8432 MHz squarewave should appear at U13-8. (iii) A high logic level should appear at U14-13, from PIA output U16-39, except for about 10 seconds following power turn-on. The fault component may now be determined from among U14, U25, U13, U16, and crystal Y1. 3. Verify for +12 VDC at U6-14. If not present, troubleshoot R4, CR2, C7. 4. Verify for -12 VDC at U6-1. If not present, troubleshoot R5, CR3, C8.

	5. Verify low levels at U28-12 (D4) and U28-5 (D1) during CHIP-SELECT negative pulses at U28-1, 19 following receipt of characters from the RS-232 port. If these are not present, fault-isolate from among U28, wires W1 and W7, and switch S8. 6. If the Exerciser is not accepting RECEIVE data at the RS-232 port, troubleshoot between receiver U11 and ACIA U15. 7. If the Exerciser RS-232 port is not echoing back received characters or outputting characters when requested to reply, troubleshoot between driver U6 and ACIA U15.
IEEE-488 interface is not functioning.	1. Verify setting of GPIB address switch S9 and for appropriate levels at U4-2, 4, 6, 8, 11. If not present, fault isolate from among switch S9, resistor array RA1, and buffer U4. 2. If the Exerciser is not responding to GPIB commands, verify for correct levels of handshake and data lines at transceiver outputs U10-2, 6 ... U1-10, 14. Also, verify for correct levels of handshake and data lines at U2-25, 23 ... 30, 29. 3. Verify low levels at U28-9 (D3) and U28-7 (D2) during negative pulses at U28-1, 19. If not present, fault isolate from among switch S8, wires W1 and W2, and buffer U28. 4. If the Exerciser is not transmitting properly over the GPIB when requested to TALK, verify for correct levels of handshake and data lines U2-25, 23, ... 30, 29. 5. All problems in the IEEE-488 interface may be fault isolated from among buffer U4; GPIA U2; inverter U27; and transceivers U10, U3, U9, and U1.

4.4 USING EXERCISER INTERNAL DIAGNOSTICS TO TROUBLESHOOT FAILURE OF 1553 FRONT END WRAPAROUND SELF-TEST

As mentioned in the discussion of failure of the internal self-test in paragraph 4.3, the Exerciser has built-in diagnostic software for troubleshooting of the 1553 front end circuitry.

A failure of the 1553 front end wraparound self-test will result in the 10-bit of the self-test fail code byte being set. The self-test fail byte for the Exerciser is defined as follows:

ERROR CODE (HEX)	FAILURE
40	Encoder/decoder wraparound test
20	RT Trigger RAM test
10	Message RAM test
08	EPROM 4 (U21) Checksum
04	EPROM 3 (U23) Checksum
02	EPROM 2 (U24) Checksum
01	EPROM 1 (U22) Checksum

The DDC part numbers for the EPROMs are as follows:

U21: 4663-1002-0090

U22: 4663-1002-0060

U23: 4663-1002-0080

U24: 4663-1002-0070

The wraparound test exercises the 1553 encoder and decoder circuitry as follows:

(i) The serial output (TTL) of encoder U50 is routed, via multiplexer U27, to the serial input of decoder U59 (top board).

(ii) The transmitter in transceiver U28 is inhibited, preventing the Exerciser from putting any traffic on the bus during self-test.

(iii) The self-test message is formatted as follows:

Message Block 1

Word 1	Word 2	Word 3
Receive Command Word 0821	Test Data Word Transmitted	Test Data Word Received

The encoder transmits two words: a receive command word, 0821, followed by the test word. Some test words are error-free and others contain induced encoding errors.

(iv) The decoded version of the test word is stored in position 3 of message block 1.

(v) A masked version (see discussion following) of the received word is compared to the known correct received word.

(vi) Steps (iii), (iv), and (v) are repeated for forty-seven (47) different test words, listed in Table 4-2.

Table 4-2. Front End Wraparound Test Words

TEST WORD NUMBER	TRANSMIT TEST WORD		KNOWN CORRECT RECEIVED WORD		ERROR TYPE
	DATA (BYTES 1,2)	ERRORS ETC. (BYTES 3,4)	DATA (BYTES 1,2)	ERRORS ETC. (BYTES 3,4)	
1	0000	0000	0000	80C0	No error-Data sync
2	FFFF	0000	FFFF	80C0	No error-Data sync
3	AAAA	0000	AAAA	80C0	No error-Data sync
4	5555	0000	5555	80C0	No error-Data sync
5	0123	4000	0123	8080	No error-Command sync
6	4567	4000	4567	8080	No error-Command sync
7	89AB	4000	89AB	8080	No error-Command sync
8	CDEF	4000	CDEF	8080	No error-Command sync
9	0000	0400	0000	8CC0	Manchester error-bit 1
10	0000	4401	0001	8C80	Manchester error-bit 2
11	0000	0402	0002	8CC0	Manchester error-bit 3
12	0000	4403	0004	8C80	Manchester error-bit 4
13	0000	0404	0008	8CC0	Manchester error-bit 5
14	0000	4405	0010	8C80	Manchester error-bit 6
15	0000	0406	0020	8CC0	Manchester error-bit 7
16	0000	4407	0040	8C80	Manchester error-bit 8
17	FFFF	0408	00FF	8CC0	Manchester error-bit 9
18	FFFF	4409	01FF	8480	Manchester error-bit 10
19	FFFF	040A	03FF	8CC0	Manchester error-bit 11
20	FFFF	440B	07FF	8480	Manchester error-bit 12
21	FFFF	040C	0FFF	8CC0	Manchester error-bit 13
22	FFFF	440D	1FFF	8480	Manchester error-bit 14
23	FFFF	040E	3FFF	8CC0	Manchester error-bit 15
24	FFFF	440F	7FFF	8480	Manchester error-bit 16
25	1235	2000	891A	8CC0	Manchester error-parity bit
26	ABCD	6000	D5E6	8C84	Manchester error-parity bit
27	0000	4100	0000	8180	High bit count error
28	FFFF	0100	FFFF	81C0	High bit count error
29	AAAA	0200	D555	8EC0	Low bit count error
30	5555	4200	AAAA	8E80	Low bit count error
31	0000	0800	0000	88C0	Parity error
32	0001	4800	0001	8880	Parity error
33	0000	1000	0821	8180	Sync zero-crossing error -early

Table 4-2. Front End Wraparound Test Words (Cont.)

TEST WORD NUMBER	TRANSMIT TEST WORD		KNOWN CORRECT RECEIVED WORD		ERROR TYPE
	DATA (BYTES 1,2)	ERRORS ETC. (BYTES 3,4)	DATA (BYTES 1,2)	ERRORS ETC. (BYTES 3,4)	
34	FFFF	5000	0000	8880	Sync zero-crossing error -early
35	1234	1010	0821	8080	Sync zero-crossing error -late
36	ABCD	5010	0821	8080	Sync zero-crossing error -late
37	0000	0110	0000	8100	Long word: +2 Bits
38	1111	5020	0821	8180	Sync error; CS
39	5555	5030	0821	8080	Sync error; CS
40	AAAA	1020	0821	8080	Sync error; DS
41	FFFF	1030	0821	8180	Sync error; DS
42	1234	0140	0089	8EC0	Word gap error
43	1234	0441	1234	84C0	Zero-crossing deviation error
44	5678	0452	5678	80C0	Zero-crossing deviation error
45	9ABC	0464	9ABC	80C0	Zero-crossing deviation error
46	DEF0	0478	DEF0	80C0	Zero-crossing deviation error
47	FFFF	5000	0821	8080	Interword gap error

Table 4-2 lists 47 transmitted and known correct receive words for the wraparound test. It should be noted, that for the known correct words, the error (third) received byte is masked with the byte 8F (hex), with the exception of test word 24, which is masked with the byte 87. That is, the message error and incorrect sync type bits (40 and 10 bits) are not part of the encoder/decoder function and are not included in the compare step and are indicated as zero in Table 4-2 and on the Exerciser front panel when performing the diagnostic procedure discussed below. For the received word/sync type (fourth) received bytes, the words are masked by the byte C0, except for word 26, where the mask byte is 80. For test word 24, the received parity error bit (08 of the third byte) is masked to zero since the detected logic sense of this bit for this test word is don't care. In addition, for test word 26, the received sync type bit is masked to zero (don't care).

The meanings of the relevant bits in the third and fourth bytes for transmitted and received words are repeated from Table 2-5 as follows:

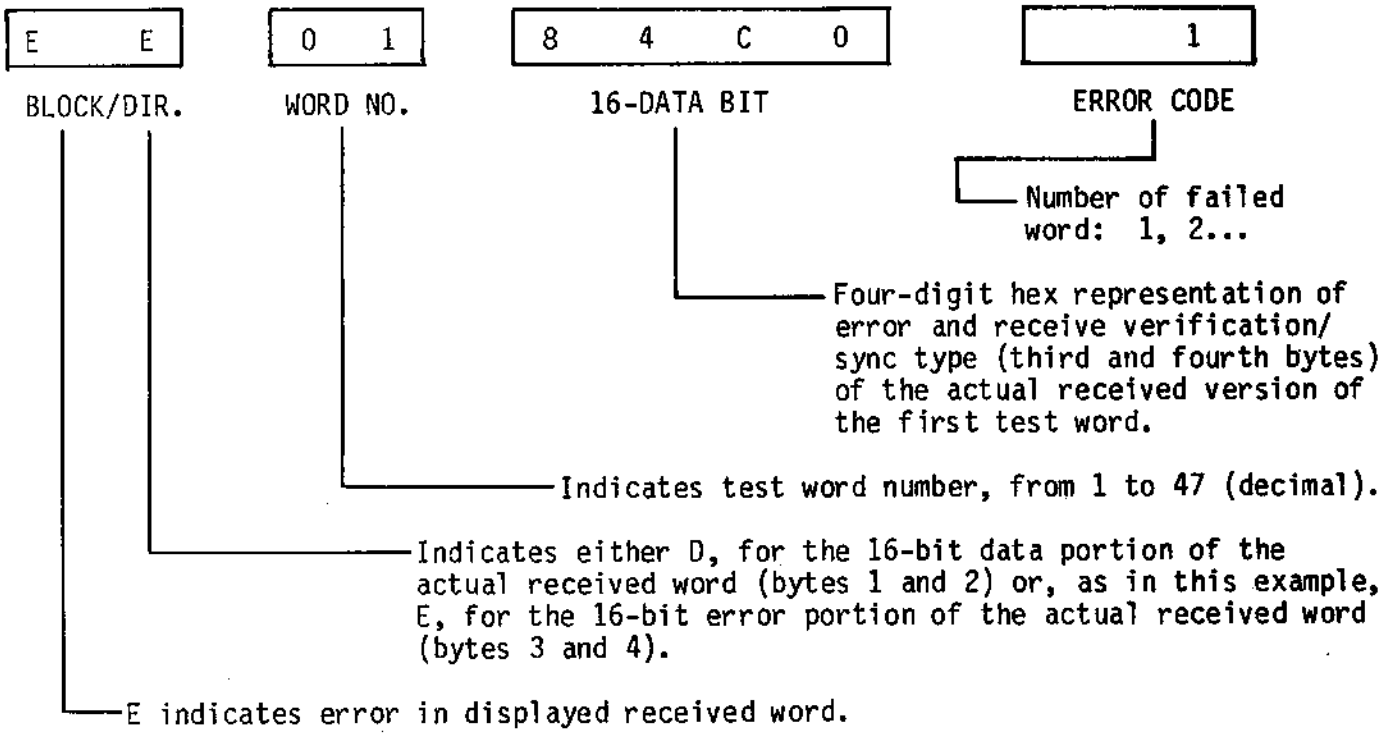
BYTE	BIT VALUE (HEX) 80	40	20	10	08	04	02	01
Transmitted Word : Error (third) byte	0	Incorrect Sync Type *	Parity Manchester Error	Sync Zero-Crossing Error	Parity Error	Manchester Encoding Error	Low Bit Count Error	High Bit Count Error
Transmitted Word : Error position (fourth) byte	1	0	0	Sync Error Position	Manchester Error Position 3	Manchester Error Position 2	Manchester Error Position 1	Manchester Error Position 0
Received Word: Error (third) byte	Pending-Receive/Transmit	0	0	0	Parity Error	Manchester Encoding Error	Low Bit Count Error	High Bit Count Error
Received Word: Receive Verification/Sync Type (fourth) byte	Transmit-Receive/Pending	Data/Command Sync Type *		0	0	0	0	0

*Note that the correct transmitted sync type for all test words is a data sync.

If the wraparound self-test fails following power turn-on (FAIL 40 indication), it is possible to determine which test word(s) were the cause of the failure by performing the following procedure:

(i) Press the CNTL and READ keys. The display will blank.

(ii) Press the CNTL and READ keys again. The display will now indicate the following (example):

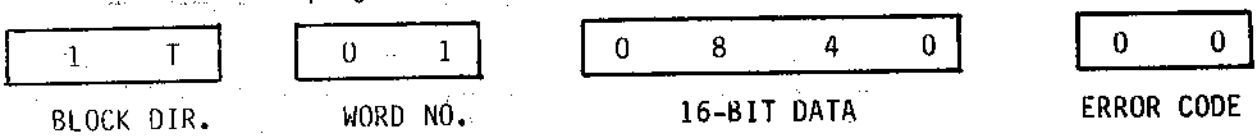


In the example shown, the failure is due to the Manchester Encoding Error bit (0400 bit) being set in the received error byte of the first test word.

occurred in the data (d) or error (E) portion of the current test word. If there are mismatches in both the data and error portions for a given word, the received 16-bit data will be displayed first, followed by the received 16-bit error coding for the word.

(iv) If CNTL and READ are pressed after all the failed test words have been reviewed, the display will revert back to the first failed data or error word and the test data may be reviewed once again.

(v) To escape from this diagnostic mode, it is necessary to enter the CLR key to put the exerciser in its normal power turn-on state. The display will then indicate:



At this time, it is possible to perform additional troubleshooting if so desired. If not, the instrument may be operated with the knowledge that a front end fault exists.

The troubleshooting procedure is as follows:

(i) Enter the following sequence via the front panel keyboard:

KEY SEQUENCE	EFFECT
CNTL, SN RP 1	Repeat mode of operation
CNTL, FR TM 9, 2, ENT	2 ms frame time
CNTL, FRMT 3, 2, 0, ENT	20 Format: Self-Test
PROG, 0	Command word of test message, 0821: Instrument's RT1 to receive one (1) data word.

KEY SEQUENCE	EFFECT
0 8 2 1	
NEXT WORD DIGIT DIGIT DIGIT DIGIT DIGIT DIGIT ENT	The test word is programmed as six hex digits. The first four digits represent 16-bit data for the test word. The last two digits represent the error byte, or third byte, of the test word.
CNTL ER BP 8 DIGIT DIGIT ENT	The two-digit hex error position or error modifier byte (fourth byte) for the transmitted test word specifies the error positioning for Manchester encoding and sync zero-crossing errors.
RUN	The message involving the test word in question is now being processed on a Repeat basis.

(ii) To view the test word message timing sequence, connect the Exerciser SYNC OUTPUT to the external trigger input of the oscilloscope. Connect the scope channels A and B to TxDATA (U50-16, TP40) and TxDATA (U50-33, TP41), respectively.

(iii) Observe the sequence illustrated in Figure 4-1. The self-test timing sequence occurs as follows:

(1) Sixteen-bit data for the command word 0821 on Memory Data Bus MD0 ~ MD15 is loaded into encoder data buffers U39 and U60 on the first rising edge of T-LOAD-L.

(2) The 16-bit error/sync type coding for the command word is loaded into latch U38 and U62 on the first rising edge of E-LOAD-L.

(3) ENCODER ENABLE is brought high to initiate the encoder's internal transmission sequence.

(4) Approximately 2 us after ENCODER ENABLE goes high, the encoder outputs a 750 ns T-LOAD pulse.

(5) The encoder starts the transmission of the command word on the falling edge of T-LOAD.

(6) The data for the test word is loaded into buffers U39, U60.

(7) The error and sync information for the test word is loaded into buffers U38, U62.

(8) The falling edge of the second T-LOAD pulse marks the start of transmission of the test word.

(9) ENCODER ENABLE is dropped. This will cause the encoder to stop transmitting at the end of the test word.

(10) Approximately 750 ns after the start of the test word, the decoder outputs a LOAD PULSE. The rising edge of this pulse loads the receive parallel word into the encoder buffer.

(11) The encoder terminates transmission at the end of the test word.

(12) 750 ns after the end of the test word, the decoder will usually output a LOAD PULSE. However, LOAD PULSE may be absent following some test words with encoding errors, particularly for sync field errors. The rising edge of LOAD PULSE latches the received test word parallel data (and errors, etc.) into decoder buffers U46, U57, and U65.

(13) Sixteen-bit test word data from decoder buffers U46 and U67 are made available on MD0 ~ MD15 by the negative pulse on R-ENBL-L. Near the end of this pulse, data is written into message RAM.

(14) Test word error (and sync type, etc.) information is made available on MD0 ~ MD15 by the negative pulse on E-READ-L. Near the end of this pulse, error information is written into message RAM.

(iv) Troubleshooting of the front end circuitry is as follows:

(1) The following faults indicate a problem in the sequence control and/or message RAM portions of the top board circuitry:

(a) T-LOAD-L or E-LOAD-L is missing.

(b) Missing or incorrect data on MD0 ~ MD15.

(c) Encoder enable stuck low (or high).

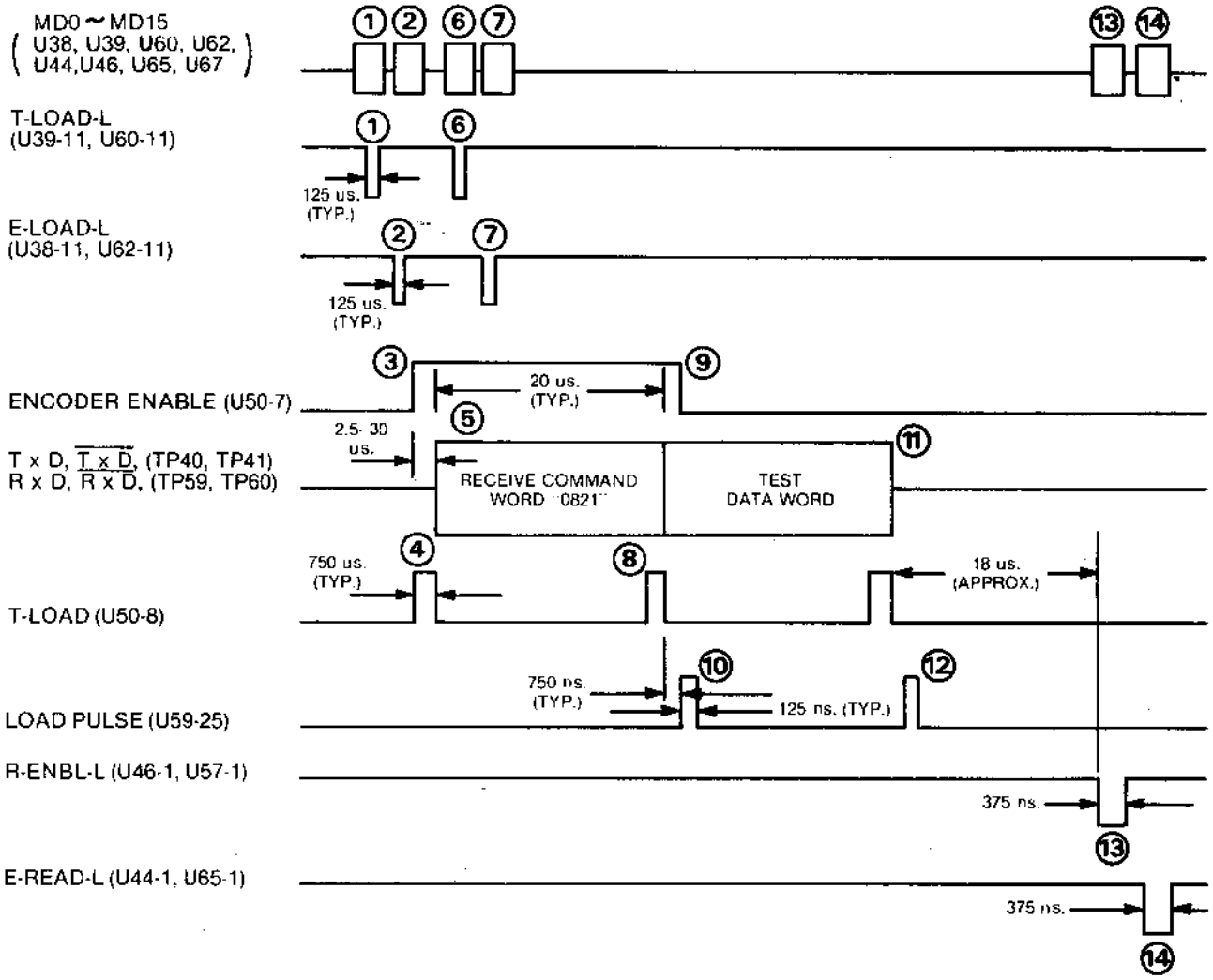
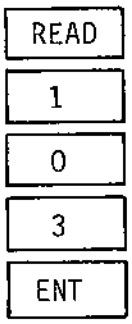


Figure 4-1. Timing Diagram for Wraparound Self-Test

(d) R-ENBL-L or E-READ-L missing.

(e) Self-test failing, even with correct received data on MD0 ~ MD15 during R-ENBL-L and E-READ-L. This may be confirmed, for a particular test word by halting the Exerciser and reading the received version of the test word memory. This is done by entering:



to read the first three bytes of the received word and by entering:



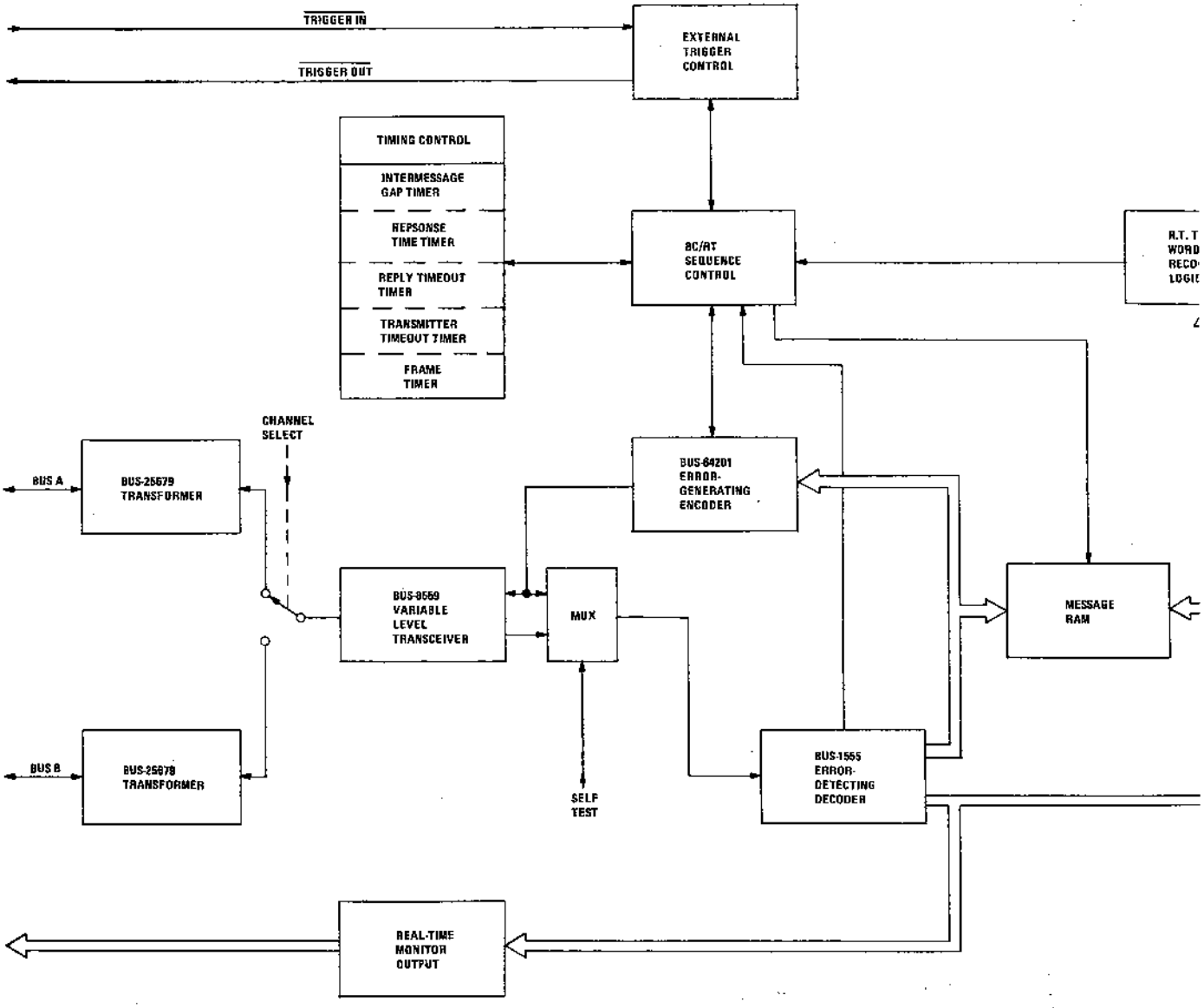
To read the fourth byte.

(2) Verify that the encoder is transmitting correct serial data on TxD and $\overline{\text{TxD}}$ for the current test word and is outputting T-LOAD pulses as shown in the timing diagram. If this is the case, skip to troubleshooting step (4).

(3) Verify that correct data and error information is presented to encoder inputs BIT 1, BIT 2, ... BIT 16, LONG WORD, ... MP3, SEP. If it is, the fault lies in BUS-64201 encoder module U50. If not, the fault is in latches U38, U39, U60, and U62.

(4) Verify that the serial data on RxD (TP59) and $\overline{\text{RxD}}$ (TP60) is identical to that on TxD (TP40) and $\overline{\text{TxD}}$ (TP41). If this is not the case, the fault is in multiplexer U27.

(5) Verify that decoder U59 is outputting correct data, error, and sync information at the time of the rising edge of LOAD PULSE (also verify for LOAD PULSE). If not, the fault lies in BUS-1555 decoder module U59. If the parallel data is correct, the fault must be isolated from among latches U44, U46, U65, and U67.


TRIGGER IN
TRIGGER OUT
EXTERNAL TRIGGER CONTROL
TIMING CONTROL
INTERMESSAGE GAP TIMER
RESPONSE TIME TIMER
REPLY TIMEOUT TIMER
TRANSMITTER TIMEOUT TIMER
FRAME TIMER
BC/RT SEQUENCE CONTROL
CHANNEL SELECT
BUS A
BUS-25079 TRANSFORMER
BUS-64201 ERROR-GENERATING ENCODER
BUS-8559 VARIABLE LEVEL TRANSCEIVER
MUX
MESSAGE RAM
BUS B
BUS-25078 TRANSFORMER
SELF TEST
BUS-1555 ERROR-DETECTING DECODER
REAL-TIME MONITOR OUTPUT

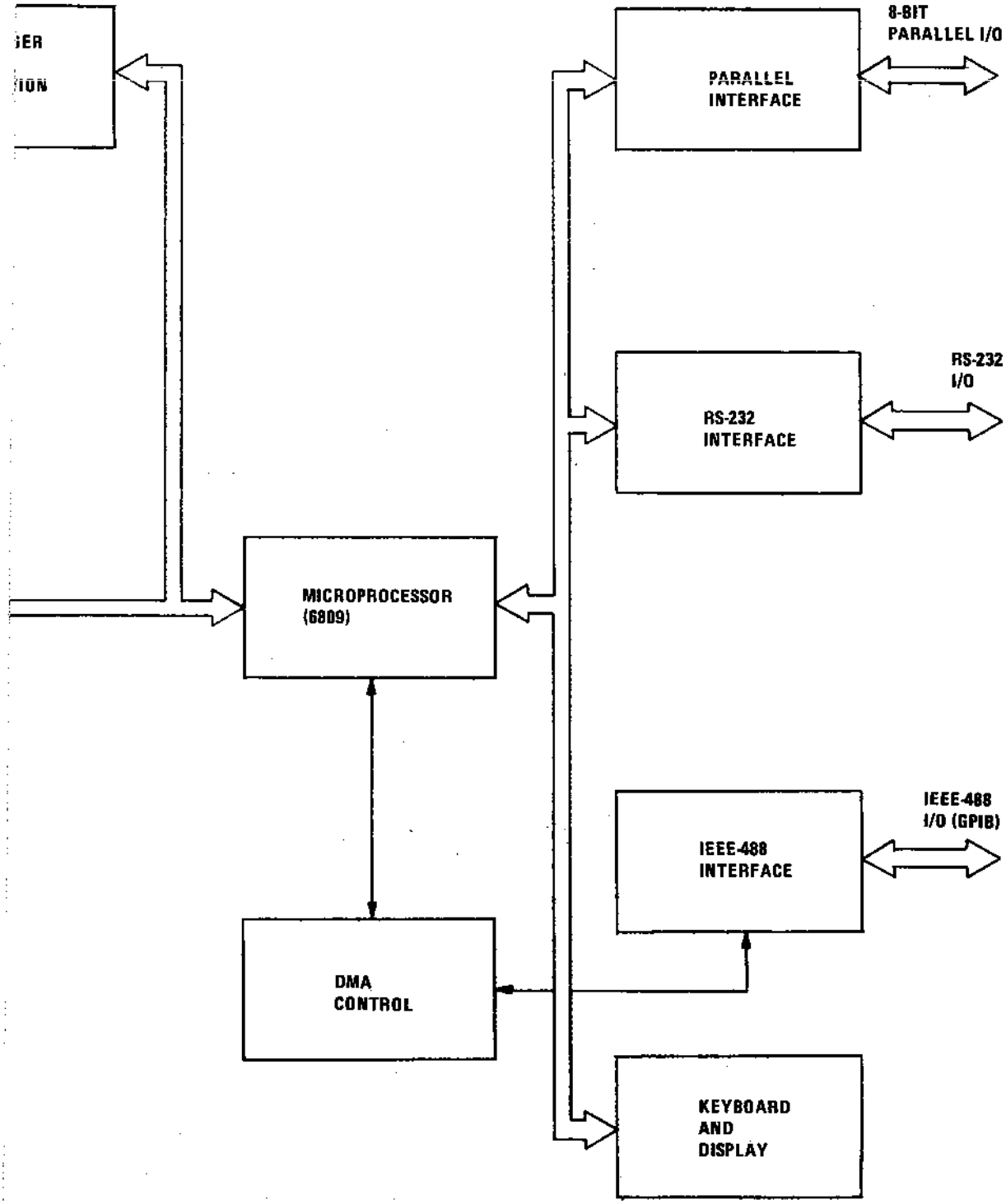
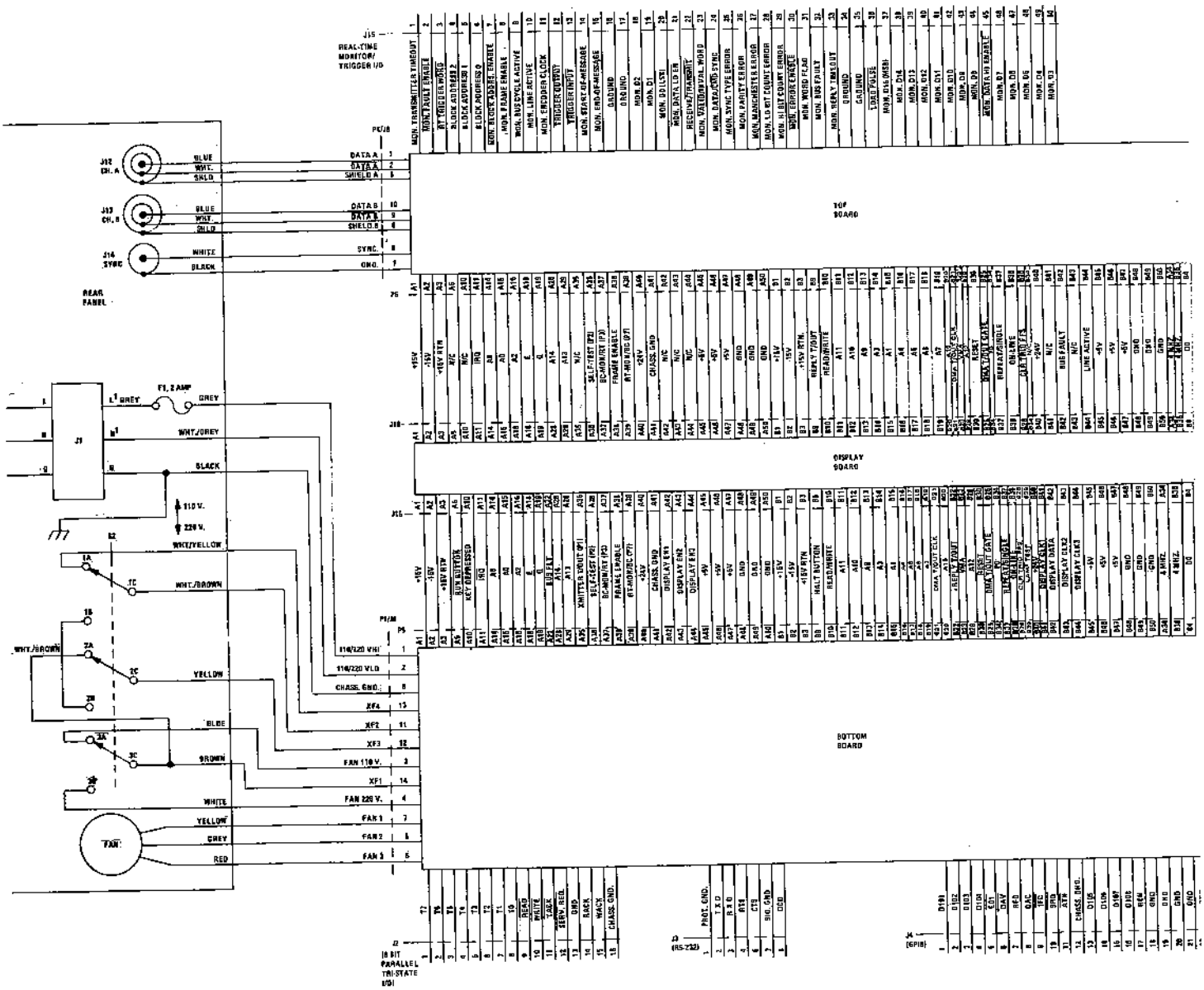


Figure 4-2. Block Diagram


REAL-TIME MONITOR/ TRIGGER I/O
REAR PANEL
TOP BOARD
DISPLAY BOARD
BOTTOM BOARD
FAN
8 BIT PARALLEL TRI-STATE I/O
(RS-232)
(GPIB)

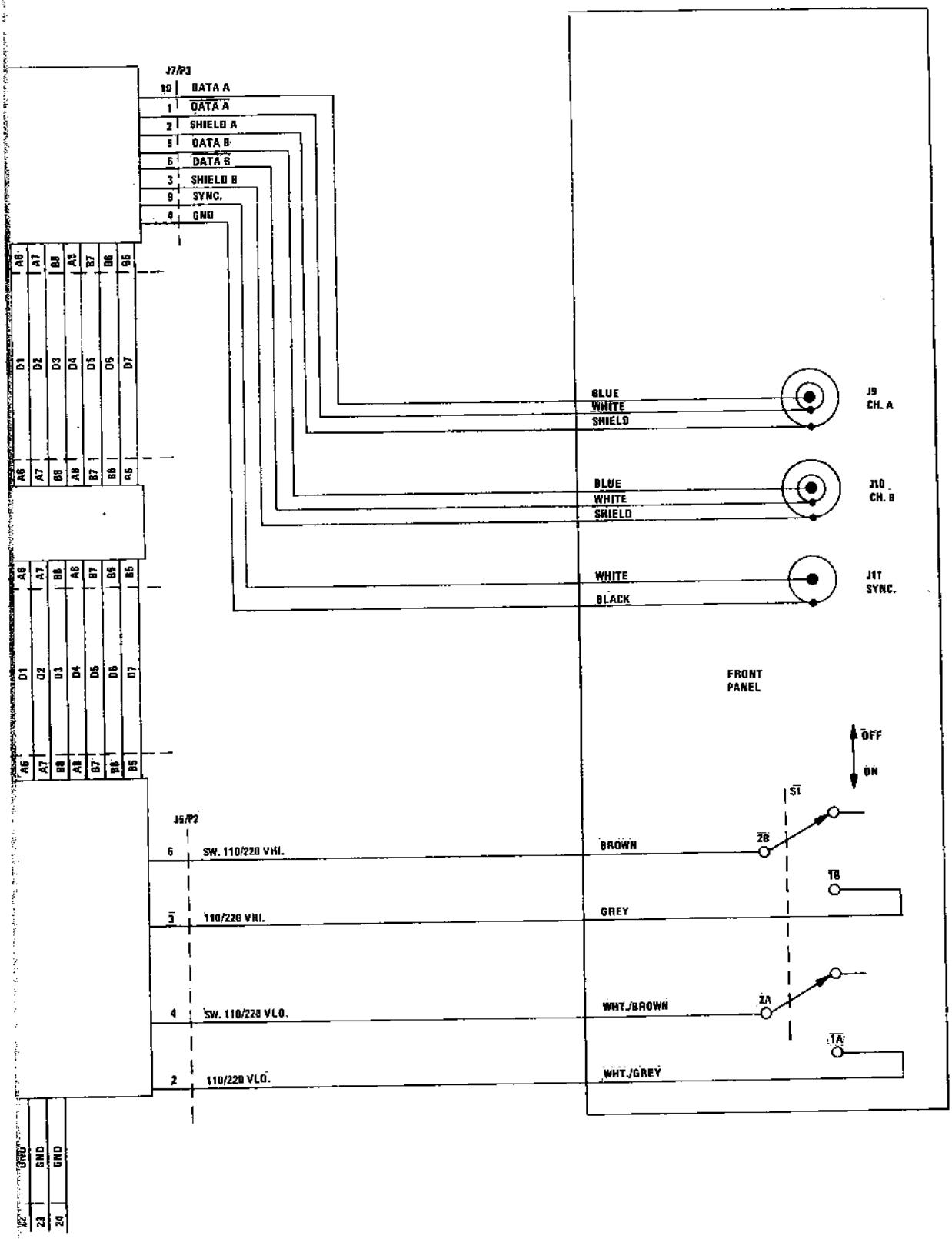


Figure 4-3. Overall Interconnection Diagram

4-25/4-26 blank

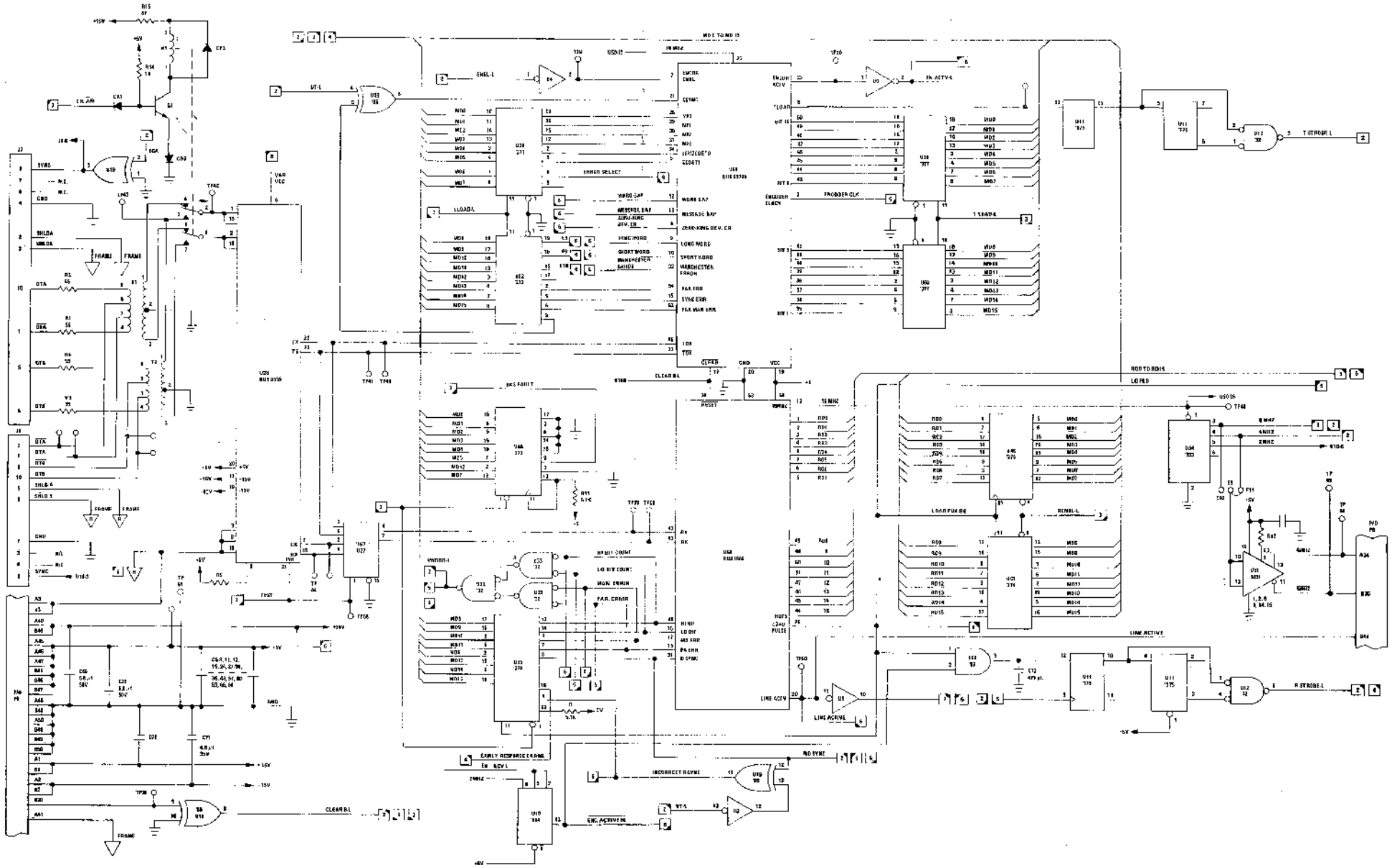


Figure 4-4. Top PCB Schematic Diagram (Sheet 1 of 6)

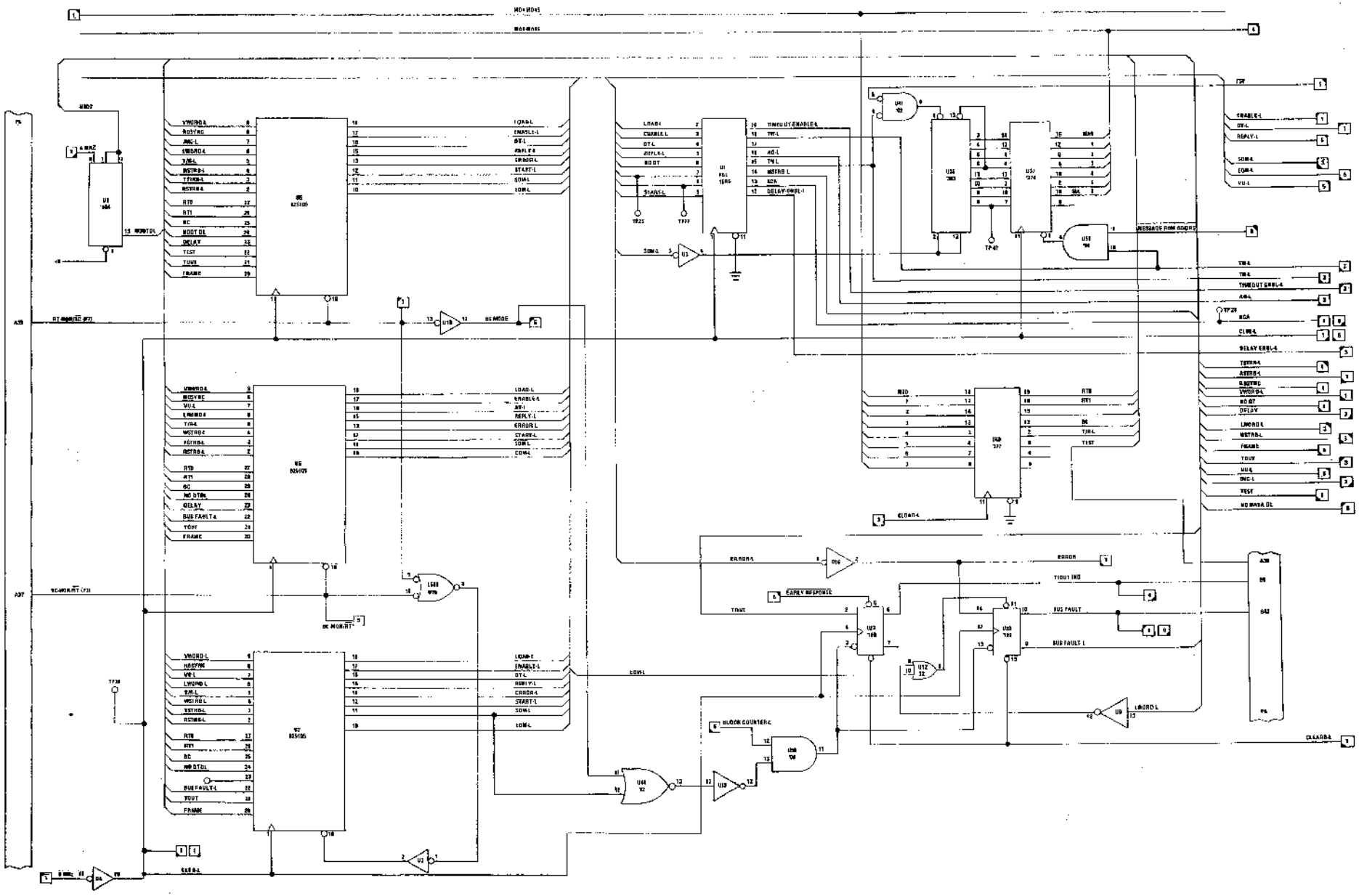
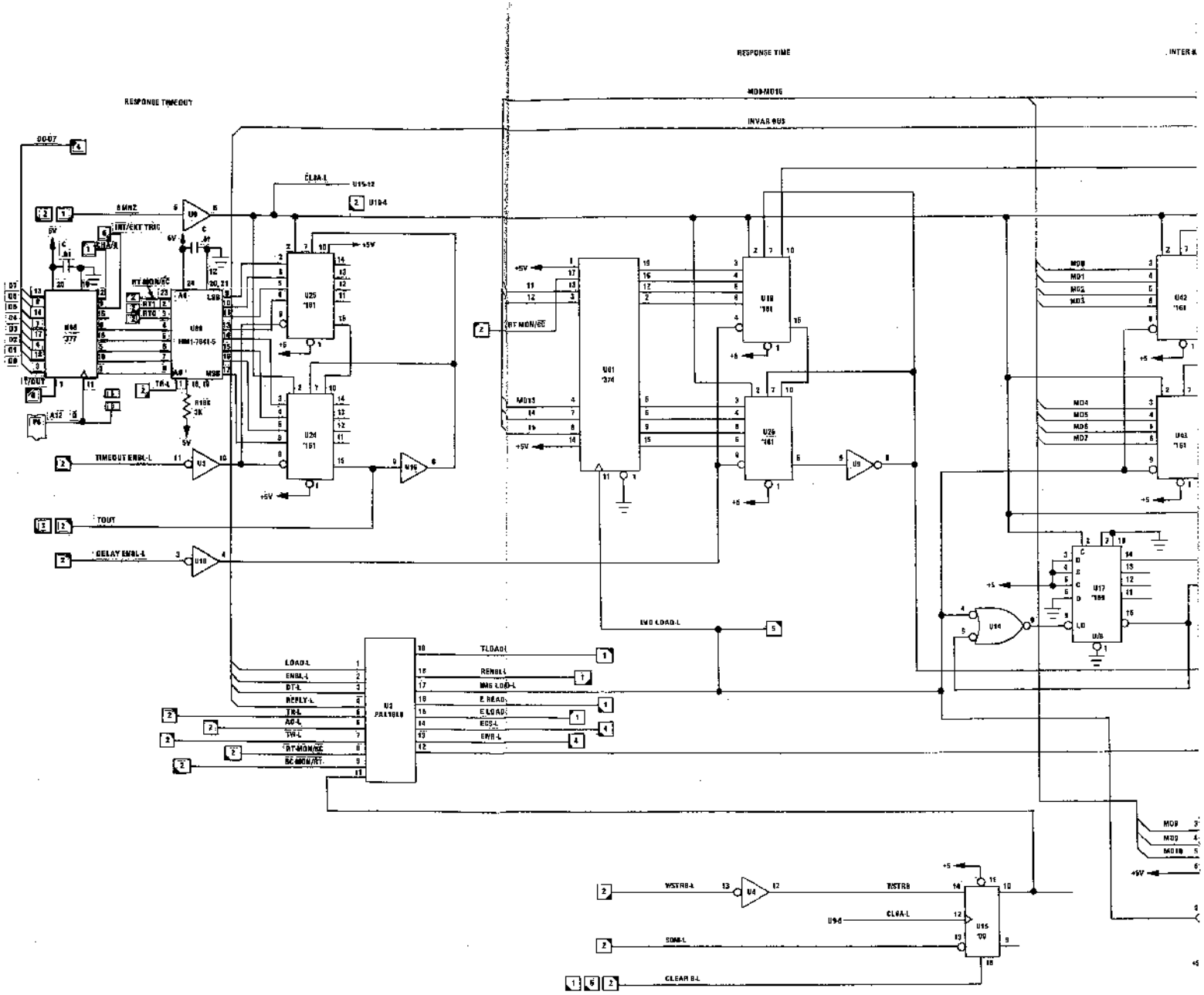


Figure 4-4. Top PCB Schematic Diagram (Sheet 2 of 6)


RESPONSE TIMEOUT
RESPONSE TIME
INTER M
MD0-MD15
INVAR BUS
D0-D7
8 MHZ
INT/EXT TRIG
CLRA-L
U15-12
U18-4
RT MON/BC
TIMEOUT ENBL-L
TOUT
DELAY ENBL-L
MD13
+5V
LOAD-L
ENBL-L
RT-L
REPLY-L
TR-L
A0-L
TW-L
RT-MON/BC
BC-MON/RT
T/O OUT
WSTRB-L
WSTRB
CLRA-L
SDMA-L
CLEAR B-L

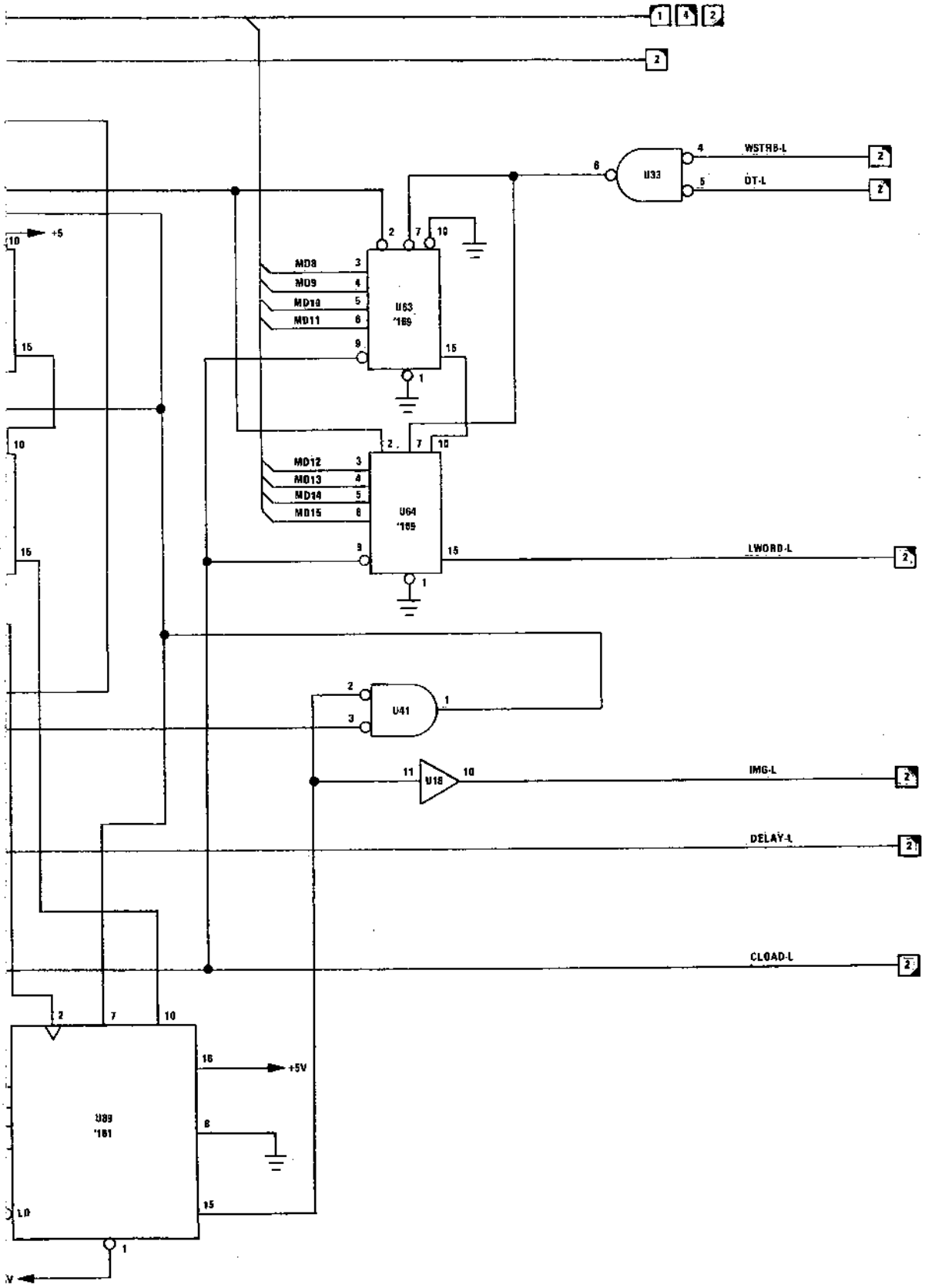


Figure 4-4. Top PCB Schematic Diagram (Sheet 3 of 6)

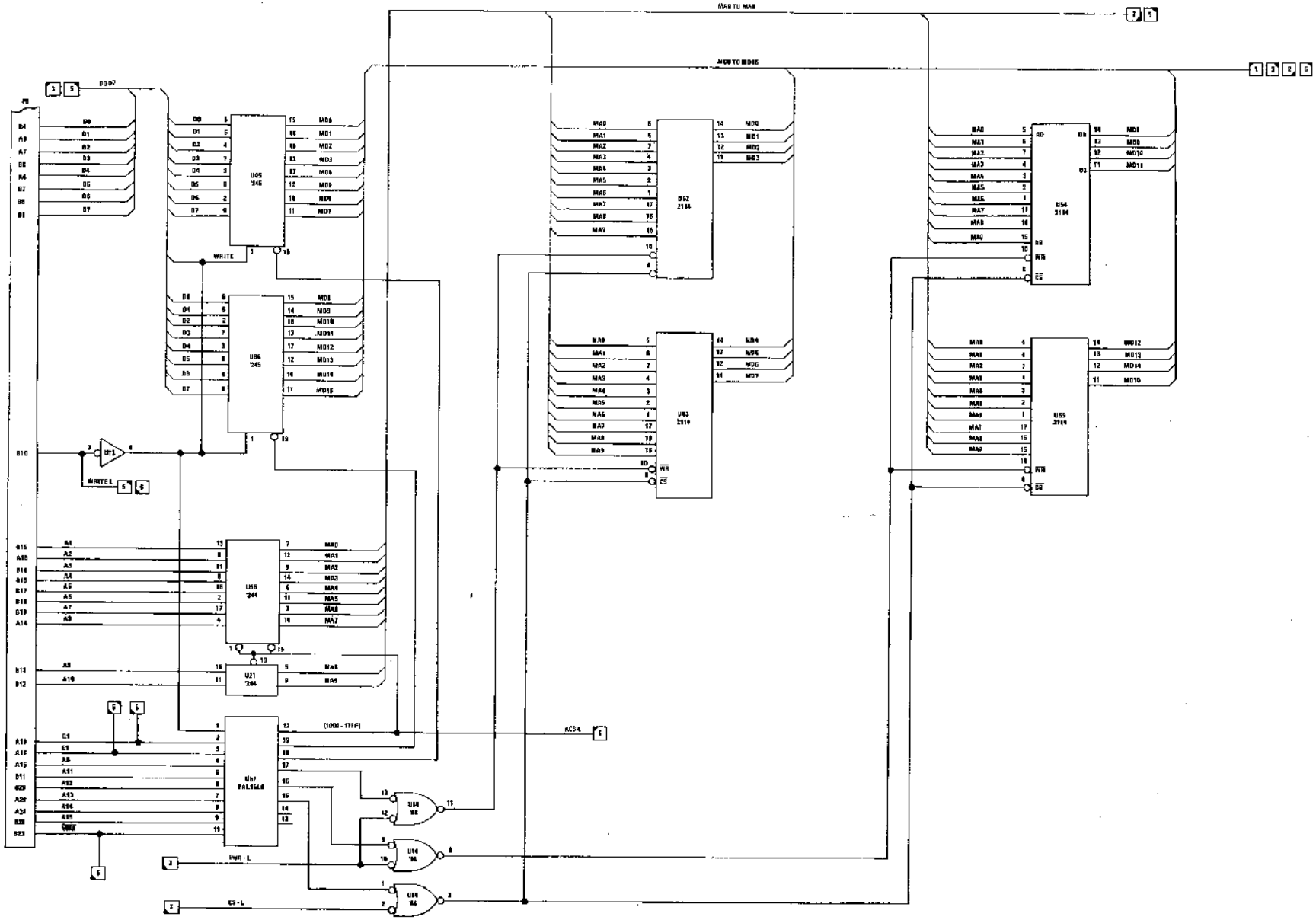


Figure 4-4. Top PCB Schematic Diagram
(Sheet 4 of 6)

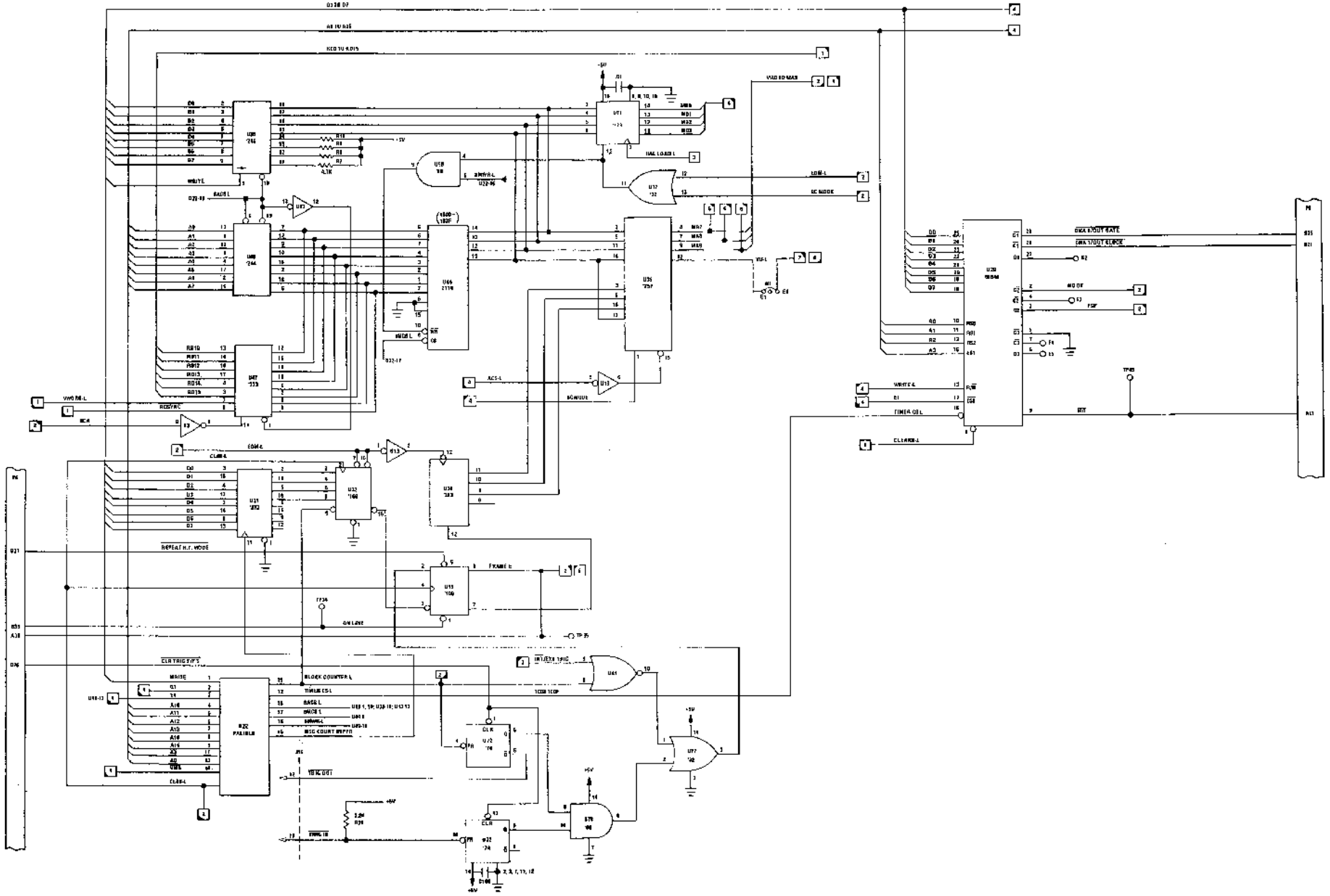


Figure 4-4. Top PCB Schematic Diagram
(Sheet 5 of 6)

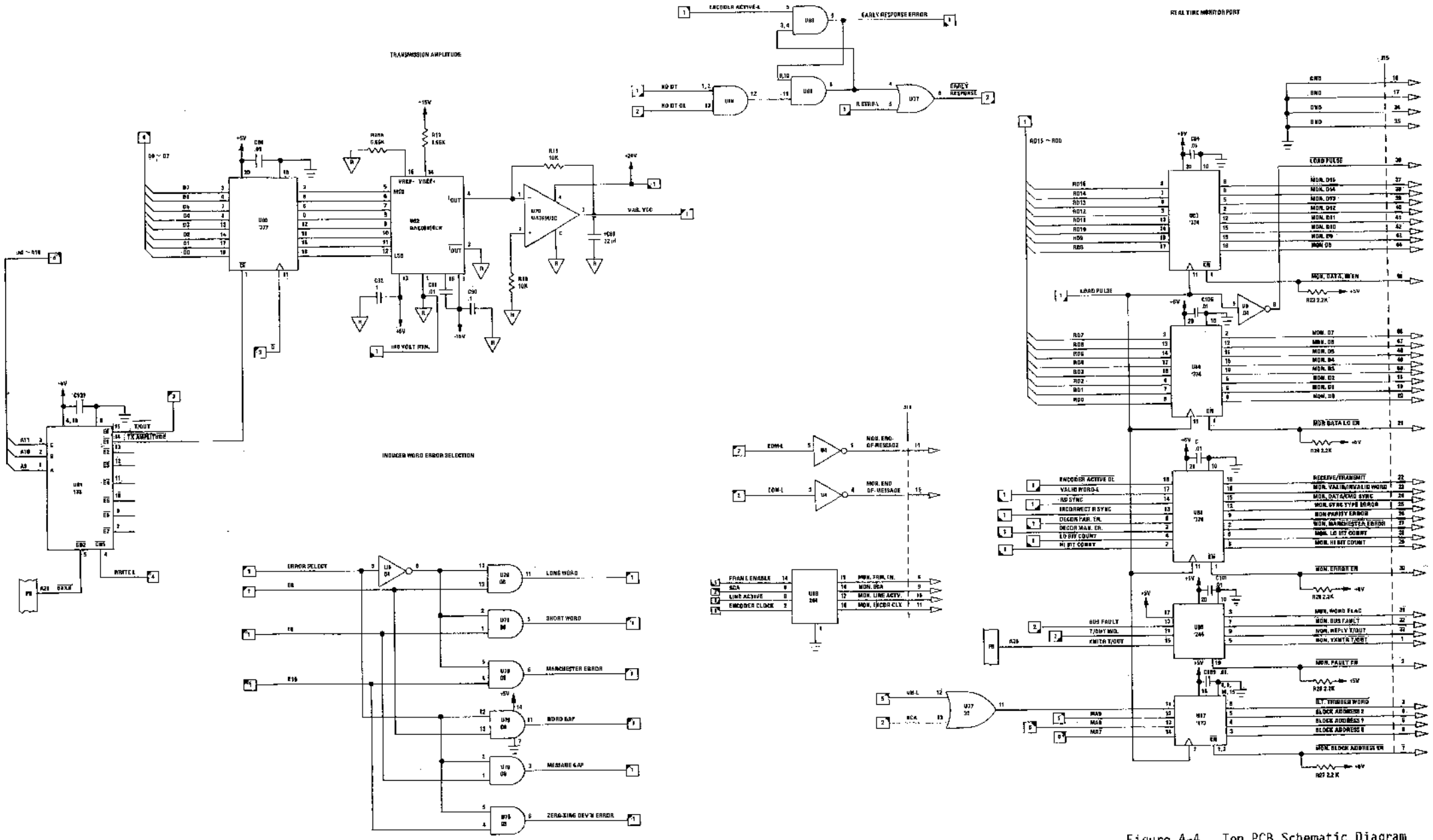


Figure 4-4. Top PCB Schematic Diagram (Sheet 6 of 6)

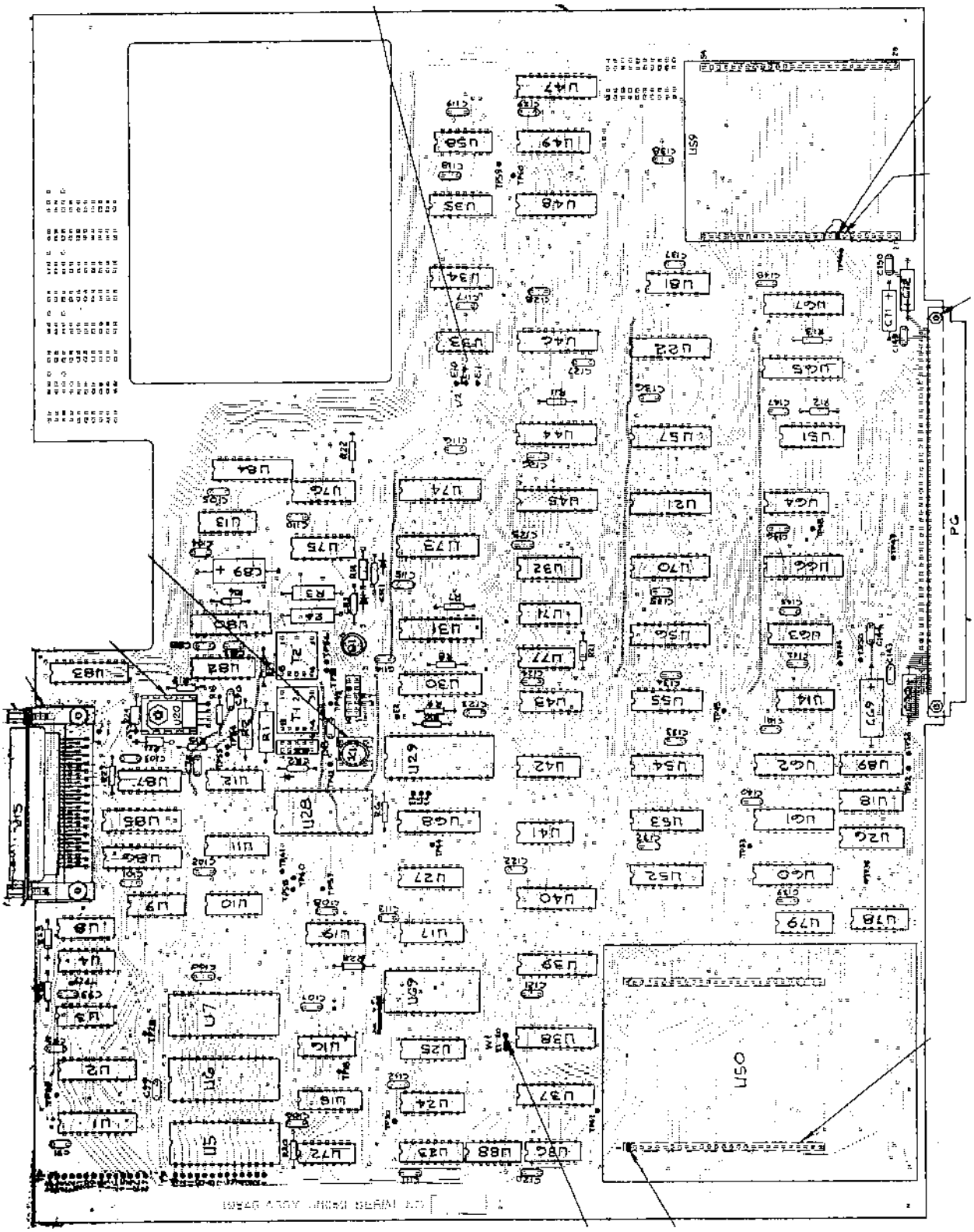


Figure 4-5. Top PCB Location Diagram

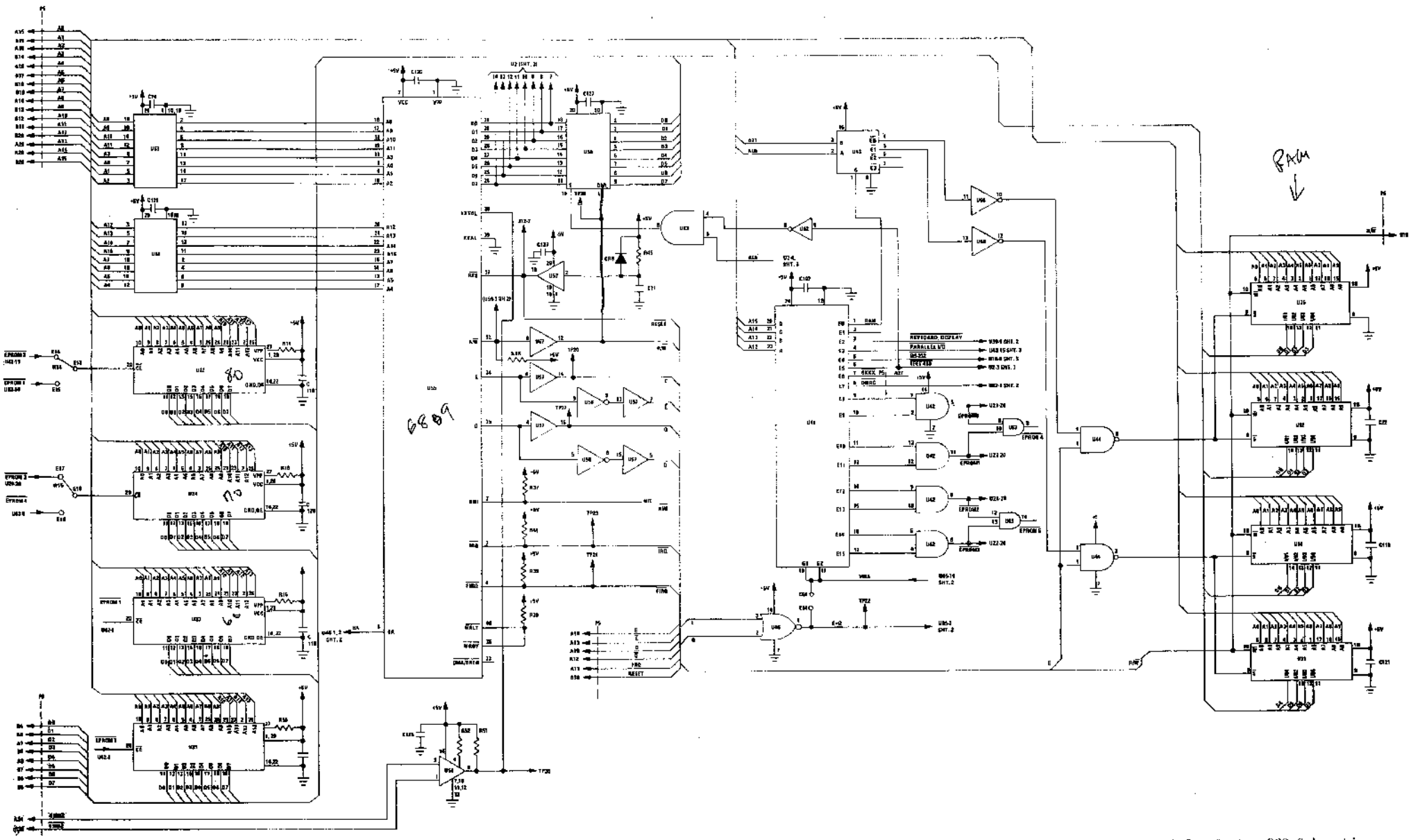


Figure 4-6. Bottom PCB Schematic Diagram (Sheet 1 of 4)

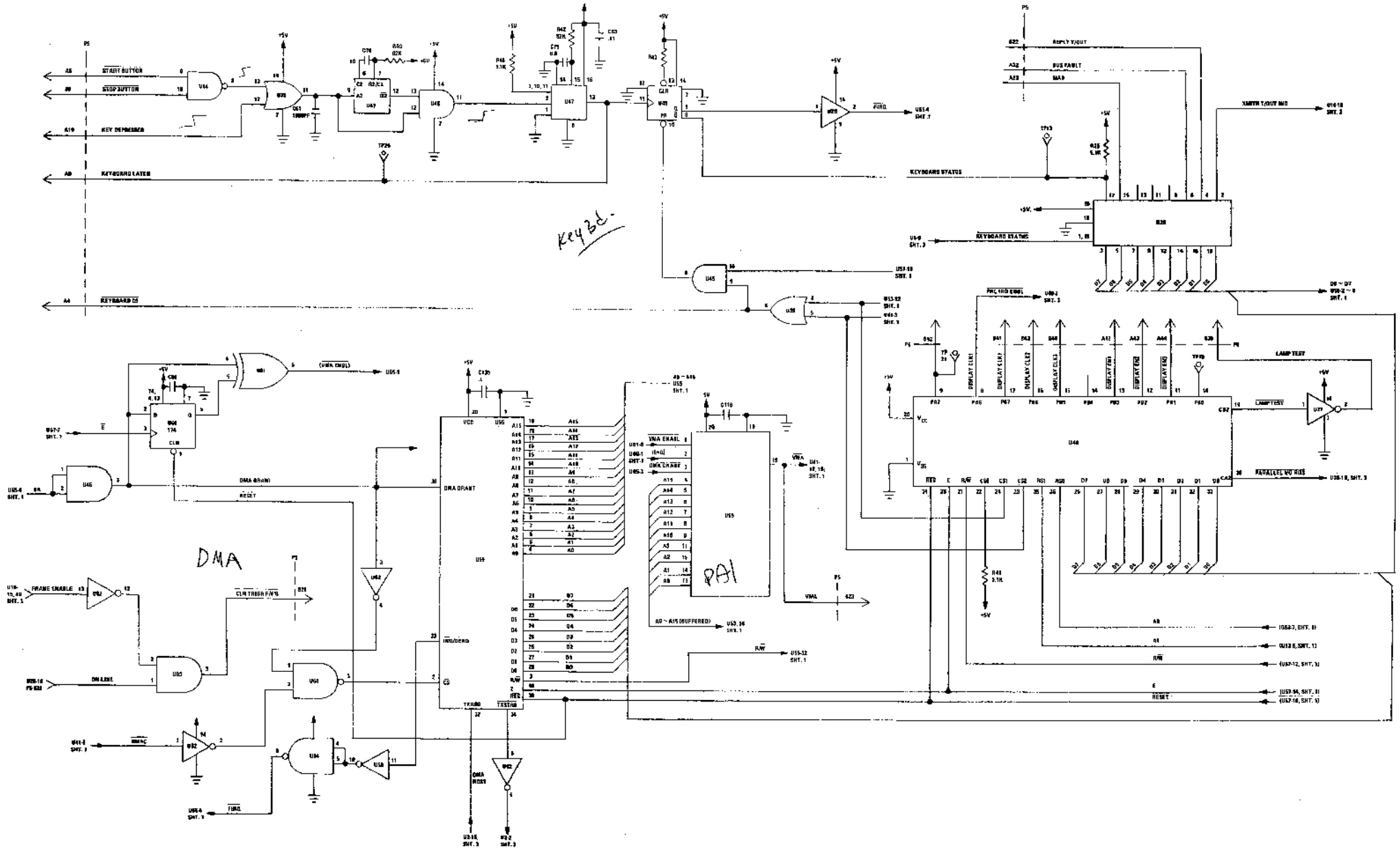


Figure 4-6. Bottom PCB Schematic Diagram (Sheet 2 of 4)

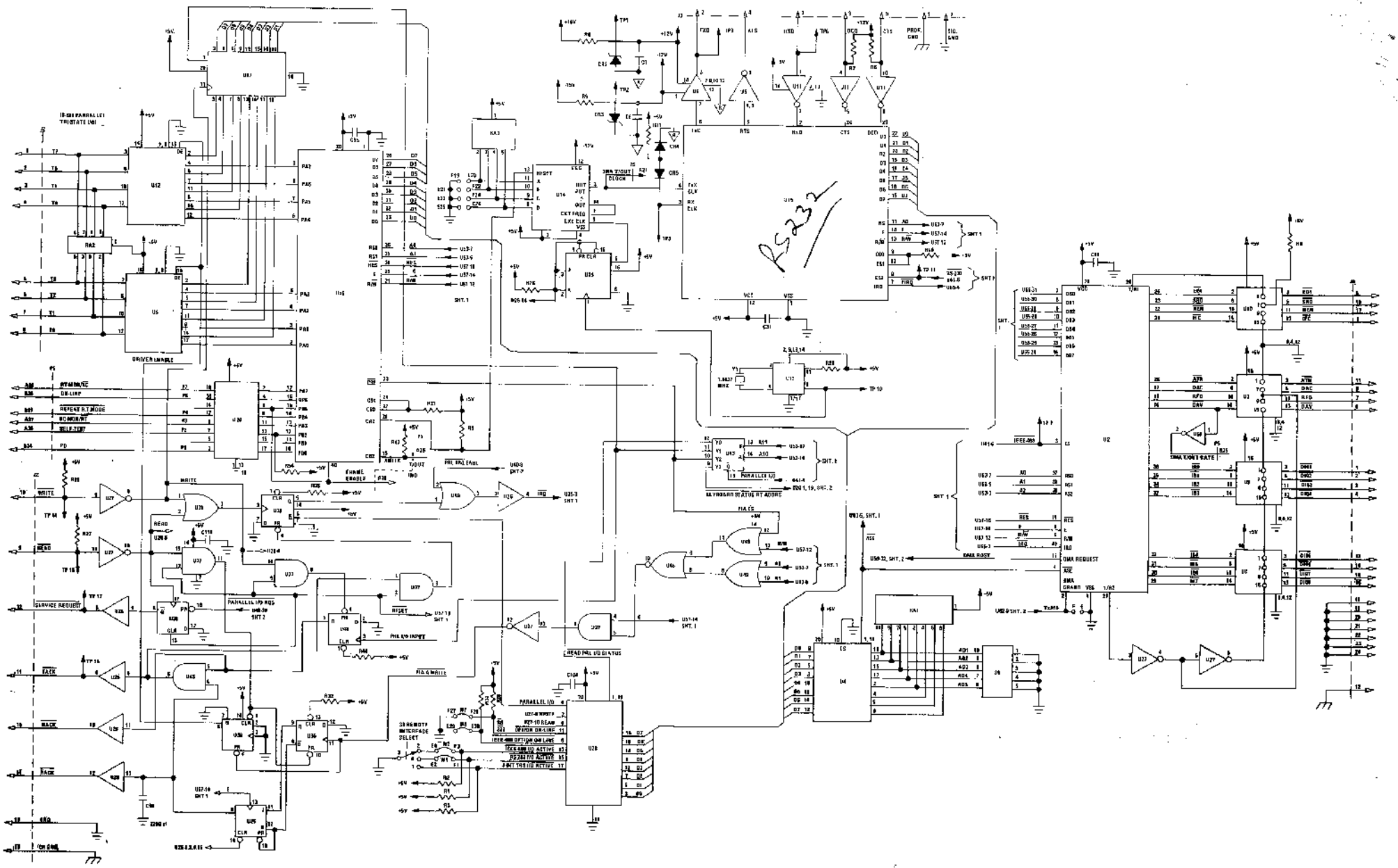


Figure 4-6. Bottom PCB Schematic Diagram (Sheet 3 of 4)

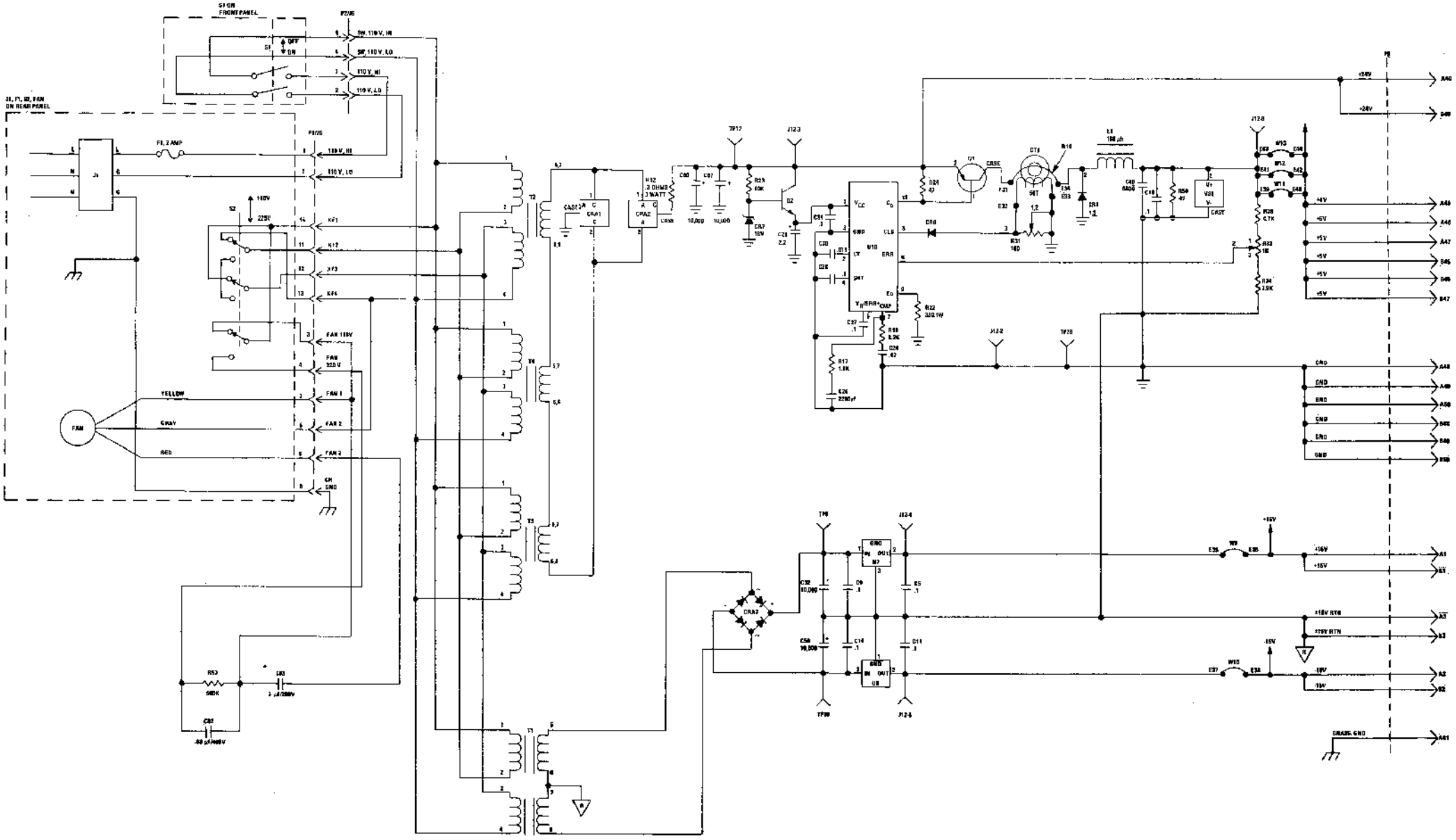


Figure 4-6. Bottom PCB Schematic Diagram (Sheet 4 of 4)

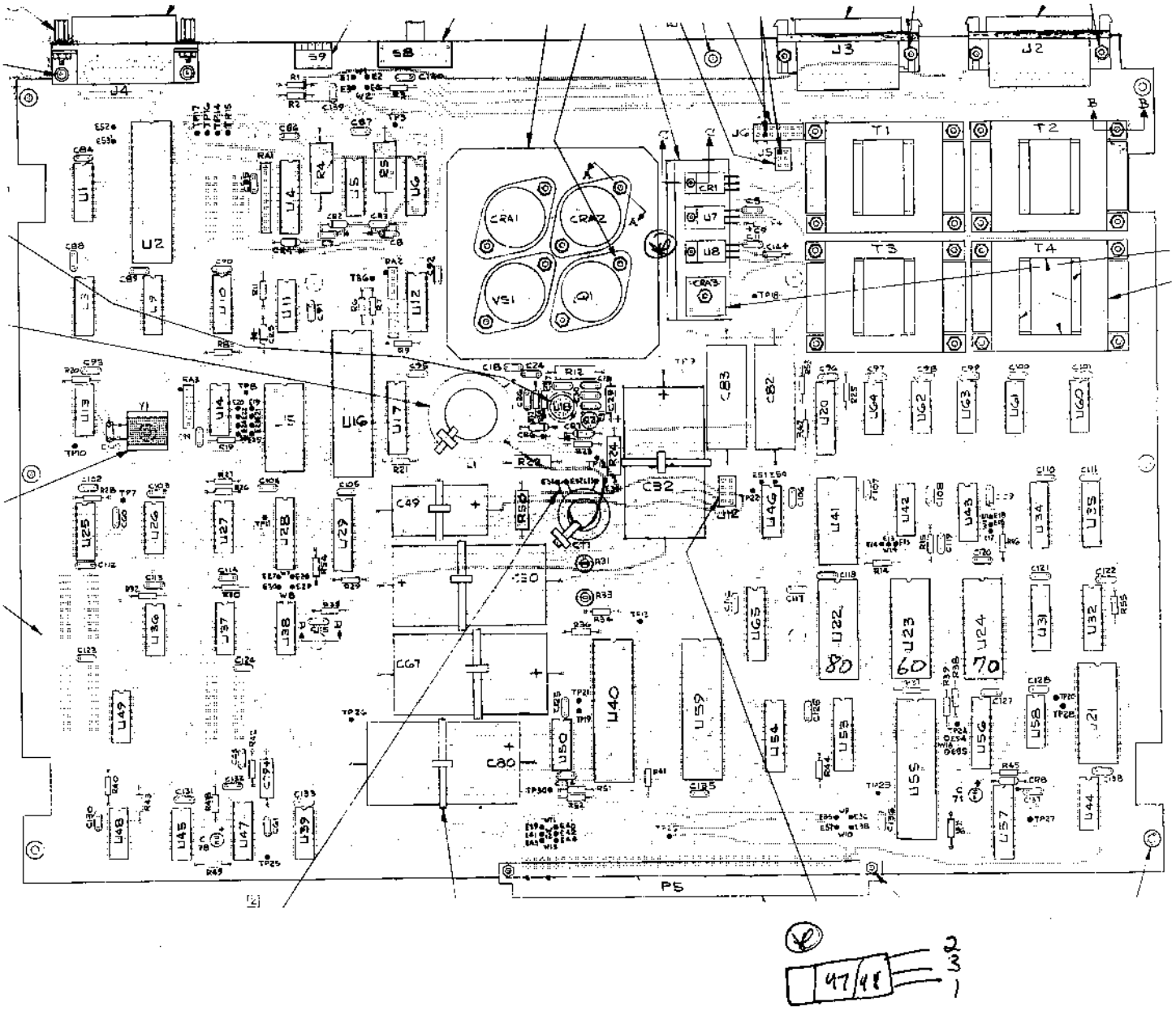


Figure 4-7. Bottom Board Parts Location Diagram

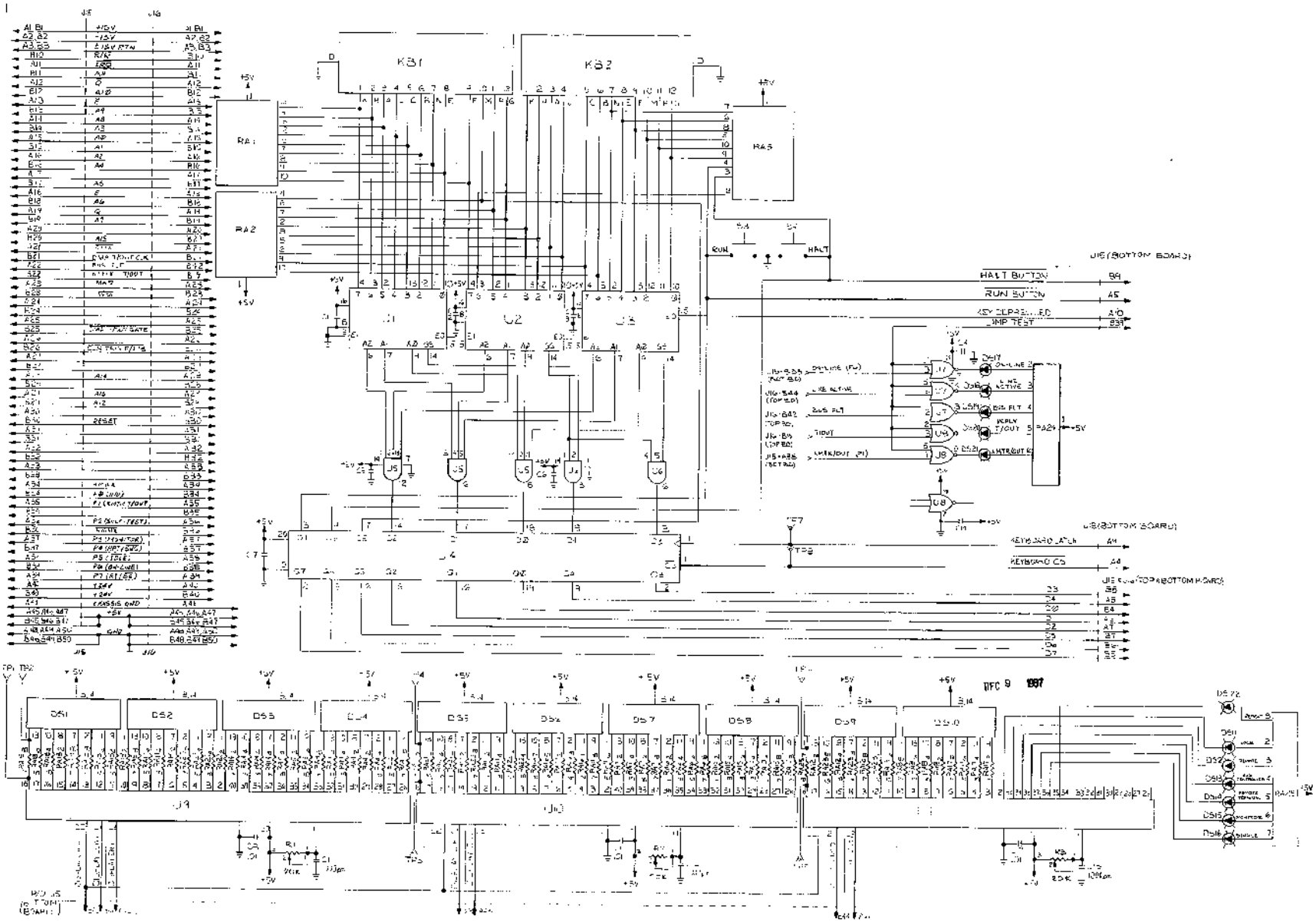
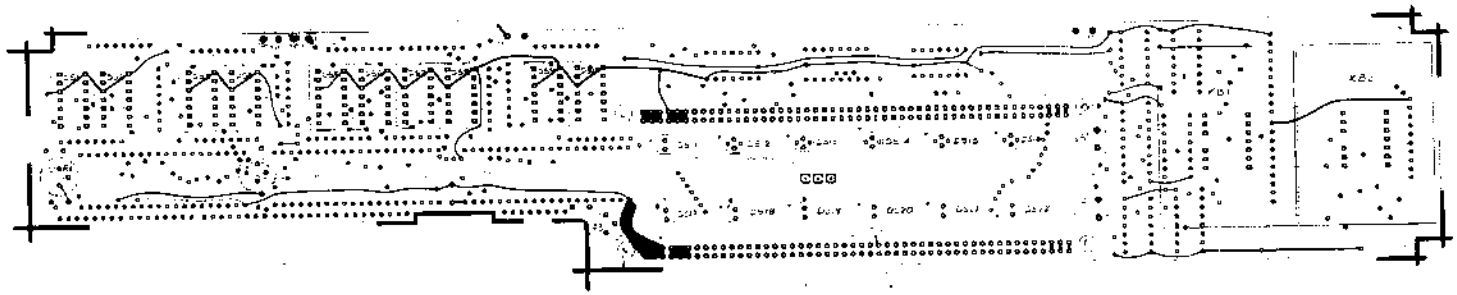
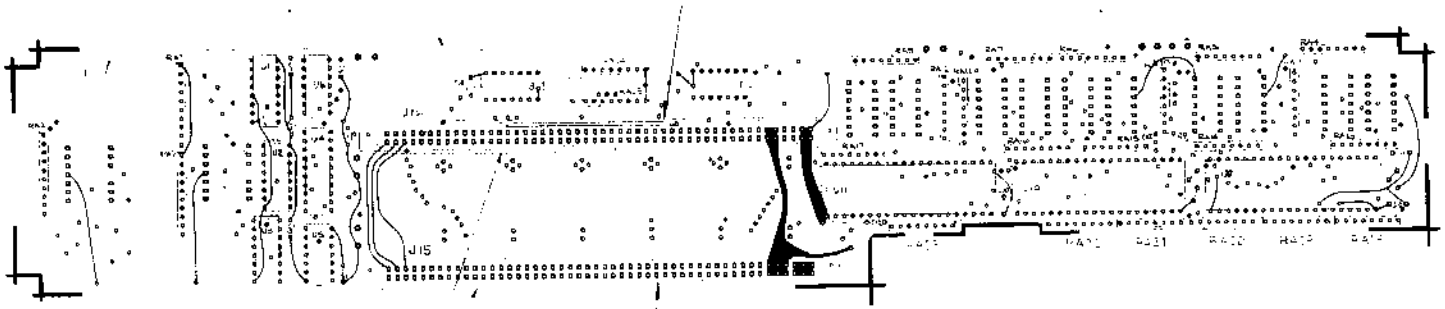


Figure 4-8. Display PCB Schematic Diagram



(a)



(b)

Figure 4-9. Display PCB Parts Location Diagram

SECTION 5

REPLACEABLE PARTS LIST

5.1 SCOPE

This section contains lists of most parts for the Model BUS-68005 MIL-STD-1553 Data Bus Exerciser.

For service involving the proprietary section of the top printed circuit board assembly, (parts not listed), please contact your ILC Field Representative or our Customer Service Department at:

ILC Data Device Corp.
105 Wilbur Place
Bohemia, NY 11716
(516) 567-5600

BUS-68005 ... TOP BD ASSY

REFERENCE DESIGNATION	QTY	DESCRIPTION	MFG PART NO.	MFG
00001	1	PRINTED WIRING BD MULTILAYER	5199-3804-90XX	DDC
C90-91,100,103,105-106,109,113,116,119-120,122-123,125,128-129,132,134,136,138-139,142,146,148	24	CAP,CER .01UF,100V,10% LEV M CKR05BX	1104-8475-0103	ANY
C89	1	CAP,TANT 22UF,50V,10%,LEV M (CSR13)	1703-2395-0226	ANY
C69	1	CAP,TANT 6.8UF,50V,10%,LEV M	1707-3395-0685	ANY
C70-72	3	CAP,TANT 6.8UF,35V,10%,LEV M (CSR13)	1703-2295-0685	ANY
C73	1	CAP,CER 470PF,50V,20%	1113-0396-0471	VITRMON
C82	1	CAP,CER .1UF,50V,10%,X7R	1113-0395-0104	VITRMON
CR1-3	3	DIODE SILICON DHD	3000-0020-0040	ANY
Q1	1	TRNSTR,NPN,TO 18	3120-2000-0060	ANY
R18	1	RES C.C. 10K,1/4W,5%	2401-2204-0103	ANY
R1-4	4	RMF 54.9,1W,1%	2601-7431-5499	MEPCO
R6-13	8	RES C.C. 5.1K,1/4W,5%	2401-2204-0512	ANY
R14,21-22	3	RES C.C. 1K,1/4W,5%	2401-2204-0102	ANY
R15	1	RES C.C. 47,1/4W,5%	2401-2204-0470	A B
R16B	1	RES C.C. 3K,1/4W,5%	2401-2204-0302	ANY
R23-27	5	RES C.C. 2.2K,1/4W,5%	2401-2204-0222	A B
R20	1	RES C.C. 2.7K,1/4W,5%	2401-2204-0272	ANY
R17,R16A	2	RMF 6.65K,1/8W,1%,100PPM (RN55D6651F)	2500-1131-6651	PRINT SZ A
R19	1	RMF 8.87K,1/8W,1%,100PPM (RN55D8871F)	2500-1131-8871	PRINT SZ A

REFERENCE DESIGNATION	QTY	DESCRIPTION	MFG PART NO.	MFG
U49,52-55	5	1K X 4 STATIC RAM 120 NS	4362-1048-0001	INTEL
U49,52-55	ALT	1K X 4 STATIC RAM 120 NS	4362-1048-0002	SINERTEK
U49,52-55	ALT	1K X 4 STATIC RAM 120 NS	4362-1048-0003	SLD ST SCI
U3-4,9,13,16	5	HEX INVERTER LO.PWR.SCHOT	4322-1148-0000	ANY
U15,23	2	DUAL J-K FLIP FLOP TTL	4322-1386-0000	ANY
U18,24-26,42-43,89	7	BINARY COUNTER	4322-1345-0000	ANY
U5	1	LOGIC SEQUENCER SPECIFICATION	4643-1002-0020	PRINT
U20	1	POWER OP AMP,4-PIN POWER WATT PKG	4119-1830-0001	FSC
U17,32,63-64	4	SYNC 4 BIT UP DOWN CTR	4322-1403-0000	ANY
U27	1	QUAD 2-LINE TO 1-LINE MUX LPS	4322-1189-0000	ANY
U2	1	OCTAL 16 INPUT SPECIFICATION	4622-1001-0020	PRINT SZ A
U28	1	BUS 68005 TOP BD HEATSINK ASSY	6003-8055-0000	PRINT SZ A
U29	1	PROGRAMMABLE TIMER MODULE	4362-1047-0001	MOTOROLA
U30,45,66	3	OCTAL BUS TRANSCEIVER	4322-1258-0000	ANY
U8,10	2	8 BIT PAR-OUT SER SHIFT RE	4322-1223-0000	ANY
U31,44,47	3	LATCH,TANS,8-BIT,LPS	4322-1278-0000	ANY
U21,48,56,70,86	5	OCTAL BUS DRIVER, LPS	4322-1241-0000	ANY
U35	1	QUAD 2 TO 1 LINE MUX TTL	4322-1296-0000	ANY
U37,46,61,65,67,83-85	8	OCTAL LATCH LPS	4322-1251-0000	ANY
U1	1	PROM SPECIFICATION	4622-1002-0010	PRINT SZ A
U11	1	QUAD D-TYPE F/F W/CLR,LPS	4322-1163-0000	ANY
U34,36	2	DIB,IC,TTL,PLASTIC DIP 0-70 DEG.	4322-1358-0000	ANY
U51	1	DUAL DIFF,TRI-STATE LINE DRIVER,TTL	4322-1336-0001	NSC
U14,58,78-79	4	QUAD 2IN POS-AND GATES	4322-1220-0000	ANY
U59	1	1553 MANCHESTER DECODER 6 00267520000	BUS1555	PRINT SZ C
U12,33,77	3	QUAD 2IN POS-OR GATES	4322-1226-0000	ANY
U19	1	QUAD 2-INPUT EXCLUSIVE OR GATE LPS	4322-1188-0000	ANY
U41	1	QUAD 2IN POS NOR GATE LPS	4322-1161-0000	ANY
U6	1	LOGIC SEQUENCER SPECIFICATION	4643-1002-0030	PRINT
U22	1	PROM SPECIFICATION	4622-1001-0070	DDC SPEC
U57	1	PROM SPECIFICATION	4622-1001-0060	DDC SPEC
U69	1	PROM SPEC	4643-1001-0030	DDC SPEC
U71,87	2	QUAD D FLIP FLOP	4322-1437-0000	ANY
U72	1	DUAL D FLIP FLOP	4322-1152-0000	ANY
U81	1	3TO8-LINE DECODER/MUX LPS	4322-1250-0000	ANY
U82	1	8 BIT DIG TO ANALOG	4392-1050-0001	NSC
U50	1	1553 ENCODER	BUS64201	PRINT SZ D
U38-40,60,62,68,73-74,80	9	OCTAL D F/F W/ENABLE,LPS	4322-1246-0000	ANY
U88	1	3 INPUT NAND GATE LPS	4323-1209-0000	ANY
T1-2	2	PULSE TRANSFORMER	BUS25679	DDC

REFERENCE DESIGNATION	QTY	DESCRIPTION	MFG PART NO.	MFG
XK1	1	SOCKET STRIP 20 PIN GLD/TIN CONTCT	5315-3300-0001	SAM TEC
J7-8	2	CONNECTOR,VERTICAL CARD,10-PIN,2 ROWS	5312-3000-0000	BERG
P6	1	CONNECTOR,MALE	5315-0100-0001	WINCHESTER
00123	4	CONN,PC BD.,FEMALE,27-PIN SINGLE ROW	5312-6200-0000	BERG
00127	4	POLARIZING PLUG	5303-5000-0000	BERG
XU3-4,8-10,12-14,16, 19,33-34,36,41,58,72, 77-79,88	20	SOCKET 14 PIN GOLD PLATED	5315-1900-0001	CIR ASSY
XU11,15,17-18,23-27, 32,35,42-43,51,63-64, 71,75-76,81,87,89	22	SOCKET 16 PIN GOLD PLATED	5315-2000-0001	CIR ASSY
XU49,52-55	5	SOCKET 18 PIN GOLD PLATED	5315-3200-0001	CIRC ASSY
XU1-2,21-22,30-31,37-40,44-48,56-57,60-62, 65-68	24	SOCKET 20 PIN GOLD PLATED	5315-3000-0001	CIRC ASSY
XU69	1	SOCKET 24 PIN GOLD PLATED	5315-2100-0001	CIRC ASSY
XU70,73-74,80,83-86	8	SOCKET 20 PIN GOLD PLATED	5315-3000-0001	CIRC ASSY
XU28	1	SOCKET 24 PIN GOLD PLATED	5315-2100-0001	CIRC ASSY
XU5-7,29	4	SOCKET 28 PIN GOLD PLATED	5315-2200-0001	CIRC ASSY
K1	1	RELAY TO-5,12V	5700-0003-5002	TELEDYNE
00148	1	CONN,FEMALE SCREW LOCK	5306-6400-0000	AMP
J15	1	CONN,PLUG 50 PIN CONTACT	5306-9800-0000	AMP
00150	1	HEATSINK	5400-0003-4001	AAVID
W1-2	2	SHORTING PLUG INSULATED	5314-2400-0001	CAMBION
00163	2	INSULATOR	5502-1463-00XX	PRINT

BUS-68005 ... BOT BD ASSY

00001	1	PRINTED WIRING BD MULTILAYER	5199-3805-30XX	PRINT SZ E
C63,89,101,104,107, 110,114,118-122,125-127,137	16	CAP,CER .01UF,50V,10%,X7R	1113-0395-0103	VITRMON
C5,7-8,11,18,27-28,31, 36,116,135	11	CAP,CER .1UF,50V,10%,X7R	1113-0395-0104	VITRMON
C9,14	2	CAP TANT 1.0UF,20PCT 35V	1706-1396-0105	COMP
C24	1	CAP,CER .47UF,50V,10%,X7R	1113-1395-0474	VITRMON
C26,60	2	CAP,CER 2200PF,100V,10%,X7R	1113-0495-0222	VITRMON
C29	1	CAP,AL ELEC,2.2UF,63V -10 + 50%,AXIAL	1713-5999-0225	SPRAGUE
C29	ALT	CAP,AL ELEC 2.2UF,50V,20%,AXIAL	1715-6396-0225	NIC
C30	1	CAP,CER.,.015UF,50V,10%,X7R	1113-0395-0153	VITRMON
C32,50,67,80	4	CAP,AL 10,000 UF,35V,20%	1714-5396-0109	NICHICON
C49	1	CAP,AL ELEC 6800UF,10V,20%	1714-5096-0688	NICHICON
C61	1	CAP,CER 1000PF,100V,10%,X7R	1113-0495-0102	VITRMON
C136	1	CAP,CER 1,0UF,50V,10%,X7R	1115-2395-0105	VITRMON

REFERENCE DESIGNATION	QTY	DESCRIPTION	MFG PART NO.	MFG
T1	1	TRANSFORMER,POWER	5210-0063-0001	SIGNAL
T2-4	3	TRANSFORMER 115/230V	5210-0066-0001	SIGAL
U1,3,9-10	4	IEEE BUS DRIVER	4322-1214-0000	MOT
U2	1	GEN PURPOSE INTERFACE ADA PTER GPIA	4362-1052-0001	MOT
U4,20,28-29,53-54,57	7	OCTAL BUS DRIVER, LPS	4322-1241-0000	ANY
U5,12	2	4 BIT BI-DIRECTIONAL TRI STATE BUFFER	4322-1406-0001	NSC
U6	1	LINE DRIVER	4192-1300-0001	NSC
U7	1	VOLTAGE REGULATOR, +15V,1.5A,TO-220	4149-3640-0001	NSC
U8	1	VOLTAGE REGULATOR, -15V,1.5A,TO-220	4149-3650-0001	NSC
U11	1	LINE RECEIVER	4192-1310-0001	NSC
U13	1	OSCILLATOR,VOLTAGE CONTROLLED	4322-1408-0001	TI
U14	1	BAUD RATE GENERATOR	4362-1046-0001	NSC
U15	1	ASYN COMM INTERFACE ADAPTER 2MHZ	4362-1055-0001	MOT
U16,40	2	P.I.A.	4362-1050-0001	MOT
U17	1	OCTAL LATCH LPS	4322-1251-0000	ANY
U18	1	SWITCHING REGULATOR TO-96	4149-3680-0001	LAMBDA
U22	1	PROM SPECIFICATION	4663-1002-0060	PRINT SZ A
U25	1	DUAL J-K FLIP FLOP	4322-1222-0000	ANY
U26	1	HEX BUFFER OC HIGH VOLT	4323-1043-0000	ANY
U27,58,62	3	HEX INVERTER LO PWR SCHOT	4322-1148-0000	ANY
U31-32,34-35	4	1K X 4 STATIC RAM LOW PWR MOS	4362-1041-0001	INTEL
U36,38,48,60	4	DUAL D FLIP FLOP	4322-1152-0000	ANY
U37,42,45,63	4	QUAD 2IN POS-AND GATES	4322-1220-0000	ANY
U39,49	2	QUAD 2IN POS-OR GATES	4322-1226-0000	ANY
U41	1	4-LINE TO 16-LINE DECODER	4322-1240-0000	ANY
U43	1	DUAL 2-LINE TO 4-LINE DECODER/DEMUX	4322-1305-0000	ANY
U44	1	QUAD 2IN POS-NAND GATES	4322-1150-0000	ANY
U46	1	QUAD 2IN POS-NOR GATE LPS	4322-1161-0000	ANY
U47	1	DUAL MONOSTABLE LO PWR SC	4322-1156-0000	ANY
U50	1	DUAL LINE RECEIVER,TTL	4322-1337-0001	NSC
U55	1	MICROPROCESSOR	4362-1049-0001	MOT
U56	1	OCTAL BUS TRANSCEIVER	4322-1258-0000	ANY
U59	1	DIRECT MEMORY CONTROLLER	4362-1056-0001	MOT
U61	1	QUAD 2-INPUT EXCLUSIVE OR GATE LPS	4322-1188-0000	ANY
U64	1	QUAD 2-INPUT NAND GATE OPEN COLLECTOR	4322-1438-0000	ANY
U24	1	PROM SPECIFICATION	4663-1002-0070	DDC
U23	1	PROM SPECIFICATION	4663-1002-0080	DDC
00110	1	CONNECTOR HARDWARE	5490-0003-1301	AMP
J5	1	6 POSITION VERTICAL CARD CONN (FEMALE)	5314-9600-0001	BERG
J6	1	DUAL STRAIGHT HEADER,36 POSITION	5312-3400-0000	BERG
00113	1	POLARIZING PLUG	5303-5000-0000	BERG

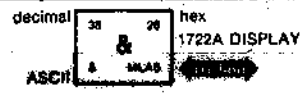
REFERENCE DESIGNATION	QTY	DESCRIPTION	MFG PART NO.	MFG
S9	1	DIP SWITCH 5,POSITION	5700-0003-0600	GRAYHILL
S8	1	SWITCH MINIATURE SLIDE SP3T	5700-0003-3901	ALCO
00116	1	CLIP	5500-0053-0000	AUGAT
VS1	1	OVER VOLTAGE PROTECTOR 6.6V 6 AMP	3099-0020-0001	LAMBDA
Y1	1	CRYSTAL 1.8432 MHZ	5500-0475-0001	VAL FISHER
J3	1	CONNECTOR,FEMALE	5315-0000-0001	TRW
J2	1	CONNECTOR, DB25 MALE	5315-0400-0001	TRW
J4	1	CONN,24-PIN,FEMALE,PC BD MOUNT	5312-9200-0000	AMP
W1-2,7-14	10	SHORTING PLUG INSULATED	5314-2400-0001	CAMBION
U65	1	PROM SPECIFICATION	4622-1001-0100	DDC SPEC
00126	4	TRANSFORMER CLAMP	5500-0136-0000	SIGNAL
00127	1	HEATSINK QUAD 3-PIN TO-3	5400-0004-1001	IERC
00128	4	INSULATOR,THERMALLY COND TO-3	5500-8710-0000	BERQUIST
00129	3	INSULATOR,THERMALLY COND TO-220	5500-0294-0000	BERQUIST
00130	8	INSULATOR SHOULDER	5500-3500-0000	NYLON
00131	1	HEATSINK	5983-3774-0000	PRINT SZ C
00132	4	SCREW,NYLON,NO. 4 X 1/2	5460-0001-9000	H,H,SM
00133	1	HEAT SINK	5900-0020-0000	IERC
P5	1	CONNECTOR,MALE	5315-0100-0001	WINCHESTER
J12	1	DUAL STRAIGHT HEADER,36 POSITION	5312-3400-0000	BERG
XU6,11,13-14,26-27, 36-39,42,44-46,48-50, 58,60-64	23	SOCKET 14 PIN GOLD PLATED	5315-1900-0001	CIR ASSY
XU1,3,5,9-10,12,25,43, 47	9	SOCKET 16 PIN GOLD PLATED	5315-2000-0001	CIR ASSY
XU31-32,34-35	4	SOCKET 18 PIN GOLD PLATED	5315-3200-0001	CIRC ASSY
XU4,17,20,28-29,53-54,56-57,65	10	SOCKET 20 PIN GOLD PLATED	5315-3000-0001	CIRC ASSY
XU15,41,59	3	SOCKET 24 PIN GOLD PLATED	5315-2100-0001	CIRC ASSY
XU22-24	3	SOCKET 28 PIN GOLD PLATED	5315-2200-0001	CIRC ASSY
XU2,16,40,55	4	SOCKET 40 PIN GOLD PLATED	5315-2300-0001	CIRC ASSY
00183	1	CABLE TIE	5500-0065-0000	PANDUIT

05-56201 X8 ON
62 56 20 1 24 "
62 28 0010 - 60

HP ASCII & HP-IB BUS CODES

B7 B6 B5 BITS B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		NUMBERS SYMBOLS		UPPER CASE		LOWER CASE	
0 0 0 0	0 0 NUL NUL	16 10 ρ DLE	32 20 SP SPACE MLA0	48 30 0 0 MLA16	64 40 @ @ MTA0	80 50 P P MTA16	96 60 ` MSA0	112 70 p P MSA16
0 0 0 1	1 1 β SOH GTL	17 11 σ DC1	33 21 ! ! MLA1	49 31 1 1 MLA17	65 41 A A MTA1	81 51 Q Q MTA17	97 61 a a MSA1	113 71 q q MSA17
0 0 1 0	2 2 γ STX	18 12 τ DC2	34 22 " " MLA2	50 32 2 2 MLA18	66 42 B B MTA2	82 52 R R MTA18	98 62 b b MSA2	114 72 r r MSA18
0 0 1 1	3 3 δ ETX	19 13 υ DC3	35 23 # # MLA3	51 33 3 3 MLA19	67 43 C C MTA3	83 53 S S MTA19	99 63 c c MSA3	115 73 s s MSA19
0 1 0 0	4 4 ε EOT SDC	20 14 φ DC4	36 24 $ $ MLA4	52 34 4 4 MLA20	68 44 D D MTA4	84 54 T T MTA20	100 64 d d MSA4	116 74 t t MSA20
0 1 0 1	5 5 ζ ENQ PPC	21 15 χ NAK PPU	37 25 % % MLA5	53 35 5 5 MLA21	69 45 E E MTA5	85 55 U U MTA21	101 65 e e MSA5	117 75 u u MSA21
0 1 1 0	6 6 η ACK	22 16 ψ SYN	38 26 & & MLA6	54 36 6 6 MLA22	70 46 F F MTA6	86 56 V V MTA22	102 66 f f MSA6	118 76 v v MSA22
0 1 1 1	7 7 BEL BEL	23 17 ω ETB	39 27 ' ' MLA7	55 37 7 7 MLA23	71 47 G G MTA7	87 57 W W MTA23	103 67 g g MSA7	119 77 w w MSA23
1 0 0 0	8 8 BS BS GET	24 18 Ω CAN SPE	40 28 ((MLA8	56 38 8 8 MLA24	72 48 H H MTA8	88 58 X X MTA24	104 68 h h MSA8	120 78 x x MSA24
1 0 0 1	9 9 HT HT TCT	25 19 √‾ EM	41 29)) MLA9	57 39 9 9 MLA25	73 49 I I MTA9	89 59 Y Y MTA25	105 69 i i MSA9	121 79 y y MSA25
1 0 1 0	10 A LF LF	26 1A → SUB	42 2A * * MLA10	58 3A : : MLA26	74 4A J J MTA10	90 5A Z Z MTA26	106 6A j j MSA10	122 7A z z MSA26
1 0 1 1	11 B VT VT	27 1B ESC ESC	43 2B + + MLA11	59 3B ; ; MLA27	75 4B K K MTA11	91 5B [[MTA27	107 6B k k MSA11	123 7B { { MSA27
1 1 0 0	12 C FF FF	28 1C ↑ FS	44 2C , , MLA12	60 3C < < MLA28	76 4C L L MTA12	92 5C \ \ MTA28	108 6C l l MSA12	124 7C ¦ ¦ MSA28
1 1 0 1	13 D CR CR	29 1D ÷ GS	45 2D - - MLA13	61 3D = = MLA29	77 4D M M MTA13	93 5D]] MTA29	109 6D m m MSA13	125 7D } } MSA29
1 1 1 0	14 E S0 S0	30 1E Σ RS	46 2E . . MLA14	62 3E > > MLA30	78 4E N N MTA14	94 5E ∧ ∧ MTA30	110 6E n n MSA14	126 7E ~ ~ MSA30
1 1 1 1	15 F SI SI	31 1F ≈ US	47 2F / / MLA15	63 3F ? ? UNL	79 4F O O MTA15	95 5F — — UUT	111 6F o o MSA15	127 7F ■ RUBOUT
	2⁰ 2¹ 2² 2³	ADDRESSED COMMANDS	UNIVERSAL COMMANDS	LISTEN ADDRESSES		TALK ADDRESSES		SECONDARY ADDRESSES OR COMMANDS

KEY



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