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Instruction Manual
For
Synchro/Resolver Angle Indicator
Model SR/HSR-203 (-488)

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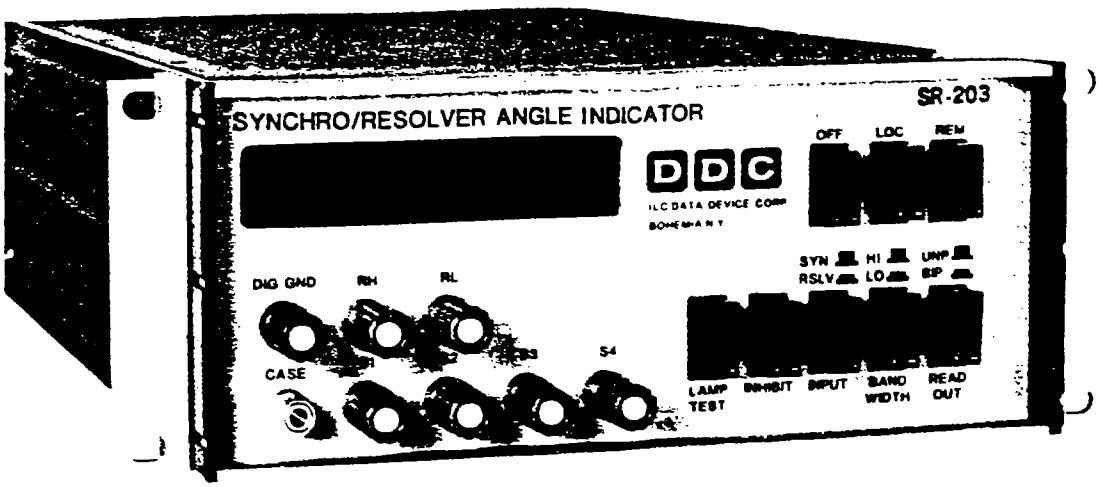


Figure 1-1. Model SR-203 Synchro/Resolver Angle Indicator

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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual contains installation, operation, and maintenance instructions for the Models SR-203 and HSR-203 Synchro/Resolver Angle Indicators, manufactured by ILC Data Device Corporation, Bohemia, New York. (See figure 1-1.) Also covered are the Models SR203-488 and HSR203-488. Except for the added IEEE-488 Interface, the SR203-488 and HSR203-488 are functionally identical to their SR-203 and HSR-203 counterparts.

To avoid repetition, information presented in this manual covers the SR-203 and SR203-488. All the data and references to the Model SR-203 (or SR203-488) are equally valid for the Model HSR-203 (or HSR203-488) except where noted. The HSR-203 differs from the SR-203 only in its accuracy and resolution. The SR-203 is accurate to $\pm 0.03°$, while the HSR-203 is $\pm .005°$ accurate. Resolution is $\pm 0.01°$ for the SR-203 and $\pm 0.001°$ for the HSR-203.

1.2 PURPOSE OF EQUIPMENT

The SR-203 is a high quality angle indicator suitable for use in precision synchro and resolver test equipment. The unit consists of a precision analog-to-digital tracking converter configured to accept synchro or resolver signals from a front panel input channel or either of two rear connector input channels. The instrument continuously converts the selected synchro or resolver inputs into BCD angular data and displays it on the front panel. Since the instrument can accept a broad range of voltages and frequencies without programming, and signal to reference phase shifts of $\pm 50°$ (max), the SR-203 can quickly accommodate a variety of inputs. Using a type II servo loop for continuous tracking, the instrument exhibits no velocity lag up to the specified tracking rates. No hangup can occur 180° away from the input angle.

In addition to serving as a high performance bench instrument, the SR-203 can be used wherever accurate angle information is required for display, control, testing, or computation. Applications include production testing of synchros and resolvers, information translators in quality control systems, machine tool control, ship and aircraft navigation systems, and antenna positioning.

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The 488 Interface is available as an option (Model SR203-488). When equipped with this option, the instrument may be linked to any programmable measurement instrument system (such as computer controlled Automatic Test Equipment (ATE) or process control systems) that operates from the IEEE-488-1975 General Purpose Interface Bus (GPIB). An abbreviated description of the IEEE-488 GPIB is included in the Appendix for general reference.

1.3 FEATURES

A number of outstanding features are incorporated into the design of this instrument, as follows:

a. Selection of synchro or resolver inputs from front panel jacks (local mode) or either of two rear panel inputs (remote mode).

b. Automatic operation over a wide range of signal input levels without the need for signal level programming.

c. No 180° hangup.

d. Display ambiguity indicator.

e. Built-in-Test (BITE) circuit - detects over-velocity or internal malfunction. Outputs the logic level and displays it on front panel.

f. Automatic correction of signal to reference phase differences of up to $\pm 50°$.

g. No warmup, no adjustments and no drift. Drift-free for the life of the instrument.

h. Selection of high or low tracking loop bandwidth from front panel switch (local mode) or via interface connector (remote mode).

i. Display and output data in unipolar format of 0-359.99° for SR-203 or 0-359.999° for HSR-203; or in bipolar format of 0 to $\pm 179.99°$ for SR-203 or 0 to $\pm 179.999°$ for HSR-203. Desired format selectable from either the front panel (local mode) or via the interface connector (remote mode).

j. Inhibit and lamp test functions selectable from either the front panel (local mode) or via the interface connector (remote mode).

k. A single switch multiplexes control between local and remote sources and between front panel and rear connector input channels.

l. When equipped with the 488 Interface, (Model SR203-488), control may be transferred to the GPIB when in the remote mode.

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1.4 OPTIONS

This instrument may be ordered in any of three physical configurations. As a portable instrument it is supplied in compact form with a carrying handle. In a second form, it is fitted with brackets, suitable for half rack mounting. It may also be ordered center-mounted in a 19" panel suitable for mounting in a 19" rack.

All instruments are supplied with a mating connector (Amphenol 17-10500-1) and a detachable line cord (Belden 17250).

1.5 PHYSICAL DESCRIPTION

The Models SR-203 and SR203-488 are small lightweight units. Figure 1-1 illustrates the SR203-488 in the half rack mount configuration. The digital display of shaft angle is plainly visible behind a rectangular cutout in the front panel. Selection of either local or remote modes is controlled by LOC and REM pushbutton switches which also apply power to the instrument. The interlocked OFF switch turns off the unit.

Binding posts under the display may be used to apply synchro or resolver signals for local mode operation. The pushbuttons to the right of the binding posts are manual controls associated with local mode operation.

Internally, the instrument consists of two printed circuit boards (a converter board and a multiplexer/488 interface board), an interboard harness, and front and rear panel harnesses. Removal of the top cover exposes the converter board. (See figure 1-2.) The converter circuits are packaged in two compact encapsulated modules. The 7-segment LED's occupy the front left portion of the board. The SR-203 contains 6 LED displays, as shown; the HSR-203 contains an additional display. The remaining components are distributed around the two modules. Power supply components are mounted at the rear of the board. A line voltage selector switch (S2) may be easily set to 115 or 230 volts.

Removal of the bottom cover exposes the multiplexer/488 interface board. (See figure 1-3.) In the Model SR203-488, IC's and other components of the 488 interface circuits occupy the central portion of the board. Power supply components on the heat sink assembly, driven by transformer T1, supply the dc power for this board. Line selector switch S2 on this board must be set to the same position as switch S2 on the converter board. Relays K1 and K2, at the rear of the board, are controlled by externally supplied signals during remote mode operation.

The rear panel, shown in figure 1-4, contains an instrument interface connector, a GPIB (General Purpose Interface Bus) connector, an address selector switch and a power connector. The address selector switch (S3) consists of eight rocker switches. Only the five LSB's are used to set the bus address.

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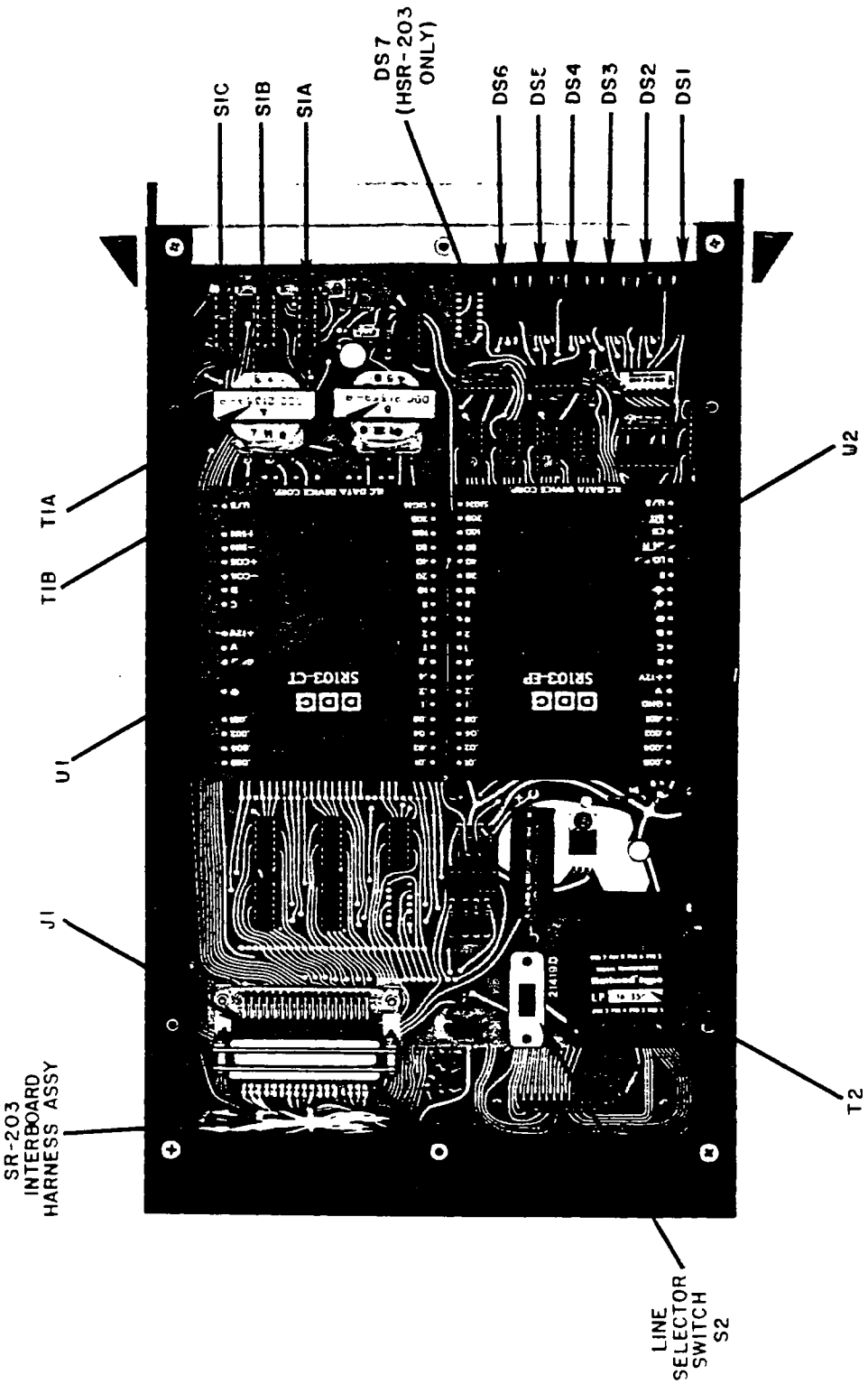


Figure 1-2. Converter Board (Top Cover Removed)

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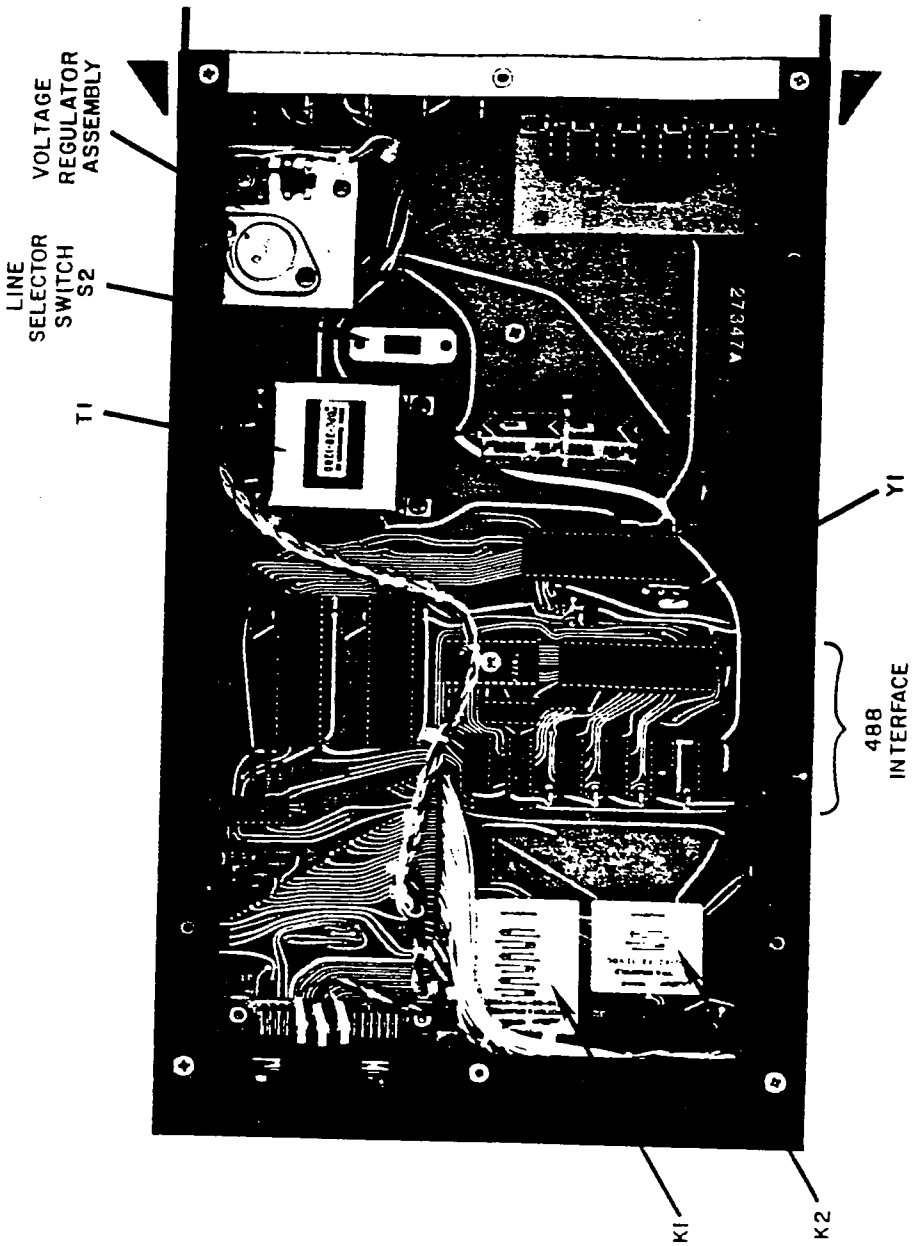


Figure 1-3. Multiplexer/488 Interface Board (Bottom Cover Removed)

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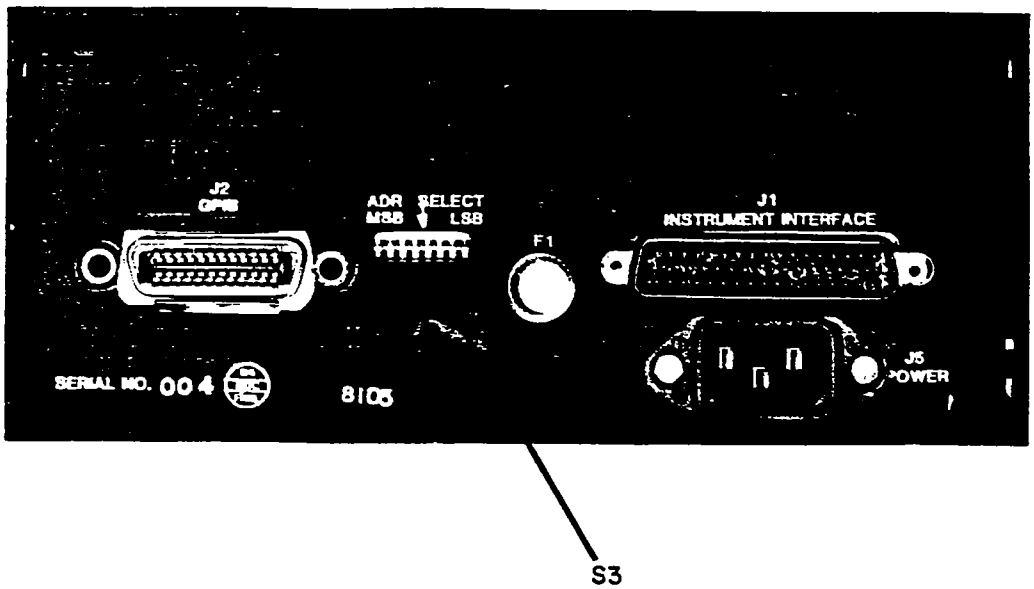


Figure 1-4. Rear View of SR-203

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1.6 TECHNICAL CHARACTERISTICS

Table 1-1 summarizes the principal characteristics of the instrument.

Table 1-1. Technical Characteristics

Angular Range	
SR-203	0.00 to 359.99° continuous rotation or 0.00 to ±179.99° bi-polar.
HSR-203	0.000 to 359.999° continuous rotation or 0.000 to ±179.999° bi-polar.
Accuracy	
SR-203	±.03°
HSR-203	±.005°
Tracking Rate, no error	
SR-203	720° / sec at 400 Hz 180° / sec at 50-60 Hz
HSR-203	72° / sec at 400 Hz 18° / sec at 50-60 Hz
Settling Time (to within 1 LSB) for a 179° step change	
High Bandwidth	
SR-203	0.6 sec
HSR-203	3.5 sec
Low Bandwidth	
SR-203	1.7 sec
HSR-203	8 sec
Open Loop Transfer Function	
High Bandwidth	
SR-203	$G = \frac{(86)^2(S/46 + 1)}{S^2(S/460 + 1)}$
HSR-203	$G = \frac{(42)^2(S/21 + 1)}{S^2(S/210 + 1)}$
Low Bandwidth	
SR-203	$G = \frac{(18)^2(S/10 + 1)}{S^2(S/100 + 1)}$
HSR-203	$G = \frac{(13)^2(S/10 + 1)}{S^2(S/100 + 1)}$
Display Resolution	
SR-203	±0.01° (5 BCD Digits)
HSR-203	±0.001° (6 BCD Digits)

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Table 1-1. Technical Characteristics (Cont'd.)

Repeatability	
SR-203	±0.01°
HSR-203	±0.002°
Reference Input	
Voltage	10-150 volts rms
Frequency	47-1000 Hz, from same source as synchro/resolver excitation
Phase, relative to signal	±50°
Input impedance	100 kilohms min.
Isolation	Transformer
Breakdown, to logic gnd	1000 V min.
Harmonic content	±10% max.
Signal Input	
Type	Synchro or resolver, transformer isolated
Voltage, L-L	Any level, 10V to 100V, auto leveling
Frequency	Same as reference
Allowable phase shift	±50° max., relative to reference
Input Impedance	
SR-203	150 kilohm min. @ 47 Hz 250 kilohm min. @ 60-1000 Hz
HSR-203	1 megohm min.
Isolation	Transformer
Breakdown, to logic gnd	1000 V min.
Digital Inputs (TTL Compatible)	
Inhibit (INH)	Logic 1 or open = track Logic 0 or gnd = hold (freeze)
Lamp Test (LT)	Logic 1 or open = θ (angle) Logic 0 or gnd = 888.88° (SR-203) or 888.888° (HSR-203)
Bandwidth (BW)	Logic 1 or open = lo bandwidth (47-1000 Hz) Logic 0 or gnd = hi bandwidth (360-1000 Hz)
Uni-polar/Bi-polar (U/B)	Logic 1 or open = uni-polar operation Logic 0 or gnd = bi-polar operation
Loading	0.5 TTL unit loads max.
Remote Channel Select	Logic 0 or gnd = channel 1 Logic 1 or open = channel 2
Remote Synchro/Resolver Select	Logic 1 or open = resolver Logic 0 or gnd = synchro

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Table 1-1. Technical Characteristics (Cont'd.)

Digital Outputs (TTL Compatible)	
Shaft Angle (ø)	
SR-203	5 BCD buffered TTL decades (18 lines total). Positive true logic, continuously available. In bi-polar mode, minus sign = logic 1 on MSB.
HSR-203	Same as SR-203, except 6 BCD decades used (22 lines total).
BITE	Logic 1 = fault (tracking failure) Logic 0 = no fault
Converter Busy (CB)	Logic 1 pulses = busy* Logic 0 = data stable
Drive Capability	4 unit TTL loads, buffered output
Display Characteristics	
Display Scan Rate	
SR-203	333 Hz
HSR-203	278 Hz
Display Duty Cycle	
SR-203	20%
HSR-203	16.7%
Display Clock	1.67 Hz
Display Clock Duty Cycle	50%
Power Input	
Voltage	115V/230V RMS**
Power	20 va max
Frequency	47-500 Hz
Isolation	Transformer
Breakdown to logic gnd	1000V DC
Temperature Range	
Operating	0°C to 55°C
Storage	-55°C to +125°C
Dimensions	
Option 1	
(carry handle)	9-3/8"W x 3-15/32"H x 14-1/2"D
Option 2	
(half-rack mount)	9-1/2"W x 3-15/32"H x 14-1/2"D
Option 3	
(center mount on 19" panel)	19"W x 3-15/32"H x 14-1/2" D
Weight	5 lbs (approx.)

*4 usec positive pulses; leading edge initiates conversion.
**Voltage selectable by two internal switches. See para. 2.1.

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Table 1-2. IEEE-488 Interface Data

Command Function: The Following subset of the IEEE-488 standard is implemented.

SH1	Full Source Handshake capability.
AH1	Full Acceptor Handshake capability.
T6	Basic Talk capabilities with Serial Poll and untalk if my listen address.
L4	Basic Listen capabilities with unlisten if my talk address.
SR1	Full Service Request capability.
RLO	Remote Local selection via manual front panel switch.
DCO	No Device Clear capability.
DTO	No Device Trigger capability.
CO	No Controller capability.

Table 1-3. IEEE-488 Interface Data

Device Commands	
Control Word (ASCII)	Function
P	Preset to Channel 1, Synchro Input, no Inhibit, no Lamp Test, High Bandwidth, Unipolar output.
S	Synchro input mode.
R	Resolver input mode.
1	Channel 1 Remote Input.
2	Channel 2 Remote Input.
H	High bandwidth select.
L	Low bandwidth select.
U	Unipolar display and output.
B	Bipolar display and output.
I	Inhibit converter tracking.
F	Enables converter tracking.
T	Enables lamp test.
D	Disables lamp test; causes angle data to be displayed.

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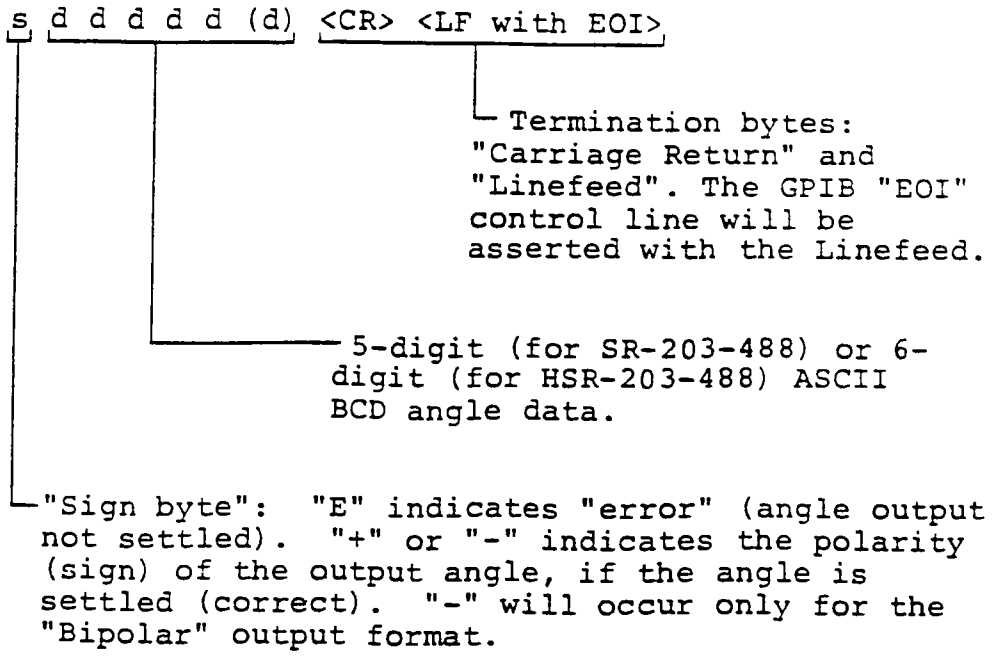


Figure 1-5. Talk Routine (Reply String)

Table 1-4. Status Byte

BIT	BIT WEIGHT (HEX)	BIT DESCRIPTION
7 (MSB)	80	Not Used.
6	40	RQS (Request for Service)
5	20	Not Used.
4	10	Not Used.
3	08	Not Used.
2	04	Not Used.
1	02	Error in input command string (illegal command received).
0	01	Command received when instrument is in "Local" control mode.

SRQ Conditions:

(1) Error in input command string.
(2) Command received when instrument is in "Local" control mode.

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SECTION 2

INSTALLATION AND OPERATION

2.1 PREPARATION FOR USE

The Models SR-203 and SR203-488 are electrically operational in all respects as shipped from the factory. Carefully remove the instrument from the packaging material and inspect the front and rear panels for damage to any parts. Unless otherwise specified, the unit is set at the factory for 115-volt operation. If in doubt, remove the top and bottom covers and check the settings of the two line selector switches. (See figures 1-2 and 1-3.) Should the instrument show any signs of damage, notify the nearest ILC Data Device Corporation field representative immediately.

2.2 INSTALLATION

No special installation procedures are required for the standard (option 1) unit. For the half rack or center mount (19" panel) options, carefully insert the unit into the rack and bolt in place with standard hardware.

2.3 CONNECTIONS

The interface connector available with the instrument must be wired to the external system. Table 2-1 lists the connector pin assignments. Crimp or solder each input and output lead to the pins as listed, then push the pins in until they lock in place.

IMPORTANT

This instrument is equipped with separate case and digital grounds. For best results, case ground (pin 3) and digital ground (pin 4) should be connected together in the external system. When the digital outputs are not used, connect the two grounds together at the instrument.

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Table 2-1. Interface Connector Pin Assignments

Pin	Function
1	Spare
2	Spare
3	Case gnd
4	Digital gnd (may be connected to case gnd)
5	S1
6	S2
7	S3
8	S4
	Remote channel 1 inputs (S4 used for resolver inputs only)
9	Ref hi
10	Ref lo
	Channel 1 ref-input
11	Converter Busy Output
12	.04°
13	.01°
14	.08°
15	.2°
16	4°
17	1°
18	Spare
19*	Lamp Test Input ($\overline{LT}$) Logic 1 = normal operation Logic 0 = lamp test (remote mode)
20*	CH1/$\overline{CH2}$ (Input) Logic 1 = Channel 2 Logic 0 = Channel 1
21	S1
22	S2
23	S3
24	S4
	Remote channel 2 inputs (S4 used for resolver inputs only)
25	Ref hi
26	Ref lo
	Channel 2 ref input

Pin	Function
27*	$\overline{INH}$ (Input) Logic 1 = track Logic 0 = inhibit
28	.02°
29	.08°
30	.1°
31	.4°
32	2°
33	8°
34	$\overline{RESET}$ (IEEE Interface) Logic 1 = Normal operation Logic 0 = Reset
35	UB (Output) Logic 1 = Unipolar Logic 0 = Bipolar
36	LOC/$\overline{REM}$ (Output) Logic 1 = Local Mode Logic 0 = Remote Mode
37*	SYN/$\overline{RES}$ Logic 1 = Resolver Logic 0 = Synchro Remote Mode
38*	UB (Input) Logic 1 = Unipolar Logic 0 = Bipolar Remote Mode
39*	BW (Input) Logic 1 = lo bandwidth (47-1000 Hz) Logic 0 = hi bandwidth (360-1000 Hz)
40	BITE (Output) Logic 1 = Not tracking (fault) Logic 0 = Normal tracking

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Table 2-1. Interface Connector Pin Assignments (Cont'd.)

Pin	Function	Pin	Function
41	.008°	46	40°
42	.004°	47	80°
		48	10°
43	.002°	49	100°
44	.001°	50	Unipolar = 200°
45	20°		Bipolar 1 = Minus (-) sign 0 = Plus

*User must supply digital input signals for SR-203 and HSR-203 instruments. For the SR203-488 and HSR203-488, these pins must not have external connections.

2.4 OPERATING CONTROLS AND INDICATORS

The controls and indicators used in the operation of the SR-203 are shown in figure 1-1. and described in Table 2-2.

Table 2-2. Operating Controls and Indicators

Item	Function
OFF pushbutton switch	When depressed, removes AC power from instrument.
LOC pushbutton switch	When depressed, applies ac power to instrument and places it in local mode.
REM pushbutton	When depressed, applies ac power to instrument and places it in remote mode.
LAMP TEST pushbutton switch	When depressed (either local or remote mode), causes all segments of all LED displays to light.
INHIBIT* pushbutton switch	When depressed, inhibits the analog-to-digital converter, freezing the LED display and digital output angle.

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Table 2-2. Operating Controls and Indicators (Cont'd.)

Item	Function
INPUT* pushbutton switch	When depressed to RSLV position, conditions converter for operation from resolver input signal. When depressed to SYN position, conditions converter for operation from synchro-formatted input signal.
BANDWIDTH* pushbutton switch	When depressed to HI, enables converter for high bandwidth (360-1000 Hz). In LO position, conditions converter for low bandwidth (47-1000 Hz).
READ OUT* pushbutton switch	When depressed to UNP, configures display circuits and visual readout for unipolar operation. In BIP position, bipolar display is enabled.
S1, S2, S3, S4, RL, RH binding posts*	Provide front panel access to locally supplied synchro or resolver and reference signals.

*Enabled only during local operation.

2.5 OPERATING PROCEDURE

2.5.1 Remote Operation

To operate the instrument from a remote location via interface connector J1, first program the proper input lines (identified in Table 2-1) for the desired input channel, synchro or resolver format, bandwidth, and read-out mode (unipolar or bipolar). Then depress the REM pushbutton switch to apply power and simultaneously place the instrument in remote mode. No other procedures are required. The digital output will track the synchro/reference input angle supplied by the external system and the LED display will indicate the digital angle. The external system may, at any time, switch the input channel, input signal format, readout mode, and bandwidth desired. During remote operation, the external system may also apply inhibit and perform the lamp test. It should be noted that, during remote operation, the local operator can only perform the lamp test.

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For instruments using the 488 interface, the remote control lines such as channel select, lamp test, inhibit, synchro/resolver select, unipolar/bipolar select and bandwidth select are controlled by the GPIB and should not be wired to the interface connector. For operation with the GPIB, the mating connector to GPIB connector J2 controls the instrument. The five LSB's of the eight ADR SELECT rocker switches on the rear panel of the instrument determine the device address. Set these switches to the required bus address, LSB to MSB as marked, before applying power.

When operating from the GPIB, the SR203-488 is controlled by the bus commands. The codes applicable to this instrument are listed in Table 3-2. Each command is ASCII encoded and applied to the instrument via the bus data lines. When addressed to listen (and if the unit is in remote mode), the unit responds to the commands.

2.5.2 Local Operation

To operate in local mode, proceed as follows:

a. Connect the synchro or resolver and reference inputs to the front panel binding posts.

b. Depress the INPUT, BANDWIDTH and READOUT pushbutton switches to the desired positions.

c. Depress the LOC pushbutton switch to apply power to the instrument and to place it in local mode. No other procedures are required. The digital output will track the synchro/resolver input and the visual readout will display the digital angle.

d. To test the display, depress and hold the LAMP TEST pushbutton. To inhibit the converter and freeze the display, depress and hold the INHIBIT pushbutton.

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SECTION 3

PRINCIPLES OF OPERATION

3.1 INTRODUCTION

This section describes the operation of the Model SR203-488 in terms of block and simplified diagrams (figures 3-1 through 3-5) and the overall schematic diagram, figure 4-1. Sufficient information is provided to support equipment maintenance down to module level.

3.2 OVERALL DESCRIPTION (See figure 3-1.)

The SR203-488 consists basically of a precision resolver-to-digital tracking converter, input circuits that apply the desired synchro/resolver and control functions to the converter in either local or remote mode, display circuits, and the 488 interface for communicating with the GPIB. The OFF/LOCAL/REMOTE switch determines the operating mode. When the LOCAL pushbutton switch is depressed, synchro or resolver and reference signals applied to the front panel jacks are routed, via the INPUT and LOCAL switches to the signal and reference isolation transformers. Depending on its setting, the INPUT switch configures the transformers for either 3-wire synchro or 4-wire resolver inputs. The transformers pass resolver and reference signals to the tracking converter which digitizes its inputs into either 18-bit BCD angle data (Model SR203-488) or 22-bit data (Model HSR203-488). The digital angle is displayed on either a 5-digit (SR203-488) or 6-digit (HSR203-488) readout and is simultaneously made available to the rear panel interface connector via the TTL output buffer or to the GPIB via the 488 interface.

The converter also generates CB (Converter Busy) and BITE (Built-In Test Equipment) signals. The CB pulses indicate when output data is changing. The BITE signal is used to indicate the presence of an abnormal condition. Both signals are applied via the TTL output buffer, to the interface connector and the 488 interface. Unbuffered CB and BITE signals pass to the display circuits to activate ambiguity and BITE indicators, respectively, under abnormal conditions.

When the LOCAL pushbutton switch is depressed, the local/remote multiplexer is conditioned for local operation. This enables the front panel logic switches, permitting operator selection of unipolar or bipolar (U/B) format and display, high or low bandwidth, and inhibit. The manual lamp test control function bypasses the multiplexer, allowing the operator to test the lamp segments in either the local or remote mode.

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When the REMOTE pushbutton switch is depressed, the synchro or resolver and reference inputs for the signal and isolation transformers are derived from either of two remote channels applied to the interface connector. Directed by a remote control signal from either the interface connector or the 488 interface, the channel 1/channel 2 select circuitry passes signals from the selected remote channel to the transformers via a synchro/resolver relay and contacts on the REMOTE switch. The synchro/resolver relay is activated by the same remote source, configuring the transformer inputs for either synchro or resolver signals.

In the remote mode, the multiplexer inputs are switched. Control of U/B format and display, bandwidth select, inhibit and lamp test is made available to the same remote control source (interface connector or 488 interface). The selected logic control signals pass through the multiplexer and TTL buffer to the tracking converter.

Operation of the 488 interface is supervised by a self-contained microprocessor in accordance with a program stored in an erasable programmable ROM. Data transfer to and from the 16-line GPIB is mediated by the controller. The 32 input-output lines at the instrument interface are independently programmed, under microprocessor control, for input or output data transfer. The device address, preset manually by the user via the address select switches, is transferred to the controller memory at power turn-on.

3.3 CONVERTER CIRCUITS, BLOCK DIAGRAM DESCRIPTION (See Figure 3-2.)

The tracking converter circuits, contained on the converter board, consist basically of a solid state control transformer (SSCT), error processor and up-down counter which operate in a continuous Type II closed loop feedback configuration. Supplied with sin θ and cos θ signals from a Scott-T input transformer, the SSCT compares the synchro or resolver input angle θ from the selected local or remote input channel with digital angle ϕ supplied by the up-down counter and generates an error voltage E which is a function of the sine of residue angle $(\theta - \phi)$. The error voltage is demodulated and integrated by the error processor which controls the up-down counter such that at null, angle θ = angle ϕ. Angle ϕ, a digital replica of the selected synchro or resolver angle, is displayed on a 5-digit (Model SR203-488) or 6-digit (Model HSR203-488) readout and is simultaneously made available to the external system via the TTL output buffers and the DBA-488.

Auto leveling signals generated by the SSCT are fed to the error processor, enabling the instrument to operate automatically with any signal input voltage between 10 and 100 volts RMS L-L.

Additional digital input and output controls, in TTL form, are designed into the unit to enhance its operation with computerized equipment. For example, when a logic 0 is applied to the $\overline{\text{INH}}$ (inhibit) input, digital angle ϕ is frozen in the up-down counter. This feature permits the external system to determine the readout at a particular point in time.

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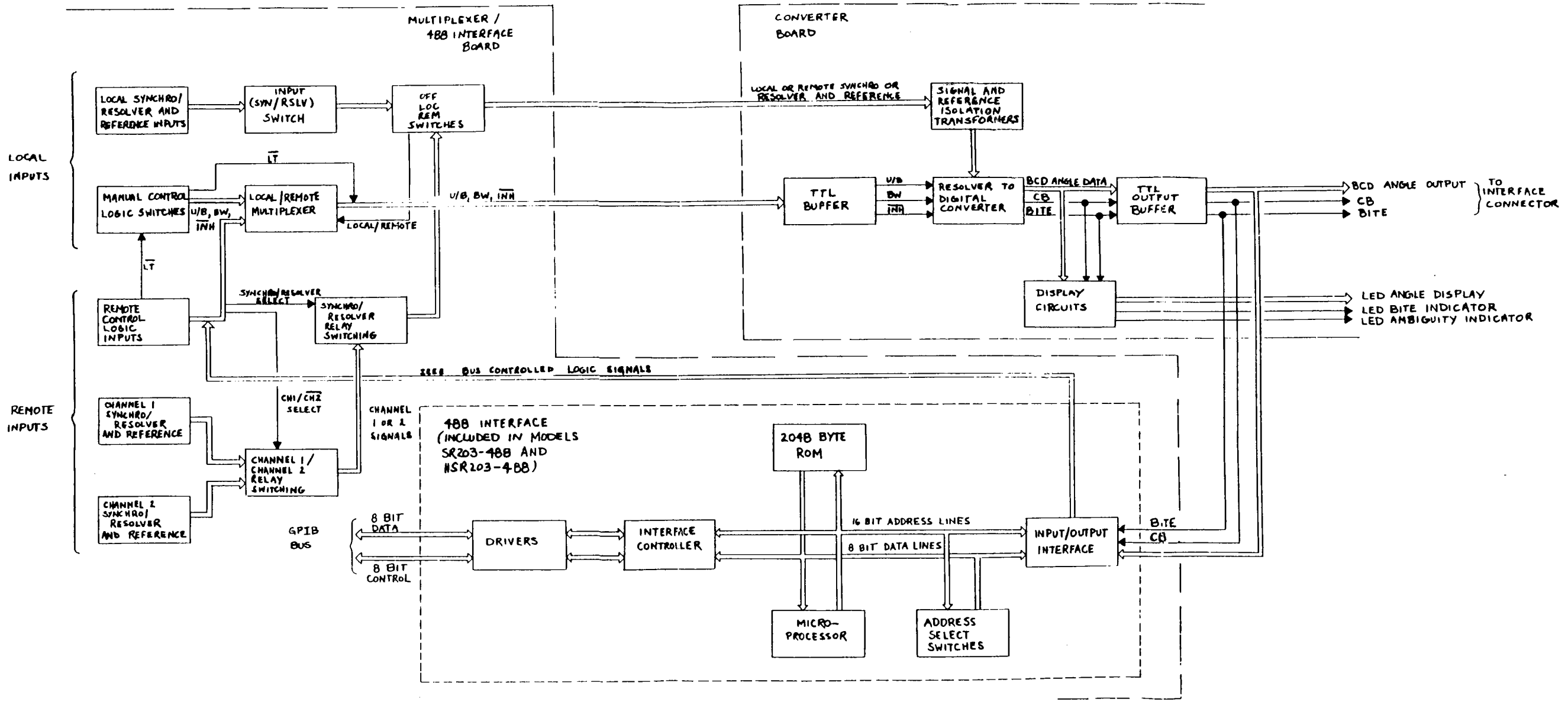


Figure 3-1. SR203-488, Block Diagram

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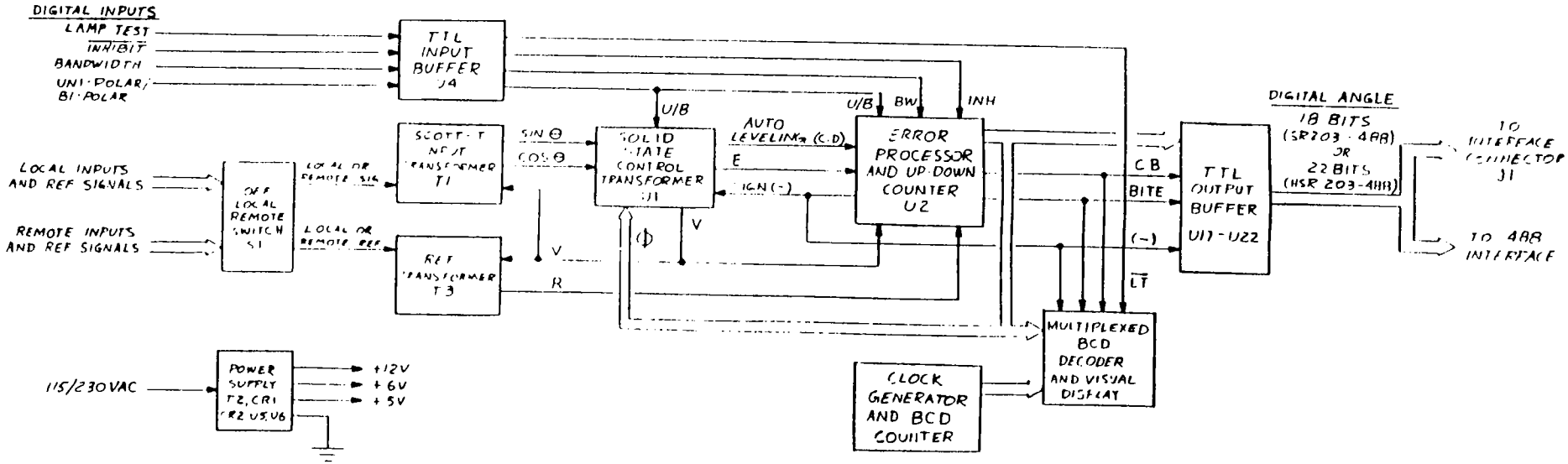


Figure 3-2. Converter Circuits, Block Diagram

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The bandwidth control input enables high bandwidth or low bandwidth operation. Selection of higher bandwidth (logic 0 input) enables higher tracking speeds and acceleration constants for signal frequencies greater than 360 Hz.

Application of a logic 1 to the U/B (unipolar/bipolar) control input programs the up-down counter, control transformer, and visual readout for unipolar operation (0 to 359.99° for the SR203-488 or 0 to 359.999° for the HSR203-488). With a logic 0 applied to input U/B, a bipolar display (0 to ±179.99°) is enabled. When negative angles are detected during bipolar operation, a minus sign is activated in the visual diaplay.

The $\overline{LT}$ (lamp test) input permits all digital displays to be tested. Application of a logic 0 to the $\overline{LT}$ input produces numeral 8 on all digital displays, effectively checking operation of all diode segments.

The error processor provides two digital output controls via the TTL output buffers and 488 Interface: CB (converter busy) and BITE (Built-In Test Equipment). A logic 1 CB pulse is generated coincident with the leading edge of each toggle pulse. CB pulses are transmitted as flags to the external system to indicate that counter output data is changing. An ambiguity indicator, the lower bar in the first digital display, is activated if excessive CB pulses are generated (jitter condition or high tracking rate). Stable data is made available to the external equipment during non-CB (logic 0) intervals. When the error processor detects an abnormal condition (such as a loss of reference or abnormally high residue angle), it generates a logic 1 on the BITE line and activates a BITE indicator, the upper bar in the first digital display.

3.4 CONVERTER CIRCUITS, DETAILED DESCRIPTION
(See Sheet 3 of Figure 4-1.)

The interface circuits on the converter board employs LS TTL logic (+5V). Internal circuits use CMOS (+12V) logic.

Three-wire synchro data or 4-wire resolver data, at any level between 10 and 100 volts RMS L-L and at any frequency between 47 and 1000 Hz*, may be applied to either the local or remote inputs. When synchro inputs are selected, either in the local or remote mode, a jumper is automatically connected to the Scott-T transformer. (The synchro/resolver control circuits are described in later paragraphs.)

The reference voltage input for either local or remote operation may be between 10 and 150 volts RMS, derived from the associated synchro or resolver excitation voltage. Selection of either the local or remote signal and reference inputs is controlled by the front panel LOC and REM switches.

---

*For operation at higher tracking rates (360 Hz or higher), the BW control input may be set to logic 0 by depressing the BANDWIDTH pushbutton switch to HI (local mode) or by transmitting a logic 0 on the BW line from the remote source (remote mode). The lower bandwidth may be selected when maximum filtering is desired. In addition, low bandwidth must be selected for 50 or 60 Hz reference and input signals.

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Precision Scott-T transformer T1 provides +sine θ, -sine θ, +cosine θ, and -cosine θ signals for SSCT U1. These signals, as well as reference current supplied by transformer T3, are referenced to voltage V (analog ground) generated by error processor and up-down counter module U2. Transformers T1 and T2 effectively isolate the instrument electrically from the external system.

SSCT U1 compares input angle θ from T1 with digital angle ϕ from the up-down counter in U2. Utilizing state-of-the-art techniques, U1 generates error signal E as a function of the sine of residue angle $(\theta - \phi)$. Module U1 also supplies trigonometric function signals C and D used for auto levelling and synthetic referencing.

In module U2, error signal E is applied to a gain controlled amplifier as a function of signals C and D, maintaining the error gradient independent of signal or reference voltage amplitude. The auto-levelled error signal is demodulated, with the phase of demodulation controlled by a synthetic reference derived from signals C and D rather than reference current R. A monitoring circuit in U2 constantly compares the synthesized reference with reference current R and prevents 180° hangup. Up to $\pm$50° phase shift of the synchro/resolver input relative to the reference input is automatically corrected for.

The demodulated signal undergoes two integrations in U2, resulting in a Type II feedback loop that eliminates velocity tracking error. A BCD counter in U2 is driven towards an exact BCD representation of the input angle as a function of residue angle amplitude and polarity. Each count of the BCD counter is equivalent to one LSB. The 18 bits (SR203-488) or 22 bits (HSR203-488), representing digital angle ϕ in direct BCD form, are fed back to SSCT U1 to maintain its closed loop operation. The digital angle is also applied to the multiplexed BCD decoder and visual display for real time monitoring and is routed to the external system through TTL output buffers.

The visual readout for the Model HSR203(-488) consists of LED displays DS1 through DS7. Display DS7, the .001 digit, is not used in the Model SR203(-488). Numerical displays DS2 through DS6 are multiplexed to a single BCD to 7-segment decoder/driver U13. Depending on the 4-bit BCD input applied to U13, current is drawn through one or more LED's in each display via a current limiting resistor in dip R1, causing a digit to be displayed.

Multiplex timing is controlled by presettable BCD up counter U23 in conjunction with clock generator U15. The counter is programmed for operation with either the 5-digit display in the SR203(-488) or the 6-digit display in the HSR203(-488). The counter is incremented by pulses from clock generator U15. Following BCD count 7, receipt of a clock pulse sets the Q4 output (pin 2) of U23 high, presetting the counter to either BCD count 2 or 3. In the SR203(-488), pins 4 and 12 of counter U23 are jumpered, producing preset count 3. In the HSR203(-488), pins 4 and 13 are jumpered, producing count 2. Thus, in the SR203(-488), the counter is continuously incremented through counts 3 to 7. In the HSR203(-488), it counts from 2 to 7.

The 1, 2, and 4 BCD outputs of counter U23 are applied to five digitally controlled analog switches U7 through U11. Analog switch U7 samples the BCD "1" outputs (decades .001, .01, .1, 1, 10, and 100) of the BCD counter in module U2. Switches U8, U9, and U10

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similarly sample the BCD "2", "4", and "8" outputs, respectively, of U2. Analog switch U11 responds to each address from the counter by grounding the cathode of an LED display via hex inverter U16. Thus, each LED display is enabled, in turn, for each BCD count, and the associated display code simultaneously multiplexed at the output of decoder/driver U13 designates the required numeral.

Assume, for example, that angle 186.352° is generated at the BCD outputs of module U2 in the HSR203(-488). For this angle, the following digital bits are set high: 100, 80, 4, 2, .2, .1, .04, .01, and .002. Table 3-1 indicates the digital code produced at the outputs of analog switches U7 through U10 at each count, the resulting display code generated by decoder/driver U13, and the corresponding LED display activated by analog switch U11. The decimal point after the units digit in the display is maintained on by +6 volts applied to DS3 via resistor R16.

In the Model SR203(-488), counter U23 is programmed for preset to count 3 rather than count 2 so that DS6, the .001 digit, is never addressed. LED DS7 is omitted from this model.

When a low level is applied to the lamp test ($\overline{LT}$) input of the instrument, current is drawn through all LED's in each display, producing a readout of 888.88° (SR203-488) or 888.888° (HSR203-488). This checks the operation of all segments in the LED's.

Table 3-1. Formation of Digital Display 186.352°

BCD Count	U7 Pin 3	U8 Pin 3	U9 Pin 3	U10 Pin 3	U13 Display Code	LED Activated	LED Weight
2	0	1	0	0	2	DS7	.001
3	0	0	0	1	8	DS3	10
4	0	1	1	0	6	DS4	1
5	1	1	0	0	3	DS5	.1
6	1	0	1	0	5	DS6	.01
7	1	0	0	0	1	DS2	100
2	0	1	0	0	2	DS7	.001

Only the three horizontal segments or bars of LED DS1 are used. The upper bar functions as a BITE indicator. If error processor module U2 detects a fault condition (e.g., missing reference), the $\overline{BIT}$ output of U2 is set low. This level is inverted by U15 (2,3) and activates the top bar of DS1 via resistor R14.

The center bar of DS1 is used to display the minus ("-") sign during bipolar operation. The high level generated by the error processor in U2 when the measured angle goes negative is inverted twice by U15 (7,6,5,4) and activates the minus sign via R13.

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The lower bar in display DS7 is the ambiguity indicator. The activating circuit for this bar consists of inverter U16 (7,10), CR4, R12, C5, and U15 (14,15). Capacitor C5 is charged through R12, so that U15-14 is set high and U15-15 is set low. When the converter is busy, the CB output of error processor U2 is set high. This causes U16-10 to drop and C5 tends to discharge through CR4. If unstable converter operation (jitter or high tracking rate) occurs, C5 discharges and U15 turns on the indicator to alert the user that the display is inaccurate.

The TTL input buffers consist of exclusive OR gates U4. These stages provide TTL to CMOS level shift functions for the digital input controls. Output buffers U17 through U22 provide the CMOS to TTL level shift functions for the digital output angle and controls.

When either the LOC or REM pushbutton switch is depressed, AC power passes through switch S1C, activating the power supply on the converter board. Switched AC power is also fed back to the mux/488 interface board. A dual full-wave bridge power supply (T2, CR1-CR3, C1-C4, U5, and U6) provides +12, +6, and +5 volts DC for the converter PC board. The +12 and +6 volt outputs are regulated by regulators U5 and U6, respectively. The two primary windings on T2 may be connected for operation for 115 volt or 230 volt primary power lines by selector switch S2. The power supply may be operated from any power line frequency between 47 and 500 Hz.

3.5 488 INTERFACE, FUNCTIONAL DESCRIPTION (See Sheet 2 of Figure 4-1.)

3.5.1 Equipment Complement

The 488 Interface consists of four bus transceivers U1-U4, interface controller U5, microprocessor U6, tri-state buffers U7 and U8, ROM U9, and peripheral interface adapters (PIA's) U10 and U11.

3.5.2 Transceivers U1 and U2

Transceivers U1-U4 serve as the interface between the GPIB and the internal logic of the 488 interface. Transceivers U1 and U2 are used for bus management and handshake signals; U3 and U4 accommodate the eight data lines. Logic levels applied to the four transmit-receive inputs of each quad transceiver from controller U5 determine which section behaves as a bus driver or receiver for the associated bus line. The $T/\overline{R}$ control for $\overline{SRQ}$ is always wired high (transmit) while those for $\overline{REN}$, $\overline{IFC}$, and $\overline{ATN}$ are wired low (receive). The remaining signals are controlled by U5. The bus transceiver outputs meet all requirements of IEEE Std. 488-1975.

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3.5.3 Interface Controller U5

Under the direction of microprocessor U6, interface controller U5 mediates the transfer of data between the 488 interface and the GPIB. Controller U5 decodes messages from the GPIB, processes those directed to the 488 interface and transfers messages to the internal data bus. It should be noted that, although the GPIB signals follow negative logic convention, positive logic is used within the 488 interface. (Thus, the signal NRFD from the GPIB is designated RFD at the input of U5.) The controller is equipped with internal registers that are selected by register select lines RS0, RS1, and RS2 and chip select $\overline{CS}$ (via microprocessor address bits A0, A1, and A2 and A14') in conjunction with the read/write (R/$\overline{W}$) signals and Ø2 clock from the microprocessor. The registers accommodate functions such as address, data in, data out, interrupt status, etc. Data transfer between U5 and U3/U4 is effected through the IBØ - IB7 lines; the DBØ - DB7 lines carry data between U5 and the internal data bus. $\overline{CS}$ enables U5 and Ø2 is a timing signal provided by U6.

3.5.4 Microprocessor U6

The 8-bit microprocessor contains registers, accumulators, a 128 X 8 bit RAM and an internal clock. The 16-line address bus (AØ-A15) supervises the operations in the 488 interface. The 8-line bidirectional data bus (DØ-D7) transfers data to and from memory and the peripheral devices. Clock pulses at pin E (Ø2) are used for timing. Upon receipt of an interrupt request ($\overline{IRQ}$) from controller U5 (upon U5's receipt of DCL on the data lines), U6 completes its current instruction then cycles through an interrupt sequence that resets the microprocessor. The read/write (R/$\overline{W}$) output of U6 controls the read/write status of controller U5 and PIA's U10 and U11.

3.5.5 ROM U9

Erasable programmable ROM U9 stores the 488 interface program in its 2048 X 8 bit memory. When enabled ($\overline{CS}$ input low) and strobed by a clock pulse from U6 (STR input), address bits AØ-A8 are decoded and data transfer is effected on the DOØ - DO7 lines.

3.5.6

PIA's U10 and U11 interface the 488 circuits with the converter circuits. Four 8-bit bidirectional data buses (PAØ - PA7 and PBØ - PB7) communicate with the instrument; an 8-bit bidirectional bus (DØ - D7) links the selected PIA's with the internal data bus. Each chip is selected by $\overline{CS2}$ low via a U6 address routed through tristate buffer U8. Register select inputs (RSØ, RS1), controlled by microprocessor U6, address registers within each PIA which provide functions such as data direction, control, peripheral interface, etc. PIA read/write operation is controlled by the R/$\overline{W}$ input from U6.

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3.5.7 Power Up and Device Address

When power is applied to the 488 interface, the logic low level across capacitor C7 (resulting from its uncharged state) initializes U5, U10, U11 and U6. The $\overline{\text{ASE}}$ (address select) output of U5 drops, enabling the outputs of address switch S3. The five preset LSB's of S3, representing the primary device address, are then transferred into a register in controller U5 for subsequent use.

3.5.8 Data Transfer

Controller U5 responds to the device address (applied via the data line inputs on the $\overline{\text{IB}}$ lines) when the GPIB sets ATN true. Notified by U5 via the DB data lines, U6 addresses ROM U9 which determines if talk or listen operation is required. If the talk mode is selected, U6 enables PIA's U10 and U11 and causes data from the instrument to be transferred through the PIA's to controller U5 which transfers the data through the $\overline{\text{IB}}$ lines to U3 and U4. These buffers, enabled by a T/$\overline{\text{R}}$2 level from U5, transfer the required data to the GPIB. Transmission of the individual data bytes is accomplished in proper sequence as a function of the handshake procedure. The bus management lines ($\overline{\text{ATN}}$, $\overline{\text{IFC}}$, $\overline{\text{SRQ}}$, $\overline{\text{EOI}}$ and $\overline{\text{REN}}$) insure that information flows through the interface lines in orderly fashion. When the last data bytes (ASCII carriage return/line feed) are transmitted, the 488 interface sets $\overline{\text{EOI}}$ true to signal the end of the data transfer. This feature permits compatible operation of the 488 interface with the HPIB system. The entire sequence is terminated by an Untalk command from the controller.

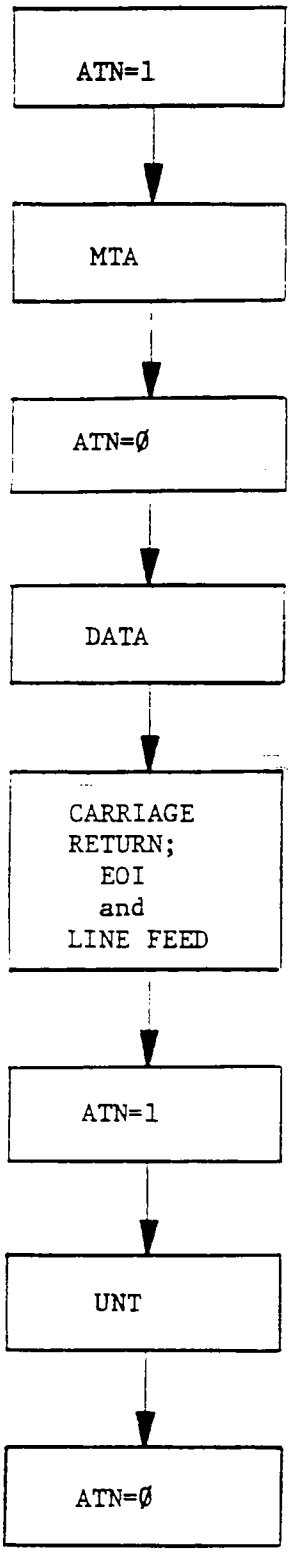
When the 488 interface listen address is received, data applied to U3 and U4 is transferred to controller U5. The microprocessor then transfers the data from U5 to the PIA's which pass the information to the instrument. An $\overline{\text{EOI}}$ or carriage return/line feed is received to indicate the end of the data transfer and the listen sequence is terminated by an Unlisten command.

3.6 SR203-488 COMMAND SEQUENCES

When operating from the IEEE-488-1975 GPIB, the SR203-488 performs the command sequences shown in Figures 3-3 and 3-4. Control code functions are listed in Table 3-2. In the talk routine (figure 3-3), the instrument transmits a sign byte (+, - or E for error) followed by 5 (for SR203-488) or 6 (HSR203-488) BCD ASCII data bytes, followed by CR (carriage return), followed by LF (line feed), when interrogated by the controller.

The listen routine (figure 3-4) indicates the possible ASCII control words that would be transmitted from a controller to the instrument. It should be noted that the 488 interface will accept all input commands regardless of the selected mode (local or remote), but these commands may be executed only when the instrument is placed in the remote mode.

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Controller sets ATN (Attention) line to true.

Controller transmits instrument talk address on the data lines.

Controller returns ATN line to false.

Instrument transmits ASCII encoded BCD data (first byte is +, -, or E for error) on the data lines. The subsequent five (for SR203-488) or six (HSR203-488) bytes constitute angular data, with the first of which representing the most significant digit, etc.

Instrument signals end of transmission by transmitting Carriage Return followed by simultaneously setting EOI (End or Identify) line to true and transmitting line feed on the data lines.

Controller sets ATN line to true.

Controller transmits an UNT (Untalk) command on the data lines.

Controller returns ATN line to false.

Figure 3-3. Talk Sequence

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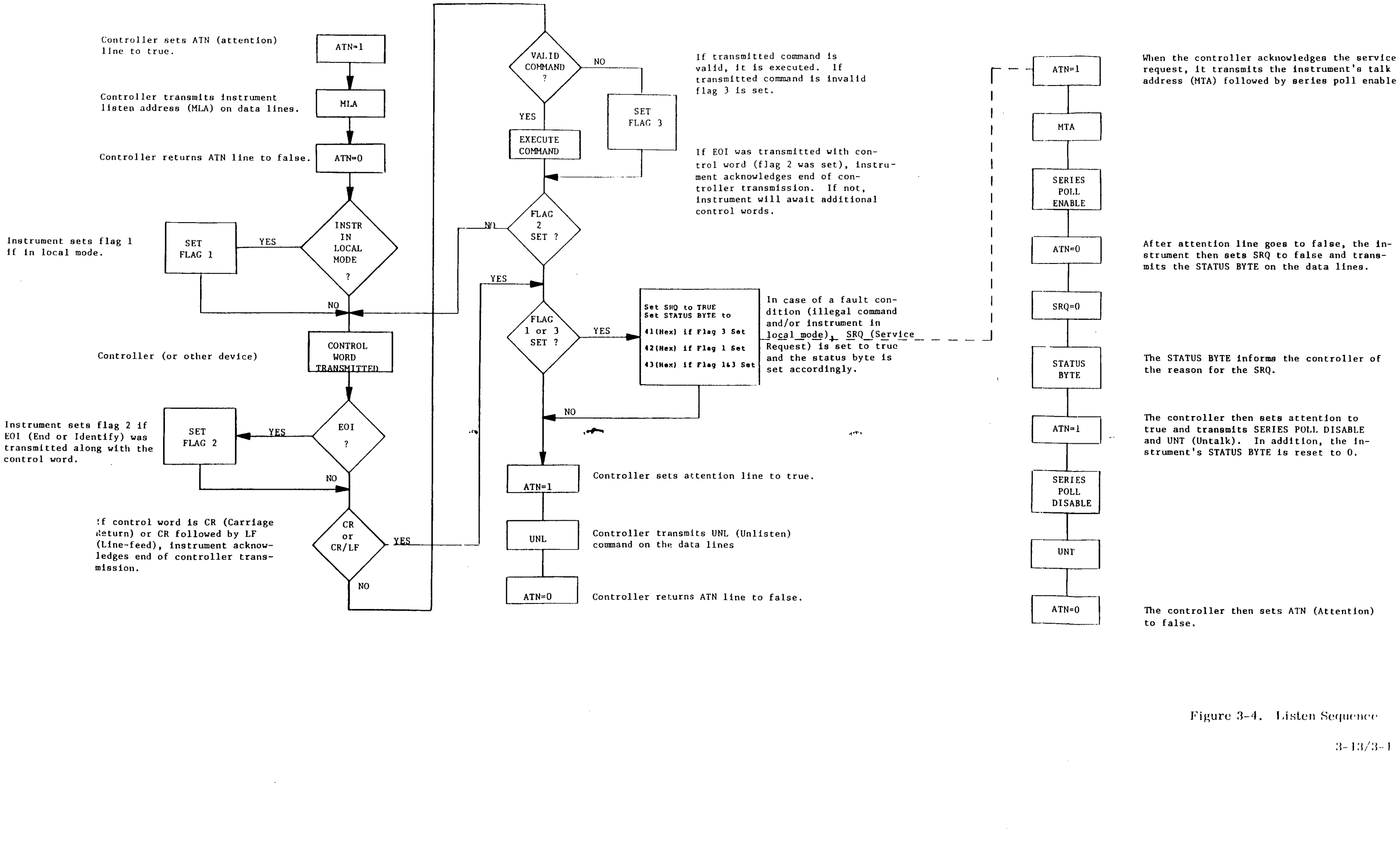


Figure 3-4. Listen Sequence

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Table 3-2. Control Code Functions

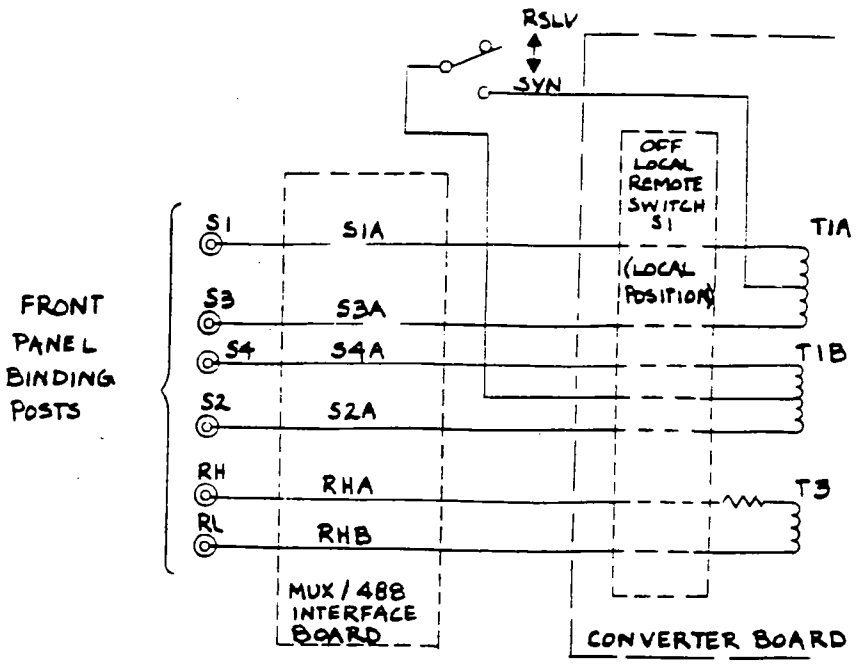
Control Word (ASCII)	Function
P (Preset)	Preset to: Channel 1 Synchro input No inhibit No lamp test High bandwidth Unipolar output
S (Synchro) R (Resolver)	Set synchro or resolver input mode
1 (Channel 1) 2 (Channel 2)	Selects remote input channel 1 or 2 on interface connector
H (High) L (Low)	Selects high or low bandwidth
U (Unipolar) B (Bipolar)	Selects unipolar or bipolar readout and output
I (Inhibit) F (Follow)	Inhibits the converter or allows it to follow (track) the input
T (Test) D (Data)	Tests lamps (+) or enables data display (D)

3.7 CONTROL CIRCUITS

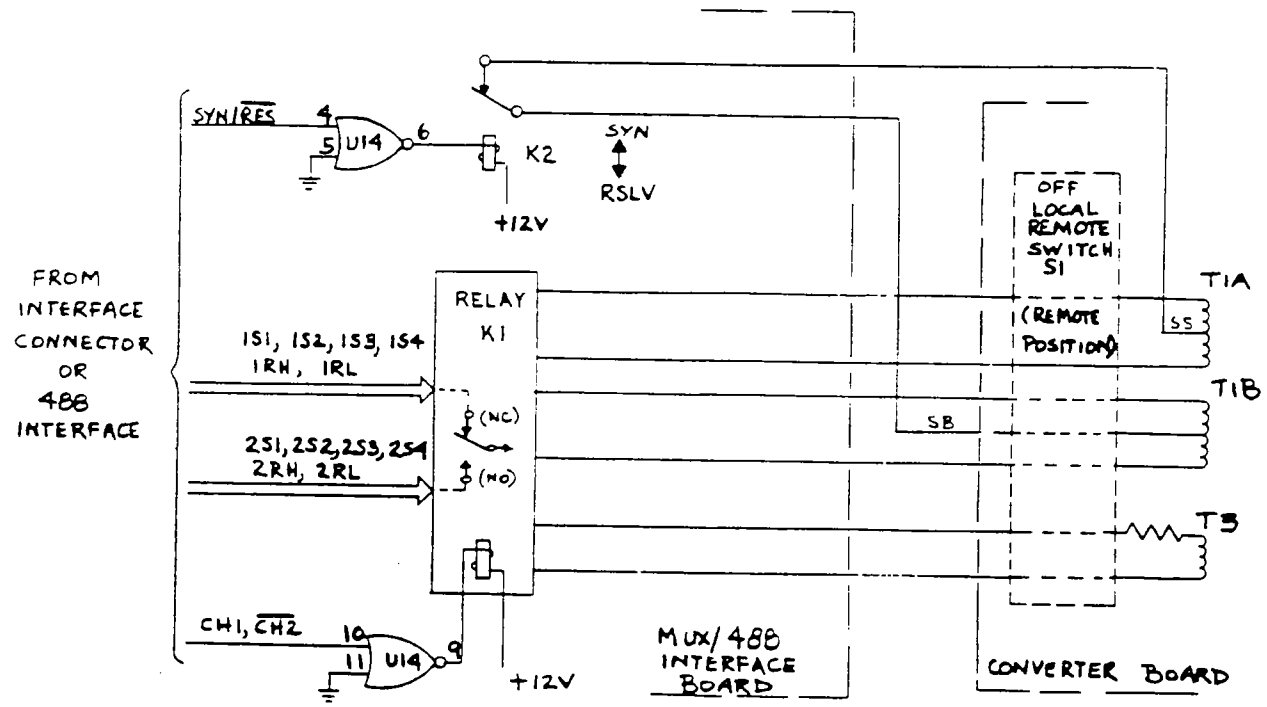
3.7.1 Local Input Channel Selection (See A, figure 3-5.)

When the LOC pushbutton is depressed, inputs S1A, S2A, S3A, S4A, SS, SA, RHA and RLA on the converter board are enabled. The four signal inputs and two reference inputs are wired back through the mux/488 interface board to the front panel binding posts marked S1, S2, S3, S4, RH, and RL. If the INPUT pushbutton switch is depressed to RSLV, input transformer taps SS and SA are left open, enabling 4-wire resolver operation. If the INPUT switch is depressed to SYN, the switch jumpers the two taps, configuring the input transformers for 3-wire synchro signals. The S4 binding post is not used for synchro operation.

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A. LOCAL MODE



B. REMOTE MODE

Figure 3-5. Input Channel Selection, Simplified Diagram

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3.7.2 Remote Input Channel Selection (See B, figure 3-5.)

When the REM pushbutton is depressed, inputs S1B, S2B, S3B, S4B, SS, SSB, RHB and RLB on the converter board are enabled. The four signal inputs and two reference inputs are connected to the output side of relay K1 on the mux/488 interface board. Relay K1 is controlled by the CH1/$\overline{\text{CH2}}$ signal derived from either the interface connector or the GPIB bus via the 488 interface. If a logic 1 (high) level is received on this line, it is inverted by NOR gate U14-9, energizing relay K1. This causes the 4-wire channel 2 resolver signals and associated reference to pass to the input transformers in the converter board. If a logic 0 level is received, relay K1 is deenergized, passing the six channel 1 inputs to the transformers.

The synchro/resolver configuration produced during remote operation is determined by the logic level on the SYN/RES line. If a logic 0 signal appears on this line, it is inverted by NOR gate U14-6 and relay K2 remains deenergized. As a result, transformer taps SS and SB are connected and the converter input transformers are configured to operate from 3-wire synchro inputs. If the SYN/$\overline{\text{RES}}$ logic level is high, the resulting logic inversion turns on relay K2 which opens the SS and SB leads. This conditions the input transformers for 4-wire resolver operation.

3.7.3 Local/Remote Selection of $\overline{\text{LT}}$, $\overline{\text{INH}}$, BW, and UB (See Figure 3-6.)

When the LOC switch is depressed, a logic 0 signal is routed to multiplexer U13, enabling the "1" inputs. This causes the front panel switches to control the logic inputs to the $\overline{\text{LT}}$ ($\overline{\text{lamp test}}$), $\overline{\text{INH}}$ ($\overline{\text{inhibit}}$), BW (bandwidth), and U/B (unipolar/bipolar) inputs of the tracking converter via the TTL buffer. If the LAMP TEST switch is depressed, ground (logic 0) is applied to the $\overline{\text{LT}}$ input of the converter board, causing all lamp segments to light. Depressing the INH switch passes a logic 0 through multiplexer U13 to the inhibit input of the converter. If the UNP/BIP switch is depressed to UNP, the logic 1 signal applied to input 1B of multiplexer U13 causes a logic 1 to appear at the UB input of the converter, producing unipolar operation. With the switch set to BIP, bipolar operation is effected. In a similar fashion, the BANDWIDTH switch selects either high bandwidth or low bandwidth operation.

When the REM switch is depressed, the "0" inputs to multiplexer U13 are enabled. This transfers control of the $\overline{\text{INH}}$, BW1, and U/B1 lines to the interface connector or the 488 interface. The $\overline{\text{LT1}}$ input is also enabled; however, lamp test may still be performed via the LAMP TEST switch since the switch bypasses the multiplexer.

3.8 POWER SUPPLY CIRCUITS (See Figure 3-7.)

Primary power is routed through fuse F1 in the mux/488 interface board, then passes to the OFF switch in the converter board. If the front panel LOC or REM switch is in its depressed position, the OFF switch contacts pass the AC power to a self-contained power supply on the converter board.

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Switched AC power from the converter board passes to power transformer T1 in the mux/488 interface board. The transformer drives a full wave bridge rectifier circuit (CRA1, VR1, C13 and C15) located in the voltage regulator assembly. (See sheet 1 of figure 4-1.) This assembly supplies +12V and +5V for the mux/488 interface board.

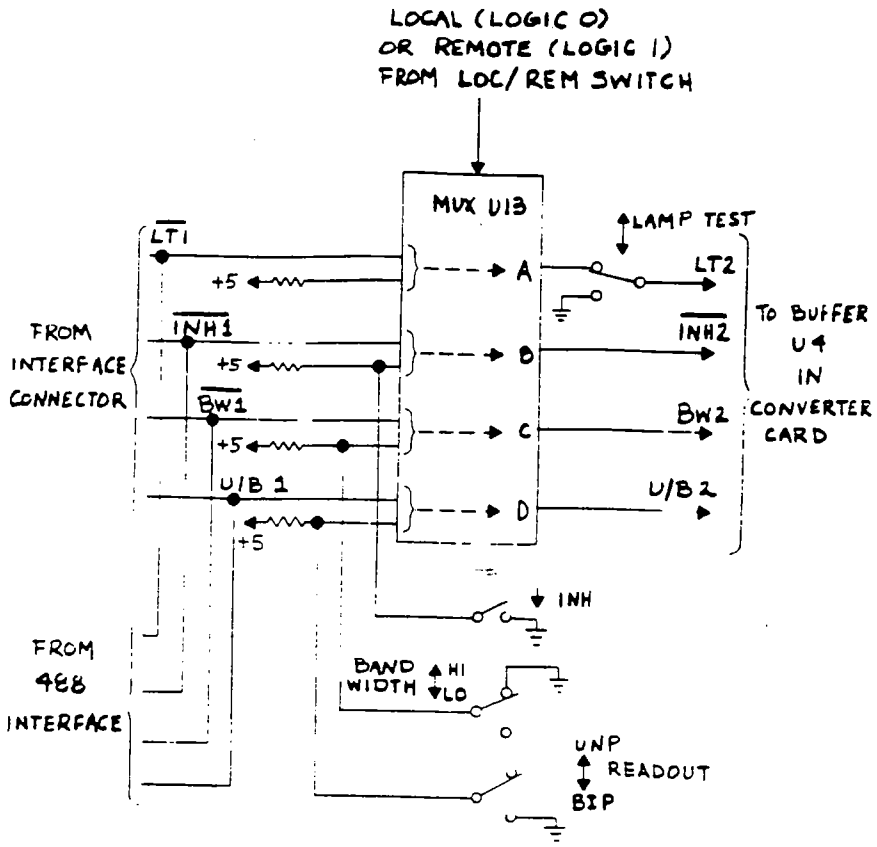


Figure 3-6. Selection of Lamp Test, Inhibit, Bandwidth and Unipolar Control Lines

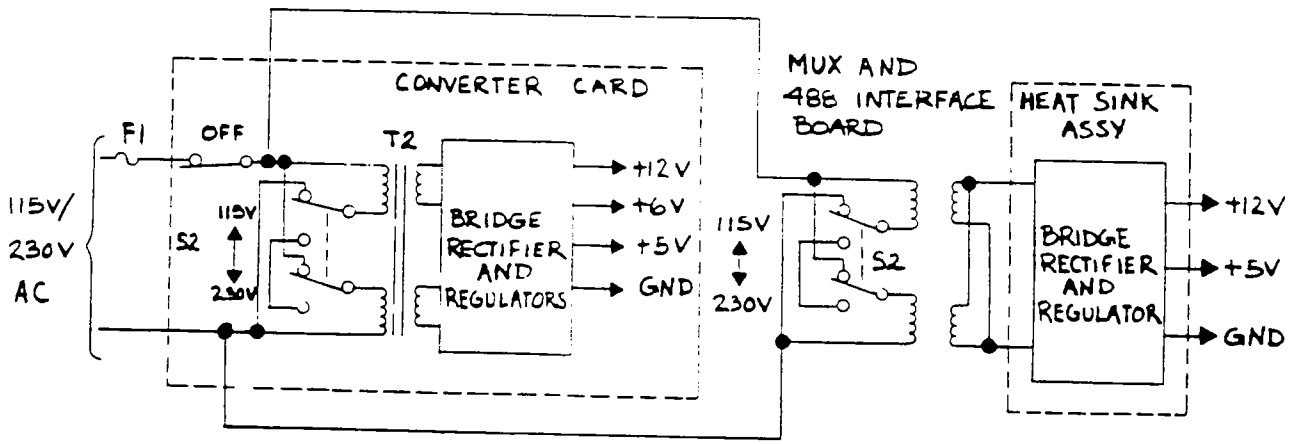


Figure 3-7. Power Supplies and Power Distribution

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SECTION 4

MAINTENANCE

4.1 GENERAL

This section contains procedures and data that will help ensure continuity of service of the instrument. Personnel involved in maintaining the equipment should be familiar with its physical make-up and principles of operation before attempting to troubleshoot it. THERE ARE NO CALIBRATION ADJUSTMENTS.

4.2 PREVENTIVE MAINTENANCE

At 6-month intervals, clean the exterior of this instrument with a soft brush or cloth. No other preventive maintenance is required.

4.3 PERFORMANCE EVALUATION AND CALIBRATION TEST

Table 4-1 provides a procedure that may be used as a routine calibration test of the converter in a new unit. A 400 Hz source (such as an oscillator and amplifier) that is capable of delivering an RMS voltage of at least 10 volts is required.

4.3.1 Local Mode Test

Depress the LOC pushbutton switch to place the instrument in local mode. In each step of Table 4-1, short the designated front panel binding posts and apply the 400 Hz signal input to the binding posts shown. Depress the READOUT switch to the UNP position. For synchro inputs, depress the INPUT pushbutton to the SYN position; for resolver inputs, depress it to RSLV. The instrument should display the angle shown within its rated accuracy ($\pm.03°$ for the Model SR-203 and $\pm.005°$ for the Model HSR-103). The reference voltage must be derived from the same 400 Hz source as the signal. Depress and hold the LAMP TEST pushbutton to verify that the LED segments are all on. Depress and hold the INHIBIT switch and verify that the display is frozen.

4.3.2 Remote Mode Test

The same test may be performed in remote mode to verify the operational status of the remote controlled circuits in the instrument. In this case, apply the synchro/resolver inputs and required control signals to INSTRUMENT INTERFACE connector J1 on the rear panel. Refer to Table 2-1 for the pinout of connector J1. Apply the proper logic

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signals to condition the instrument for unipolar operation, synchro/resolver signals, and channel 1 operation, then depress the REM pushbutton switch. In each step of Table 4-1, short the designated input leads and apply the 400 Hz input signal to the channel 1 input connections. Repeat the remote test for channel 2. Accuracy of the displayed angle should be the same as that specified above for the local mode.

4.4 CORRECTIVE MAINTENANCE

Corrective maintenance consists of procedures designed to correct problems that have caused the instrument to malfunction. Corrective maintenance procedures include troubleshooting, repair, and replacement. No adjustments are required for this instrument.

4.4.1 Test Equipment Required

A good general purpose dual-channel oscilloscope, VTVM, 400-Hertz oscillator and a synchro equipped with a calibrated dial are required for corrective maintenance.

4.4.2 Troubleshooting

Table 4-2 is included to facilitate troubleshooting. The table does not include all possible faults that may occur but it does provide a systematic logical approach to trouble localization and indicates areas that should be checked. Using this data as a guide, in conjunction with the overall schematic diagram of figure 4-1 and the wiring data in Table 4-4, it should be possible to localize equipment malfunctions to the level of a replaceable part. Signal values are defined in Table 4-3.

When troubleshooting, one channel of the oscilloscope should be synchronized to the reference voltage. One cycle of the reference should be set up as a time base against which the magnitude and phase of signals developed in the instrument can be compared.

All IC's, except U5 and U6 on the converter board, are plugged into sockets, simplifying their replacement. Normal CMOS handling procedures should be observed when changing any of the CMOS IC's.

Maintenance of the 488 interface circuits in the field is limited since its programmed operations occur under control of the IEEE bus controller and the stored internal program. Check that the power supply on the heat sink assembly is delivering +5 volts.

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Table 4-1. Test Summary

Signal Type	Shorted Input Leads	Input Connections Hi	Input Connections Lo	Display
Synchro	S1, S3	S1/S3	S2	180.00° *
		S2	S1/S3	000.00° *
	S2, S3	S1	S2/S3	240.00° *
		S2/S3	S1	60.00° *
	S1, S2	S3	S1/S2	120.00°
		S1/S2	S3	300.00°
Resolver	S2, S3, and S1, S4	S2/S3	S1/S4	45.00°
		S1/S4	S2/S3	225.00°
	S1, S2, and S3, S4	S1/S2	S3/S4	315.00° *
		S3/S4	S1/S2	135.00° *

Table 4-2. Troubleshooting Chart

Trouble	Corrective Action
A. No display in either local or remote mode or abnormal display with instrument inhibited	Check the following: 1. Fuse F1 2. AC power 3. Settings of 115V/230V switches 4. Power supplies (see troubles B and C) 5. Clock U15, counter U23 and multiplexer switches U7 through U11 on converter board. 6. Driver U12, decoder U13, and resistor network R1 in converter board display circuits. 7. LED displays DS1-DS6 (or DS7 in HSR-203)
B. Abnormal power supply voltages on converter board	Check the following: 1. AC voltage across primary winding of T2 2. DC voltage across C1 and C2. 3. Outputs of U5 and U6 with U1 and U2 removed.

*Revised 12/82

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Table 4-2. Troubleshooting Chart (Cont'd.)

Trouble	Corrective Action
C. Abnormal power supply voltages on mux/488 interface board	Check the following: 1. AC voltage across primary winding of T1. 2. DC voltage across C13 (on heat sink assembly). 3. DC voltage across C15 (on heat sink assembly).
D. Incorrect display angle	Check the following on the converter board: 1. Measure DC voltage at V. If abnormal, remove U2 and recheck voltage. If it is now normal, replace U2. 2. Check voltages at ±S and ±C. If abnormal, remove U1 and recheck. If voltages are now normal, replace U1. 3. Inhibit converter, change input angle, and check voltages at e and e'. a. If signal at e is abnormal, replace U1. b. If signal at e is normal, but signal at e' is abnormal, check signals at C and D. c. If signals at C and D are normal, replace U2. d. If signals at C and D are abnormal, replace U1. 4. Remove U2 and check signal at R. If signal at R is normal, and signals at e', C and D are normal, replace U2.
E. Display is unstable (jitter)	1. Check that input signals are at proper levels. 2. Set bandwidth control to low bandwidth.
F. Abnormal TTL outputs	1. Check +5V supply in converter board. 2. Check TTL buffers U17 through U22 in converter board.

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Table 4-2. Troubleshooting Chart (Cont'd.)

Trouble	Corrective Action
G. Abnormal display in remote mode (for both synchro and resolver inputs)	Check relay K1 and NOR gate U14-9 on mux/488 interface board.
H. Abnormal display in remote mode for either synchro or resolver inputs	Check relay K2 and NOR gate U14-6 on on mux/488 interface board.
I. Failure to control lamp test, inhibit, bandwidth and/or read-out mode in remote mode	Check multiplexer U13 in mux/488 interface board.

Table 4-3. Signal Values (Converter Board)

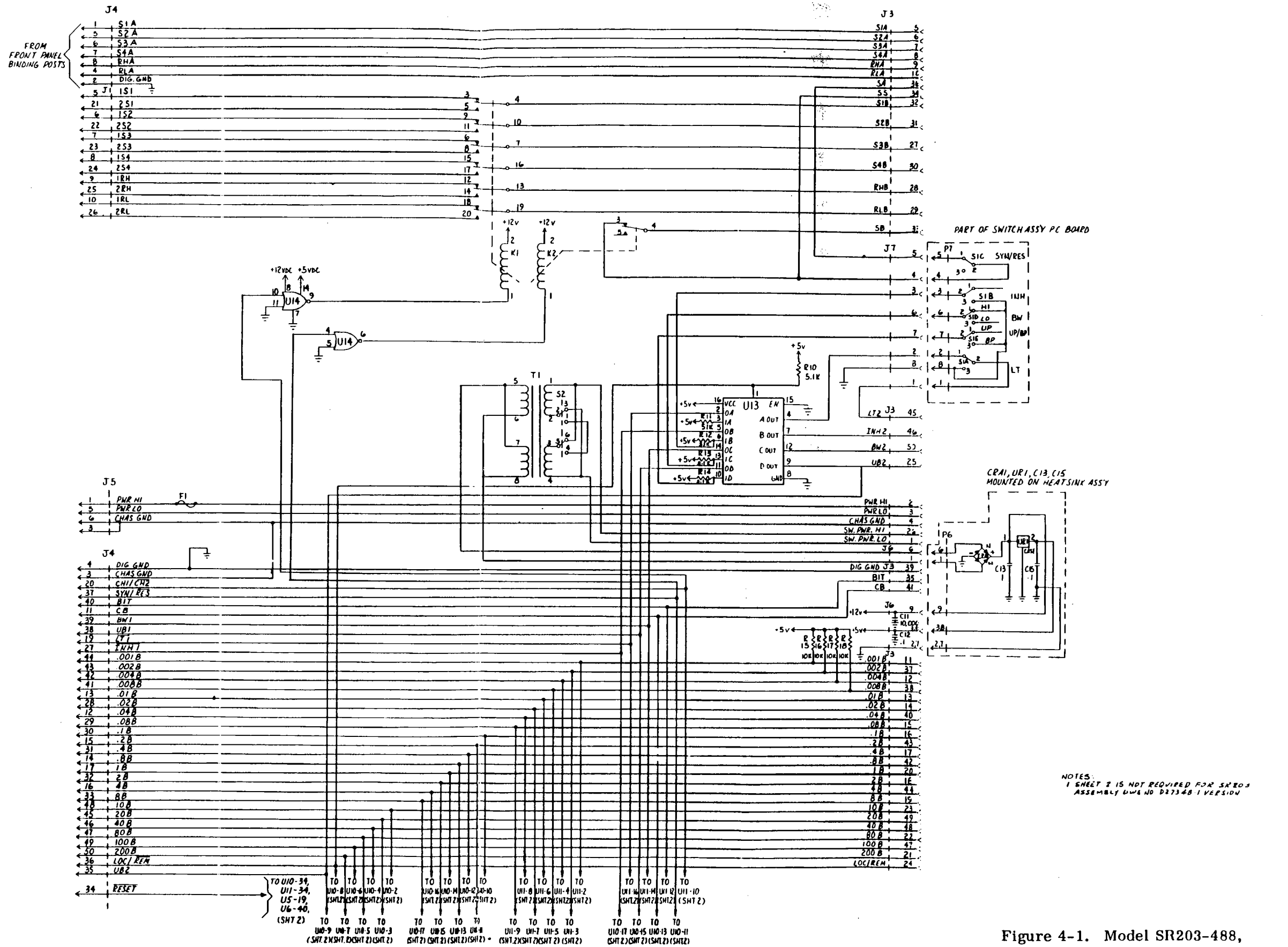
Signal	Value
V	+6 ± 0.6V DC
R	6V peak @ 115V ref with U2 removed (distorted sine wave)
e	20 mV peak/0.1° @ 90V L-L
e'	200 mV peak/0.1° @ 90V L-L (for HSR-103, 2V RMS peak/0.1°)
C	0-0.7V RMS @ 90V L-L (depending on angular error)
D	0-0.7V RMS @ 90V L-L (depending on angular error)
+S	0-2V RMS @ 90V L-L (depending on input angle)
-S	0-2V RMS @ 90V L-L (depending on input angle)
+C	0-2V RMS @ 90V L-L (depending on input angle)
-C	0-2V RMS @ 90V L-L (depending on input angle)

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Table 4-4. Interboard Harness Assy, Wiring List

From Mux Bd A1P1	To Converter Bd A2P1	From Mux Bd A1P1	To Converter Bd A2P1
1	37	26	36
2	1	27	23
3	2	28	25
4	3	29	26
5	5	30	24
6	6	31	22
7	7	32	21
8	8	33	18
9	9	34	35
10	10	35	40
11	44	36	34
12	42	37	43
13	13	38	41
14	28	39	4
15	29	40	12
16	30	41	11
17	31	42	14
18	32	43	15
19	33	44	16
20	17	45	38
21	50	46	27
22	47	47	49
23	48	48	46
24	19	49	45
25	39	50	20

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NOTES:
1 SHEET 2 IS NOT REQUIRED FOR SR203 ASSEMBLY DWG NO D27348 1 VERSION

Figure 4-1. Model SR203-488, Schematic Diagram (Sheet 1 of 3)

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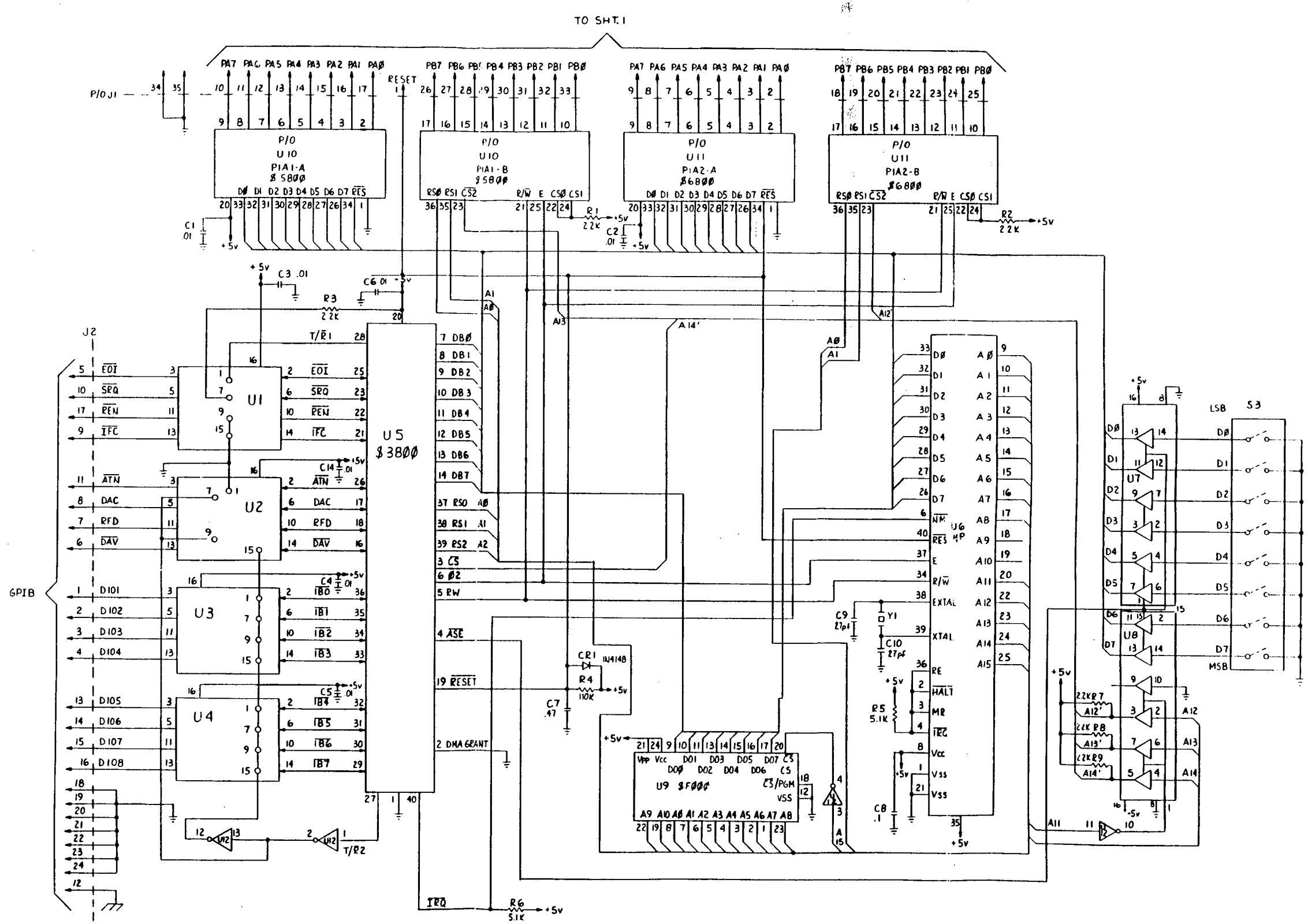


Figure 4-1. Model SR203-488, Schematic Diagram (Sheet 2 of 3)

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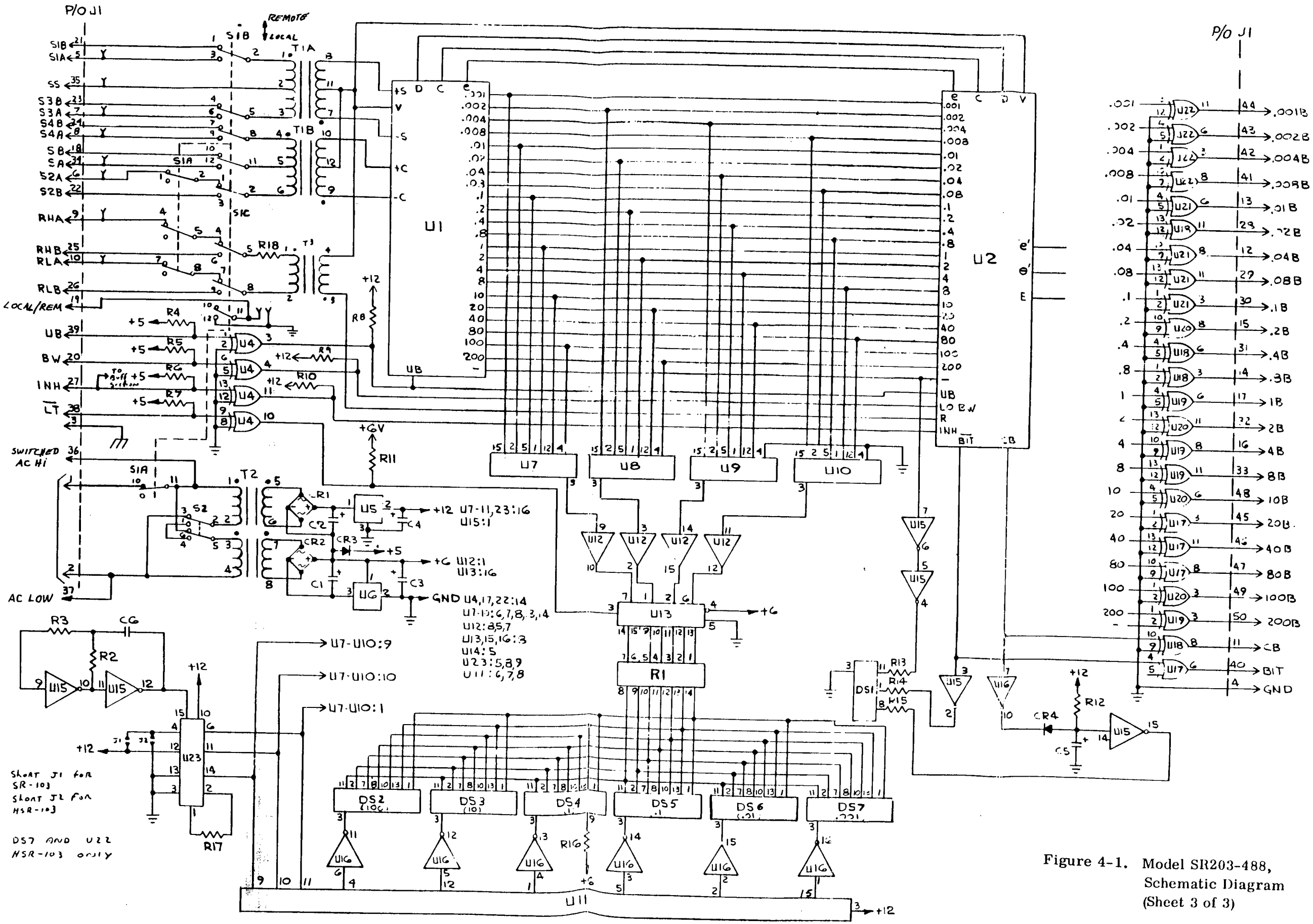


Figure 4-1. Model SR203-488, Schematic Diagram (Sheet 3 of 3)

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SECTION 5

PARTS LIST

5.1 GENERAL

This section contains the parts list (Tables 5-1 through 5-7) for the Models SR-203, HSR-203, SR203-488, and HSR203-488. Each maintenance significant part is identified by reference symbol, part number and manufacturer. For each part, the tables also include a reference to a figure that shows its physical location in the instrument.

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Table 5-2. SR203-488 and HSR203-488 Parts List

Reference Symbol	Part No.	Description	Man	Qty	Figure
--	D27348-2	Mux-488 Interface Board	DDC	1	1-3
--	A27884-1* A27884-2**	Converter Board Assy	DDC	1	1-2
--	C27678	SR-203/HSR-203 Voltage Reg Assy	DDC	1	1-3
	D27888	SR-203 Interboard Harness Assembly	DDC	1	1-2
	C27889	SR-203 Harness, Rear Panel	DDC	1	
	C7890	SR-203 Harness, Front Panel	DDC	1	
J1-J6	111-0110-001	Binding Posts, Blue	EF Johnson	6	1-1
J7	111-0103-001	Binding Posts, Black	EF Johnson	1	1-1
J8	137	Binding Post	H.H. Smith	1	1-1
--	17-10500-1-390	Receptacle	Amphenol	1	1-4
--	17-314-01	Cable Housing	Amphenol	1	1-4
--	17250	Line Cord	Belden	1	1-4

*Used in Model SR203-488.
**Used in HSR203-488.

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A.6 3-WIRE HANDSHAKE PROCEDURE

The 3-wire handshake procedure, repeated for each byte transferred from a source to one or more acceptors, ensures that each listener is ready to accept data, that the information on the data lines is valid, and that the data has been accepted by all listeners. The DAV line is controlled by the source (talker); the NDAC and NRFD lines are controlled by the acceptors (listeners).

Figure A-2 illustrates the handshake cycle for a source and several acceptors.

a. Both source and acceptors start in a known state. The source initializes DAV to high (false, data not valid) and the acceptors initialize NRFD to low (true, none are ready for data) and NDAC to low (true, none have accepted the data).

b. The source checks that both NRFD and NDAC are not high, then places the first data byte on the DIO lines. (If both lines are sensed high, the error condition ends the procedure.)

c. When all acceptors are ready to accept the first data byte, NRFD goes high.

d. After data is settled and valid and the source has sensed NRFD high, it sets DAV low (data is valid).

e. The first acceptor sets NRFD low then accepts the first byte. The other receptors follow suit at their own rates.

f. Each acceptor sets NDAC high to indicate that it has accepted.

g. When NDAC is sensed high by the source (after all acceptors have accepted the data byte), it sets DAV high (data on DIO lines no longer valid). At this point, one data byte transfer has been completed.

h. Upon sensing DAV high, the acceptors set NDAC low.

i. Source and acceptor initial conditions are now reestablished and the next handshake cycle may be initiated.

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Table 5-3. Parts List for Multiplexer Board (D27348-1)
and Multiplexer/488 Interface Board (D27348-2) (Cont'd.)

Reference Symbol	Part No.	Description	Man	Qty	Figure
K1	T10-E2-Y6-12VDC	Relay, 6PDT, 12V	P & B	1	1-1
K2	T10-E2-Y2-12VDC	Relay, DPDT, 12V	P & B	1	1-1
R1*-R3*, R7*-R9*	RCR07G222JS	Resistor, 2.2K, 5%, 1/4W		6	1-1
R4*	RCR07G114JS	Resistor, 110K, 5%, 1/4W		1	1-1
R5*, R6*, R10-R14	RCR07G512JS	Resistor, 5.1K, 5%, 1/4W		7	1-1
R15-R18	RCR07G103JS	Resistor, 10K, 5%, 1/4W		4	1-1
S2	46256LFR	Switch, slide	Switchcraft	1	1-1
S3*	76PB08	Switch, SPDT, Edge Mounted	Grayhill	1	1-1
T1	DCP-20-1200	Transformer, 115V/230V Pri, 10/20V Sec, 24 VA	Signal	1	1-1
U1-U4*	MC3448AP	IEEE Bus Driver	Motorola	1	1-1
U5*	MC68488P	GPIA		1	1-1
U6*	MC6802P	Microprocessor		1	1-1
U7, U8*	DM70L97J	Tri-state Hex Buffer		2	1-1
U9*	CP27677A	EPROM, 2716, (Programmed for SR/HSR203-488), 2K X 8	DDC	1	1-1
U10, U11*	MC6821P	PIA		2	1-1
U12*	74LS04N	Hex Inverter		1	1-1

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Table 5-3. Parts List for Multiplexer Board (D27348-1) and Multiplexer/488 Interface Board (D27348-2)

Reference Symbol	Part No.	Description	Man	Qty	Figure
C1*-C6*, C14*	VP22BY103MB	Capacitor, ceramic, .01 uf, 20%, 100V	Vitramon	7	1-1
C7*	VP23BY474KB	Capacitor, ceramic, 0.47 uf, 10%, 100V	Vitramon	1	1-1
C8, C12	VP22BY104MB	Capacitor, ceramic, 0.1 uf, 20%, 100V	Vitramon	2	1-1
C9*, C10*	VP22BY270Kb	Capacitor, ceramic, 27 pf, 10%, 100V	Vitramon	2	1-1
C11	16ELA10000	Capacitor, electrolytic, 10,000 uf, 16V, +50 -10%	Nichicon	1	1-1
CR1	1N4148	Diode, silicon		1	1-1
F1	GMW-1	Fuse, 1A	Buss	1	1-4
J1	205869-1	Connector, Plug, 50 Pin	Amp	1	
J2*	552791-2	Connector, 24 Pin	Amp	1	
J3	65781-061	Connector, Vertical Card, 50-Pin	Berg	1	1-1
J4, J5	65614-136	Dual Straight Header, 36 Position	Berg	1	1-1
J6	65781-041	Connector, Vertical Card, 10 Pin	Berg	1	1-1
J7	75290-108	Connector, Vertical Card, 8 Pin	Berg	1	1-1

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Table 5-4. Parts List for SR-203 Converter Board (A27884-1) and HSR-203 Converter Board (A27884-2)

Reference Symbol	Part No.	Description	Man	Qty	Figure
C1	25ELA2200	Capacitor, tant, 2200 uf, 25V DC	Nichicon	1	5-2
C2	25ELA470	Capacitor, tant, 470 uf, 25V DC	Nichicon	1	5-2
C3	16ULA10-1	Capacitor, electrolytic, 10 uf, 10V DC, +50 -10%	Nichicon	2	5-2
C4, C5	50ULAI.0	Capacitor, electrolytic, 1 uf, 50V DC	Nichicon	1	5-2
C6	CK05BX102M	Capacitor, cer, 1000 pf ±20%, 100V		1	5-2
C7	16ULA100	Capacitor, electrolytic, 100 uf, 16V DC	Nichicon	1	5-2
CR1, CR2	KBP02	Diode bridge	GI	2	5-2
CR3, CR4	1N4148	Diode		2	5-2
DS1-DS7*	5082-7653 Cat B	Display, 7 segment	Hewlett Packard	7*	5-2
J1	205869-1	Connector, plug, 50-pin	Amp	1	5-2
RA1	899-3-R100	Resistive network, 14-pin dip	Beckman	1	5-2
R2, R12, R17	RCR07G204JS	Resistor, 200K, 5%, 1/4W		3	5-2
R3	RCR07G205JS	Resistor, 2 Meg, 5%, 1/4W		1	5-2
R4-R7	RCR07G103JS	Resistor, 10K, 5%, 1/4W		4	5-2

*DS7 not used in SR-203.

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Table 5-3. Parts List for Multiplexer Board (D27348-1) and Multiplexer/488 Interface Board (D27348-2) (Cont'd.)

Reference Symbol	Part No.	Description	Man	Qty	Figure
U13	54LS157J	Quad 2-Line to 1-Line Mux		1	1-1
U14	UHP-233	Quad, 2-Input NOR Power Driver	Sprague	1	1-1
XF1	HWA-AF	Fuseholder	Buss	1	1-1
XU1-XU4, XU7, XU8, XU13	640358-3	IC Socket, 16-Pin	Amp	7	1-1
XU5, XU6, XU10, XU11	640379-3	IC Socket, 40-Pin	Amp	4	1-1
XU9	640361-3	IC Socket, 24-Pin	Amp		1-1
XU12, XU14	640357-3	IC Socket, 14-Pin	Amp		1-1
Y1*	SCM18, 4.0 MHz	Crystal, 4.0 Mhz	Sentry	1	1-1
	B27387	SR-203 Switch Subassy	DDC	1	1-1
	D27347	PC Board, Double	DDC	1	1-1

*Not included in Multiplexer Board (D27348-1).

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Table 5-4. Parts List for SR-203 Converter Board (A27884-1) and HSR-203 Converter Board (A27884-2) (Cont'd.)

Reference Symbol	Part No.	Description	Man	Qty	Figure
U12	CD4050AE	CMOS Hex buffer	RCA	1	5-2
U13	4511B	CMOS BCD to 7-segment decoder/driver		1	5-2
U15	CD4049BE	CMOS Hex buffer	RCA	1	5-2
U16	9666PC	Darlington Transistor Array	Fairchild	1	5-2
U17-U22*	74LS86	Quad exclusive OR gate		1	5-2
U23	4516B	4-Bit Binary Counter		1	5-2
XU4, XU17-XU22*	14-810-90	14 Pin Dip Socket	Aries	7	5-2
--	D21419	Double PC Board	DDC	1	5-2

*U22 and XU22 not used in SR-203.

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Table 5-4. Parts List for SR-203 Converter Board (A27884-1) and HSR-203 Converter Board (A27884-2) (Cont'd.)

Reference Symbol	Part No.	Description	Man	Qty	Figure
R8-R11	RCR07G303JS	Resistor, 30K, 5%, 1/4W		4	5-2
R13-R15	RCR07G102JS	Resistor, 1 K ohms, 5%, 1/4W		1	5-2
R16	RCR07G201JS	Resistor, 200 ohms, 5%, 1/4W		1	5-2
R18	RCR07	Resistor, 110K, 5%, 1/4W		1	5-2
S1 (A, B, C)	3GA15FA101 BLK/AMBER	Switch, pushbutton	IEE Shadow	1	5-2
S2	46256LFR	Switch, slide	Switchcraft	1	5-2
T1	C21359	Synchro/Resolver Input Transformer Pair	DDC	1	5-2
T2	A21357	Power Transformer	DDC	1	5-2
T3	C24014	Reference Transformer	DDC	1	5-2
U1	D21405-1 D21405-2*	Solid State Control Transformer	DDC	1	5-2
U2	D21431-1 D21431-2*	Error Processor and Up-Down Counter	DDC	1	5-2
U4	74L86N	Quad exclusive OR gate		1	5-2
U5	UA78L12AHC	Pos. Voltage Regulator	Fairchild	1	5-2
U6	UA79M6HC	Neg. Voltage Regulator	Fairchild	1	5-2
U7-U11	40518	CMOS Analog mux/demux 8 channel		5	5-2

* Component part number for HSR-203 units.

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Table 5-6. SR-203 Switch Subassembly (B27387), Parts List

Reference Symbol	Part No.	Description	Man	Qty	Figure
--	B27386	Board, single	DDC	1	5-1
P7	65516-108	Header, Straight, 8 positions	Berg	1	5-1
S1	5G15FA101 BKBL2UEEF	Switch, 5-Sta, 2 Pole, 3 P-P, 4 and 5 Mom	IEEE/SH	1	5-1

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Table 5-5. SR-203/HSR-203 Voltage Regulator Subassy Parts List

Reference Designation	Part No.	Description	Man	Qty	Figure
C13	A105A	Capacitor, tant, 1.0 uf, 20%, 100V	Comp	1	5-3
C15	VP22BY104MB	Capacitor, ceramic, 0.1 uf, 20V, 100V	Vitramon	1	5-3
CRA1	VH148	Diode Bridge, Silicon	Varo	1	5-3
P6	65043-032	Housing, Mini	Berg	1	5-3
	48116	Gold Plated Pin, Male Crimped	Berg	9	5-3
VR1	LM323K	Voltage Regulator, +5V, 3A, T0-3	National	1	5-3
XVR1	P080-1G4	Socket, T0-3	Augat	1	5-3

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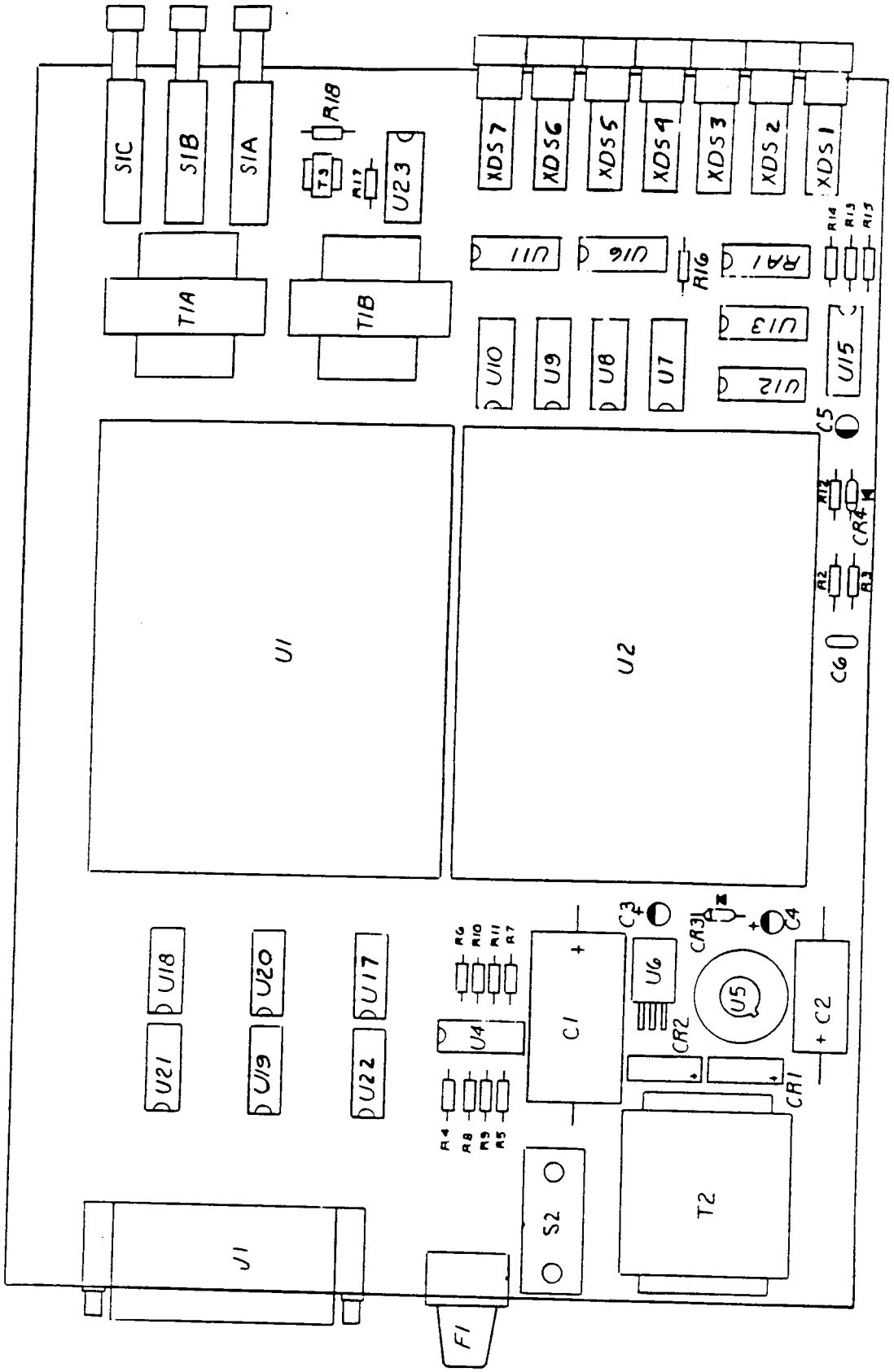


Figure 5-1. SR-203 Converter Board (A27884-1) and HSR-203 Converter Board (A27884-2), Parts Location

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Table 5-7. Inter-Board Harness Assembly Parts List

Reference Symbol	Part No.	Description	Man	Qty	Figure
A1P1	48116	Gold plated pin	Berg	50	5-4
	65043-012	Housing, mini-latch	Berg	1	5-4
A2P1	17-10500-1-390	Receptacle	Amphenol	1	5-4
	17-314-01	Housing, Cable	Amphenol	1	5-4
	205980-1	Screw, Retainer-Male	Amp	2	5-4

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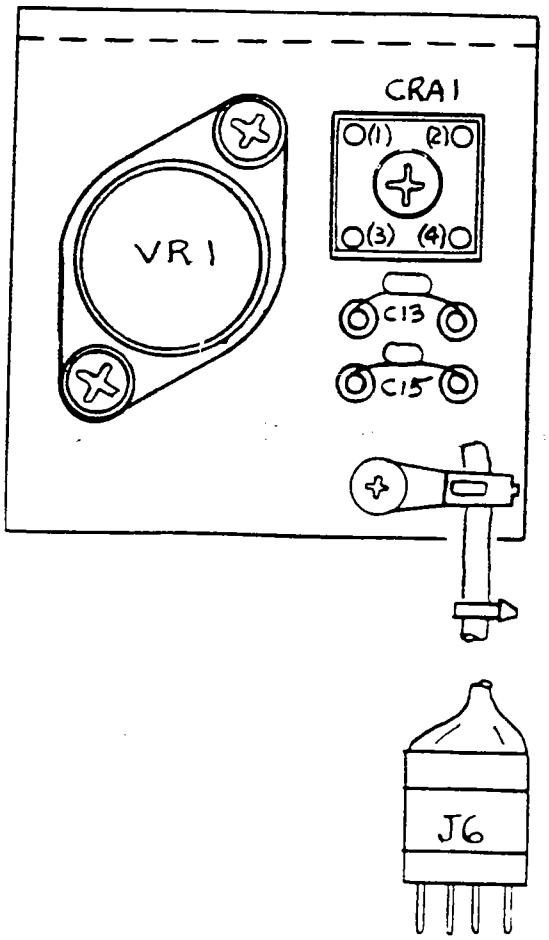


Figure 5-3. SR-203/HSR-203 Voltage Regulator Subassembly, Parts Location

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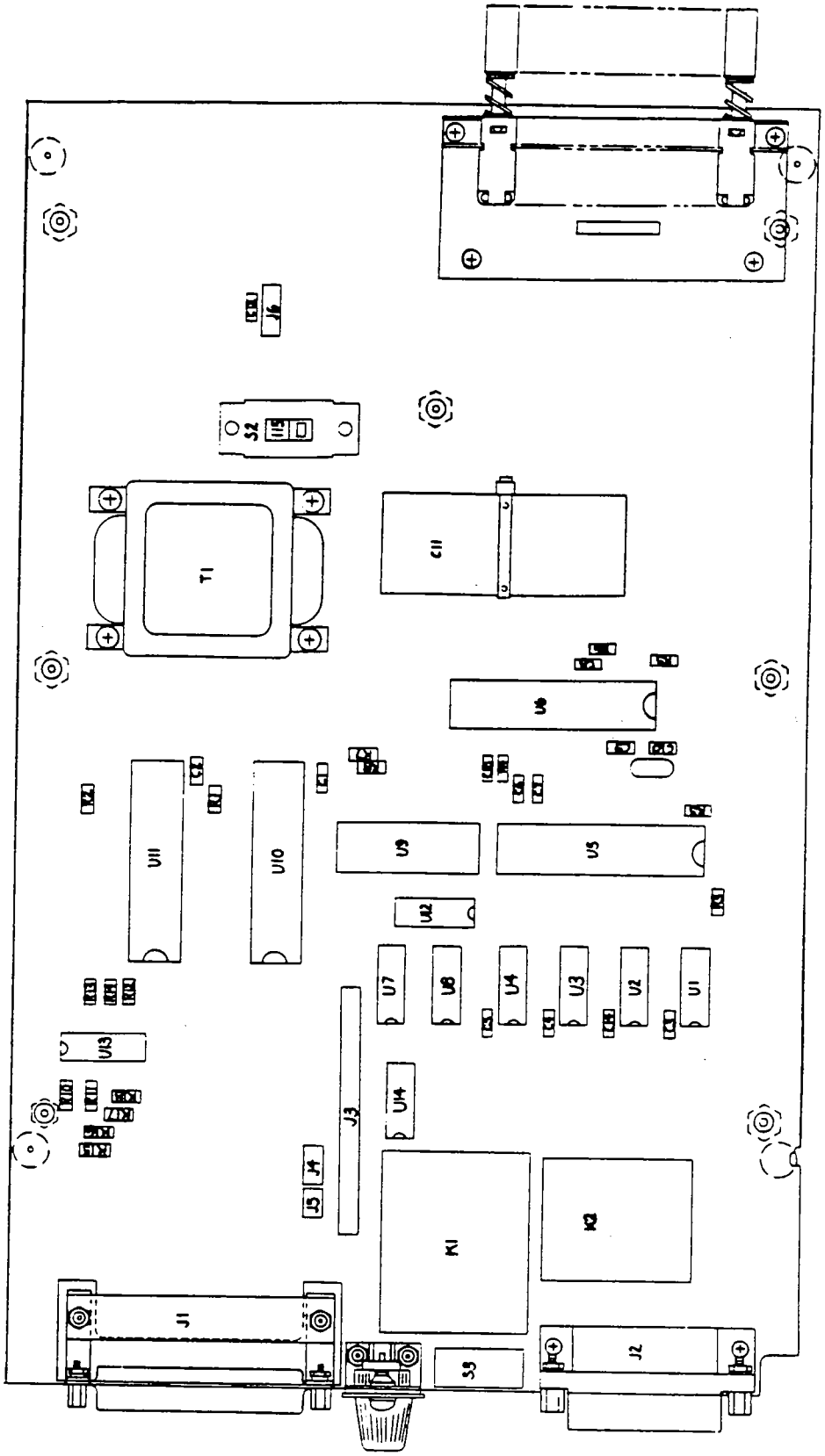


Figure 5-2. Multiplexer Board (D27348-1) and Multiplexer/488 Interface Board (D27348-2), Parts Location

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APPENDIX

THE IEEE-488 GPIB

A.1 INTRODUCTION

The following abbreviated description of the IEEE-488 GPIB is included for reference. For complete bus details, consult IEEE Standard 488-1975 Digital Interface for Programmable Instrumentation. Copies of IEEE 488-1975 may be purchased from the IEEE (Institute of Electrical and Electronics Engineers) or from the American National Standards Institute, both of which are located in New York, N. Y.

A.2 BASIC STRUCTURE AND CONSTRAINTS

The GPIB is a byte-serial bit-parallel interface system. It is structured with 16 lines consisting of the following:

a. Eight data bus lines for transmission of ASCII characters. Data is asynchronous and generally bidirectional.

b. Five bus management (control) signal lines.

c. Three data byte transfer control lines (handshake).

The system includes constraints on the number of devices, data rate, total transmission length, and is confined to exchange of digital data.

A.3 BASIC BUS TERMINOLOGY

a. Controller - A device that can address other devices to listen or to talk.

b. Listener - A device that can be addressed through the bus to receive messages from another device or the controller via the bus.

c. Talker - A device that can be addressed through the bus to transmit messages to another device or the controller via the bus.

NOTE

Controller, listener, and talker capabilities may occur individually and collectively in devices interconnected by the GPIB. (See fig. A-1.)

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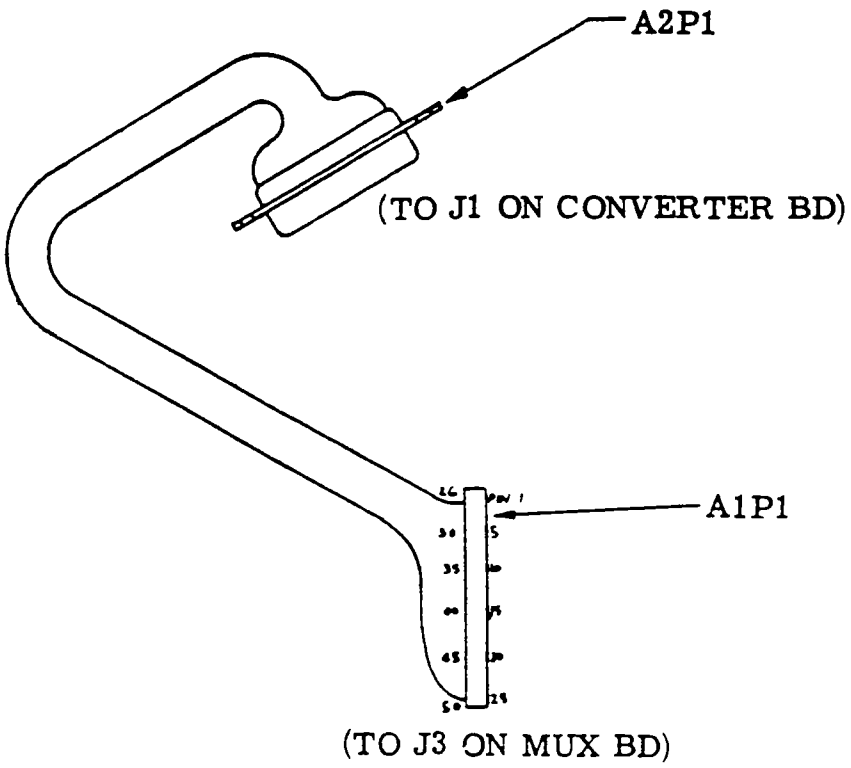


Figure 5-4. Interboard Harness Assembly, Parts Location

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A.4 INTERFACE BUS SIGNALS

NOTE

The IEEE Standard 488-1975 is defined for a negative logic format:

Logic 0 = False = High ($\geq$2.0V)
Logic 1 = True = Low ($\leq$0.8V)

a. EOI (End or Identify). True level on this bus management (control) line indicates end of multiple byte transfer. When used with ATN, performs parallel polling sequence.

b. SRQ (Service Request). Device sets this control line true when it requires service from the interface controller.

c. REN (Remote Enable). This controller driven line is used with other messages to select source of device programming data (e.g., front panel or interface control).

d. IFC (Interface Clear). This controller driven line is set true to place all bus-connected devices in their idle states.

e. ATN (Attention). This control line specifies how data on the data lines are to be interpreted and which devices must respond to the data. When ATN is true, the DI01-DI08 lines carry addresses or commands. When ATN is set false, the data lines carry data.

f. NDAC (Not Data Accepted). When set false by a device, this handshake line indicates that data has been accepted.

g. NRFD (Not Ready for Data). When set false by a device, this handshake line indicates that the device is ready to accept data.

h. DAV (Data Valid). When set true, this handshake line indicates that information on the data lines is available and valid.

i. DI01-DI08 (Data Input-Output). These lines carry data in bit-parallel, byte-serial form. Information on the lines represents either address/commands or data, depending on the logic state of the ATN line.

j. Unlisten Command. This command is transmitted on the data lines in conjunction with ATN true to terminate the device listen function.

k. Untalk Command. This command is transmitted on the data lines in conjunction with ATN true to terminate the device talk function.

A.5 REMOTE MESSAGE CODING

Table A-1 shows the coding of some of the control messages transmitted on the IEEE bus. The 1 and 0 designations refer to the logic states (negative logic convention). X = don't care. A1-A5 specify the five address bits set within the device by the address select switches.

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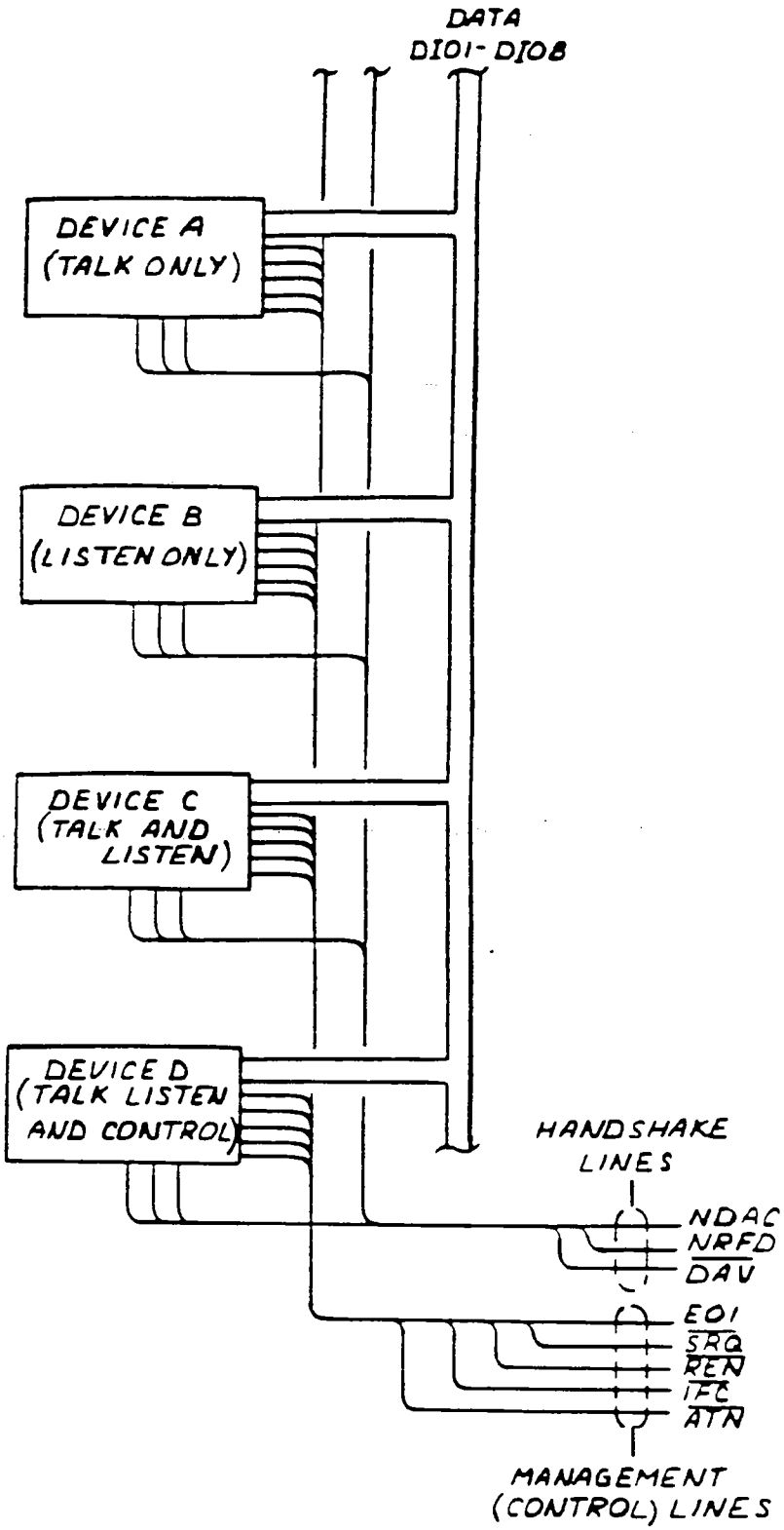


Figure A-1. Interface Connections and Bus Structure

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A.6 3-WIRE HANDSHAKE PROCEDURE

The 3-wire handshake procedure, repeated for each byte transferred from a source to one or more acceptors, ensures that each listener is ready to accept data, that the information on the data lines is valid, and that the data has been accepted by all listeners. The DAV line is controlled by the source (talker); the NDAC and NRFD lines are controlled by the acceptors (listeners).

Figure A-2 illustrates the handshake cycle for a source and several acceptors.

a. Both source and acceptors start in a known state. The source initializes DAV to high (false, data not valid) and the acceptors initialize NRFD to low (true, none are ready for data) and NDAC to low (true, none have accepted the data).

b. The source checks that both NRFD and NDAC are not high, then places the first data byte on the DIO lines. (If both lines are sensed high, the error condition ends the procedure.)

c. When all acceptors are ready to accept the first data byte, NRFD goes high.

d. After data is settled and valid and the source has sensed NRFD high, it sets DAV low (data is valid).

e. The first acceptor sets NRFD low then accepts the first byte. The other receptors follow suit at their own rates.

f. Each acceptor sets NDAC high to indicate that it has accepted.

g. When NDAC is sensed high by the source (after all acceptors have accepted the data byte), it sets DAV high (data on DIO lines no longer valid). At this point, one data byte transfer has been completed.

h. Upon sensing DAV high, the acceptors set NDAC low.

i. Source and acceptor initial conditions are now reestablished and the next handshake cycle may be initiated.

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TABLE A-1. MESSAGE CODING

Message	I/O Data								Handshake			Control				
	DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01	DAV	NRFD	NDAC	ATN	EOI	SRQ	IFC	REN
ATN (Attention)	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X
Data Byte	D8	D7	D6	D5	D4	D3	D2	D1	X	X	X	X	X	X	X	X
DAV (Data Available)	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X
NRFD (Not Ready for Data)	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X
NDAC (Not Data Accepted)	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X
DCL (Device Clear)	X	ø	ø	1	ø	1	ø	ø	X	X	X	X	X	X	X	X
End	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X
Go to Local	X	0	0	0	0	0	0	1	X	X	X	X	X	X	X	X
Identify	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X
IFC (Interface Clear)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X
MLA (My Listen Address)	X	ø	1	A5	A4	A3	A2	A1	X	X	X	X	X	X	X	X
MTA (My Talk Address)	X	1	ø	A5	A4	A3	A2	A1	X	X	X	X	X	X	X	X
REN (Remote Enable)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
SRQ (Service Required)	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X
Unlisten	X	ø	1	1	1	1	1	1	X	X	X	X	X	X	X	X
Untalk	X	1	ø	1	1	1	1	1	X	X	X	X	X	X	X	X

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This warranty does not cover any products which have been subjected to mis-use, neglect, accident or improper installation or application. Nor shall it apply to products which have been repaired or altered outside of our factory by other than an authorized service representative of DDC.

For implementation of warranty service or repair, DDC must be contacted for return or repair authorization. A return material authorization number will be issued upon evaluation of all pertinent details regarding the matter. No material will be accepted by DDC without an authorization number.

Defective material authorized for return should be shipped at customer expense, prepaid and insured. Upon determination of applicability of this warranty, material will be repaired or replaced. Material determined to be covered by this warranty will be returned to sender prepaid, at the expense of ILC Data Device Corporation.

DDC reserves the right to repair or replace, at its option, at no charge to the sender, any materials found to be within the limitations of this warranty.

Materials returned for reasons not within the limitations of this warranty will be subject to a minimum charge for handling and evaluation. Products found to be within specifications or outside the limitations of this warranty will be returned at customer expense.

DDC requests immediate notification for any claims arising from damage in transit in order to determine carrier responsibility.

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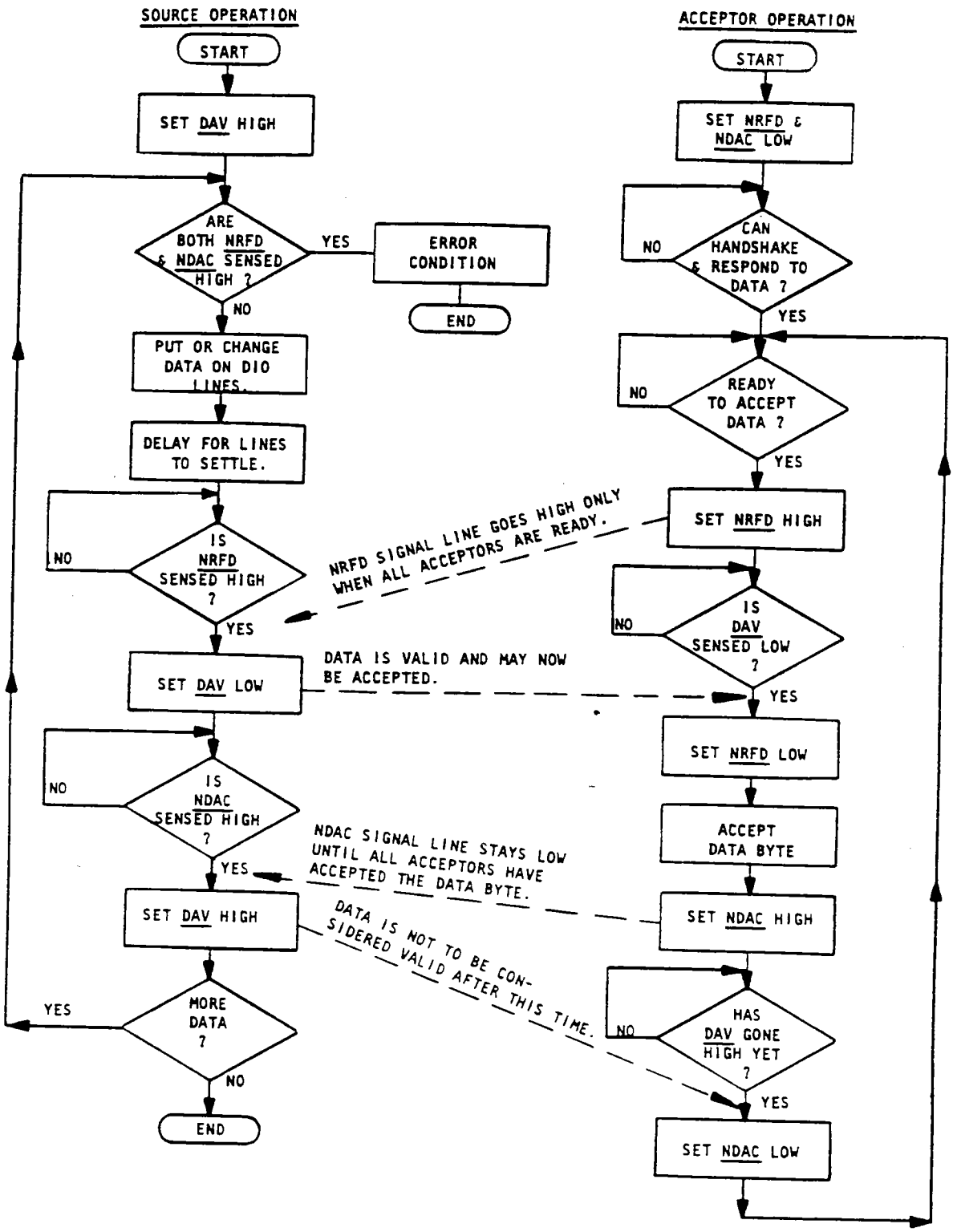


Figure A-2. Handshake Timing Sequence

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