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# Hardware Manual
# MIL-STD-1553 Tester/Simulator
# PCI Interface Card
## *MN-65572iX-001*

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RECORD OF CHANGE

| Revision | Date | Pages | Description |
|---|---|---|---|
| A | Jan., 2000 | All | Original Issue |
| B | Oct., 2000 | 62-142 | Function Definitions corrected |
| C | Aug, 2002 | All | Software section removed, Fig 13 modified |
| D | Feb, 2003 | 6 | New Figure 1, and Table 1 |
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# HOW TO USE THIS MANUAL

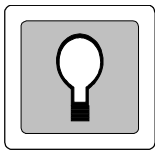
This manual uses typographical and iconic conventions to assist the reader in understanding the content. This section will define the text formatting and icons used in the rest of the manual. This manual is formatted with a 'Scholar Margin' where many tips, symbols or icons will be located.

For the full text of this manual, ***BU-65572iX*** will be used to identify both the ***BU-65572iX*** and the ***BU-65570iX***. In those cases where there is a difference, the appropriate part number will be identified.

## TEXT USAGE

- **BOLD**– text that is written in bold letters indicates important information and table, figure, and chapter references.
- ***BOLD ITALIC***– will designate DDC Part Numbers.
- `Courier New–` is used to indicate code examples.
- <…> - Indicates user entered text or commands.

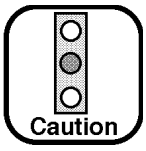
## SYMBOLS AND ICONS



The Idea/Tip icon will be used to identify a handy bit of supplementary information that may be useful to the user.



The Note icon signifies important supplementary information that will be useful to the user.



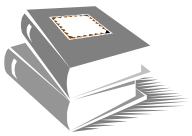

The Caution icon identifies important information that presents a possibility of damage to the product if not heeded.



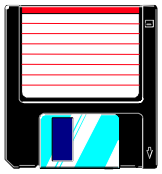

Much stronger than a Caution, the Warning icon presents information pertaining to hazards that will cause damage to the product and possible injury to the user.



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The Reference icon indicates that there is related material in this manual or in another specified document.



The Disk Icon describes information that is related to software.

## SPECIAL HANDLING AND CAUTIONS

The ***BU-65572iX-300*** uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.




- Turn off power to the PC and unplug from wall.
- **NEVER** insert or remove card with power turned on.
- Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.
- Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

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# INTRODUCTION

The ***BU-65572iX*** provides full, intelligent interfacing between one or two MIL-STD-1553 Data Buses and a PCI Bus. The ***BU-65572iX*** is packaged on a half-size IBM PC/AT printed circuit board with a PCI bus interface. Features of the board include:

- Plug-and-Play (PnP) compatible for easy installation
- Onboard processor operating at 40MHz
- 64 Kbytes of on-board Program RAM
- 64 Kbytes of shared static RAM per installed channel
- DMA transfer of monitored data to host data buffer
- IRIG-B time tagging combined with 32-bit onboard time tag counter
- Software configuration of bus connection
- Software configuration of bus loading
- Variable output transceivers, 0 – 28 volts with 4096 incremental steps (Only the ***BU-65572i*** model)

Application software has the capability to simulate Bus Controller, all 31 Remote Terminals, and Monitor simultaneously on each of the installed buses. There is additional capability to synchronize the onboard time tags of all of the operating cards with one command. Included with each ***BU-65572iX*** PCI Card is the DDC Menu and the Runtime Library with example source. The library supports 'C' and LabVIEW® programming. All software and updates are posted on the DDC web site.

## WHAT IS INCLUDED IN THIS MANUAL?

This manual contains a detailed installation guide for the ***BU-65572iX*** PCI Card and a complete listing of the software supplied with the card. The RTL Library, DLL, and Driver installations for Windows® 95, 98, Windows NT®, and Windows 2000 will be covered in this manual.



The library software provides a level of abstraction such that it is not necessary to understand the operation of the chip set.



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# SYSTEM REQUIREMENTS

An IBM compatible PC with an Pentium 233 MHz processor or better.
Windows 95, 98, NT, or 2000 operating system.
One available PCI slot in the main board.

# TECHNICAL SUPPORT

In the event that problems arise beyond the scope of this manual, you can visit the DDC web site and review the FAQ page. If you still have questions you can get in touch with DDC by calling:

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44 (1635) 811140 Fax: 44 (1635) 32264
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DDC also has an Internet World Wide Web site, which allows customers to easily download new revisions of software and documentation. The Internet address is **www.ddc-web.com**.

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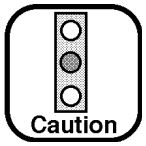
We will update the product as new functions are developed or major bugs are fixed, to the extent of the warranty period. These updates will be made available on our web site from time to time. Prior to calling DDC for updated material, please visit our web site for the latest versions.



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# HARDWARE INSTALLATION

The ***BU-65572iX*** card is a PCI Target device and may be inserted into any PCI 2.1, or higher, compatible slot. When installing the card, the following should be observed:




**NEVER** insert or remove the card with the power turned on.

**ALWAYS** take proper precautions to guard against static damage. Use a wrist strap if available, or ensure proper static grounding by touching the power supply cover **WITH POWER OFF**.




Insert the card at a slight angle so that the connectors first protrude from the rear opening and then gently press the card into the motherboard connector. Secure with proper hardware.

Make sure that adjacent cabling and wiring do no hinder the airflow around the card.

The ***BU-65572iX*** does not contain any configuration jumpers for selection of bus connection. Selection of direct or transformer coupling is performed by way of functions provided in the RTL. In addition to this, there are no jumpers needed for card installation, as the ***BU-65572iX*** is a true Plug and Play design. Interrupts and memory selections will be performed by the operating system as the boot system progresses.



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# DISCRETE I/O CONNECTOR "J1" PINOUTS

This connector (Soldered on the board) is a 25-pin "Subminiature D Connector" (Amp P/N 747846-4). Pin numbering designations for "J1" are shown below.

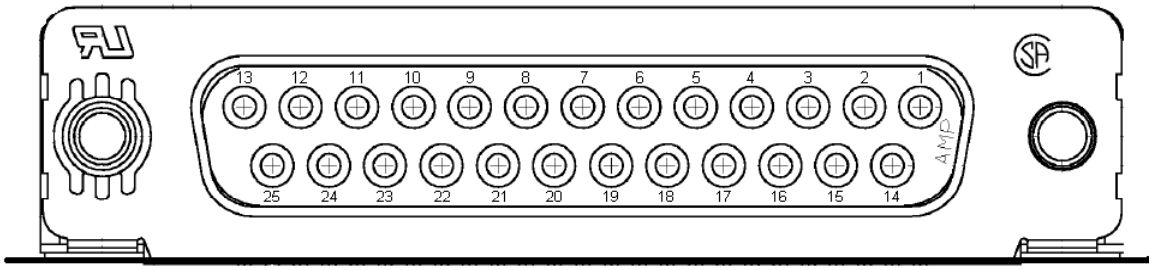



**Figure 1. 25-Pin "J1" Discrete I/O Connector (As viewed from BU-65570/72i Card Edge)**

Models BU-65570/72i are shipped with "J1" mating connector and backshell kit as listed in table below.

**Table 1. Supplied I/O Connector Components**

| Description | AMP # | Quantities |
|---|---|---|
| **SHIELDING ENCLOSURE KIT, PLUG, SIZE 3, 25 POSN, AMPLIMITE HDE-20** | **747948-5** | **1** |



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## CARD PINOUT

This section describes pinouts for the card. The card has two connectors, a DB-9 that is used for 1553 Bus I/O and a DB-25 that is used for discrete, power and IRIG. The pinouts for these connectors are shown in following figures.

**NOTE:** All ground returns are connected to the chassis ground.

| Pin | Description |
|---|---|
| 1 | CH1_TXA_L |
| 2 | CH1_TXA |
| 3 | CH1_TXB |
| 4 | CH1_TXB_L |
| 5 | GND (connected to shell) |
| 6 | CH2_TXA_L |
| 7 | CH2_TXA |
| 8 | CH2_TXB |
| 9 | CH2_TXB_L |

**Table 2. J2: 1553 Bus 'D' Connector**



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| Pin | Description |
|---|---|
| 1 | N/C |
| 2 | Chassis Ground |
| 3 | Chassis Ground |
| 4 | Chassis Ground |
| 5 | IRIG Mod |
| 6 | Channel 1 Discrete Out 1 |
| 7 | Channel 1 Discrete Out 2 |
| 8 | Channel 1 Discrete Out 3 |
| 9 | Channel 1 Discrete Out 4 |
| 10 | Channel 2 Discrete Out 1 |
| 11 | Channel 2 Discrete Out 2 |
| 12 | Channel 2 Discrete Out 3 |
| 13 | Channel 2 Discrete Out 4 |
| 14 | Chassis Ground |
| 15 | +5 Volts |
| 16 | +5 Volts |
| 17 | IRIG In |
| 18 | Channel 1 Monitor Trigger In |
| 19 | Channel 1 Monitor Trigger Out |
| 20 | Channel 1 BC Trigger In |
| 21 | Channel 1 BC Trigger Out |
| 22 | Channel 2 Monitor Trigger In |
| 23 | Channel 2 Monitor Trigger Out |
| 24 | Channel 2 BC Trigger In |
| 25 | Channel 2 BC Trigger Out |

**Table 3. J1: Discrete I/O**



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# DRIVER INSTALLATION

## WINDOWS 95/98

For a Windows 95/98 installation continue with the following installation instructions. If using another operating system, skip to the relevant installation section.

1) Install the card as described in the beginning of the **HARDWARE INSTALLATION** section.

2) Turn on the computer.

3) The **Add New Hardware Wizard** window will appear after boot-up:




**Figure 2. Found New Hardware**

4) Click on the **Next** button.



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**Figure 3. Search for Driver**

5) Highlight Search for the best driver for your device (Recommended) radio button.

6) Click on the **Next** button.




**Figure 4. Specify Driver Location**



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7) Insert the BUS-69068 Installation Disk.

Select the **Floppy disk drives** option.

NOTE: If you are installing the software from a CD, highlight **CD-ROM drive** check box and uncheck the **Floppy disk drives** check box.

9) Click on the **Next** button to locate the ***BU-65572iX-300*** device driver.

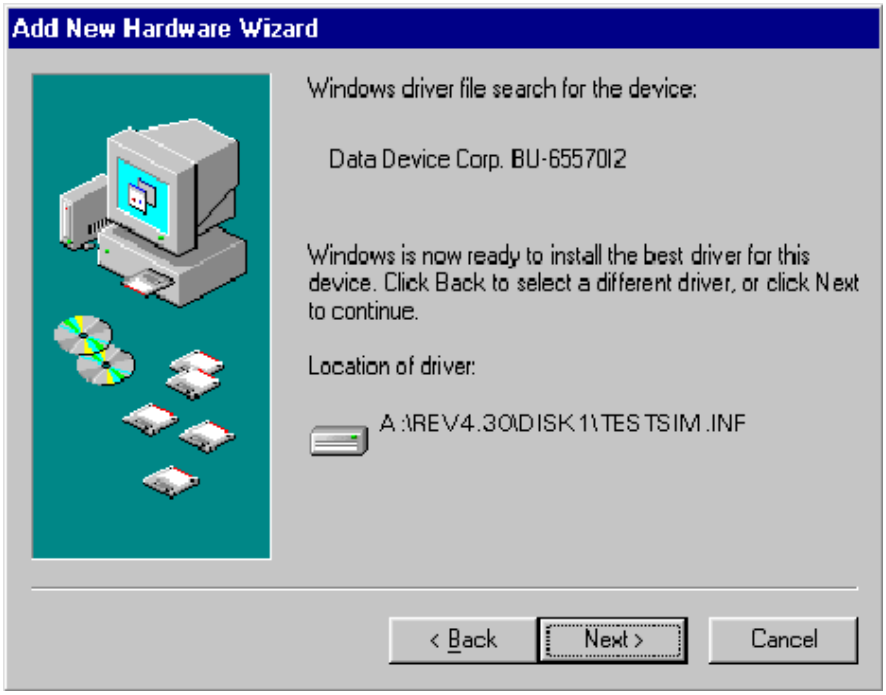



**Figure 5. Found Driver**

10) Click on the **Next** button to install the device driver.



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**Figure 6. Finished Install of Driver**

11) Click on the **Finish** button to confirm the installation.




**Figure 7. Confirm Driver Installation**

12) Click on the **Finish** button to close the Add New Hardware Wizard.

13) Continue configuring the device by installing the BUS-69068 RTL software or the BUS-69065 TestSim Menu. Both software



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packages include the **DDC 1553 Card Manager,** which is used to configure the card and assign a device ID.



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# WINDOWS NT 4.0

For a Windows NT installation, continue with the following installation instructions. If using another operating system, skip to the relevant installation section.



***NOTE:*** *The user must have administrator rights when using Windows NT.*

1) Install the card as described in the previous **HARDWARE INSTALLATION** section.

2) Turn on the computer.

Insert the ***BUS-69068S0 Installation Disk*** into the floppy drive.



***NOTE:*** *If you are installing the software from a CD, follow the instructions that come with your CD.*

4) Click on the Windows **Start** button.

5) Click on **Run**.

6) In the **Open** window type ***A:\Setup.exe***.

7) Click **OK.**

8) Follow any instructions that may appear on the screen. The computer will need to be rebooted for the device driver to run.

9) Once rebooted, proceed with the **DDC 1553 Card Manager** instructions.



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# WINDOWS 2000

For a Windows 2000 installation continue with the following installation instructions. If using another operating system, skip to the relevant installation section.

***NOTE:*** *The user must have administrator rights when using Windows 2000.*

1) Install the card as described in the beginning of the **HARDWARE INSTALLATION** section.

2) Turn on the computer.

3) The **Found New Hardware Wizard** window will appear after boot-up:




**Figure 8. Found New Hardware**

4) Click on the **Next** button.



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**Figure 9. Search for Driver**

5) Click on Search for a suitable driver for my device.

6) Click on the **Next** button.

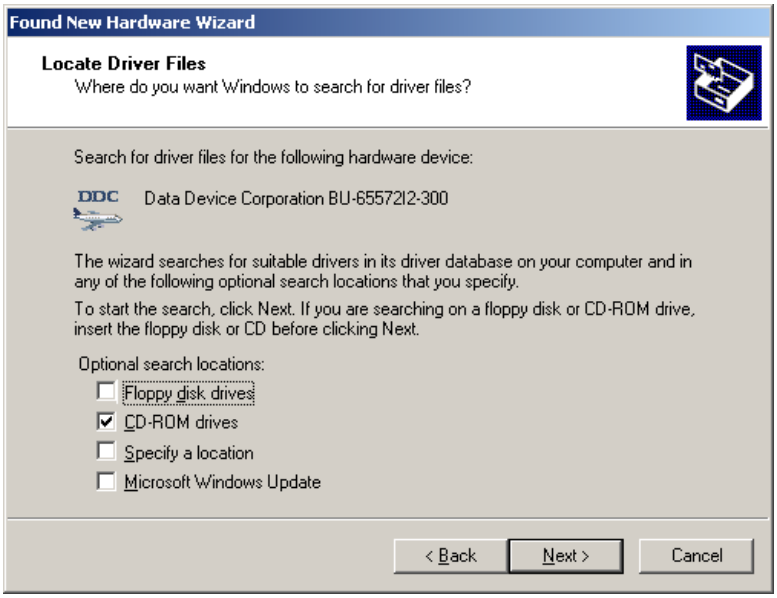



**Figure 10. Specify Driver Location**

7) Insert the ***BUS-69068S0*** Installation Disk.

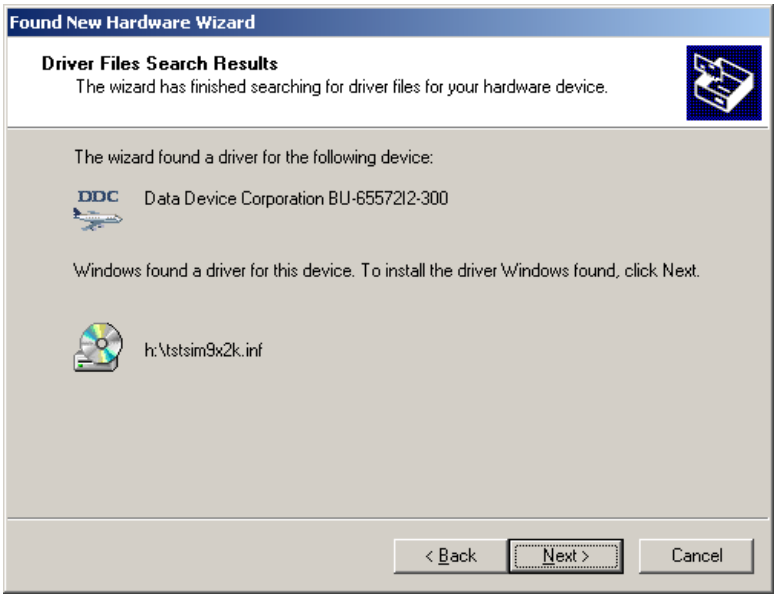
Select the **Floppy disk drives** option.

***NOTE**: If you are installing the software from a CD, highlight **CD-ROM drive** check box and uncheck the **Floppy disk drives** check box.*



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9) Click on the **Next** button to locate the ***BU-65572iX-300*** device




driver.

**Figure 11. Found Driver**

10) Click on the **Next** button to install the device driver.




**Figure 12. Finished Install of Driver**

11) Click on the **Finish** button to confirm the installation.



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12) Continue configuring the device by installing the ***BUS-69068S0*** RTL software or the ***BUS-69065S0*** TestSim Menu. Both software packages include the **DDC 1553 Card Manager,** which is used to configure the card and assign a device ID.



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# HARDWARE CONFIGURATION

The ***BU-65572iX*** is a PCI device, and as such does not require any jumpers or switches to set the base address or interrupt values. The job of configuration for Plug-and-Play PCI configuration is performed by the PC BIOS. During the initial power on boot process, the BIOS performs an enumeration of the PCI bus and provides a configuration in the system that satisfies the card requirements. The card provides the BIOS with details of how much memory it requires, and any other operating parameters that the system needs to know by way of configuration registers built into the card. These registers are configured at the factory to contain the optimum values for the operation of the ***BU-65572iX***. The ***BU-65572iX*** PCI card and software drivers allow for shared interrupts, thus simplifying the installation and reducing the risk of device conflicts.

Once the card has been properly installed, its configuration information is stored to the Windows Registry. The card information stored in the Registry is accessed and controlled through the use of the **DDC 1553 Card Manager**. The **DDC 1553 Card Manager** can be used to view the status of installed cards, and map an installed card to a device number. In order to access an installed card you **must** assign it a device number. Setting up the **DDC 1553 Card Manager** is shown in the RTL (***MN-69068***) and the Test/Sim GUI (***MN-69065***) manual.



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# HARDWARE OPERATION

## GENERAL

The ***BU-65572iX*** is the next generation DDC PCI Tester/Simulator which can simultaneously simulate a MIL-STD-1553 BC, all RTs, and an intelligent MT simultaneously on two 1553 buses.

Full error detection features are provided in all modes of operation. In addition, user specified errors including bit count and Manchester II errors may be injected in BC and any of the emulated RT modes.

Operational characteristics of the ***BU-65572iX*** such as output voltage level, bus termination, and coupling configuration are all software controllable using functions provided in the software library.

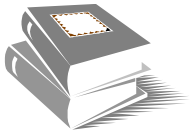
## BUS CONTROLLER MODE

The ***BU-65572iX*** Bus Controller supports all MIL-STD-1553B message formats. Up to 1024 unique receive, transmit, mode code, and RT to RT messages may be defined at one time for each of the installed channels. A frame can contain up to 1024 unique messages.

Programmable attributes within a message include time to next message, bus (channel A or channel B), intermessage routines, and injected error. The time to next message defines the time from the start of the present message to the start of the next message. The time to next message is programmable up to 65,535 msec in 1-μsec increments.

### *Minor And Major Frames*

The execution of messages is controlled by a message list referred to as a frame. The frame specifies the contents and timing of complete communication runs by the BC. Each entry in the frame is either a reference to a message or a special frame symbol. The entire frame is referred to as a major frame and is divided into minor frames each of equal time duration.



Loading message ID handles into an U16BIT array specifies a frame. Each message ID uniquely identifies a message that was previously defined by the function ddcDefMessage (see ***BU-69068*** manual). Other elements that can be placed into a frame list are ‘Frame Symbols’. The



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frame symbols identify special operations that should be performed at that point. For example the symbol 'END_OF_MINOR' specifies that the BC must stop message processing until the minor frame time counter expires. Then, once the timer expires, the counter is reset with the Minor frame time, and the next message in the list will be processed.

Every frame list must have at least one entry of 'END_OF_MAJOR'.

The minor frame time is based on a programmable 32-bit counter with 1 μsec resolution. The ***BU-65572iX*** supports major frames of up to 1024 messages per installed channel, with a period of up to 72 minutes.

## *BC Error Injection*

Error conditions may be injected on a message by message basis. The ***BU-65570I/72I*** supports three categories of injected BC Errors: length errors, encoding errors, and gap errors. Length Errors include both word count errors and bit count errors. Word Counts of -32 to +1 words may be programmed. Bit counts of +3, +2, +1, -3, -2, or -1 bit may be programmed on any word within the message.

Encoding errors are implemented though the use of two simple yet powerful mechanisms for modifying the output of the ***BU-65572i'***s Manchester encoder. The two modifying functions are glitch and inverse. A glitch error will force the output of the encoder to an idle bus condition for the specified period of time.

An inverse error will invert the output of the encoder for the specified period of time. The word number, starting time, and width specify the placement of the error. The error may be placed in any word within the message and its starting time may be programmed in 500 nsec with a width of up to 3 μsec. This error injection is capable of generating a host of errors including invalid sync patterns, parity errors, and Manchester bi-phase errors.

A gap of 3, 4, or 5 μsec (measured mid-parity crossing to mid-sync crossing) may be inserted between any two words in a message. This allows for a "dead time" gap between words of 1,
2, or 3 μsec.

## *Inserting Asynchronous Messages*

The ***BU-65572iX*** allows an asynchronous message to be inserted while the card is running. The inserted message will be executed upon completion of the current message. The user will define all



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asynchronous messages after the END_OF_MAJOR frame symbol and insert the message into the running frame by calling the insert message routine. The hardware does all of the work.



Once the frame has been defined and the BC is running, asynchronous messages may be inserted at any time by asserting the 'ddcInsertMessage' (see ***BU-69068*** manual) routine. This routine specifies which 1553 device the operation should be processed by, and the message index in the frame list that should be inserted. The asynchronous message will be inserted immediately following the present message.



It should be noted that if enough messages are inserted into a minor frame, the messages could overrun the minor frame time. In this case, all of the messages will be processed, and the first message of the next minor frame will occur immediately.

## *BC Intermessage Routines*

Upon completion of a BC message, the ***BU-65572i***"s on-board processor will execute up to 2 intermessage routines. Intermessage routines are used to implement automatic retries on failed messages as well as other "end of message" functions.

Intermessage routines are used to signal the user application that an interrupt has been generated. This can occur at the end of a message for BC operation, when a data table has been accessed in RT operation, or when the Monitor stack is 1/3 full.

Another use of intermessage routines is to signal external hardware that a specific event occurred. As messages are being processed by the ***BU-65572iX***, discrete signals can be set and cleared at the 25 pin 'D' connector. These discretes can be used to synchronize an oscilloscope or other external device.

There are also intermessage routines that will listen at the 'D' connector for inputs that can be used to initiate operations in the ***BU-65572iX***.

## *Response Timeout*

The ***BU-65572iX*** BC RT's and MT support programmable response timeout values ranging from 2 to 29 μsecs in 1-μsec increments.



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# RT MODE

The ***BU-65572iX*** can simultaneously simulate the operation of 31 unique remote terminals (RTs) plus a broadcast address for each of the installed channels. The ***BU-65572iX*** maintains "last status" and "last command" words allowing for full support of transmit last command and transmit status mode commands. The ***BU-65572iX*** supports full RT command illegalization for each transmit or receive message based on RT address and sub-address. In addition, individual mode commands may be illegalized.

## *RT Error Injection*

Error conditions may be injected on an individual RT/SA basis. The ***BU-65572iX*** supports five categories of injected RT errors: length errors, encoding errors, gap errors, status address errors, and response errors. Length errors include both word count errors and bit count errors. Word counts of -32 to +1 words may be programmed. Bit counts of +3, +2, +1, -3, -2, or -1 bit may be programmed on any word within the message.

Error specifications are attached to the data tables that are mapped to a RT and Sub-address combination. This provides for a large number of possibilities for injecting errors. An application can map more than one data table to any given RT/SA combination. This means that the RT can respond with different errors each time it is accessed.

Encoding errors are implemented though the use of two simple yet powerful mechanisms for modifying the output of the ***BU-65572i'***s Manchester encoder. The two modifying functions are glitch and inverse. A glitch will force the output of the encoder to an idle bus condition for the specified period of time. An inverse will invert the output of the encoder for the specified period of time. The word number, starting time, and width specify the placement of this error. The error may be placed in any word within the message. The starting time is programmed in 500 nsec increments from the beginning of the specified word. The width of the error is specified in 50 nsec increments up to 3 μsec. This error injection scheme lends itself to generating a host of errors including invalid sync patterns, parity errors, and Manchester bi-phase errors.

A gap of 3, 4, or 5 μsec (measured mid parity crossing to mid-sync crossing) may be inserted between any two words in message. This allows for a "dead time" gap between words of 1, 2, or 3 μsec. A status address error may be injected in which the RT responds with a status word containing a RT address, which does not match the terminal's RT address. The RT may be programmed to respond with any value from zero to 31 in its status response.



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The ***BU-65572iX*** supports three types of response errors: no response, a late response, or a response on the wrong bus. No response errors may be programmed for a single bus (Bus A or Bus B) or for both buses. Injecting a no response error on one bus provides a simple mechanism for testing bus controller retry conditions. A late response may be programmed in the range of 2 to 30 μsecs in 1 μsec increments.

### *RT Intermessage Routines*

The RT section of the ***BU-65572iX*** also supports intermessage routines. Upon completion of a RT message the ***BU-65572iX***'s on-board processor executes two intermessage routines. The data table that was used by the RT for a given message specifies which intermessage routines will be executed. Refer to TABLE 3 for a summary of the ***BU-65572iX*** 's intermessage routines.

As with the Bus Controller operation, the RT intermessage routines specify special actions to take place at the end of the current message processing. One of the more common actions that are taken is to signal the application that the hardware completed the message by generating an interrupt to the system. Other actions will cause discretes to be set or cleared and data tables to be swapped. And since each RT / Sub-address can be assigned a block of data tables, each message to the RT can result in different actions being taken.

## BC/RT DATA TABLES



For each of the installed 1553 channels, the ***BU-65572iX*** maintains 1024 data tables within the shared RAM. Each data table may be up to 32 words in length. The total memory allocation for all data tables is restricted to 12K words. These data tables are common to both BC and RT. Internal lookup tables map each RT address, T/R, sub-address combination (RT mode) and message number (BC mode) to a chosen data table. Data tables may be read or written to in real time by the user (‘ddcReadData’ or ‘ddcWriteData’) (see ***BU-69068*** manual) and may be either single or double buffered. Double buffering can be used to avoid the memory access contention that occurs when the PC's application and the 1553 bus access data tables simultaneously. The ***BU-65572iX*** provides an optional block data mode in which the data table number associated with a given RT message is incremented after completion of the message. The block data mode is implemented as a circular data structure. Each RT command (RT address, T/R, and sub-address) has three data table numbers associated with it: first, last, and current. The current data table number will be incremented after completion of

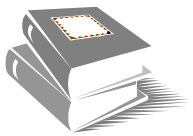


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message until the value of 'last' is reached, at which point the current table number will rollover to the value of first. The incrementing of the current data table is accomplished through the use of an intermessage routine.

## MONITOR MODE

The ***BU-65572iX*** contains an independent message monitor for each bus with the ability to filter messages in real time. Monitor selection or filtering is performed through the use of a lookup table based on the RT address, T/R, and sub-address of command words. Monitored messages are stored in the shared RAM on the ***BU-65572iX***, which allocates 6K words for the monitor stack. Each entry in the monitor stack contains a header followed by a variable number of data words. Contained with the message header are the receive/transmit command(s), receive/transmit status, message format, Bus (A or B), a capture flag, word count (actual number of words in the message), a detected error field, and a 32-bit time tag (1 µsec resolution).



The transfer of the messages from the card's circular buffer to the host memory/disk is determined by the capture flag, which is set upon detection of a predefined event as specified by the 'ddcCaptureEvent' (see ***BU-69068*** manual) command. Capture events include immediate, command template match, exception, or trigger. The command template event is based on a 16-bit command word with a 16-bit mask. Exception events may be programmed for any exception: invalid command, invalid data, invalid status, gap preceding data, response time error, wrong RT address error, status set condition or an illegal command. The trigger event uses one of the four monitor input pins on the 25-pin D-type connector as a trigger input.

The ***BU-65572iX*** supports DMA transfers using its PCI Bus Mastering Mode. The Monitor mode can autonomously transfer monitored data to host buffer without host CPU intervention. This greatly improves the efficiency of both the host and the ***BU-65572iX***.

## INTERRUPTS

For each of the installed channels, both the BC/RT and the Monitor may generate interrupts on a common output to the PCI back plane (#INTA). The hardware interrupt vector used by the ***BU-65572iX*** is selected by the Plug-and-Play capability of the PCI back plane and BIOS. An important aspect of PCI interrupts is that they are sharable. This means that the ***BU-65572iX*** can share an interrupt for all buses on the card and all ***BU-65572iX*** cards in the computer.



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As interrupts are generated, the ***BU-65572iX*** device driver will acknowledge the interrupt by clearing the computer hardware and then enter an interrupt vector onto a queue that can contain up to 64 interrupt actions. Each vector on the queue will be sent by the system to the user application. This will only occur when the applications interrupt service routine (ISR) is completed processing all previous interrupts. This action ensures that the user ISR is not interrupted.

## *BC Interrupt Generation*

BC interrupts may be enabled by a global interrupt mask for successful messages, communication errors, status set conditions, or on selected frame symbols (skip, break point, major frame, and minor frame symbols). The criteria for a status set condition are programmed globally through the status mask. The status mask allows any of the 16 bits within the RT status word to be ignored. The status mask affects the generation of interrupts as well as the detected error field that is stored in the message structure.

BC interrupts are issued by the intermessage routines associated with messages allowing for selective interrupt generation on a message by message basis. A two-word vector is pushed onto a circular queue for each interrupt request and is transparent to the user. The queue can hold up to 64 interrupt vectors; thus, the host computer is not required to immediately acknowledge the interrupt request.

## *RT Interrupt Generation*

RT interrupts may be enabled by a global interrupt mask for transmit/receive messages with no message error, mode commands with no message error, transmit/receive messages with the message error bit set, or mode commands with the message error bit set.

RT interrupts are issued by intermessage routines associated with data tables allowing for selective interrupt generation on a message by message basis. A two-word vector pushed onto a circular queue for each interrupt and is transparent to the user. The queue can hold up to 64 interrupt vectors; thus, the host computer is not required to immediately acknowledge the interrupt request.

## *Monitor Interrupts*

Monitor interrupts may be generated after each message is received or after one third of the monitor's circular buffer has been filled

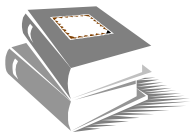


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(approximately 2K words). This allows for either real-time analysis or mass collection/storage of monitored data.

# OTHER FEATURES

## *Variable Amplitude Transceiver*



The ***BU-65572iX*** provides variable amplitude transceivers for each 1553 channel installed on the card. The output of the variable transceiver is software controllable in the range of 0.0 volts to 28.0 volts. This range is covered in 4096 steps. The user application is able to modify this amplitude in real by calling the 'ddcSetAmp' (see ***BU-69068*** manual) library function.

The transceiver outputs can be individually controlled for each of the installed channels, while the two transceivers for a given channel will be varied simultaneously. Functions for controlling the transceiver outputs are available in the 'C' library that is provided with the card.

## *IRIG-B support*

Inter-Range Instrument Group (IRIG) Standard 200-95 recognition is supported by the ***BU-65572iX*** boards. The implementation of this standard into the 1553 tester/simulator board enables all messages to be tagged with time-of-day information, allowing accurate correlation between messaging on the 1553 bus and other hardware and software events that are occurring in the system. This is especially useful when trying to identify the cause of a system problem that may be directly related to message data sent over the 1553 bus. The IRIG-B timestamp for each of the installed channels may be individually selected. This allows one channel to use the internal 32 bit Time-Tag clock, while another channel will stamp the messages with the IRIG-B time. The IRIG-B timestamp, if enabled, will be combined with the internal timestamp to provide µs accuracy.

When IRIG is enabled on the card, the monitor message header will contain two more words than in the previous versions. These two words, which are tacked onto the end of the header, specify the IRIG high and IRIG low words of the timestamp. A feature of adding new entries to the header is the ability to maintain the existing 32-bit internal time tag of the ***BU-65572iX***. When this feature is operating, the internal 32-bit time tag is reset to zero each time a new IRIG signal is received (about once per



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second). This means that the long term accuracy of the time tags is as good as the IRIG generator in the system.

## *IRIG-B Specifications*

- Rate-scaled serial time code
- 1st word is time-of-year in BCD notation including days, hours, minutes, seconds, and fractions of seconds
- DDC Usage - Mode B, Not using Straight Binary Seconds
- Range = 1 Second to 1 Year
- The initial time 0h 0m 0s January 1 of the present year
- Pulse Code Modulation on 1KHz carrier
- One full Time Code is received every second.

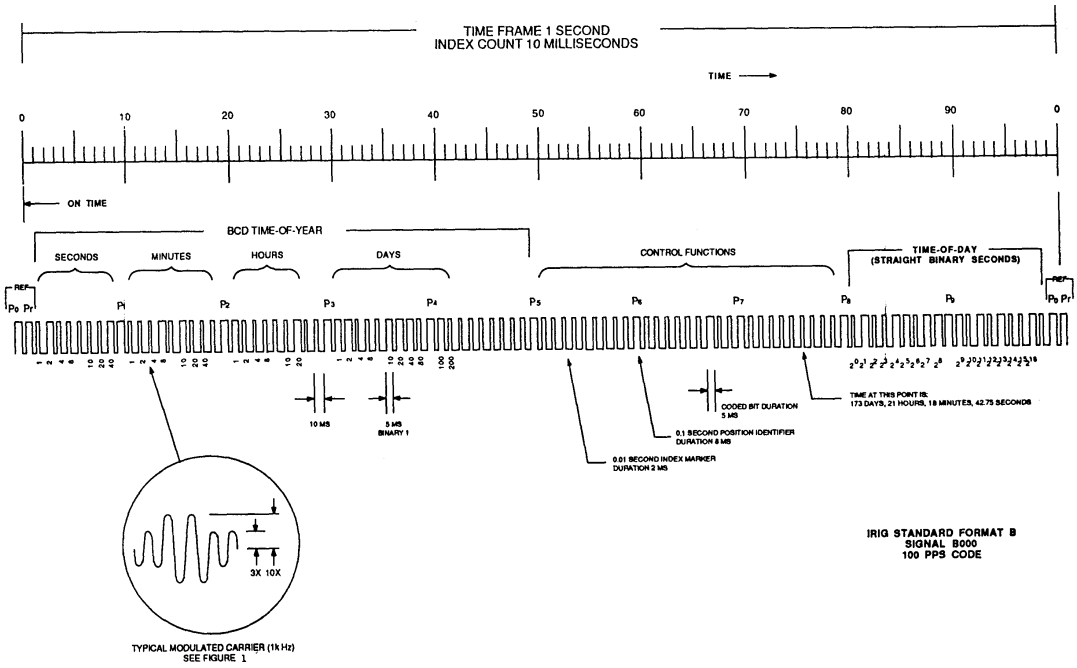



**Figure 13. Sample IRIG Signal Timing**



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## *Monitor DMA to Host Buffer*

The ***BU-65572iX*** is fully compliant to the PCI standards for both Target and Master applications. As a PCI master, the ***BU-65572iX*** is capable of performing DMA block data transfers from the monitor buffers on the card to a user buffer in the host memory. This will allow the transfer of data without interrupting the host processor, enabling it to perform other more important tasks.

When the application calls the 'ddcEnableDma' routine, the size of the DMA buffer must be specified. The DMA buffer size must be greater than 32K words. If it is not greater than this size, then the routine will return with an error. If the size of the DMA buffer is too large, than the system will not be able to allocate it and again the routine will fail. Since this buffer is dynamically allocated from non-swappable system resources, the DMA buffer size should not be too large. The buffer size can affect system operation if too much memory is requested.

The DMA buffer is not directly accessable to the application. All operations that will be performed on the DMA buffer must be made through the appropriate RLT routines.

## *Software Control Of Bus Configuration*

The ***BU-65572iX*** has the capability of being connected to the bus as either Transformer Coupled or Direct Coupled. Transformer coupling enables the card to be connected to the 1553 bus with a long stub of up to 20 feet. Direct coupling requires that the card be connected to the 1553 bus by a stub of no more than 1 foot. The coupling configuration is dynamically configurable via functions provided in the 'C' library. Relays on the board are used to select the correct signal path direct or transformer coupled for each of the installed channels.

This card also has the capability of modifying the bus termination to one of three different loads. If the bus termination is set to None, then the effective impedance is infinite ohms. If the bus is set to Full, then the bus termination will be 37.5 ohms. A setting of Half will cause a bus termination of 75.0 ohms. This control makes it quite simple to connect the ***BU-65572iX*** directly to another 1553 device without the need of an external load. As with the bus coupling mode, the bus termination mode is dynamically configurable via software functions provided in the 'C' library which control relays for each installed channel.



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### *Discrete Outputs*

This new Tester/Simulator design will include four discrete outputs per channel. These four outputs are set to logic ‘1’ and cleared to logic ‘0’ by use of eight new intermessage routines. The format of the routine names is SET_DISCRETE_X and RESET_DISCRETE_X. These discrete outputs may be used for signaling external equipment when a specific event or message has occurred. The intermessage routine can be attached to any message, data table, or frame symbol providing a wide variety of debug possibilities.



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# APPENDIX A

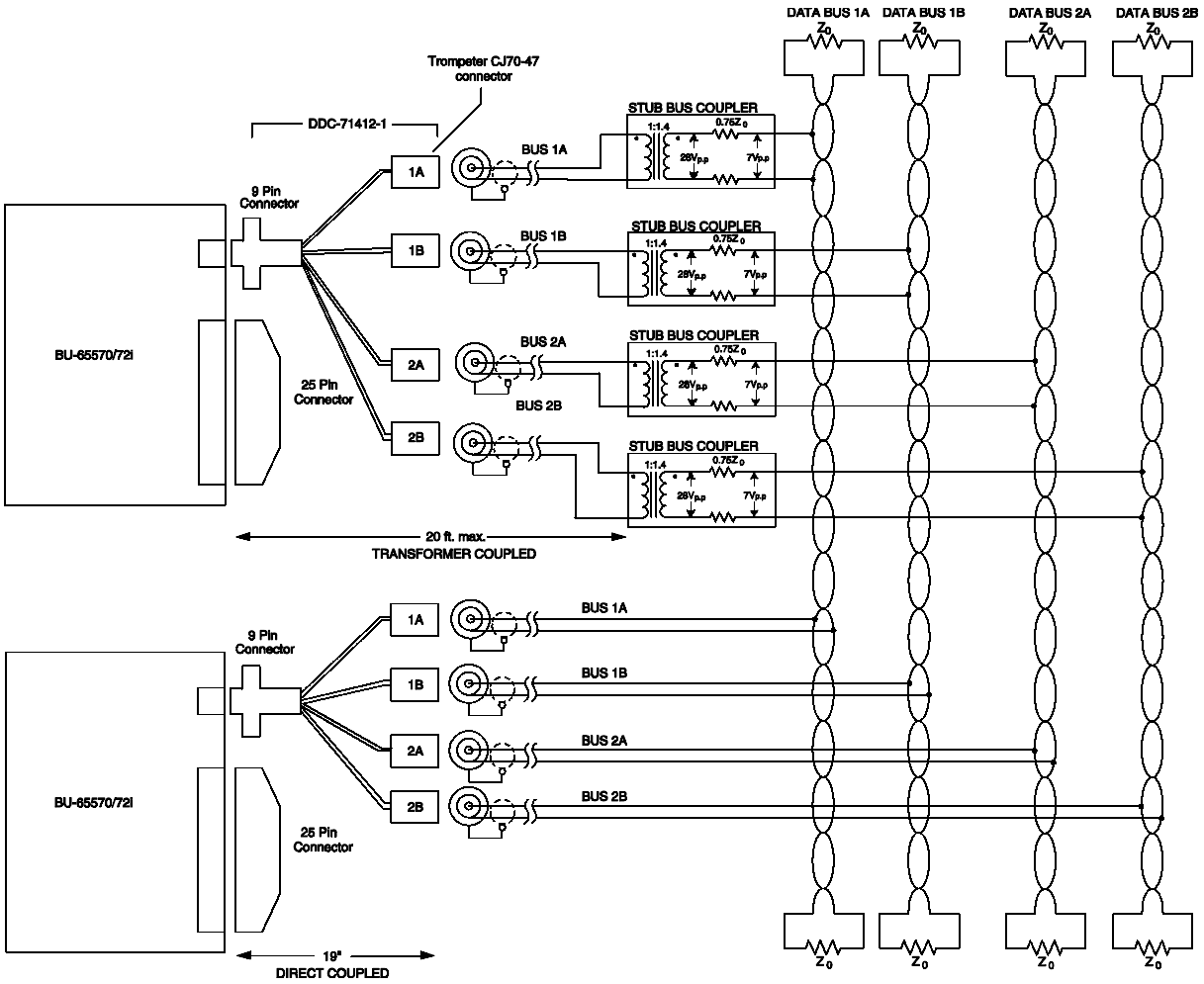



**Figure 14. Bus Configuration**

Figure 14 shows a common bus configuration using the ***BU-65572i2*** card. The top half of the picture shows how to hook up the ***BU-65572i2*** card to a Transformer coupled bus using bus couplers. The Bottom half of the picture shows how to hook up the ***BU-65572i2*** card to a Direct Coupled bus.



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