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APPLICATION NOTES

MIL-STD-1553 STANDARDS AND COMPONENTS: FREQUENTLY ASKED QUESTIONS

By

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INTRODUCTION

This application note provides relevant information for users of DDC's MIL-STD-1553 products. While the questions relate primarily to our data bus component products (mostly the ACE and derivative series), the answers to many questions are also applicable for users of our 1553 board level products.

Note that **all** of the questions in this note were actually asked by at least one of our customers. In many cases, the same question has been posed by a number of customers.

The application note is divided into nine sections, which are listed below. In addition, many of the sections are divided into subsections.

(1) *Standards: MIL-STD-1553, MIL-STD-1760, STANAG-3838.* This section covers issues relating to these standards, along with the 1553 RT Validation Test Plan.

(2) *ACE and Mini-ACE.* This is the longest section. It includes questions and answers on the ACE/Mini-ACE's general characteristics, operation of the BC, RT, and Monitor modes, interrupts, troubleshooting, and self-test. Since the Enhanced Mini-ACE is a superset of the ACE and Mini-ACE, most of the questions and answers in this section are also applicable for the Enhanced Mini-ACE and PCI Enhanced Mini-ACE. In addition, the issues addressed in this section are also applicable to SP'ACE.

(3) *Enhanced Mini-ACE*, and ...

(4) *PCI Enhanced Mini-ACE.* The questions and answers in these two sections relate to DDC's two latest generations of 1553 components. This includes discussions about the upgrade path from ACE/Mini-ACE to Enhanced Mini-ACE.

(5) *Rad Hard/Space Components.* This section includes questions and answers on the BU-61582 SP'ACE and the BU-65621 space grade BC/RT/MT chip.

(6) *RT Components.* This section includes questions about the BUS-65112, BUS-65142, and the BU-61703/5 Simple System RT.

(7) *Power/Thermal Questions.* This section includes questions and answers on current and power specifications, transceiver duty cycle, dual redundancy, and thermal issues.

(8) *Transformers.* This section includes transformer layout related information, along with a table of all of Beta Transformer Technology's (BTTC's) transformers for the Mini-ACE, Enhanced Mini-ACE, and PCI Enhanced Mini-ACE.

(9) *Connectors, Cables, and Breadboarding Sockets.* This includes information on mating connectors for DDC's 1553 boards, and a breadboarding socket for the Mini-ACE and Enhanced Mini-ACE.

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STANDARDS: MIL-STD-1553, MIL-STD-1760, STANAG-3838

STANDARDS: MIL-STD-1553

Q. Can two RTs be connected to the same stub cable?

A. According to MIL-STD-1553, the stubs are technically not part of the RTs. Therefore, the two RTs, tested **individually**, should each be able to pass the MIL-STD-1553B input impedance test (1000 ohms minimum, transformer coupled).

In terms of input impedance testing, if the two RTs connected together were to be considered (and therefore tested) as a single "RT," it is highly doubtful that the two RTs taken in parallel would pass the MIL-STD-1553B input impedance spec.

Depending upon the overall electrical configuration of the main bus on a platform (e.g., an aircraft), i.e., the number of stubs, lengths, spacings, impedances, etc., it would be **highly likely** to be able to connect two RTs using the same stub cable and have a reliably functional system. The most likely outcome is that such a configuration **would** work reliably, especially for a relatively short bus, low number of stub taps, and short stub lengths.

Note however, that in terms of bus system topology, that connecting two RTs to the same stub is not compliant to MIL-STD-1553.

Q. Is it allowable to use a 25 foot stub between a bus coupler and a terminal?

A. For a transformer-coupled (stub-coupled) RT, MIL-STD-1553B **recommends** (but does not require) a maximum stub length of 20 feet connecting between a bus coupling box and a single terminal (BC, RT, or monitor). The main intent of this stipulation is to minimize the stub loading on the main bus. Excessively long stubs and/or stubs terminated in low impedances can load down the main bus and result in transmission line reflections, and therefore waveform distortions. This can have the effect of increasing the bit error rate for terminals receiving data on the bus or, in extreme circumstances, cause terminals to stop receiving completely.

However, it is not all that uncommon for implementations to exceed the 25 foot recommendation. If you don't have too many of these types of loads on a particular 1553 bus (and the bus is not too long), then the terminals on it **should** operate reliably.

A transformer-coupled BC or RT is required to transmit a stub voltage of 18 to 27 volts peak-to-peak on its stub, which translates to a voltage on the main bus in the range of 6.36 to 9.54 volts peak-to-peak. A direct-coupled BC or RT is required to transmit 6.0 to 9.0 volts on the bus. Using the lower (direct-coupled) number and assuming a very short data bus (i.e., no attenuation on the main bus) this results in a minimum **received** voltage of 4.24 volts peak-to-peak on the stub for a transformer-coupled BC or RT.

In considering cable attenuation, MIL-STD-1553B requires that a bus network must be designed to provide a voltage between 1.0 and 14.0 volts peak-to-peak at the input to every stub-coupled terminal. The minimum stub signal of 1.0 volt corresponds to a voltage of 1.41 volts peak-to-peak on the main bus. Assuming a minimum voltage transmitter, this allows for an attenuation ratio for the main bus of 4.24 to 1 (6/1.41), or 12.6 dB. This provides for a wide margin, in terms of cable lengths as well as terminal transmitter output and receiver threshold characteristics.

MIL-STD-1553B also requires that a transformer-coupled receiver **must accept** (in the case of an RT, must respond to) any voltage in the range of 0.86 to 14.0 volts peak-to-peak. This provides 0.14 volts margin between the lowest terminal input voltage and the maximum receiver threshold voltage. In addition, a BC or RT is required to **not accept** a voltage below 0.2 volts peak-to-peak (i.e., an RT receiving a voltage below this level must not respond).

Of course, the other consideration is transmission line reflections. Reflection problems can interfere with the operation of terminals on the bus. However, assuming there is a limited number of long stubs (longer than 20 feet), the bus should operate reliably.

For the effect of the 25 foot stub cable, refer to Figure I-1.7 on page I-16 in our MIL-STD-1553 Designer's Guide, Sixth edition. For a transformer-coupled terminal, assuming a "1553B transformer", increasing the stub length from 20 to 25 feet will have the effect of reducing the (worst-case) impedance looking from the bus from about 500 ohms to 400 ohms, representing a 25% increase in the stub loading.

Note that a "1553B transformer" implies a bus coupling transformer with a minimum open circuit impedance of 3000 ohms, as specified in paragraph 4.5.1.5.1.1.1 of MIL-STD-1553B.

Q. We are thinking of using MIL-STD-1553B in an application where the length of the bus will be on the

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order of 100 meters (300 feet). My question is whether or not it is possible to use a 300 foot long bus with a high degree of confidence.

A. MIL-STD-1553B has no maximum bus length, and I have heard of instances where 1000 foot buses have operated successfully. You need to consider the following:

(1) You may want to perform a bus loading analysis/simulation. That is, consider the cable attenuation (for a long bus, you can buy heavier twinax cable with lower resistance per foot, and therefore lower attenuation), the number of bus taps (stubs), and the length and spacing of the stubs. I suggest that you either simulate this or build a mock-up. However, for a 300 foot bus with a reasonable number of terminals, it is unlikely that you will see a problem.

(2) You need to consider the BC response timeout time value. A 1000 foot bus results in a round-trip time of 3 to 4 µs. With our ACE, Mini-ACE, and Enhanced Mini-ACE series bus controllers, the minimum nominal BC timeout value is 18.5 µs. In addition, you may program this parameter for higher nominal timeout values of 22.5, 50.5, or 128.0 µs.

STANDARDS: 1553 VALIDATION TESTING

Q. How is MIL-STD-1553 terminal input impedance measured?

A. For the impedance measurement, we (DDC) use an HP 4192 impedance analyzer. The correct voltage for measuring input impedance, per the 1553 test plan, is in the range from 1.0 to 2.0 Vrms, applied on the stub. Assuming a 15 volt transceiver and therefore a stub-coupled turns ratio of 2:1, this results in a voltage of 2.0 to 4.0 Vrms applied at receiver inputs to the 1553 terminal hybrid. In order to get a stable impedance measurement, the guard conductor from the analyzer needs to be connected to the transformer center tap on the stub side.

Q. For performing the RT Validation Test Plan noise (bit error rate) test, is it necessary to use the noise gate?

A. At one time, the noise gate was required for our older generation series terminals, the BUS-61553 (AIM-HY) and the BUS-61559 (AIM-HY'er).

However, the need for the noise gate has been **eliminated** by the decoder design used in the ACE, Mini-ACE (Plus), the Enhanced Mini-ACE, and the SP'ACE. The new decoder provides improved filtering at the end of a received message, eliminating the need for the noise gate.

STANDARDS: MIL-STD-1760

Q. What are the additional requirements for a MIL-STD-1760 RT, beyond the requirements of MIL-STD-1553?

A. There are several additional requirements:

(1) The stub-coupled transmitter voltage must be a minimum of 20 volts peak-to-peak (the requirement for MIL-STD-1553B is 18 volts peak-to-peak).

(2) There are requirements regarding the RT address. Part of these may be satisfied by latching the RT address (from the 1760 connector) soon after power turn-on. For more details, refer to the answer to the next question.

(3) A 1760 compliant RT must be able to respond on the bus within 150 ms following power turn-on. At this time, it is permitted to respond with the "Busy" status word set. This indicates that while the RT is "alive," it is not yet able to transfer data. Alternatively, it may respond with valid data.

(4) Within 500 ms following power turn-on, the RT must be responding with data as defined by the 1760 standard, with the "Busy" status bit **not** set. This means that the RT's host processor must be fully up and running at this time.

(5) For a bus controller, most of the MIL-STD-1760 requirements are fulfilled by means of software, rather than by hardware. One "gray area" is with regards to the 1760 requirement to transmit and verify (at the receiving end) a checksum with every message.

The checksum requirement may be implemented by either hardware or software. DDC's opinion is that it is better to fulfill this requirement in software rather than hardware. The reason for this is that a software verification provides for a complete "end-to-end" integrity verification.

What we mean by "end-to-end" is that the checksum, if implemented in software, encompasses the operation not only of the 1553 (1760) communications interface, but also of the BC's and RT's host microprocessors and memory, along with the BC's and RT's embedded processor and firmware.

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Keep in mind that the integrity of the 1553 (1760) communication link is still checked by the BC and RT hardware, by means of the parity bit transmitted and checked with each word of every message transmitted across the bus.

Q. Are there special considerations for MIL-STD-1760 regarding RT address, and how to meet these requirements using Mini-ACE?

A. Yes. There are several considerations:

(1) For MIL-STD-1760, the RT address **must** be provided from the 1760 connector. That is, it must **not** be programmed by the RT's host processor software.

(2) When any of the RT address signals are connected to logic "0," there must be a minimum of 5 mA of current in the wire to the 1760 connector. Assuming a 5V power supply, this implies the need for pull-up resistors of less than 1KΩ between +5V and each of the RT address signals.

(3) Note that for routing the RTAD signals to the 1760 connector, it is suggested that some form of ESD protection - either capacitors or clamping diodes - be used. Note that this is just a suggestion, it is not a MIL-STD-1760 requirement.

(4) The RT address must be latched into the RT within 10 ms following power turn-on. In addition, it must not change after it has been latched. There are a few different methods for doing this, depending on one's interpretation of the 1760 standard:

With Mini-ACE, there are several possible means for specifying an RT address for MIL-STD-1760 applications. A common element of all of these methods is that the RT address input signals must be connected to the 1760 connector. The possible methods are as follows:

(a) Use the RT address inputs directly by connecting RT_AD_LAT to logic "0."

(b) Connect the RT address signals to the 1760 connector, connect RT_AD_LAT to logic "1," and have the host processor latch the data from the Mini-ACE RT address inputs under software control, by means of Configuration Registers 3, 4, and 5.

(c) Use a reset circuit to provide a rising edge to RT_AD_LAT sometime **after** power turn-on reset (that is, after the MSTCLR input to the Mini-ACE has settled to logic "1"). This edge will cause the signals on RTAD4-RTAD0 and RTADP to be internally latched. By doing this, if one of the wires to the 1760 connector breaks following turn-on (e.g., when the 1760 connector disengages when the store is fired), the RT address will remain latched internally.

Q. For MIL-STD-1760, is there an option for the Mini-ACE (Plus) to boot up as an RT with the Busy bit set?

A. RT Auto-Boot with the Busy bit set is a feature for the BU-65179 RT version of the Mini-ACE and the versions of the Enhanced Mini-ACE with 4K X 16 RAM, but not of the BU-65178 and BU-61588 Mini-ACE, and the BU-61688/89 Mini-ACE Plus. The BU-65179's "AUTO_BOOT" feature (i.e., to initialize to RT mode with the Busy bit set at power turn-on) is intended for MIL-STD-1760 applications. This helps the 1760 RT designer meet the requirement to be responding to 1553 commands within 150 ms after power-up. By comparison, the BU-65178 RT initializes to "Idle" mode, rather than RT mode, at power turn-on. In "Idle" mode, the host processor must write to Configuration Register #1 to initialize the BU-65178 to RT mode.

STANDARDS: STANAG-3838 AND EFA

Q. Are the ACE, Mini-ACE, and Enhanced Mini-ACE compliant to STANAG 3838 and EFA?

A. Yes. The ACE, Mini-ACE, and Enhanced Mini-ACE **are** compliant to STANAG-3838. In addition, these terminals include functionality to accommodate the requirements for EFA, the EuroFighter Aircraft. These features include:

(1) Providing a mechanism for separating received broadcast data from non-broadcast data. This requirement is met by providing an option for two separate lookup tables; this is, the use of either a single received/broadcast table, or separate receive and broadcast lookup tables.

(2) Provide an option to automatically clear the Service request status word bit following reception of a Transmit vector word mode command.

(3) Provide options to automatically clear the value of the internal time tag to zero following reception of a Synchronize without data mode command, and/or to automatically load the time tag register with the received data word following reception of a Synchronize with data mode command. In addition,

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the Enhanced Mini-ACE bus controller includes an option to automatically transmit the contents of the time tag register as the data word for a Synchronize (with data) mode command.

(4) The TX_INH_A and TX_INH_B inputs are pinned out of the Mini-ACE (Plus) hybrids. This is a requirement for STANAG-3910 for EFA.

(5) An RT requirement to provide a means of ensuring data consistency. The Mini-ACE (and Enhanced Mini-ACE) RT's circular buffering and double buffering mechanisms are provided specifically for this purpose.

(6) In its default RT configuration, the Mini-ACE treats subaddress 31, as well as subaddress 0, as mode code subaddresses, and provides the capability to illegalize individual mode code commands for either or both of these subaddresses.

(7) There is capability for the host processor to read the value of the RT flag status bit (via bit 7 of Configuration Register #1 in RT ENHANCED MODE).

(8) EFA/STANAG-3838 compliant RTs **must not implement** the DYNAMIC BUS CONTROL, SELECTED TRANSMITTER SHUTDOWN, and OVERRIDE SELECTED TRANSMITTER SHUTDOWN mode commands. The Mini-ACE provides the capability to illegalize any or all of these mode codes, under software control.

(9) STANAG-3838 for EFA requires that all RTs **must implement** the following mode commands: Synchronize without data, Synchronize with data, Transmit status word, Initiate self-test, Override transmitter shutdown, Reset remote terminal, Transmit vector word, Transmit last command, and Transmit BIT word. The ACE, Mini-ACE (Plus), and Enhanced Mini-ACE RTs implement all of these.

(10) In addition to Service request, STANAG-3838 for EFA requires implementation of the following RT status word bits: Broadcast command received, Busy (per MIL-STD-1553B Notice 2), Subsystem flag, and Terminal flag. It requires that the Dynamic bus control acceptance bit not be used. All of the ACE series RTs meet all of these requirements.

(11) All ACE RTs meet the EFA STANAG-3838 RT requirement for implementing all 30 non-mode code subaddresses (1-30).

(12) Regarding RT address: EFA/STANAG-3838 requires that this be user settable in accordance with MIL-STD-1553B Notice 2. Notice 2 requires that "no single point failure shall cause a terminal to validate a false address." The ACE series RTs meet this requirement by the inclusion of its RTADP (RT Address Parity) input signal.

ACE AND MINI-ACE

ACE AND MINI-ACE: WHERE ARE THEY USED?

Q. Could you please supply me with a specific aerospace industry use for the Mini-ACE product?

A. Our MIL-STD-1553 terminals are used in a wide variety of avionics applications. These include mission computers, flight control computers, displays, transducers, data storage systems, memory loader/verifiers, stores management systems, and missiles. Our 1553 terminals are also used in space applications, including satellites, launch vehicles, space vehicles, and the International Space Station. MIL-STD-1553 is also used on tanks and other ground vehicles.

ACE VS. MINI-ACE/MINI-ACE PLUS

Q. What are the differences in pinout and features of the ACE vs. the Mini ACE and Mini-ACE Plus?

A.(1) The ACE includes a TAG_CLK Input signal. There is no TAG_CLK input on the standard Mini-ACE. We have found that most ACE users do **not** require this input signal. Without using TAG_CLK, you have software programmable options of 2, 4, 8, 16, 32, and 64 µs/LSB, with 64 µs/LSB being the most commonly used time tag resolution. Use of the TAG_CLK input (for the original ACE) allows for other resolutions; for example, 10 or 20 µs/LSB.

(2) The Mini-ACE does **not** include a MEMENA-OUT output signal. This feature is not required for the Mini-ACE buffered mode. If you design for transparent mode, the signal MEMENA-OUT (low) may be derived by gating IOEN (low) **OR** DTACK (low).

(3) The Mini-ACE (Plus) does **not** bring out the INCMD output signal.

(4) For Mini-ACE (Plus), the register bit EXPANDED CROSSING ENABLED (bit 11 of Configuration Register #6) is obsolete. That is, expanded zero crossing, in which

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the 1553 Manchester decoders sample using **both** edges of the clock input (CLK_IN) is **always enabled**. As a result, the Mini-ACE's duty cycle tolerance for CLK_IN is tightened from 33% to 67%, to 40% to 60%.

Q. Are there any features that the BU-61688 Mini-ACE has that the BU-61586 ACE does not have?

A. Yes.

(1) For Mini-ACE, the TX_INH_A and TX_INH_B input signals are pinned out. For the ACE, these signals are generally not brought out, except for the BU-61586X6 (5 volt) versions.

(2) The BU-61688 (Mini-ACE Plus) has 64K X 16 of internal shared RAM, in comparison to the BU-61586 (ACE), which has 12K X 16 RAM.

(3) The BU-61688 Mini-ACE, like the BU-61586 ACE, allows the use of 16 MHz or 12 MHz clock inputs. However, if your board has a 10 MHz or 20 MHz clock available, the BU-61689 version of the Mini-ACE Plus can use either of these.

(4) In the BU-61688's (Mini-ACE Plus) BC mode, register #0B, the BC FRAME TIME REMAINING REGISTER, will return the actual frame time remaining. For the BU-61586 ACE, this register will return a value of zero.

Q. Are the BU-61585 ACE and the BU-61689 Mini-ACE Plus pin compatible? Are there other differences?

A. (1) They are **not** pin compatible. The BU-61585 is in a 1.0 X 1.9 inch package. The BU-61689 is in a 1.0 X 1.0 inch package.

(2) The BU-61585 runs off either a 12 MHZ or 16 MHZ clock, while the BU-61689 runs off a 10 MHZ or 20 MHZ clock. The BU-61688 is identical to the BU-61689, but runs off a 12 MHZ or 16 MHZ clock.

(3) BU-61585 has 12K X 16 of RAM (or, alternatively, can be configured to have 8K X 17), while the BU-61689 (or BU-61688) has 64K X 16 of RAM.

Q. Have both the ACE and Mini-ACE passed MIL-STD-1553 RT validation testing?

A. Yes. The Mini-ACE hybrid, which incorporates a 5V (only) transceiver (there are no 15V or 12V versions of the Mini-ACE) **has passed** the MIL-STD-1553 RT Validation Test Plan (VTP). This test comprehensively exercises both the transceiver and protocol (logic) portions of the Mini-ACE hybrids. The Mini-ACE passed the RT VTP **at all three temperatures** (-55, +25, and +125 degrees C). We have a test report available. If you would like a copy, we can supply it.

In addition, Appendix E of our ACE User's Guide is a report of the BU-61580D2-110 ACE passing the RT VTP. The RT protocol chip used in the Mini-ACE and Mini-ACE plus (BU-61688/89) hybrids includes the same RT protocol functionality as the protocol chip used in the original BU-61580 ACE hybrid.

MINI-ACE VS. MINI-ACE PLUS

Q. What are the pin compatibility issues between Mini-ACE and Mini-ACE Plus?

A. For the Mini-ACE (BU-65178/61588), the upper four address lines (A15-A12) are not used. However, use of the 4K RAM (Mini-ACE) version with the 4 address lines connected to A15-A12 provides a compatibility path to the BU-61688/89 Mini-ACE Plus with its 64K of RAM. For the BU-65179 Mini-ACE RT with auto-boot, these signals take on different functions, and should not be connected to A15-A12.

ACE AND MINI-ACE: GENERAL

Q. What is the purpose of the ACE's TX_INH (Transmit Inhibit) input signals?

A. These provide a hardware mechanism for shutting down a faulty 1553 transmitter. In addition, these signals may be used to ensure that a Mini-ACE (Plus) cannot transmit when configured for monitor mode. Also, the TX_INH inputs provide compliance to the EFA/STANAG-3910 spec.

Q. I have a question concerning the Mini-ACE's TX_INH_A and TX_INH_B signals. Do these need an external pull down if not used?

A. For normal operation (i.e., assuming that you want to use, rather than shut off, the 1553 transmitters), the TX_INH_A and TX_INH_B inputs should be hardwired to logic "0" (ground).

Make a **direct connection** to ground, rather than through a pull-down resistor. A pull-down resistor (e.g., 10K ohms) will **not** provide a reliable logic "0" connection, due to leakage current (the max leakage I_{IL} is about 400 µA).

Q. The way we've always configured the ACE and Mini-ACE is for the 16-bit Buffered Mode. Is it correct to say that they use DMA?

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A. Sort of. The memory configuration of the ACE/Mini-ACE's buffered mode is referred to as "shared RAM", rather than DMA. However, in operation, the shared RAM interface uses a DMA-type mechanism in that there are data transfers between the Mini-ACE's protocol logic (encoder/decoder and memory management logic) and the internal shared RAM, that take place **not** under CPU control.

That is, these transfers take place **autonomously**, independent of the host CPU. Since the host processor may also access this internal shared RAM, the Mini-ACE includes internal arbitration logic. This logic acts as a "traffic cop," to enable, at any point in time, for either the host processor or the Mini-ACE's internal logic, **but not both simultaneously**, access to the shared RAM.

Q. What is the ACE/Mini-ACE's radiation tolerance?

A. In 1995, we had radiation testing performed on a BU-61581 ACE, with 1.25 micron J' protocol chip and 15V transceiver. Quoting from the report of this testing: at 2.8K rads, 5K rads, and 10K rads; and, for neutron fluences of $1.20 \cdot 10^{12}$ and $2.80 \cdot 10^{12}$, "The devices encountered no failures at this level." There were no single event effects exhibited at proton fluences of $1.0 \cdot 10^{10}$ protons/cm^2.

Q. We are using the BU-61580 as a 1553 bus controller. We are only using bus A and not bus B. Do we need to terminate bus B on pins 34 and 35, and, if so, what is the easiest way of doing it? We don't want to use the 1.4:1 transformer if not necessary, because of the extra cost.

A. As long as you're not using bus B, there's no need for a coupling transformer or termination resistors.

Q. Are there any special grounding considerations for the Mini-ACE?

A. In the original ACE, the analog (transceiver) and digital grounds are not connected together inside the hybrid. In the Mini-ACE, as a means of reducing the effects of ground bounce, these grounds **are** connected together inside the hybrid.

Basically however, the same rules apply: when transmitting, the large ground currents flow through the transformer (primary) center tap, not through the hybrid ground pins. Therefore, you still need to:

(1) Connect all three Mini-ACE ground pins directly to the (digital) ground plane.

(2) Use heavy ground traces to the transformer center tap connections.

(3) This trace (to the transformer center taps) should connect through a low-impedance path to the +5V power supply return. Alternatively, you can connect this trace directly to the board's ground plane, assuming that the ground plane serves as both analog and digital ground (and return paths).

(4) Of course, the ground and supply planes should NOT extend directly under the transformers or the analog signal traces. The added capacitance could make the terminal's input impedance fall below the 1553B stub-coupled minimum of 1000 ohms.

Q. For the BU-61588 Mini-ACE, please clarify the note regarding decoupling capacitors. Are one 10 µf and one 0.1 µf recommended for each of the two Vcc pins for a total of two 10 µf and two 0.1 µf?

A. For the BU-61588, it is recommended to put individual 10 µf and 0.1 µf capacitors near **each** of the two transceiver power pins (20 and 72). Pin 72 is the +5V power input to the Channel A transceiver, while pin 20 is the +5V power input to the Channel B transceiver.

To minimize the trace lengths (and therefore parasitic inductance) to each of these power inputs, it is best to provide separate decoupling for each.

Q. For the BU-65179, how is the clock frequency specified? Also, how does the RT AUTO-BOOT function work?

A. For the BU-65179, CLK_SEL_1 and CLK_SEL_0 are used to designate the frequency of the CLK_IN input as follows:

CLK_SEL_1	CLK_SEL_0	Clock Frequency
0	0	10 MHz
0	1	20 MHz
1	0	12 MHz
1	1	16 MHz

As for the RT_BOOT_L signal: if it is connected to logic "1", the BU-65179 initializes in "Idle" mode. In this case, it is necessary for the host processor to write values of logic "1" and logic "0" to bits 15 and 14 respectively of

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Configuration Register #1 to put the BU-65179 online as a functioning (responding) RT. In addition, all of the RT status word bits will be either set or cleared as the result of writing to Configuration Register #1.

If RT_BOOT_L is connected to logic "0," the BU-65179 will initialize as a functioning RT **without** having to write to Configuration Register #1. In addition, the RT status word "Busy" bit will initialize as set, while all of the other RT status word bits will initialize as cleared. That is, the BU-65179 RT **will respond** with its "Busy" bit set **immediately** following power turn-on.

ACE AND MINI-ACE: BC MODE

Q. For Mini-ACE/Mini-ACE Plus and Enhanced Mini-ACE BC, how does intermessage gap timing work?

A. For Mini-ACE (Plus) and Enhanced Mini-ACE, the BC provides a "time-to-next-message" parameter (rather than true "intermessage gap time") for each BC message. The "time-to-next-message" parameter defines the time from the start of the current message to the time of the start of the subsequent message.

In addition, the BC architecture of the Enhanced Mini-ACE enables you to implement a true "intermessage gap time" function by means of the DLY (delay) instruction. The delay time is programmable in 1 µs steps, up to 65.535 ms. The overall intermessage gap time will then be approximately 10 µs plus the value of the DLY parameter.

Q. For the Mini-ACE BC, when will the BC END_OF_FRAME interrupt occur?

A. The BC END_OF_FRAME interrupt is issued at the completion of the last message of the frame, **regardless** of whether or not the Intermessage Gap Time (time-to-next-message) timer and/or the BC frame timer have timed out.

Q. For the ACE BC mode, is the time tag word written at the start of a message, the end of a message, or both?

A. The Time Tag word is written to the BC descriptor stack during the start-of-message sequence **and** again during the end-of-message sequence.

Q. What must the RT address input be when the device is used only as a BC?

A. For BC operation, it doesn't matter. However, if you plan on running the ACE/Mini-ACE self-test vectors, you **must** connect the RT address inputs RTAD4-RTAD0 to a valid RT address (0 to 30) with correct parity (i.e., odd parity for RTADP) in order for the self-test vectors to pass.

Q. Are there any pull-ups required on the Mini-ACE RT address signals?

A. The Mini-ACE's RT address signals include internal pull-ups. Actually, these are active current sources (from +5V), with the current values between approximately 50 and 400 µA. For best noise immunity, the RT address inputs should be connected **directly** to either +5V or LOGIC GROUND. In particular, pull-down resistors should not be used.

Q. Am I correct in assuming that the BC command stack (in ENHANCED mode) rolls over at multiples of 4*(Selected Command Stack Size)?

A. No. The size of the BC/RT command stack is programmable by means of bits 14 and 13 of Configuration Register #3. The four choices are:

Bit 14	Bit 13	Stack Size
0	0	256 words (64 messages)
0	1	512 words (128 messages)
1	0	1024 words (256 messages)
1	1	2048 words (512 messages)

For example, if bits 14 and 13 are both "0," the stack will roll over every 256 words, or 64 messages. The stack will roll over at an address equal to **modulo the programmed stack size** (e.g., 256, 512, ...).

Q. Does the Mini-ACE have a combined BC/Monitor mode?

A. No, the ACE does not include an explicit BC-MT mode. However, with the Mini-ACE bus controller mode, you essentially get a monitor for "free." In the ACE's BC message block, **all** of the words of a message are stored: that is, the BC's Command Word, the RT's Status Word (including **both** status words for an RT-to-RT transfer), and any and all Data Words transmitted by the BC or the RT. In addition,

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the Mini-ACE will flag any error conditions: either failure of its own loopback test, and/or any no responses or errors in responses from RTs. So, in essence, you're getting all the functions of a bus monitor with the ACE's BC mode. Also, the Mini-ACE **does** include a combined RT/Monitor mode. In this mode, the ACE operates as a full-function RT for one RT address, and a selective message monitor for all other RT addresses.

Q. We are using two Mini-ACEs on two separate processor cards separated by a VME bus connection. We are trying to synchronize these two devices such that they send out minor frames or a Synchronize without data mode code message on two separate buses within a guaranteed 100 µs of each other. What mechanisms do you suggest for allowing us to do this?

A. For synchronizing between two Mini-ACEs, the external trigger is probably a good mechanism to use. To use the external trigger feature, you need to program bits 8, 7, and 6 of Configuration Register #1 as follows:

Bit 8 (FRAME AUTO-REPEAT): logic "1"

Bit 7 (EXTERNAL TRIGGER ENABLED): logic "1"

Bit 6 (INTERNAL TRIGGER ENABLED): logic "0"

This will configure the Mini-ACE for a "single frame," such that each frame may be initiated by a rising edge to the EXT_TRIG input signal, or by a software start command. The EXT_TRIG input signals should be connected together to a circuit generating this rising edge. By so doing, the Synchronize mode commands from the two Mini-ACEs will be very tightly synchronized.

Alternatively, you could use the software start mechanism; i.e., writing a value of 02h to the Start/Reset Register to each of the two Mini-ACEs. As long as you perform these two write cycles within a few microseconds, the start of transmission for the two Synchronize (without data) mode commands will be tightly synchronized.

ACE AND MINI-ACE: RT MODE

Q. For the BU-65178, what means are there for specifying RT address?

A. There are three methods:

(1) Hardwire RT_AD_LAT to logic "0." This will configure the RT address to be hardwired, by means of RTAD4-RTAD0 and RTADP.

(2) Hardwire RT_AD_LAT to logic "1." In this configuration, the BU-65178's RT address will be programmable by means of Configuration Register #5. Note that when you write Configuration Register #5, the RT address will be latched from the RTAD4-RTAD0 and RTADP pins, and not from the processor address bus (D15-D0). However, if you connect RTAD4 to D5 .... RTAD0 to D1, and RTADP to D0, this will allow the RT address to be software programmable.

(3) Include a circuit to provide a low-to-high transition on the RT_AD_LAT input pin (sometime **after** $\overline{\text{MSTCLR}}$ has settled to logic "1"). This will cause the values presented on RTAD-4-RTAD0 and RTADP to be latched internally on this rising edge.

Q. What is the function of the BU-65178 Mini-ACE's $\overline{\text{SSFLAG}}$/EXT_TRIG input?

A. For the BU-65178 RT Mini-ACE, the **only** function of the $\overline{\text{SSFLAG}}$/EXT_TRIG input signal is as a $\overline{\text{SSFLAG}}$ (Subsystem Flag) input. The "EXT_TRIG" function is not applicable to the BU-65178 RT. EXT_TRIG is a BC and Monitor function that is only applicable to the BU-61588 Mini-ACE BC/RT/MT, and the BU-61688/89 Mini-ACE Plus BC/RT/MT.

If $\overline{\text{SSFLAG}}$ is connected to logic "0," this will cause the Subsystem Flag bit in the RT Status word to be set to logic "1." If $\overline{\text{SSFLAG}}$ is connected to logic "1," the value of Subsystem Flag will be determined by the software programming of Configuration Register #1. Therefore, if you don't intend to use this function, I recommend that you hardwire $\overline{\text{SSFLAG}}$/EXT_TRIG to logic "1."

One use of the $\overline{\text{SSFLAG}}$ input is to provide a hardware mechanism for a processor watchdog timer to be able to signal to the 1553 RT that it has timed out (i.e., that the processor has hung up).

Q. We have connected the Mini-ACE's $\overline{\text{SSFLAG}}$ input pin to a processor watchdog timer circuit. Whenever the host fails to retrigger the watchdog timer, the $\overline{\text{SSFLAG}}$ pin is latched low in order to indicate a sub-system malfunction/failure. We are looking to run a power-up built-in test on the watchdog circuit, such that when we allow this timer to time out we can read the RT Status Word (Register 0E) and verify that the $\overline{\text{SSFLAG}}$ bit is indeed set.

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The problem is that the SSFLAG pin is sampled and the Status Word is updated only during a Start-of-Message (SOM) sequence. An SOM can occur only when the RT receives a command from the external Bus Controller. At the time when we want to run this test, we cannot tell whether the Bus Controller is up and running. The test may therefore fail either due to a watchdog failure or a delayed BC start-up.

The question is: is there a way to cause the RT to sample the SSFLAG input pin and update the Status Word without waiting for an SOM to occur? That is, is it possible to trigger a SOM from the host side?

A. **Yes**. There is a way of causing the RT Status Register to update. It involves use of the Enhanced Mini-ACE's test mode. Here's what you need to do:

(1) Cause the watchdog timer to time-out, which will cause the Enhanced Mini-ACE's SSFLAG input signal to be logic "0."

(2) Read the RT Status Word Register (register address 0E). If SUBSYSTEM FLAG, bit 2 of this register, returns logic "1," then you can skip the following steps. If this bit is logic "0," then you need to perform steps (3) through (7).

(3) Make sure that the Enhanced Mini-ACE is programmed for RT mode, and that ENHANCED MODE is enabled; i.e., bit 15 of Configuration Register 3 is logic "1."

(4) Read, and then re-write, Configuration Register #4, setting the value of the three lower bits to 111 (binary). This will put the Enhanced Mini-ACE in GENERAL TEST MODE.

(5) Write a value of 2000 (hex) to Test Mode Register 3 (register address 13 (hex)). This will cause the RT Status Word Register to update (as if a message has been received from the BC).

(6) Read, and then re-write, Configuration Register #4, this time setting the value of the three lower bits to 000 (binary). This will put the Enhanced Mini-ACE back into its normal RT mode of operation.

(7) Once again, read the RT Status Word Register (register address 0E). If SUBSYSTEM FLAG, bit 2 of this register, returns a value of logic "1," then the test has passed.

Q. For Mini-ACE, I understand the hardware setting of RT Address. One design we saw had a "software settable option," by writing to a register. My assumption is that this must use an external register outside the ACE, is that correct?

A. The Mini-ACE's software programmable RT address does not require an external register. For the BU-65178/79 or BU-61588 Mini-ACE or the BU-61688/689 Mini-ACE Plus, the steps to use the software programmable RT address feature are as follows (the first two steps are hardware design; the last four steps are software programming):

(1) Connect the signal RT_AD_LAT to logic "1."

(2) Connect RTAD4 to data bus D5, RTAD3 to D4, …, RTAD0 to D1, and RTADP to D0.

(3) Program the ACE for ENHANCED MODE, by setting bit 15 of Configuration Register #3 to logic "1."

(4) Enable the RT address to be software programmed by setting LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5 (bit 3 of Configuration Register #4) to logic "1."

(5) Program the RT address by writing to Configuration Register #5, using the bit mapping defined in step (2).

(6) To prevent the software from inadvertently changing the RT address, clear LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5 (bit 3 of Configuration Register #4) to logic "0."

Q. If the host sets the SERVICE REQUEST bit in Configuration Register #1 to logic "0," and the "Clear Service Request" feature is used, is it possible for the BC to not see the Service Request bit set to logic "1" in the RT Status Word?

A. Yes. If the host sets SERVICE REQUEST to logic "0" between the SOM and EOM sequences for a Transmit vector word mode code message, the ACE RT will respond with the Service Request status bit equal to "0," and the SERVICE REQUEST register bit will automatically clear to logic "1." Therefore, the BC will never see the Service request bit set to logic "1." The rationale for this is that the BC should only send a Transmit vector word mode command after it has detected a Service request bit of logic "1" in a previous message.

Q. When the time tag is loaded on a Synchronize with data mode command, and the time tag resolution is 64 µs/LSB, does the counter wait

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64 µs before it increments? That is, is the resolution countdown cleared when the time tag value is loaded, or is it free running?

A. The Time Tag counter is loaded **immediately** (i.e., asynchronously) following receipt of the data word for a Synchronize (with data) mode code. In addition, the 64 µs clock circuit is reset to zero at this time. That is, the time tag counter won't increment an LSB until a **full 64 µs** has elapsed.

Q. If ENHANCED MODE CODE HANDLING is enabled, for a receive mode command, will the data word be stored in the third word of the message descriptor in the RT stack and/or the individual fixed location in shared RAM? On a transmit mode command, where will the Mini-ACE read data from?

A. For a receive mode command with data, the data word will be stored in both places: the third word of the message descriptor **and** the enhanced mode code data table. For mode commands without data, the third word of the descriptor will not be written to. For a transmit mode code command, the data will be read from the enhanced mode code data table and written to the third word of the descriptor.

Q. I have a question about the RT subaddress double-buffering mode. For broadcast receive subaddress 19 programmed for double-buffered mode, the first transmission from the bus controller goes to 0x4A0, as it should because this is block 0 of the buffer. The second set of data should go to 0x4C0 -- block 1 of the buffer, but it does not. The data ends up at 0x480. This is 32 words below the base address of the buffer, rather than 32 words above the base address of the buffer.

If I move the base of the buffer to 0x4C0, the double buffering works fine. The first transmission from the BC goes to 0x4C0 and the second transmission goes to 0x4E0. It also works normally if I change the base of the buffer to 0x540. But, if I move the base of the buffer to 0x5A0 the problem occurs again. The first transmission goes to 0x5A0 and the second transmission goes to 0x580 when it should go to 0x5C0.

A. The way the subaddress double buffering works is that after a valid message is received to a receive(/broadcast) or broadcast subaddress with double buffering enabled, then bit 5 of the lookup table pointer will be **toggled**.

That is, the updated lookup table pointer value = (old lookup table pointer value **XOR** 32), and **not** (old lookup table pointer + 32).

In other words, if the pointer's value is initially XXXX XXXX XX00 0000, it becomes XXXX XXXX XX10 0000. Similarly, if it's value is XXXX XXXX XX10 0000, it "ping-pongs" to a value of XXXX XXXX XX00 0000.

Q. We are using a Single Board Computer VME card with a BU-61580 ACE. What happens when a Bus Controller (also using a BU-61580) tries to communicate with a BU-61580 whose RT address is correct, but parity is incorrect?

A. A BU-61580 RT configured with an incorrect RT Address parity bit will **not** receive or respond to commands to its own RT address. Note however that the BU-61580 will still be able to **receive** commands and data sent to the broadcast address (address 31).

ACE AND MINI-ACE: MONITOR MODE

Q. For using the Mini-ACE in Monitor mode, can I use the two RAM areas A and B to organize double buffering?

A. Yes. That way, you can "ping-pong" between the two areas. While one is storing 1553 monitored data, the second one can be read out by the host processor.

Q. Current area (A or B) command or data stack overflow causes the stack pointer to wrap to the beginning of the same stack, so that in the case of the data stack this causes corruption of the oldest message. Correct?

A. Yes, the command and/or data stack pointer(s) will roll over to the top of the stack. As you point out, this can cause message corruption. What I suggest to avoid such a problem is that when your host processor initializes the stack pointer, to position it down from the top.

In the case of the monitor data stack, I would allow for 35 words at the top of the stack, to accommodate the maximum size message to be received; i.e., an RT-to-RT transfer, with the second command word + 32 data words + 2 status words. Similarly, for the monitor

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command stack, I would suggest initializing the stack pointer such that there are four locations -- the size of one message descriptor -- free at the top of the stack.

For the BU-61588 (4K internal RAM), what I would suggest is to use a monitor command stack size of 256 words for each of area A and area B. Likewise, for the monitor data stack, I would use a stack size of 1024 words for each of the two data stacks.

For the case of the Enhanced Mini-ACE, the **50% rollover interrupt** feature should be used. That is, the monitor may be programmed to issue interrupt requests when the monitor data stack **and/or** the monitor command (descriptor) stack is 50% or 100% full. In this way, the host can read data from the most recently filled half data stack or half descriptor stack, while the monitor continues to store new data received from the 1553 bus in the other half stack.

Q. When will the corresponding interrupt (rollover) occur? The stack pointer rollover event is not reflected in the MT SOM or EOM sequence.

A. For the command stack, the command stack rollover interrupt occurs at the beginning of a received message. For the monitor data stack rollover, the interrupt occurs at the **end of the message** that resulted in the rollover. In either case, the event will be reflected in the Interrupt Status Register (assuming that interrupts are enabled for these events).

Q. Let's suppose, for example, that Monitor Command Stack Pointer A (0x0102) is given an initial value of 0x0600 and the Monitor Command (descriptor) Stack size is 256 bytes. I thought that the command data is then written into addresses 0x0600 through 0x0500 and the next byte of command data will be written once more into 0x0600 address, isn't it? If I initialize Pointer A to 0x05FC, will it roll over to the 0x05FC address?

A. If you initialize for a Command Stack size of 256, and initialize the Command Stack Pointer A (location 0x0102) to a value of 0x0600, it will increment by four (4) at the **start** of each received (monitored) message. That is, it will increment to 0x0604, 0x0608, ... 0x06F8, 0x06FC, before rolling back to 0x0600.

By so doing, note that the 4-word descriptor for the first monitored message received and stored will be stored in locations 0x0600-0x0603. The descriptor for the second received message will go in 0x0604-0x0607, ... the descriptor for the 64th message will go in 0x06FC-0x06FF and, if enabled, a Monitor Command Stack Rollover interrupt will be generated at the start of that (the 64th) message. The descriptor for the 65th message will then overwrite that for the first message, in locations 0x0600-0x0603.

Q. Suppose I do the following: Initialize stack to 0x600, for example, and interrupt on stack rollover. This interrupt will be of highest priority and the first that I will do will be area switching. According to my calculations, I have at least 27 µs for area switching, which is more than enough for me.

A. That should work OK. I just suggest that during your interrupt service routine that you initialize the (A or B) Command Stack pointer to 0x0604, rather than 0x0600.

The reason is that 27 µs could be marginal for the case where the message which caused the command stack rollover is a broadcast mode code with no data words. In this case, if the inter-message gap time is 4 µs (per -1553B), there could **theoretically** be a gap time between the start of successive messages of about 22 µs. By initializing to 0x0604 rather than 0x0600, the message descriptor stored at 0x0600-0x0603 will not be overwritten.

Note, however, that the minimum inter-message gap for most bus controllers is approximately 10 µs (or more).

Q. Can I reinitialize the Command (or Data) stack pointer "on the fly"? And if yes, when is this new value taken in to consideration by firmware?

A. You may reinitialize (write to) the Command Stack Pointer location **at any time**. The Mini-ACE includes an arbitration circuit, to prevent "crashes" between memory accesses by the internal logic circuitry and by your host processor.

Keep in mind, the digital portion of the BU-61588 does **not** include any internal processor or "firmware." It's a state machine logic circuit.

The Monitor Command Stack pointer is sampled to determine the starting location for the current message's 4-word descriptor, **and** incremented by four, **and** re-written during the monitor start-of-message (SOM) transfer sequence.

The Mini-ACE arbitration logic prevents you from writing to memory (e.g., the Monitor Command Stack Pointer) **during** the monitor SOM transfer sequence.

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Therefore, if you write to the stack pointer **before** the SOM sequence, the **new** value will be used for the next message that comes in. However, if you write to the Command Stack Pointer **after** the SOM sequence for a message that has occurred, then **that** (current) message will store its descriptor information (Block Status Word, Time Tag, etc.) at the **old** (previous) location; that is, the one that was accessed during the message's SOM sequence.

If you initialize the Command Stack Pointer to 0x0604, then the 64th message, which will result in a Command Stack Rollover Interrupt (if enabled) at the **start** of the message, will result in the descriptor to be stored in 0x0600-0x0603. Therefore, if your interrupt service routine does not react fast enough, the 64th message will **not** overwrite a descriptor in 0x0600-0x0603, since there was no descriptor stored there previously.

Q. For the Mini-ACE's selective monitor mode, when do the Monitor Command Stack and Data Stack rollovers occur?

A. The way that the Monitor Command Stack and Data Stack operate is that they always roll over at an address boundary of **modulo the programmed stack size**, regardless of the values that the pointers were initialized to.

Q. It appears that the Mini-ACE Message Monitor ignores a "No Response" error condition when there is a data word with parity error in the message. Is this correct?

A. The ACE monitor **stops** monitoring once an error (for example, a parity error) is detected in a message. Therefore, the monitor will **not** detect a subsequent response timeout condition in the same message. In fact, if there is a response to a message with an error (e.g., parity), the monitor will interpret the status word as the command word for a new message.

ACE AND MINI-ACE: INTERRUPTS

Q. Will the Interrupt Status Register's MASTER INTERRUPT bit be set for an event/condition that is masked "disabled?"

A. No. MASTER INTERRUPT will only occur for an event/condition that is enabled by means of the Interrupt Mask Register.

ACE AND MINI-ACE: TROUBLESHOOTING

Q. My BU-61580 RT doesn't respond to commands from the bus controller. What should I look at?

A. Here are a few things that you can look at:

(1) You need to make sure that RDAD4 through RTAD0 are connected to +5V or GROUND for the correct desired RT address **and** that the RT address parity signal, RTADP, is connected to +5V or GND, to ensure a correct odd parity sum. That is, the number of logic "1"s for RTAD4-RTAD0 AND RTADP must be an odd number. For example, if your desired RT Address is 0, then RTADP must be connected to logic "1." If the RT address parity is incorrect, the BU-61580 RT will not recognize any messages that the BC sends to its RT address.

(2) You need to provide a properly terminated 1553 bus (that is, 70 to 85 ohms at each end of the bus). An unterminated bus may result in transmission line reflections, resulting in waveform distortions. In such a case, the RT may not recognize an otherwise valid message from the bus controller.

(3) Make sure that you have a clean 16 MHZ clock input to CLK_IN. Note that 16 MHZ is the default clock frequency for the BUS-61580. You may also use a 12 MHZ clock for the BU-61580, but this would require you to modify your initialization software by programming for ENHANCED mode and then programming bit 15 of Configuration Register #5 to logic "1."

In addition, you need to make sure that the clock input has a duty cycle in the range of 40% to 60%, and does not have significant undershoot, overshoot, or transition noise on the rising and falling edges. If you see any of these types of problems, they are generally layout related: either transmission line type reflections (possibly from long - more than 1 or 2 inches - "stub" traces) and/or from crosstalk from other signals on your board.

(4) You need to make sure that the center taps of your isolation transformers are grounded on the "primary" side; that is, the side of the transformers connected to the BU-61580. If you don't ground the center taps, you **might** be able to receive messages from the bus controller, but the BU-61580 RT won't be able to transmit any responses.

Q. We have a custom DSP board with two BU-65170 Mini-ACEs. On occasion, one of the BU-65170s stops

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generating interrupts to the DSP following reception of BC-RT messages. I have not been able to pin this event on anything the DSP is doing. I have two questions:

(1) What can cause the interrupts to stop? The Interrupt Mask Register (00h) is not being corrupted and the messages on the 1553 bus are still valid. I believe the BU-65170 is responding with correct status since our monitor is not showing any errors, but I have not verified this by hooking a scope to the bus.

(2) What is the best way to "jump start" the 65170 when this happens?

A. You say that the Interrupt Mask Register is not getting corrupted. Here are some things for you to consider:

(1) You should determine whether or not the BU-65170's descriptor stack pointer continues to increment. If it does, this points to an "interrupt-specific" type of error. In this case, you should read the value of the messages' Block Status Words to try to gain insight into the problem.

If the stack pointer is not incrementing, this points to an error receiving and processing valid messages from the 1553 bus. This could possibly be a bus controller, termination, transformer, or other electrical problem; an inadvertent change in the BU-65170's RT address; a power glitch; an inadvertent hardware reset (MSTCLR input pulsing low); or a software problem (e.g., inadvertently writing an incorrect value to a register).

(2) What interrupt are you enabling? EOM? Others?

(3) Is the BU-65170's interrupt output (INT) configured as a pulse or level type signal (bit 3 of Configuration Register #2)? Remember, if it's configured as a level, you won't get a subsequent interrupt until you first clear the INT output and Interrupt Status Register from the previous interrupt.

(4) Are you using INTERRUPT STATUS AUTO CLEAR (bit 4 of Configuration Register #2)? If you are not, it is necessary to write a value of "1" to bit 2 (INTERRUPT RESET) of the Start/Reset Register in order to clear the Interrupt Status Register and the INT output (if it's programmed for "level"). If INT is programmed to provide a level type of interrupt and is not cleared following the first interrupt request, then the host will not detect subsequent interrupt requests.

(5) Another thing that you might look at: try setting ENHANCED INTERRUPTS, bit 15 of Configuration Register #2 to logic "1" (note that to use this feature, it is first necessary to write a value of logic "1" to ENHANCED MODE, bit 15 of Configuration Register #3). By doing this, it is possible for bits in the Interrupt Status Register to become set, even if the respective events/conditions have been disabled from causing interrupt requests. Therefore, I would suggest to write a value of 0000h to the Interrupt Mask Register to disable all interrupts, and then periodically poll the Interrupt Status Register. In this scenario, the ISR bits (e.g., EOM) should still become set. Of course, it will then be necessary to clear the ISR by either AUTO-CLEAR, or by writing a value of 0004h (INTERRUPT RESET) to the Start/Reset Register.

(6) You need to make sure that the values of registers other than the Interrupt Mask Register are not changing. For example, that the upper two bits (15 and 14) of Configuration Register #1 are staying as "1" and "0" respectively (for example, a combination of "0" and "0" will cause the BU-65170 to revert to its "idle" (non-active) mode.

(7) You need to verify that the BU-65170's RT address (and parity) inputs are not changing.

(8) Finally, you need to ensure there isn't a hardware related problem between the BU-65170's INT output and your DSP's interrupt request input, such as logic related to interrupt requests from other hardware circuits.

ACE AND MINI-ACE: SELF-TEST ISSUES

Q. How is the Mini-ACE put into its general test mode?

A. By setting the MSB (bit 15) of Configuration Register 3 (ENHANCED MODE), and then writing a value of 7 (111) to the three LS bits of configuration register 4.

Q. How are the test vectors interpreted?

A. To illustrate by example:

V W R 0003 0001 means a vector write to register 3 the value 0001.

V R R 0000 0040 means a vector read (and verify) of register 0 the expected value 0040.

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V W M 0000 0655 means a vector write to memory location 0 the value 0655.

Q. I downloaded the test vectors from the DDC web page. It turns out that there is an acelib function that loads and executes these vectors. The function is called BuVectorTest(). I've used BuVectorTest() to run the BC/RT/MT vectors (TEST.VEC) on our Radstone PMC1553 card.

There appear to be only a couple of failures, all in the "Interrupt Status Register & Interrupt Mask Tests" section. Could you take a quick look at the failures below?

The first failure is at line 85 of TEST.VEC:

V R R 0013 ECEB

the register address 0013 (hex) appears to be test mode register 3, which isn't documented in the ACE user's guide. The expected data is ECEB, but we get ECFB.

If I comment out line 85 (with the letter 'D' at the beginning of the line), I get a second failure at line 86 of TEST.VEC:

V R R 0006 FFFF

It looks like we want the ISR to be FFFF (it was set to this value at line 84). Instead, we get a value of 0 from the ISR. Should it be possible to write to the ISR and expect to get back what we wrote to it (in test mode)?

A. The problem that you are seeing has to do with the ACE's host processor responding to an interrupt request, and then reading the ISR (Interrupt Status Register). As a result, the value of the ISR is getting cleared to 0.

Test register 0013h is a reading of the ACE's internal state. Register 0006 is the ISR.

To prevent this problem from occurring and to enable your ACE to pass self-test, you will need to either:

(1) Have the ACE's host processor disable interrupts during self-test; or

(2) Make sure that the ACE's host processor does NOT read the value of the ACE's ISR during the interrupt service routine while you are in self-test.

Q. Is there any means to exercise, and therefore test the ACE/Mini-ACE/Enhanced Mini-ACE/SP'ACE's transmitter fail safe timer? Verifying the operation of this circuit is required by the RT Validation Test Plan (paragraph 5.2.1.3.7).

A. To induce a transmitter timeout condition for the ACE/SP'ACE/Mini-ACE, set the lower three bits (TEST MODE) of Configuration Register #4 to a value of 4 (100). This configures the ACE test mode for "Failsafe timer" test mode. When you do this, the ACE will transmit until a timeout condition occurs for **every transmission**. That is, for every RT response, or for every BC message transmitted. The value of the failsafe timeout timer is either 668 µs for ACE or SP'ACE, or 660.5 µs for Mini-ACE or Enhanced Mini-ACE.

Q. When we put the Mini-ACE into test mode, and issue a test command 0x2000 on Test Mode Register 3 (0x13), do we transmit any data on the bus? Being a Remote Terminal, we are not supposed to transmit anything unless actually commanded by the Bus Controller.

A. When the RT is in TEST MODE, the Enhanced Mini-ACE will **not** transmit any words on the 1553 bus.

ENHANCED MINI-ACE

MINI-ACE-TO-ENHANCED MINI-ACE UPGRADE

Q. What are the pinout differences between Mini-ACE and Enhanced Mini-ACE?

A. The Mini-ACE and Enhanced Mini-ACE have nearly identical pinouts, **with the following exceptions:**

Pin 25: For Mini-ACE, this signal is "Test Output (RX-B)". For Enhanced Mini-ACE, this signal is INCMD_L/MCRESET_L (output).

Pin 26: For Mini-ACE, this signal is "Test Output ($\overline{\text{RX-B}}$)". For versions of the Enhanced Mini-ACE with 64K X 16 RAM (BU-61864/61865), this signal is "Vcc-RAM" (+5V). For the versions of Enhanced Mini-ACE with 4K X 16 RAM, this pin is UPADDREN (see below).

Pin 37: For both Mini-ACE and Enhanced Mini-ACE, this signal is "Vcc-LOGIC". However, for the BU-61743, BU-61843, and BU-61864 versions of the Enhanced Mini-ACE, this voltage is +3.3V. For the BU-61745, BU-61845, and BU-61865 versions of Enhanced Mini-ACE, this voltage is +5V.

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Pin 65: For Mini-ACE, this signal is "Test Output ($\overline{\text{RX-A}}$)". For Enhanced Mini-ACE, this signal is LOGIC GND.

Pin 67: For Mini-ACE, this signal is "Test Output (RX-A)". For Enhanced Mini-ACE, this signal is LOGIC GND.

In addition, for versions of Enhanced Mini-ACE with 4K of RAM (BU-61843(5) BC/RT/MT and BU-61743(5) RT), note that there are different, or potentially different pin functions on the following pins:

Pin 26: UPADDREN. If this pin is logic "1," then pins 8 (A14), 66 (A15), 70 (A12), and 71 (A13) function as the upper 4 address lines, A15-A12. Note that this provides compatibility with the BU-65178 and BU-61588 Mini-ACE, and the BU-61688/61689 Mini-ACE Plus.

However, if UPADDREN (pin 26) is connected to logic "0", then the functions of these four pins behave more like the BU-65179 version of the Mini-ACE, as follows:

Pin 8: CLK_SEL_0

Pin 66: CLK_SEL_1

CLK_SEL_1 and CLK_SEL_0 are used to designate the frequency of the CLK_IN input as follows:

CLK_SEL_1	CLK_SEL_0	Clock Frequency
0	0	10 MHz
0	1	20 MHz
1	0	12 MHz
1	1	16 MHz

Note that for **all** versions of Enhanced Mini-ACE, clock frequency selection may also be done via software.

Pin 70: $\overline{\text{RT_AUTO_BOOT}}$ If this pin is connected to logic "0," the Enhanced Mini-ACE will initialize in RT mode with the Busy bit set following power turn-on. If hardwired to logic "1," the Enhanced Mini-ACE will initialize in either Idle mode (if it's an RT-only part), or as in BC mode (if it's a BC/RT/MT part).

Pin 71: Assuming that UPADDREN is logic "0," then this pin **must** be tied to Vcc-LOGIC (+5V or +3.3V).

Q. For RT operation, what are the functional and architectural differences between the Mini-ACE and the Enhanced Mini-ACE?

A. The Enhanced Mini-ACE is available in versions for which the logic sections are powered by 3.3V. The Mini-ACE is not; its logic may only be powered by +5V. In addition, the Enhanced Mini-ACE's ENHANCED CPU ACCESS feature allows for a shorter maximum holdoff time for processor-to-ACE memory and register transfers. This time has been reduced from about 2.8 µs max (at 16 MHz) for Mini-ACE, to about 600 ns max (at 16 MHz) for Enhanced Mini-ACE.

Also, for RT mode, the Enhanced Mini-ACE includes the following new architectural features:

(1) Global circular buffer. That is, a circular buffer that may be used by all subaddresses or a subset of all subaddresses. Note that both the Mini-ACE and Enhanced Mini-ACE RTs have circular buffers that may be programmable by individual subaddresses.

(2) The addition of a 50% rollover interrupt for circular buffers. Note that both the Mini-ACE and Enhanced Mini-ACE also have interrupts for (100%) circular buffer rollover.

(3) An interrupt status queue. This provides a chronology of up to the last 32 interrupts, including the reason(s) for the interrupts, and pointers to the individual message descriptors.

(4) Fully autonomous built-in protocol and RAM self-tests. For the Mini-ACE, a protocol self-test may be performed by means of the host processor writing and reading/verifying test vectors.

(5) With the Enhanced Mini-ACE, there is a bit more flexibility for implementing a software programmable RT address. That is, with Mini-ACE, to do this, RTAD4-0 and RTADP **must** be connected to D5-D0. This means you can't select between an address from an external connector or software by means of software. With the Enhanced Mini-ACE RT, you can do this fully under software control.

Q. Is a software driver developed for the Mini-ACE compatible with the Enhanced Mini-ACE?

A. The Enhanced Mini-ACE **is** software backfit compatible with the Mini-ACE, with the following two exceptions:

(1) In the BU-61588, bit 8 of the RT BIT Word Register (and in the BIT word transmitted to the BC) is CHANNEL B/$\overline{\text{A}}$. With the BU-61865, bit 8 is BIT TEST FAIL. It will set to a value of logic "1" if

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there is a failure of the Enhanced Mini-ACE's built-in protocol self-test.

(2) With the Mini-ACE, to run the protocol self-test, it is necessary for the host processor to write and read/verify the test vectors. With the BU-61865 Enhanced Mini-ACE, all the host processor needs to do is to write a register bit; the self-test vectors are then run autonomously by the BU-61865 Enhanced Mini-ACE. When the self-test is complete, an interrupt request will be issued to the host (if enabled) and the results of the self-test will be available in a register to be read. In addition, the Enhanced Mini-ACE provides a separate additional autonomous self-test for the 4K or 64K internal RAM.

Alternatively, there are self-test vectors for the Enhanced Mini-ACE that may be run from the host processor. Note however that these test vectors are **different** than those for the Mini-ACE.

ENHANCED MINI-ACE: LOGIC COMPATIBILITY

Q. Is the 3.3 volt Enhanced Mini-ACE 5 volt tolerant?

A. Yes. The 3.3V Enhanced Mini-ACE is 5 volt tolerant. The absolute maximum rating for "Logic Input Voltage" is 6.0V. The Enhanced Mini-ACE's input and I/O pad cells include clamping diodes to LOGIC GROUND, but do **not** include clamping diodes to Vcc.

Q. Are there internal pull-up resistors on the Enhanced Mini-ACE's digital inputs?

A. Yes. There are active pull-ups on all of the inputs and I/O, except for the clock input. More accurately, these are current sources from VCC, with the current value in the range from 50 to 350 µA. In addition, there are Schmidt triggers on all digital input signals (including I/Os), including the clock input.

CLK_IN is a CMOS type input. Its V_{Il} is $0.2 \bullet V_{CC}$ max, its V_{IH} is $0.8 \bullet V_{CC}$ min, and the minimum Schmidt hysterisis window is 1 volt. The other inputs are TTL type, with V_{Il} = 0.7V max, V_{IH} = 2.1V min, and a minimum Schmidt hysterisis window of 0.4V.

ENHANCED MINI-ACE: BC MODE

Q. For the Enhanced Mini-ACE, are there any "rollover" enforcements for the op-code instruction list? Same question for the Command/Status blocks.

A. There are **no** rollover enforcements for the Enhanced Mini-ACE's BC op code instruction list or for the Command/Status blocks.

Q. For the Enhanced Mini-ACE, what is the minimum BC inter-message gap time?

A. For the Non-Enhanced BC mode (i.e., **not** using the autonomous BC message sequence control engine), the nominal BC intermessage gap time for the Enhanced Mini-ACE is the same as for the Mini-ACE (Plus) hybrids, approximately 9.5 µs.

However, for the Enhanced Mini-ACE's enhanced BC mode (using the autonomous message sequence control engine), the typical value for intermessage gap time is approximately 10 clock cycles longer than for the non-enhanced BC mode. This accounts for the time for the message sequence control engine to fetch op code and parameter words from the BC Instruction List, and to execute the op code (assuming an Execute Message (XEQ) instruction). That is, an additional 1.0 µs at 10 MHz, 833 ns at 12 MHz, 625 ns at 16 MHz, or 500 ns at 20 MHz.

Also, note that if ENHANCED CPU ACCESS, bit 14 of Configuration Register #6, is set to logic "1," the Enhanced Mini-ACE's arbitration logic will interleave host transfers in between individual SOM or EOM word transfers. In this scenario, host transfers **could** have the effect of lengthening the intermessage gap time.

For each host access during an SOM or EOM sequence, the intermessage gap time will be lengthened by 6 clock cycles for each host access in buffered mode, or by 7 clock cycles in transparent mode. Since there are 7 internal transfers during SOM and 5 during EOM, this could **theoretically** lengthen the intermessage gap (for buffered mode) by up to 72 clock cycles; i.e., up to 7.2 µs with a 10 MHz clock, 6.0 µs with a 12 MHz clock, 4.5 µs with a 16 MHz clock, or 3.6 µs with a 20 MHz clock. Note that this worst case delay would only occur in the case of a burst access by the host processor.

However, note that if you set ENHANCED CPU ACCESS to logic "0," the maximum **host** wait time (i.e., maximum delay from the $\overline{\text{STRBD}}$/$\overline{\text{SELECT}}$ inputs asserted low-to-$\overline{\text{READYD}}$ output low) increases from 612 ns (for a host read) or 550 ns (for a host write) to about 2.8 µs. Therefore, the tradeoff is between increased host holdoff time (which, on average, won't occur very often) vs a potential occasional increase in the BC intermessage gap time.

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Q. Does the call stack "clear" when a Halt instruction is executed?

A. The call stack pointer clears when you start the bus controller by means of the Start/Reset Register.

Q. Does the BC General Purpose Queue pointer point to the next location in the queue? That is, in order to see the last value placed into the queue, should I examine the previous location (modulo 64)?

A. The general purpose queue pointer points to the **next** address location, modulo 64. That is, the location **following** the last location written by the BC.

Q. When using the Enhanced Mini-ACE Enhanced BC mode, is it safe to use locations 0x100 - 0x107 for messages, etc. Or should they still be "RESERVED"?

A. Yes, it is safe to use these locations for control/status blocks or data blocks. In the enhanced BC mode, these locations are not "reserved."

Q. What is the number of words in the BC Control/Status block?

A. The value of the pointer parameter in the BC instruction list (e.g., for the Execute Message instruction) **must be modulo 8**. That is, the three LSBs of this word must always be "000." The length of the Control/Status block should be:

8 words - for messages that are **not** RT-to-RT transfers and are not referenced by an XQF (Execute and Flip) instruction, or 16 words - for messages that are either RT-to-RT transfers and/or are referenced by an XQF (execute and flip) instruction.

Q. Does the op code parity bit cover just the op-code field, or the entire instruction word? What happens in the case of a parity error?

A. The parity bit covers the entire instruction code word, not just the op-code field. Note that the parity is odd. If the BC fetches an instruction with a parity error, an erroneous op code, and/or one of the "fixed value" bits (bits 9-5) is the wrong value, then the BC will trap out (halt), and the BC OP CODE PARITY ERROR interrupt will be issued, if enabled.

Q. If a masked status bit is set in an RT status response for the most recent message, will this cause the "BAD MESSAGE" condition code to be set?

A. No.

ENHANCED MINI-ACE: RT MODE

Q. How does the Enhanced Mini-ACE's RT global circular buffer option operate?

A. The RT Global Circular Buffer is a programmable option for any subset of the 30 receive(/broadcast) and/or 30 broadcast subaddresses. The size of the global circular buffer is programmable by means of bits 11, 10, and 9 of Configuration Register #6.

To enable received words for a particular receive(/broadcast) subaddress to be stored to the global circular buffer, it is necessary to program bits 15, 7, 6, and 5 of the respective subaddress control word to logic "1."

If SEPARATE BROADCAST DATA is enabled (bit 0 of Configuration Register #2 = logic "1"), then to enable received words for a particular broadcast subaddress to be stored to the global circular buffer, it is necessary to program bits 15, 2, 1, and 0 of the respective subaddress control word to logic "1."

The pointer to the RT circular buffer is stored in location 101 (if area A is the currently active area, per CURRENT AREA B/$\overline{A}$, bit 13 of Configuration Register #1) or 105 (if area B is the currently active area).

ENHANCED MINI-ACE: SELF-TEST

Q. What are the Enhanced Mini-ACE's self-test capabilities?

A. In Bus Controller and Remote Terminal modes, there is a continuous on-line loopback self-test performed for each message transmitted. In the loopback self-test, the respective (CH. A or CH. B) receiver/decoder samples each word transmitted. For all words transmitted by the Enhanced Mini-ACE (or for that matter, ACE or Mini-ACE) BC or RT, the validity of the "received" version is verified. Also, there is a bit-by-bit comparison check between the transmitted and received versions of the last word transmitted.

If there is a failure of the loopback self-test, the "ERROR FLAG" and "LOOP TEST FAIL" bits will be set in the message's Block Status Word. In addition, if enabled, an interrupt will be issued to the host processor. Also, in RT mode, bit 14 (for Channel B) or bit 13 (for Channel A) will be set in the RT BIT Word Register, and transmitted to the BC in response to a Transmit BIT word mode command. In addition, in RT mode, assuming that bit 2 of Configuration Register #3, RTFAIL/RTFLAG WRAP ENABLE, is programmed to logic "1," the Terminal Flag bit will be set in the status word response to the next non-broadcast message.

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As for the comprehensive protocol self-test and RAM self-test, these may be initiated by a command from the host processor at any time, by writing logic "1" to the respective bit of the Start/Reset Register. The results of these tests are then made available to the host by means of polling and/or interrupts. If the protocol self-test fails, bit 8 (BIT TEST FAIL) of the RT's BIT word and BIT Word Register will be set to logic "1." However, keep in mind that when either the protocol or RAM self-test is being performed, the Enhanced Mini-ACE will be **offline**; that is, not able to receive or transmit on the 1553 bus.

Q. Are the Enhanced Mini-ACE internal registers corrupted as a result of running the self-test vectors?

A. No. When the self-test is performed, the first part of the test stores the value of the registers temporarily into memory. When the test is complete, the register values are restored. As long as the host does not attempt a write operation before the test is complete, the final values in the registers will be the same as the initial values.

Note that the Time Tag Register **will** continue to increment at the same rate as prior to the start of the test (i.e., no time is lost). Also, the protocol self-test cannot be performed if the BC or Monitor is presently enabled (started), or the RT is not idle, or the memory test is currently in progress. The BC frame timer and message timers will be restored to zero, but this should not matter since these will be reinitialized when the BC is enabled.

Also, if the protocol self-test fails and assuming that RTFAIL-TO-TERMINAL FLAG AUTO-WRAP is enabled, the Terminal flag status bit will be set to logic "1" and the results of the RT's last loopback test will be lost. The command stack register, data address pointer register, and the Subaddress Control Word Register will be reset to zero. In addition, the interrupt output will be cleared; it will be re-asserted only if the BIT test complete interrupt was enabled.

Q. For the Enhanced Mini-ACE built-in self-test, if the flag supplying the results of the comprehensive protocol self-test and RAM self-test is faulted in the "PASS" state, how is that detected?

A. While the Enhanced Mini-ACE's protocol or RAM self-test is being performed, the host **may** access the BIT Test Status Register (register address 1Ch). However, the host may **not** access any of the other registers; if it does, the self-test will be aborted.

While the test is being performed, the "PROTOCOL SELF-TEST PASSED" bit (bit 12) and "RAM BUILT-IN SELF-TEST PASSED" bit (bit 5) will normally be logic "0." If you poll this register while the self-test is being performed and the "PASSED" bit for the test that's being performed returns a value of logic "1," this indicates that the bit is stuck high.

Also, after the self-test completes, you may poll the final value of the self-test ROM address register and self-test data register. These are both test registers, which are made accessible by setting 64-WORD REGISTER SPACE, bit 2 of Configuration Register #6, to a value of logic "1."

Assuming that the test has run to successful completion, the expected values of these two registers are known. If one of the "PASSED" bits is logic "1," but the value of either of these registers doesn't match the expected value, this would indicate a fault in the self-test logic.

Q. How is the Enhanced Mini-ACE's self-test initiated?

A. For Enhanced Mini-ACE, the protocol and RAM self-tests may be initiated by means of the Start/Reset Register (write only, register address 03). In particular, to initiate the RAM self-test, you would write a value of logic "1" to bit 9 of this register. To initiate the protocol self-test, you would write a value of logic "1" to bit 7.

Q. What exactly is done in the Enhanced Mini-ACE RAM self-test?

A. The RAM test works as follows: a pattern of 0, 1, 2, 3,... is written to addresses 0, 1, 2, 3..., (data = address) and then read back and verified. After that, the inverse pattern ("data = address inverted") pattern is written, read back, and verified.

Q. How long does the Enhanced Mini-ACE's RAM self-test take to perform?

A. The memory test takes a total of 10 clock cycles per RAM location. That is, for each word location, it takes 5 clocks to write and read/verify the "data = address" pattern, and another 5 clocks to write and read/verify the "data = inverted address" pattern.

Therefore, for an Enhanced Mini-ACE hybrid with 4K RAM locations, it takes a total of 40,960 clock cycles to perform the memory self-test. For a clock frequency of 16 MHz, this is 2.56 ms. For a hybrid with 64K RAM locations, it takes a total of 655,360 clock cycles to run the memory self-test. For a clock frequency of 16 MHz, this is 40.96 ms.

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PCI ENHANCED MINI-ACE

Q. Is the BU-62865 PCI Enhanced Mini-ACE PCI 3.3 or 5.0 Volt compliant?

A. It is **5 volt** powered, and intended for use in a 5 volt PCI signaling environment.

Q. Is a self-test performed on the PCI Enhanced Mini-ACE in the same manner as for the Enhanced Mini-Ace?

A. No. However, you will still be able to run essentially the same self-test for the "1553" portion of the terminal that is performed on the BU-61865 (Enhanced Mini-ACE). Note however that the stimulus/response vectors will need to be written and read/verified by the PCI host; that is, the vectors will **not** be included in on-chip ROM.

Q. Does the PCI Enhanced Mini-ACE include RAM parity checking?

A. Yes. The BU-62865 BC/RT/MT, the 64K RAM version of the PCI Enhanced Mini-ACE, **does** incorporate RAM parity checking.

RAD HARD/SPACE COMPONENTS

SP'ACE

Q. What are the BU-61582's (SP'ACE's) radiation characteristics?

A. Total Dose:
1 Mrad
Single Event Upset:
10^{-7} errors per bit-day (LET threshold of 59 Mev/mg/cm^2)
Single Event Latchup:
Immune
Dose Rate:
10^{10} rads(Si)/sec
Neutron Fluence:
$2 \cdot 10^{13}$ neutrons/cm^2

Q. What is the ESD rating of the BU-61582 SP'ACE?

A. The ESD rating of the BU-61582's digital I/O signals is Class 1. That is, it is between 0 and 1500 volts. The MIL-STD-1553 analog transceiver signals (TX/RX-A, $\overline{\text{TX/RX-A}}$, TX/RX-B, and $\overline{\text{TX/RX-B}}$) provide an ESD immunity level of 7,000 volts with no protection. This value may be increased by means of external circuitry, involving the use of full-wave diode bridges, and either Zener diodes or transorbs.

Q. Does the SP'ACE support a software-programmable RT address?

A. There are two different versions of the SP'ACE:

(1) The BU-61582XX, for which the RT address is hardwired; and ...

(2) The BU-61583XX, for which the RT address may be programmed by means of software control. To make the BU-61583's RT address software programmable, you would need to connect RTAD4-RTAD0 to D5-D1, and RTADP to D0.

Q. For SP'ACE, what are the advantages of a shared RAM interface over the use of dual Port RAM?

A. (1) Dual port RAM is significantly more expensive than conventional single-port RAM. It also uses up more real estate than using the shared RAM that's inside the SP'ACE.

(2) If dual port RAM is used, the design will still need external tri-state buffers for the address and data buses, to isolate the SP'ACE buses from the buses connecting to the host processor. These are necessary to enable the host to access the SP'ACE's internal registers. This entails additional real estate and cost.

(3) In terms of software, there are no differences between the use of internal shared RAM and external dual port RAM.

(4) The penalty in terms of bus bandwidth utilization for using shared, rather than dual port, RAM is **very** insignificant. It's a function of the level of bus traffic, but even assuming 1,000 32-word messages per second, and assuming the use of 8-bit RAM in a SP'ACE, a host bus contention situation will only occur about 2.0 to 2.5% of the time.

(5) There is no difference, in terms of worst-case holdoff time between the use of dual port RAM and shared RAM. The reason is that even with external dual port RAM, there will still be a need to access the SP'ACE's registers (through the tri-state buffers). For a dual port RAM interface, the SP'ACE's host interface will need to be configured for its transparent mode. This results in a one clock cycle **increase** over the buffered (shared RAM) configuration in the time required to access the SP'ACE's internal registers.

Q. Does the SP'ACE include a mechanism to ensure against the possibility of a "babbling terminal?"

A. In compliance with MIL-STD-1553B, the SP'ACE and all of our other 1553 products include a transmitter timeout circuit. That is, they include a circuit

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that operates independently from the encoder/transmitter to automatically shut down the transmitter if it attempts to transmit longer than the longest allowable transmission time of 660 µs. For the SP'ACE, the timeout value is 668 µs. If the transmitter timer (sometimes called a watchdog timer) times out, it will: (1) shut down the Manchester encoder circuit; and (2) bring the TX_INH (transmit inhibit) inputs to the CH. A or CH. B transmitter to logic "1," which shuts down the 1553 transmitter.

Q. We have an application for the BU-61582 SP'ACE, involving both RT and Monitor modes. When the SP'ACE is in Monitor mode, we need very high assurance that the SP'ACE will never attempt to transmit on the 1553 bus. What do you suggest?

A. The recommended configuration is for us to supply you with a version of the BU-61582 SP'ACE product that is modified to bring out the TX_INH (Transmit Inhibit) signals. The SP'ACE's mode (BC, RT, Monitor, or simultaneous RT/Monitor) is selectable, by host software, by means of Configuration Register #1. Keep in mind that the SP'ACE is designed to never transmit while in Monitor mode. To provide an extra level of assurance that the SP'ACE will never transmit on the bus while in Monitor mode, I would recommend bringing out the TX_INH signals. This way, the SP'ACE monitor is prevented from transmitting by two independent methods: (1) under non-fault conditions, the SP'ACE's Monitor mode will never attempt to transmit on the 1553 bus; and (2) if there was a fault in which the monitor did attempt to transmit on the 1553 bus, the assertion of the respective TX_INH input to logic "1" by external hardware will serve to block any transmission on the 1553 bus.

BU-65621

Q. Is there a Standard Military (DESC) drawing for the BU-65621 JRAD chip?

A. Yes. The number is 5962-94A03. In addition, there is also an Altered Item Drawing (AID) from Honeywell SSEC, who is the foundry for the BU-65621 chip. Honeywell's number for the AID is 22019712.

Q. Does the BU-65621 include any internal memory?

A. The BU-65621 chip does not include any on-chip memory. However, we can supply a transceiverless version of the BU-61582 SP'ACE, the BU-61582X0. The BU-61582X0 hybrid includes the JRAD protocol chip that's in the BU-65621, plus 16K X 16 of internal RAM, but no transceiver.

Q. Can the BU-65621 operate as a BC, RT or MT?

A. In addition to self-test mode, the BU-65621 has five (5) normal modes of operation:

1. Bus Controller (BC)
2. Remote Terminal (RT)
3. Word Monitor
4. Selective Message Monitor
5. Simultaneous RT and Selective Message Monitor

Q. We plan on using Honeywell's 32Kx8 memory chip in conjunction with the BU-65621. We are trying to decide whether to use one or two memory chips for the BU-65621's external, buffered RAM interface. How does the memory width effect the data throughput of the 1553 controller?

A. Honeywell's 32K X 8 RAM **will** work. We integrate this chip into our SP'ACE hybrid, which also includes the same "JRAD" chip that's in the BU-65621. The use of 8-bit RAM should not have any appreciable effect on throughput.

However, you should be aware that the time for your host processor to access the buffered RAM (through the BU-65621) increases by roughly a factor of two (with respect to using 16-bit wide RAM), due to the increased time to transfer data to/from the 8-bit RAM. That is, assuming a 16 MHz clock input, there will be an increase from 312 ns max to 562 ns max for an uncontended access, and an increase from about 3.0 µs to about 6.0 µs for a contended access.

If you're considering the use of the BU-65621 with the Honeywell RAM chip, note that the BU-61582X0 transceiverless SP'ACE integrates these two chips into a single 1.0 by 1.9 inch hybrid.

RT COMPONENTS

Q. What are the differences between BUS-65112 and BUS-65142?

A. (1) BUS-65112 uses a 12 MHZ clock, while BUS-65142 uses a 16 MHZ clock.

(2) For a Transmit (RT-to-BC transfer) message: for BUS-65112, R/$\overline{W}$ is low, except that it pulses high during the transfer cycle period defined by $\overline{DTREQ}$ being high. For BUS-65142, R/$\overline{W}$ is low for the

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command word transfer, then goes high and stays high (it doesn't pulse).

(3) The maximum $\overline{\text{DTREQ}}$-to-$\overline{\text{DTGRT}}$ time is 1.5 µs for BUS-65112, and 2.1 µs for BUS-65142.

Q. What are the BUS-65143's power consumption and dissipation?

A. For BUS-65143 (+5V/-12V power), the maximum current drain is:

For +5V: 115 mA max

For -12V: At idle (non-transmitting): 70 mA max; at 50% transmit duty cycle: 185mA max; at 100% transmit duty cycle: 305 mA max.

For the BUS-65143 power dissipation, assuming a total external dissipation of 1.4 watts {in the isolation transformer (140 mW), coupling transformer (80 mW), isolation resistors (450 mW each) and termination resistors (150 mW each)} when transmitting:

At idle: 1.415 watts max

At 50% duty cycle: 2.125 watts max

Q. Is there a recommended way of decoupling for the BU-61705 Simple System RT? Any particular values and number of capacitors should be used?

A. We recommend a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor for each of the two transceivers [VCC-CH. A(B)] pins (72 and 20), and a 0.1 µF ceramic capacitor on Vcc-LOGIC, pin 37.

POWER AND THERMAL QUESTIONS

Q. What is meant by "hottest die" power dissipation?

A. "Hottest die power dissipation" refers to the active transceiver chip. That is, at any given time, the hottest die will be for the transceiver for the "active" (transmitting) bus channel; i.e., either Channel A or Channel B.

Q. What equation should I use for performing a thermal calculation for the Mini-ACE Plus? What is the Θ_{JC} for the hybrid?

A. The junction-to-case thermal resistance (Θ_{JC}) for Mini-ACE (Plus) is 6.8 degrees C per watt.

That is, $T_J = T_C + (6.8 \bullet P_{DISS})$, where T_J = hottest die junction temperature, T_C = hybrid case temperature, and P_{DISS} = hottest die dissipation.

Q. The Mini-ACE power ratings are given for transmitter duty cycles of 25%, 50%, 100%, and Idle. What does this mean?

A. This refers to the percentage of time that the bus controller is actually **transmitting** on the 1553 bus; that is, not transmitting or receiving, just transmitting. For example, if the BC sends a message with a command word + 32 data words to each of 10 RTs once per second, the duty cycle would be:

10•[(1 + 33)•(20 µs)]/1 sec = 0.66%

Q. If the BC is polling each of 10 RTs once per second, can I use the 25% duty cycle?

A. Referring to the calculation above, you can **almost** use the "idle" duty cycle. Whatever your actual duty cycle is, you can calculate the power usage and dissipation; it's a linear interpolation.

Q. Do the power ratings given apply to a dual bus?

A. Yes. MIL-STD-1553 operates as a "standby redundant" bus. That is, the BC usually sends most of its messages on the "primary" bus (typically Bus A). The BC will only switch over to the secondary bus (typically Bus B) if it detects a failure on the primary bus, or if there is a failure of one (or more) RTs on the primary bus.

Clause 4.6.3.1 of MIL-STD-1553B states that "Only one data bus shall be active at a given time …" On most 1553 terminals, it is **not** possible to transmit on both 1553 buses simultaneously.

Q. I have a BUS-63125 transceiver on a board that doesn't get -15 V in production board test. If I ground the -15 V input to the board during test instead of -15 V, will this damage the BUS-63125?

A. Grounding the -15V input to the BUS-63125 transceiver will **not** damage the BUS-63125. Of course, the BUS-63125 won't be able to transmit or receive in this condition.

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TRANSFORMERS

TRANSFORMERS: BOARD LAYOUT

Q. Other than the rules concerning no planes above or below the transformers, as well as the 1553 analog signals going to and from them, what other considerations are there regarding the placement of 1553 transformers?

A. It is advantageous for the 1553 transformers to be located as close as possible to the connector(s) where the 1553 signals leave the board.

It is desirable that the connections from the transformer primaries (Mini-ACE side) center taps to your 5V RETURN (presumably the ground plane) to be as thick as possible, since these will be conducting large currents when transmitting, on the order of 500 to 600 mA. The traces from the Mini-ACE Tx/Rx-A(B) pins to the transformer will need to conduct the same current, but at 50% duty cycle when transmitting. The traces from the transformer secondary to the 1553 stub will conduct up to about 100 to 150 mA.

TRANSFORMERS: ESD

Q. What is the effect of the BUS-29854 isolation transformer on a 1553 terminal's ESD immunity?

A. The transformer **improves** the ESD immunity of the overall 1553 terminal. By definition, a 1553 BC or RT terminal consists of both the analog/digital circuitry (e.g., the BU-61582X2) **and** the isolation transformers.

A MIL-STD-1553 coupling transformer is required to exhibit a minimum common-mode rejection ratio of 45 dB at 1 MHz. Since the isolation transformers that comprise part of the 1553 terminals are similarly constructed (in some cases, they're the same transformer), they will generally have the same common-mode rejection characteristics.

Assuming that the ESD disturbance is applied between one of the 1553 stub (or bus) conductors and ground (which is generally the case), the transformers' common-mode rejection will, in effect, increase the ESD immunity of the overall terminal.

TRANSFORMERS: BTTC PART NUMBERS

Q. The Mini-ACE data sheet mentions transformers B-3226 (through-hole) and B-3227 (SMT) on sheet 4. We've been using the double-stacked TST-9007. Are all of these correct? Are there any new, smaller, shorter or perhaps surface-mount transformers?

A. For Mini-Ace and Enhanced Mini-ACE, all of the transformers that you list have the correct turns ratios of 1:2.5 direct coupled, or 1:1.79 transformer (stub) coupled. The B-3226 is a single through-hole transformer, 0.625 X 0.625, with a max height of 0.250". B-3227 is also a 0.625 X 0.625 single surface mount transformer, but with a max height of 0.275". TST-9007 is a dual transformer, 0.625 X 0.625, max height of 0.280".

Beta Transformer Technology Corporation (BTTC), a subsidiary of DDC, manufactures transformers in a variety of mechanical configurations with the required turns ratio. The table on page 24 provides a listing of many of these. Note that for the BU-6XXXXX**4** versions of the Enhanced Mini-ACE, which includes McAir compatible transceivers, **only** the B-3818 or B-3819 transformers may be used.

For the BU-6XXXXX**3** versions, **any** of the transformers listed in the table may be used.

For additional information, contact BTTC at (631) 244-7393 or www.bttc-beta.com.

CONNECTORS, CABLES, AND BREADBOARDING SOCKETS

Q. What is the mating connector(s) and cable for DDC's 1553 board products?

A. The mating connector is Trompeter part number PL75-47. Trompeter, a supplier of both connectors and cables for 1553, may be reached at (818) 707-2020. One type of cable that we have used is M17-176-00002.

Q. Is there a breadboarding socket for the Mini-ACE and Enhanced Mini-ACE 72-lead flatpack package?

A. Yes. There is a socket available from Azimuth Electronics. The part number is 6224-53-21X. Note that this socket is only applicable for the flatpack (BU-6XXXXFX) package only; it is not applicable for the formed gull lead package (BU-6XXXXGX). The contact information for Azimuth Electronics is as follows:

2650 El Camino Real
San Clemente, CA, 92672
TEL: (949) 492-6481
FAX: (949) 492-0744

web: http://www.azimuth-electronics.com

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BTTC TRANSFORMERS FOR USE WITH MINI-ACE (PLUS) AND ENHANCED MINI-ACE	
TRANSFORMER CONFIGURATION	**BTTC Part Number**
Single epoxy transformer, through-hole, 0.625" X 0.625", 0.250" max height	B-3226
Single epoxy transformer, through-hole, 0.625" X 0.625", 0.220" max height. May be used with BU-6XXXXX4 (McAir) version of Enhanced Mini-ACE.	B-3818
Single epoxy transformer, flat pack, 0.625" X 0.625", 0.275" max height	B-3231
Single epoxy transformer, surface mount, 0.625" X 0.625", 0.275" max height	B-3227
Single epoxy transformer, surface mount, hi-temp solder, 0.625" X 0.625", 0.220" max height. May be used with BU-6XXXXX4 (McAir) version of Enhanced Mini-ACE	B-3819
Single epoxy transformer, flat pack, 0.625" X 0.625", 0.150" max height	LPB-5014
Single epoxy transformer, surface mount, 0.625" X 0.625", 0.150" max height	LPB-5015
Dual epoxy transformer, twin stacked, 0.625" X 0.625", 0.280" max height	TST-9007
Dual epoxy transformer, twin stacked, surface mount, 0.625" X 0.625", 0.280" max height	TST-9017
Dual epoxy transformer, twin stacked, flat pack, 0.625" X 0.625", 0.280" max height	TST-9027
Dual epoxy transformer, side by side, through-hole, 0.930" X 0.630", 0.155 max height	TLP-1205
Dual epoxy transformer, side by side, flat pack, 0.930" X 0.630", 0.155 max height	TLP-1105
Dual epoxy transformer, side by side, surface mount, 0.930" X 0.630", 0.155 max height	TLP-1005
Single metal transformer, flat pack, 0.630" X 0.630", 0.175" max height	HLP-6014
Single metal transformer, surface mount, 0.630" X 0.630", 0.175" max height	HLP-6015

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