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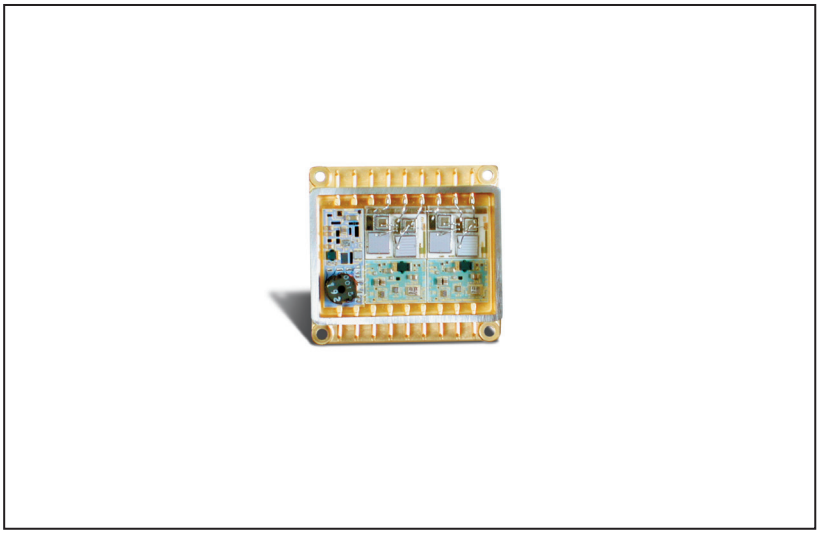
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PWR-82340 and PWR-82342

SMART POWER H-BRIDGE MOTOR DRIVES



DESCRIPTION

The PWR-82340 and PWR-82342 are 30 A H-bridge motor drive hybrids. The PWR-82340 has a 200 V rating and uses MOSFETs in the output stage while the PWR-82342 has a 500 V rating and an IGBT output stage. Both types have individual fast recovery diodes internally connected across the output drive transistors to clamp inductive flyback. This new series of Smart Power Motor Drives has CMOS Schmitt Trigger inputs for high noise immunity. High- and low-side input logic signals are XOR'd in each phase to prevent simultaneous turn-on of in-line transistors, thus eliminating a shoot-thru condition. The internal logic controls the high- and low-side gate drives for each phase and can operate from +5 to +15 V logic levels. The internal power supply provides a constant voltage source to the floating high side gate drives. This provides constant output performance for switching frequencies from DC to 50 kHz.

APPLICATIONS

Packaged in small cases, these hybrids are an excellent choice for high performance, high reliability motor drives for military and aerospace servo-amps and speed controls. Among the many applications are robotics; electromechanical valve assemblies; actuator systems for flight control surfaces on military and commercial aircraft; antenna and radar positioning; fan and blower motors for environmental conditioning; thrust and vector position control of mini subs, drones, and RPV's; compressor motors for cryogenic coolers; and high-power inverters. The PWR-82340/342 hybrids are ideal for harsh military environments where shock, vibration, and temperature extremes are evident, such as missile applications where fin actuator systems control missile direction. The PWR-82340 and PWR-82342 operate over the -55°C to +125°C temperature range and are available with military processing.

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- Military Processing Available

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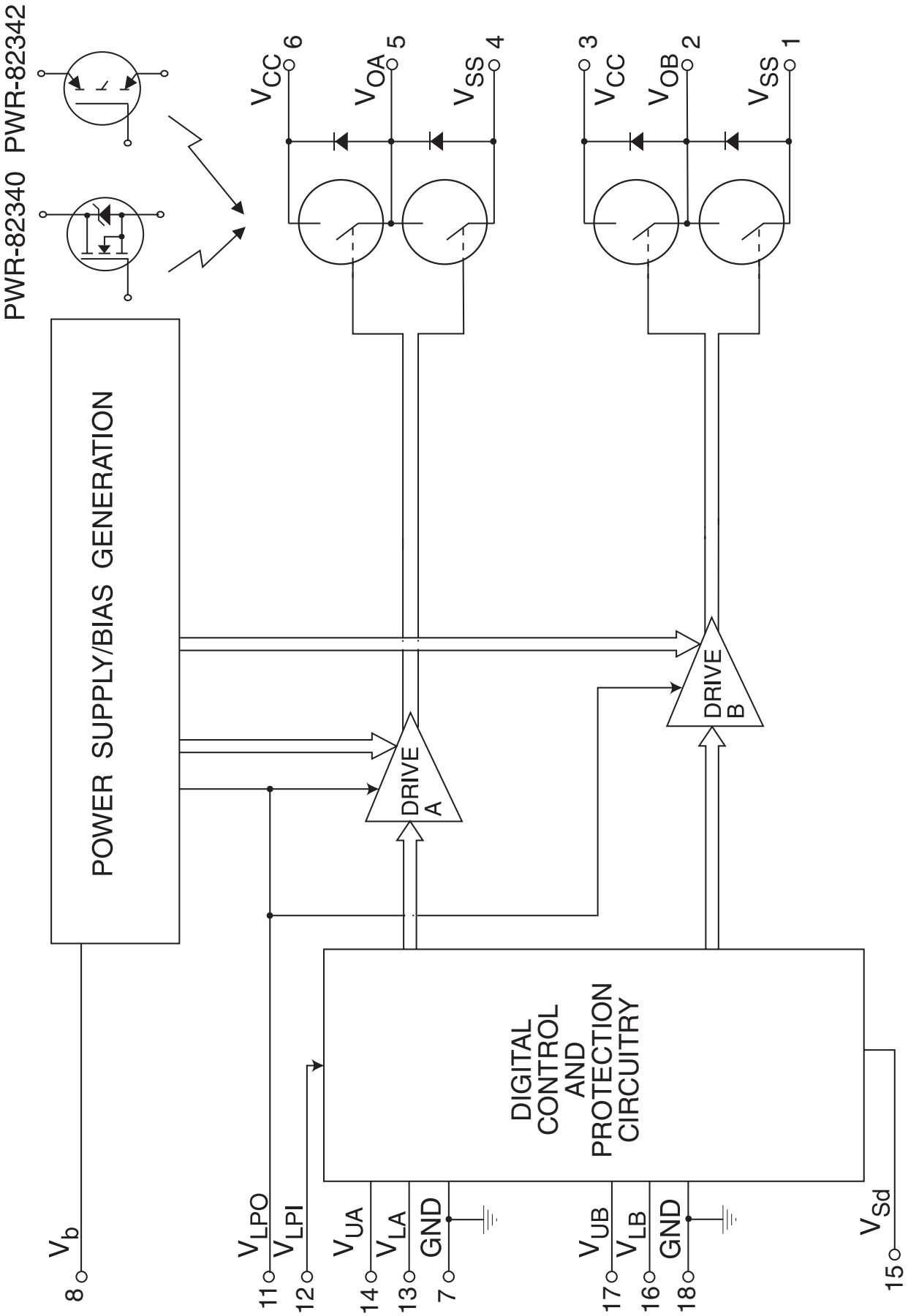


FIGURE 1. PWR-82340/342 BLOCK DIAGRAM

TABLE 1. PWR-82340 AND PWR-82342 ABSOLUTE MAXIMUM RATINGS (TC = +25°C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	PWR-82340 VALUE	PWR-82342 VALUE	UNITS
SUPPLY VOLTAGE	V_{CC}	200	500	V
BIAS VOLTAGE	V_b	50	50	V
LOGIC POWER-IN VOLTAGE	V_{LPI}	18	18	V
INPUT LOGIC VOLTAGE	V_U V_L V_{Sd}	V_{LPI} + 0.5	V_{LPI} + 0.5	V
OUTPUT CURRENT **CONTINUOUS** **PULSED**	I_o I_{op}	30 50	30 50	A A
OPERATING FREQUENCY	f_O	50	25	kHz
CASE OPERATING TEMPERATURE	T_C	-55 to +125	-55 to +125	°C
CASE STORAGE TEMPERATURE	T_{CS}	-55 to +150	-55 to +150	°C

TABLE 2. PWR-82340 AND PWR-82342 SPECIFICATIONS TC = +25°C UNLESS OTHERWISE SPECIFIED)

			PWR-82340			PWR-82342			
PARAMETERS	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
OUTPUT									
Output Current Continuous (see FIGURES 19 and 15)	I_O				30			30	A
Supply Voltage	V_{cc}	see note 1		140	200		270	500	V
Output On Resistance (each FET)(see FIGURE 14A)	R_{on}	I_o = 30 A			0.1				ohm
Output Voltage Drop (each IGBT)(see FIGURES 14B)	$V_{CE(SAT)}$	I_o = 30 A						3.8	V
Instant Forward Voltage (flyback diode)(see FIGURE 13)	V_F	I_p = 30 A (see note 2)			1.15			1.70	V
Reverse Recovery Time (flyback diode)	t_{rr}	I_f = 1 A, I_r = 1 A			50			50	nsec
Reverse Leakage Current at T_C = +25°C	I_r	see note 3			10			10	µA
Reverse Leakage Current at T_C = +125°C	I_r	see note 3			1			1	mA
BIAS SUPPLY									
Input Bias Voltage (T_C = -55 to +125°C)	V_b		14		45	15		45	V
Quiescent Bias Current (see note 4)(see FIGURE 16)	I_{bq}	V = 28 V		27	40		27		mA
Bias Current (T_C = -55 to +125°C)	I_b	V_b = 28 V(see note 5)	30			24		35	mA
(see FIGURES 17 and 18)					1.4				
Inrush Current (T_C = -55 to +125°C)	I_{ir}	V_b = 28 V			2			1.4	A
Logic Power Input Current	I_{LPI}	see note 6						2	mA
INPUT SIGNALS (SEE FIG. 7)		**Pin Connections**							
Positive Trigger Threshold Voltage	V_P	Pin 11 and 12	9		12.9	9		12.9	V
Negative Trigger Threshold Voltage	V_N	connected	2.1		6	2.1		6	V
Hysteresis Voltage	V_H	Pin 11 and 12	3		10.8	3		10.8	V
Positive Trigger Threshold Voltage	V_P	connected	3		4.3	3		4.3	V
Negative Trigger Threshold Voltage	V_N	see note 6	0.7		3	0.7		3	V
Hysteresis Voltage	V_H	see note 6	1		3.6	1		3.6	V
SWITCHING CHARACTERISTICS (see FIGURE 2)		**Test 1 Conditions**							
Upper Drive:		Pin 11 and 12							
Turn-on propagation delay	$t_{d\ (on)}$	connected			840			810	nsec
Turn-off propagation delay	$t_{d\ (off)}$	+15 V logic			1020			860	nsec
Shut down propagation delay	t_{Sd}	I_O = 30 A peak			800			810	nsec
Turn-on rise time	t_r	PWR-82340			125			100	nsec
Turn-off fall time	t_f	V_{CC} = 140 V			125			150	nsec
Lower Drive:		PWR-82342							
Turn-on propagation delay	$t_{d\ (on)}$	V_{CC} = 270 V			850			800	nsec
Turn-off propagation delay	$t_{d\ (off)}$				1000			870	nsec
Shut down propagation delay (see FIGURE 9)	t_{Sd}				800			770	nsec
Turn-on rise time	t_r				125			100	nsec
Turn-off fall time	t_f				125			150	nsec

TABLE 2. PWR-82340 AND PWR-82342 SPECIFICATIONS (CONTINUED)
TC = +25°C UNLESS OTHERWISE SPECIFIED)

			PWR-82340			PWR-82342			
PARAMETERS	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
SWITCHING CHARACTERISTICS (see FIGURE 2) **Upper Drive:**		**Test 2 Conditions** see note 6							
Turn-on propagation delay	$t_{d\ (on)}$	+5 V logic			1090			1050	nsec
Turn-off propagation delay	$t_{d\ (off)}$	I_O = 30 A peak			1315			1150	nsec
Shut down propagation delay	t_{Sd}	PWR-82340			1100			850	nsec
Turn-on rise time	t_r	V_{CC} = 140 V			125			100	nsec
Turn-off fall time	t_f	PWR-82342			125			150	nsec
		V_{CC} = 270 V							
SWITCHING CHARACTERISTICS **LowerDrive:**		**Test 2 Conditions**							
Turn-on propagation delay	$t_{d(on)}$	see note 6			1125			1050	nsec
Turn-off propagation delay	$t_{d(off)}$	+5V logic			1290			1150	nsec
Shut-down propagation delay (see FIGURE 9)	t_{Sd}	I_O = 30 A peak			1100			850	nsec
Turn-on Rise Time	t_r	PWR-82340			125			100	nsec
Turn-off Fall Time	t_f	V_{CC} =140 V			125			150	nsec
		PWR-82342							
		V_{CC} = 270 V							
DEAD TIME	t_{dt}		1000						nsec
MINIMUM PULSE WIDTH	t_{pw}		150			175			nsec
THERMAL									
Maximum Thermal Resistance	θ_{j-c}	each transistor			0.85			0.85	°C/W
Maximum Lead Soldering Temp.	T_S	see note 7			250			250	°C
Junction Temperature Range	T_j		-55		150	-55		150	°C
Case Operating Temperature	T_{CO}		-55		125	-55		125	°C
Case Storage Temperature	T_{CS}		-55		150	-55		150	°C
WEIGHT					3.88 (110)			3.88 (110)	oz (g)

Notes:
1. For Hi-Rel applications, derating per MIL-S-19500 should be observed. (Derate V_{cc} to 70%.)
2. Pulse width ≤ 300 µs, duty cycle ≤ 2%.
3. For PWR-82340 V_{CC} = 140 V, V_U, V_L = logic '0' and for PWR-82342 V_{CC} = 350 V, V_U, V_L = logic '0.'
4. V_U, V_L = logic '0' on pins 13 to 17.
5. For PWR-82340 f_O = 30 kHz and for PWR-82342 f_O = 10 kHz.
6. Pin 12 connected to external +5 V supply.
7. Solder 1/8" from case for 5 seconds maximum.

INTRODUCTION

The PWR-82340 and PWR-82342 are 30 A motor drive hybrids rated at 200 V and 500 V respectively. The PWR-82340 uses a MOSFET output stage and the PWR-82342 has an IGBT output stage for high speed, high current, and high efficiency operation. The PWR-82342 also offers high voltage performance of an IGBT for use in 270 V systems. These motor drives are ideal for use in high performance motion control systems, servo amplifiers, and motor speed control designs. Furthermore, Multiaxis systems requiring multiple drive stages can benefit from the small size of these power drives.

The PWR-82340/342 can be driven directly from a PWM, DSP, or a custom ASIC that supplies digital signals to control the upper and lower transistors of each phase. These highly integrated drive stages have Schmitt trigger digital inputs that control the high and low side of each phase. Digital protection of each phase eliminates an in-line firing condition by preventing simultaneous turn-on of both the upper and lower transistors. The logic controls the high- and low-side gate drivers.

Operation from +5 to +15 V logic levels can be programmed by applying the appropriate voltage to pin 12 (V_{LPI}). The PWR-82340/342 has a ground referenced low-side gate drive.

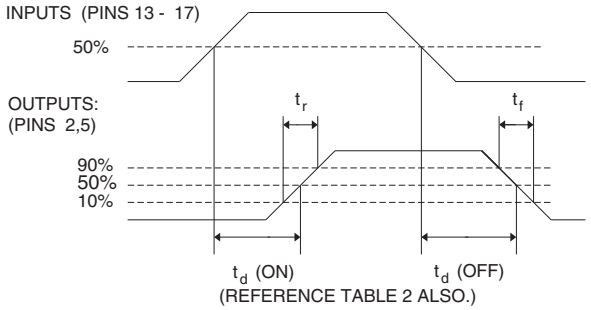


FIGURE 2. INPUT/OUTPUT TIMING RELATIONSHIPS

An internal DC-DC converter supplies a floating output to each of the two high-side drives. This provides a continuous high-side gate drive even during a motor stall. Pin 11 (VLPO) supplies a +15 V output, which can be used to power the internal logic when system usage requires +15 V logic. The high- and low-side gate drivers control the N-channel MOSFET or IGBT output stage. The MOSFETs used in the PWR-82340 allow output switching up to 50 kHz, while the high-speed IGBTs in the PWR-82342 can switch at 25 kHz. A flyback diode parallels each output transistor and controls the regenerative energy produced by the motor. These fast recovery diodes have faster reverse switching times than the intrinsic body diode of the MOSFETs used in the PWR-82340. They also protect the IGBTs used in the PWR-82342 from exceeding their Emitter-to-Collector breakdown voltage. Use of a copper case and solder attachment of the output transistors achieves a low thermal resistance of 0.85°C/W maximum. Care should be taken to adequately heatsink these motor drives to maintain a case temperature of +125°C. Junction temperatures should not exceed +150°C. The PWR-82340/342 does not have internal short circuit or overcurrent protection which, if required, must be added externally to the hybrid.

BIAS VOLTAGES

The PWR-82340 and PWR-82342 motor drive hybrids require a power supply (Vb) for operation. Based on the Vb, the hybrid generates two independent, floating supplies internally, which eliminates the need for external bias voltages for each phase. In order for the internal power supply to generate these voltages, the input bias voltage (Vb) must be between +15 to +45 Vdc and configured as shown in FIGURE 3A.

If the bus voltage (Vcc) is between 15 ≤ V ≤ 45V that may be used for the power supply as well by using the configuration shown in FIGURE 3B. In most avionic systems this can be accomplished by connecting the Vb pin to the MIL-STD-704D, +28 Volt bus.

In any case, a 0.01 µf decoupling capacitor (Cb) must be connected between Vb (pin 8) and GND.

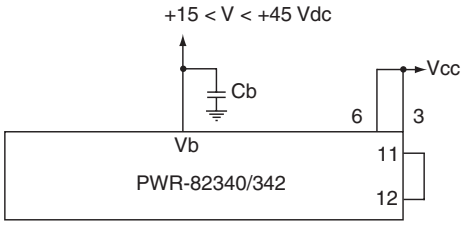


FIG. 3A

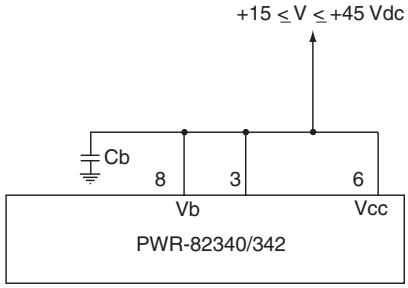


FIG. 3B

FIGURE 3. CONNECTION TO BUS VOLTAGE TO DEVELOP PROPER INPUT BIAS VOLTAGE

DIGITALLY CONTROLLED INPUTS

The PWR-82340 and PWR-82342 use Schmitt triggered digital inputs (with hysteresis) to ensure high noise immunity. The trigger switches at different points for positive and negative going signals. Hysteresis voltage (VH) is the difference between the positive going voltage (VP) and the negative going voltage (VN) (see FIGURE 4). The digital inputs have programmable logic levels, which allows the hybrid to be used with different types of control logic with an input voltage range of +5 to +15 V, such as TTL or CMOS logic. The PWR-82340 and PWR-82342 internal power supply generates a +15 Vdc (VLPO) on pin 11. This output can only be used to power the internal digital circuitry within the hybrid. **Do not use this +15 V output to power any circuitry external to the hybrid**. Pin 12 is the logic power input (VLPI) for the digital circuitry inside the hybrid. **A 0.01 uF, 50 V ceramic capacitor must be placed between this pin (12) and GND as close to the hybrid as possible**. When using 15 V control circuitry, the logic power input (pin 12) can be connected directly to the logic power output (pin 11) of the hybrid. There is no need for an additional external power supply. **When using 5 V control logic, an external +5 VDC supply must be connected between pin 12 of the hybrid, and GND — leave Pin 11 open (N/C)**. The control circuitry can be as simple as a PWM, or as sophisticated as a microprocessor or custom ASIC, depending on the system requirements. The Block Diagram in FIGURE 5 shows a typical interface of the PWR-82340 and PWR-82342 with a motor and control logic in a Servo-Amp System.

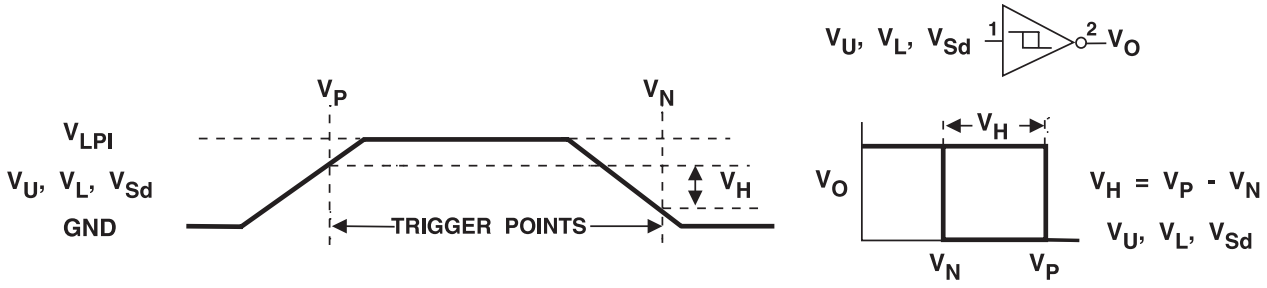


FIGURE 4. HYSTERESIS DEFINITION AND CHARACTERISTICS

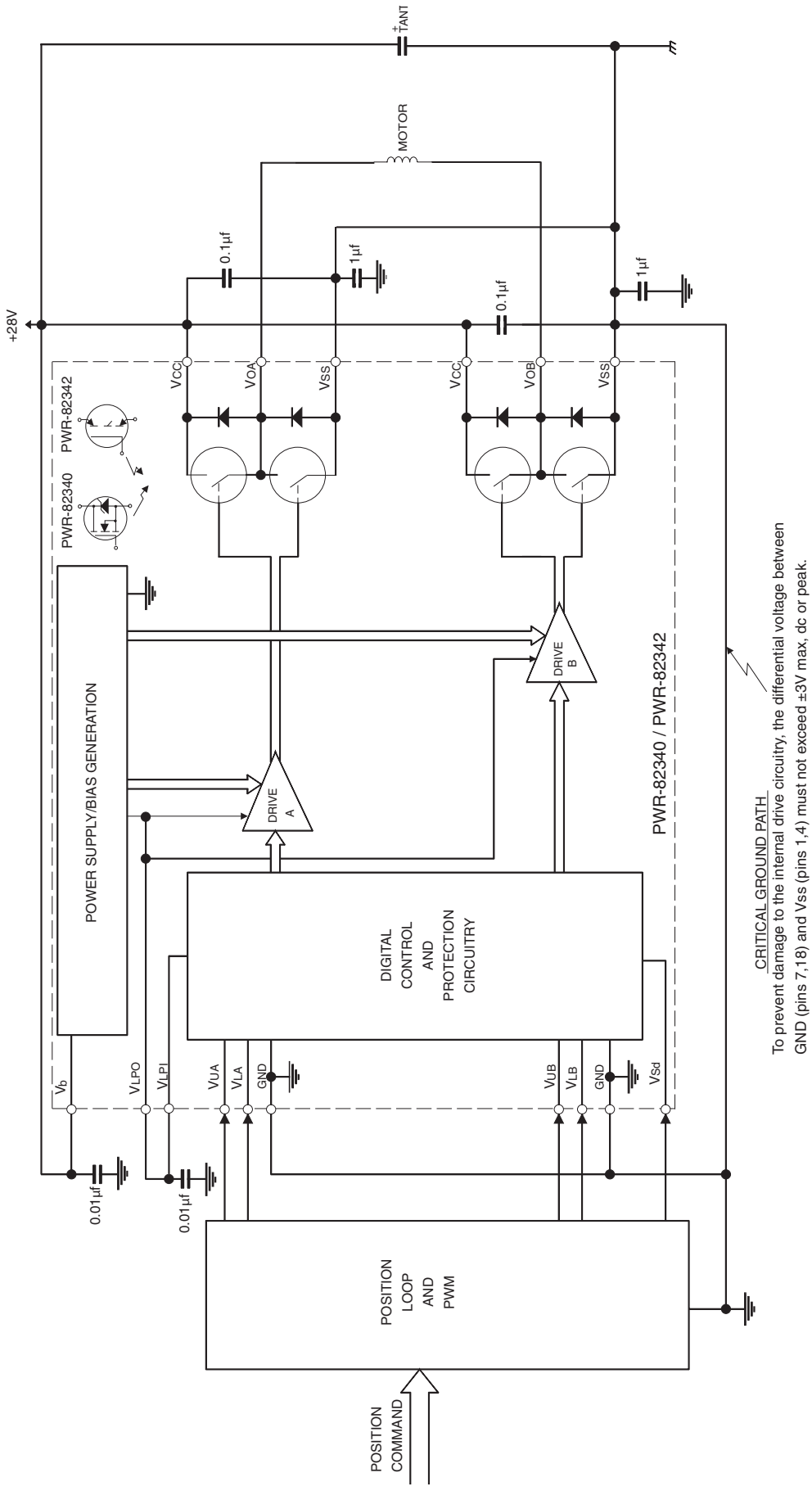


FIGURE 5. PWR-82340/342 TYPICAL INTERFACE WITH A MOTOR AND PWM

SHUT-DOWN INPUT (VSD)

Pin 15 (VSd) provides a digital shut-down input, which allows the user to completely turn off both the upper and lower output transistors in both phases. Application of a logic '1' to the VSd input will latch the Digital Control/Protection circuitry thereby turning off all output transistors. The Digital Control/Protection circuitry remains latched in the off state and will not respond to signals on the VL or VU inputs while the VSd has a logic '1' applied. When the user or the sense circuitry (as in FIGURE 7) returns the VSd input to a logic '0,' and then the user sets the VL and VU inputs to a logic '0' the output of the Digital Control/ Protection circuitry will clear the internal latch. When the next rising edge (see FIGURE 6) occurs on the VL or VU digital inputs, the output transistors will respond to the corresponding digital input. This feature can be used with external current limit or temperature sense circuitry to disable the drive if a fault condition occurs (see FIGURE 7).

INTERNAL PROTECTION CIRCUITRY

The hybrid contains digital protection circuitry, which prevents in-line transistors from conducting simultaneously. This, in effect, would short circuit the power supply and would damage the output stage of the hybrid. The circuitry allows only proper input signal patterns to cause output conduction. Figure 6 and Table 3 show these timing relationships. If an improper input requested that the upper and lower transistors of the same phase conduct together, the output would be a high impedance until removal of the illegal code from the input of the PWR- 82340 or PWR-82342. A dead time of 1000 nsec minimum should still be maintained between the signals at the VU and VI pins; this ensures the complete turn off of any transistor before turning on its associated in-line transistor.

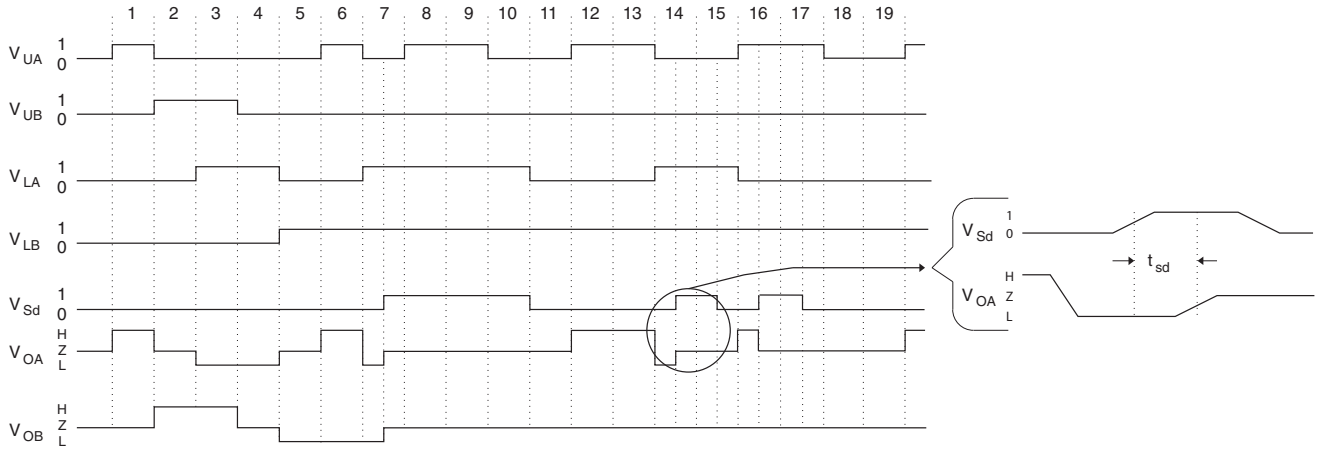


FIGURE 6. SHUT-DOWN (VSD) TIMING RELATIONSHIPS

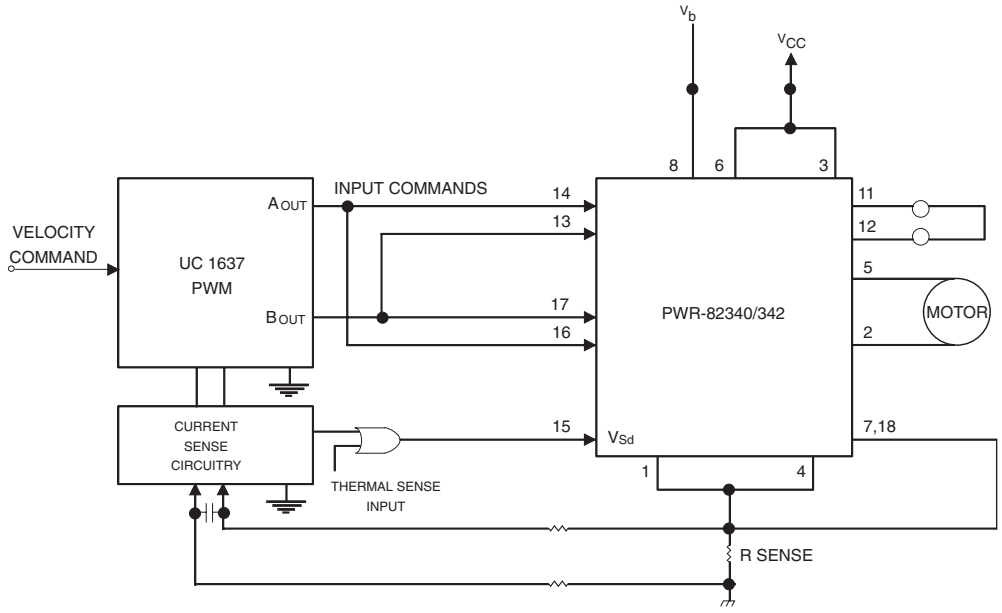


FIGURE 7. FUNCTIONAL SHUT-DOWN INPUT USED WITH CURRENT-SENSING CIRCUITRY

PWR-82340 POWER DISSIPATION (SEE FIGURE 8)

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses.

VCC = 140 V(Bus Voltage)
IOA = 20 A (see FIGURE 9) ; IOB = 30 A; (see FIGURE 8)
ton = 20 ms (see FIGURE 9); T = 40 ms (period)
Ron = 0.1 W (on resistance see Table 2, Io = 30 A, Tc = 25 °C)
ts1 = 250 ns (see FIGURE 9); ts2 = 250 ns (see FIGURE 8)
fo = 25 kHz(switching frequency)
Vf is the diode forward voltage, Table 2, Io = 30 A,Tc = 25 °C
Vf(avg) = 1.15 V
If is the diode forward current

1. Conduction Losses (PC)

PC = I(t)2 x Ron = I motor rms2 x Ron

$$I_{motor\ rms} = \sqrt{\left(I_{OB}^2 - I_{OB}(I_{OB} - I_{OA}) + \frac{(I_{OB} - I_{OA})^2}{3}\right)\left(\frac{t_{on}}{T}\right)}$$

$$I_{motor\ rms} = \sqrt{\left(30^2 - 30\ (30 - 20) + \frac{(30 - 20)^2}{3}\right)\left(\frac{20}{40}\right)}$$

$P_C = (17.80\ A)^2 \times (0.1\ \Omega)$
$P_C = 31.68$ Watts

2. **Switching Losses (P_S)**

$P_S = \{V_{CC}\ [I_{OA}\ (t_{s1}) + I_{OB}\ (t_{s2})]\ f_o\} / 2$
$P_S = \{140\ [20\ (250\ ns) + 30\ (250\ ns)]\ 25k\} / 2$
$P_S = 21.88$ Watts

3. **Flyback diode Losses (P_{df})**

$P_{df} = I_f\ (avg) \times V_f\ (avg)$
$I_f\ (avg) = [(I_{OB} + I_{OA})/2] / 2 = [(30 + 20)/2] / 2 = 12.5$ A
$P_{df} = 12.5\ A \times 1.15$ V
$P_{df} = 14.38$ Watts

To calculate the maximum power dissipation of the output transistor as a function of the case temperature use the following equation. (Reference FIGURE 20 to ensure you don't exceed the maximum allowable power dissipation of each transistor.)

$$P_Q = P_C + P_S$$

To calculate Total Power dissipated in the hybrid use:

$$P_{Total} = \sum_{i=1}^{4} [P_{ci} + P_{si} + P_{dfi}]$$ where i = each transistor or diode.

PWR-82342 POWER DISSIPATION (SEE FIGURE 8)

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses.

VCC = 270 V(Bus Voltage)
IOA = 20 A (see FIGURE 9) ; IOB = 30 A; (see FIGURE 8)
ton = 50 ms (see FIGURE 9); T = 100 ms (period)
VCE(SAT) = 3.8 V (see TABLE 2, Io = 30 A, Tc = 25 °C)
ts1 = 300 ns (see FIGURE 9); ts2 = 300 ns (see FIGURE 8)
fo = 10 kHz(switching frequency)
Vf is the diode forward voltage, Table 2, Io = 30 A,Tc = 25 °C
Vf(avg) = 1.70 V
If is the diode forward current

1. Conduction Losses (PC)

PC = I(t)2 x VCE(SAT) = IAVG x VCE(SAT)

$$I_{AVG} = \left(\frac{(I_{OB} + I_{OA})}{2}\right)\left(\frac{t_{on}}{T}\right)$$

$$I_{AVG} = \left(\frac{(30 + 20)}{2}\right)\left(\frac{50}{100}\right)$$

$P_C = (12.5\ A) \times (3.8\ V)$
$P_C = 47.50$ Watts

2. Switching Losses (P_S)

$P_S = \{V_{CC}\ [I_{OA}\ (t_{s1}) + I_{OB}\ (t_{s2})]f_o\} / 2$
$P_S = \{270\ [20\ (300ns) + 30\ (300ns)]10k\} / 2$
$P_S = 20.25$ Watts

3. Flyback diode Losses (P_{df})

$P_{df} = I_s\ (avg) \times V_f\ (avg)$
$I_f\ (avg) = [(I_{OB} + I_{OA}) / 2] / 2 = [(30 + 20) / 2] / 2 = 12.5$ A
$P_{df} = 12.5\ A \times 1.70$ V
$P_{df} = 21.25$ Watts

To calculate the maximum power dissipation of the output transistor as a function of the case temperature use the following equation. (Reference FIGURE 18 to ensure you don't exceed the maximum allowable power dissipation of each transistor.)

$$P_Q = P_C + P_S$$

To calculate Total Power dissipated in the hybrid use:

$$P_{Total} = \sum_{i=1}^{4} [P_{ci} + P_{si} + P_{dfi}]$$ where i = each transistor or diode.

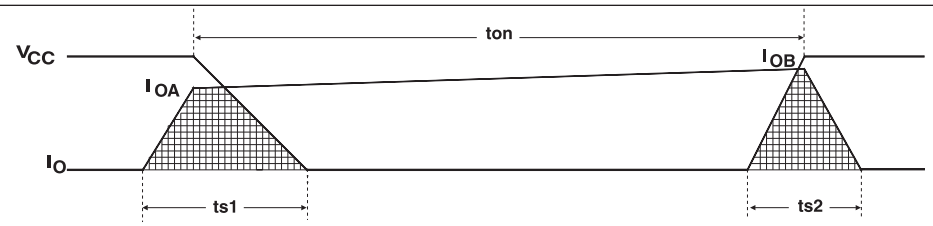


FIGURE 8. OUTPUT CHARACTERISTICS

GROUND CONNECTIONS

LAYOUT AND EXTERNAL COMPONENTS

Important Information - The following information regarding layout guidelines and required external components is critical to the proper operation of these motor drives.

External connections can be easily made to the hybrid by any of the following methods:

- Solder a wire around each pin.

- Use a printed circuit board with a cutout that will enable the printed circuit board to slide over the pins.

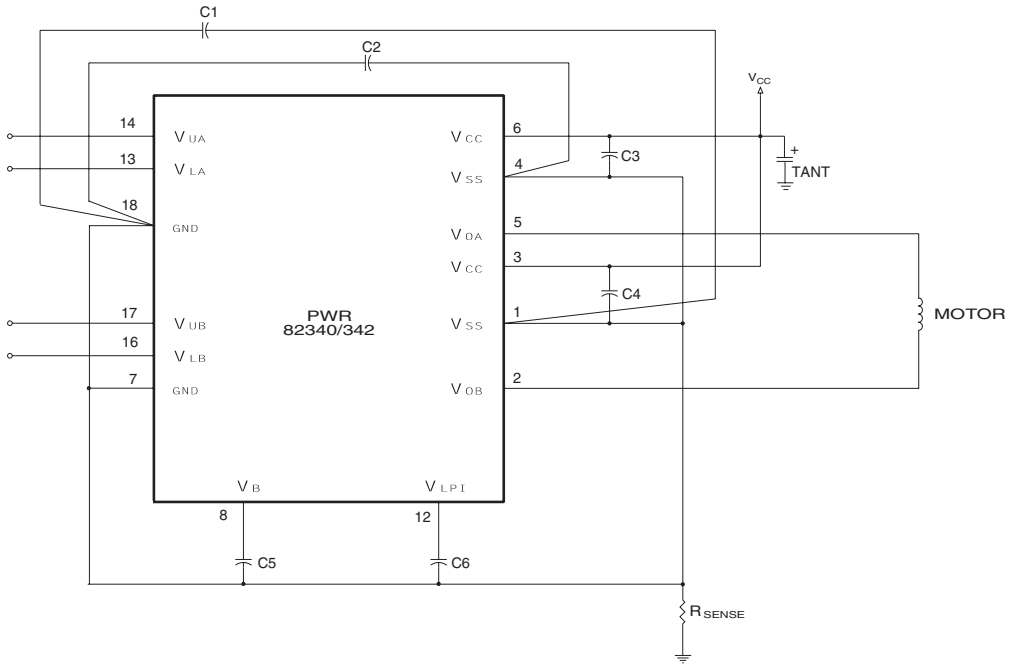
Permanent damage will result to the motor drive if the user does not make the following recommended ground connections that will ensure the proper operation of the hybrid.

The Vb and logic grounds are on pins 7 and 18 (GND). The Vss connections for the output stage are on pins 1 and 4 (Vss). To prevent damage to the internal drive circuitry, the differential voltage between GND (pins 7, 18) and Vss (pins 1, 4) must not exceed ±3 V max, dc or peak. This includes the combined voltage drop of the associated ground paths and the voltage drop across Rsense (see FIGURE 9). For example, a value for Rsense of 0.025 W will give a voltage drop of 1.25 V at 50 A and allow enough margin for the voltage drop in the ground conductors. Locate Rsense 1" - 2" maximum from the hybrid. It is critical that all ground connections be as short, and of lowest impedance, as the system allows.

C1 and C2 are 1 µF, 10 V ceramic capacitors that provide a low ac impedance between each Vss pin and GND. You must use one capacitor for each Vss pin-to-GND connection (total of two capacitors in all). These capacitors are independent of the type of drive scheme used. Since placement of these capacitors is critical, place these capacitors across the hybrid, if possible. Please note, on FIGURE 10, that C1 and C2 must go directly from terminal to terminal on the hybrid — do not daisy chain along the ground return.

C3 and C4 are the 0.1 µF ceramic bypass capacitors that suppress high frequency spiking. The voltage rating should be 2x the maximum system voltage. These capacitors should be located as close to the hybrid as possible.

Care must be taken to control the regenerative energy produced by the motor in order to prevent excessive voltage spiking on the Vcc line. Accomplish this by placing a capacitor or clamping diode between Vcc and the high power ground return.



Notes:
C1, C2 = 1.00 µF, 10 V CERAMIC CAPACITORS
C3, C4 = 0.10 µF, CERAMIC CAPACITORS
C5 = 0.01 µF, 100 V CERAMIC CAPACITOR
C6 = 0.01 µF, 50 V CERAMIC CAPACITOR
TANT = REFER TO MAGNUM MOTOR DRIVE POWER SUPPLY CAPACITIOR SELECTION APPLICATION NOTE (AN/H-7)

FIGURE 9. PWR-82340/342 GROUND CONNECTIONS

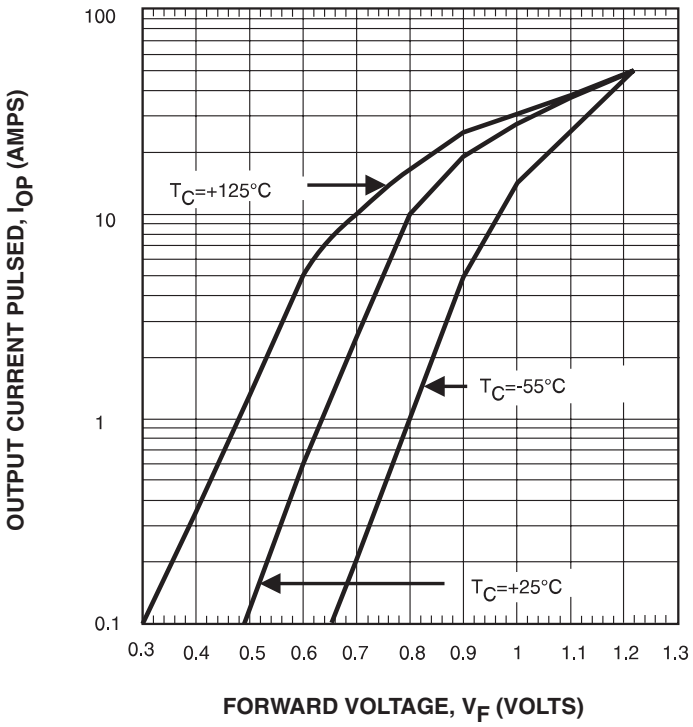


FIGURE 10A. PWR-82340 TYPICAL FORWARD VOLTAGE DROP OF FLYBACK DIODES

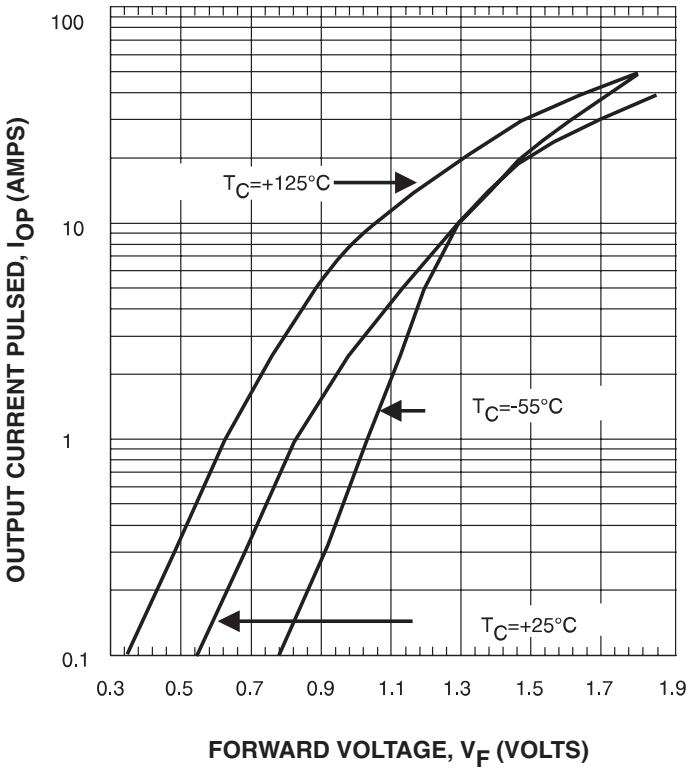


FIGURE 10B. PWR-82342 TYPICAL FORWARD VOLTAGE DROP OF FLYBACK DIODES

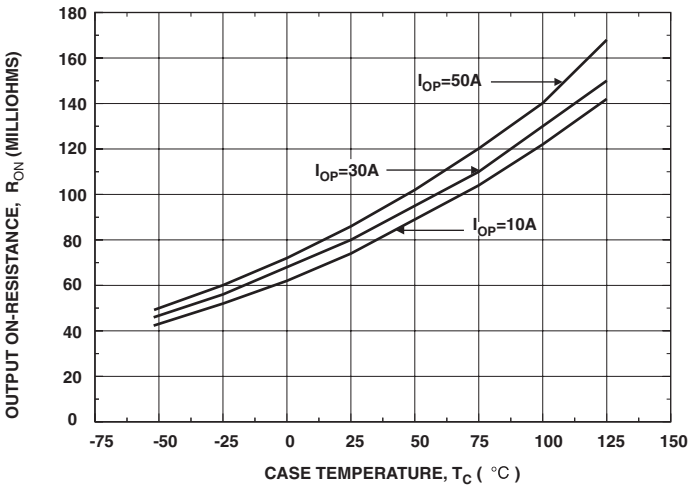


FIGURE 11A. PWR-82340 TYPICAL ON RESISTANCE VARIATION WITH TEMPERATURE

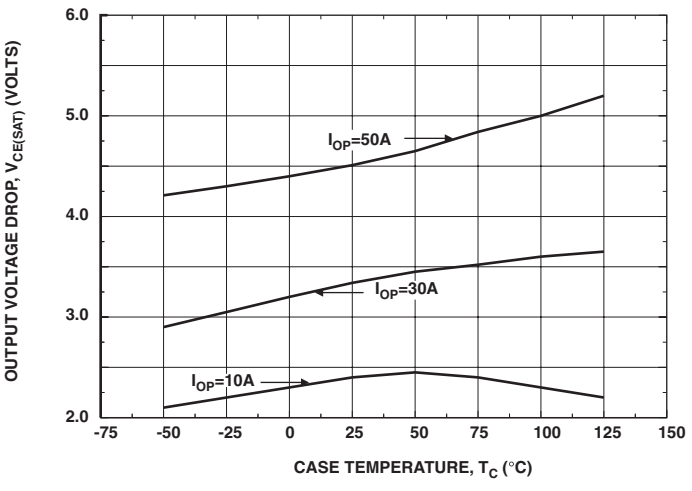


FIGURE 11B. PWR-82342 TYPICAL VCE(SAT) VARIATION WITH TEMPERATURE

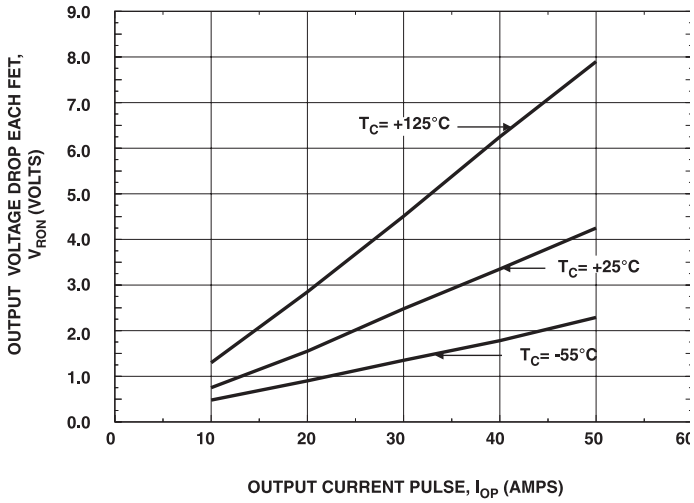


FIGURE 12A. PWR-82340 TYPICAL OUTPUT ON VOLTAGE DROP VERSUS OUTPUT CURRENT

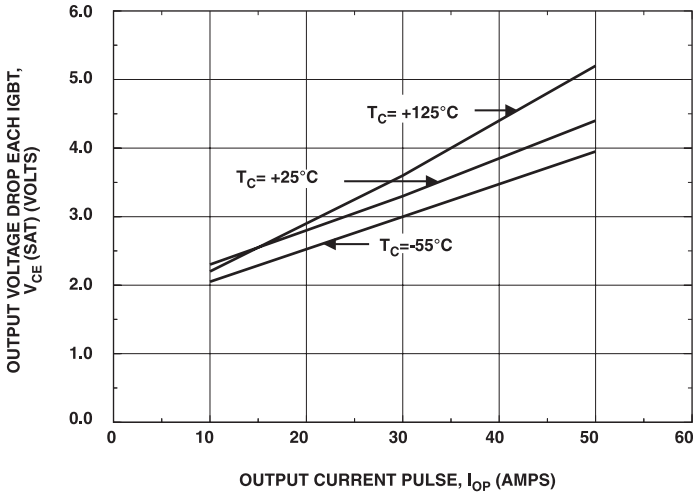


FIGURE 12B. PWR-82342 TYPICAL OUTPUT ON VOLTAGE DROP VERSUS OUTPUT CURRENT

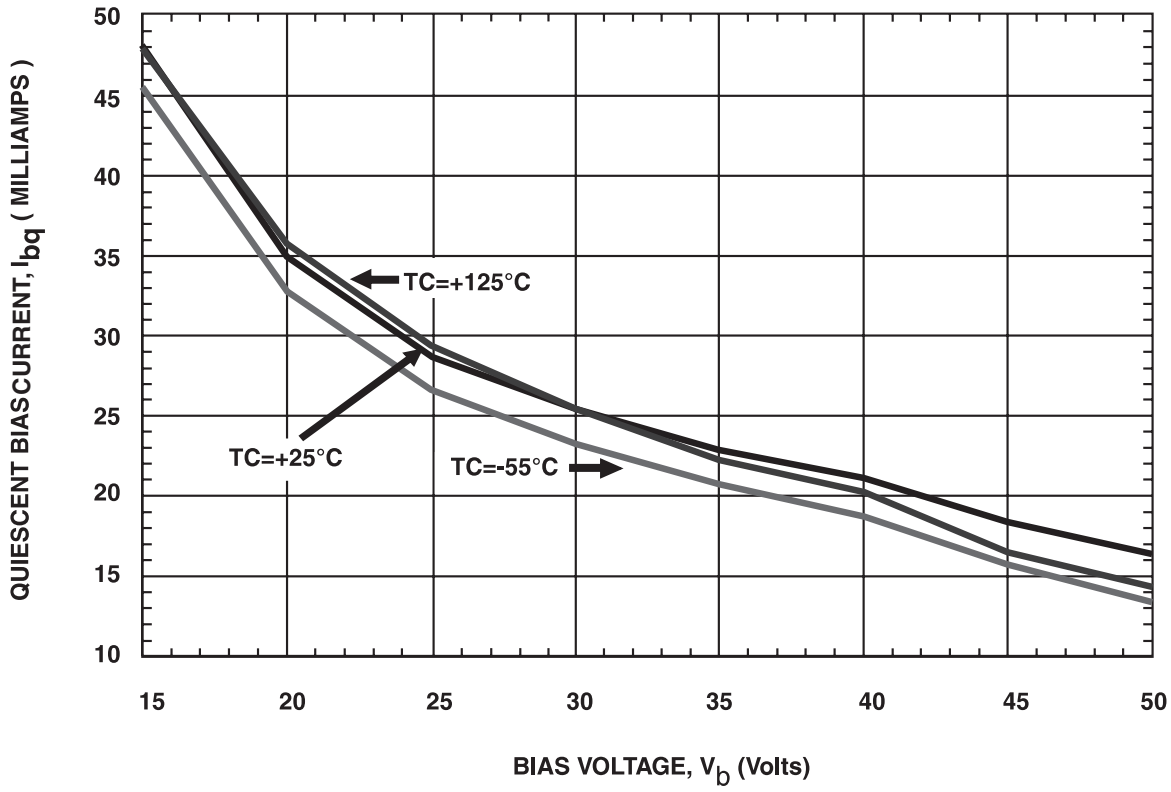


FIGURE 13. PWR-82340/342 TYPICAL QUIESCENT BIAS CURRENT VERSUS BIAS VOLTAGE

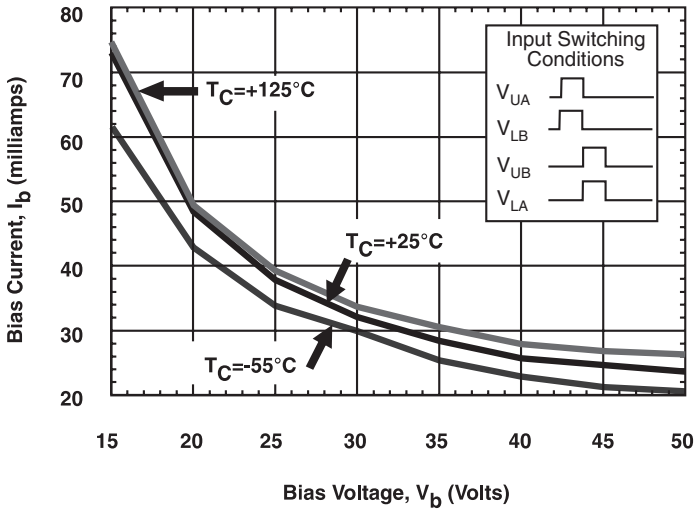


FIGURE 14A. PWR-82340 TYPICAL BIAS CURRENT VERSUS BIAS VOLTAGE AT F_0 = 30 KHZ

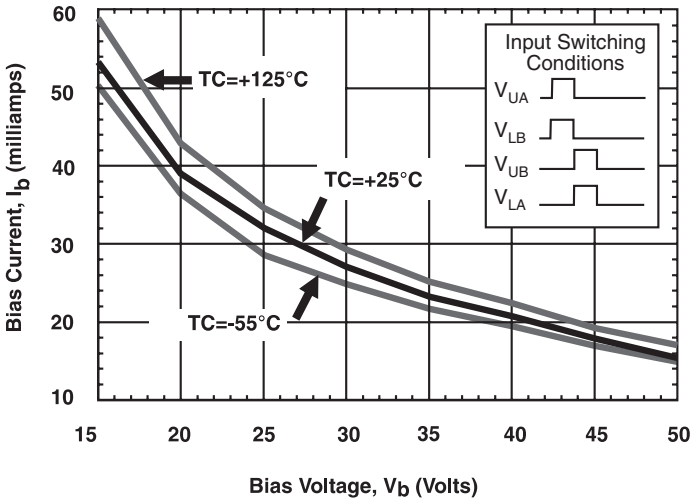


FIGURE 14B. PWR-82342 TYPICAL BIAS CURRENT VERSUS BIAS VOLTAGE AT F_0 = 10 KHZ

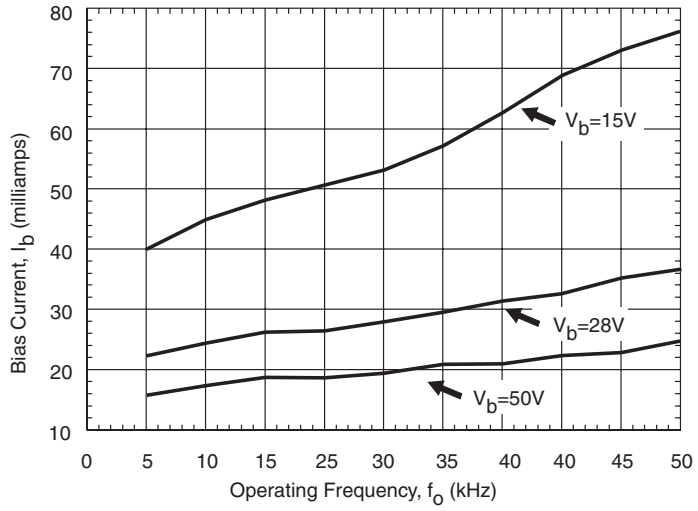


FIGURE 15A. PWR-82340 TYPICAL BIAS CURRENT VERSUS OPERATING FREQUENCY

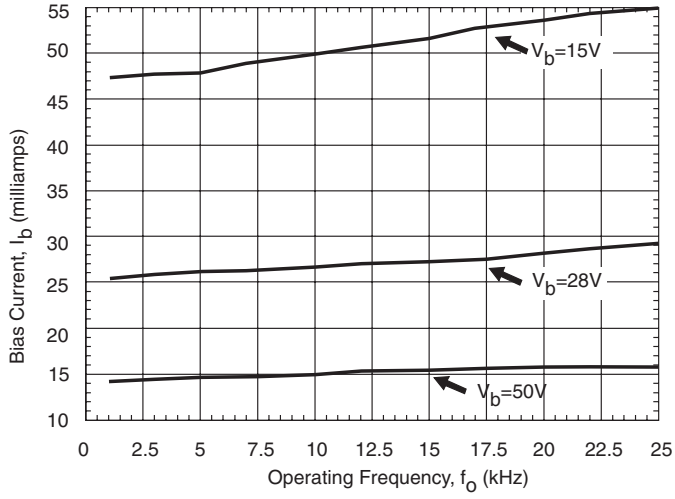


FIGURE 15B. PWR-82342 TYPICAL BIAS CURRENT VERSUS OPERATING FREQUENCY

MOUNTING

The package bolts to part of the chassis or even the motor assembly itself, depending on system requirements. In applications where this isn't convenient, the hybrid can be mounted to its own heatsink. The heat transfer in a hybrid is from semiconductor junction to the bottom of the hybrid case. The flatness and maximum temperature of this mounting surface are critical to proper performance and reliability, because this is the only method of dissipating the power created in the hybrid. Use a mounting surface flatness of 0.004 inches/inch maximum. This interface can be improved with the use of a thermal compound or pad. The heatsink should be designed to insure that the case temperature does not exceeded +125°C.

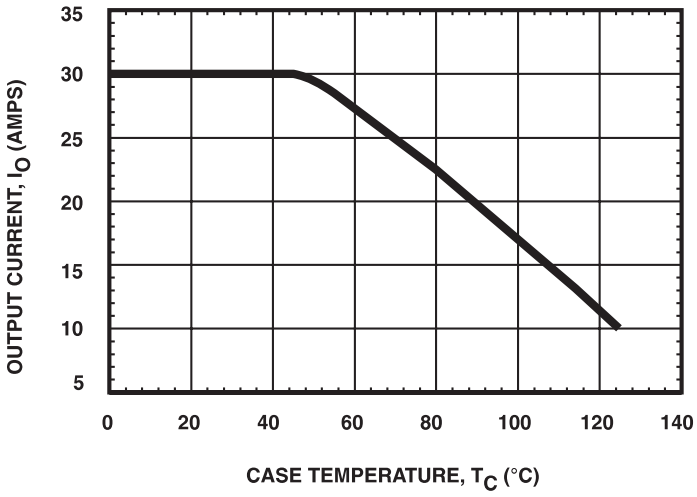


FIGURE 16A. PWR-82340
MAXIMUM ALLOWABLE CONTINUOUS OUTPUT CURRENT VERSUS CASE TEMPERATURE

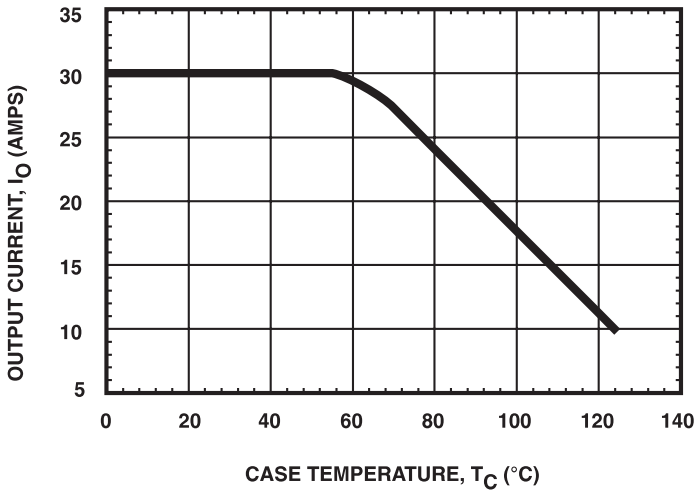


FIGURE 16B. PWR-82342
MAXIMUM ALLOWABLE CONTINUOUS OUTPUT CURRENT VERSUS CASE TEMPERATURE

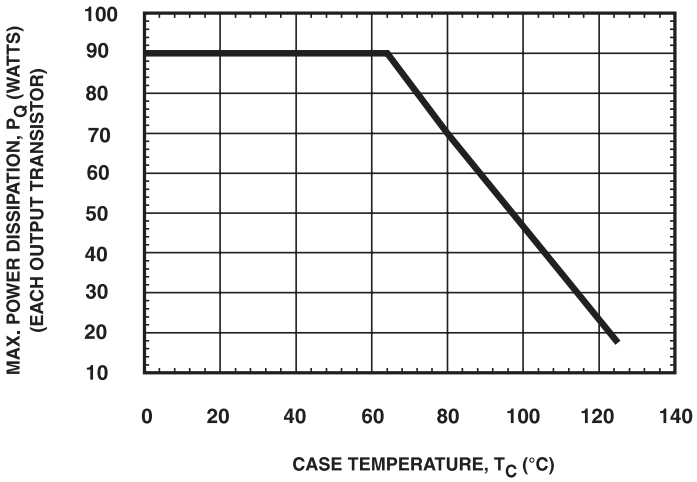
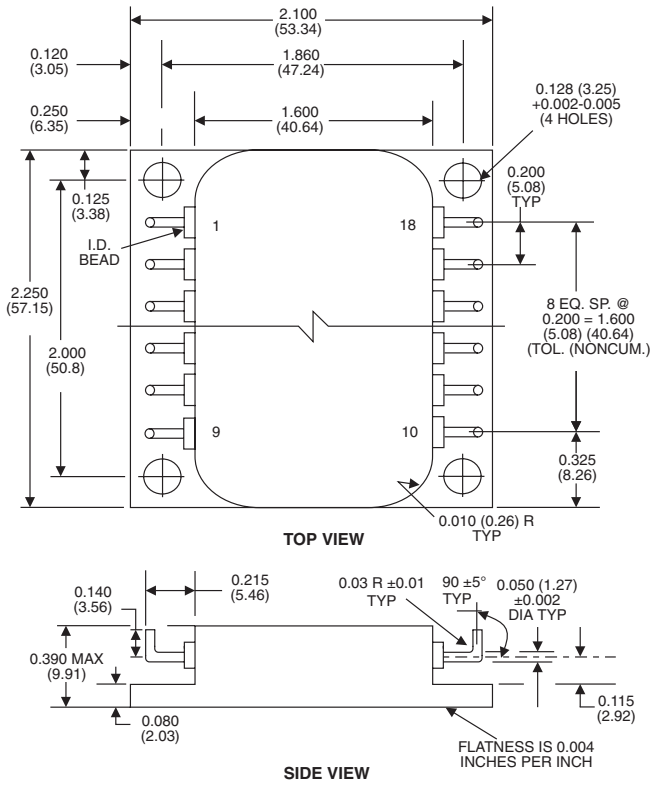


FIGURE 17. PWR-82340 AND PWR-82342 MAXIMUM ALLOWABLE POWER DISSIPATION OF EACH OUTPUT TRANSISTOR VERSUS CASE TEMPERATURE

TABLE 3. INPUT-OUTPUT TRUTH TABLE

INPUTS						OUTPUTS
UPPERS		LOWERS		CONTROL		
V_{UA}	V_{UB}	V_{LA}	V_{LB}	V_{Sd}	V_{OA}	V_{OB}
0	0	1	1	0	L	L
0	1	1	0	0	L	H
1	0	0	1	0	H	L
1	1	0	0	0	H	H
1	X	1	X	0	Z	X
X	1	X	1	0	X	Z
0	0	0	0	0	Z	Z
X	X	X	X	1	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)



NOTE: Dimensions in inches (mm).

FIGURE 18. PWR-82340 AND PWR-82342 MECHANICAL OUTLINE

TABLE 4. PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	V_{SS}	18	GND
2	V_{OB}	17	V_{UB}
3	V_{CC}	16	V_{LB}
4	V_{SS}	15	V_{Sd}
5	V_{OA}	14	V_{UA}
6	V_{CC}	13	V_{LA}
7	GND	12	V_{LPI}
8	V_b	11	V_{LPO}
9	N/C	10	N/C
Note: Pins 3 and 6 are internally connected;Pins 7 and 18 are internally connected.			

ORDERING INFORMATION

PWR-8234X -X X 0

Reliability Grade:
0 = Standard DDC Procedures.
1 = Military processing available.
2 = Military processing available without QCI testing.

Temperature Range:
1 = -55 to +125°C
3 = 0 to +70°C

Rating:
0 = 200 V using MOSFETs
2 = 500 V using IGBTs

These products contain tin-lead solder finish as applicable to solder dip requirements.

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS

TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 (note 1), 1030 (note 2)	TABLE 1

Notes:
1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

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RECORD OF CHANGE

For PWR-82340 Data Sheet

Revision	Date	Pages	Description
L	11/2009	3, 5	Removed Preliminary Stamp. Edit to Input Signals in Table 2. Edits to Bias Voltage Section. Deleted Figure 4. Updated Figure 10.
M	1/2010	2, 3, 5, 6, 11, 12, 14	Updated Figure 1. Deleted V zener specs from Table 2. Updated Input Signals section in Table 2. Updated Figure 3. Updated Figure 5. Updated Figure 13. Updated Figures 14A and 14B. Updated Captions for Figures 15A and 15B. Updated Table 4.

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