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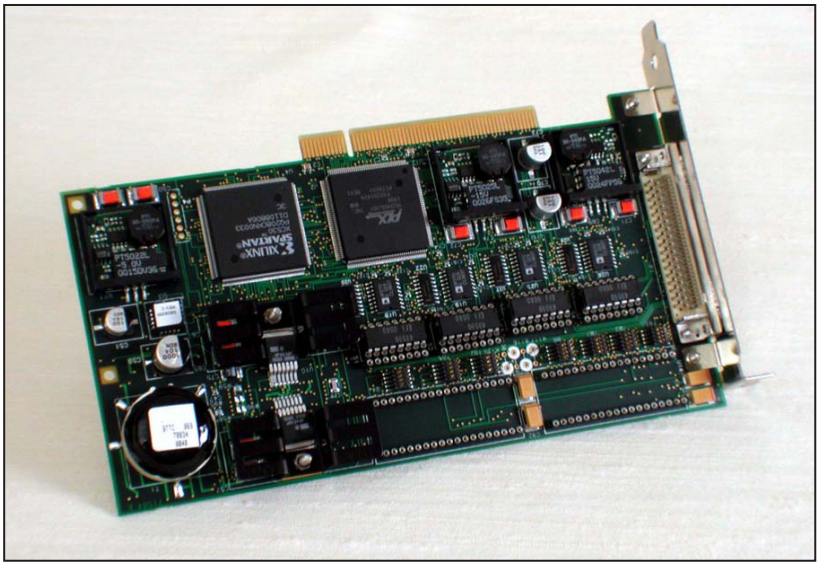
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SB-36200IX

COMBINATION S/R-TO-DIGITAL AND DIGITAL-TO-S/R PCI BUS CONVERTER CARD

Make sure the next Card you purchase has...

DDC on Board®



DESCRIPTION

The SB-36200IX is a PCI bus card that contains four channels of fully independent Synchro/Resolver-to-Digital (S/R-D) conversion and up to two channels of Digital-to-Synchro/Resolver (D-S/R) conversion. The SB-36200IX card has an onboard programmable oscillator to support a voltage range of 0 to 26 Vrms from 360 to 7kHz.

SYNCHRO/RESOLVER-TO-DIGITAL

The resolution (10, 12, 14 or 16 bit) and bandwidth (100 Hz/300 Hz) are software programmable. Each channel has an independent signal and reference input. The standard inputs are solid state. Signal connections are provided through a 68-pin mini D-type connector (P1).

DIGITAL-TO-SYNCHRO/RESOLVER

The SB-36200IX PCI card has up to two channels of fully independent Digital-to-Synchro or Digital-to-Resolver conversion. For each channel the conversion process is implemented using DDC D/S or D/R converters DSC-11520, DSC-11524 or DR-11525 (See hybrid data sheets for output characteristics).

APPLICATIONS

The SB-36200IX has been designed for modern, high performance industrial and military position feedback, control, and test systems. Typical motion feedback applications include motor control, machine tool control, antenna control, robotics, and process control systems. The SB-36200IX is supplied with a Windows GUI which creates a simple graphical interface to analyze or simulate position information, direction and BIT.

FEATURES

- Includes Four RD-19230 Converters
- Software Programmable: Resolution (10, 12, 14, or 16 Bit) and Bandwidth (100/300 Hz)
- Input Amplitude: 2 $V_{rms(L-L)}$, 11.8 $V_{rms(L-L)}$
- Optional Two Channels of Digital-to-Synchro/Resolver Conversion
- Dynamic Rotation
- Two-Speed Measurement and Simulation
- Onboard Programmable Oscillator with 1.5 VA Drive
- Software Support
  - High Level API Libraries for Windows 9x/2000/XP/NT and Linux
  - dataSIMS/dataMARS
  - LabVIEW (contact factory)
- 0° to 71° C Standard Operating Temperature
- Velocity Output
- Output Amplitudes: 11.8 $V_{rms(L-L)}$ Synchro, 11.8 $V_{rms(L-L)}$ Resolver, 2 $V_{rms(L-L)}$ Direct
- Output Voltages can be Scaled Lower
- A quad B Encoder Emulation

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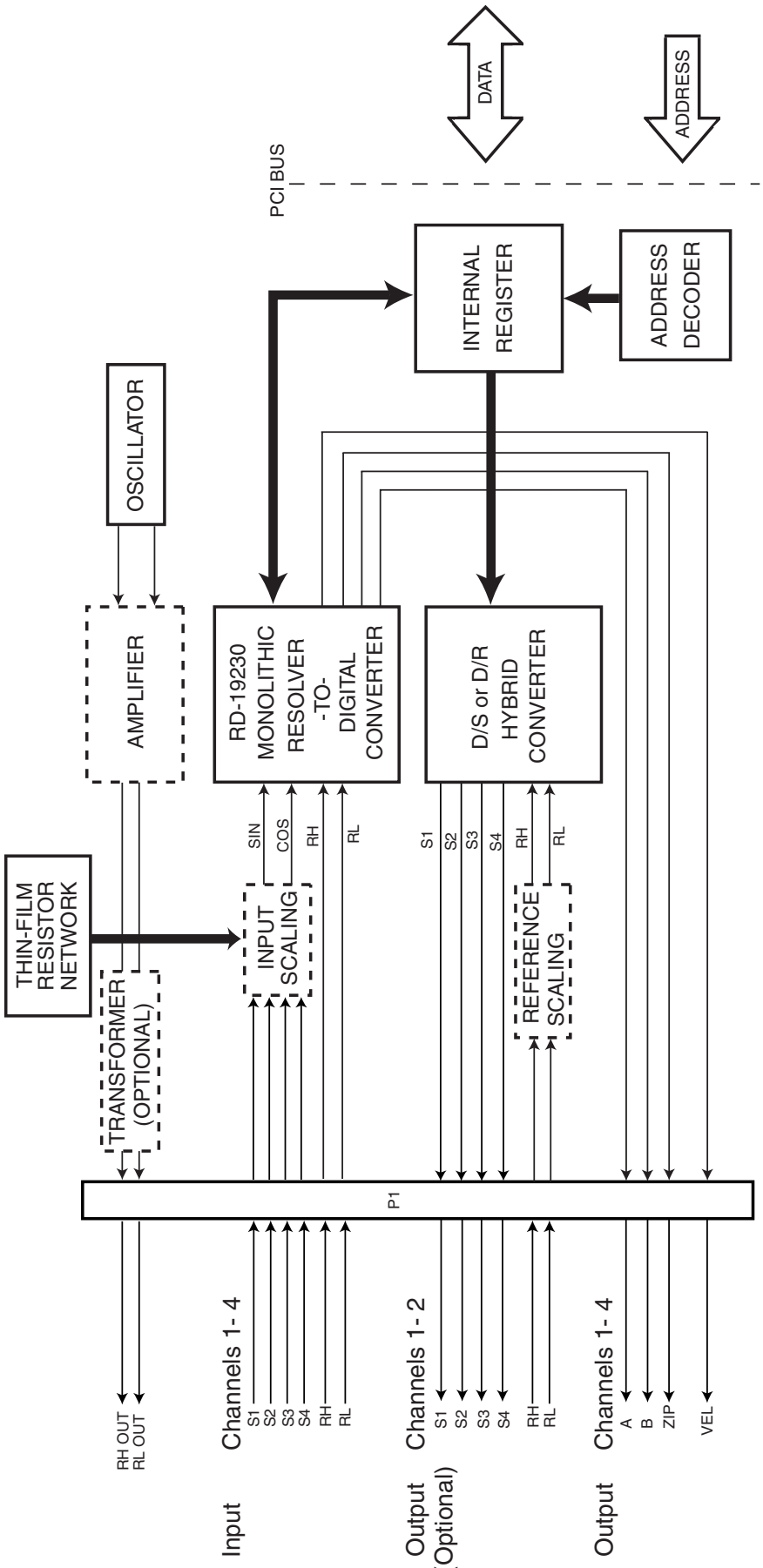


FIGURE 1. SB-36200IX BLOCK DIAGRAM

TABLE 1. SB-36200IX SPECIFICATIONS (PER CHANNEL)

These specifications apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation and 10% harmonic distortion.

PARAMETER	UNIT	VALUE		
RESOLUTION	Bits	10, 12, 14, or 16 programmable		
		Input Frequency		
		47 -1k (NOTE 2)	1k - 4k	4k - 7k
ACCURACY (S/R-D) RD-19230 (1 Min + 1 LSB)	Minutes	1 + 1 LSB	1 + 1 LSB	2 + 1 LSB
ACCURACY (D-S/R)				
DSC-11520-305	Minutes	1	For frequencies higher than 1 kHz use the DR-11525 and refer to the converter data sheet specifications.	
DR-11525-305	Minutes	1		
DSC-11524-304	Minutes	2		
OSCILLATOR		(Option A)		
Carrier Frequency	Hz	360 - 7k		
Voltage Range	Vrms	0 - 26		
Drive	mA. max	60		
SIGNAL INPUT (S/R-D)		Solid State		
(Synchro Type)	Vrms L-L	11.8		—
• Zin line-to-line	Ohms	52k		—
• Zin each line-to-ground	Ohms	35k		—
(Resolver Type)	Vrms L-L	11.8		2Vrms direct
• Zin single ended	Ohms	70k		10M ‖ 20pF (NOTE 1)
• Zin differential	Ohms	140k		N/A
Common-mode Range	V	30 max.		N/A
R/D REFERENCE INPUT	Vrms	4.4	26	115
Voltage Range	Vrms	2 - 40	12 - 40	62 - 130
Input Impedance				
• Single Ended	kOhms	200	100	600
• Differential	kOhms	400	200	1200
D/R REFERENCE INPUT	Vrms	4.4	26	115
Input Impedance				
• Single Ended	kOhms	45	25	125
• Differential	kOhms	90	50	250
D - S/R DRIVE				
DSC-11520	mA(rms)	2 max		
DSC-11524	mA(rms)	15 max		
DR-11525	mA(rms)	2 max		
DYNAMIC ROTATION	rps min/max	at 12 bit resolution (0.03 to 2014) at 16 bit resolution (0.05 to 125)		

TABLE 1. SB-36200IX SPECIFICATIONS (CONT.) (PER CHANNEL)

These specifications apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation and 10% harmonic distortion.

PARAMETER	UNIT	VALUE
DIGITAL OUTPUTS (S/R-D)		
A, B, Zero Index Pulse(ZIP) Drive Capability		50 Pf+ Logic 0: 1 TTL load, 1.6 mA at 0.4 V max. Logic 1: 10 TTL loads, -0.4 mA at 2.8 V min.
After Set into A quad mode		Logic 0: 100 mV max. driving CMOS Logic 1: +5 V supply minus 100mV min. driving CMOS
DIGITAL INPUTS (D-S/R) Logic Type		Natural binary angle, parallel positive logic CMOS and TTL compatible. Inputs are CMOS transient protected. Logic 0 = 0 to +1 V Logic 1 = 2.2 V to +5 V
	µA	20 max to GND (bits 1 - 16)
	µA	20 max to +5 V (/LL, /LM, /LA)
		(See timing diagrams in D-S/R data sheets)
POWER SUPPLY (NOTE 5)		
Voltage	Vdc	+5
S/R-D Current	Amax	0.5 with oscillator, no load, 4 channels (worst case)
D-S/R Current	Amax	1.3 with oscillator, no load, 2 channels (worst case)
TEMPERATURE RANGE		
Operating (SB-3620XIX-3XX)	°C	0 to +70
Storage	°C	-40 to +85
PHYSICAL CHARACTERISTICS	in. (mm.)	7.7 x 4.2 x 0.91 (195.6 x 106.7 x 23.1)

NOTES:
1. ‖ = "in parallel with."
2. If the frequency is between 47 and 1 kHz, then there will be 1 LSB jitter in the S/R-D.
3. See specific converter data sheets for further specifications.
4. Requires a 5V PCI card slot, will not operate on a 3.3V PCI slot.

TABLE 2. DYNAMIC CHARACTERISTICS (S/R-D)

TYPE		400 HZ NOMINAL			
Resolution (bits)		10	12	14	16
Bandwidth (Hz)	Low	*	*	100	
	High	300		**	**
Tracking Rate (rps)		320	80	20	5
Scale Factor (Volts/rps)		.0125	.05	.2	.8

* Not Recommended - Low bandwidths in low resolutions may induce spin around and the part will not settle.
**High bandwidths in high resolutions may be used with carrier frequencies above1.5 kHz.

TABLE 3. VELOCITY CHARACTERISTICS (S/R-D)

PARAMETER	UNITS	TYPICAL	MAX. / MIN.
POLARITY Voltage Range	V	4.0	
VOLTAGE SCALING (resolution dependent)	Volts/rps	Typical Tracking Rate (See TABLE 2)	
SCALE FACTOR			
Error	%	10	20 (max.)
Scale Factor TC	PPM / deg C	100	200 (max.)
Reversal Error	%	1	2 (max.)
Linearity	% output	0.5	1 (max.)
Zero Offset	mV	5	15 (max.)
Zero Offset TC	uV / deg C	15	30 (max.)
Load	k Ohms		10 (min.)

SYNTHESIZED REFERENCE

The RD-19230 input converters contain a synthesized reference, which eliminates errors due to phase shift between the reference and the signal inputs up to 45°. Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. Due to the inductive nature of resolvers and synchros, their output signals lead the reference input signal (RH and RL). When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. Therefore this is the perfect solution to combat phase shift error to 45°.

BUILT-IN-TEST

Built-In-Test (BIT) will flag Loss-Of-Signal (LOS) and Loss-Of-Reference (LOR) fault conditions. Also, excessive error is detected by monitoring the demodulator output, which is proportional to the difference between the analog input and the digital output. When it exceeds approximately 100 LSBs of positive or 250 LSBs of negative error (in the selected resolution), the BIT will be asserted. This condition can occur any time the analog input changes at a rate in excess of the maximum tracking rate. During power up, the converter may see a large difference between the sin/cos inputs and the digital output angle held in its counter. BIT will be asserted until the converter settles within approximately 250 LSBs of the final result.

ONBOARD INTERNAL REFERENCE OSCILLATOR

The onboard oscillator is available with a 1.5VA output drive capability. This onboard reference oscillator may be looped back to each input channel's independent reference input. Frequency and voltage are software programmable.

INTERNAL INCREMENTAL OPTICAL ENCODER EMULATION

The card can be programmed to encoder emulation mode (Refer to FIGURES 2 and 3). These outputs are available on the P1 connector A, B & ZIP (which is the zero index pulse). The timing of the A, B output is dependent on the rate of change of the synchro/resolver position (rps or degrees per second) and the encoder resolution latched into the converter.

DUAL BANDWIDTHS

The user can program bandwidth for each input channel independently through software. Each can be programmed for bandwidths of either 100 or 300Hz.

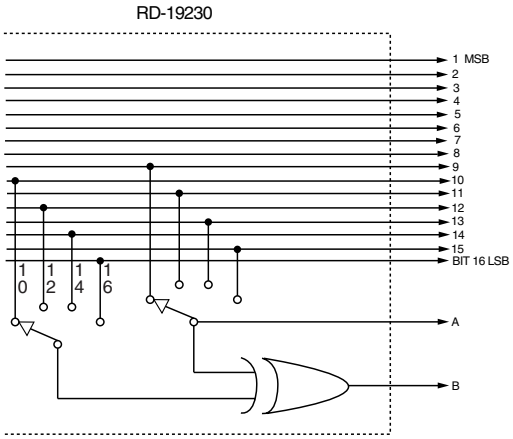


FIGURE 2. INCREMENTAL ENCODER EMULATION RESOLUTION CONTROL

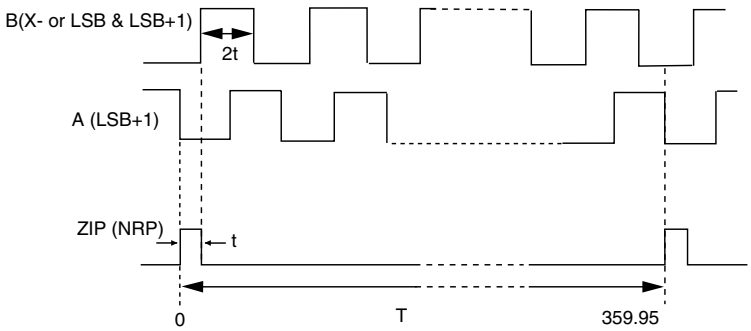


FIGURE 3. INCREMENTAL ENCODER EMULATION

S/R SIGNAL INPUT CONFIGURATION

Configuration for the synchro/resolver inputs is accomplished by the use of specific thin-film resistor networks installed on the card. These networks also scale the input voltage to the converter for a choice of either 2V L-L or 11.8V L-L.

SYNCHRO/RESOLVER-TO-DIGITAL

Refer to FIGURE 4 for socket locations on the card. TABLE 4 lists the resistor network and location for each input option.

TABLE 4. SIGNAL INPUT CONFIGURATION

INPUT TYPE	THIN FILM RESISTOR NETWORK	LOCATION
2V Direct	DDC - 55688-1	Lower Sockets
11.8V Resolver	DDC - 49530	Lower Sockets
11.8V Synchro	DDC - 49530	Upper Sockets

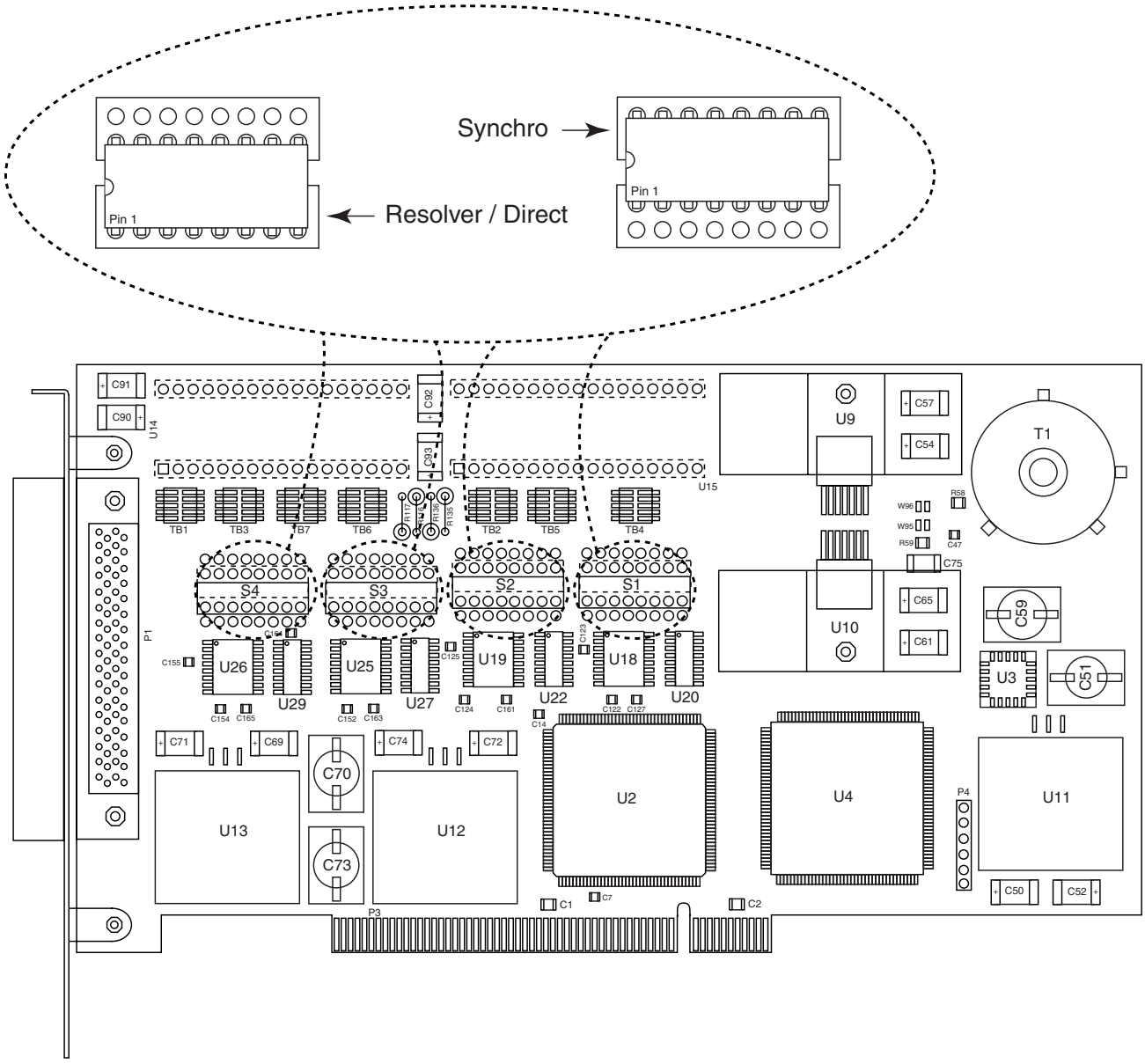


FIGURE 4. INPUT SIGNAL CONFIGURATION

S-R/D SIGNAL OUTPUT AND D/S-R INPUT CONFIGURATION

The PCI bus provides the 16-bit data word (digital angle). The address and data bits are multiplexed. The 16-bit data is available on the bus for hardware or software manipulation via the AD[1-16] lines. The pinouts for a standard 5 V PCI bus are shown in TABLE 5. Side “A” and side “B” of the SB-36200IX card are identified in FIGURE 5.

SIGNAL CONNECTIONS

• Synchro Mode Connect S1, S2, S3
  S1 = X
  S2 = Z
  S3 = Y

• Resolver Mode Connect
  S3 = +SIN
  S1 = -SIN
  S2 = +COS
  S4 = -COS

• Single-ended Mode Connections
  - When using 2V single-ended configurations, S1 and S4 on card connector are no-connect. S1 and S4 must be commonly tied to card ground.
  S3 to +SIN
  S2 to +COS
  S1 and S4 common to card ground

• Ground Connections
  - For velocity and single-ended inputs or outputs, reference to AGND.
  - For A quad B signals, reference to PWR GND.
  - For single-ended oscillator, reference to PWR GND.

SOFTWARE

Software programmable resolutions, in 10, 12, 14 or 16 bit resolutions, are attainable. The user can also program bandwidth for each input channel independently through software. The card can be programmed for bandwidths of either 100 or 300Hz.

Windows GUI example software and DOS console application example software are included. The provided DLL allows the

TABLE 5. (5 V) PCI BUS PINOUTS

PIN	SIDE B	SIDE A	PIN	SIDE B	SIDE A
1	-12V	TRST#	32	AD[17]	AD[16]
2	TCK	+12V	33	C/BE[2]#	+3.3V
3	Ground	TMS	34	Ground	FRAME#
4	TDO	TDI	35	IRDY#	Ground
5	+5V	+5V	36	+3.3V	TRDY#
6	+5V	INTA#	37	DEVSEL#	Ground
7	INTB#	INTC#	38	Ground	STOP#
8	INTD#	+5V	39	LOCK#	+3.3V
9	PRSNT1#	Reserved	40	PERR#	SDONE
10	Reserved	+5V (I/O)	41	+3.3V	SBO#
11	PRSNT2#	Reserved	42	SERR#	Ground
12	Ground	Ground	43	+3.3V	PAR
13	Ground	Ground	44	C/BE[1]#	AD[15]
14	Reserved	Reserved	45	AD[14]	+3.3V
15	Ground	RST#	46	Ground	AD[13]
16	CLK	+5V (I/O)	47	AD[12]	AD[11]
17	Ground	GNT#	48	AD[10]	Ground
18	REQ#	Ground	49	Ground	AD[09]
19	+5V (I/O)	Reserved	50	Connector Key	Connector Key
20	AD[31]	AD[30]	51	Connector Key	Connector Key
21	AD[29]	+3.3V	52	AD[08]	C/BE[0]#
22	Ground	AD[28]	53	AD[07]	+3.3V
23	AD[27]	AD[26]	54	+3.3V	AD[06]
24	AD[25]	Ground	55	AD[05]	AD[04]
25	+3.3V	AD[24]	56	AD[03]	Ground
26	C/BE[3]#	IDSEL	57	Ground	AD[02]
27	AD[23]	+3.3V	58	AD[01]	AD[00]
28	Ground	AD[22]	59	+5V (I/O)	+5V (I/O)
29	AD[21]	AD[20]	60	ACK64#	REQ64#
30	AD[19]	Ground	61	+5V	+5V
31	+3.3V	AD[18]	62	+5V	+5V

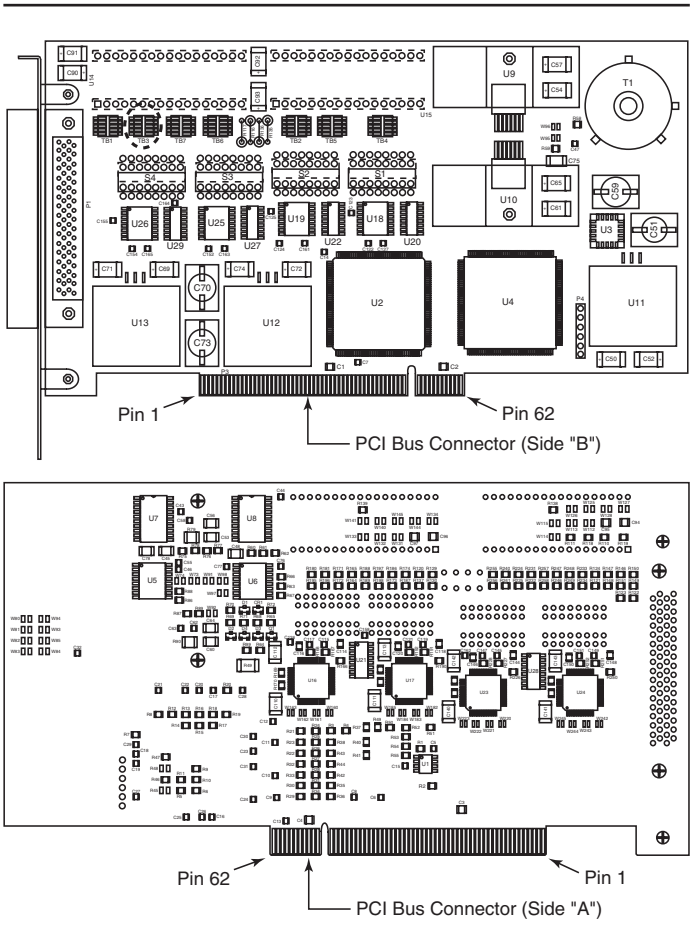


FIGURE 5. 5V-PCI BUS

user to create custom application software. The software DLL provides function calls to control resolution, bandwidth, reference amplitude and reference frequency. This provides access to angular information and can drive dynamic rotation of the output.

Support is also available for *dataSIMS* software. Contact DDC software applications department for details.

CARD PINOUTS

The card uses one 68-pin mini D connector for input and output connections. The pinouts for the mating connector are shown in TABLE 6 and FIGURE 6.

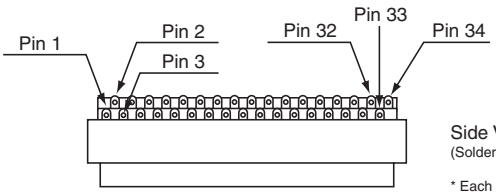
Note: All ground returns are connected to the chassis ground.

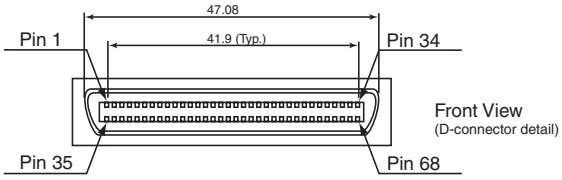
INPUT CONNECTIONS

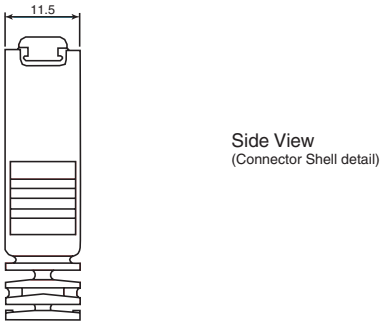
The P1 connector contains all input signal connections for each channel. Along with synchro/resolver inputs this connector also contains each channel's reference input connection for RH/RL. To use the internal board oscillator instead of an outside reference signal, loop back the internal reference signal "RH/RL out" into each specific channel's reference input.

OUTPUT CONNECTIONS

The P1 connector contains the Digital-to-Synchro/Resolver signals as well as velocity and the encoder emulation outputs A, B, & ZIP. (BIT is available from a read register accessed on the PCI bus.). Card has 68-pin connector, N10268-5242VC, mini D ribbon.







P/N: Acon HPBW-3168-10S-N-KV3 or KV7 (68 pin connector solder plug and junction shell)

FIGURE 6. 68-PIN D-TYPE MATING CONNECTOR

TABLE 6. SB-36200IX P1 PINOUTS

PIN	NAME	INPUT OR OUTPUT	PIN	NAME	INPUT OR OUTPUT
1	B-S/D-Channel A	O	35	A-S/D-Channel A	O
2	ZIP-S/D-Channel A	O	36	ZIP-S/D-Channel B	O
3	B-S/D-Channel B	O	37	A-S/D-Channel B	O
4	B-S/D-Channel C	O	38	A-S/D-Channel C	O
5	ZIP-S/D-Channel C	O	39	ZIP-S/D-Channel D	O
6	B-S/D-Channel D	O	40	A-S/D-Channel D	O
7	VEL-S/D-Channel A	O	41	VEL-S/D-Channel D	O
8	VEL-S/D-Channel B	O	42	POWER GROUND **	
9	VEL-S/D-Channel C	O	43	N/C*	
10	N/C*		44	AGND-D/R-Channel A**	
11	S1-D/R-Channel A	O	45	S3-D/R-Channel A	O
12	S2-D/R-Channel A	O	46	S4-D/R-Channel A	O
13	RL-D/R-Channel A	I	47	RH-D/R-Channel A	I
14	N/C*		48	AGND-D/R-Channel B**	
15	S1-D/R-Channel B	O	49	S3-D/R-Channel B	O
16	S2-D/R-Channel B	O	50	S4-D/R-Channel B	O
17	RL-D/R-Channel B	I	51	RH-D/R-Channel B	I
18	N/C*		52	AGND-S/D-Channel D**	
19	S1-S/D-Channel D	I	53	S3-S/D-Channel D	I
20	S2-S/D-Channel D	I	54	S4-S/D-Channel D	I
21	RL-S/D-Channel D	I	55	RH-S/D-Channel D	I
22	N/C*		56	AGND-S/D-Channel C**	
23	S1-S/D-Channel C	I	57	S3-S/D-Channel C	I
24	S2-S/D-Channel C	I	58	S4-S/D-Channel C	I
25	RL-S/D-Channel C	I	59	RH-S/D-Channel C	I
26	POWER GROUND**		60	AGND-S/D-Channel B**	
27	S1-S/D-Channel B	I	61	S3-S/D-Channel B	I
28	S2-S/D-Channel B	I	62	S4-S/D-Channel B	I
29	RL-S/D-Channel B	I	63	RH-S/D-Channel B	I
30	POWER GROUND**		64	AGND-S/D-Channel A**	
31	S1-S/D-Channel A	I	65	S3-S/D-Channel A	I
32	S2-S/D-Channel A	I	66	S4-S/D-Channel A	I
33	RL-S/D-Channel A	I	67	RH-S/D-Channel A	I
34	INT REF - 26 - RH	O	68	INT REF - RL	O

NOTES:
I=Input O=Output
* Leave pin unconnected.
** All power gnds, D/R-AGND's and AGND's are internally connected together to a digital ground reference.

SCALING LOWER OUTPUT VOLTAGES

All output voltages can be scaled down by lowering the required reference input voltage as follows:

$$\text{Reference Input Voltage} = \frac{\text{Desired Output Voltage}}{X}$$

(Where X is the output option ratio multiplier - refer to Table 7).

Example (using an 11.8 volt synchro option 1 card):

Desired Output Voltage = 9V $_{L\text{-}L}$
Multiplier X = .45 (for option #1)

(note that desired output voltage is lower than the card selection output voltage)

$$\text{Reference Input Voltage} = \frac{9\ V_{L\text{-}L}}{.45}$$

Reference Input Voltage = 20 V

TABLE 7. REFERENCE MULTIPLIER (FOR NON-STANDARD D-S/R OUTPUT VOLTAGES)

OUTPUT OPTION	OUTPUT TYPE	NOMINAL REFERENCE INPUT (VRMS)	MULTIPLIER X
1	11.8V $_{L\text{-}L}$ Synchro	26	**0.45**
2	11.8V $_{L\text{-}L}$ Resolver	26	**0.45**
3	11.8V $_{L\text{-}L}$ Synchro	115	**0.10**
4	2V Direct (single ended)	4.4	**0.455**

TABLE 8. INTERNAL REFERENCE OSCILLATOR OUTPUTS

OSCILLATOR OUTPUT OPTION #	VOLTAGE OUTPUT	P1 CONNECTOR PIN	
A	26 Vrms	RH = 34	RL = 68

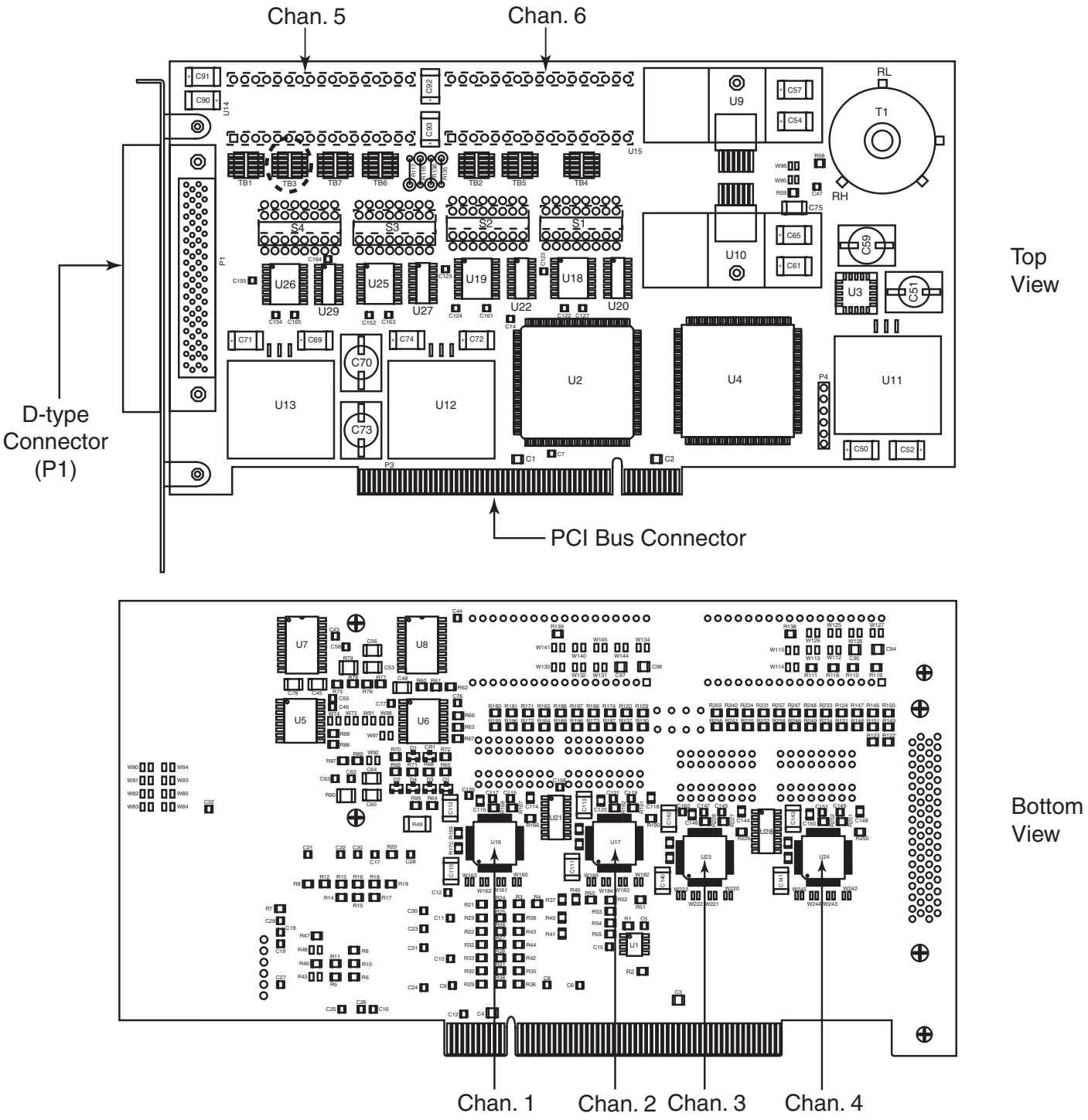


FIGURE 7. SB-3620X CARD ASSEMBLY

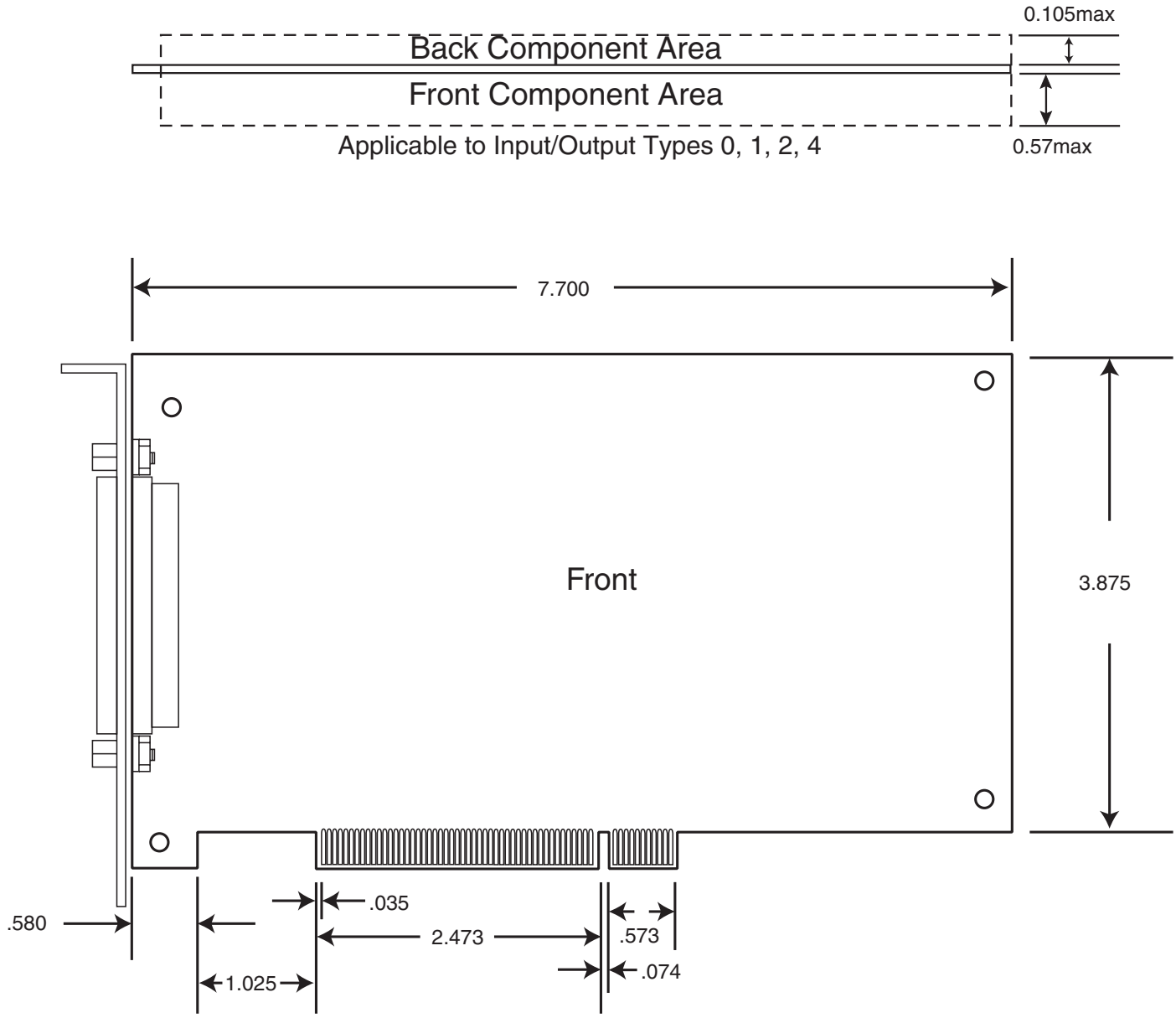


FIGURE 8. MECHANICAL OUTLINE

ORDERING INFORMATION

SB-3620 X I X -X X X X

Supplemental Process Requirements
Blank = None / N = Conformal Coat (Note 6)

Hybrid Type and Accuracy Output / Input (Notes 1 & 8):
Output (Up to 2 channels), Input RD-19230 (4-channels pre-installed)

Output Selection / Accuracy / Power	Input Selection / Accuracy
0 = No Output Converters	RD-19230 (1 min + 1 LSB)
1 = DSC-11520-305 (1 min)(2 mA)	RD-19230 (1 min + 1 LSB)
5 = DSC-11524-304 (2 min)(15 mA)	RD-19230 (1 min + 1 LSB)
B = DR-11525-305 (1 min)(2 mA)	RD-19230 (1 min + 1 LSB)

Number of Channels:
4 = Four channels (Synchro/Resolver-to-Digital) minimum configuration (Notes 3 & 4)
5 = Five channels (4 channels Synchro/Resolver-to-Digital, 1 channel Digital-to-Synchro/Resolver) (Note 5)
6 = Six channels (4 channels Synchro/Resolver-to-Digital, 2 channels Digital-to-Synchro/Resolver) (Note 5)

Temperature Range:
3 = 0° to +71°C

Oscillator Output (Note 7):
A = 1.5 VA Drive, 26 Vrms Transformer Isolation (60 mA max)
B* = 1.5 VA Drive, 115 Vrms Transformer Isolation (13 mA max)
*Discountinued Q2, 2010

Input / Output Type (Notes 1, 2):

R/D Input	D/R Output	Ref/Freq Input	Osc Op Req	Hybrid Type	BW (Note 9)
1 = 11.8 Vrms L-L Synchro	11.8 Vrms L-L Synchro	26 V (400Hz)	A	0, 1, 5	100/300
2 = 11.8 Vrms L-L Resolver	11.8 Vrms L-L Resolver	26 V (400Hz)	A	0, 5, B	100/300
3* = 90 Vrms L-L Synchro	11.8 Vrms L-L Synchro	115 V (60Hz)	B	0, 1, 5	15/45
4 = 2 Vrms	2 Vrms	4.4 V (400Hz)	A	0, B	100/300

*Discountinued Q2, 2010

Notes:
1. See Table 1 for accuracy vs. frequency.
2. The 2 V Resolver single ended option is available only with DR-11525 converters. For non-standard configurations please contact DDC or its local representative. For single-ended mode, S1, S4 on the card connector P1 are no connect. Use associated analog ground per output channel for S1, S4 resolver outputs used.
3. Without a D/R output converter there is no wrap around self-test.
4. For use only with hybrid option 0.
5. Not for use with hybrid type option 0.
6. For conformal coated boards all components will be soldered down with no sockets.
7. Oscillator output is programmable to the maximum voltage of option selection. Frequency range is programmable per the Table 1 specifications table.
8. See specification table for accuracy over frequency range.
9. Card Bandwidth: Software programmable for 100 or 300Hz.
10. The above products contain tin-lead solder.

INCLUDED ACCESSORIES:
-Mating Connector
-MN36200 Hardware/Software Manual
-Software (CD Format)

SUGGESTED MATING CONNECTORS:
-Ribbon: 3M-10168-6000EC
-Solder Back: Acon-HBW32-68K3207

STANDARD DDC PROCESSING FOR DISCRETE MODULES/PC BOARD ASSEMBLIES		
TEST	**METHOD(S)**	**CONDITION(S)**
INSPECTION / WORKMANSHIP	IPC-A-610	Class 3
ELECTRICAL TEST	DDC ATP	—

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RECORD OF CHANGE

For SB-36200IX Data Sheet

Revision	Date	Pages	Description
P	6/2010	1, & 3 thru 12	Updated Description and Features, updated Tables 1, 2, 4, 6, & 8, updated Figures 5, 7, 8, 9, & 10, textual edits, updated Ordering Information

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