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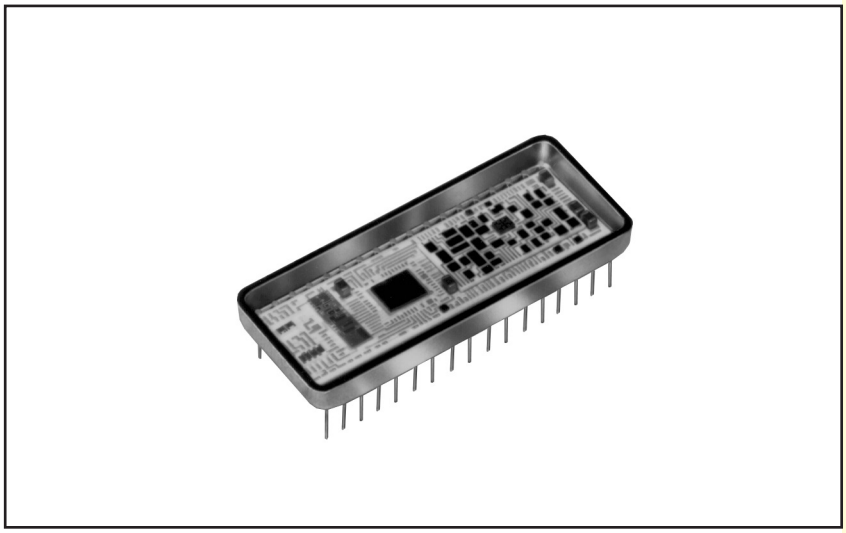
SDC-14560

SYNCHRO-TO-DIGITAL CONVERTER



FEATURES

- Programmable Resolution: 10, 12, 14 or 16 Bits
- High-Quality Velocity Output
- Eliminates Tachometer
- Accuracy to ±1.3 Arc Minutes
- Small Size
- Synchro or Resolver Input
- Synthesized Reference Eliminates 180° Lock-Up
- Control Transformer Mode

DESCRIPTION

The SDC-14560 is a series of high-reliability Synchro or Resolver-to-Digital (S/R-D) converters with user-programmable resolution of 10, 12, 14, or 16 bits. Other features of the SDC-14560 are high-quality velocity output and hermetic seal.

User-programmable resolution has been designed into the SDC-14560 to increase the capabilities of modern motion control systems. The precise positioning attained at 16-bit resolution and fast tracking of a 10-bit device are now available from one 36- pin double DIP hybrid. Velocity output (VEL) from the SDC-14560 is a ground-based voltage of 0 to ±10 VDC with a linearity to 0.7%. Output voltage is positive for an increasing angle.

The SDC-14560 series accepts broadband inputs: 360 Hz to 1 kHz, or 47 Hz to 1 kHz. The digital angle output from the SDC-14560 is a natural binary code, parallel positive logic and is TTL/CMOS compatible. Synchronization to a computer is accomplished via a converter busy (CB) and an inhibit ($\overline{\text{INH}}$) input.

APPLICATIONS

Because of its high reliability, accuracy, small size, and low power consumption, the SDC-14560 is ideal for the most stringent and severe industrial and military ground or avionics applications. All models are available with MIL-PRF-38534 processing as a standard option.

Designed with three-state output, the SDC-14560 is especially well suited for use with computer-based systems. Among the many possible applications are radar and navigation systems, fire control systems, flight instrumentation, and flight trainers or simulators.

DDC® Data Device Corporation

Data Device Corporation
105 Wilbur Place
Bohemia, New York 11716
631-567-5600 Fax: 631-567-7358
www.ddc-web.com

FOR MORE INFORMATION CONTACT:

Technical Support:
1-800-DDC-5757 ext. 7771

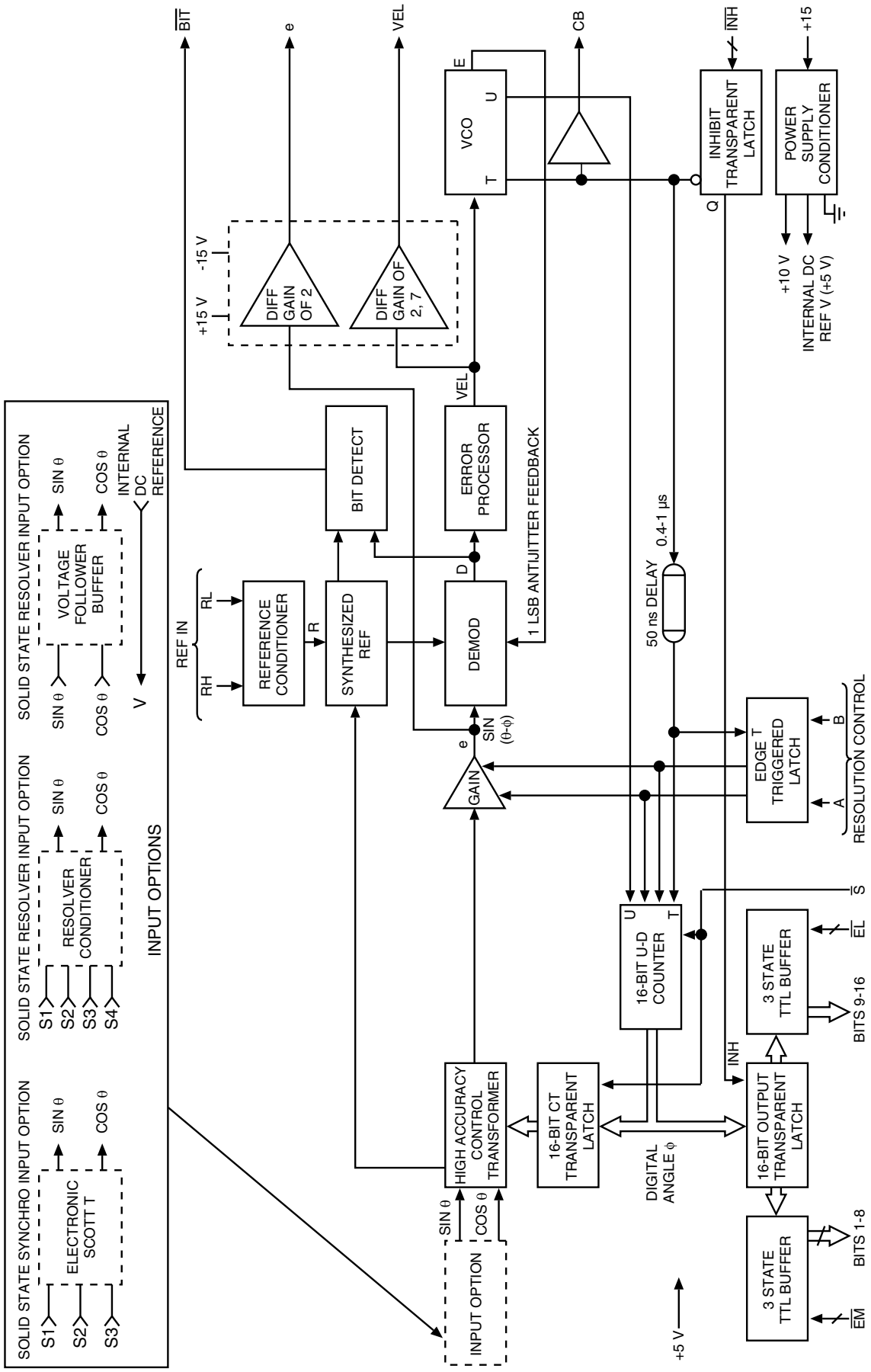


FIGURE 1. SDC-14560 BLOCK DIAGRAM

TABLE 1. SDC-14560 SPECIFICATIONS

Apply over temperature range power supply range reference frequency and amplitude ranges; 10% signal amplitude variation; and up to 10% harmonic distortion in the reference.

PARAMETER	UNIT	VALUE
RESOLUTION(1)	Bits	10, 12, 14, or 16
ACCURACY(2)	Min	±4, ±2, or ±1 +1LSB
REPEATABILITY	LSB	1 max
DIFFERENTIAL LINEARITY	LSB	1 max in the 16th bit
REFERENCE INPUT CHARACTERISTICS		
Carrier Frequency Ranges		
Nominal 400 Hz Units	Hz	360-1000
Nominal 60 Hz Units	Hz	47-1000
Voltage Range	Vrms	4-130
Input Impedance		
Single Ended	Ohm	250k min
Differential	Ohm	500k min
Common Mode Range	V	210 peak max 500 transient peak
SIGNAL INPUT CHARACTERISTICS (voltage options and minimum input impedance balanced)		
Synchro		11.8 VL-L / 90 VL-L
Zin Line to Line	Ohm	17.5k / 130k
Zin Each Line to Gnd	Ohm	11.5k / 85k
Resolver		11.8 VL-L / 26 VL-L
Zin Single Ended	Ohm	23k / 50k
Zin Differential	Ohm	46k / 100k
Zin Each Line to Gnd	Ohm	23k / 50k
Common Mode Range	V	25 max / 60 max
Direct (1.0 VL-L)		
Input Signal Type		sin and cos resolver signals referenced to converter internal DC reference V.
sin/cos Voltage Range	Vrms	1 V nominal, 1.15 V max
Max Voltage w/o Damage		15 V continuous 100 V Peak Transient
Input Impedance	Ohm	Zin > 20M//10 pF voltage follower
REFERENCE SYNTHESIZER		
±Sig/Ref Phase Shift	Deg	60 max, 45 typ
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs		Logic 0 = 0.8 V max Logic 1 = 2.0 V min Loading = 30 µA max P.U. current source to +5 V//5 pF max CMOS transient protected
Inhibit ($\overline{INH}$)		Logic 0 inhibits Data stable after 0.5 µs
Enable Bits 1 to 8 ($\overline{EM}$)		Logic 0 enables Logic 1 High Z
Enable Bits 9 to 16 ($\overline{EL}$)		Logic 0 enables Logic 1 High Z
$\overline{S}$ (Control Transformer)		Logic 0 for use as CT
Resolution Control (A & B)		B / A / Resolution: 0 / 0 / 10 bits 0 / 1 / 12 bits 1 / 0 / 14 bits 1 / 1 / 16 bits
(Unused Output Data Bits Are Set to 0)		

TABLE 1. SDC-14560 SPECIFICATIONS (CONT.)

PARAMETER	UNIT	VALUE
Output Parallel Data	bits	10, 12, 14, or 16 parallel lines; natural binary angle, positive logic
Converter Busy (CB)		0.4 to 1 µs positive pulse; leading edge initiates counter update.
$\overline{BIT}$		Logic 0 for fault.
Drive Capability		50 pF plus rated logic drive. Logic 0; 1 TTL load, 1.6 mA at 0.4 Vmax Logic 1; 10 TTL loads 0.4 mA at 2.8 V min High Z; 10 µA//5 pF max Logic 0; 100 mV max driving CMOS Logic 1; +5 V supply minus 100 mV min driving CMOS
ANALOG OUTPUTS (3)		
Velocity (VEL)		See TABLES 3 and 4
AC error (e)	mV rms	50 per LSB of error (10-bit mode) 25 per LSB of error (12-bit mode) 12.5 per LSB of error (14-bit mode) 6.3 per LSB of error (16-bit mode)
Load	kOhm	3 min
DYNAMIC CHARACTERISTICS		See TABLE 3.
POWER SUPPLY CHARACTERISTICS (Note 3)		+15 V / +5 V / -15 V
Nominal Voltage		
Voltage Range	±%	5 / 10 / 5
Max Voltage w/o Damage	V	+18 / +8 / -18
Current	mA max	25 / 10 / 15
TEMPERATURE RANGES		
Operating		
-30X	°C	0 to +70
-10X	°C	-55 to +125
Storage	°C	-65 to +150
THERMAL RESISTANCE		
Junction to Case, θ_{jc}	°C/W	8
Junction to Ambient, θ_{ja}	°C/W	20
PHYSICAL CHARACTERISTICS		
Size	in. (mm)	1.9 x 0.78 x 0.21 (48.3 x 19.8 x 5.3) 36-Pin Double Dip
Weight	oz. (g)	0.7 max (20)
TRANSFORMERS CHARACTERISTICS (See ordering information for list of Transformers. Reference Transformers are Optional for Both Solid-State and Voltage Follower Input Options.)		
400 Hz TRANSFORMERS		
Reference Transformer		
Carrier Frequency Range		360 - 1000 Hz
Voltage Range		18 - 130 V
Input Impedance		40 kΩ min
Breakdown Voltage to GND		1200 V peak

TABLE 1. SDC-14560 SPECIFICATIONS (CONTD)

PARAMETER	UNIT	VALUE
TRANSFORMERS CHARACTERISTICS (contd)		
Signal Transformer		360- 1000 Hz
Carrier Frequency Range		
Breakdown Voltage to GND		700 V peak
Minimum Input Impedances (Balanced)		Synchro $Z_{IN}(Z_{SO})$ | Resolver Z_{IN}
90 V L-L		180 Ω | 100k Ω
26 V L-L		- | 30k Ω
11.8 V L-L		20k Ω | 30k Ω
60 Hz TRANSFORMERS		
Reference Transformer		
Carrier Frequency Range		47 - 440 Hz
Input Voltage Range		80 - 138 V rms; 115 V rms nominal resistive
Input Impedance		600 kΩ min resistive
Input Common-Mode Voltage		500 V rms transformer isolated
Output Description		+R (in phase with RH-RL) and - R (in phase with RL- RH) derived from op-amps. Short Circuit proof.
Output Voltage		3.0 V nominal riding on ground reference V. Output Voltage level tracks input level.
Power Required		4 mA typ, 7 mA max from +15 V supply.
Signal Transformer		47 - 440 Hz
Carrier Frequency Range		10 - 100 V rms L-L; 90 V rms L- L nominal
Input Voltage Range		148 kΩ min L-L balanced resistive
Input Impedance		±500 V rms transformer isolated Resolver output, - sine (- S) + cosine (+C) derived from op-amps. Short circuit proof.
Input Common Mode Voltage		1.0 V rms nominal riding on ground reference V.
Output Description		Output voltage level tracks input level.
Output Voltage		4 mA typ, 7 mA max from +15 V supply.
Power Required		

Note:
(1) Pin programmable.
(2) See TABLE 6.
(3) It is recommended to place 0.1uF external bypass capacitors on the ±15V supplies for higer noise immunity on the analog Velocity and AC error (e) outputs.

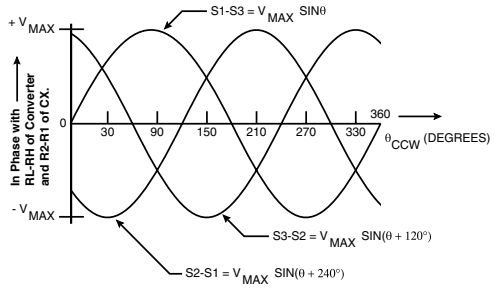
INTRODUCTION

The circuit shown in FIGURE 1, the SDC-14560 Block Diagram, consists of three main parts: the signal input; a feedback loop, whose elements are the control transformer, demodulator, error processor, VCO and up-down counter; and digital interface circuitry including various latches and buffers.

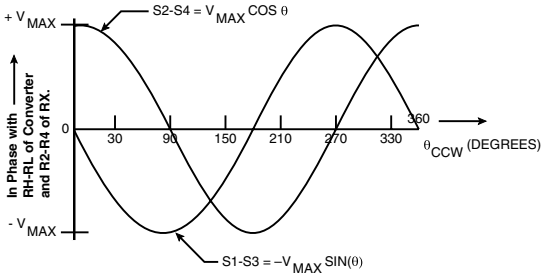
SIGNAL INPUTS

The SDC-14560 series offers three input options: synchro, resolver, and direct. In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the input terminals. Synchro signals, which are of the form $\sin\theta\cos\omega t$, $\sin(\theta + 120°)\cos\omega t$, and $\sin(\theta + 240°)\cos\omega t$ are internally converted to resolver format; $\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$. Direct inputs accept 1 Vrms inputs in resolver form, ($\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$) and are buffered prior to conversion. FIGURE 2 illustrates synchro and resolver signals as a function of the angle θ.

The solid state signal and reference inputs are true differential inputs with high AC and DC common mode rejection. *Input impedance is maintained with power off.*



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 2. SYNCHRO AND RESOLVER SIGNALS

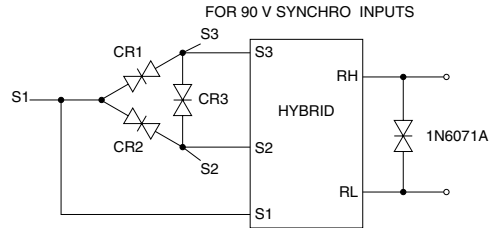
SOLID-STATE BUFFER INPUT PROTECTION - TRANSIENT VOLTAGE SUPPRESSION

The solid-state signal and reference inputs are true differential inputs with high AC and DC common rejection, so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The current AC peak +DC common mode voltage should not exceed the values in TABLE 1.

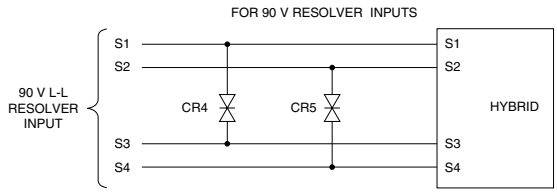
The 90 V line-to-line systems may have voltage transients which exceed the 500 V specification. These transients can destroy the thin-film input resistor network in the hybrid. Therefore, 90 V_{L-L} solid-state input modules may be protected by installing voltage suppressors as shown. Voltage transients are likely to occur whenever synchro or resolver are switched on and off. For instance, a 1000 V transient can be generated when the primary of a CX or TX driving a synchro or resolver input is opened. See FIGURE 3.

FEEDBACK LOOP

The feedback loop produces a digital angle ϕ which tracks the analog input angle θ to within the specified accuracy of the con-



CR1, CR2, and CR3 are 1N6136A, bipolar transient voltage suppressors or equivalent.



CR4 and CR5 are 1N6136A, bipolar transient voltage suppressors or equivalent.

FIGURE 3. CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS

verter. The control transformer performs the following trigonometric computation:

$$\sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

where θ is the angle representing the resolver shaft position, and ϕ is the digital angle contained in the up/down counter. The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) \rightarrow 0$, so that ϕ will represent the shaft position θ. The output of the demodulator is an analog DC level proportional to $\sin(\theta - \phi)$. The error processor receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives a Voltage-Controlled Oscillator (VCO). The VCO's clock pulses are accumulated by the up/down counter. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which make the converter a Type II tracking servo. In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without a lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

SYNTHESIZED REFERENCE

The synthesized reference section of the SDC-14560 eliminates errors caused by quadrature voltage. Due to the inductive nature of synchros and resolvers, their signals lead the reference signal (RH and RL) by about 6°. When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. In a 12- or 14-bit converter it is not necessary to compensate for the reference signal's phase shift. A 6° phase shift will, however, cause problems for the one minute accuracy converters. As shown in FIGURE 1, the converter synthesizes its own $\cos(\omega t + \alpha)$ reference signal from the $\sin\theta\cos(\omega t + \alpha)$, $\cos\theta\cos(\omega t + \alpha)$ signal inputs and from the $\cos \omega t$ reference input. The phase angle of the synthesized reference is determined by the signal input The reference input is used to choose between the +180° and -180° phases. The synthesized reference will always be exactly in phase with the signal input, and quadrature errors will therefore be eliminated. The synthesized reference circuit also eliminates the 180° false error null hangup.

Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given by the following formula:

$$\text{Error} = \text{Quad/F.S. signal} * \tan(\alpha)$$

Where: Error is in radians
Quad/F.S. signal is per unit quadrature input level.
α = signal to reference phase shift in degrees.

A typical example of the magnitude of this source of error is as follows:

Quad/F.S. signal = .001
α = 6
Error = 0.35 min ≈1 LSB in the 16th bit.

Note: Quad/F.S. is composed of static quadrature which is specified by the resolver or synchro supplier plus the speed voltage which is given by:

$$\text{Speed Voltage} = \text{rotational speed/carrier frequency}$$

Where: Speed Voltage is the per unit ratio of electrical rotational speed in RPS divided by carrier frequency in Hz.

This error is totally negligible for up to 14-bit converters. For 16-bit converters, where the highest accuracy possible is needed and where the quadrature and phase shift specifications can be higher, this source of error could be significant. The reference synthesizer circuit in the converter which derives the reference from the input signal essentially sets α to zero resulting in complete rejection of the quadrature.

DIGITAL INTERFACE

The digital interface circuitry has three main functions: to latch the output bits during an inhibit command so that the stable data can be read; to furnish both parallel and three-state data formats; and to act as a buffer between the internal CMOS logic and the external TTL logic.

In the SDC-14560, applying an inhibit command will lock the data in the transparent latch without interfering with the continuous tracking of the feedback loop. Therefore, the digital angle is always updated, and the inhibit can be applied for an arbitrary amount of time. The inhibit transparent latch and the 50 ns delay are part of the inhibit circuitry. The inhibit circuitry is described in detail in the logic input/output section.

LOGIC INPUT/OUTPUT

Logic angle outputs consist of 10, 12, 14 or 16 parallel data bits and CONVERTER BUSY (CB). All logic outputs are short-circuit proof to ground and +5 Volts. The CB output is a positive, 0.4 to 1.0 µs pulse. Data changes about 50 ns after the leading edge of the pulse because of an internal delay. Data is valid 0.2 µs after the leading edge of CB, the angle is determined by the sum of the bits at logic "1". Digital outputs are three-state and two bytes wide; bits 1-8 (MSBs) are enabled by the signal $\overline{EM}$, bits 9-16 (LSBs) are enabled by the signal $\overline{EL}$. Outputs are valid

(logic “1” or “0”) 150 ns max after setting $\overline{EM}$ or $\overline{EL}$ low, and are high impedance within 100 ns max of setting $\overline{EM}$ or $\overline{EL}$ high. Both $\overline{EM}$ and $\overline{EL}$ are internally pulled-up to +5 V at 30 µA max.

The inhibit ($\overline{INH}$) input locks the transparent latch so the bits will remain stable while data is being transferred (see FIGURE 1). The output is stable 0.5 µs after $\overline{INH}$ is driven to logic “0”, see FIGURE 4. A logic “0” at the T input latches the data, and a logic “1” applied to T will allow the bits to change. The inhibit transparent latch prevents the transmission of invalid data when there is an overlap between CB and $\overline{INH}$. While the counter is not being updated, CB is at logic “0” and the $\overline{INH}$ latch is transparent.

When CB goes to logic “1” the $\overline{INH}$ latch is locked. If CB occurs after $\overline{INH}$ has been applied, the latch will remain locked and its data will not change until CB returns to logic “0”; if $\overline{INH}$ is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50 ns delay is to prevent a race condition between CB and $\overline{INH}$ where the up-down counter begins to change as an $\overline{INH}$ is applied. Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps and generates a converter busy pulse. Output data change is initiated by the leading edge of the CB pulse, delayed by 50 ns, nominal. Valid data is available at the outputs 0.2 µs after the leading edge of CB, see FIGURE 5.

RESOLUTION CONTROL

Resolution control is via two logic inputs, A and B. The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To ensure that no race conditions exist between counting and changing the resolution, inputs A and B are latched internally on the trailing edge of CB, as illustrated in FIGURE 6.

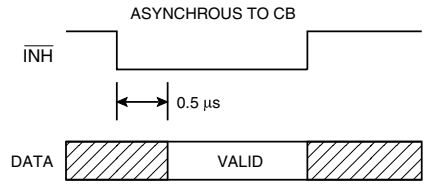


FIGURE 4. INHIBIT TIMING DIAGRAM

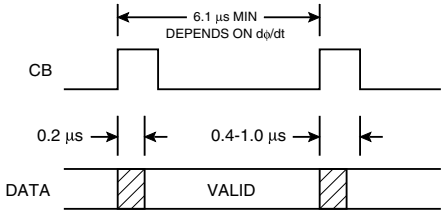


FIGURE 5. CONVERTER BUSY TIMING DIAGRAM

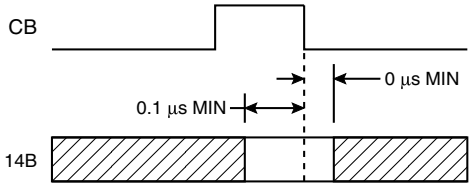


FIGURE 6. RESOLUTION CONTROL TIMING DIAGRAM

TABLE 2. DIGITAL ANGLE OUTPUTS

BIT	DEG/BIT	MIN/BIT
1 MSB	180.0	10800.0
2	90.0	5400.0
3	45.0	2700.0
4	22.5	1350.0
5	11.25	675.0
6	5.625	337.5
7	2.813	168.75
8	1.406	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14	0.0220	1.32
15	0.0110	0.66
16	0.0055	0.33

Note: $\overline{EM}$ enables the MSBs and $\overline{EL}$ enables the LSBs.

Digital angle outputs are buffered and are provided in a two byte format. The first byte always contains the MSBs (bits 1-8) and is enabled by placing $\overline{EM}$ (pin 26) to logic “0”. Depending on the user-programmed resolution, the second byte will have bits 9 through 10, 9 through 12, or 9 through 14, while operating at 10-, 12-, or 14-bit resolution, respectively. Placing $\overline{EL}$ (pin 25) to logic “0” enables the second byte, the LSBs. A logic “0” will be present on all the unused least significant bits. TABLE 2 lists the deg/bit for the digital angle outputs.

BUILT-IN-TEST

The Built-In-Test output ($\overline{BIT}$) monitors the level of error (D) from the demodulator. D represents the difference in the input and output angles and ideally should be zero; if it exceeds approximately 65 LSBs (of the selected resolution) the logic level at $\overline{BIT}$ will change from a logic 1 to logic 0. This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will also change to logic 0 for an over-velocity condition, because the converter loop cannot maintain input-output or if the converter malfunctions where it cannot maintain the loop at a null. BIT will also be set if a total Loss-of-Signal (LOS) and/or a Loss-of-Reference (LOR) occurs.

DYNAMIC PERFORMANCE

A Type II servo loop (Kv = ∞) and very high acceleration constants give the SDC-14560 superior dynamic performance, as listed in TABLE 2. If the power supply voltages are not the ±15 V DC nominal values, the specified input rates will increase or decrease in proportion to the fractional change in voltage. A Control Loop Block Diagram is shown in FIGURE 7, and an Open Loop Bode Plot is shown in FIGURE 8. The values of the transfer function coefficients are shown in TABLE 3.

An inhibit input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronously to CB is: (A) apply the inhibit, (B) wait 0.5 µs min., (C) transfer the data and (D) release the inhibit.

TABLE 3. DYNAMIC CHARACTERISTICS									
PARAMETER	UNITS	BANDWIDTH							
		400 HZ				60 HZ			
RESOLUTION	BITS	10	12	14	16	10	12	14	16
Input Frequency	Hertz	360-1000				47-1000			
Tracking Rate	RPS min	160	40	10	2.5	40	10	2.5	0.61
Bandwidth	Hertz	220	*	54	*	40	*	14	*
K_a	1/sec² nom	81.2k	*	12500	*	3k	*	780	*
A1	1/sec nom	2.0	*	0.31	*	0.29	*	0.078	*
A2	1/sec nom	40k	*	40k	*	10k	*	10k	*
A	1/sec nom	285	*	112	*	55	*	28	*
B	1/sec nom	52	*	52	*	13	*	13	*
acc-1 LSB lag	Deg/sec² nom	28.4k	7.1k	275	69	1k	264	17.2	4.3
Settling Time	ms max	160	160	300	800	350	550	1400	3400

Note: * means the same as value to the left.

As long as the converter maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as when the power is initially applied, the response will be critically damped. FIGURE 9 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to final value is a function of the small signal settling time. For Velocity output, the simple filter shown in FIGURE 10 will eliminate the one overshoot for step velocity input and will filter the carrier frequency ripple.

ANALOG OUTPUTS

The analog outputs are velocity (VEL) and AC error (e). Both outputs can swing ±10 V min. with respect to ground when the voltage level of the ±15 V power supplies are 15 V. The output level range changes proportionally if the power supply levels are not at 15 V.

Note: The SDC-14560 does not have any bypass capacitance on the ±15V power supply lines internal to the hybrid. For higher noise immunity on the analog outputs, it is highly recommended that 0.1uF capacitors are placed externally between the ±15V supply lines and ground.

The AC error, e, is proportional to the error (θ - ϕ) with a scaling of 50 mV/LSB (10-bit mode), 25 mV/LSB (12-bit mode) 12.5 mV/LSB (14-bit mode), and 6.3 mV/LSB (16-bit mode). Velocity output characteristics are listed in TABLE 4.

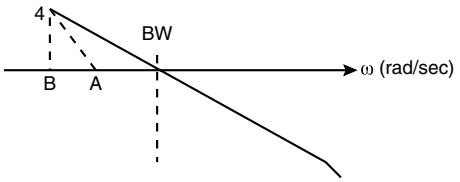


FIGURE 8. OPEN LOOP BODE PLOT

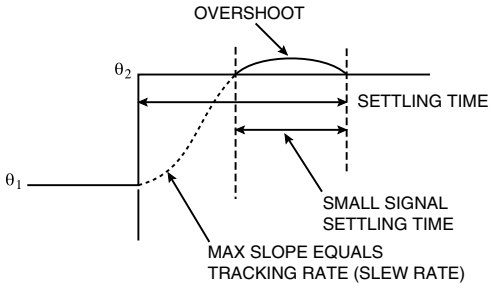


FIGURE 9. RESPONSE TO A STEP INPUT

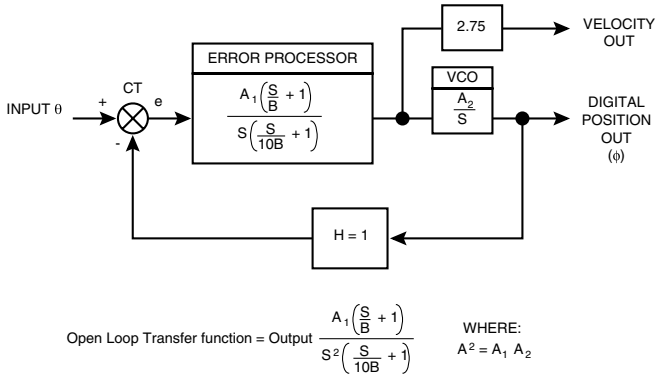


FIGURE 7. CONTROL LOOP BLOCK DIAGRAM

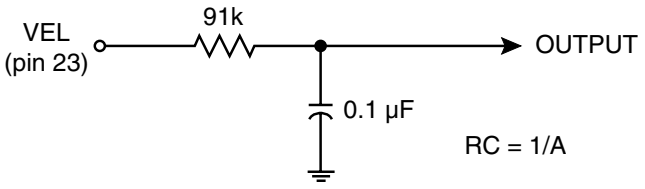


FIGURE 10. VELOCITY FILTER

VELOCITY OUTPUT

The Velocity output (VEL) from the SDC-14560 is a DC voltage proportional to angular velocity $d\theta/dt = d\phi/dt$. The velocity input is the second integrator, as shown in FIGURE 7. Its linearity is dependent solely on the linearity of the voltage controlled oscillator (VCO). Due to the highly linearized VEL output, the electromechanical tachometer can now be eliminated from motion control systems. Bandwidth (BW) and the acceleration constant (K_a) can be determined from the formulas shown:

$$BW(Hz) = BW(rad/sec)/2\pi$$
$$K_a = A^2$$

Figure 11 illustrates a typical use of an SDC-14560 connected as an S/D using the VEL output to stabilize the position loop.

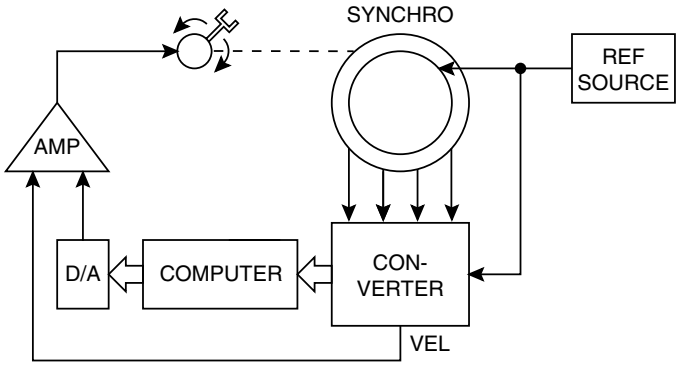


FIGURE 11. CONVERTER WITH VEL TO STABILIZE POSITION

Outputs e and VEL are not required for normal operation of the converter. V is used as an internal DC reference with the direct input option. Maximum loading on V is 40k Ohm; maximum loading for e and VEL is 3k Ohm. The velocity characteristics are shown in TABLES 4 and 5.

Output e is not closely controlled or characterized. Consult the factory for further information.

FIGURES 12, 13, and 14 are the synchro, resolver, and direct input connection diagrams, respectively.

TABLE 4. VELOCITY CHARACTERISTICS

PARAMETER	UNITS	STANDARD		HI LIN	
		TYP	MAX	TYP	MAX
Polarity		Positive for increasing angle.			
Output Voltage	V	±13	±10min	±13	±10min
Voltage Scaling	RPS/10 V	See Voltage Scaling Table 5.			
Scale Factor	%	10	15	10	15
Scale Factor TC	PPM/°C	100	200	100	200
Reversal Error	%	1	2	0.5	0.7
Reversal Error	PPM/°C	25	50	25	50
TC	% output	1	2	0.5	0.7
Linearity	PPM/°C	25	50	25	50
Linearity TC	mV	15	40	15	40
Zero Offset	µV/°C	25	50	25	50
Zero Offset TC	kOhm	-	3 min	-	3 min
Load					

TABLE 5. VELOCITY VOLTAGE SCALING

BW	RESOLUTION (values in RPS/Volt)			
	10	12	14	16
HI	16	4	1	0.25
LO	4	1	0.25	0.063

Note: If the resolution is changed while the input is changing, then the velocity output voltage and the digital output will have a transient until it settles to the new velocity scaling at a speed determined by the bandwidth. If additional information is required consult the factory.

TABLE 6. OVERALL ACCURACY (MIN.) VS. RESOLUTION

ACCURACY GRADE (MINUTES)	RESOLUTION PROGRAMMED TO:			
	10 BIT	12 BIT	14 BIT	16 BIT
±1 +1 LSB	22.1	6.3	2.3	1.3
±2 + 1 LSB	23.1	7.3	3.3	2.3
±4 + 1 LSB	25.1	9.3	5.3	4.3

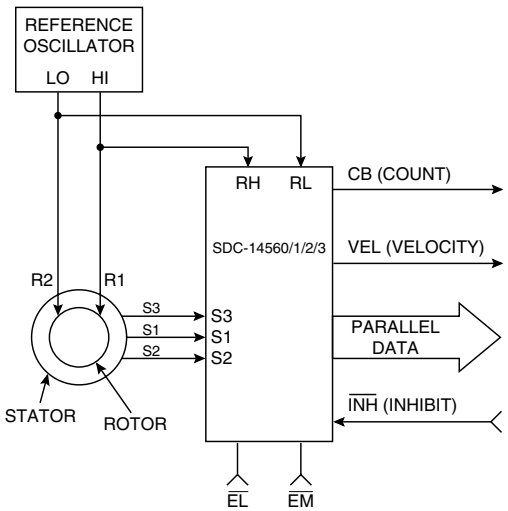


FIGURE 12. SYNCHRO INPUT CONNECTION DIAGRAM

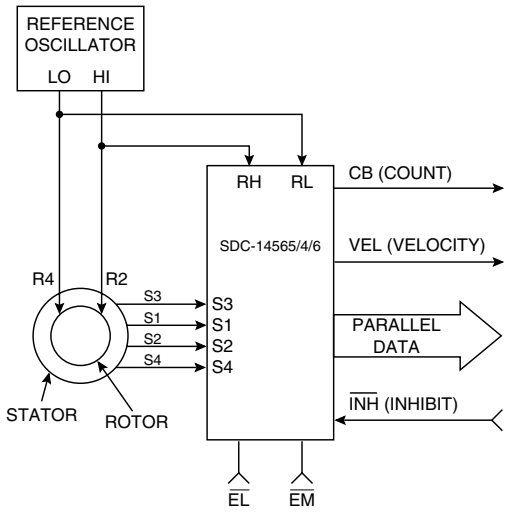


FIGURE 13. RESOLVER INPUT CONNECTION DIAGRAM

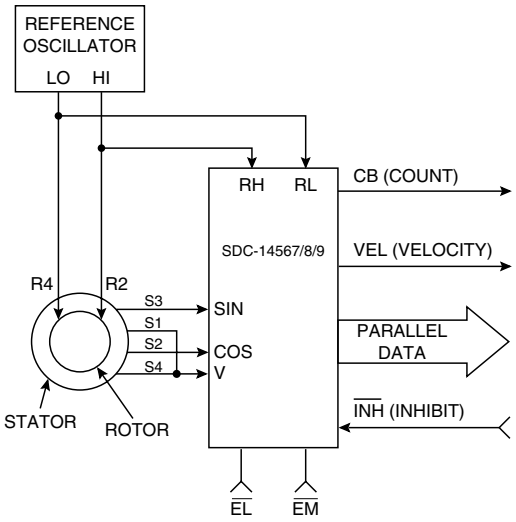


FIGURE 14. DIRECT INPUT CONNECTION DIAGRAM

CONTROL TRANSFORMER (CT) MODE

The SDC-14560 can also be used as a solid-state Control Transformer. The CT mode is used when the AC error (e) is needed to drive an external control loop. When the SDC-14560 is in CT mode, (e) is generated by the difference angle of the analog input and the digital input.

Referring to the equation below, the output of the SDC-14560 in CT mode (e) is an AC voltage (e), which varies as the sine of the difference between the analog input angle from a Synchro and a digital input angle from the user.

$$e = \sin(\theta - \phi)\cos\omega t$$

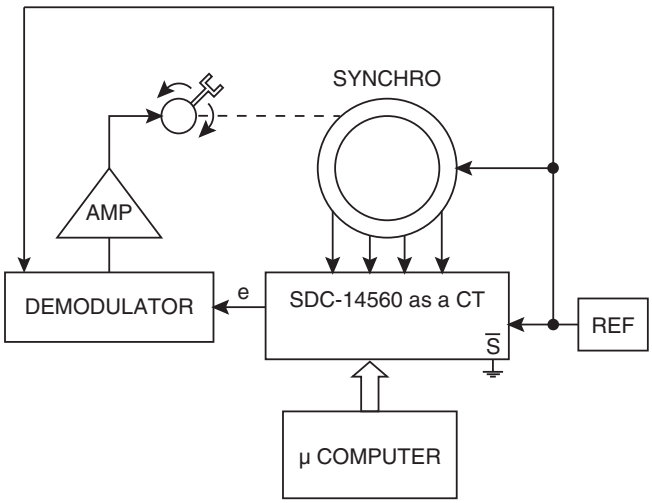


FIGURE 15. CT MODE APPLICATION

FIGURE 16 illustrates a block diagram of the SDC-14560 in CT mode. The procedure to enable this function is to disable the up-down counter by setting $\overline{S}$ (pin 30) to logic "0". This changes the digital output data lines into digital inputs.

When the SD-14560 is functioning as a CT, the digital inputs are double buffered, where $\overline{EM}$ is redefined as LM (LATCH MSBs), $\overline{EL}$ is redefined as LL (LATCH LSBs) and $\overline{INH}$ becomes $\overline{LA}$ (LATCH ALL). Data should be valid for the time any latch is enabled. See FIGURE's 18 & 19 for timing diagrams.

Control transformers are frequently used as error signal generators in closed servo loops. They are useful when digital remote control of a position servo must be accomplished.

The CT Mode can be applied in servo systems, as shown in Figure 15. In this application, changes in position are commanded by the microcomputer through signals fed to the CT. Then the generated ouput (e) goes through a demodulator and DC power amplifiers that drive the motor.

TRANSFORMERS

FIGURE 17 illustrates the Transformer Connection Diagram. These transformers are designed for the voltage follower buffer input option to the SDC-14560. However, the reference transformers may also be used with the solid-state buffer input options.

Passive transformers are considerably larger in size for 60 Hz than for 400 Hz. To minimize size, active transformers are utilized over passive devices for 60 Hz. These active 60 Hz transformers have op-amp outputs and require connection to a +15 V power supply.

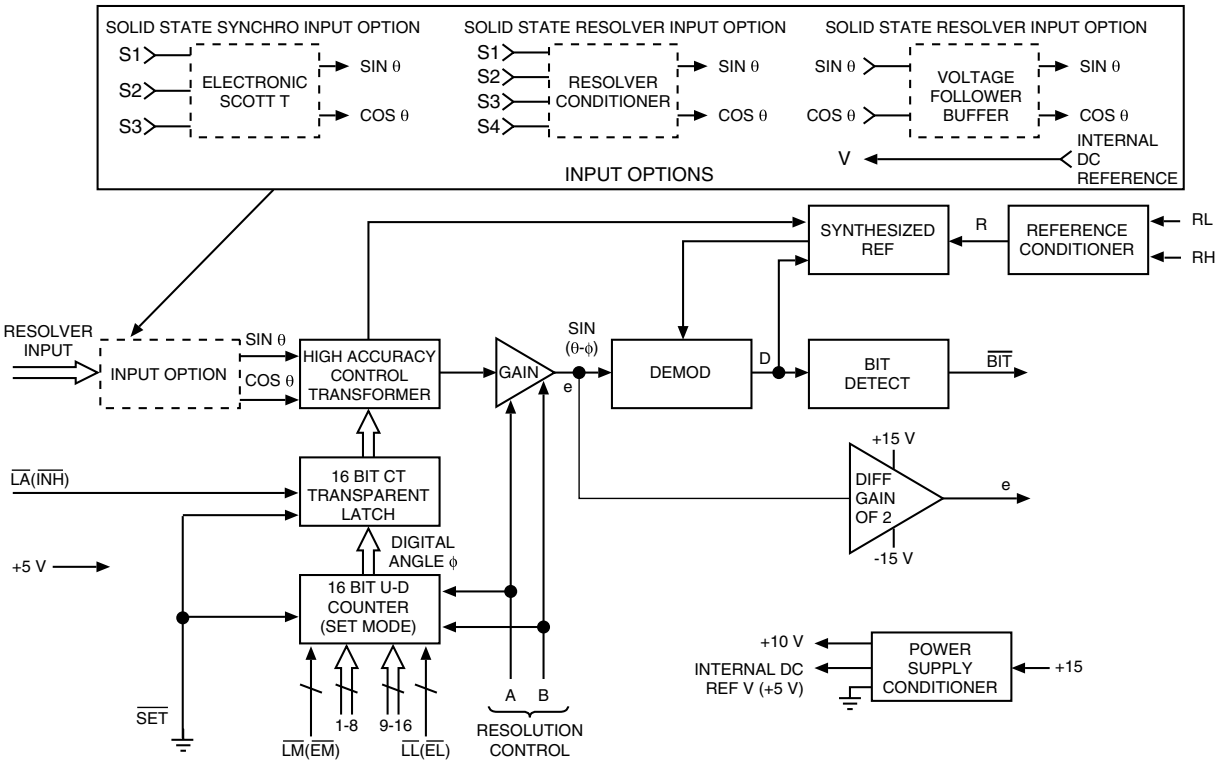


FIGURE 16. CT MODE BLOCK DIAGRAM

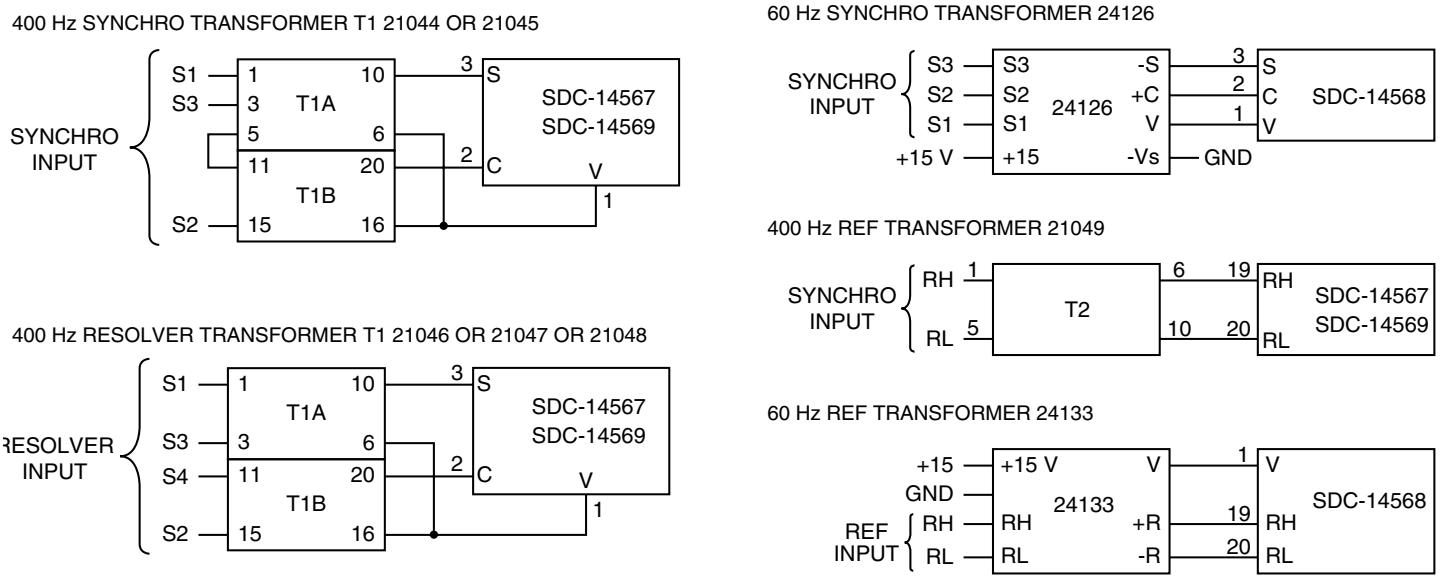


FIGURE 17. TRANSFORMER CONNECTION DIAGRAM

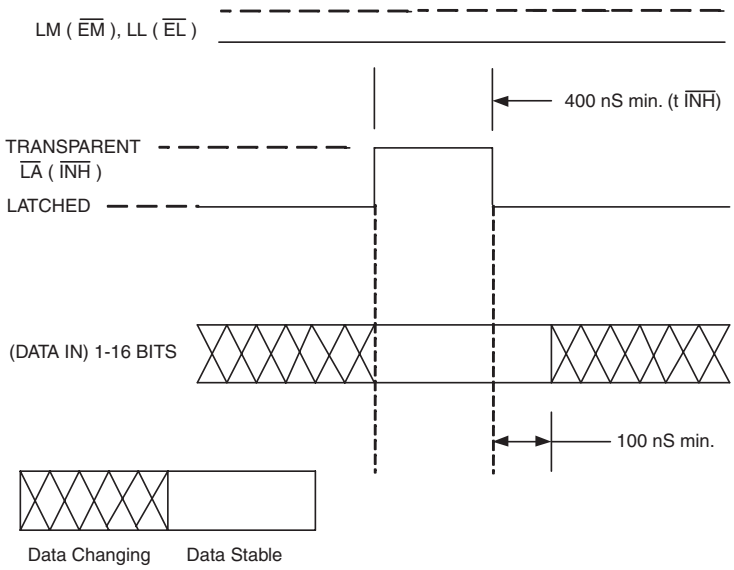


FIGURE 18. LL, LM, $\overline{LA}$ TIMING DIAGRAM (16-BIT)

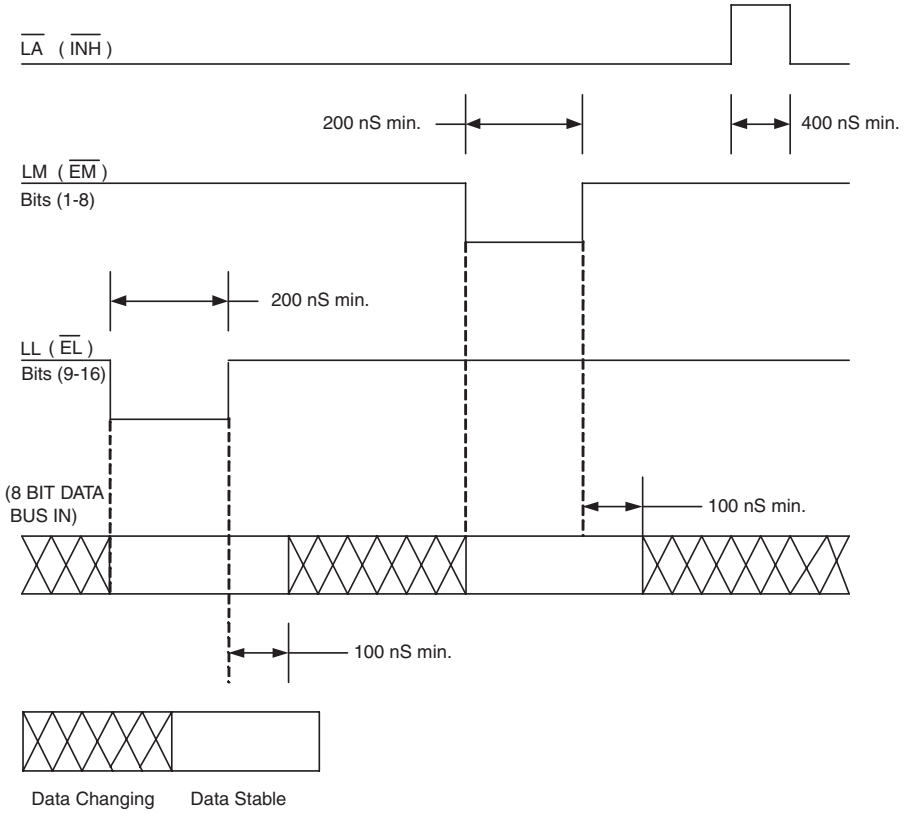
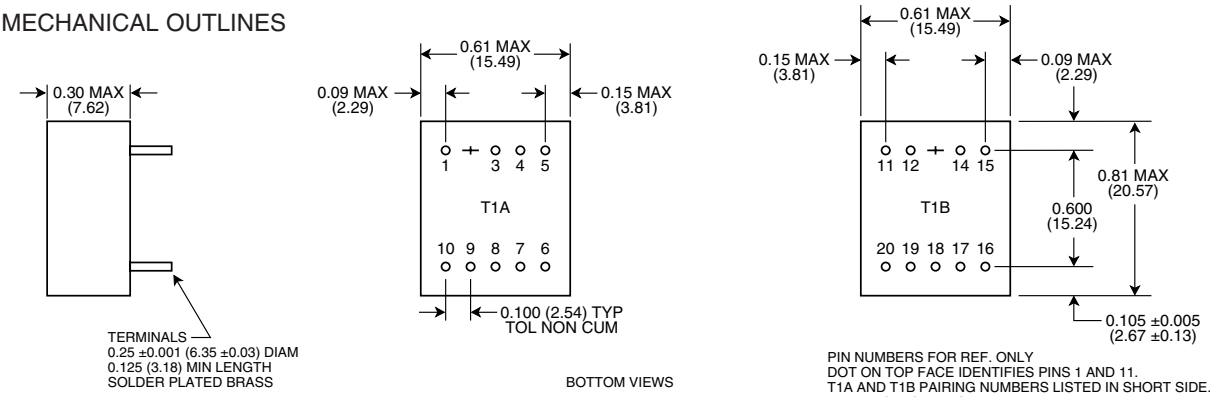


FIGURE 19. LL, LM, $\overline{LA}$ TIMING DIAGRAM (8-BIT)

These external transformers are for use with converter modules with voltage follower buffer inputs.

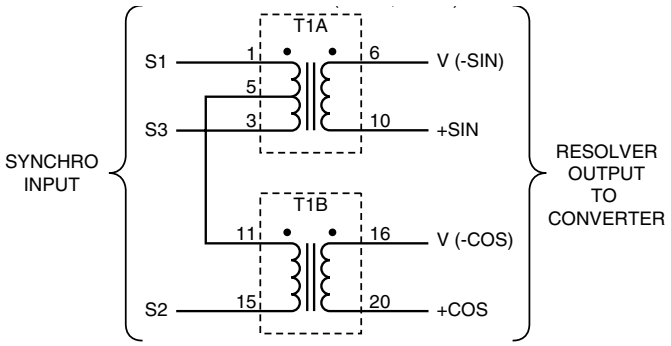
400 Hz SYNCHRO AND RESOLVER TRANSFORMER DIAGRAMS (TIA AND TIB)
EACH TRANSFORMER CONSISTS OF TWO SECTIONS, TIA AND TIB

1. MECHANICAL OUTLINES

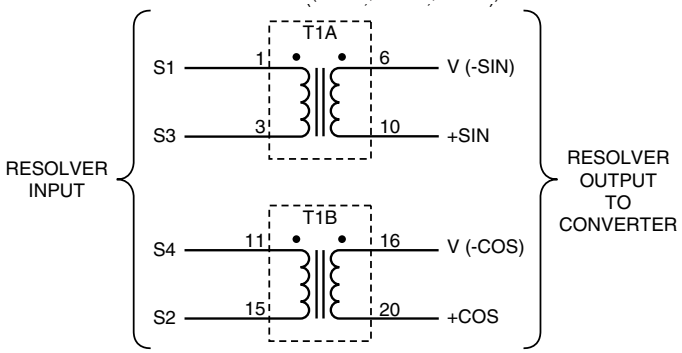


2.SCHEMATIC DIAGRAMS

A. SYNCHRO (21044, 21045)

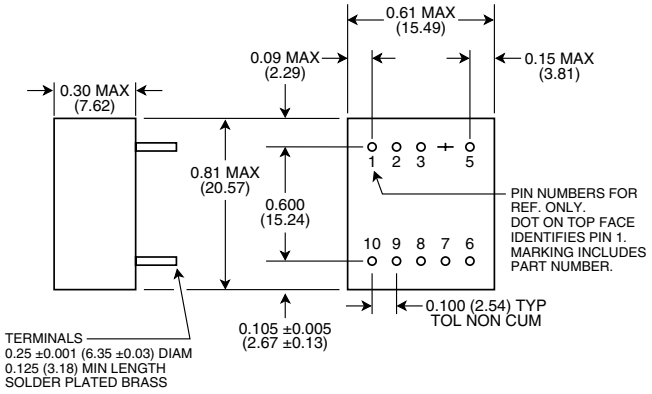


B. RESOLVER (21046, 21047, 21048)

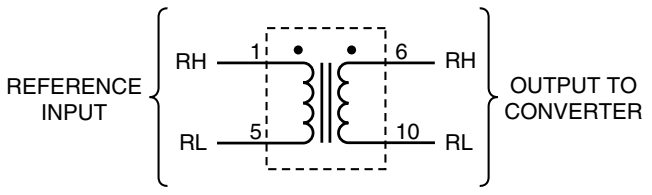


400 Hz REFERENCE TRANSFORMER DIAGRAMS (T2)

1. MECHANICAL OUTLINE



2.SCHEMATIC DIAGRAM



60 Hz SYNCHRO AND REFERENCE TRANSFORMER DIAGRAMS

The mechanical outline is the same for the synchro input transformer (24126) and the reference input transformer (24133), except for the pins. Pins for the reference transformer are shown in parenthesis ( ) below. An asterisk * indicates that the pin is omitted.

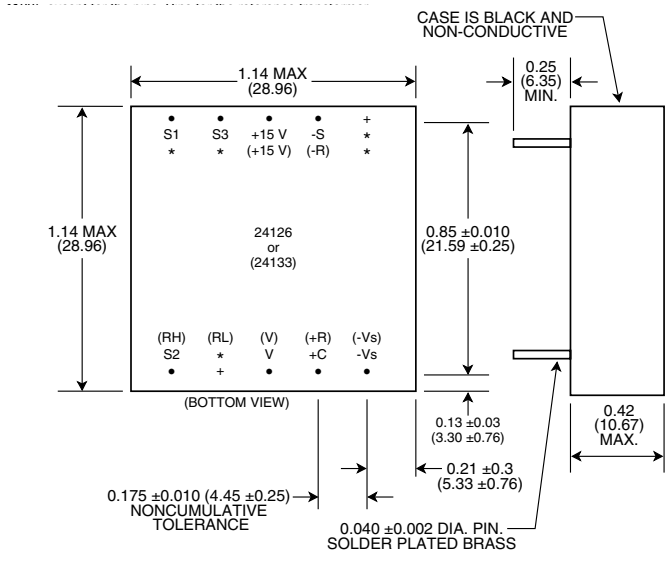
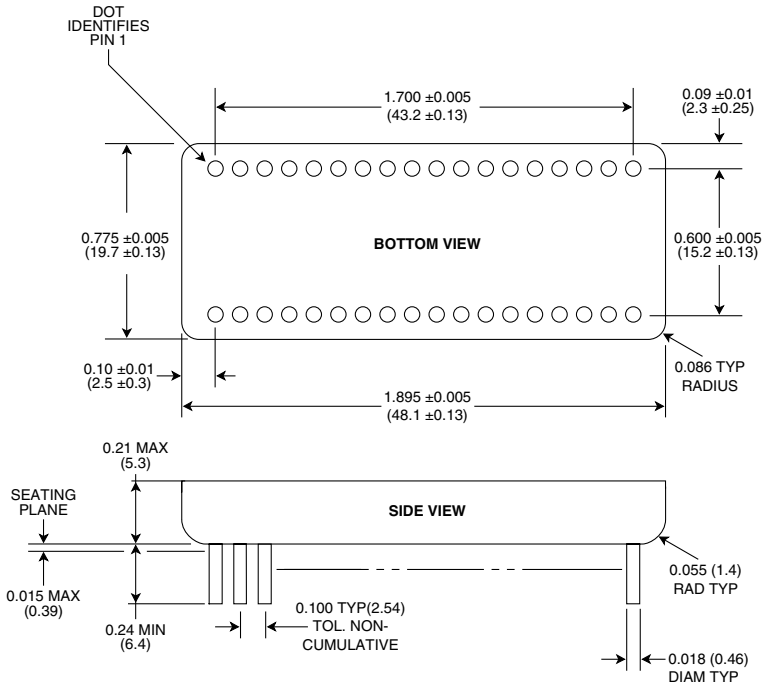


FIGURE 20. TRANSFORMER MECHANICAL OUTLINES

TABLE 7. SDC-14560 PIN CONNECTION/FUNCTIONS			
PIN NO.	**FUNCTION**	**PIN NO.**	**FUNCTION**
1	S1(R) S1(S) V(X)	36	B
2	S2(R) S2(S) +C(X)	35	A
3	S3(R) S3(S) +S(X)	34	$\overline{\text{BIT}}$
4	S4(R) - -	33	$\overline{\text{INH}}$
5	1 (MSB)	32	+15 V
6	2	31	-15 V
7	3	30	$\overline{\text{S}}$
8	4	29	GND
9	5	28	+5 V
10	6	27	e
11	7	26	$\overline{\text{EM}}$
12	8	25	$\overline{\text{EL}}$
13	9	24	CB
14	10 (LSB 10-BIT MODE)	23	VEL
15	11	22	16 (LSB 16-BIT MODE)
16	12 (LSB 12-BIT MODE)	21	15
17	13	20	RL
18	14 (LSB 14-BIT MODE)	19	RH
Note: “(R)” means resolver, “(S)” means synchro, and “(X)” means direct.			



Notes:
1. Dimensions shown are in inches (mm).
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.01(0.25) of outline dimensions.
   Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.
5. Case is electrically floating.

FIGURE 21. SDC-14560 MECHANICAL OUTLINE 36-PIN DDIP (KOVAR)

ORDERING INFORMATION

SDC-1456X-XXXX

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = 100% Pull Test
- Q = 100% Pull Test and Pre-Cap Source Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source Inspection
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source Inspection and 100% Pull Test
- Blank = None of the Above

Accuracy:
- 2 = 4 Minutes + 1 LSB
- 4 = 2 Minutes + 1 LSB
- 5 = 1 Minute + 1 LSB

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Configuration:
- 0 = 11.8 V, 400 Hz, Synchro
- 1 = 90 V, 400 Hz, Synchro
- 2 = 90 V, 60 Hz, Synchro
- 3 = 11.8 V, 400 Hz, Synchro, Hi Lin Velocity
- 4 = 26 V, 400 Hz, Resolver
- 5 = 11.8 V, 400 Hz, Resolver
- 6 = 11.8 V, 400 Hz, Resolver, Hi Lin Velocity
- 7 = 1 V, 400 Hz, Direct Resolver
- 8 = 1 V, 60 Hz, Direct Resolver
- 9 = 1 V, 400 Hz, Direct Resolver, Hi Lin Velocity

*Standard DDC Processing with burn-in and full temperature test — see table on next page.
These products contain tin-lead solder finish as applicable to solder dip requirements.

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS		
	MIL-STD-883	
TEST	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 (Note 1) 1030 (Note 2)	TABLE 1

Notes:

1. For Process Requirement "B"* (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

TRANSFORMER ORDERING INFORMATION

TYPE	FREQ.	REF. VOLTAGE	L-L VOLTAGE	PART NUMBERS	
				REF. XFMR	SIGNAL XFMR
Synchro	400 Hz	115 V	90 V	21049	21045*
Synchro	400 Hz	26 V	11.8 V	21049	21044*
Resolver	400 Hz	115 V	90 V	21049	21048*
Resolver	400 Hz	26 V	26 V	21049	21047*
Resolver	400 Hz	26 V	11.8 V	21049	21046*
Synchro†	60 Hz	115 V	90 V	24133-1 24133-3	24126-1 24126-3

* The part number for each 400 Hz synchro or resolver isolation transformer includes two separate modules as shown in the outline drawings.

† 60 Hz synchro transformers are available in two temperature ranges:
1 = -55°C to +105°C
3 = 0°C to +70°C

Notes:
(1) Signal transformers are for use with configuration options 7, 8, and 9. See Figure 17 for details.
(2) Reference transformers may be used with any configuration of the same frequency.

Please visit our Web site at **www.ddc-web.com** for the latest information.

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For Technical Support - 1-800-DDC-5757 ext. 7771

Headquarters, N.Y., U.S.A. - Tel: (631) 567-5600, Fax: (631) 567-7358
United Kingdom - Tel: +44-(0)1635-811140, Fax: +44-(0)1635-32264
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Japan - Tel: +81-(0)3-3814-7688, Fax: +81-(0)3-3814-7689
World Wide Web - http://www.ddc-web.com

RECORD OF CHANGE

For SDC-14560 Data Sheet

Revision	Date	Pages	Description
T	12/09	1, 3, 4, 6, 7, 8, 13	Resolver common mode range spec Added external bypass capacitance recommendation Added CT mode application figure Added Velocity application figure Part number correction in transformer ordering info page and added notes