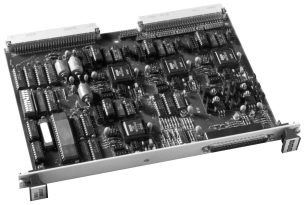


VME/VXI COMPATIBLE FOUR CHANNEL S/D-R/D CONVERTER CARD

DESCRIPTION

The SDC-36017 is a register-based "B" size VME/VXI card containing four channels of synchro/resolver-to-digital converters. Each independent channel can accept 2 V_{L-L}, 11.8 V_{L-L} or 90 V_{L-L} synchro or resolver signals. Additionally, the bandwidth and resolution of each channel can be jumper programmed.

The SDC-36017 contains a reference oscillator which is computer programmable over the frequency range of 320 to 10,200 Hz in 40 Hz steps, and the voltage range of 0 to 6.6 Vrms in 26 mVrms steps. The card can be configured to provide all I/O connections via the P2 connector for VME applications. Software drivers and libraries in "C" are available on request.

APPLICATIONS

The SDC-36017 was designed for modern high performance industrial and military control systems. Typical applications include motor control, machine tool control, robotics, aircraft control surface position and process control systems.

FEATURES

- ***Contains Four Independent Converter Channels***
- ***Accepts Synchro or Resolver Inputs***
- ***Programmable On-Card Reference Oscillator***
- ***Velocity Output Signals for Each Channel***
- ***VME/VXI Compatible "B" Size Card***
- ***Jumper Programmable Resolution and Bandwidth***
- ***VME I/O Jumper Connections for P2***

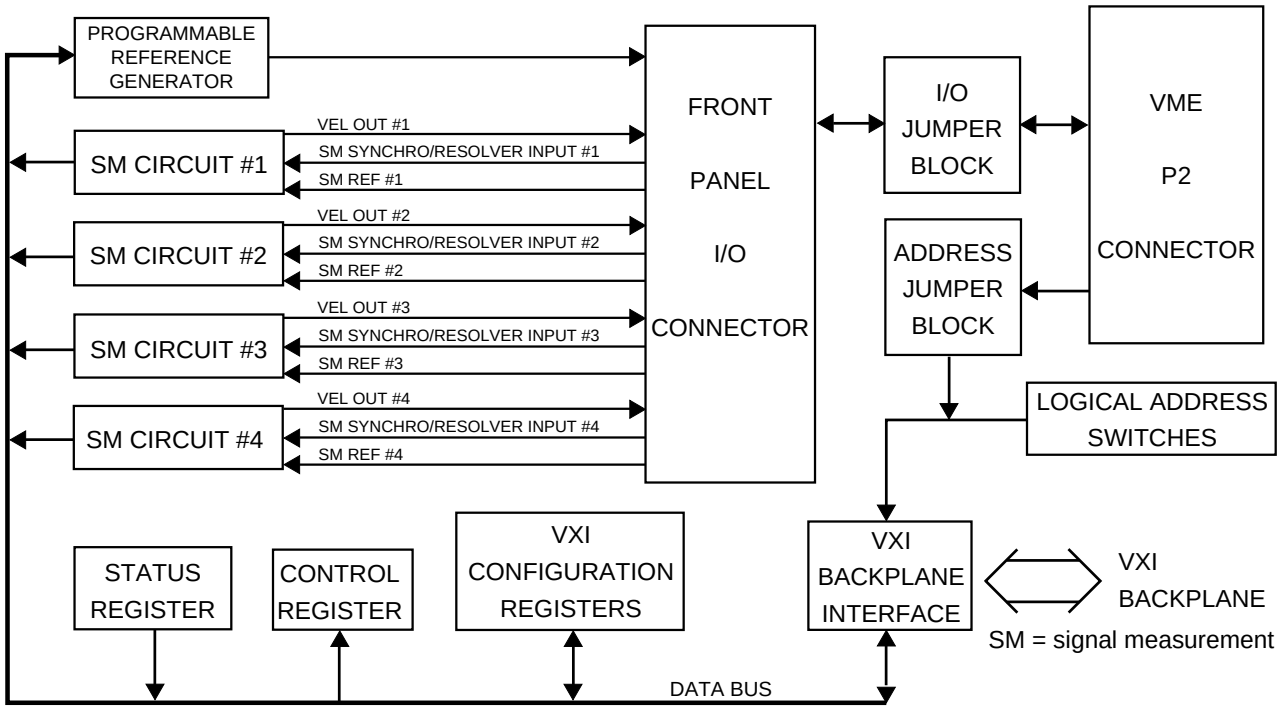


FIGURE 1. SDC-36017 BLOCK DIAGRAM

TABLE 1. SDC-36017 SPECIFICATIONS

PARAMETER	UNIT	VALUE		
POWER SUPPLY				
Current drain (with four RDC-19222 Converters)				
+5 V	mA	450 max		
+12 V	mA	150 max		
-12 V	mA	180 max		
REFERENCE INPUT VOLTAGE RANGE	Vrms	4 - 120		
PROGRAMMABLE REFERENCE OSCILLATOR		**MIN**	**MAX**	**TOL**
Voltage (26mV steps)	Vrms	0	6.6	±10
Frequency (40 Hz steps) — see Note 2	Hz	320	10.2k	±10
Current	mA		100	
Short Circuit	mA		170	
			(typ)	
DYNAMIC CHARACTERISTICS see Note 3		**LOW**		**HIGH**
Bandwidth	Hz	14		98
Maximum Tracking Rate	rps	2.1		2.5
Volts / rps		1.24		1.6
Settling Time (179° step)				
10-Bit Mode	ms	400		90
12-Bit Mode	ms	500		100
14-Bit Mode	ms	1100		180
16-Bit Mode	ms	2500		360
TEMPERATURE RANGE				
Operating	°C	0 to +50		
Storage	°C	-25 to +85		
PHYSICAL CHARACTERISTICS				
Size (“B” size VME/VXI Card)	inches (cm)	9.20 x 6.41 x 0.78 (23.37 x 16.28 x 1.99)		

Notes:
1) Specifications for the RDC-19222 are detailed in the RDC-19220 Series data sheet.
2) Although the on-board oscillator can be programmed up to 10,200 Hz, each channel’s RDC-19222 is configured for the standard internal clock rate (Rs = 30 kΩ) so the maximum reference frequency is 5,000 Hz.
3) For serial numbers below 91, the bandwidth options are low (100 Hz), high (300 Hz) or user installed. Units with serial numbers 91 or higher have a low (14 Hz), high (100 Hz) or user installed option.

TABLE 2. SDC-36017 MEMORY MAP

HEX OFFSET	READ	WRITE
00	ID REGISTER	NOT USED
02	DEVICE TYPE	NOT USED
04	STATUS REGISTER	CONTROL REGISTER
06	SM #1 ANGLE	NOT USED
08	SM #2 ANGLE	NOT USED
0A	SM #3 ANGLE	NOT USED
0C	SM #4 ANGLE	NOT USED
0E	NOT USED	NOT USED
10	EXTENDED MODEL NO.	OSCILLATOR FREQUENCY
12	NOT USED	OSCILLATOR LEVEL

INTRODUCTION

Each of the four converter channels are electrically identical but can be jumper programmed independently for different options. The heart of each channel is DDC's RDC-19222 Monolithic resolver-to-digital converter. Configuration options are determined by the external circuitry. For detailed converter operation consult the RDC-19220 Series data sheet.

Each channel of the SDC-36017 may be configured to accept 2 V_{L-L}, 11.8 V_{L-L} or 90 V_{L-L} synchro or resolver signals by selecting the associated resistor thin-film network (see Configuration sheet on page 9). The format of the input signals (i.e., synchro or resolver) is jumper programmable for each individual channel.

The resolution of each channel can be jumper programmed to be 10-, 12-, 14-, or 16-bits. Each channel also contains three jumper programmable bandwidth options which consist of Low (15 Hz), High (100 Hz), and Custom. If using the Custom option, bandwidth component values are determined (refer to the RDC-19220 data sheet) and installed onto the SDC-36017 circuit card assembly by the end user. A complete description of all the jumper settings is contained in the Configuration section of this data sheet. Note: Using the Low (15 Hz) bandwidth option is not recommended for 10- or 12-bit resolution applications.

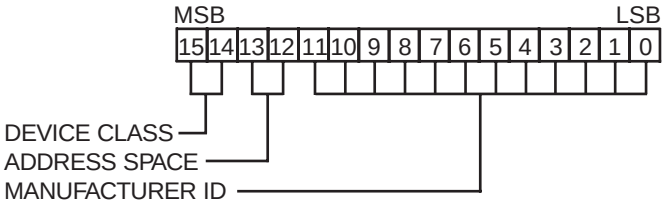
The converter for each channel can be Inhibited and/or Enabled under computer control. Refer to the Register information section for details on computer programmable features.

The reference oscillator is software programmable for both frequency and amplitude through two 8-bit binary values contained in on-card registers, and the output is transient protected. At power-turn-on the initial setting of the oscillator is undefined; any frequency and amplitude combination may be present at this time. FIGURE 1 illustrates the SDC-36017 Block Diagram.

For VME applications, the I/O signals can be connected to the VME P2 connector using terminal (jumper) blocks. Signals are always present on the Front Panel I/O Connector (J1).

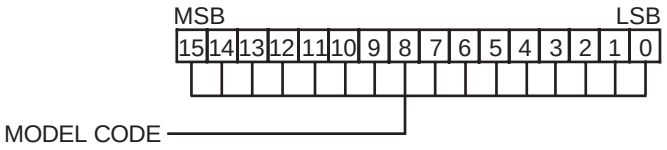
REGISTER ADDRESSING

The SDC-36017 is addressed in typical Logical Base Address and Offset fashion in accordance with the VXI BUS System Specification, and utilizes 10 of the allocated 64 registers to communicate with the VXI system. A Memory Map of these ten registers is listed in TABLE 2 and the registers are described in detail in FIGURES 2 through 9.



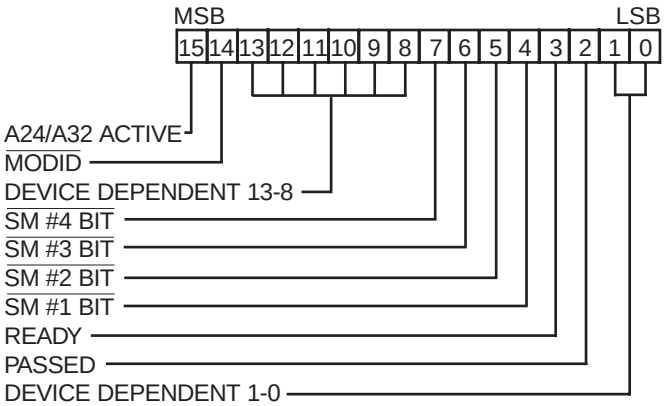
- Device Class - Both bits are set to logic 1 to define a Register-Based VXI Device.
- Address Space - Both bits are set to logic 1 to define a A16 Only VXI Device.
- Manufacturer ID - Contains DDC's manufacturer ID number. 4072 (FFE8h).

FIGURE 2. ID REGISTER BIT MAP



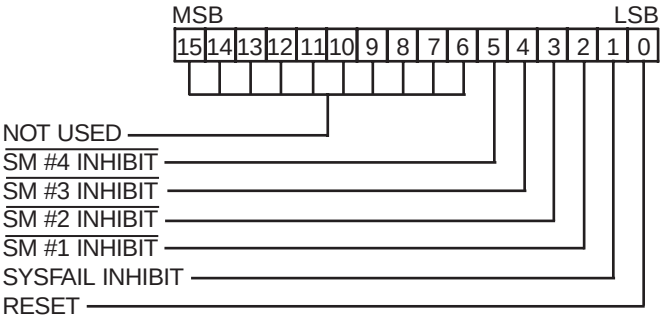
- Model Code - Contains DDC's model number (F19Ah).

FIGURE 3. DEVICE TYPE BIT MAP



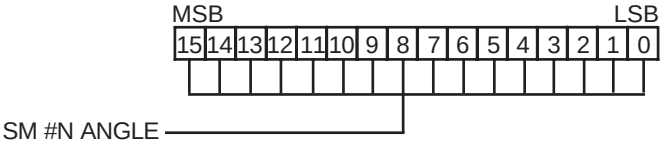
- A24/A32 Active - Device dependent bit for A16 devices permanently set to logic 1.
- MODID - The SDC-36017 does not support MODID capability so this bit is permanently set to logic 1.
- SM #N BIT - These N bits where N = 1 to 4 are normally at logic 1 state. These bits will go to logic 0 if the associated signal measurement section N is unable to track the input synchro/resolver signal. This can happen if the synchro/resolver input is rotating too fast or if the synchro/resolver input is missing altogether. This bit may also go to logic 0 momentarily if a large step input is applied to the converter.
- Ready - Permanently set to logic 1.
- Passed - Permanently set to logic 1.
- Device Dependent 1-0 - Permanently set to logic 1.

FIGURE 4. STATUS REGISTER BIT MAP



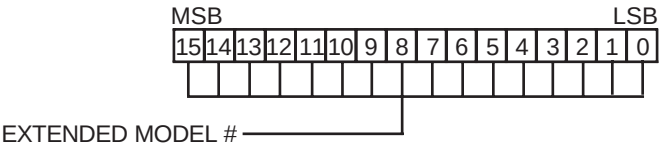
- SM #N Inhibit - A logic 0 on any of these bits (N bits, where N = 1 to 4) inhibits the associated converter. This feature can be used to synchronize the converters to external events or to each other. These bits must be set to the logic 1 for the converters to track the input synchro/resolver signals.
- Sysfail Inhibit - The Sysfail function is not used on the SDC-36017 so this bit is non-functional.
- Reset - A logic 1 on this bit will reset the SDC-36017 to the power-on state. This bit should normally be set to logic 0. Note: It is not necessary to clear this bit after setting it. The act of writing the logic 1 to the bit position initiates the card reset which internally clears the bit back to logic 0 within 125 ns.

FIGURE 5. CONTROL REGISTER BIT MAP



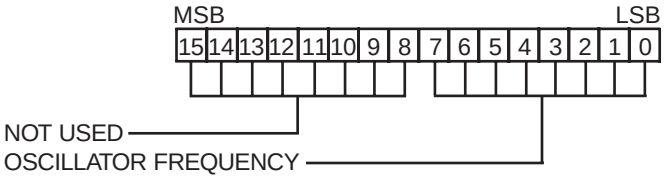
- SM #N Angle - These four registers contain the angle read by the Measurement section N, where N = 1 through 4. Bit 15 has an angular bit weight of 180°, bit 14 has a weight of 90° etc., down to bit 0 which has a weight of 0.0055° (rounded to 4 decimal places).

FIGURE 6. SM #N ANGLE REGISTER BIT MAP



- Extended Model # - contains the DDC extended model number for the card. (0001h) This number may vary for custom configurations.

FIGURE 7. EXTENDED MODEL # REGISTER BIT MAP

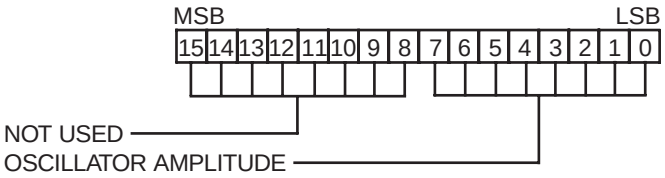


- Oscillator Frequency - The value of this byte controls the frequency of the Reference Oscillator. The frequency of the oscillator (±10%) is related to this binary value by the following formula:

  Oscillator Frequency (Hz) = binary value • 40 Hz

  Note: Programming the oscillator for frequencies less than 320 Hz will not damage the oscillator, however the operating characteristics are not guaranteed to be within ±10% of the programmed value.

FIGURE 8. OSCILLATOR FREQUENCY REGISTER BIT MAP



- Oscillator Amplitude - The value of this byte controls the amplitude of the reference oscillator. The amplitude of the oscillator (±10%) is related to this binary value by the following formula:
  Oscillator Amplitude (Vrms) = binary value • 0.026 Vrms

FIGURE 9. OSCILLATOR AMPLITUDE SET REGISTER BIT MAP

BINARY ANGLE-TO-DECIMAL ANGLE CONVERSION ALGORITHM

Conversion of the Binary Angular Data into Decimal Angular Data is simply a matter of adding all of the Decimal Angular weights for all of the binary bits which are set to logic 1. Bit weights are as listed in TABLE 3. For example if the Measurement section is programmed for 16-bit resolution and the Binary Angular measurement is:

"0 1 1 0 1 1 0 0 0 0 0 0 0 0 0 0"

The Decimal Angle will be:

(0 • 180)
\+ (1 • 90)
\+ (1 • 45)
\+ (0 • 22.5)
\+ (1 • 11.25)
\+ (1 • 5.625)
\+ (0 • all other bit weights)

Total = 151.875°

If the 16-bit binary value is treated as an binary integer (in this example, it has the hex value of 6C00h and the decimal value of 27648) the binary angle can be calculated by the following formula:

$$\text{Decimal Angle} = \frac{360 \bullet \text{Binary Integer Value}}{65536}$$

which for this example is:

$$\text{Decimal Angle} = \frac{360 \bullet 27648}{65536} = 151.875°$$

TABLE 3. DIGITAL ANGLE OUTPUT BIT WEIGHTS

BIT	DEG/BIT	MIN/BIT
1 MSB	180.0	10800.0
2	90.0	5400.0
3	45.0	2700.0
4	22.5	1350.0
5	11.25	675.0
6	5.625	337.5
7	2.813	168.75
8	1.406	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14	0.0220	1.32
15	0.0110	0.66
16	0.0055	0.33

CONFIGURATION OPTIONS

Each channel contains four jumper blocks which are used to configure the associated channel. TABLES 4 through 6 list the jumpers required for the programmable options. When using standard input voltages and bandwidths (90V, 11.8V, or 2.0V input and 15 or 100 Hz bandwidth) the card will be configured at the factory. If a custom bandwidth is used, the covers must be removed, and components installed on CA1-4 and jumpers as required.

Note: The board will be configured at the factory if the configuration sheet on Page 9 is completed and sent with the order. If no configuration sheet is received, parts may ship separately.

TABLE 4. TERMINAL BLOCK SELECTION

CHANNEL	CONFIGURATION OPTION		
	Input Mode	Resolution Mode	Bandwidth
1	TB1, TB2	TB3	TB4
2	TB5, TB6	TB7	TB8
3	TB9, TB10	TB11	TB12
4	TB13, TB14	TB15	TB16

TABLE 5. INPUT MODE SETTINGS

MODE	TERMINAL BLOCK JUMPERS			
	CHA 1=TB1 CHA 2=TB5	CHA 3 =TB9 CHA 4=TB13	CHA 1=TB1 CHA 2=TB6	CHA 3=TB10 CHA 4=TB14
SYNCHRO	7-13 10-16	8-14 11-17	9-15 12-18	1-5 2-6
RESOLVER	1- 7	2-8	3-9	1-5 2-6

TABLE 6. CHANNEL RESOLUTION SETTINGS

RESOLUTION	TERMINAL BLOCKS JUMPERS
	CHA 1 = TB3 CHA 2 = TB7 CHA 3 = TB11 CHA 4 = TB15
S/R 10 BITS	1-4 3-6
S/R 12 BITS	1-4
S/R 14 BITS	3-6
S/R 16 BITS	NONE

TABLE 7. BANDWIDTH

BANDWIDTH	JUMPER PIN NUMBERS	
	4	6
100 Hz	7	9
15 Hz	1	3
CUSTOM	N/C	N/C

Notes:
1. User selected bandwidth components should not be installed in board when factory high/low bandwidth settings are to be used.
2. It is not recommended to use the Low (15 Hz) bandwidth option for 10- or 12-bit resolutions.

TABLE 8. BANDWIDTH SPECIFICATIONS

	LOW RANGE*	HIGH RANGE				UNIT
RESOLUTION	**16**	**10**	**12**	**14**	**16**	**BITS**
BANDWIDTH	15	100				Hz
MAXIMUM TRACKING RATE	2.0	150	39	10	2.5	rps
SCALING	1.9	0.025	0.1	0.025	1.6	Volts/rps

* Low range not recommeded for 10-, 12-, or 14-bit modes.

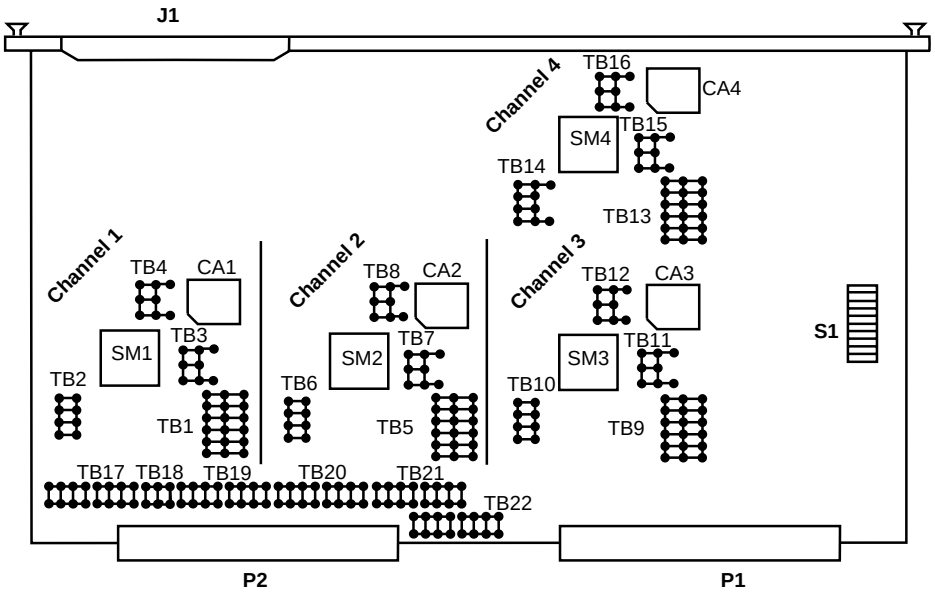


FIGURE 10. SDC-36017 COMPONENT/TERMINAL BLOCK LOCATIONS (COVER REMOVED)

LOGICAL ADDRESS SWITCH

The Logical Address switch is a 10 position DIP switch located on the SDC-36017 printed circuit card assembly. This switch is preset at the factory to the logical address of 2 as shown in TABLE 9. If desired the Logical Address can be changed to any other Logical Address from 00h to FFh using TABLE 9 as a reference.

Note 1: The SDC-36017 is a static configuration, slave device. As such it should not be assigned to Logical Addresses 0 or 255 (00h or FFh) to avoid conflicting with other VXI instrumentation. Setting the Logical Address to 1 may also cause a problem as some Slot 0 controllers utilize this address.

Note 2: Each VXI instrument is assigned a 64-byte memory area in the A16 address space. Decoding of these 64-bytes requires the use of the lower address bits (05 and lower). The Logical Address utilizes the next 8 address bits (13 to 06), and address bits 15 and 14 are defined by the VXI specification to be in the logic 1 state.

TABLE 9. LOGICAL ADDRESS SWITCH SETTINGS

SWITCH	OFF (OPEN)	ON	PRESET HEX VALUE
SW10	-	-	NOT USED
SW9	-	-	NOT USED
SW8		X	2
SW7	X		
SW6		X	
SW5		X	
SW4		X	0
SW3		X	
SW2		X	
SW1		X	

P2 HARDWIRED ADDRESS OPTION

Signals BA6-BA13 can replace the logical address switch (S1) for VME applications only. To use this option, hardwire desired low address bits (of BA6-BA13) to GND on the P2 connector and install jumpers TB81-TB93. All positions of logical address switch S1 must be set to the ON (FFh) position. See Table 11 for optional BA6-BA13 signal connections.

VXI INTERFACE CONNECTOR

The SDC-36017 requires only the P1 connector of the VXI backplane; signal connections are listed in TABLE 11.

SIGNAL I/O CONNECTOR

The converter I/O signals are brought off the SDC-36017 through a 37-pin male D-type connector (J1) mounted on the front panel. The signal connections are listed in TABLE 11. Terminal (jumper) blocks allow connection of I/O signals through the VME P2 connector; this should be used for VME applications only. Signals are always present on the Front Panel I/O Connector (J1).

TABLE 10. VXI/VME P1 CONNECTOR PIN FUNCTIONS

PIN	ROW A	ROW B	ROW C
1	D00	-	D08
2	D01	-	D09
3	D02	-	D10
4	D03	BG0IN	D11
5	D04	BG0OUT	D12
6	D05	BG1IN	D13
7	D06	BG1OUT	D14
8	D07	BG2IN	D15
9	GND	BG2OUT	GND
10	SYSCLK	BG3IN	-
11	GND	BG3OUT	BERR
12	DS1	-	SYSRESET
13	DS0	-	LWORD
14	WRITE	-	AM5
15	GND	-	-
16	DTACK	AM0	-
17	GND	AM1	-
18	AS	AM2	-
19	GND	AM3	-
20	IACK	GND	-
21	IACKIN	-	-
22	IACKOUT	-	-
23	AM4	GND	A15
24	A07	-	A14
25	A06	-	A13
26	A05	-	A12
27	A04	-	A11
28	A03	-	A10
29	A02	-	A09
30	A01	-	A08
31	-12V	-	+12V
32	+5V	+5V	+5V

TIMING REQUIREMENTS

All data to and from the SDC-36017 card is transferred through standard read/write cycles. However, the following precautions must be taken:

Relays are used to switch the measurement section synchro/resolver input line-to-line levels to allow time for them to settle out (approximately 10 ms). If an angular step input is applied to the measurement section, enough time must be allocated to allow the tracking converter to reacquire the input angular position. This could take up to 500 ms for a 180° step for 100 Hz bandwidth (2500 ms for 15 Hz bandwidth). During this time the $\overline{\text{SM BIT}}$ signal may be a logic “0.”

In order to guarantee that the measured binary angular data is stable during the computer read time, the following sequence must be followed:

1. Set the associated $\overline{\text{Inhibit}}$ bit in Control Register to logic low to latch the data.

2. Wait at least 1 µs for the Measurement section to settle out.

3. Read the angular information.

4. Return the $\overline{\text{Inhibit}}$ bit to the logic high state.

5. Process the retrieved data to calculate the angular position.

TABLE 11. SDC 36017 SIGNAL CONNECTIONS							
SYMBOL	**J1**	**JUMPERS**	**P2**	**SIGNAL**	**J1**	**JUMPERS**	**P2**
1S1	19	TB19 1-16	C16	2S1	15	TB20 1-16	C11
1S2	37	TB19 2-15	C17	2S2	33	TB20 2-15	A12
1S3	18	TB19 3-14	A17	2S3	14	TB20 3-14	C12
1S4	36	TB19 4-13	A18	2S4	32	TB20 4-13	A13
1RH	17	TB19 5-12	C18	2RH	13	TB20 5-12	C13
1RL	35	TB19 6-11	A19	2RL	31	TB20 6-11	A14
1VEL	16	TB19 7-10	C19	2VEL	12	TB20 7-10	C14
1A GND	34	TB19 8-9	A20	2A GND	30	TB20 8-9	A15
3S1	11	TB21 1-16	C6	4S1	7	TB22 1-16	A3
3S2	29	TB21 2-15	C7	4S2	25	TB22 2-15	A2
3S3	10	TB21 3-14	A7	4S3	6	TB22 3-14	A1
3S4	28	TB21 4-13	A8	4S4	24	TB22 4-13	A4
3RH	9	TB21 5-12	C8	4RH	5	TB22 5-12	C4
3RL	27	TB21 6-11	A9	4RL	23	TB22 6-11	C3
3VEL	8	TB21 7-10	C9	4VEL	4	TB22 7-10	C2
3A GND	26	TB21 8-9	A10	4A GND	22	TB22 8-9	C1
BA6		TB17 1-16	C25	PA OUT	3	TB18 1-6	C22
BA7		TB17 2-15	C26	OS GND	21	TB18 2-5	C23
BA8		TB17 3-14	C27	DIG GND	2	TB18 3-4	C24
BA9		TB17 4-13	C28				
BA10		TB17 5-12	C29				
BA11		TB17 6-11	C30				
BA12		TB17 7-10	C31				
BA13		TB17 8-9	C32				

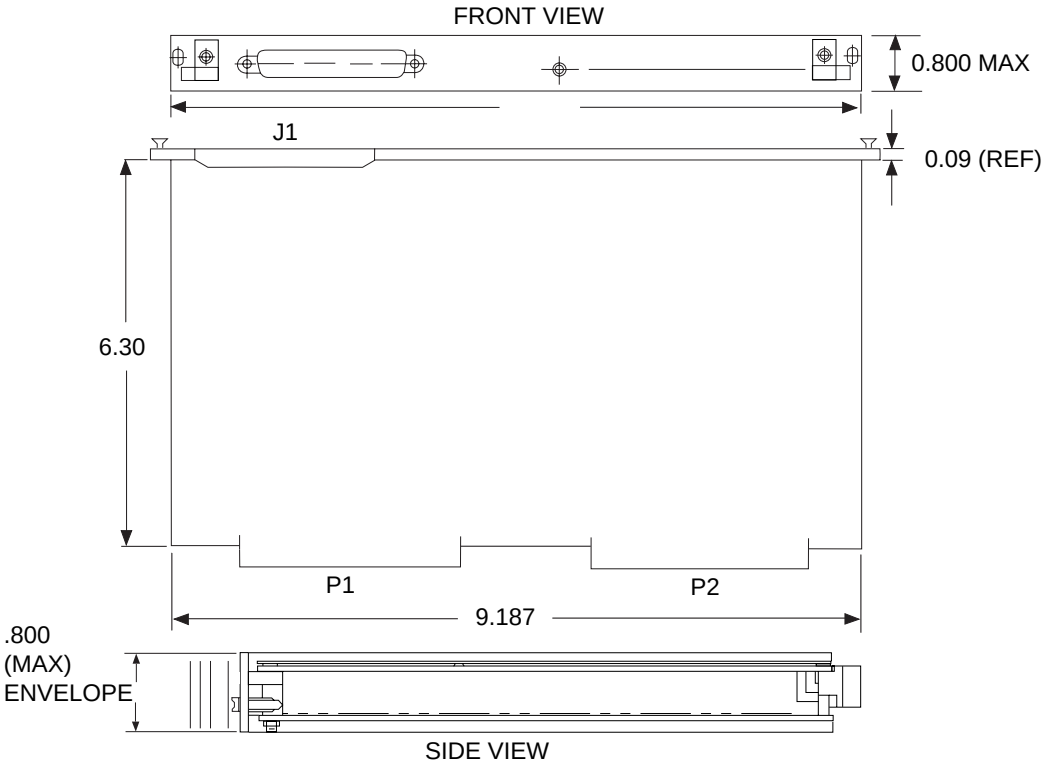


FIGURE 11. SDC-36017 MECHANICAL OUTLINE

NOTES

SDC-36017 ORDERING SUPPLEMENT

CONFIGURATION INFORMATION

COMPANY NAME:_____ **CONTACT:**_____

LOCATION:_____

PHONE #:_____ **FAX #:**_____

P.O. #:_____ **DATE:**_____

CHANNEL 1	CONVERTER P/N:	RDC19222-_____				
	RESOLUTION:	10 12	14	16 BIT		(Circle One)
	BANDWIDTH:	HIGH (100 Hz)	LOW (15 Hz)		CUSTOM(Note 2)	(Circle One)
	INPUT:	SYNCHRO	RESOLVER			(Circle One)
	L-L Volts RMS	2 V Direct	11.8		90	(Circle One)
	(Additional Components)	(DDC-55688)	(DDC-49530)		(DDC-49590)	
CHANNEL 2	CONVERTER P/N:	RDC19222-_____				
	RESOLUTION:	10 12	14	16 BIT		(Circle One)
	BANDWIDTH:	HIGH (100 Hz)	LOW (15 Hz)		CUSTOM(Note 2)	(Circle One)
	INPUT:	SYNCHRO	RESOLVER			(Circle One)
	L-L Volts RMS	2 V Direct	11.8		90	(Circle One)
	(Additional Components)	(DDC-55688)	(DDC-49530)		(DDC-49590)	
CHANNEL 3	CONVERTER P/N:	RDC19222-_____				
	RESOLUTION:	10 12	14	16 BIT		(Circle One)
	BANDWIDTH:	HIGH (100 Hz)	LOW (15 Hz)		CUSTOM(Note 2)	(Circle One)
	INPUT:	SYNCHRO	RESOLVER			(Circle One)
	L-L Volts RMS	2 V Direct	11.8		90	(Circle One)
	(Additional Components)	(DDC-55688)	(DDC-49530)		(DDC-49590)	
CHANNEL 4	CONVERTER P/N:	RDC19222-_____				
	RESOLUTION:	10 12	14	16 BIT		(Circle One)
	BANDWIDTH:	HIGH (100 Hz)	LOW (15 Hz)		CUSTOM(Note 2)	(Circle One)
	INPUT:	SYNCHRO	RESOLVER			(Circle One)
	L-L Volts RMS	2 V Direct	11.8		90	(Circle One)
	(Additional Components)	(DDC-55688)	(DDC-49530)		(DDC-49590)	

CARD S/N:_____

NOTES: 1) PLEASE COMPLETE PART NUMBERS IN THE CHANNELS YOU WISH TO POPULATE.
2) JUMPERS WILL BE INSTALLED FOR THE CUSTOM BANDWIDTH, BUT THE CUSTOMER IS STILL REQUIRED TO INSTALL CA1-4.
3) IF WE **DO NOT RECEIVE** THIS INFORMATION PARTS WILL BE SHIPPED SEPARATELY.

PLEASE RETURN THIS FORM TO SALES REP. OR FAX TO DDC.
ATTN: CUSTOMER SERVICE
TOLL FREE #: 1-800-332-5757
FAX #: (631) 567-7358

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ORDERING INFORMATION

SDC-36017 - Card Assembly (requires converters and thin-film resistor networks)

CONVERTERS:

RDC-19222 -3 0 2 - Converter

- Accuracy:
  - 2 = 4 min ±1 LSB
  - 3 = 2 min ±1 LSB
- Reliability:
  - 0 = Standard DDC Procedures
- Operating Temperature Range:
  - 3 = 0 to +70°C
- Package:
  - 2 = 44 pin J-Lead with +5 V-only option

THIN-FILM RESISTOR NETWORKS:

DDC-49530 = 11.8 V inputs
DDC-49590 = 90 V inputs
DDC-55688 = 2 V resolver

Notes:

1. The SDC-36017 is a “B” size VME/VXI card.
2. Converters and resistor networks are ordered separately as listed above. Sockets are included on the SDC-36017.
3. Mating connectors are supplied with the SDC-36017. The connectors are part of Positronic’s MD 37F 20Y00 kit. Positronic's address is: 423 N. Cambell Ave., Springfield, Missouri 65801
4. DDC reserves the right to supply ceramic packages in place of plastic packages for the converters.
5. If custom bandwidth configuration is used consult factory to receive the RDC-19220 Series External Component Selection Software, or visit our website at www.ilcddc.com to download software.

PLEASE INCLUDE THE CONFIGURATION INFORMATION WITH YOUR ORDER. SEE PAGE 9.

DDC™
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ILC DATA DEVICE CORPORATION
REGISTERED TO ISO 9001
FILE NO. A5976

C-09/99-500

PRINTED IN THE U.S.A.