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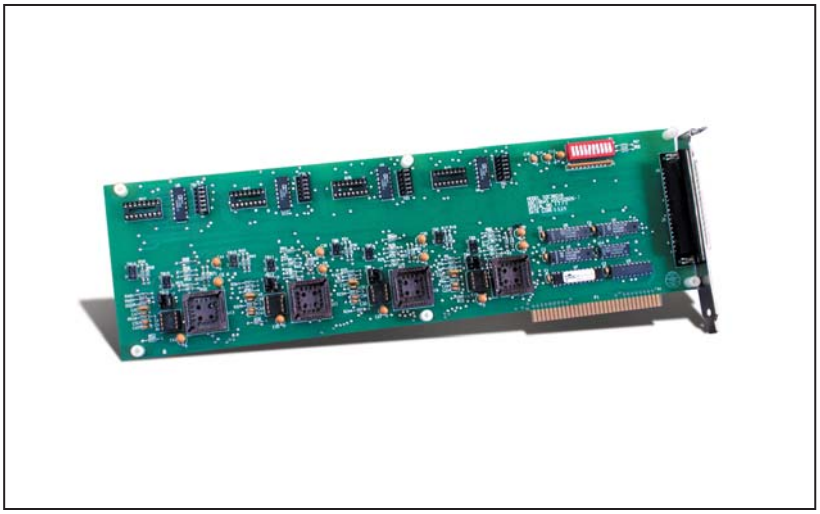
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SDC-36016

FOUR-CHANNEL S/D-R/D CONVERTER ISA CARD



DESCRIPTION

The SDC-36016 is a versatile, full-size 8-bit ISA card which can be configured for one to four channels of fully independent synchro-to-digital or resolver-to-digital conversions. For each channel, the conversion process is implemented using a DDC RDC-19222(S) 16-bit Monolithic converter.

Each converter channel can be configured for a 90V or 11.8V line-to-line differential, synchro or resolver format, or 2V single-ended input. Each channel can be programmed for 10-, 12-, 14-, or 16-bit resolution, and 100 Hz, 300 Hz, or a user-defined bandwidth.

Custom line-to-line voltages are also available. Consult the factory for information regarding this feature. Each channel provides a separate reference input signal which can be programmed to accept two voltage ranges. Also, DDC has designed the product to operate over a frequency range of 360 Hz to 5 kHz. Lower carrier frequency operation can be achieved with user-defined bandwidth.

In addition to the angular position data available, each channel provides a ±4V Velocity Signal, which is accurate to 1% of the rotational rate.

Software available on request includes drivers in “C,” Pascal, LabWindows, LabWindows/CVI, and demonstration software, which exhibits the SDC-36016’s capabilities.

APPLICATIONS

DDC designed the SDC-36016 for modern, high-performance industrial and military control systems. Typical applications include motor control, machine tool control, robotics, aircraft control surface position, and process control systems.

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Data Device Corporation
105 Wilbur Place
Bohemia, New York 11716
631-567-5600 Fax: 631-567-7358
www.ddc-web.com

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DDC on Board®

FEATURES

- One to Four Independent Converter Channels
- Accepts Synchro or Resolver Inputs
- Velocity Output Signal for Each Channel
- Low-Cost Design
- Jumper Programmable Resolution and Bandwidth
- Jumper-Programmable Reference Voltage Inputs
- Synthesized Ref Option Available

FOR MORE INFORMATION CONTACT:

Technical Support:
1-800-DDC-5757 ext. 7771

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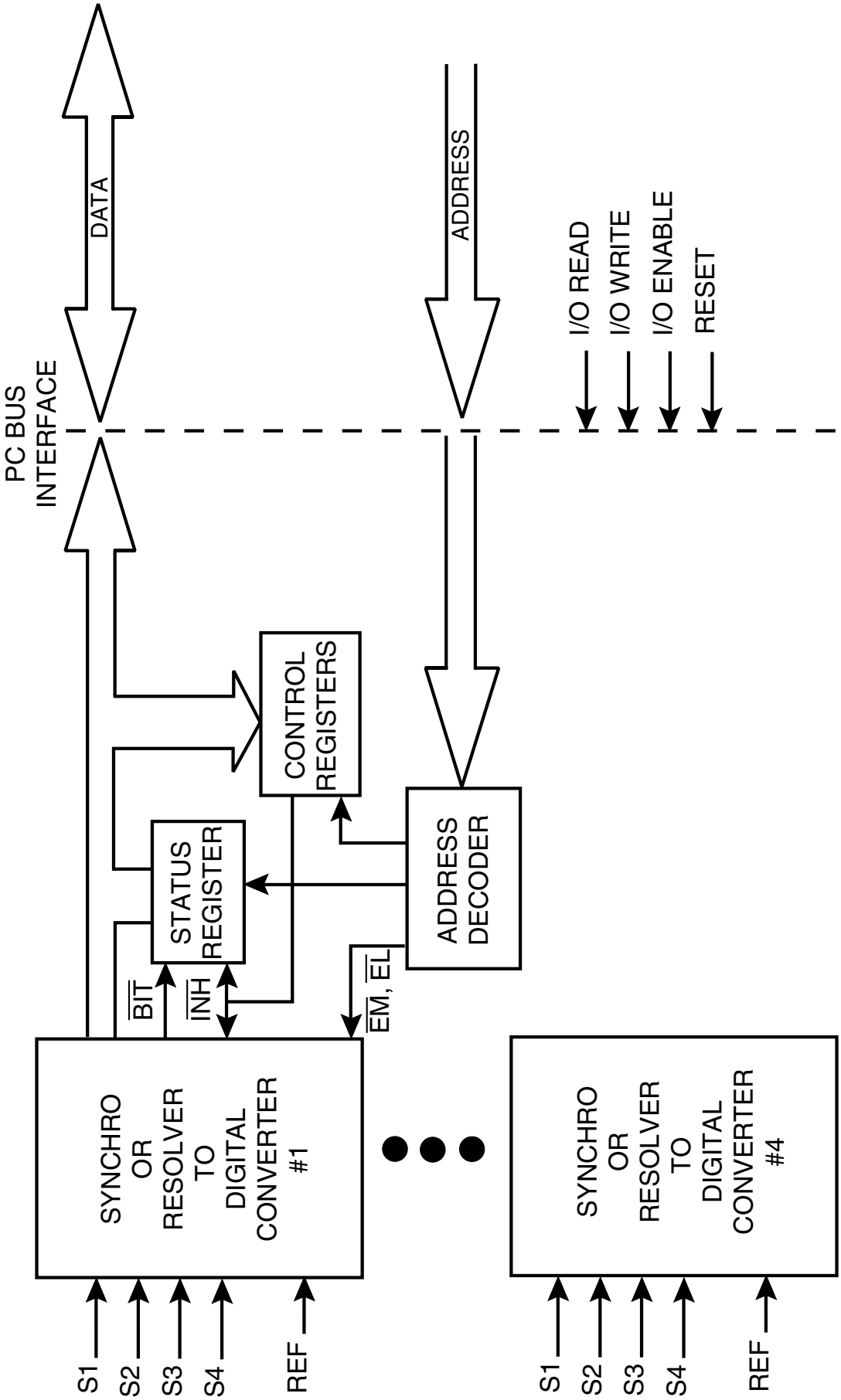


FIGURE 1. SDC-36016 BLOCK DIAGRAM

TABLE 1. SDC-36016 SPECIFICATIONS PER CHANNEL (NOTE 1)
These specs apply over the rated power supply, temperature, and reference frequency ranges; and 10% signal amplitude variation & 10% harmonic distortion. Board has an 8 bit ISA/EISA BUS compatible output.

PARAMETER	UNIT	VALUE		
Resolution	Bits	10, 12, 14, or 16		
Accuracy	Min	2 to 4 ±1 LSB (Note 3)		
Repeatability	LSB	1 max		
Differential Linearity	LSB	1 max		
Reference Input (RH,RL)				
Carrier Frequency Note 4	Hz	360-5000	Differential	
Type (Differential)		(S)	NON(S)	S or NON S
Voltage Range Note 2	V_{rms}	8-30	2-50	40-150
Input Impedance				
•Differential	Ohms	100K		500K min
•Single ended	Ohms	50K		250K min
Common-Mode Range	V_p	50		200
		100		300 transient pk
Signal Input (Voltage options and minimum input impedance, balanced)				
Synchro	**VL-L**		**11.8**	**90**
•Z_{in} line to line	Ohms		52K	195K
•Z_{in} each line to gnd	Ohms		35K	130K
Resolver	**VL-L**	**2**	**11.8**	**90**
•Z_{in} single ended	Ohms	10M min ||20pF Note 5	70K	260K
•Z_{in} differential	Ohms	N/A	140K	520K
Common-Mode Range	V	N/A	30 max	180max
Dynamic Characteristics		See Table 4		
Analog Outputs Velocity(VEL)		See Table 5		
Power Supply Characteristics				
Nominal Voltage	V	+5	+12	-12
Maximum Current	mA	200	50	50
Physical Characteristics				
Size	in.	4.2 x 13.3 x 0.77		
	(cm.)	(10.7 x 33.8 x 2.0)		

Note 1: For complete specifications on the RDC-19222 or RDC-19222(S) converters, go to the DDC Website for data sheet downloads at www.ddc-web.com.
Note 2: S refers to RDC-19222S, NON S refers to RDC-19222.
Note 3: Depending on converter accuracy grade and signal input configuration. Signal input configuration using thin-film network adds 1' of error.
Note 4: Operation with other carrier frequencies achieved with user-defined bandwidth, see FIGURE 7.
Note 5: || -in parallel with.

INTRODUCTION

Each of the four converter channels are electrically identical but can be jumper programmed independently for different options. In addition, through software, the SDC-36016 card can be configured to convert two 2-speed inputs by using one channel for each speed input (1 coarse and 1 fine input per 2-speed input). The software supplied with this card demonstrates this function.

The heart of each channel is DDC's RDC-19222(S) Monolithic Resolver-to-Digital converter (ordered separately). The circuitry external to the RDC-19222(S) provides the configuration options. For technical information on the RDC-19222(S) consult its data sheet.

Each channel of the SDC-36016 may be configured to accept 90 VL-L or 11.8 VL-L synchro or resolver signals, 2V single-ended inputs, or custom line-to-line voltages. Consult the factory regarding the custom line-to-line feature. Input levels are configured by the installation of thin-film network(s) R15, R29, R43, and R57. See FIGURE 9 and ordering information.

The synchro or resolver format for each channel is jumper programmable for the 90V and 11.8V line-to-line voltage levels. The 2V input format is resolver only (see FIGURE 8). In addition, each channel's resolution can be jumper programmed for 10-, 12-, 14-, or 16-bits.

Each channel also contains three jumper-programmable bandwidth filtering options which consist of Low (100 Hz), High (300 Hz), and User Defined. For the User Defined option, the bandwidth component values are determined by the end user, installed onto 8-pin DIP carriers and then plugged into the appropriate sockets on the SDC-36016 circuit card assembly (see FIGURES 7 and 8). A complete description of all jumper settings is detailed in this data sheet.

The angular data for each channel can be INHIBITED (frozen) or ENABLED (allowed to track the input angle) under computer control. Refer to the Register section for details on the computer programmable features. A block diagram of the SDC-36016 is shown in FIGURE 1.

SYNTHESIZED REFERENCE

The RD-19222(S) input converters contain a synthesized reference, which eliminates errors due to phase shift between the reference and the signal inputs up to 45°. Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. Due to the inductive nature of resolvers and synchros, their output signals lead the reference input signal (RH and RL). When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. Therefore this is the perfect solution to combat phase shift error to 45°.

REGISTER ADDRESSING

The SDC-36016 is addressed in typical Base Address and Offset fashion and uses ten contiguous bytes of memory in the I/O address space. A Memory Map of the ten registers is listed in TABLE 2 and the registers are described in detail in FIGURES 2 through 5.

TABLE 2. SDC-36016 MEMORY MAP

HEX OFFSET	READ	WRITE
00	Status Register	Control Register
01	Not Used	Not Used
02	Channel 1 Angle LSBs	Not Used
03	Channel 1 Angle MSBs	Not Used
04	Channel 2 Angle LSBs	Not Used
05	Channel 2 Angle MSBs	Not Used
06	Channel 3 Angle LSBs	Not Used
07	Channel 3 Angle MSBs	Not Used
08	Channel 4 Angle LSBs	Not Used
09	Channel 4 Angle MSBs	Not Used

BASE ADDRESS SWITCH

The Base Address of the SDC-36016 is preset at the factory to 300h (HEX) as listed in TABLE 3. In this configuration the SDC-36016 will occupy the address space of 300h to 309h (plus 310 through 31F which is not actually used by the SDC-36016 but enables the data bus drivers). The Base Address can be changed to any address from 000h to 3F0h in increments of 16 using TABLE 3 as a reference.

TABLE 3. SDC-36016 FACTORY SET BASE ADDRESS DIP SWITCH SETTINGS

SWITCH	OFF (OPEN)	ON	FUNCTION
SW6 SW5	X X		HEX 3
SW4 SW3 SW2 SW1		X X X X	HEX 0
— — —		— — —	HEX 0

TABLE 4. DYNAMIC CHARACTERISTICS

LOW BANDWIDTH

PARAMETER	UNITS	RESOLUTION			
		10	12	14	16
Reference Frequency Range	Hz	360-20K*	360-11K*	360-7K	360-5K
Tracking Rate (TR)	RPS min (typ)	128 (160)	32 (40)	8 (10)	2 (2.5)
Bandwidth(Closed Loop)	Hz nom	100	100	100	100
Ka	$1/sec^2$ nom	50K	50K	50K	50K
A_1	1/sec nom	1.22	1.22	1.22	1.22
A_2	1/sec nom	41K	41K	41K	41K
A	1/sec nom	222	222	222	222
B	1/sec nom	111	111	111	111
Acceleration (1 LSB lag)	deg/sec^2 nom	17.6K	4400	1100	275
Settling Time (179° step)	ms max	90	100	140	320

HIGH BANDWIDTH

PARAMETER	UNITS	RESOLUTION			
		10	12	14	16
Reference Frequency Range	Hz	1.2-20K*	1.2-11K*	1.2-7K	1.2-5K
Tracking Rate (TR)	RPS min (typ)	1152 (1440)	288 (360)	72 (80)	18 (20)
Bandwidth(Closed Loop)	Hz nom	300	300	300	300
Ka	$1/sec^2$ nom	444K	444K	444K	444K
A_1	1/sec nom	1.4	1.4	1.4	1.4
A_2	1/sec nom	323	323	323	323
A	1/sec nom	666	666	666	666
B	1/sec nom	333	333	333	333
Acceleration (1 LSB lag)	deg/sec^2 nom	156K	39K	9.8K	2.4K
Settling Time (179° step)	ms max	18	20	25	50

* Max carrier for 'S' option is 10Khz (RDC-19222S)

TRANSFER FUNCTION

The dynamic performance of the converter can be determined from its Transfer Function.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient and $A^2 = A_1A_2$

and B is the frequency of lead compensation.

$$\text{Error Processor, G1 Gain} = \frac{A_1\left(\frac{S}{B}+1\right)}{S\left(\frac{S}{10B}+1\right)}$$

$$\text{VCO, G2} = \frac{A_2}{S}$$

TABLE 5. VELOCITY CHARACTERISTICS			
PARAMETER	**UNITS**	**TYPICAL**	**MAX/MIN**
Polarity	Positive for increasing angle		
Voltage Range	±V	4.0	
Voltage Scaling (resolution dependent)	RPS/V	Typical TR (See TABLE 4) / 4	
Scale Factor Error	±%	10	20 (max.)
Scale Factor TC	PPM/°C	100	200 (max.)
Reversal Error	±%	1	2 (max.)
Linearity	% output	0.5	1 (max.)
Zero Offset	mv	5	15 (max.)
Zero Offset TC	µV/°C	15	30 (max.)
Load	kΩ		10 (min.)

JUMPER SETTINGS

Each of the four channels has an accompanying set of four jumper blocks as listed in TABLE 6. The physical configuration of each type of jumper block is identical for each function. The jumper configurations are described in the following paragraphs.

TABLE 6. CHANNEL JUMPER BLOCKS				
FUNCTION	**CH 1**	**CH 2**	**CH 3**	**CH 4**
SYN/RES	TB1	TB5	TB9	TB13
REF LEVEL	TB2	TB6	TB10	TB14
RESOLUTION	TB3	TB7	TB11	TB15
BANDWIDTH	TB4	TB8	TB12	TB16

SYNCHRO/RESOLVER JUMPER CONFIGURATION

For RESOLVER inputs the left two rows of pins in the block below are all jumpered together. For example, pins 1-7, 2-8, 3-9, 4-10, 5-11, and 6-12 are jumpered.

For SYNCHRO inputs the right two rows of pins in the block below are all jumpered together. For example, pins 7-13, 8-14, 9-15, 10-16, 11-17, and 12-18 are jumpered.

Synchro/Resolver Jumper Block Pin Configuration:

1	7	13
2	8	14
3	9	15
4	10	16
5	11	17
6	12	18

REFERENCE LEVEL JUMPER CONFIGURATION

For a 2V to 50V or 8-30V reference, jumper pins 1-4 and 3-6 are listed in block below. For a 40V to 150V reference no jumpers are required.

Note: Unused jumpers can be stored at positions 1-2, 2-3, 4-5, or 5-6. Pins 2 and 5 are unconnected.

Reference Level Jumper Block Configuration:

1	4
2	5
3	6

RESOLUTION JUMPER CONFIGURATION

For 10 Bits of resolution, connect jumpers 1-4 and 3-6.

For 12 Bits of resolution, connect jumper 1-4.

For 14 Bits of resolution, connect jumper 3-6.

For 16 Bits of resolution, no jumpers are installed.

Resolution Jumper Block Configuration:

WARNING!

To prevent personal injury always remove the I/O CONNECTOR prior to servicing the SDC-36016.

The I/O connector may contain HIGH VOLTAGES (115V and 90V).

These voltages may be present even if the power to the computer is turned OFF.

BANDWIDTH JUMPER CONFIGURATIONS

Select terminal block from TABLE 6 that corresponds to desired channel to be programmed.

For HIGH BANDWIDTH, connect jumpers 2-3 and 7-8.

For LOW BANDWIDTH, connect jumpers 1-2 and 8-9.

For USER DEFINED BANDWIDTH, no jumpers are installed.

Note: Unused jumpers can be stored at positions 1-4, 2-5, and 3-6 since pins 4, 5, and 6 are unconnected.

Bandwidth Jumper Block Configuration:

1	4	7
2	5	8
3	6	9

SIGNAL I/O CONNECTOR

The SDC-36016's I/O signals are brought off the circuit card through a 37-pin male D-type connector mounted on the rear of the circuit card. The signal connections are listed in TABLE 7.

(Note: Mating connector is supplied with the SDC-36016 card. See Note 4 of Ordering Information.)

TABLE 7. SDC-36016 "D" TYPE CONNECTOR WIRING

NAME	PIN NUMBER			
	CH 1	CH 2	CH 3	CH 4
S1	36	32	28	24
S2	17	13	9	5
S3	35	31	27	23
S4	16	12	8	4
VEL	33	29	25	21
RH	34	30	26	22
RL	15	11	7	3
GND	14	10	6	2
DIGITAL GND	37	1	19	20

BINARY ANGLE TO DECIMAL ANGLE CONVERSION ALGORITHM

The conversion of the Binary Angular Data into Decimal Angular Data is simply a matter of adding all of the Decimal Angular weights for all of the binary bits which are set to logic 1. For example, if the Measurement section is programmed for 16 bits of resolution and the binary angular measurement is

"0110110000000000"

The decimal angle will be:

(0 • 180)
+ (1 • 90)
+ (1 • 45)
+ (0 • 22.5)
+ (1 • 11.25)
+ (1 • 5.625)
+ (0 • all other bit weights)

Total = 151.875 degrees

If the 16 bit binary value is treated as an integer value, which in this case has the hex value of 6C00 and the decimal value of 27648, the angle can be calculated by the following formula:

$$\text{Decimal Angle} = \frac{360 \bullet \text{Decimal Integer Value}}{65536}$$

which for this example is:

$$\text{Decimal Angle} = \frac{360 \bullet 27648}{65536} = 151.875 \text{ degrees}$$

BIT	DESCRIPTION
07	$\overline{\text{CHANNEL 4 BIT}}$
06	$\overline{\text{CHANNEL 3 BIT}}$
05	$\overline{\text{CHANNEL 2 BIT}}$
04	$\overline{\text{CHANNEL 1 BIT}}$
03	$\overline{\text{CHANNEL 4 INHIBIT}}$
02	$\overline{\text{CHANNEL 3 INHIBIT}}$
01	$\overline{\text{CHANNEL 2 INHIBIT}}$
00	$\overline{\text{CHANNEL 1 INHIBIT}}$

$\overline{\text{CHANNEL \#N BIT}}$ - These bits, (where N = 1 to 4) are normally at the logic 1 state. These bits will go logic 0 if the associated signal measurement section N is unable to track the input synchro/resolver signal. This can happen if the S/R input is rotating too fast or if the S/R signal is missing all together. These bits may also go to logic 0 momentarily if a large angular step input signal is applied to the input of the converter.

$\overline{\text{CHANNEL \#N INHIBIT}}$ - These bits (where N = 1 to 4) provide a real time read back of the associated INHIBIT bits in the Control Register.

FIGURE 2. STATUS REGISTER BIT MAP

BIT	DESCRIPTION
07	NOT USED
06	NOT USED
05	NOT USED
04	NOT USED
03	$\overline{\text{INHIBIT CHANNEL 4}}$
02	$\overline{\text{INHIBIT CHANNEL 3}}$
01	$\overline{\text{INHIBIT CHANNEL 2}}$
00	$\overline{\text{INHIBIT CHANNEL 1}}$

INHIBIT CHANNEL #N - A logic 0 on any INHIBIT CHANNEL #N bit (where N = 1 to 4) causes the angular data associated with the channel to freeze at the angular position present during the high to low transition of the respective bit. A logic 1 releases the INHIBIT condition.

FIGURE 3. CONTROL REGISTER BIT MAP

BIT	DESCRIPTION
07 (MSB)	BIT 1 (180.000 DEG)
06	BIT 2 (90.000 DEG)
05	BIT 3 (45.000 DEG)
04	BIT 4 (22.500 DEG)
03	BIT 5 (11.250 DEG)
02	BIT 6 (5.625 DEG)
01	BIT 7 (2.813 DEG)
00	BIT 8 (1.406 DEG)

CHANNEL #N MSBs - These registers (one for each channel) provide access to the Most Significant eight bits (MSBs) of angular position data for the channel addresses in accordance with the Memory Map listed in TABLE 2.

FIGURE 4. CHANNEL MSBs REGISTER BIT MAP

BIT	DESCRIPTION
07	BIT 9 (0.703 DEG)
06	BIT 10 (0.350 DEG)
05	BIT 11 (0.175 DEG)
04	BIT 12 (0.087 DEG)
03	BIT 13 (0.044 DEG)
02	BIT 14 (0.022 DEG)
01	BIT 15 (0.011 DEG)
00 (LSB)	BIT 16 (0.005 DEG)

CHANNEL #N LSBs - These registers (one for each channel) provide access to the Least Significant eight bits (LSBs) of angular position data for the channel addresses in accordance with the Memory Map listed in TABLE 2.

FIGURE 5. CHANNEL LSBs REGISTER BIT MAP

TIMING REQUIREMENTS

Data to and from the SDC-36016 card is controlled by the computer using standard I/O Read/Write cycles, however, the following precautions must be taken.

If a step input is applied to any channel, enough time must be allocated to allow the tracking converter to reacquire the input angular position. This could take up to 500ms for a 180° step. During this time the $\overline{\text{BIT}}$ signal will be asserted. In order to guarantee that the two bytes of binary angular data are from the same instantaneous angular position the following sequence must be used:

1. Set the $\overline{\text{INHIBIT}}$ bit for the associated converter channel in the Control Word to logic 0 to latch the converter's data.

2. Read the two bytes of angular information in any sequence.

3. Return the $\overline{\text{INHIBIT}}$ bit to logic 1. This returns latch to transparent mode to resume tracking the converter's output data.

4. Process the retrieved data to calculate the angular position.

COMPUTER INTERFACE CONNECTOR

The SDC-36016 inputs place one LS-TTL load on each of the IBM data bus lines and uses one standard TTL signal level to drive the data bus. The pin number and function of the computer interface signals are listed in TABLE 8.

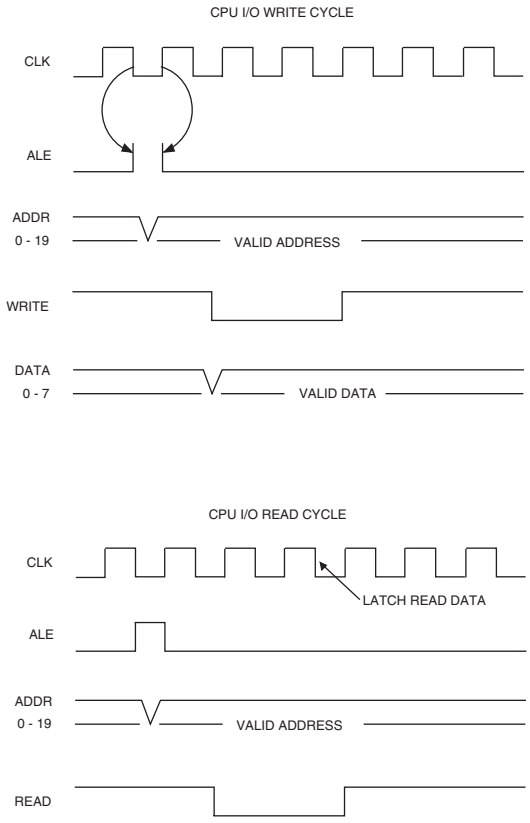


FIGURE 6. CPU I/O READ AND WRITE CYCLES

EXAMPLE: RESOLUTION -16 bits, CARRIER FREQUENCY 60Hz, BANDWIDTH - 15 Hz, MAX. TRACKING - 2 RPS. The required component values for this example are shown in their corresponding locations (See Note):

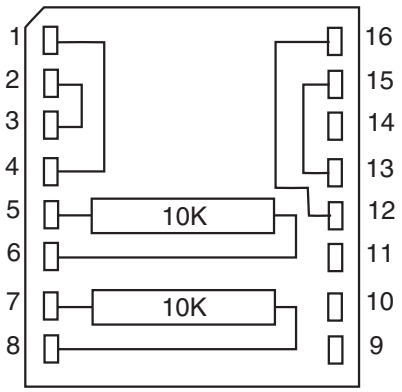


Note: This illustrates one SDC-36016 channel's component selection. The channel 1 user bandwidth carrier location corresponds to location 1 in the mechanical outline, which is located to the left of U8. Up to three other bandwidth component placement locations are available depending on the number of channels installed. The channel 2 bandwidth carrier location is labeled No. 2 (to the left of U10) in the outline. Channel 3 carrier location corresponds to location 3 and channel 4 is location 4. Locations 3 and 4 are to the left of U11 and U13 respectively.

External Component Selection Software is available from DDC to calculate values of components for user defined bandwidth. Consult factory for more information.

FIGURE 7. EXAMPLE OF USER DEFINED BANDWIDTH COMPONENTS AND THEIR PLACEMENT

2V DIRECT, RESOLVER INPUT AND WIRING *



This is the wiring for the 16-pin component carrier required when a 2V direct resolver input is used. The resistors are 10K + 5%, $^1/_8$ watt rating minimum. The user can wire their own or purchase DDC P/N 55688.

* This carrier is installed as required in locations R15 (for channel 1), R29 (for channel 2), R43 (for channel 3), and R57 (for channel 4) as shown in FIGURE 9 (Dot indicates pin 1).

FIGURE 8. WIRING DIAGRAM OF DDC P/N 55688

TABLE 8. COMPUTER INTERFACE SIGNALS					
PIN	**SIGNAL NAME**	**FUNCTION**	**PIN**	**SIGNAL NAME**	**FUNCTION**
A1	I/O CHCK	NOT USED	B1	GND	SIGNAL GROUND
A2	D7	DATA BIT 7	B2	RESET	SYSTEM RESET
A3	D6	DATA BIT 6	B3	+5V	POWER SUPPLY
A4	D5	DATA BIT 5	B4	IRQ2	NOT USED
A5	D4	DATA BIT 4	B5	-5V	NOT USED
A6	D3	DATA BIT 3	B6	DRQ2	NOT USED
A7	D2	DATA BIT 2	B7	-12V	POWER SUPPLY
A8	D1	DATA BIT 1	B8	$\overline{\text{OWS}}$	NOT USED
A9	D0	DATA BIT 0	B9	+12V	POWER SUPPLY
A10	I/O CHRDY	NOT USED	B10	GND	SIGNAL GROUND
A11	AEN	ADDRESS ENABLE	B11	$\overline{\text{MEMW}}$	NOT USED
A12	A19	NOT USED	B12	$\overline{\text{MEMR}}$	NOT USED
A13	A18	NOT USED	B13	$\overline{\text{IOW}}$	I/O WRITE
A14	A17	NOT USED	B14	$\overline{\text{IOR}}$	I/O READ
A15	A16	NOT USED	B15	$\overline{\text{DACK3}}$	NOT USED
A16	A15	NOT USED	B16	DRQ3	NOT USED
A17	A14	NOT USED	B17	$\overline{\text{DAK1}}$	NOT USED
A18	A13	NOT USED	B18	DRQ1	NOT USED
A19	A12	NOT USED	B19	DACK0	NOT USED
A20	A11	NOT USED	B20	CLK	NOT USED
A21	A10	NOT USED	B21	IRQ7	NOT USED
A22	A9	ADDRESS BIT 9	B22	IRQ6	NOT USED
A23	A8	ADDRESS BIT 8	B23	IRQ5	NOT USED
A24	A7	ADDRESS BIT 7	B24	IRQ4	NOT USED
A25	A6	ADDRESS BIT 6	B25	IRQ3	NOT USED
A26	A5	ADDRESS BIT 5	B26	$\overline{\text{DACK2}}$	NOT USED
A27	A4	ADDRESS BIT 4	B27	T/C	NOT USED
A28	A3	ADDRESS BIT 3	B28	ALE	NOT USED
A29	A2	ADDRESS BIT 2	B29	+5V	POWER SUPPLY
A30	A1	ADDRESS BIT 1	B30	OSC	NOT USED
A31	A0	ADDRESS BIT 0	B31	GND	SIGNAL GROUND

SDC-36016 ORDERING SUPPLEMENT

CONFIGURATION INFORMATION

COMPANY NAME:_____ **CONTACT:**_____

LOCATION:_____

PHONE #:_____ **FAX #:**_____

P.O. #:_____ **DATE:**_____

CHANNEL 1	CONVERTER P/N:	RDC-19222-_OR RDC-19222S-				
	RESOLUTION:	10	12	14	16 BIT	(Circle One)
	BANDWIDTH:	HIGH (300 Hz)		LOW (100 Hz)		(Circle One)
	REFERENCE:	26		115		(Circle One)
	INPUT:	SYNCHRO		RESOLVER		(Circle One)
	L-L Volts RMS	2		11.8	90	(Circle One)
	(Additional Components)	(DDC-55688)		(DDC-49530)	(DDC-49590)	
CHANNEL 2	CONVERTER P/N:	RDC-19222-_OR RDC-19222S-				
	RESOLUTION:	10	12	14	16 BIT	(Circle One)
	BANDWIDTH:	HIGH (300 Hz)		LOW (100 Hz)		(Circle One)
	REFERENCE:	26		115		(Circle One)
	INPUT:	SYNCHRO		RESOLVER		(Circle One)
	L-L Volts RMS	2		11.8	90	(Circle One)
	(Additional Components)	(DDC-55688)		(DDC-49530)	(DDC-49590)	
CHANNEL 3	CONVERTER P/N:	RDC-19222-_OR RDC-19222S-				
	RESOLUTION:	10	12	14	16 BIT	(Circle One)
	BANDWIDTH:	HIGH (300 Hz)		LOW (100 Hz)		(Circle One)
	REFERENCE:	26		115		(Circle One)
	INPUT:	SYNCHRO		RESOLVER		(Circle One)
	L-L Volts RMS	2		11.8	90	(Circle One)
	(Additional Components)	(DDC-55688)		(DDC-49530)	(DDC-49590)	
CHANNEL 4	CONVERTER P/N:	RDC-19222-_OR RDC-19222S-				
	RESOLUTION:	10	12	14	16 BIT	(Circle One)
	BANDWIDTH:	HIGH (300 Hz)		LOW (100 Hz)		(Circle One)
	REFERENCE:	26		115		(Circle One)
	INPUT:	SYNCHRO		RESOLVER		(Circle One)
	L-L Volts RMS	2		11.8	90	(Circle One)
	(Additional Components)	(DDC-55688)		(DDC-49530)	(DDC-49590)	

NOTES: 1) PLEASE COMPLETE PART NUMBERS IN THE CHANNELS YOU WISH TO POPULATE.
2) IF YOU REQUIRE A BANDWIDTH OTHER THAN LISTED ABOVE CONTACT FACTORY.
3) IF WE **DO NOT RECEIVE** THIS INFORMATION PARTS WILL BE SHIPPED SEPARATELY.

PLEASE RETURN THIS FORM TO SALES REP. OR FAX TO DDC.
ATTN: CUSTOMER SERVICE
TOLL FREE #: 1-800-332-5757
FAX #: (631) 567-7358

CC: CUSTOMER SERVICE S.O. FILE FINISHED GOODS
DISCRETE PROD CONTROL S.O.#_____

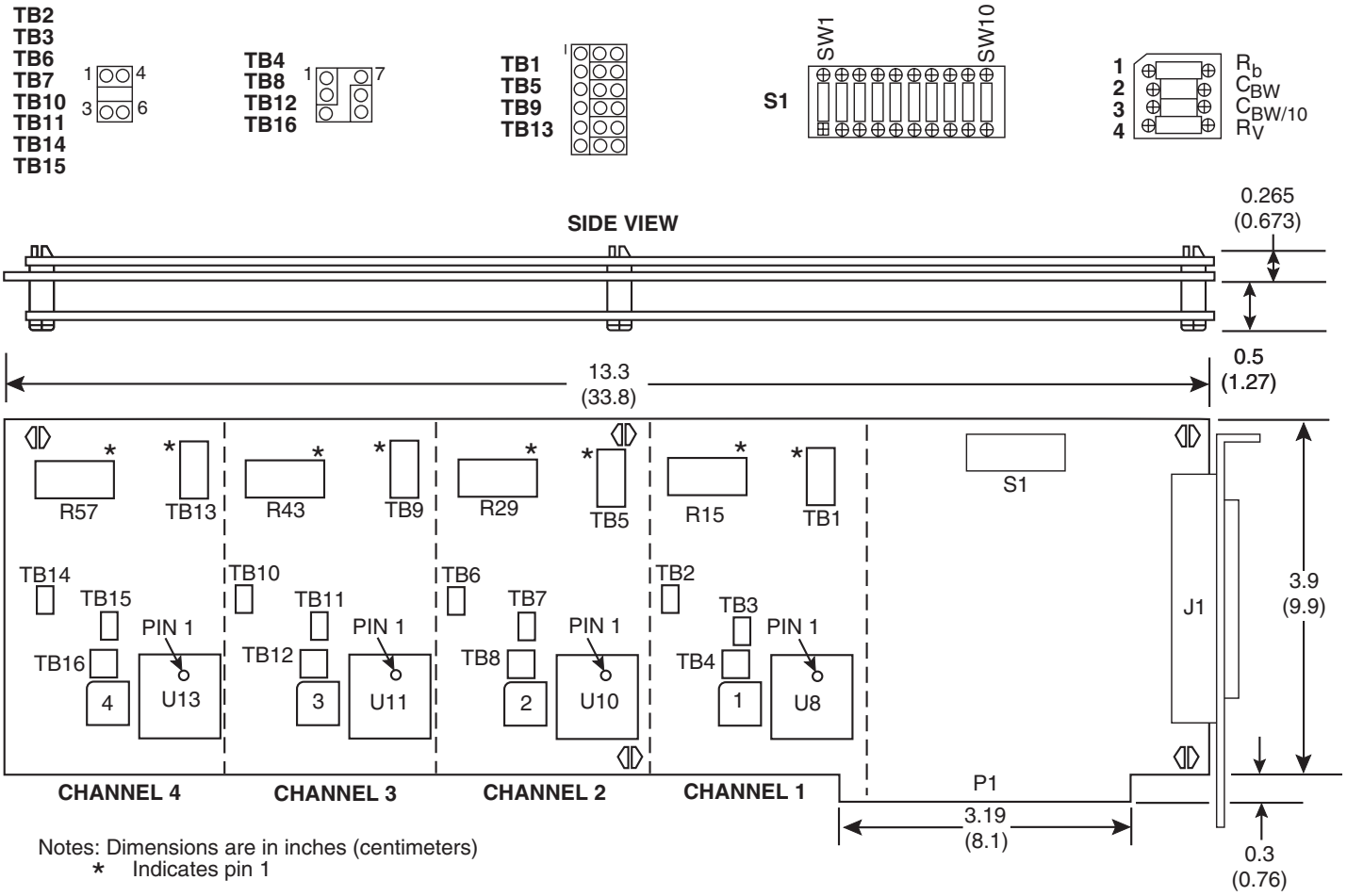


FIGURE 9. SDC-36106 MECHANICAL OUTLINE

ORDERING INFORMATION - CARD ASSEMBLY:

Card Assembly: SDC-36016

Notes:

1. The SDC-36016 is a standard, full-size 8-bit ISA card (4.2 x 13.3 x 0.77 inches)
2. Converters and thin-film networks must be ordered separately, as listed on next pages.
3. The SDC-36016 ordering supplement page of this data sheet must be completed & submitted with order for the factory to configure card with selected converters, thin film networks and required parameter settings. Without a configuration sheet all parts will ship as user installed and user must configure parameter sections.
4. Mating connectors are supplied with the SDC-36016. The connectors are part of Positronic's MD 37F 20Y00 kit. (Positronic's address is: 423 N. Campbell Ave., Springfield, Missouri, 65801, website: http://www.positronic.com)
5. Demonstration software is supplied with the card.
6. RDC converters and thin film networks are mounted in sockets and are removable.

THIN-FILM RESISTOR NETWORKS: (Data sheets on thin film networks is available for download from the DDC Website)

(Operating temperature range: -55 to +125°C)

DDC-49530 = 11.8V inputs

DDC-49590 = 90V inputs

DDC-55688-1 = 2V resolver

ORDERING INFORMATION FOR NON S REFERENCE CONVERTER:

RDC-1922X-XXX (Ceramic Package)

Accuracy:
2 = 4 minutes ± 1 LSB

Process Requirements:
0 = Standard DDC Processing, no Burn-In*
1 = MIL-PRF-38534 Compliant
2. = Standard DDC Processing with Burn-In

Temperature Grade:
1 = -55 to +125°Ct

Package:
2 = 44-Pin J-Lead**

ORDERING INFORMATION FOR NON S REFERENCE CONVERTER

RDC-19222 - XXX **(Plastic Package: 44-pin J-Lead)**

Accuracy:
2 = 4 minutes + 1 LSB
3 = 2 minutes + 1 LSB

Process Requirements:
0 = No Burn-In

Temperature Grade:
2 = -40 to +85°C
3 = 0 to +70°C
A = -40 to +125°C

ORDERING INFORMATION FOR SYNTHESIZED REFERENCE CONVERTER

RDC-19222S - XXX **(Plastic Package: 44-pin J-Lead)**

Accuracy:
2 = 4 minutes + 1 LSB
3 = 2 minutes + 1 LSB
5 = 1 minute + 1 LSB

Process Requirements:
0 = No Burn-In

Temperature Grade:
2 = -40 to +85°C
3 = 0 to +70°C

RDC-1922XS - XXX **(Ceramic Package)**

Accuracy:
3 = 2 minutes + 1 LSB

Process Requirements:
0 = Standard DDC Processing, without Burn-In
1 = MIL-PRF-38534 Compliant
2 = Standard DDC Processing, with Burn-In

Temperature Grade / Data Requirements:
1 = -55 to +1

Package:
2 = 44-Pin J-Lead

These products contain tin-lead solder.

STANDARD DDC PROCESSING FOR PLASTIC MONOLITHIC PRODUCTS		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION / WORKMANSHIP	2017	—
ELECTRICAL TEST	DDC ATP	—

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 (note 1), 1030 (note 2)	TABLE 1

Notes:
1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

The information in this data sheet is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith.
Specifications are subject to change without notice.

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105 Wilbur Place, Bohemia, New York, U.S.A. 11716-2426

For Technical Support - 1-800-DDC-5757 ext. 7771

Headquarters, N.Y., U.S.A. - Tel: (631) 567-5600, Fax: (631) 567-7358
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