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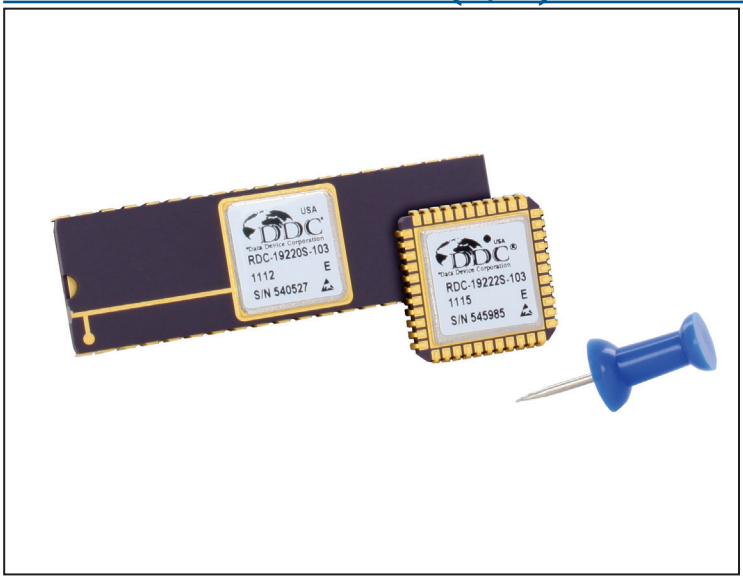
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RDC-19220S/2S/8S

16-BIT MONOLITHIC TRACKING RESOLVER-TO-DIGITAL (R/D) CONVERTER



DESCRIPTION

The 19220S/2S/8S is a low-cost, versatile, state-of-the-art 16-bit monolithic Resolver-to-Digital (R/D) converter. This single chip converter offers programmable features such as resolution, bandwidth and velocity output scaling.

Resolution programming allows selection of 10, 12, 14, or 16 bits, with accuracies to 2 minutes. This feature combines the high tracking rate of a 10-bit converter with the precision and low-speed velocity resolution of a 16-bit converter in one package.

The internal Synthesized Reference section eliminates errors due to quadrature voltage. Previously, a 6 degree phase shift caused problems for a 16-bit converter. The synthesized reference capability ensures operation with a phase shift up to 45 degrees. The velocity output (VEL) from the 19220S/2S/8S, which can be used to replace a tachometer, is a 4 V signal referenced to ground. The full-scale value of VEL is set by the user with a single resistor.

The 19220S/2S/8S converter is available with an operating temperature ranges of -55° to +125°C. Class K available through RDC-19228S ordering information

APPLICATIONS

The low cost, small size, high accuracy, and versatile performance of the 19220S/2S/8S converter makes it ideal for use in modern high performance motion control systems. Typical applications include motor control, radar antenna positioning, machine tool control, robotics, and process control. MIL-PRF-38534 processing is also available.

FEATURES

- Accuracy up to 2 Arc Minutes
- Frequency Range of 47 to 10KHz
- Internal Synthesized Reference
- +5 Volt Only Option (19222S/8S)
- Programmable:
  - Resolution: 10-, 12-, 14-, or 16-Bit
  - Bandwidth
  - Tracking
- Differential Resolver Input Mode
- Velocity Output Eliminates Tachometer
- Built-In-Test (BIT) Output, No 180° Hang-Up
- -55° to +125°C Operating Temperature Available
- Programmable for LVDT Input
- Lead Free (RoHS) Option
- Maximize Your Risk Mitigation: Class K Available Where Failure is Not Acceptable and Repair is Not Feasible
- Space Applications (RDC-19228S)
  - Class K Option
  - Rad Report to Specific Lot Build

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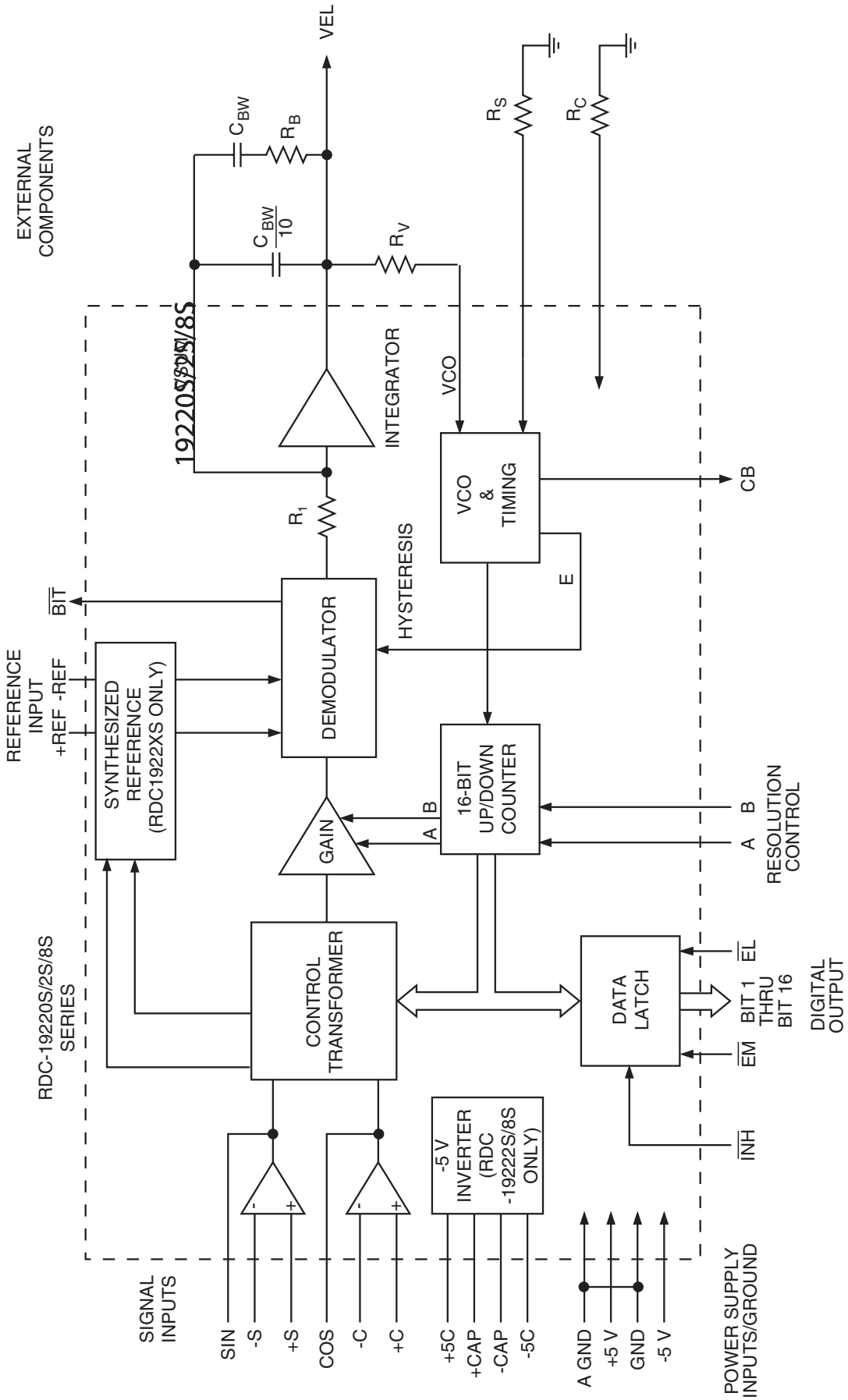


FIGURE 1. RDC-19220S/2S/8S BLOCK DIAGRAM

TABLE 1. RDC-19220S/2S/8S SERIES SPECIFICATIONS

These specifications apply over the rated power supply, temperature and reference frequency ranges, and 10% signal amplitude variation and harmonic distortion

PARAMETER	UNIT	VALUE			
RESOLUTION	Bits	10, 12, 14, or 16 (notes 1 & 2)			
FREQUENCY RANGE	Hz	47 - 1k (note 4)	1k - 4k	4k - 7k	4k - 10 k
ACCURACY -XX2 (NOTE 3)	Min	4 + 1 LSB	4 + 1 LSB	4 + 1 LSB	5 + 1 LSB
-XX3 (NOTE 3)	Min	2 + 1 LSB	2 + 1 LSB	3 + 1 LSB	4 + 1 LSB
Repeatability	LSB	±1	±1	±2	±2
Differential Linearity	LSB	±1	±1	±2	±2
REFERENCE		(+REF, -REF)			
Type		Differential			
Voltage: Differential	Vpp	10 max (note 8)			
Single Ended	Vp	±5 max (note 8)			
Overload	V	±25 continuous 100 transient (note 11)			
Frequency	Hz	47 to 10k			
Input Impedance	Ω	10M min //20 pf			
±Sig/Ref Phase Shift	deg	45 max from 400 Hz to 10 kHz (note 5)			
SIGNAL INPUT		(+S, -S, SIN, +C, -C, COS)			
Type		Resolver, differential, groundbased			
Voltage: Operating	Vrms	2 ±15%			
Overload	V	±25 continuous (note 11)			
Input impedance	Ω	10M min ‖ 10 pf			
DIGITAL INPUT/OUTPUT (NOTE 9)					
Logic Type		TTL/CMOS compatible			
Inputs		Logic 0 = 0.8 V max. / Logic 1 = 2.0 V min. Loading=10 µA max P.U. current source to +5 V //5 pF max., CMOS transient protected			
Inhibit ($\overline{INH}$)		Logic 0 inhibits; Data stable within 150 nS			
Enable Bits 1 to 8 ($\overline{EM}$)		Logic 0 enables; Data stable within 150 nS (Logic 0 = Transparent) Logic 1 = High Impedance, Data High Z within 100 nS			
Enable Bits 9 to 16 ($\overline{EL}$)		Logic 0 enables; Data stable within 150 nS (Logic 0 = Transparent) Logic 1 = High Impedance, Data High Z within 100 nS			
Resolution and Mode Control (A & B) (see notes 1 & 2)		Mode	B	A	Resolution
		Resolver	0	0	10 bits
		"	0	1	12 bits
		"	1	0	14 bits
		"	1	1	16 bits (Preset, see Note 9)
		LVDT/RVDT	-5V	0	8 bits
		"	0	-5V	10 bits
		"	1	-5V	12 bits
		"	-5V	-5V	14 bits
Outputs					
Parallel Data (Note 12)		10, 12, 14 or 16 parallel lines; natural binary angle positive logic (see note 2)			
Converter Busy (CB)		0.25 to 0.75 µs positive pulse leading edge initiates counter update			
Built-in-Test ($\overline{BIT}$)		Logic 0 for BIT condition. ±180 LSBs of positive or negative error, with a filter of 500 µs total, Loss-of-Signal (LOS) less than 500 mV, or Loss-of-Reference (LOR) less than 500 mV.			
Drive Capability		50 pF+ Logic 0; 1 TTL load, 1.6 mA at 0.4 V max. Logic 1; 10 TTL loads, = 0.4 mA at 2.8 V min Logic 0; 100 mV max driving CMOS Logic 1; +5 V supply minus 100 mV min driving CMOS High Z; 10 uA ‖ 5 pF max			

TABLE 1. RDC-19220S/2S/8S SERIES SPECIFICATIONS

These specifications apply over the rated power supply, temperature and reference frequency ranges, and 10% signal amplitude variation and harmonic distortion

PARAMETER	UNIT	VALUE			
DYNAMIC CHARACTERISTICS		(at maximum bandwidth)			
Resolution	bits	10	12	14	16
Tracking Rate (Note 6)	rps	1152	288	72	18
Bandwidth (Closed Loop) Max	Hz	1200	1200	600	300
Ka (Note 10)	1/sec²	5.7M	5.7M	1.4M	360k
A1	1/sec	19.5	19.5	4.9	1.2
A2	1/sec	295k	295k	295k	295k
A	1/sec	2400	2400	1200	600
B	1/sec	1200	1200	600	300
Acceleration (1 LSB lag)	deg/s²	2M	500k	30k	2k
Settling Time (179° step)	msec	2	8	20	50
VELOCITY CHARACTERISTICS					
Polarity		Positive for increasing angle			
Voltage Range(Full Scale) (Note 12)	V	±4 (at nominal ps)			
Scale Factor Error	%	10 typ		20 max	
Scale Factor TC	PPM/C	100 typ		200 max	
Reversal Error	%	0.75 typ		1.3 max	
Linearity	%	0.25 typ		1.0 max	
Zero Offset	mV	5 typ		10 max	
Zero Offset TC	µV/C	15 typ		30 max	
Load	kΩ			8 min	
Noise	Vp/V	1 typ		0.125 min, 2 max	
POWER SUPPLIES		(notes 6 and 7)			
Nominal Voltage	V	+5		-5	
Voltage Range	%	±5		±5	
Max Volt. w/o Damage	V	+7		-7	
Current	mA	17 typ, 25 max (each)			
TEMPERATURE RANGE					
Operating (Case)					
-10X, -40X	°C	-55 to +125			
Storage					
-10X, -40X	°C	-65 to +150			
THERMAL RESISTANCE					
Junction-to-Case (θjc)					
40-pin DDIP (ceramic)	°C/W	4.6			
44-pin J-Lead (ceramic)	°C/W	2.4			
PHYSICAL CHARACTERISTICS					
Size					
40-pin DDIP	in(mm)	2.0 x 0.6 x 0.2 (50.8 x 15.24 x 5.08)			
44-pin J-Lead	in(mm)	0.690 square (17.526)			
Weight		Ceramic			
40-pin DDIP	oz(g)	0.24 (6.80)			
44-pin J-Lead	oz(g)	0.064 (1.84)			

Notes: 1. Unused data bits are set to logic "0."
2. In LVDT mode, bit 16 is LSB for 14-bit resolution or bit 12 is LSB for 10-bit resolution
3. Accuracy specification below for LVDT mode, null to + full scale travel (45 degrees) (2-wire configuration).
4 Minute part = 0.15% + 1 LSB of full scale "resolution set"
2 Minute part = 0.07% + 1 LSB of full scale "resolution set"
Accuracy specification below for LVDT mode, full scale travel (90 degrees) (3-wire configuration).
4 Minute part = 0.07% + 1 LSB of full scale "resolution set"
2 Minute part = 0.035% + 1 LSB of full scale "resolution set"
Note that these accuracy specifications are for the converter and do not consider any front end external resistor tolerances.
4. If the frequency is between 47Hz and 1kHz, then there may be 1 LSB of jitter at quadrant boundaries.
5. The maximum phase shift tolerance will degrade linearly from 45 degrees at 400 Hz to 30 degrees at 60 Hz.
6. See text, General Setup Considerations.
7. When using internally generated -5V the internal -5V charge pump when measured at the converter pin, may be as low as -20% (or -4V).
8. A signal less than 500 mV will assert BIT.
9. Any unused input pins can be left floating (unconnected). All TTL & CMOS input pins are internally pulled up to +5 volts.
10. KA= Acceleration Constant, for a full definition see the RD/RDC application manual acceleration lag section.
11. When in overload condition the converter will not operate to specification and will not be damaged.
12. Dynamic accuracy may be degraded in high bandwidth system applications. See Theory of Operation section for details

THEORY OF OPERATION

The RDC-19220S/2S/8S series of converter is a single CMOS custom monolithic chip. It is implemented using mixed signal CMOS technology which merges precision analog circuitry with digital logic to form a complete high-performance tracking resolver-to-digital converter. For user flexibility and convenience, the converter bandwidth, dynamics, and velocity scaling are externally set with passive components.

FIGURE 1 is the RDC-19220S/2S/8S Functional Block Diagram. The converter operates with ±5 V DC power supplies. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of two main sections; a converter and a digital interface. The converter front-end consists of sine and cosine differential input amplifiers. These inputs are protected to ±25 V with 2 kΩ resistors and diode clamps to the ±5 V DC supplies. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 16-bit digital angle ϕ. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $SIN\theta COS\phi - COS\theta SIN\phi = SIN(\theta-\phi)$ using amplifiers, switches, logic and capacitors in precision ratios.

Note: The transfer function of the CT is normally trigonometric, but in LDVT mode the transfer function is triangular (linear) and could thereby convert any linear transducer output.

The converter accuracy is limited by the precision of the computing elements in the CT. For enhanced accuracy, the CT in these converters uses capacitors in precision ratios, instead of the more conventional precision resistor ratios. Capacitors, used as computing elements with op-amps, need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate (70 kHz) to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The DC error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which together with the velocity integrator forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above. The settings of the various error processor gains and break frequencies are done with external resistors and capacitors so that the converter loop dynamics can be easily controlled by the user.

Dynamic accuracy may be degraded in applications with a high system bandwidth. This dynamic accuracy error is usually not an issue when using the device's analog velocity output or position output data in a control-loop because they are inherently filtered due to comparatively low bandwidths in most applications.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Transfer Function Block Diagrams and its Bode Plots (open and closed loop). These are shown in FIGURES 2, 3, and 4.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient and $A^2 = A_1A_2$
and B is the frequency of lead compensation.

The components of gain coefficient are error gradient, integrator gain and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT+Error Amp+Demod with 2 Vrms input)

- Integrator gain = $\frac{C_S F_S}{1.1 C_{BW}}$ volts per second per volt

- VCO Gain = $\frac{1}{1.25\ R_V C_{VCO}}$ LSBs per second per volt

where: Cs = 10 pF
Fs = 70 kHz when Rs = 30 kΩ
Fs = 100 kHz when Rs = 20 kΩ
Fs = 125 kHz when Rs = 15 kΩ
Cvco = 50 pF

RV, RB, and CBW are selected by the user to set velocity scaling and bandwidth.

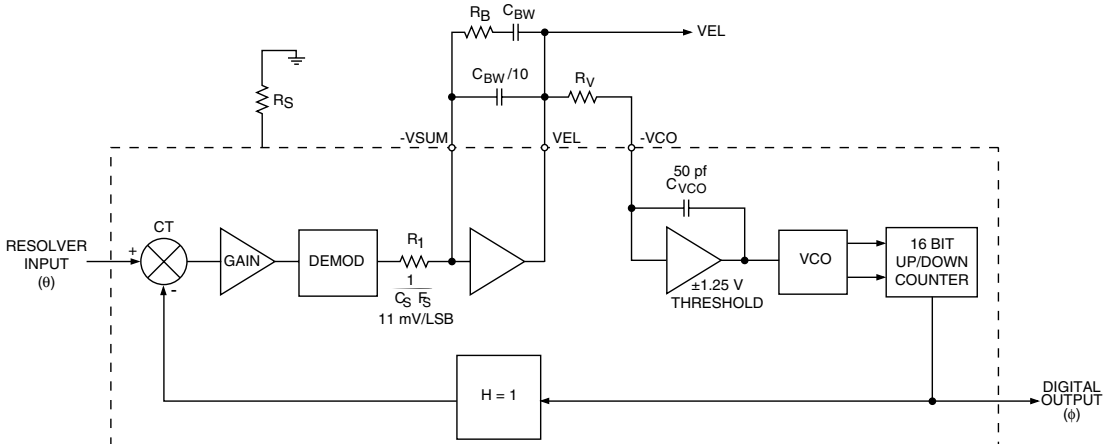


FIGURE 2. TRANSFER FUNCTION BLOCK DIAGRAM #1

FEATURES

SYNTHESIZED REFERENCE

The synthesized reference section of the RDC-119220S/2S/8S eliminates errors caused by quadrature voltage which is due to a phase shift between the reference and the signal lines. Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. Due to the inductive nature of synchros and resolvers, their signals lead the reference signal (RH and RL) by about 6°.

When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. As shown in FIGURE 1, the converter synthesizes its own COS($\omega t + \alpha$) reference signal from the SIN θ COS($\omega t + \alpha$), COS θ – COS($\omega t + \theta$) signal inputs and from the COSωt reference input. The phase angle of the synthesized reference is determined by the signal input. The reference input is used to choose between the +180° and -180° phases. The synthesized reference will always be exactly in phase with the signal input, and quadrature errors will therefore be reduced. The synthesized reference circuit also eliminates the 180° false error null hang up.

Due to the inductive nature of resolvers, the output signals typically lead the reference by 6°, and a 6° phase shift will cause problems for a 1.3 / 2.3 arc minute accuracy converter. A synthesized reference will always be exactly in phase with the signal input.

BUILT-IN-TEST (BIT)

The Built-In-Test output ($\overline{BIT}$) monitors the level of error from the demodulator. This signal is the difference in the input and output angles and ideally should be zero; if it exceeds approximately ±180 LSBs of positive or negative error (of the selected resolution) the logic level at $\overline{BIT}$ will change from a logic 1 to a logic 0.

A 500µs delay occurs before the excessive error bit becomes active. The dynamic delay is responsive to the active filler loop.

This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will also change to logic 0 for an overvelocity condition, because the converter loop cannot maintain input/output or if the converter malfunctions where it cannot maintain the loop at a null. During normal operation BIT may assert on power-up.

$\overline{BIT}$ will also be set low for a detected Loss-of-Signal (LOS) and/or a Loss-of-Reference (LOR). The $\overline{BIT}$ signal may pulse during certain error conditions (i.e., converter spin around or signal amplitude on threshold of LOS).

LOS will be detected if both sin and cos input voltages are less than 500 mV peak. LOR will be detected if the differential reference voltage is less than 500 mV peak.

The LOS has a filter on it to filter out the reference. Since the lowest specified frequency is 47hz (-27ms) the filter must have a time constant long enough to filter this out. Time constants of 50ms or more are possible.

GENERAL SETUP CONSIDERATIONS

Note: For detailed application and technical information see the RD/RDC converter applications manual which is available for download from the DDC web site @ www.ddc-web.com.

The following recommendations should be considered when installing the RDC-19220S/2S/8S Resolver-to-Digital (R/D) converter:

1) TR/BW RATIO

When setting the bandwidth (BW) and Tracking Rate (TR) (selecting five external components), the system requirements need to be considered. For the greatest noise immunity, select the minimum BW and TR the system will allow per TABLE 2.

Selecting a fBW that is too low relative to the maximum application tracking rate can create a spin-around condition in which the converter never settles. The relationship to insure against spin-around is as follows (TABLE 2.):

2) GROUNDS

There are two internal ground planes to reduce analog input noise due to digital ground currents.The resolver inputs and velocity output are referenced to AGND. The digital inputs and outputs are referenced to GND. The AGND and GND pins must be tied together as close to the package as possible, or unstable results may occur.

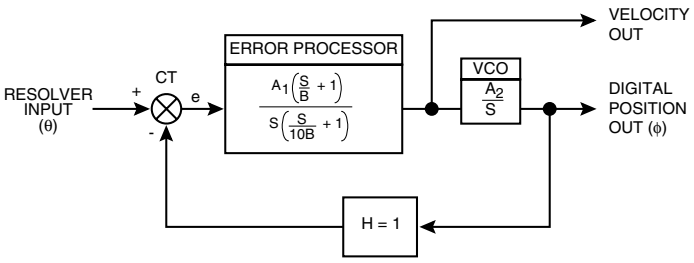


FIGURE 3. TRANSFER FUNCTION BLOCK DIAGRAM #2

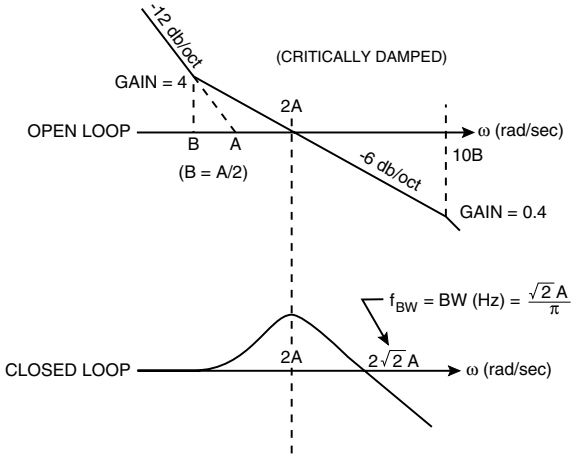


FIGURE 4. BODE PLOTS

TABLE 2. TRACKING/BW RELATIONSHIP	
RPS (MAX)/BW	RESOLUTION
1	10
0.50	12
0.25	14
0.125	16

3) BANDWIDTH AND VELOCITY

Setup of bandwidth and velocity scaling for the optimized critically damped case should proceed as follows:

DDC has external component selection software which considers all the criteria below and, in a simple fashion, asks the key parameters (carrier frequency, resolution, bandwidth, and tracking rate) to derive the external component values.

- Select the desired f_{BW} (closed loop) based on overall system dynamics.

- Select $f_{carrier} \geq 3.5 f_{BW}$

- Select the applications tracking rate (in accordance with TABLE 3), and use appropriate values for R SET and R CLK

- Compute $Rv = \frac{\text{Full Scale Velocity Voltage}}{\text{Tracking Rate (rps)} \times 2^{\text{resolution}} \times 50\text{ pF} \times 1.25\text{ V}}$

- Compute $C_{BW}\text{ (pF)} = \frac{3.2 \times Fs\text{ (Hz)} \times 10^8}{Rv \times (f_{BW})^2}$

- Where Fs = 67 kHz for R CLK = 30 KΩ
  100 kHz for R CLK = 20 KΩ
  125 kHz for R CLK = 15 KΩ

- Compute $R_B = \frac{0.9}{C_{BW} \times f_{BW}}$

- Compute $\frac{C_{BW}}{10}$

As an example:
Calculate component values for a 16-bit converter with 100Hz bandwidth, a tracking rate of 10RPS and a full scale velocity of 4 volts.

- $Rv = \frac{4\text{ V}}{10\text{ rps} \times 2^{16} \times 50\text{ pF} \times 1.25\text{ V}} = 97655\ \Omega$

- Compute $C_{BW}\text{ (pF)} = \frac{3.2 \times 67\text{ kHz} \times 10^8}{97655 \times 100\text{ Hz}^2} = 21955\text{ pF}$

- Compute $R_B = \frac{0.9}{21955 \times 10^{-12} \times 100\text{ Hz}} = 410\text{ k}\Omega$

Note: DDC has software available to perform the previous calculations. Contact DDC to request software or visit our web site at www.ddc-web.com to download software.

4) POWER SUPPLY

Power supplies are ±5 VDC. For lowest noise performance it is recommended that a 0.1µF or larger cap be connected from each supply to ground near the converter package. When using +5V and -5V supplies to power the RDC-19222S/8S converter, pins 22, 23, 25 and 26 must be no connection, and the 10µF cap between -CAP and + CAP is not installed.

When using the built-in -5 V inverter (only available on RDC-19222S/8S package), connect as shown in Figure 5. The current drain from the +5 V supply doubles. No external -5 V supply is needed. The power supply 47µf caps shown may be substituted with 10µf caps if the power supply lines are clean (minimal noise).

When using the built-in -5 V inverter, the maximum tracking rate should be scaled for a velocity output of 3.5 V max. Use the following equation to determine tracking rate used in the formula in Step 5:

$$\frac{TR\text{ (required)} \times (4.0)}{(3.5)} = \text{Tracking rate used in calculation}$$

Note: When using the highest BW and Tracking Rates, use of the -5 V inverter is not recommended.

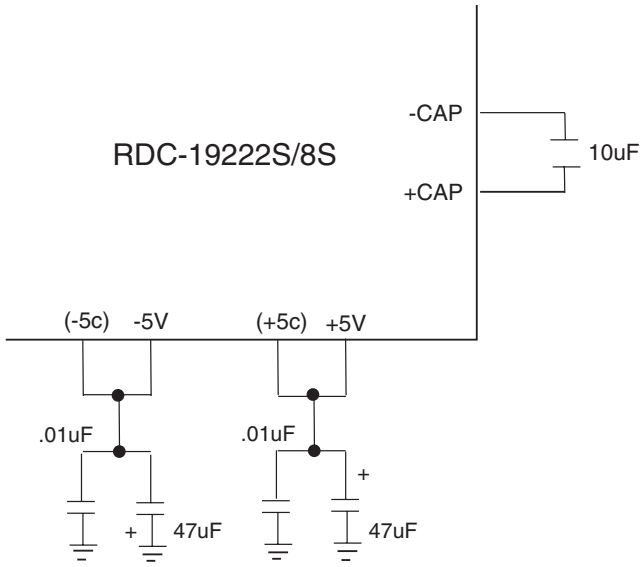


FIGURE 5. -5V BUILT-IN INVERTER

5) HIGHER TRACKING RATES AND CARRIER FREQUENCIES

Tracking rate (nominally 4 V) is limited by two factors: velocity voltage saturation and maximum internal clock rate (nominally 1,333,333 Hz). An understanding of their interaction is essential to extending performance.

The General Setup Considerations section makes note of the selection of Rv for the desired velocity scaling. Rv is the input resistor to an inverting integrator with a 50 pF nominal feedback capacitor. When it integrates to -1.25 V, the converter counts up 1 LSB and when it integrates to +1.25 V, the converter counts down 1 LSB. When a count is taken, a charge is dumped on the capacitor such that the voltage on it changes 1.25 V in a direction to bring it to 0 V. The output counts per second per volt input is therefore:

$$\frac{1}{(R_V \times 50\text{ pF} \times 1.25)}$$

As an example:

Calculate Rv for the maximum counting rate, at a VEL voltage of 4 V.

For a 12-bit converter there are 2^{12} or 4096 counts per rotation. 1,333,333/4096 = 325 rotations per second or 333,333 counts per second per volt.

$$R_V = \frac{1}{(333{,}333 \times 50\ pF \times 1.25)} = 48k\ Ohms$$

The maximum rate capability of the RDC-19220S/2S/8S is set by R_S. When R_S = 30 kHz it is nominally 1,333,333 counts/second, which equates to 325 rps (rotations per second). This is the absolute maximum; it is recommended to only run at < 90% of this rate (as given in TABLE 3), therefore the minimum RV will be limited to 55 kOhms.

6) TRANSFORMER ISOLATION

System requirements often include electrical isolation. There are transformers available for reference and synchro/resolver signal isolation. TABLE 5 includes a listing of the most common transformers. The synchro/resolver transformers reduce the voltage to 2 Vrms for a direct connection to the converter. See FIGURES 6A, 6B, 6C, and 6D for transformer layouts and schematics, and FIGURE 7 for typical connections.

TABLE 3. TRACKING RATE (MAX) IN RPS

RC / RSET (Ω)	RS / RCLK (Ω)	RESOLUTION			
		10	12	14	16
30k	30k	1152	288	72	18

Depending on the resolution select one of the values from this row, for use in converter max tracking rate formula. (See formula in Step 5.) Lower RS=Faster tracking rate Lower Resolution = Faster tracking rate

Note: R_C "Rcurrent" = RSET (Legacy Nomenclature)
R_S "Rsample" = RCLK
Note: The rates shown in Table 3 are based on ~90% of the nominal internal clock rate.

TABLE 4. CARRIER FREQUENCY (MAX) IN KHZ

RC / RSET (Ω)	RS / RCLK (Ω)	RESOLUTION			
		10	12	14	16
30k	30k	10	10	5	5

Note: R_C "Rcurrent" = RSET (Legacy Nomenclature)
R_S "Rsample" = RCLK
Note: For higher tracking rates not listed, contact the factory.

TABLE 5. TRANSFORMERS

P/N	TYPE	FREQUENCY (HZ)*	IN (VRMS)*	OUT (VRMS)**	ANGLE ACCURACY***	LENGTH (IN)	WIDTH (IN)	HEIGHT (IN)	FIGURE NUMBER	AVAILABLE FROM (NOTE1)
52034	S - R	400	11.8	2	1	0.81	0.61	0.3	5A	BETA
52035	S - R	400	90	2	1	0.81	0.61	0.3	5A	BETA
52036	R - R	400	11.8	2	1	0.81	0.61	0.3	5B	BETA
52037	R - R	400	26	2	1	0.81	0.61	0.3	5B	BETA
52038	R - R	400	90	2	1	0.81	0.61	0.3	5B	BETA
B-426	Reference	400	115	3.4	N/A	0.81	0.61	0.32	5C	BETA
24133-X	Reference	60	115	3/6 ****	N/A	1.125	1.125	.42	5D	DDC

* ±10% Frequency (Hz) and Line-to-Line input voltage (Vrms) tolerances
** 2 Vrms Output Magnitudes are -2 Vrms ±0.5% full scale
*** Angle Accuracy (Max Minutes)
**** 3 Vrms to ground or 6 Vrms differential (±3% full scale)
Dimensions are for each individual main and teaser
60 Hz Synchro transformers are active (requires ±15 Vdc power supplies)
400 Hz transformer temperature range: -55°C to +125°C
60 Hz transformer (24133-X) temperature ranges: add to part number -1 or -3,
-1 = -55°C to +85°C
-3 = 0 to +70°C

Note 1: Refers to the company from which the transformer can be purchased.

Beta Transformer Technology Corporation
www.bttc-beta.com

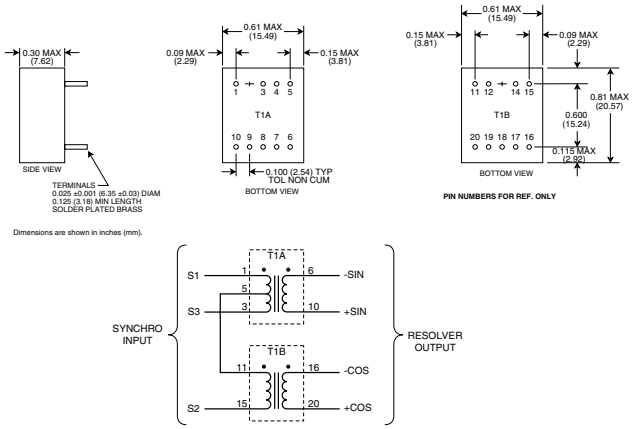


FIGURE 6A. TRANSFORMER LAYOUT AND SCHEMATIC (SYNCHRO INPUT - 52034/52035)

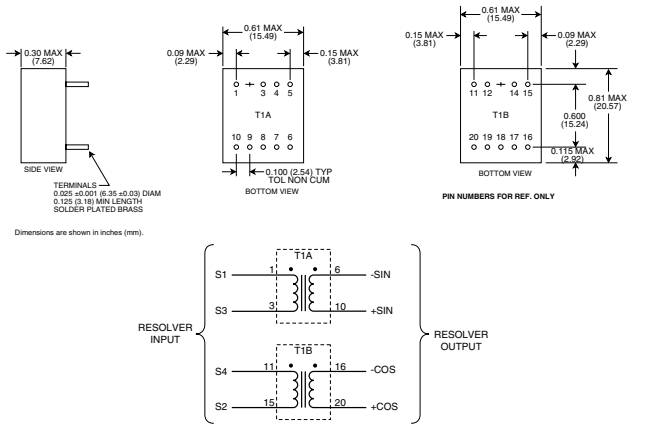
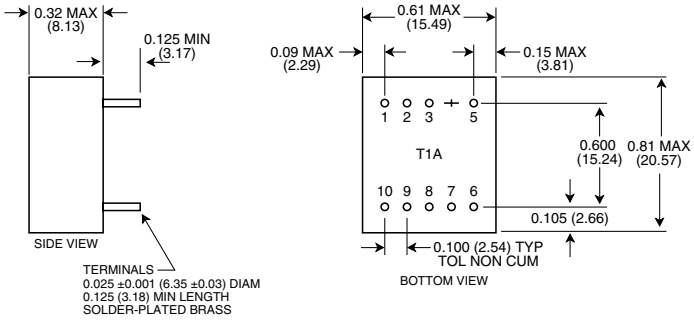


FIGURE 6B. TRANSFORMER LAYOUT AND SCHEMATIC (RESOLVER INPUT - 52036/52037/52038)



Dimensions are shown in inches (mm).

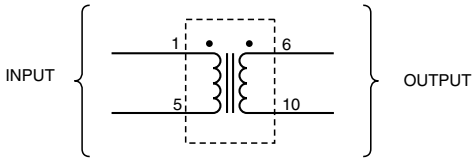
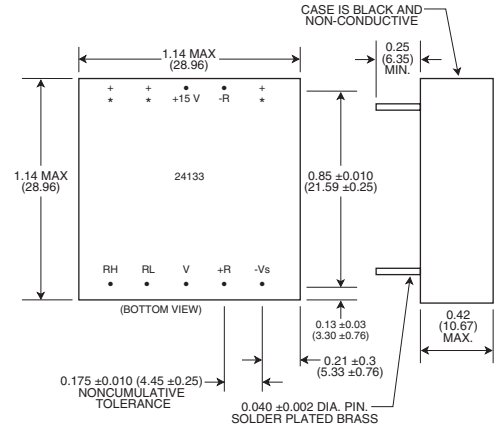
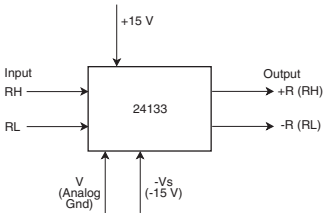


FIGURE 6C. TRANSFORMER LAYOUT AND SCHEMATIC (REFERENCE INPUT - B-426)





An asterisk * indicates that the pin is omitted.

FIGURE 6D. 60 Hz REFERENCE TRANSFORMER DIAGRAM (REFERENCE INPUT - 24133)

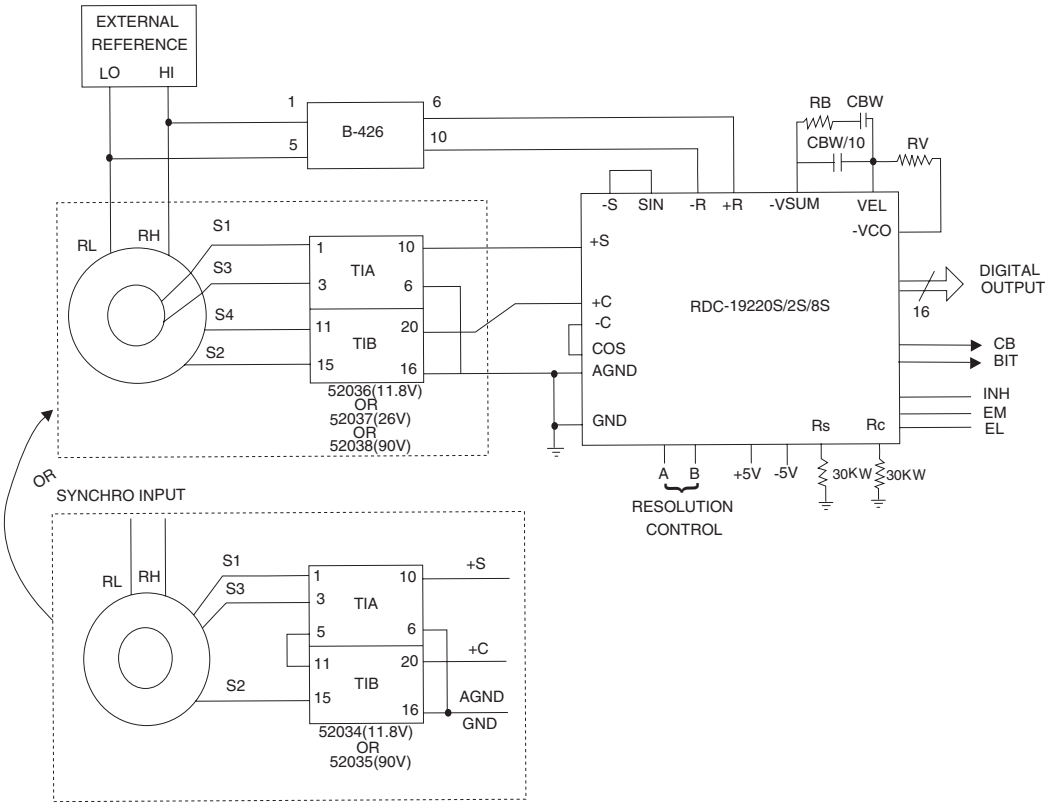


FIGURE 7. TYPICAL TRANSFORMER CONNECTIONS

TYPICAL INPUT CONNECTIONS

FIGURES 8 through 10 illustrate typical input configurations

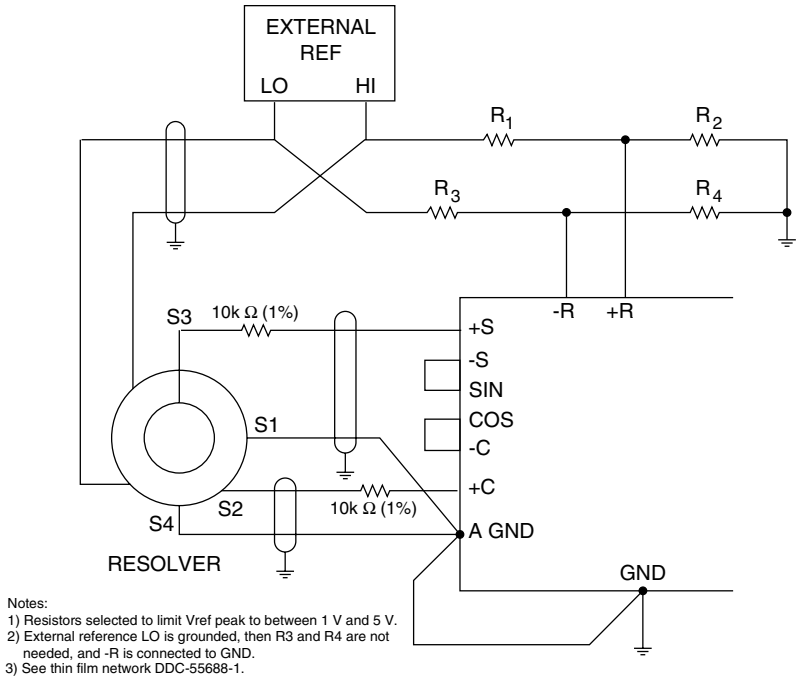
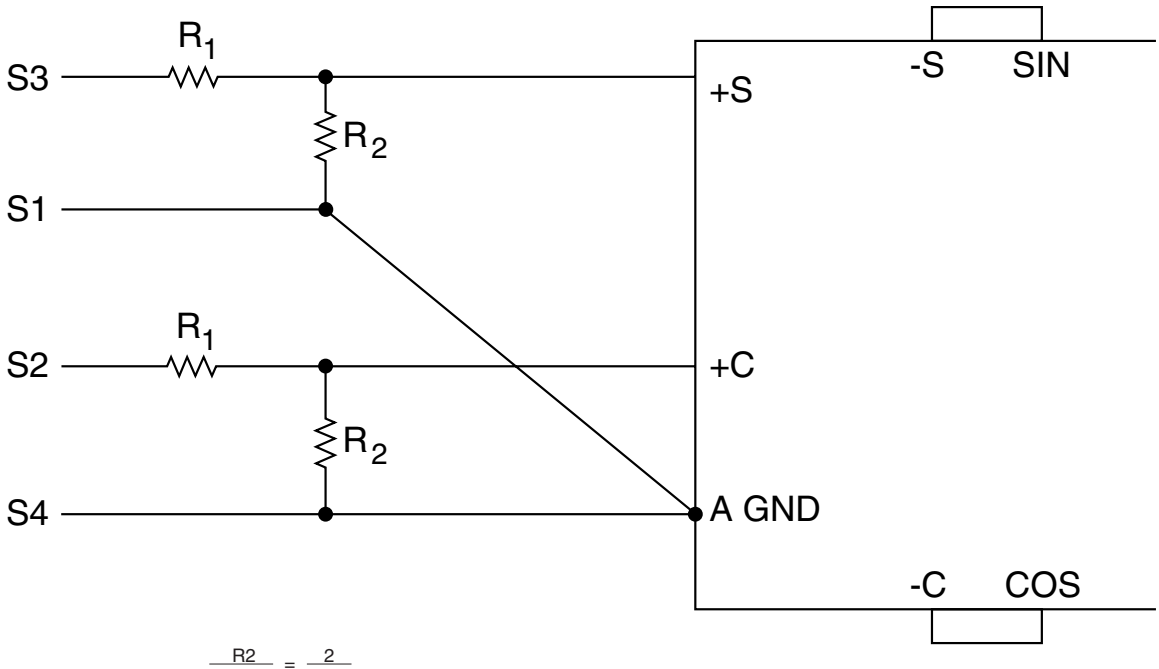


FIGURE 8. TYPICAL CONNECTIONS, 2 V RESOLVER, DIRECT INPUT



$$\frac{R2}{R1 + R2} = \frac{2}{X\ Volt}$$

R1 + R2 should not load the Resolver too much; it is recommended to use a R2 = 10k.

R1 + R2 Ratio Errors will result in Angular Errors,
2 cycle, 0.1% Ratio Error = 0.029° Peak Error.

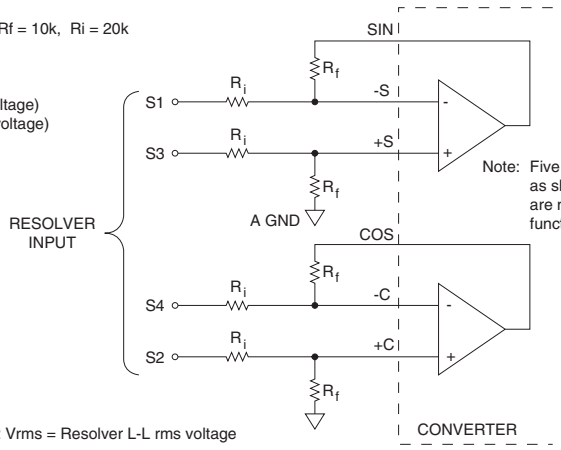
FIGURE 9. TYPICAL CONNECTIONS, X- VOLT RESOLVER, DIRECT INPUT

Examples of Component Calculations:

1) 2V in, need gain of 1, use 10k for Rf and Ri
Gain = Rf/Ri

2) 4 V in, need gain of 0.5, Rf = 10k, Ri = 20k

To calculate Ri:
Select 10k for Rf
Ri = Rf x 0.5 x (input L-L voltage)
Ri = 10k x 0.5 x (input L-L voltage)



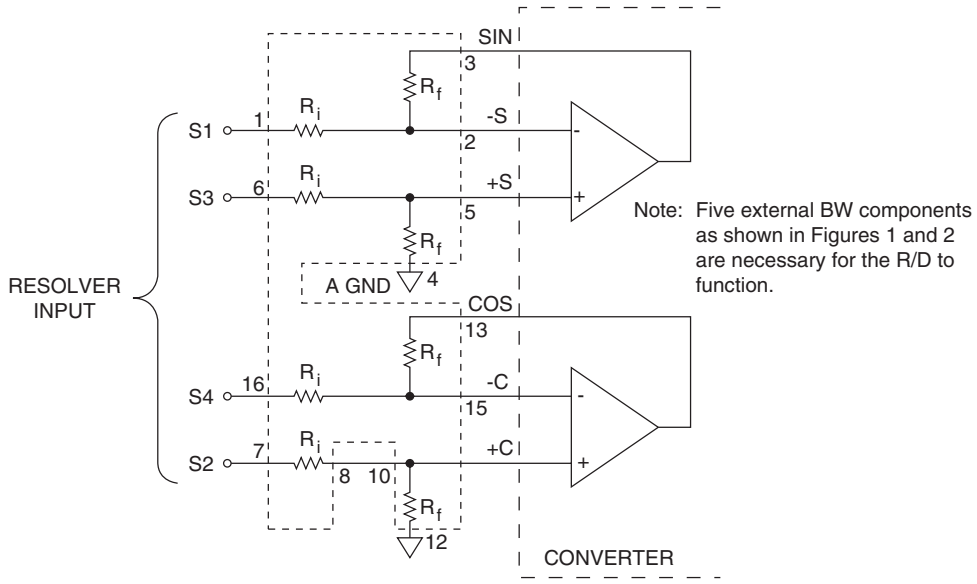
$\frac{Ri}{Rf}$ X 2 Vrms = Resolver L-L rms voltage

Rf ≥ 6 kΩ

S1 and S3, S2 and S4, and RH and RL should be ideally twisted shielded, with the shield tied to AGND at the converter.

For 2V direct inputs use 10k Ohm matched resistors for Ri and Rf.

FIGURE 10A. DIFFERENTIAL RESOLVER INPUT



S1 and S3, S2 and S4, and RH and RL should be ideally twisted shielded, with the shield tied to AGND at the converter.

For DDC-49530: Ri = 70.8 k ohms, 11.8 V input, synchro or resolver.

For DDC-49590: Ri = 270 k ohms, 90 V input, synchro or resolver.

Maximum additional error is 1 LSB, using recommended thin film package.

Input options affect DC offset gains and therefore carrier frequency ripple and jitter. Offset gains associated with differential mode (offset gain for differential configuration = 1+Rf/Ri) and direct mode (offset gain for direct configuration = 1) show differential mode will always be higher. Higher DC offsets cause higher carrier frequency ripple due to the demodulation process. This carrier frequency ripple rides on top of the DC error signal, causing jitter. A higher carrier frequency versus bandwidth ratio will help to decrease ripple and jitter associated with offsets. In summary, R/Ds with differential inputs are more susceptible to offset problems than R/Ds in single-ended mode. R/Ds in higher resolutions, such as 16 bit, will further compound offset issues due to higher internal voltage gains. Although the differential configuration has a higher DC offset gain, the differential configuration's common mode noise rejection makes it the preferred input option. The tradeoffs should be considered on a design to design basis. Also refer to FAQ-GIQ-021.

FIGURE 10B. DIFFERENTIAL RESOLVER INPUT, USING DDC-49530, DDC-57470 (11.8 V),DDC-73089 (2V), OR DDC-49590 (90 V)

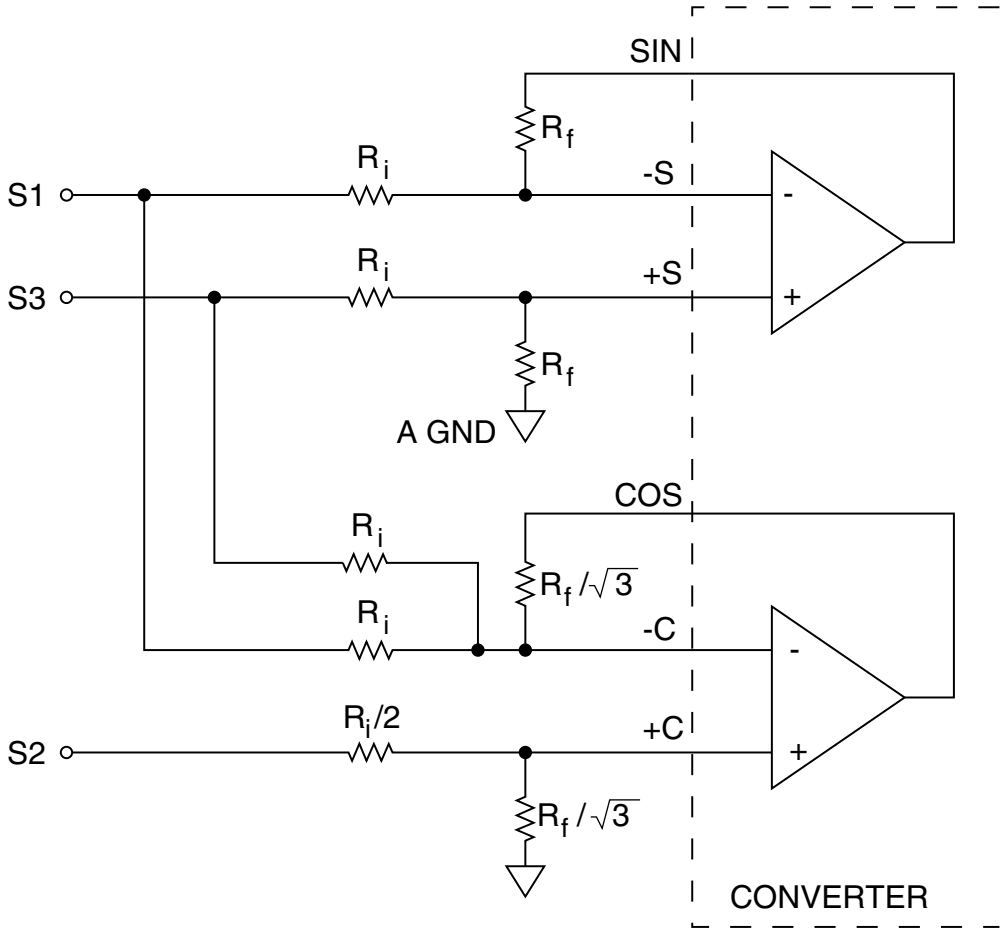
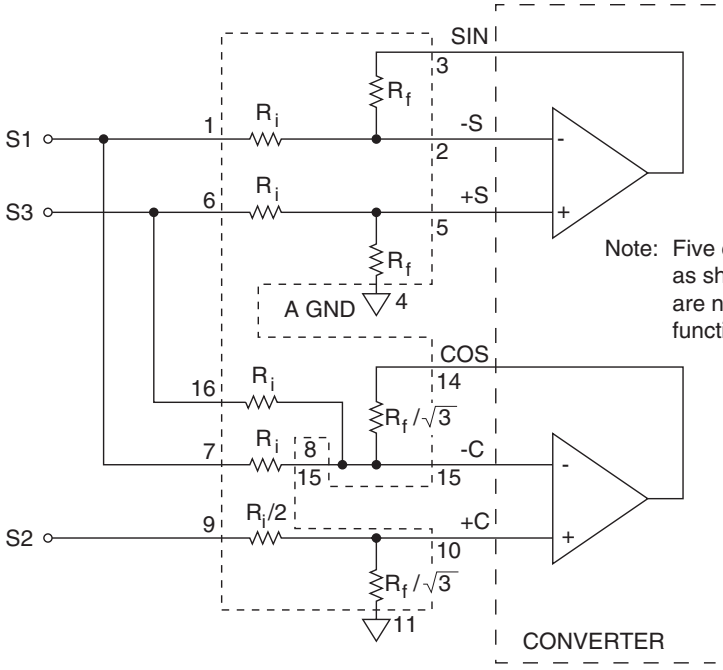


FIGURE 10C. SYNCHRO INPUT



Note: Five external BW components as shown in Figures 1 and 2 are necessary for the R/D to function.

S1, S2, and S3 should be triple twisted shielded; RH and RL should be twisted shielded, In both cases the shield should be tied to AGND at the converter.
90 V input = DDC-49590: Ri = 270 kΩ, 90 V input, synchro or resolver.
11.8 V input = DDC-49530: Ri = 70.8 kΩ, 11.8 V input, synchro or resolver.
Maximum additional error is 1 LSB when using recommended thin-film package.

FIGURE 10D. SYNCHRO INPUT, USING DDC-49530/DDC-57470 (11.8 V) OR DDC-49590 (90 V)

VELOCITY TRIMMING

RDC-19220S/2S/8S specifications for velocity scaling, reversal error, and offset are contained in TABLE 1. Velocity scaling and offset are externally trimmable for applications requiring tighter specifications than those available from the standard unit. FIGURE 11 shows the setup for trimming these parameters with external potentiometers. It should also be noted that when the resolution is changed, velocity scaling is also changed. Since the VEL output is from an integrator with capacitor feedback, the VEL voltage cannot change instantaneously. Therefore, when changing resolution while moving, there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth.

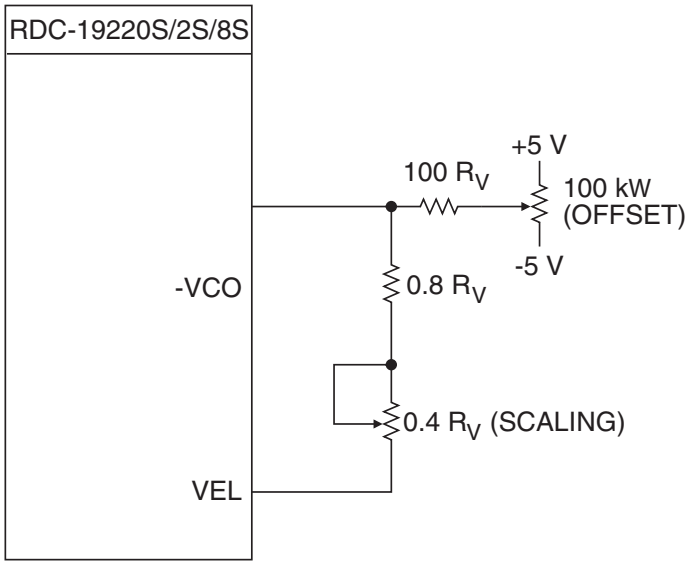


FIGURE 11. VELOCITY TRIMMING

LVDT (LINEAR VARIABLE DIFFERENTIAL TRANSFORMER) MODE

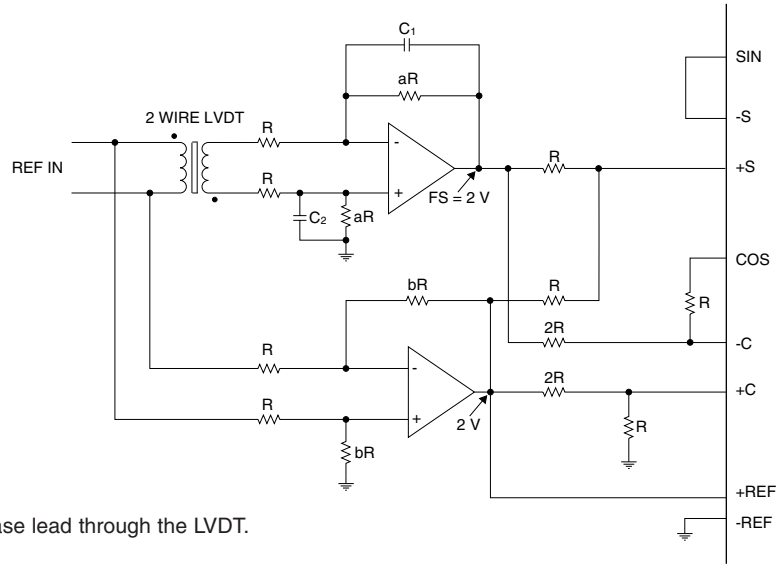
As shown in TABLE 1 the RDC-19220S/2S/8S unit can be made to operate as a LVDT-to-digital converter by connecting Resolution Control inputs A and B to "0," "1," or the -5 volt supply. In this mode the RDC-19220S/2S/8S functions as a ratiometric tracking linear converter. When linear AC inputs are applied from an LVDT the converter operates over one quarter of its range. This results in two less bits of resolution for LVDT mode than are provided in resolver mode.

The LVDT output signals will need to be scaled to be compatible with the converter input. FIGURE 12B is a schematic of an input scaling circuit applicable to 3-wire LVDTs. The value of the scaling constant "a" is selected to provide an input of 2 Vrms at full stroke of the LVDT. The value of scaling constant "b" is selected to provide an input of 1 Vrms at null of the LVDT. Suggested components for implementing the input scaling circuit are a quad opamp, such as a 4741 type, and precision thin-film resistors of 0.1% tolerance. FIGURE 12A illustrates a 2-wire LVDT configuration.

Data output of the RDC-19220S/2S/8S is Binary Coded in LVDT mode. The most negative stroke of the LVDT is represented by ALL ZEROS and the most positive stroke of the LVDT is represented by ALL ONES. The most significant 2 bits (2 MSBs) may be used as overrange indicators. Positive overrange is indicated by code "01" and negative overrange is indicated by code "11" (see TABLE 6).

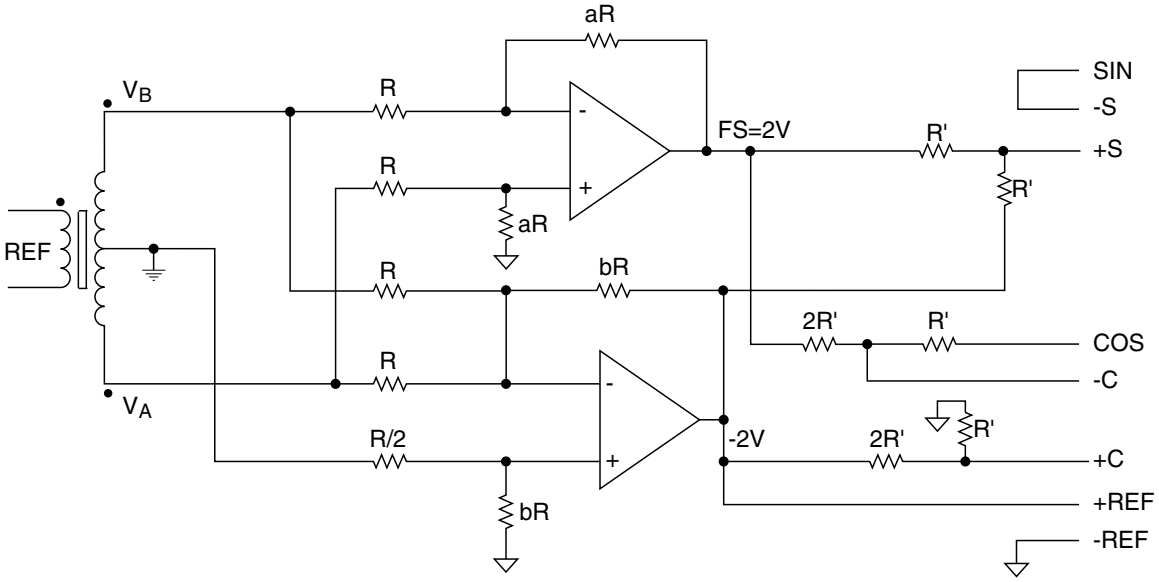
TABLE 6. LVDT OUTPUT CODE FOR FIGURE 12B

LVDT OUTPUT	OVER RANGE	MSB DATA		LSB
+ over full travel	01	xxxx	xxxx	xxxx
+ full travel -1 LSB	00	1111	1111	1111
+0.5 travel	00	1100	0000	0000
+1 LSB	00	1000	0000	0001
null	00	1000	0000	0000
- 1 LSB	00	0111	1111	1111
-0.5 travel	00	0100	0000	0000
- full travel	00	0000	0000	0000
- over full travel	11	xxxx	xxxx	xxxx



$C_1 = C_2$, set for phase lag = phase lead through the LVDT.

FIGURE 12A. 2-WIRE LVDT DIRECT INPUT



Notes;

1. R 10kΩ
2. Consideration for the value of R is LVDT loading.
3. RMS values given.
4. Use the absolute values of Va and Vb when subtracting per the formula for calculating resistance values, and then use the calculated sign of "Va and Vb" for calculating SIN and COS. The calculations shown are based upon full scale travel being to the Va side

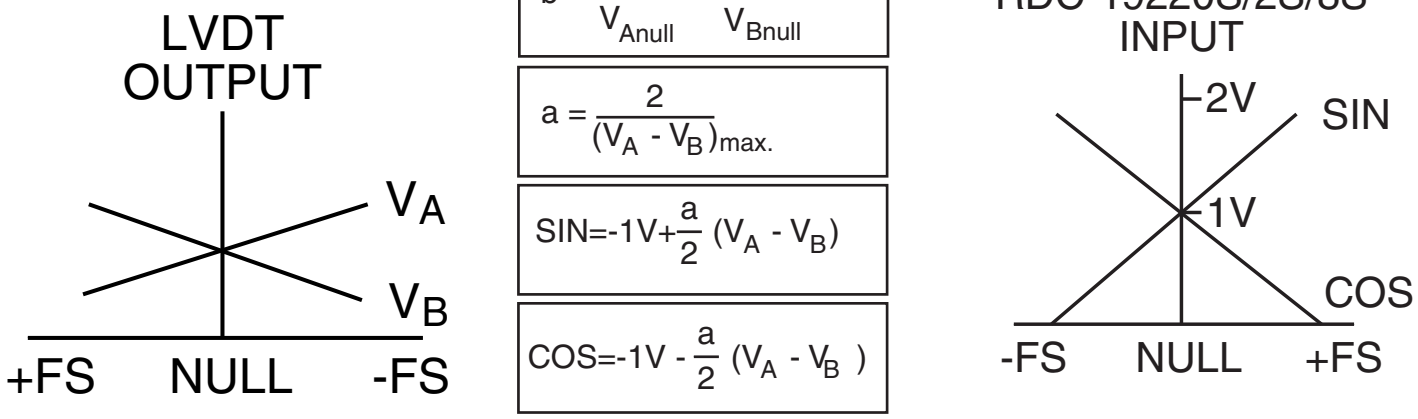


FIGURE 12B. 3-WIRE LVDT SCALING CIRCUIT

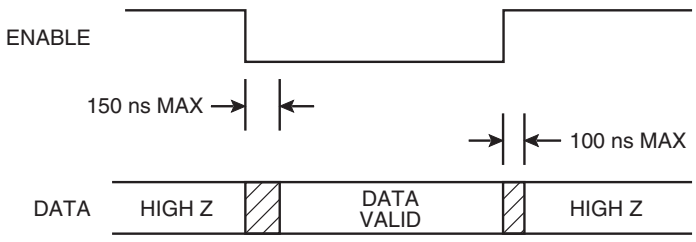
INHIBIT, ENABLE, AND CB TIMING

The Inhibit ($\overline{INH}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter.

Output angle data is enabled onto the tri-state data bus in two bytes. Enable MSBs ($\overline{EM}$) is used for the most significant 8 bits and Enable LSBs ($\overline{EL}$) is used for the least significant 8 bits. The tri-state data bus returns to the high impedance state 100 ns maximum after the rising edge of the enable signal.

The Converter Busy (CB) signal indicates that the tracking converter output angle is changing 1 LSB. 16 Bit data read

EM/EL set low / ground



Note: For 16 BIT BUS operation, EM/EL may be tied to ground for transparent mode, as long as only 1 R/D channel is on the data bus.

FIGURE 13. ENABLE TIMING

16 BIT DATA READ/TIMING SETUP

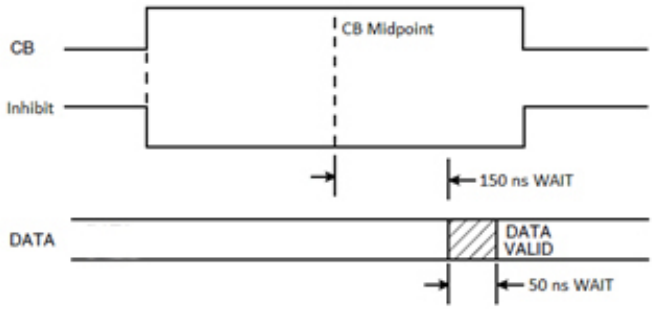


FIGURE 14. 16 BIT DATA READ

EM/EL set low / ground

Set inhibit low on CB start edge. Calculate inhibit wait time for when a valid data read can be done.

Inhibit wait time = 1 / (40 x Fs) + 150ns + 50ns

FS value for inhibit wait time calculation

RS VALUE USED*	FS VALUE
30Kohms	67,000
20Kohms	100,000
15Kohms	134,000

***Note:** RS resistor value is set for max tracking rate and installed as an external component.

SAMPLE 16-BIT DATA READ SEQUENCE USING INHIBIT ONLY

To read data in the shortest time duration, inhibit must be started on CB start edge. To do a data read without monitoring CB start edge, the worst case wait timing is defined below.

Presets: EM and EL must be set low or hard grounded, no need to monitor and trigger inhibit on CB start edge when using this worst case timing sequence:

1. Inhibit (set to Low).
2. Wait 575 ns.
3. Read 16-bit data bus.
4. Inhibit (set to High).
5. Repeat next data read from step 1.

NOTE: This timing sequence is for worst case timing using the inhibit pin only for control without monitoring the CB start edge. For the shortest data read wait time, CB start edge must be used for initializing an inhibit and a calculation must be performed for best time of inhibit.

TABLE 8. RDC-19220S PINOUTS (40-PIN)

#	NAME	DESCRIPTION	#	NAME	DESCRIPTION
1	A	Resolution Control	40	+5 V	Power Supply
2	B	Resolution Control	39	$\overline{EL}$	Enable LSBs (see note)
3	$\overline{INH}$	Inhibit	38	Bit 16	LSB
4	+REF	+Reference Input	37	Bit 8	
5	-REF	-Reference Input	36	Bit 15	
6	-VCO	Neg VCO Input	35	Bit 7	
7	-VSUM	Vel Sum Point	34	Bit 14	
8	VEL	Velocity Output	33	Bit 6	
9	+C	Signal Input	32	Bit 13	
10	COS	Signal Output	31	Bit 5	
11	-C	Signal Input	30	Bit 12	
12	+S	Signal Input	29	Bit 4	
13	+SIN	Signal Output	28	Bit 11	
14	-S	Signal Input	27	Bit 3	
15	-5 V	Power Supply	26	Bit 10	
16	R_S	Sampling Set	25	Bit 2	
17	R_C	Current Set	24	Bit 9	
18	$\overline{EM}$	Enable MSBs	23	Bit 1	MSB
19	A GND	Analog Ground	22	CB	Converter Busy
20	GND	Ground	21	$\overline{BIT}$	Built-In-Test

Note:
1) The RDC-19220S requires both ±5 V power supplies.

TABLE 9. RDC-19222S/8S PINOUTS (44-PIN, +5 V ONLY)

#	NAME	DESCRIPTION	#	NAME	DESCRIPTION
1	$\overline{EL}$	Enable LSBs	23	-CAP	Neg. Terminal
2	+5 V	Power Supply (see note)	24	GND	Ground
3	A	Resolution Control	25	+CAP	Pos. Terminal
4	B	Resolution Control	26	+5C (+5V)	Pos. Supply Cap
5	$\overline{INH}$	Inhibit	27	$\overline{BIT}$	Built-In-Test
6	+REF	+Reference Input	28	CB	Converter Busy
7	-REF	-Reference Input	29	Bit 1	MSB
8	-VCO	Neg VCO Input	30	Bit 9	
9	-VSUM	Vel Sum Point	31	Bit 2	
10	VEL	Velocity Output	32	Bit 10	
11	+C	Signal Input	33	Bit 3	
12	COS	Signal Output	34	Bit 11	
13	-C	Signal Input	35	Bit 4	
14	+S	Signal Input	36	Bit 12	
15	SIN	Signal Output	37	Bit 5	
16	-S	Signal Input	38	Bit 13	
17	-5 V	Power Supply	39	Bit 6	
18	RS	Sampling Set	40	Bit 14	
19	RC	Current Set	41	Bit 7	
20	$\overline{EM}$	Enable MSBs	42	Bit 15	
21	A GND	Analog Ground	43	Bit 8	
22	-5C (-5 V)	Neg. Supply Cap	44	Bit 16	LSB

Note:
1) When using the built-in -5 V inverter: connect pin 2 to 26, pin 17 to 22, and a 10 µF/10 VDC capacitor from pin 23 (negative terminal) to pin 25 (positive terminal). Connect a 47 µF/10 VDC capacitor from -5 V to GND. The current drain from the +5 V supply doubles. No external -5 V supply is needed.
2) The RDC-19222S can be used with ± 5 V or +5 V only.

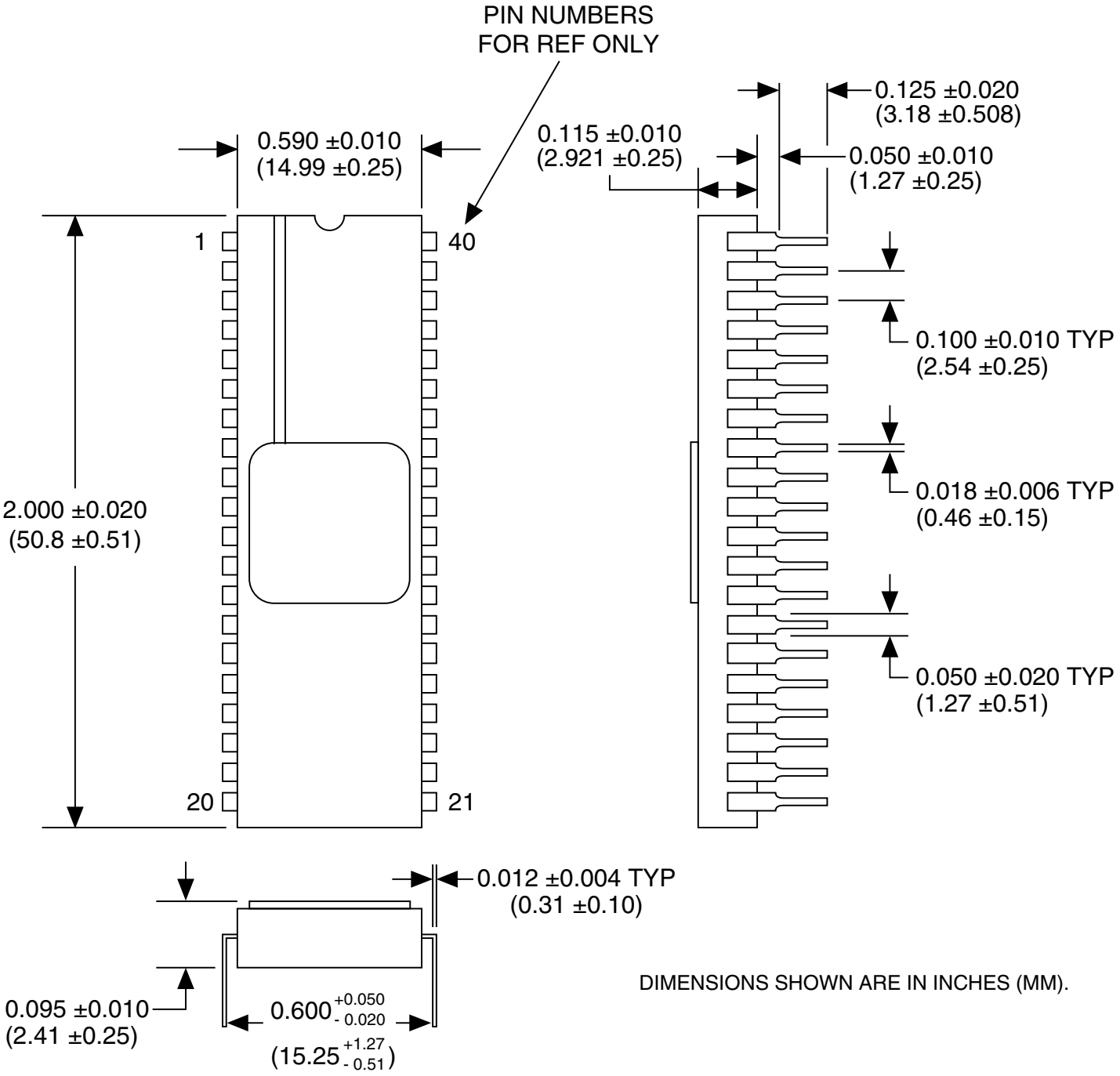


FIGURE 15. RDC-19220S (40-PIN DDIP) CERAMIC PACKAGE MECHANICAL OUTLINE

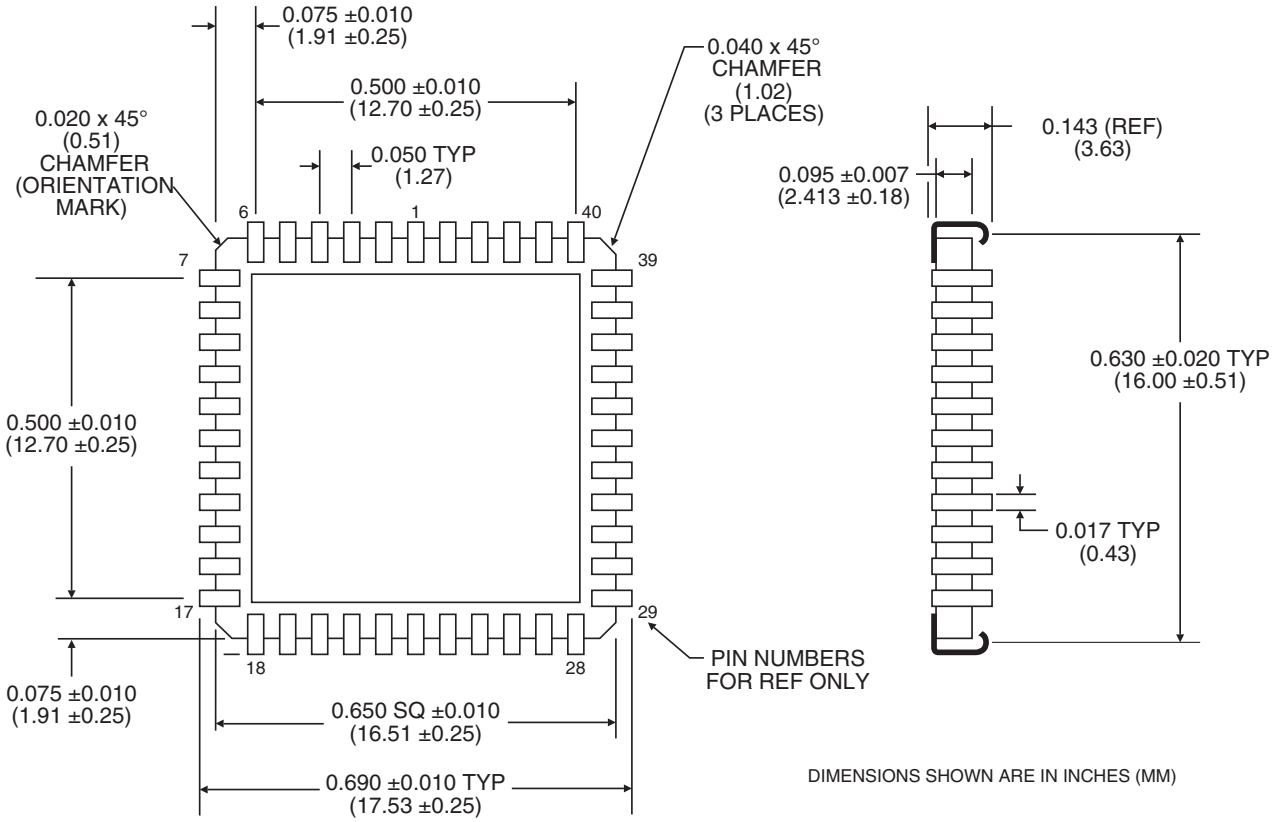


FIGURE 16. RDC-19222S/8S (44-PIN CERAMIC J-LEAD) MECHANICAL OUTLINE

THIN-FILM RESISTOR NETWORKS FOR MOTION FEEDBACK PRODUCTS

DDC converters such as the RDC-19220S/2S/8S require closely matched 2Vrms Sin/Cos input voltages to minimize digital error. DDC has custom thin-film resistor networks that provide the correctly matched 2Vrms converter outputs for 11.8Vrms Resolver/Synchro or 90Vrms synchro applications.

Any imbalance of the resistance ratio between the Sin/Cos inputs will create errors in the digital output. DDC's custom thinfilm resistor networks have very low imbalance percentages. The networks are matched to 0.02%, which equates to 1 LSB of error for a 16-bit application.

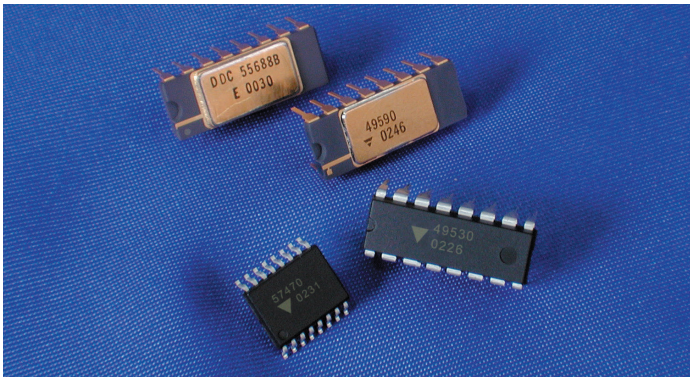


FIGURE 17. THIN FILM RESISTOR NETWORKS

TABLE 9. THIN-FILM RESISTOR NETWORKS

THIN FILM RESISTOR NETWORK	INPUT VOLTAGE (VRMS)	OUTPUT VOLTAGE (VRMS)	PACKAGE TYPE
DDC-55688-1	2 Single Ended	2	Ceramic DIP
DDC-49530	11.8	2	Plastic DIP
DDC-57470	11.8	2	Surface Mount
DDC-49590	90	2	Ceramic DIP
DDC-76037	2 Differential	2	Plastic DIP
DDC-73089-1	2 Differential	2	Surface Mount
DDC-57471	90	2	Surface Mount

Notes:
1. For thin film network specifications see the "Thin Film Network Specifications for Motion Feedback Products" Data Sheet available from the DDC web site.
2. Operating temperature range is -55°C to +125°C.

ORDERING INFORMATION

RDC-1922XS-XXXX (Ceramic Package)

Supplemental Process Requirements:
- T = Tape and Reel (Not available in 40-pin DDIP package)
- S = Pre-Cap Source Inspection
- L = 100% Pull Test
- Q = Pre-Cap Source and 100% Pull Test
- K = One Lot Date Code
- W = One Lot Date Code and Pre-Cap Source Inspection
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, Pre-Cap Source Inspection and 100% Pull Test
- Blank = None of the Above

Accuracy (Note 3):
- 2 = 4 minutes + 1 LSB
- 3 = 2 minutes + 1 LSB

Process Requirements:
- 0 = Standard DDC Processing (Note 1), without Burn-In
- 1 = MIL-PRF-38534 Compliant (Note 2)
- 2 = Standard DDC Processing (Note 1), with Burn-In
- 3 = MIL-PRF-38534 Compliant (Note 2), with PIND testing
- 4 = MIL-PRF-38534 Compliant (Note 2, 4), with Solder Dip (Not available in lead free)
- 5 = MIL-PRF-38534 Compliant (Note 2, 4), with PIND testing, and Solder Dip (Not available in lead free)
- 6 = Standard DDC Processing (Note 1), with PIND testing, and Burn-In
- 7 = Standard DDC Processing (Note 1, 4), with Solder Dip, and Burn-In (Not available in lead free)
- 9 = Standard DDC Processing (Note 1, 4), with Solder Dip, without Burn-In (Not available in lead free)

Temperature Grade / Data Requirements:
- 1 = -55 to +125°C
- 4 = -55 to +125°C, with Variables Test Data

Package: (Lead Free) (Note 3)
- 0 = 40-Pin DDIP, ("+5 volt only" power supply feature - not available)
- 2 = 44-Pin J-Lead (RoHS compliant) (Note 6)

Notes:
1. Standard DDC processing with burn-in and full temperature test. See table below
2. MIL-PRF-38534 product grading is designated with the following dash numbers:
   - Class H is a -11X, 13X, 14X, 15X, 41X, 43X, 44X, 45X
   - Class G is a -21X, 23X, 24X, 25X, 51X, 53X, 54X, 55X
   - Class D is a -31X, 33X, 34X, 35X, 81X, 83X, 84X, 85X
3. See specifications table 1 for accuracy over frequency range.
4. These products contain tin-lead solder finish "SN63" as applicable to solder dip requirements.
5. Package is lead free provided no solder dip Processing Requirement option is selected. Lead finish is gold over nickel.
6. Package is RoHS compliant provided no solder dip Processing Requirement option is selected.

PACKAGING:

RDC-19222S/8S are shipped in JEDEC trays that are acceptable for use with pick and place operation.

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS

TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 (note 1), 1030 (note 2)	TABLE 1

Notes:
1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

ORDERING INFORMATION

RDC-19228S-4XXX **(MIL-PRF-38534 Class K) (Note 1, 2, 3)**

Mandatory Process Requirements (one of the following must be selected):
- L = 100% Pull Test (standard on this device)
- Q = Pre-Cap Source and 100% Pull Test Inspection (contact factory)
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, Pre-Cap Source Inspection and 100% Pull Test (contact factory)

Accuracy: (Note 4)
- 3 = 2 minutes + 1 LSB

Process Requirements: (Burn-In is in accordance with MIL-STD-883)
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip (Note 5)

Temperature Grade / Data Requirements:
- 4 = -55 to +125°C, with Variables Test Data

Package: (Lead Free) (Note 6)
- 8 = Class K, 44-Pin J-Lead Ceramic Package

Notes:
1. MIL-PRF-38534 Class K device
2. Rad data by lot code available upon request
3. Includes X-Ray
4. See table 1 in data sheet for accuracy over frequency range
5. Solder dip process requirement option contains tin-lead solder finish "SN63"
6. Package is lead free provided no solder dip process requirement option is selected. Lead finish is gold over nickel.
7. Package is RoHS compliant provided no solder dip processing option is selected
8. RDC-19228S are shipped in JEDEC trays that are acceptable for use with pick-and-place operation

The information in this data sheet is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith.
Specifications are subject to change without notice.

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