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PRELIMINARY

SDC-36017
Four Channel
Synchro/Resolver-to-Digital
VXI/VME Card
User's Guide

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1.0 Description

1.1 SDC-36017 User's Guide

Thank you for purchasing ILC Data Device Corporation's SDC-36017 4 Channel Synchro/Resolver to Digital VXI/VME Card. This guide can be read sequentially to first familiarize you with the card's physical features, jumper locations, etc. It continues with hardware configuration. The guide then covers installation and using the supplied software to develop custom applications.

1.2 Hardware

The SDC-36017 is a Register Based "B" size VXI/VME card containing four channels of Synchro/Resolver to Digital converters. Each channel is totally independent, can accept 11.8V LL Synchro or Resolver signals, and can be jumper programmed for bandwidtth and resolution. The SDC-36017 incorporates the RDC-19222 in its design, the latest in DDC's generation of high performance Synchro/Resolver converter monolithics.

The SDC-36017 card was designed for quick setup time. Bandwidth can be set to 100Hz or 15 Hz depending on the application. (For boards with serial numbers less than 91, bandwidth can be 100Hz or 500 Hz. Please refer to section 2.1.3 Bandwidth Options.)Selection is done using jumpers since all necessary components are included on the board. Carriers are also included for the option of adding extra components for selection of custom bandwidth.

Additionally, the SDC-36017 contains a Reference Oscillator which is computer programmable over the frequency range of 320 to 10200 Hz in 40 Hz steps, and the voltage range of 0 to 6.6 Vrms in 26 mVrms steps. The card can be configured to provide all I/O connections to the P2 connector for VME applications.

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1.3 Software

The SDC-36017 is a register based VXI/VME card. Software communication with the card is done by reading and writing to 12 16-Bit registers. Any controller card such as an imbedded PC card that allows register communication can access the card.

The 'C' library included with the SDC-36017 card, simplifies the communication by doing the necessary bit manipulation and register mapping. This higher level abstraction allows for the end user's concentration on the application software, not on hardware level code.

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2.0 Configuring the SDC-36017 VXI/VME Card

2.1 Convertor Jumper Blocks

Each of the four converter channels are electrically identical but can be jumper programmed independently for different options. The heart of each of the four channels is DDC's RDC-19222 Monolithic Resolver-to-Digital converter. For detailed converter operation consult the RDC-19222 data sheet.

Configuration of the SDC-36017 is done using jumper pins. LA (Logical Address) Selection is done using a Dip switch package. Refer for Figure 1 for the placements of the various jumper blocks associated with each convertor and the Dip switch package. Table 1 gives an index to the proper block number associated to a particular convertor.

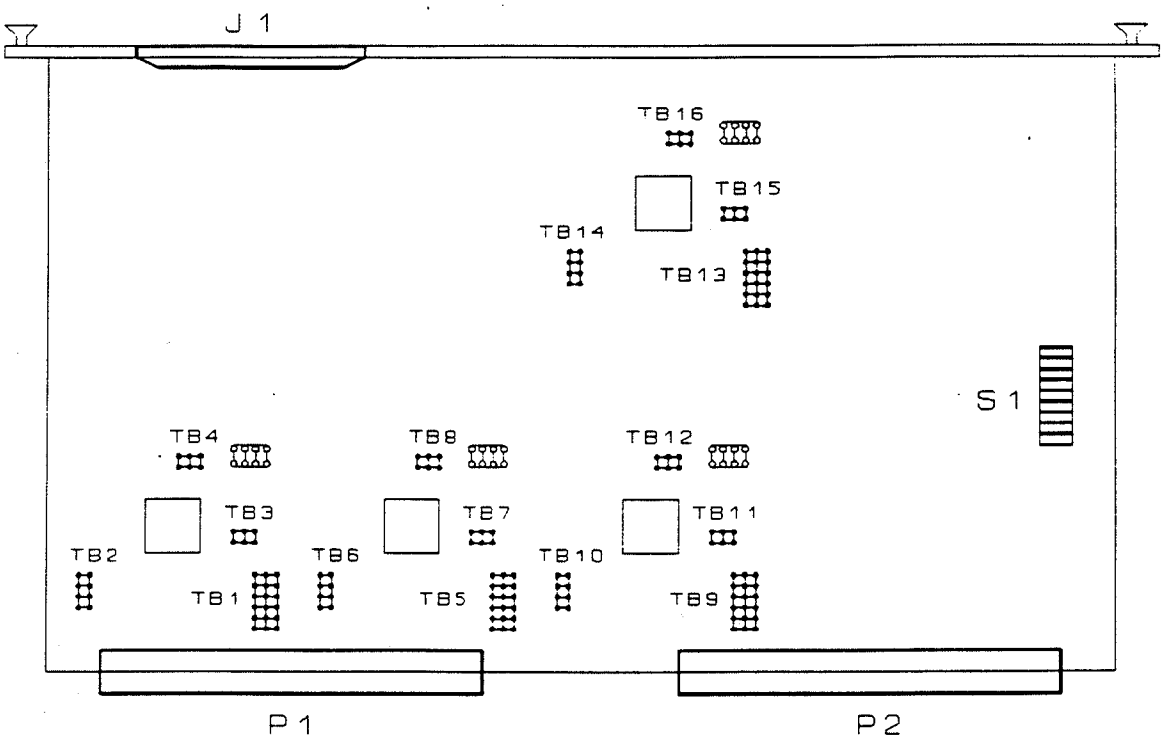


Figure 1.

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Channel	Input Mode	Resolution	Bandwith
1	TB1 TB2	TB3	TB4
2	TB5 TB6	TB7	TB8
3	TB9 TB10	TB11	TB12
4	TB13 TB14	TB15	TB16

Table 1.

2.1.1 Input Mode Jumper Connections

The input mode of each convertor (Synchro/Resolver) is set using a combination of two table blocks. Refer to Table 2 for the jumper configurations for blocks 1, 5, 9 and 13. Refer to Table 3 for the jumper configurations of blocks 2, 6, 10, and 14.

N/C = No Connect

Mode	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 12
Synchro	13	14	15	16	17	18
Resolver	1	2	3	N/C	N/C	N/C

Table 2.

Mode	Pin 1	Pin 2	Pin 3	Pin 4
Synchro	5	6	N/C	N/C
Resolver	5	6	N/C	N/C

Table 3.

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The below example sets up Synchro mode on channel 1 of the SDC-36017 VXI/VME card. Please note the jumper connections.

TB1

1	7	13
2	8	14
3	9	15
4	10	16
5	11	17
6	12	18

TB2

1	5
2	6
3	7
4	8

2.1.2 Channel Resolution Jumper Connections

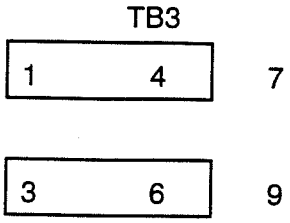
The resolution of each channel can be programmed to be 10, 12, 14, or 16 Bits in Synchro or Resolver mode. The resolution is selected with terminal block 3, 7, 11 and 15. Refer to Tables 4 for the jumper configuration information.

Resolution	Mode	Pin 4	Pin 6
10 Bit	Synchro/Resolver	1	3
12 Bit	Synchro/Resolver	1	N/C
14 Bit	Synchro/Resolver	N/C	3
16 Bit	Synchro/Resolver	N/C	N/C

Table 4.

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The below example sets up channel 1 for 10 Bit Resolution with the SDC-36017 card in Synchro or Resolver mode. Please note the jumper connections.



2.1.3 Bandwidth Options

Each channel also contains three jumper programmable bandwidth options. As of July 1996 (serial number 91 and higher), the bandwidth options on the SDC-36017 are Low (15 Hz), High (100 Hz), and User Installed. Prior to July 1996 (serial numbers less than 91) the bandwidth options on the SDC-36017 are Low (100 Hz), High (500 Hz), and User Installed.

The bandwidth option for each channel is configured using jumper block 4, 8, 12 and 16. For the user installed option, the bandwidth component values are determined by the end user and installed onto the SDC-36017 circuit card assembly.

Refer to Table 5A for units with a serial number less than 91. Refer to Table 5B for units with a serial number of 91 or greater than 91.

TABLE 5A.

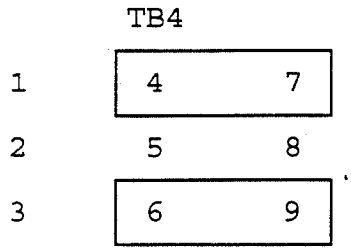
Bandwidth	Pin 4	Pin 6
100 Hz	7	9
500 Hz	1	3
CUSTOM	N/C	N/C

TABLE 5B.

Bandwidth	Pin 4	Pin 6
100 Hz	7	9
15 Hz	1	3
CUSTOM	N/C	N/C

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The below example sets up channel 1 for the 100 Hz bandwidth setting. Please note the jumper connections.



NOTE:

User selected bandwidth components must NOT be installed in board when factory high/low bandwidth settings are to be used. Software has been created for component selection of custom bandwidth's. Please contact the factory for ordering of the RDC-19220 component selection utility.

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2.2 Logical Address Selection

The A16 addressing option should be used with the SDC-36017 VXI/VME card. Access of the card is done with register addressing with a Base and offset format. The base or Logical Address (LA) switch is a 10 position DIP switch located on the SDC-36017 printed circuit card assembly. This switch is preset at the factory to the logical address of 2 as shown in Table 6. This table should be used as a reference in selection of a logical address from 0x00 thru 0xFF.

The SDC-36017 is a static configuration, slave device and should not be assigned to Logical Address 0 or 255 (0x00 , 0xFF) to avoid conflicting with other VXI instrumentation. Setting the Logical Address to 1 may also cause a problem as some Slot 0 controllers use this address.

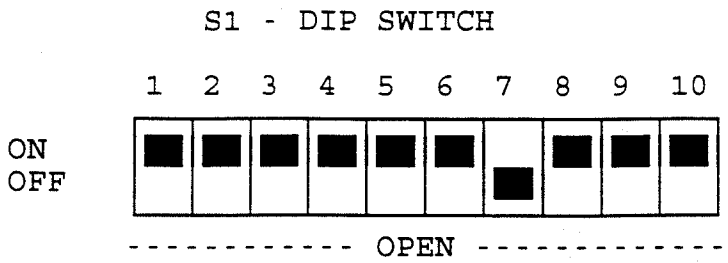
Each Register based VXI instrument is assigned a 64 byte memory area in the A16 address space. To decode these 64 bytes requires the use of the lower address bits (05 and lower). The Logical Address utilizes the next 8 address bits (13 to 06) and address bits 15 and 14 are defined by the VXI specification to be the logic 1 state.

Switch Position	OFF (OPEN)	ON	VALUE
SW10	-	-	-
SW9	-	-	-
SW8	LOGIC 1	LOGIC 0	1
SW7	LOGIC 1	LOGIC 0	2
SW6	LOGIC 1	LOGIC 0	4
SW5	LOGIC 1	LOGIC 0	8
SW4	LOGIC 1	LOGIC 0	16
SW3	LOGIC 1	LOGIC 0	32
SW2	LOGIC 1	LOGIC 0	64
SW1	LOGIC 1	LOGIC 0	128

Table 6.

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The below example sets the SDC-36017 VXI/VME card to the Logical Address of 2. Please note the DIP Switch positions.



2.3 P1 and P2 VXI Interface Connectors

The SDC-36017 requires only the P1 connector of the VXI backplane; signal connections are listed in Table 7. The convertor I/O signals are brought off the SDC-36017 through a 50 pin D type connector (J1) mounted on the front panel. The signal connections are listed in Table 8. These signal are always present on the J1 connection. They can also be routed to the VME P2 connector; This should be used for VME applications only. Jumper blocks P3 through P8 are used to select the lines to be routed through he P2 connector.

2.4 Timing Requirements

All data to and from the SDC-36017 card is transferred through standard Read/Write cycles, however the following precautions must be taken.

If an angular step input is applied to the Measurement section, enough time must be allocated to allow the tracking converter to reacquire the input angular position. This could take up to 500 ms for a 180 degrees step. During this time the *SM BIT signal may be asserted.

For some high speed applications, if a National Instruments VXI-MXI interface or equivalent is being used, small timing delays may be found in the communication between the SDC-36017 card and the controlling PC. For more detailed information please consult the factory.

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VXI/VME P1 CONNECTOR PIN FUNCTIONS

PIN	ROW A	ROW B	ROW C
1	D00	-	D08
2	D01	-	D09
3	D02	-	D10
4	D03	*BG0IN	D11
5	D04	*BG0OUT	D12
6	D05	*BG1IN	D13
7	D06	*BG1OUT	D14
8	D07	*BG2IN	D15
9	GND	*BG2OUT	GND
10	SYSCLK	*BG3IN	-
11	GND	*BG3OUT	*BERR
12	*DS1	-	*SYSRESET
13	*DS0	-	*LWORD
14	*WRITE	-	AM5
15	GND	-	-
16	*DTACK	AM0	-
17	GND	AM1	-
18	*AS	AM2	-
19	GND	AM3	-
20	*IACK	GND	-
21	*IACKIN	-	-
22	*IACKOUT	-	-
23	AM4	GND	A15
24	A07	-	A14
25	A06	-	A13
26	A05	-	A12
27	A04	-	A11
28	A03	-	A10
29	A02	-	A09
30	A01	-	A08
31	-12V	-	+12V
32	+5V	+5V	+5V

TABLE 7.

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VXI/VME J1 SIGNAL CONNECTOR

SIGNAL	J1	JUMPERS	P2
1S1	19	TB19 1-16	C16
1S2	37	TB19 2-15	C17
1S3	18	TB19 3-14	A17
1S4	36	TB19 4-13	A18
1RH	17	TB19 5-12	C18
1RL	35	TB19 6-11	A19
1VEL	16	TB19 7-10	C19
1A GND	34	TB19 8-9	A20
2S1	15	TB20 1-16	C11
2S2	33	TB20 2-15	A12
2S3	14	TB20 3-14	C12
2S4	32	TB20 4-13	A13
2RH	13	TB20 5-12	C13
2RL	31	TB20 6-11	A14
2VEL	12	TB20 7-10	C14
2A GND	30	TB20 8-9	A15
3S1	11	TB21 1-16	C6
3S2	29	TB21 2-15	C7
3S3	10	TB21 3-14	A7
3S4	28	TB21 4-13	A8
3RH	9	TB21 5-12	C8
3RL	27	TB21 6-11	A9
3VEL	8	TB21 7-10	C9
3A GND	26	TB21 8-9	A10
4S1	7	TB22 1-16	A3
4S2	25	TB22 2-15	A2
4S3	6	TB22 3-14	A1
4S4	24	TB22 4-13	A4
4RH	5	TB22 5-12	C4
4RL	23	TB22 6-11	C3
4VEL	4	TB22 7-10	C2
4A GND	22	TB22 8-9	C1
PA OUT	3	TB18 1-6	C22
OS GND	21	TB18 2-5	C23
DIGITAL GND	2	TB18 3-4	C24
B6		TB17 1-16	C25
B7		TB17 2-15	C26
B8		TB17 3-14	C27
B9		TB17 4-13	C28
B10		TB17 5-12	C29
B11		TB17 6-11	C30
B12		TB17 7-10	C31
B13		TB17 8-9	C32

TABLE 8.

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2.5 Reference Oscillator

The Reference Oscillator is completely software programmable for both the Frequency and Amplitude of the Oscillator through 8 bit binary values contained in the on-card registers. The Frequency of the Oscillator can be programmed from 320 to 10,200 Hz in 40 Hz steps, and the Amplitude of the Oscillator can be programmed from 0 Vrms to 6.6 Vrms in 26 mVrms steps. The Oscillator can supply up to 100 mA rms of current and is short circuit and transient protected. The short circuit current limit is set for 170 mA Peak (typical). The frequency and amplitude of the oscillator are accurate to within ± 10 %. At Power-Turn-On the initial setting of the Oscillator is undefined, any voltage and frequency combination may be present at this time.

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3.0 Software Control of the SDC-36017 VXI/VME Card

3.1 Memory Map

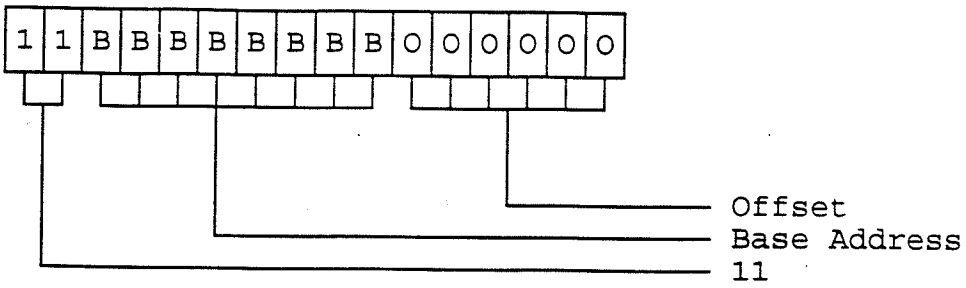
Each Register based VXI instrument is assigned a 64 byte memory area in the A16 address space. To decode these 64 bytes requires the use of the lower address bits (05 and lower). The lower bits are considered the offset of the memory address. The Logical Address utilizes the next 8 address bits (13 to 06) . These bits can be considered the base address. The offset added to the base address allows a specific memory location to be accessed. Since 16 bit words are used with the SDC-36017 card, the offsets increment by 2. Refer to Table 9 for a complete description of the memory offsets.

HEX Offset	READ	WRITE
00	ID REGISTER	NOT USED
02	DEVICE TYPE	NOT USED
04	STATUS REGISTER	CONTROL REGISTER
06	SM#1 ANGLE	NOT USED
08	SM#2 ANGLE	NOT USED
0A	SM#3 ANGLE	NOT USED
0C	SM#4 ANGLE	NOT USED
0E	NOT USED	NOT USED
10	EXTENDED MODEL NO.	OSCILLATOR FREQUENCY
12	NOT USED	OSCILLATOR LEVEL

Table 9.

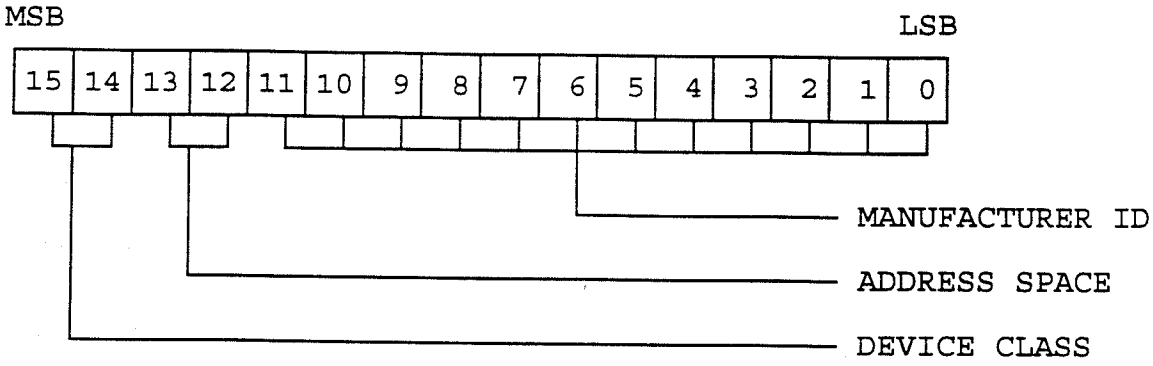
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An example of the creation of a Register address is explained below.



3.2 Register Mapping

3.2.1 ID REGISTER



The ID REGISTER gives information on the manufacture, address space, and device class of the card. Reading this register of the SDC-36017 card will give the following data.

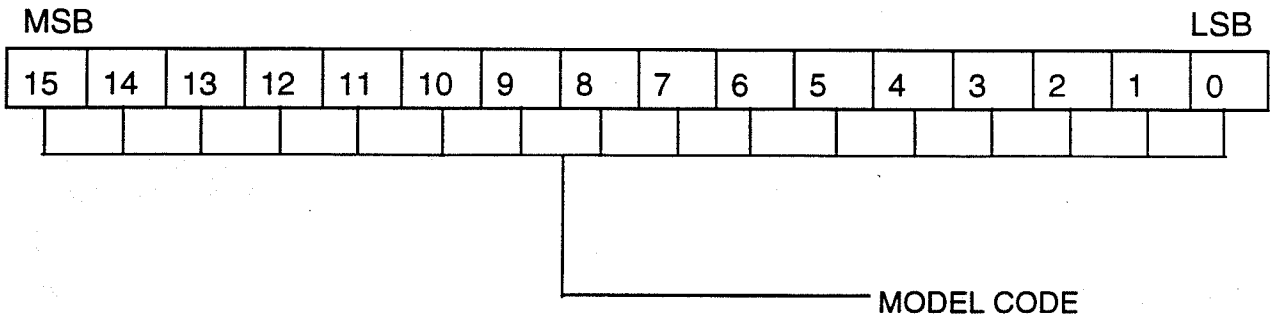
(BITS 15-14) DEVICE CLASS - Both bits are set to a logic 1 to define a Register Based VXI Device.

(BITS 13-12) ADDRESS SPACE - Both bits are set to logic 1 to define an A16 Only VXI Device.

(BITS 11-0) MANUFACTURER ID - Contains DDC's manufacturer ID number. 4072 (0xFE8)

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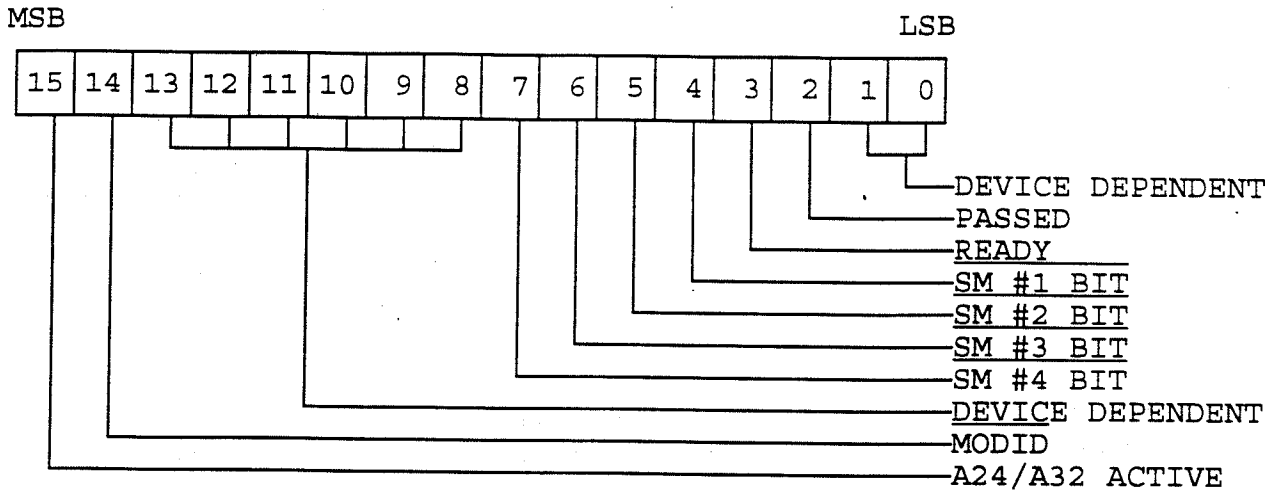
3.2.2 DEVICE TYPE REGISTER



The DEVICE TYPE REGISTER gives information on the model number of the VXI instrument. Reading this register will return F19A h.

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3.2.3 STATUS REGISTER



The STATUS REGISTER gives information on the status of the SDC-36017 card. Reading this register will return data reflecting the current state of the following card conditions.

(BIT 15) A24/A32 ACTIVE - Permanently set to 1 since A16 is used.

(BIT 14) $\overline{\text{MODID}}$ - Not supported, Permanently set to 1.

(BITS 13-8) DEVICE DEPENDENT - Permanently set to 1.

(BITS 7-4) $\overline{\text{SM \#N BIT}}$ - These N bits where N = 1 to 4 are normally at a logic 1 state. These bits will go to logic 0 if the associated Signal Measurement section N is unable to track the input Synchro/Resolver signal. This can happen if the Synchro/Resolver input is rotating too fast, or if the input is missing altogether. This bit may also go to logic 0 momentarily if a step input is applied to the converter.

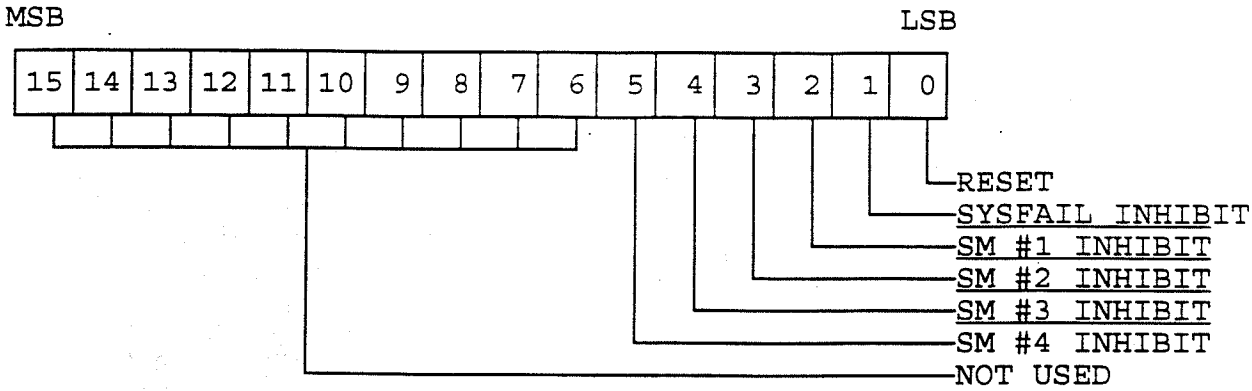
(BIT 3) READY - Permanently set to a logic 1.

(BIT 2) PASSED - Permanently set to a logic 1.

(BITS 1-0) DEVICE DEPENDENT - Permanently set to a logic 1.

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3.2.4 CONTROL REGISTER



The DEVICE TYPE REGISTER gives information on the status of the SDC-36017 card. Reading this register will return data reflecting the current state of the following card conditions.

(BITS 15-6) NOT USED - N/C

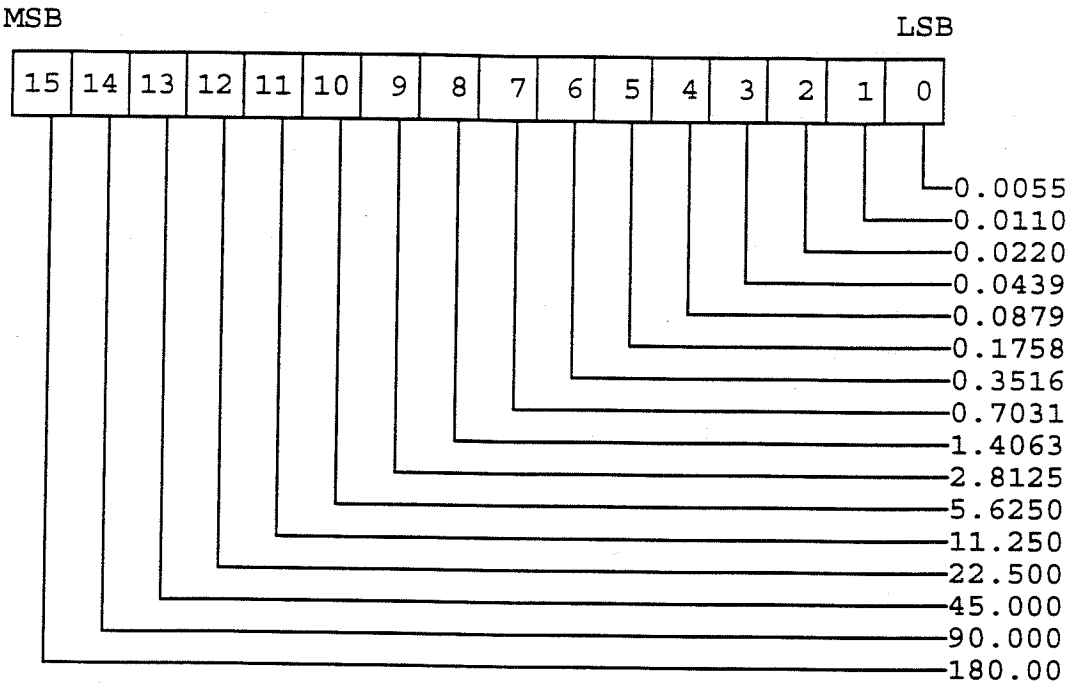
(BITS 5-2) SM #N INHIBIT - These N bits where N = 1 to 4. A logic 0 on any of these bits inhibits the associated converter. This feature can be used to time synchronize the converters to external events or to each other. These bits must be set to the logic 1 in order for the converters to track the input Synchro/Resolver signals.

(BIT 1) SYSFAIL INHIBIT - Not Used - N/C

(BIT 0) RESET - A logic 1 on this bit will reset the SDC-36017 to the power-on state. This bit should normally be set to logic 0. NOTE: it is not necessary to clear this bit after setting it. The act of writing the logic 1 to the bit position initiates the card reset which internally clears the bit back to logic 0 with 125 ns.

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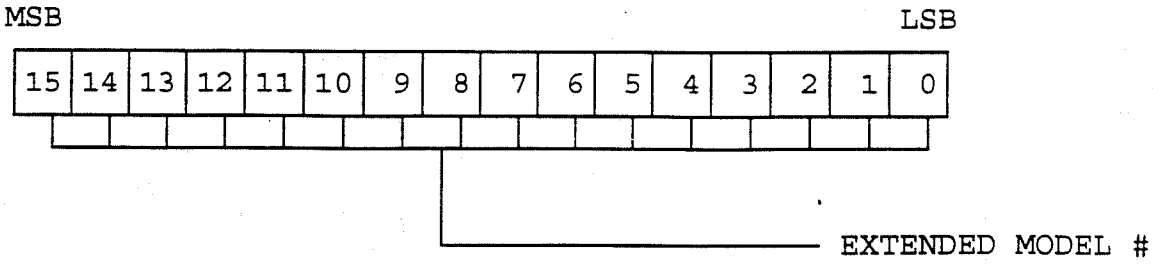
3.2.5 SM #N ANGLE REGISTER



The SM #N REGISTER gives the current binary angular data read from the RDC-19222 Convertors. To ensure this data is valid through the read cycle, the channel that is to be read should be inhibited before the read is done. This ensure the binary data is latched and will remain consistent during the read cycle. The channel should be un-inhibited if continued tracking is desired after the read. The bits reflect binary weights which equate to the decimal angle. For resolution mode lower than 16 bits, the unused LSB bits should be masked from the binary angle before conversion since these bits are invalid and should be ignored.

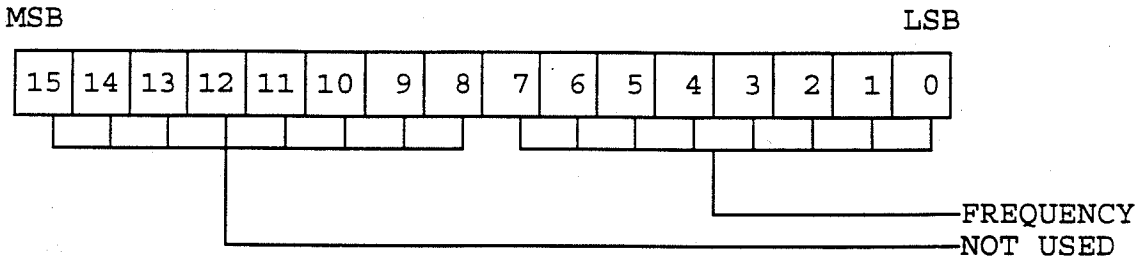
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3.2.6 EXTENDED MODEL# REGISTER



The reading the EXTENDED MODEL# REGISTER gives DDC's extended model number for the card.

3.2.6 OSCILLATOR FREQUENCY REGISTER



(BITS 7-0) OSCILLATOR FREQUENCY - The value of this byte controls the frequency of the Reference Oscillator. The frequency of the oscillator (+-10%) is related to this binary value by the following formula:

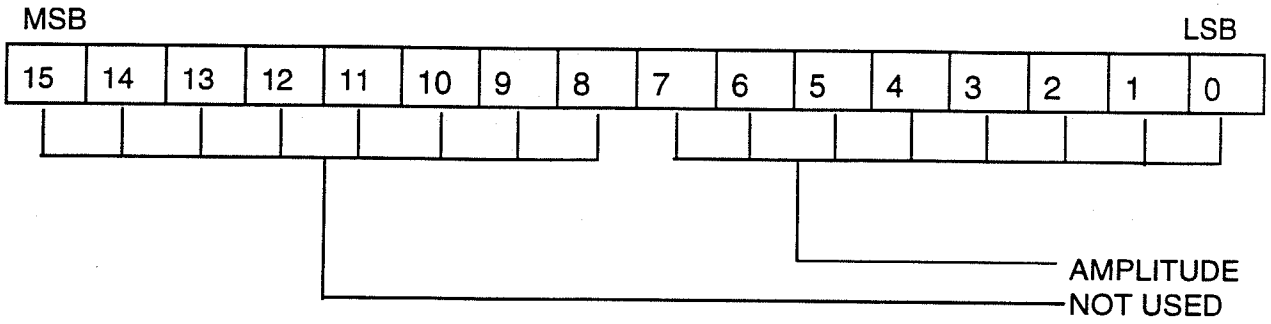
Oscillator Frequency (Hz) = binary value * 40 Hz

NOTE:

Programming the oscillator for frequencies less than 320 Hz will not damage the oscillator, however the operating characteristics are not guaranteed to be within +-10% of the programmed value.

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3.2.7 OSCILLATOR AMPLITUDE REGISTER



(BITS 7-0) OSCILLATOR AMPLITUDE - The value of this byte controls the amplitude of the Reference Oscillator. The amplitude of the oscillator (± 10 %) is related to this binary value by the following formula:

Oscillator Amplitude (Vrms) = binary value * 0.026 Vrms

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3.3 Register Programming the SDC-36017

3.3.1 Initializing the SDC-36017

When the SDC-36017 card is first powered up, the control status of the card and the characteristics of the internal reference generator is undefined. The following steps should be done before valid angular data should be read from the card.

The following description assumes the card is at address 0x02 and uses the National Instruments MXI-VXI register interface commands in the VIC command line programmer.

1. Read ID REGISTER

vxiin 1, 0xC080, 2

(returns)
value = 0xFFE8

2. Read DEVICE TYPE

vxiin 1, 0xC082, 2

(returns)
value = 0xF19A

3. Set CONTROL register to un-inhibit all channels.

vxiout 1, 0xC084, 2, 0x003C

4. Set the oscillator FREQUENCY to 0

vxiout 1, 0xC090, 2, 0x0000

5. Set the oscillator AMPLITUDE to 0

vxiout 1, 0xC092, 2, 0x0000

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3.3.1 Data from the SDC-36017

Since all the channels were set to the un-inhibit condition, the converters are currently tracking the Synchro/Resolver input. Valid data can be read from the convertor. The BIT, built in test lines coming from the convertors can be tested by first supplying the reference signals (to spec) and issuing the following command.

vxiin 1, 0xC084, 2

This should return the following if a valid reference is present:

value = 0xFFFF

The following is returned if the reference signal is too low or not present on any of the channels:

value = 0xFF0F

If the BIT test works, the convertors can be tested by supplying a valid reference and passing in a Synchro/Resolver signal of 90.000 degrees. The following command will read the angle from convertor number 1.

vxiin 1, 0xC086, 2

(returns angular data)
value = 0x4000

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Module Name: SDC36017 (include)
Compiler: BCC version 3.1

(1994) ILC Data Device Corp.

```
int             SDC36017_Initialize (int);
void            SDC36017_inhibit (int);
void            SDC36017_track (int);
int             SDC36017_Read_bite (int);
unsigned int    SDC36017_Read_angle (int);
int             SDC36017_Close (void);
```


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Module Name: SDC36017 (code)
Compiler: BCC version 3.1

(1994) ILC Data Device Corp.

```
#include "sdc36017.h"
#include <nivxi.h>

unsigned int    SDC36017_Address    = 0x0000;
unsigned int    SDC36017_Init       = 0;
unsigned int    SDC36017_Control    = 0;
unsigned int    reg_temp            = 0;


int  SDC36017_Initialize (int address)
{
        SDC36017_Address    = (0xC000|(address<<6));
        SDC36017_Init       = 1;
        SDC36017_Control    = 0x003C;
        VXIout(1,SDC36017_Address+0x4,2,SDC36017_Control);
        return (0);
}


void SDC36017_inhibit (int channel)
{
        if (SDC36017_Init)

                {SDC36017_Control&=(~(1<<(channel+2)));
                VXIout(1,SDC36017_Address+0x4,2,SDC36017_Control);}
}


void SDC36017_track (int channel)
{
        if (SDC36017_Init)

                {SDC36017_Control&=(~(1<<(channel+2)));
                SDC36017_Control|=(1<<(channel+2));
                VXIout(1,SDC36017_Address+0x4,2,SDC36017_Control);}
}
```


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Module Name: SDC36017 (code)
Compiler: BCC version 3.1

(1994) ILC Data Device Corp.

```
int SDC36017_Read_bite (int channel)
{
        if (SDC36017_Init)

                {VXIin(1,SDC36017_Address + 0x4,2,&reg_temp);
                 if (reg_temp&(1 < <(channel + 4))) return 1; else return 0;}

        return 0;
}


unsigned int SDC36017_Read_angle (int channel)
{
        if (SDC36017_Init)

                {VXIin(1,((SDC36017_Address + 0x6) + (channel*0x2)),2,&reg_temp);
                return (reg_temp);}

        return 0;
}


int  SDC36017_Close ()
{
        SDC36017_Address    = 0x0000;
        SDC36017_Init       = 0;
        SDC36017_Control    = 0;
        return (0);
}
```


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