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Delphi Engineering Group, Inc.

ADC3255

User Manual

Version 1.30

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1 ABOUT THIS DOCUMENT

This manual describes the operation and use of the ADC3255, 2 Gsps Data Acquisition Board.

1.1 Document Revision History

Revision	Date	Changes
1.00	10/06/2006	Initial Release.
1.10	12/14/2006	Updated “Problematic DeMux Clock Delay Values Over Clock Input Range” Table.
1.20	01/18/2007	Added Board Configuration section (including PLL documentation). Corrected front panel connector documentation.
1.30	04/28/2008	Revised Top Level Block Diagram. Revised Trigger Timing Diagram. Added PCI interface details. Added PLL Reference details. Added Configuration Jumpers section. Corrected some DMA Register bit field definitions. Added DMA Limitations section.

Table 1 – Document Revision History

1.2 Conventions

This document uses the following conventions:

- When referring to the state of a bit or bits, set indicates a logical one and clear indicates a logical zero.
- This document prefixes hexadecimal values with the characters “0x”, such as with 0x0 and 0x100008FD.
- Addresses are defined in terms of bytes unless otherwise specified.

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1.3 Acronyms

Acronym	Definition
ADC	Analog to Digital Converter
BAR	Base Address Register
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ISR	Interrupt Service Routine
KB	Kilobyte
MB	Megabyte
PCI	Peripheral Component Interconnect
PCI-X	Peripheral Component Interconnect Extended
PMC	PCI Mezzanine Card
PMC-X	PCI-X PMC

Table 2 – Acronyms

2 BOARD OVERVIEW

The ADC3255 is a PMC-X (PCI-X PMC) 10-bit analog to digital converter board with a customizable onboard Xilinx Virtex 4 FPGA. Buffering of the digitized data is provided onboard via a 64 KB, dual-port RAM which is internal to the FPGA and is capable of operating as a circular buffer for realtime continuous data flow. A 128 or 256 MSample DRAM buffer is also present onboard. The board is capable of sampling at rates of 200 Msps up to 2 Gsps. The host board can read the buffered sample data through the PCI bus.

2.1 Board Architecture

The heart of the board is the Atmel 10-bit ADC, which operates at a clock rate of up to 2 GHz. From the ADC, the converted data stream is sent to a matching DeMux chip. The DeMux chip broadens the data stream and sends it across a double data rate, 40-bit wide bus at 1/4th the input clock frequency. This bus then feeds into the FPGA where it is buffered in the FPGA's internal RAM and optionally can be simultaneously buffered in the board's DRAM. The FPGA's clock is supplied from the board clock signal but is divided down to 1/8th the board clock rate. The FPGA also provides the PCI access to the host board. Peripheral components provide reset, trigger, clock processing, and FPGA configuration.

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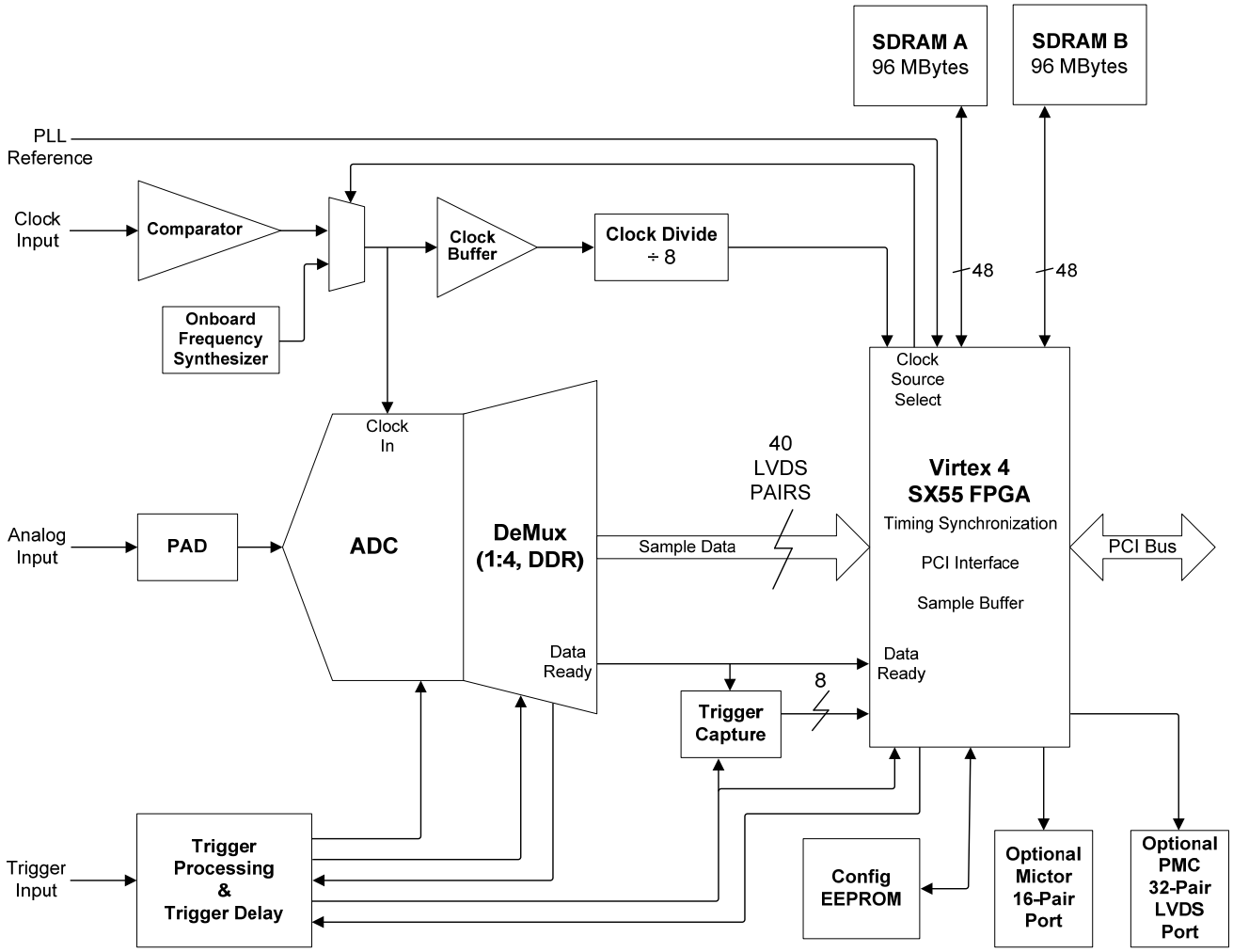


Figure 1 - ADC3255 Top Level Block Diagram

3 REQUIREMENTS

3.1 Power Requirements

All power to the ADC3255 is provided through the PMC connectors. The host system must be able to provide adequate current levels to the board.

Typical +3.3V current draw: 1.80 Amps
Typical +5V current draw: 4.15 Amps

3.2 Cooling Requirements

The ADC3255 must be cooled either by conduction or by convection to prevent damage to the board and ensure normal operation. The following requirements must be met to ensure adequate cooling.

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Convection Cooled:
Minimum Air Flow: 400 LFM
Ambient Air Temperature (Commercial)*: 0°C to +50°C
Ambient Air Temperature (Industrial)*: -40°C to +70°C

Conduction Cooled:
Cold Wall Temperature (Commercial): 0°C to +65°C
Cold Wall Temperature (Industrial): -40°C to +80°C

*0-90% RH Non-Condensing.

4 HARDWARE INTERFACES

4.1 Front Panel Inputs

All front panel I/O connectors are SMA female type and have 50 ohms impedance terminated to ground. Signals are AC coupled onboard after the termination.

4.1.1 Analog Input

Maximum signal amplitude before clipping occurs is approximately 0 dBm when the board's gain adjustment is at the default level. Analog input gain is adjustable via a board register. Input signal bandwidth is from 100 KHz to 3.0 GHz (-3 dB).

4.1.2 Clock Input

Input clock power range is -10 dBm to +10 dBm. A clock input signal is required for the operation of the board unless the onboard PLL is used to provide the board's clock. The supplied clock input signal is buffered and scaled down for use as the FPGA clock (FPGA Clock = Clock Input / 8). ADC clock phase is adjustable via a board register.

4.1.3 PLL Reference

Input must be a sine wave or square wave, with an amplitude range of -2 dBm to +10 dBm at 50 MHz, with a 50% duty cycle. The ADC3255 also has an onboard PLL reference which can be enabled instead of using the external PLL reference. Configuration of onboard/external PLL reference is done via a board register.

4.1.4 Trigger Input

Input must be a 1V to 3.3V peak to peak signal with a rise time of 10-90% < 10 ns. A trigger event is initiated by a positive transition on the trigger input. At the end of a capture event, the trigger circuitry is again reset to wait for another trigger event. Trigger delay and threshold are adjustable via board registers.

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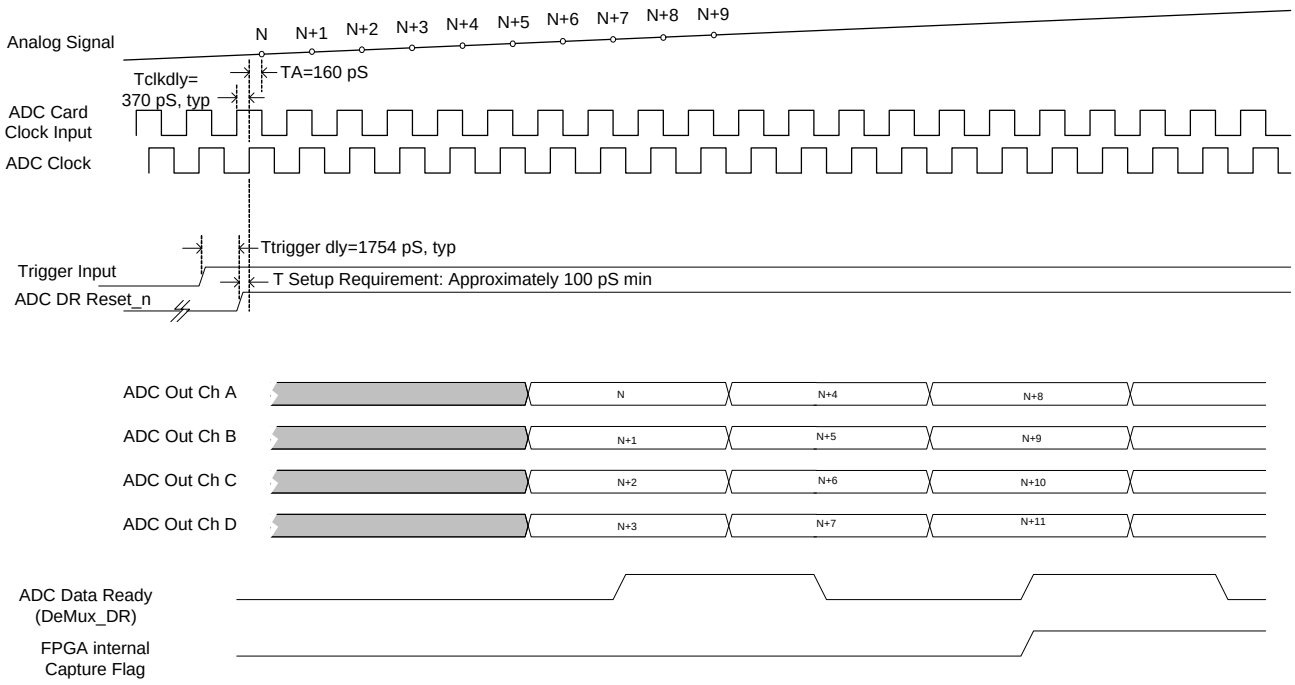


Figure 2 - Trigger Timing

4.2 PCI Interface

The board mates with a PMC/PMC-X connector on the host board and uses 3.3V signaling. This interface supplies all the communication for initialization and configuration data for the board, from and to the host. The board obtains the power needed to operate from the PMC connectors exclusively. It operates using +3.3V and +5V as provided through the PMC connectors.

Operating in PCI-X mode, the interface conforms to the PCI-X 2.0 Mode 1 standard. Bus configuration is 64-bits with speeds of 100/66 MHz. Operation in PCI-X mode at 133 MHz is not officially supported because data integrity cannot be guaranteed across the board's temperature range at this speed.

Operating in PCI mode, the interface conforms to the PCI 3.0 standard. Bus configuration is 64/32-bits with speeds up to 33 MHz. Operation in PCI mode at 66 MHz is not officially supported because data integrity cannot be guaranteed across the board's temperature range above 33 MHz.

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4.3 LEDs

Several LEDs are present on the board, providing visual feedback regarding the board's state.

LED	Color	Designation	Description
LED1	Green	FPGA Running LED	Turns on when the FPGA finishes loading firmware and is running.
LED2	Green	PLL Lock LED	Turns on when PLL has locked onto its reference signal.
LED3	Red	FPGA RAM Collision Full LED	Turns on when an FPGA RAM full collision has occurred, and turns off when the FPGA RAM Collision Full bit in register 1 is cleared.
LED4	Green	Input Clock LED	Toggles when Input Clock is present. Toggle rate is proportional to Input Clock rate.
LED5	Green	PCI Clock LED	Toggles when PCI Clock is present. Toggle rate is proportional to PCI Clock rate.

Table 3 – LEDs

4.4 Configuration Jumpers

Several jumpers are present on the board, providing various configuration options.

Jumper	Designation	Description
JP1	Reserved	Reserved.
JP2	Force 66 MHz PCI-X	When installed, forces the device to run at 66 MHz in PCI-X mode. This jumper has no effect in PCI mode.
JP3	Reserved	Reserved.
JP4	Reserved	Reserved.
JP5	PCI-X Disable	When installed, forces PCI mode by disabling PCI-X capability on the device.
JP6	Reserved	Reserved.

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5 PCI INTERFACE

5.1 Base Address Registers

5.1.1 BAR 0 (FPGA RAM)

PCI Base Address Register 0 (BAR0) is the location of FPGA RAM. For PCI burst read access, the internal address counter is automatically incremented. Full-length burst mode is supported. The size of the FPGA RAM is 64 KB. FPGA RAM is dual-port and as such can be read from while sample data is being written to it. The FPGA RAM has the capability of being used as a circular buffer (see register 1 and register 6 definitions).

FPGA RAM is mapped as follows:

First byte of FPGA RAM = BAR0 Address + 0
Last byte of FPGA RAM = BAR0 Address + 0xFFFF

5.1.2 BAR 1 (DRAM)

PCI Base Address Register 1 (BAR1) is the location of the DRAM buffer. For PCI burst read access, the internal address counter is automatically incremented. Full-length burst mode is supported. The actual size of the DRAM is 192 MB however; the DRAM is mapped as a 256 MB window from the PCI bus. The DRAM buffer holds up to 128 MSamples. The DRAM cannot be read from while sample data is being written to it. For boards with the 384 MB DRAM option, double the values listed in this document as appropriate.

DRAM is mapped as follows:

First byte of DRAM = BAR1 Address + 0
Last byte of DRAM = BAR1 Address + 0x0FFF FFFF

5.1.3 BAR 2 (Registers)

Base Address Register 2 (BAR2) is used to access control and status information. It consists of several registers that are each 32 bits wide and addressed as follows:

Register 1 Address = BAR2 address + 8 (0x8)
Register 2 Address = BAR2 address + 16 (0x10)
Register 3 Address = BAR2 address + 24 (0x18)
Register 4 Address = BAR2 address + 32 (0x20)
Register 5 Address = BAR2 address + 40 (0x28)
Register 6 Address = BAR2 address + 48 (0x30)
Register 7 Address = BAR2 address + 56 (0x38)
Register 8 Address = BAR2 address + 64 (0x40)
Register 9 Address = BAR2 address + 72 (0x48)
Register 10 Address = BAR2 address + 80 (0x50)
Register 11 Address = Reserved
Register 12 Address = BAR2 address + 96 (0x60)
Register 13 Address = BAR2 address + 104 (0x68)
Register 14 Address = BAR2 address + 112 (0x70)

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Register 15 Address = BAR2 address + 120 (0x78)
Register 16 Address = Reserved
Register 17 Address = Reserved
Register 18 Address = BAR2 address + 144 (0x90)

5.2 Registers

5.2.1 Register 1 (Board Control/Status)

PCI Address	BAR2 + 0x8							
Designation	Test Pattern Data	Clear Address Counters	DeMux Test Data	Data Endianness	Enable Bit Packing	Ignore FPGA RAM Full	Auto Trigger	Pause Capturing
Bit(s)	7	6	5	4	3	2	1	0
Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PCI Address	BAR2 + 0x8					
Designation	FPGA RAM Active Address	Reserved	FPGA RAM Collision Full	FPGA RAM Empty	FPGA RAM Near Empty	Capturing Event
Bit(s)	31-16	15-12	11	10	9	8
Mode	R	R	R/W	R	R	R

Pause Capturing

Configures whether the capturing process is running or paused.

0 = Capturing process can run.
1 = Capturing process is paused.

Auto Trigger

When set, input from the external trigger is ignored and triggers are automatically generated internally by the FPGA as soon as a capture event is complete. When clear, external trigger is used.

Ignore FPGA RAM Full

If FPGA RAM becomes full and this bit is set, data will continue to be captured to FPGA RAM while the Pause Capturing bit is still clear. If FPGA RAM becomes full and this bit is clear, data will stop being captured to FPGA RAM even if the Pause Capturing bit is still clear.

Enable Bit Packing

Configures the bit packing option.

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0 = Bit packing is disabled.
1 = Bit packing is enabled.

Data Endianness

When set, data read from BAR0 and BAR1 is little endian. When clear, data read from BAR0 and BAR1 is 16-bit big endian.

DeMux Test Data

When set, DeMux test data is used as input.

Clear Address Counters

When set, the FPGA RAM Active Address and DRAM Active Address are reset to zero. This bit is ignored unless the Pause Capturing bit is set.

Test Pattern Data

When set, test pattern data is used as input.

Capturing Event

If true, a capture event is currently in progress. This bit is set when a trigger event occurs, and is cleared after the stop vector is reached.

FPGA RAM Near Empty

If true, FPGA RAM has less than 8 KB of unread sample data.

FPGA RAM Empty

If true, FPGA RAM is empty.

FPGA RAM Collision Full

If true, FPGA RAM is at least 7/8th full. After the FPGA has set this bit, it can be cleared by the user.

FPGA RAM Active Address

Address within FPGA RAM that is currently active for writing new sample data.

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5.2.2 Register 2 (FPGA RAM Vectors)

PCI Address	BAR2 + 0x10	
Designation	FPGA RAM Stop Vector	FPGA RAM Start Vector
Bit(s)	31-16	15-0
Mode	R/W	R/W

FPGA RAM Start Vector

Determines the length of delay from a trigger event to the beginning of data capture for each FPGA RAM capture event.

FPGA RAM Stop Vector

Determines the stopping point of data capture for each FPGA RAM capture event.

5.2.3 Register 3 (Board Configuration 1)

PCI Address	BAR2 + 0x18			
Designation	Clock Phase	Trigger Threshold	DeMux Clock Delay	Reserved
Bit(s)	31-24	23-16	15-8	7-0
Mode	R/W	R/W	R/W	R/W

DeMux Clock Delay

Adjusts the data clocking delay between the ADC and DeMux.

Trigger Threshold

Adjusts the board's trigger threshold.

Clock Phase

Adjusts the board's clock phase.

5.2.4 Register 4 (DRAM Start Vector)

PCI Address	BAR2 + 0x20
Designation	DRAM Start Vector
Bit(s)	31-0
Mode	R/W

DRAM Start Vector

Determines the length of delay from a trigger event to the beginning of data capture for each DRAM capture event.

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5.2.5 Register 5 (DRAM Stop Vector)

PCI Address	BAR2 + 0x28
Designation	DRAM Stop Vector
Bit(s)	31-0
Mode	R/W

DRAM Stop Vector

Determines the stopping point of data capture for each DRAM capture event.

5.2.6 Register 6 (IRQ Status/Mask)

PCI Address	BAR2 + 0x30							
Designation	DRAM B Write Complete Status	DRAM A Write Complete Status	DRAM Full Status	DMA Complete Status	FPGA RAM Collision Full Status	FPGA RAM Collision Empty Status	FPGA RAM Partly Filled Status	Capture Event Complete Status
Bit(s)	7	6	5	4	3	2	1	0
Mode	R	R	R	R	R	R	R	R

PCI Address	BAR2 + 0x30	
Designation	Reserved	Capture Event Count Status
Bit(s)	15-9	8
Mode	R	R

PCI Address	BAR2 + 0x30							
Designation	DRAM B Write Complete Mask	DRAM A Write Complete Mask	DRAM Full Mask	DMA Complete Mask	FPGA RAM Collision Full Mask	FPGA RAM Collision Empty Mask	FPGA RAM Partly Filled Mask	Capture Event Complete Mask
Bit(s)	23	22	21	20	19	18	17	16
Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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PCI Address	BAR2 + 0x30
Designation	Capture Event Count Mask
Bit(s)	31-24
Mode	R/W

Capture Event Complete Status

If set, an interrupt was generated because a capture event has completed.

FPGA RAM Partly Filled Status

If set, an interrupt was generated because FPGA RAM has acquired 8 KB or more of sample data from the last read address.

FPGA RAM Collision Empty Status

If set, an interrupt was generated because a read from FPGA RAM has occurred before new sample data has been acquired.

FPGA RAM Collision Full Status

If set, an interrupt was generated because FPGA RAM has 8 KB or less of available space before colliding with the last read address.

DMA Complete Status

If set, an interrupt was generated because a DMA transfer has completed.

DRAM Full Status

If set, an interrupt was generated because DRAM has 1 MB or less of available space before reaching the last address of DRAM.

DRAM A Write Complete Status

If set, an interrupt was generated because DRAM memory A has completed writing data.

DRAM B Write Complete Status

If set, an interrupt was generated because DRAM memory B has completed writing data.

Capture Event Count Status

If set, an interrupt was generated because the number of capture events completed matches the 8-bit value in the Capture Event Count.

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Capture Event Complete Mask

When set, an interrupt will be generated when a capture event has completed.

FPGA RAM Partly Filled Mask

When set, an interrupt will be generated when FPGA RAM has acquired 8 KB of sample data or more from the last read address.

FPGA RAM Collision Empty Mask

When set, an interrupt will be generated when a read from FPGA RAM occurs before new sample data has been acquired.

FPGA RAM Collision Full Mask

When set, an interrupt will be generated when FPGA RAM has 8 KB or less of available space before colliding with the last read address.

DMA Complete Mask

When set, an interrupt will be generated when a DMA transfer has completed.

DRAM Full Mask

When set, an interrupt will be generated when DRAM has 1 MB or less of available space before reaching the last address of DRAM.

DRAM A Write Complete Mask

When set, an interrupt will be generated when DRAM A has completed writing data.

DRAM B Write Complete Mask

When set, an interrupt will be generated when DRAM B has completed writing data.

Capture Event Count Mask

If non-zero, an interrupt will be generated when the number of capture events completed matches this 8-bit value.

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5.2.7 Register 7 (DRAM Control/Status)

PCI Address	BAR2 + 0x38				
Designation	Reserved	DRAM Test Mode	Reserved	Ignore DRAM Full	Enable DRAM Capture
Bit(s)	7	6-4	3-2	1	0
Mode	R	R/W	R	R/W	R/W

PCI Address	BAR2 + 0x38					
Designation	DRAM Active Address	Reserved	DRAM Read Cache Updating	DRAM B Writing	DRAM A Writing	DRAM Full
Bit(s)	31-16	15-12	11	10	9	8
Mode	R/W	R	R/W	R	R	R/W

Enable DRAM Capture

When set, the device enables utilization of the DRAM buffer and utilizes the FPGA RAM and DRAM vectors when performing acquisition. If one set of vectors has a larger stop vector than the other, the capture process will continue until both sets of vectors are serviced. When clear, the DRAM buffer is disabled and only the FPGA RAM vectors are utilized for board control.

Ignore DRAM Full

If DRAM becomes full and this bit is set, data will continue to be captured to DRAM while the Pause Capturing bit is still clear. If DRAM becomes full and this bit is clear, data will stop being captured to DRAM even if the Pause Capturing bit is still clear.

DRAM Test Mode

Used to generate test data in DRAM.
000: Test Pattern disabled
001: Test Pattern 1 = 0x55
010: Test Pattern 2 = 0xAA
011: Test Pattern 3 = 0xFF
100: Test Pattern 4 = 0x00
111: User-Defined Pattern via DRAM Test Pattern in register 8

DRAM Full

If true, DRAM is at most 512 KB from being full.

DRAM A Writing

Indicates if DRAM A is currently writing.

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DRAM B Writing

Indicates if DRAM B is currently writing.

DRAM Read Cache Updating

Indicates if the DRAM Read Cache is currently being updated.

DRAM Active Address

Address within DRAM that is currently active for writing new sample data. This value corresponds to bits 26 through 12 of the current write address within DRAM.

5.2.8 Register 8 (DRAM Test Pattern)

PCI Address	BAR2 + 0x40	
Designation	DRAM Test Pattern	Reserved
Bit(s)	31-16	15-0
Mode	R/W	R

DRAM Test Pattern

User-definable data pattern that will be written to DRAM when DRAM Test Mode in register 7 is set to User-Defined Pattern. Data pattern will be written in place of acquired data during data capture.

5.2.9 Register 9 (Board Configuration 2)

PCI Address	BAR2 + 0x48		
Designation	Reserved	Trigger Delay	ADC Gain
Bit(s)	31-16	15-8	7-0
Mode	R	R/W	R/W

ADC Gain

Adjusts the board's ADC gain.

Trigger Delay

Adjusts the board's trigger delay.

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5.2.10 Register 10 (Board Temperature)

PCI Address	BAR2 + 0x50	
Designation	Reserved	Board Temperature
Bit(s)	31-12	11-0
Mode	R	R

Board Temperature

Temperature data. See Temperature/Data Relationship table for description.

5.2.11 Register 12 (DMA Source Address)

PCI Address	BAR2 + 0x60
Designation	DMA Source Address
Bit(s)	31-0
Mode	R/W

DMA Source Address

Specifies the beginning address within the DMA source from which the DMA operation will read.

5.2.12 Register 13 (DMA Destination Address)

PCI Address	BAR2 + 0x68
Designation	DMA Destination Address
Bit(s)	31-0
Mode	R/W

DMA Destination Address

Specifies the beginning destination address in the host system where a DMA operation will write.

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5.2.13 Register 14 (DMA Transfer Length)

PCI Address	BAR2 + 0x70
Designation	DMA Transfer Length
Bit(s)	31-0
Mode	R/W

DMA Transfer Length

Specifies the total number of bytes to transfer for each DMA transfer. Lengths are limited to multiples of 8.

5.2.14 Register 15 (DMA Control/Status)

PCI Address	BAR2 + 0x78					
Designation	Reserved	DMA Transfer Width	Reserved	DMA Source	Reserved	DMA Start
Bit(s)	7-5	4	3	2	1	0
Mode	R/W	R/W	R/W	R/W	R/W	R/W

PCI Address	BAR2 + 0x78		
Designation	DMA Complete	Reserved	DMA Burst Length
Bit(s)	31	30-20	19-8
Mode	R	R/W	R/W

DMA Start

When set, a DMA operation is started. This bit will automatically clear when the DMA operation is complete.

DMA Source

Specifies the source of data for DMA operations. When clear, data source is FPGA RAM. When set, data source is DRAM.

DMA Transfer Width

Specifies the width of transfers over the PCI interface for DMA operations. When clear, transfer width is 32-bits. When set, transfer width is 64-bits.

DMA Burst Length

Specifies the number of contiguous PCI transfers to be attempted during DMA operations. After each burst, control of the PCI bus is released to give other PCI devices a chance to

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perform pending operations on the bus. See the “DMA Bursts” section for further information about DMA bursts.

DMA Burst Lengths are specified in units of 8-bytes. Because of this, a DMA transfer performed with a burst length of 256 will attempt 256 contiguous PCI transfers in 64-bit mode, but will attempt 512 contiguous PCI transfers in 32-bit mode.

DMA Complete

This bit is set when a DMA transfer completes and is automatically cleared when read.

5.2.15 Register 18 (PLL Control)

PCI Address	BAR2 + 0x90		
Designation	Enable PLL	PLL Reference	Reserved
Bit(s)	31	30	29-0
Mode	R/W	R/W	R/W

Enable PLL

Specifies whether the onboard PLL is enabled or disabled.

0 = Disable PLL
1 = Enable PLL

PLL Reference

Specifies the PLL’s reference signal source.

0 = External PLL reference
1 = Onboard oscillator

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6 BOARD USAGE

6.1 Board Configuration

6.1.1 DeMux Clock Delay

Register 3 holds the DeMux Clock Delay value, which is used to configure timing adjustments necessary for clean signal acquisition at different input clock rates. The DeMux Clock Delay may need to be adjusted as environmental conditions change as its performance does not scale linearly over temperature.

The default DeMux Delay value is 0xE6. Use the following table to find a non-problematic DeMux Clock Delay setting for a given clock rate.

Board Clock (MHz)	Problematic DeMux Delay Values Over Input Clock Range																
2000																	
1900																	
1800																	
1700																	
1600																	
1500																	
1400																	
1300																	
1200																	
1100																	
1000																	
900																	
800																	
700																	
600																	
500																	
400																	
300																	
200																	
	0x00	0x10	0x20	0x30	0x40	0x50	0x60	0x70	0x80	0x90	0xA0	0xB0	0xC0	0xD0	0xE0	0xF0	0xFF
DeMux Delay Value (Shaded cells can be problematic)																	

Table 4 - Problematic DeMux Clock Delay Values Over Clock Range

6.1.2 Trigger Threshold

Trigger Threshold is adjustable via an 8-bit bit field in register 3. This adjustment facilitates triggering from a wide variety of trigger signals.

6.1.3 Clock Phase

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Clock Phase is adjustable via an 8-bit bit field in register 9. The Clock Phase adjustment alters the phase relationship between the clock signal and the analog input signal. This adjustment is ideal for synchronizing a clock signal among multiple boards. Cabling differences and minor variations between boards can be compensated for with this adjustment. The range of the Clock Phase adjustment is approximately +- 120 ps around the center value.

6.1.4 Trigger Delay

Trigger Delay is adjustable via an 8-bit bit field in register 9. This adjustment is ideal for synchronizing a trigger signal among multiple boards. Cabling differences and minor variations between boards can be compensated for with this adjustment. The range of the Trigger Delay adjustment is approximately +- 275 ps around the center value.

6.1.5 ADC Gain

ADC Gain is adjustable via an 8-bit bit field in register 9. This adjustment is ideal for matching input levels of multiple boards. Cabling differences and minor variations between boards can be compensated for with this adjustment. The range of the ADC Gain adjustment is approximately +- 10% around the center value.

6.1.6 Onboard PLL

The onboard PLL can be utilized to provide an alternative to using the front panel clock input as the board's clock signal. The PLL provides a 2 GHz board clock when enabled.

The reference signal for the PLL is provided by an onboard 50 MHz oscillator, or alternatively by an external PLL reference signal via the front panel input. When the external PLL reference signal is used, the PLL will synchronize with this signal.

When the PLL is enabled, the external board clock input must not be supplied. If the PLL is enabled and an external board clock is supplied, digitization performance will be degraded due to the two clock signals mixing.

Register 18 provides controls for enabling/disabling and configuring the PLL.

6.2 FPGA RAM

FPGA RAM is a 64 KB, dual-port memory block located within the ADC3255's FPGA. It is addressable at PCI BAR0. The dual-port capability coupled with status and control bits available in registers enable the use of FPGA RAM as a circular buffer for high-speed, continuous flow applications. For PCI burst read access, the internal address counter is automatically incremented. Full-length burst mode is supported.

FPGA RAM is mapped as follows:

First byte of FPGA RAM = BAR0 Address + 0
Last byte of FPGA RAM = BAR0 Address + 0xFFFF

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6.2.1 Continuous Data Flow From FPGA RAM

For continuous block transfer, the use of interrupts and careful memory management are necessary. Blocks of input data from the FPGA RAM should be read into a buffer in a rotating fashion similar to a FIFO implementation. Depending on how rapidly the input data is utilized, the input data buffer memory size should be some multiple of the FPGA RAM size. Since the memory blocks are addressable, address pointers to the FPGA RAM and the buffer memory would need to be maintained. The memory status is checked before each block transfer. If the status indicates empty, then the data collector task should wait until the FPGA RAM Empty bit or the FPGA RAM Near Empty bit are cleared. When a Full status is sensed, then the data collection has fallen behind. The data acquisition should then hold until memory space is available.

6.3 DRAM

DRAM is a reference to the 192 MB of DRAM located on the board. DRAM is addressable at PCI BAR1. Because sample data in DRAM is internally packed, DRAM is mapped as a 256 MB window from the PCI bus. DRAM holds up to 128 MSamples. DRAM cannot be read from while sample data is being written to it. For PCI burst read access, the internal address counter is automatically incremented. For boards with the 384 MB DRAM option, double the values listed in this document as appropriate.

DRAM is mapped as follows:

First byte of DRAM = BAR1 Address + 0
Last byte of DRAM = BAR1 Address + 0x0FFF FFFF

6.3.1 Using DRAM

When capture to DRAM is disabled, the DRAM is not utilized and the standard status/control bits such as DRAM A/B Writing, DRAM Active Address, etc. are thus also not utilized.

6.3.1.1 DRAM Write Cache

The DRAM Write Cache is a cache between the FPGA and the DRAM used to buffer sample data before it is written into DRAM.

The DRAM Write Cache must be empty before:

A) Reading data from DRAM.

B) Clearing Address Counters.

If either of those actions are performed before the DRAM Write Cache is empty, the DRAM controller in the FPGA could be thrown into a bad state.

To ensure the DRAM Write Cache is empty, read register 7 and ensure that the DRAM A Writing and DRAM B Writing status bits are clear.

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6.3.1.2 DRAM Read Cache

The DRAM Read Cache is an 8 KB cache between the FPGA and the DRAM used to buffer sample data before it is read across the PCI bus. The board's DRAM controller reads data from DRAM in 8 KB increments beginning at address 0. This yields DRAM Read Cache boundaries at addresses 0x0, 0x2000, 0x4000, and so on up to the end of DRAM.

Read requests that begin on an offset not lying on an 8 KB increment will not be serviced until the DRAM Read Cache has read from the next lowest 8 KB increment up to the requested offset. An example of this is when the user issues a 32-bit PCI read from DRAM base, followed by a read from DRAM base + 12 KB. The delay to the servicing of the first read is negligible since it lies on an 8 KB boundary. The second read will not be serviced until the DRAM Read Cache has read from 8 KB up to 12 KB from DRAM.

An exception to the previous rule is if the DRAM Read Cache already has the desired offset's data loaded from a previous read; in this case it will be serviced immediately. This also can pose a problem in the case where a read(s) within an 8 KB increment is performed, then a capture writes new data into that location in DRAM, then another read(s) is performed within the same 8 KB increment without first performing a read in a different 8 KB increment of DRAM. In this case the DRAM Read Cache will not have been forced to update with the new data from the capture, and will be stale.

When reading a block of data from DRAM in PCI burst mode, care must be taken to prevent reading across a DRAM Cache boundary (0x2000, 0x4000, etc.). To ensure that only valid data is read, ensure that a burst read operation stops at the end of the current DRAM Read Cache boundary and another burst read operation starts at the beginning of the next DRAM Read Cache boundary.

6.4 Input Modes

Input modes are configured via control bits in register 1.

6.4.1 Raw Data

Samples are taken from the analog input signal and stored as 10-bit, unsigned integers each occupying 16 bits.

6.4.2 Counting Pattern Test Data

The input signal is ignored in this mode. The FPGA generates a test pattern, which is a continuously incrementing count from 0 to 1023. Every time the count reaches 1023, it wraps back to 0 and continues in this manner until capturing is paused. Counting pattern samples are stored as 10-bit, unsigned integers each occupying 16 bits. This mode of input is useful for debugging purposes.

6.4.3 DeMux Test Data

Input in this mode is the output from the DeMux while the DeMux ignores its input signal. Samples are stored as 10-bit, unsigned integers each occupying 16 bits. This mode of input is useful for debugging purposes.

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6.5 Auto Triggering

If the Auto Trigger bit in register 1 is set, trigger events will automatically be generated upon completion of every capture event. In this mode, trigger events will be generated on the FPGA clock cycle following the FPGA clock cycle in which each capture event ends. If the Auto Trigger bit is set while a capture event is not taking place, a trigger event will be generated on the following FPGA clock cycle.

6.6 Start/Stop Vectors

FPGA RAM start/stop vectors are each 16 bits and are located in register 2. DRAM start/stop vectors are 32 bits each and are located in registers 4 and 5 respectively. Units for both values are in FPGA clock cycles. Each FPGA clock cycle yields 8 samples from the DeMux bus.

6.6.1 Start Vectors

The start vector determines the length of delay from a trigger event to the beginning of data capture. This value is also known as the capture event delay. The minimum recommended capture event delay for the ADC3255 is 3. If a capture event delay from 1 to 2 is used, all samples captured before the 3rd FPGA clock cycle from the trigger event will be indeterminate. Please refer to the Trigger Timing Diagram for further details regarding data acquired at the beginning of a capture event. A capture event delay of 0 will actually yield a capture event delay of 65536 since it will not be reached until the 16-bit start vector has counted to its maximum and then wrapped around to 0.

6.6.2 Stop Vectors

The stop vector determines the stopping point of data capture for each capture event. The stop vector minus the start vector determines the length of each capture event.

6.6.3 Start/Stop Vector Usage

With a capture event delay of 32 and a stop vector of 40, after a trigger event, data capture would begin after 32 FPGA clock cycles and end when the 40th FPGA clock cycle had completed. This example would store 64 samples (8 samples per FPGA clock cycle) to the desired RAM buffer(s) per trigger event. If in external triggering mode, after a stop vector has been reached the board begins waiting for another trigger event to occur. If in auto-triggering mode, after a stop vector has been reached, a trigger event will be generated on the next FPGA clock cycle.

6.6.4 Start/Stop Vector Considerations When Capturing To Both Buffers

When capture to DRAM is enabled, stop vectors of the FPGA RAM and DRAM can affect each other's capture operation. If one stop vector is greater than the other is, and the lesser stop vector has been reached, new trigger events will be ignored until the buffer with the greater stop vector has completed its capture event by reaching its stop vector.

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6.6.5 DRAM Capture Event Size

For DRAM vectors, the capture event size (calculated by subtracting the Start Vector from the Stop Vector) is internally controlled by the FPGA to be in multiples of 2 FPGA clocks due to the DRAM burst size. When the FPGA utilizes the DRAM stop vector, it acquires bits 31 through 1 from the actual DRAM stop vector, but acquires bit 0 from the DRAM start vector. This scheme guarantees that the capture event size will be a multiple of 2 FPGA clocks.

6.7 Interrupts

Register 6 contains 16 bits for IRQ status and 16 bits for IRQ mask for configuring the desired initiation of interrupts. A PCI interrupt will be generated at the transition of each event enabled in the mask portion of the register. IRQ events are enabled when their corresponding bit in the IRQ mask portion of the register is set, and disabled when the bit is clear. In the case of the Capture Event Count, an interrupt is generated when the number of capture events completed matches the 8-bit value in the mask, or if the 8-bit value in the mask is zero, the interrupt is disabled. Interrupt are cancelled upon the reading of the IRQ status register, including the mask portion, since it is treated as a 32-bit register.

6.8 DMA

The ADC3255 is capable of performing DMA transfers utilizing PCI burst mode for high-performance data transfer. DMA operation is controlled via registers 12 through 15. Refer to the bit definitions for these registers for more details about DMA operation.

6.8.1 Performing DMA Transfers

To perform a typical DMA transfer:

A) Configure DMA operation parameters such as the source/destination addresses, transfer width, transfer length, and burst length.

B) If using the DMA Complete IRQ for DMA transfer completion notification, set the DMA Complete IRQ Mask bit in register 6.

C) Set the Start DMA bit in register 15 to initiate the DMA Transfer.

D) If using the DMA Complete IRQ, check the value of the DMA Complete bit in your ISR to determine when the DMA transfer has completed. If not using the DMA Complete IRQ, poll the DMA Complete bit in register 15 to determine when the DMA transfer has completed.

6.8.2 DMA Bursts

DMA bursts are sequences of contiguous PCI transfers that are attempted during DMA operations. After each burst, control of the PCI bus is released to give other PCI devices a chance to perform pending operations on the bus. Bursts can be interrupted by other PCI devices and the DMA will resume the transfer from where it left off.

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Depending on the system, larger DMA Burst Lengths usually provide better throughput performance, but will more heavily monopolize the PCI bus. Other devices on the bus can interrupt DMA operations, but their throughput rates will likely be reduced.

6.8.3 64-Bit DMA Transfers

There are cases where 64-bit PCI transfers will not be available. When this is the case, transfer width will default to 32-bits. A common cause for this limitation is if the board is plugged into a 32-bit PCI slot.

6.8.4 DMA Limitations

6.8.4.1 DMA from DRAM across DRAM Read Cache Boundaries

DMA transfers from DRAM (BAR1) are limited in size by the DRAM Read Cache. DMA transfers must not span across a DRAM Read Cache boundary or invalid data will be transferred. To ensure that only valid data is transferred, ensure that a DMA transfer stops at the end of the current DRAM Read Cache boundary and another DMA transfer starts at the beginning of the next boundary. See the “DRAM” section for further information about the DRAM Read Cache.

6.8.4.2 DMA Transfer Length Multiples

DMA Transfer Lengths are limited to multiples of 8 bytes. Lengths which do not lie on an 8 byte boundary will be modified internally by truncating the length to the next lowest 8 byte boundary (e.g., a user-specified length of 1028 would be truncated to 1024).

6.9 Bit Packed Sample Data

Sample data can be bit packed by setting the Enable Bit Packing bit in register 1.

6.9.1 Bit Packed Sample Data in FPGA RAM

When bit packing is enabled, three samples are stored in each 32-bits of FPGA RAM instead of the normal two samples. Enabling Bit Packing increases the number of samples that can be stored in FPGA RAM by 1.5 times. Refer to the Bit Packing Data Organization figure for sample organization details when using bit packing.

6.9.2 Bit Packed Sample Data in DRAM

When bit packing is enabled, three samples are contained in every 32 bits that are read across the PCI bus from DRAM instead of the normal two samples. When bit packing is enabled, the DRAM address window is 2/3 the size of the standard DRAM address window. Bit packing does not increase the number of samples that can be stored in DRAM because the ADC3255’s DRAM controller already packs sample data internally. Refer to the Bit Packing Data Organization figure for sample organization details when using bit packing.

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6.9.3 Bit Packed Sample Data Organization

The following figure illustrates how sample data is presented when read across the PCI bus from FPGA RAM/DRAM when using bit packing.

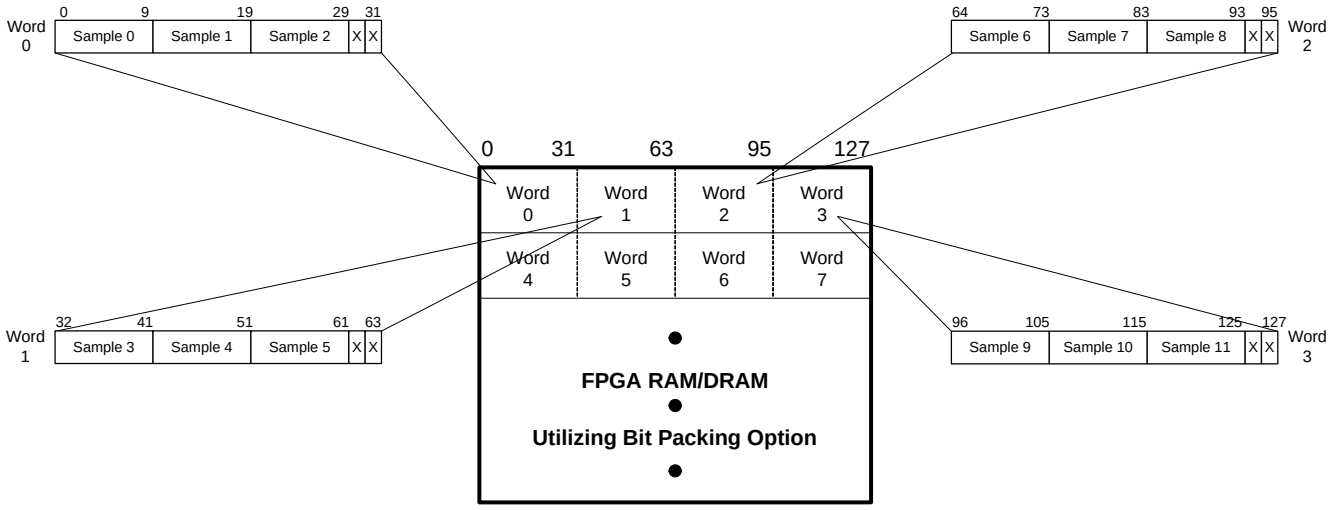


Figure 3 - Bit Packed Data Organization

6.10 Temperature Sensor

Register 10 contains temperature data retrieved from the onboard temperature sensor. The temperature data is a 12-bit, signed integer. A temperature data reading of zero corresponds to 0°C. Every increment corresponds to 1/16th of one degree Celsius; for example: 0x191 / 16 = +25.0625°C. Refer to the Temperature/Data Relationship Table for more examples.

Temperature Data (Hex)	Sensor Temperature (°C)
0x370	**+55**
0x191	**+25.0625**
0x000	**0**
0xE6F	**-25.0625**
0xC90	**-55**

Table 22 - Temperature/Data Relationship

7 SOFTWARE REQUIREMENTS

7.1 PCI Enumeration

To allow software access to the board, typically the host system will detect the board during PCI enumeration at system reset. During enumeration, data such as the device's BARs, interrupt line, etc. are configured in the device's PCI Configuration Space by the host system.

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Following enumeration, the device's Command Register in its PCI Configuration Space must be configured to allow memory I/O operations to/from the device's BARs.

7.2 Board Initialization

The following is a typical example of the board initialization process. When the following steps have been completed, data collection can be initiated by clearing the Pause Capturing bit in register 1.

A) The FPGA RAM Active Address and DRAM Active Address are reset to zero by setting and then clearing the Clear Address Counters bit in register 1.

B) FPGA RAM and DRAM Start/Stop Vectors are configured.

C) The following options are then configured in register 1:
   Auto Trigger en/disabled.
   Input data source (Analog input, Test Pattern Data, or DeMux Test Data).
   Ignore FPGA RAM Full en/disabled.
   Data Endianness configured.
   Bit Packing en/disabled.

D) The following options are then configured in register 7:
   Activate DRAM en/disabled.
   Ignore DRAM Full en/disabled.

E) The DeMux Clock Delay, Trigger Threshold, and Clock Phase in register 3 are modified if necessary.

F) The ADC Gain in register 9 is modified if necessary.

G) Any desired interrupt masks are enabled in register 6.

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