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Find the *Delta Information Systems / GDP Space Systems RNG201* at our website: *Click HERE*

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Satellite Modems & Ranging Systems: RF IF & Sub-Carrier
SGLS Satellite Modems & Ranging Systems – RF IF & Sub-Carrier
Link and Mission Simulation & Validation
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# SGLS Satellite Modems & Ranging Systems – RF IF & Sub-Carrier

*Model RNG201 SGLS Ranging Processor PCI Card*



The RNG201 is a high performance, multiple format, Ranging Processor. Both forward link range code generation and return link range processing functions are accommodated. The RNG201 is unique in eight major ways. 1) It processes major ranging formats: SGLS, USB, ESA and Commercial. 2) It is programmable to select SGLS code rates and USB / ESA Major Tone frequencies. 3) It is programmable for SGLS, USB and ESA code lengths. 4) Doppler and Range estimates are included in the process. 5) Adjustable acquisition and tracking bandwidths enhance operation in low signal-to-noise applications. 6) A tunable, high dynamic range, high selectivity front end is incorporated to minimize adjacent signal interference and ranging signal distortion. 7) An all-digital design improves accuracy, stability and resolution. 8) Reconfigurable logic allows for modifications to accommodate unique customer needs.

The RNG201 generates the forward link ranging signal using digital processing and an NCO clocked by a high rate oscillator locked to an external frequency reference. The digital signal is passed to a D/A, smoothing filter and output signal conditioner to create the Ranging Output for transmission to the satellite. The return link Ranging Input is passed through input signal conditioning and a tunable anti-alias filter to minimize noise and interference. The signal is then digitized and digitally filtered to reduce noise and interference. A digital Phase Lock Loop (PLL) is used to acquire and track the phase of the Major Tone (SGLS Clock). A frequency search is performed over an adjustable range at an adjustable rate. Acquisition is assisted by a Doppler frequency offset estimate, if available. Once acquired, the phase of the received signal is compared to the phase of the transmitted signal. The phase comparison provides a high-resolution measure of the time delay between the transmitted and received signal. After the Major Tone is acquired, the Minor Tones and Code Components are sequentially acquired to resolve range ambiguity. Ambiguity Resolution is assisted by a Range estimate, if available. If lock is lost, the acquisition process can be automatically reinitiated using the last Major Tone frequency and Range measurement as an aid. Different bandwidths may be set for the acquisition mode versus the tracking mode. These settings can be automatically set based on the measured signal-to-noise ratio. In the tracking mode, a 3rd order PLL is used to prevent acceleration errors from developing.

Outputs from the Ranging Processor include: the measured Range, acquisition status, tracking status, signal quality and alarm conditions. This information is provided by way of the PCI Bus. A self-test feature internally loops-back the Ranging Output to the Ranging Input for calibration and operation verification. All status and control is via the PCI Bus. All I/O is via the card front panel. The PCI Bus is fully compliant with PCI Local Bus Specification Revision 2.2.

Features | Specs | Documents (.pdf)

- Selectable Format: SGLS, USB, ESA or Commercial
- SGLS:
  - Selectable Code Length: Long (818,000 km), Medium (91,000 km) and Short (11,000 km)
  - Tunable Code Rate: 100 kbps to 1 Mbps
- USB:
  - Selectable Major Tones: High (500 kHz), Medium (100 kHz) and Narrow (20 kHz)
  - Selectable Ambiguity Resolution Code: Long (958,000 km), Medium (119,000 km) and Short (15,000 km)
- Enhanced Acquisition through Doppler and Range Acquisition Aids
- Adjustable Acquisition and Tracking Bandwidths for Performance Optimization
- High Selectivity, Tunable Anti-Aliasing Filter Minimizes Interference and Distortion
- All Digital Processing Provides High Resolution, Stability and Accuracy
- Flexible, Reconfigurable-Logic Design Allows Modification for Unique Requirements

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