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Mini PMAC2

INTRODUCTION

Overview

The Mini-PMAC2 is a member of the PMAC2 family of boards optimized for interface to 1 or 2 sine waves or direct PWM servo drives and for pulse-and-direction stepper drives. It has two channels of servo interface circuitry, but its software is capable of 8 axes of control. It is completely software compatible with the PMAC2-PC and PMAC2-Lite.

The Mini-PMAC2 is a 2/3-sixed ISA-bus expansion card with a small piggyback board containing the CPU board. While the Mini-PMAC2 is capable of ISA bus communications, with or without the optional on-board dual-ported RAM, it does not need to be inserted into an ISA expansion slot. Communications can be done through the standard on-board RS-232 serial port; standalone operation is possible.

Board Configuration

Base Version

The base version of the Mini PMAC2 provides a 2/3-slot board with:

- 40 MHz DSP56002 CPU
- 128k x 24 zero-wait-state SRAM active memory
- 512k x 8 flash memory for user backup & firmware
- Latest released firmware version
- RS-232 serial interface, ISA (PC) bus interface
- 1 16-node MACRO interface IC
- 2 channels axis interface circuitry, each including:
  - 3 output command signal sets, configurable as either:
    - 2 serial data streams to external DACs, 1 pulse-and-direction
    - 3 PWM top-and-bottom pairs
  - 3-channel differential/single-ended encoder input
  - 9 input flags, 2 output flags
  - Interface to 2 external serial ADCs, 8 to 18 bits
- 2 channels supplemental interface circuitry, each including:
  - 2-channel differential/single-ended encoder input
  - 1 output command signal set, configurable as pulse-&-direction or PWM top-and-bottom pair
- Display, MACRO, muxed I/O, direct I/O interface ports
- PID/notch/feedforward servo algorithms
- 1-year warranty from date of shipment
- One manual per set of 1 to 4 PMACs in shipment
- (Cables, mounting plates, mating connectors not included)

Option 2: Dual Ported RAM

Dual-ported RAM provides a very high-speed communication path for bus communication with the host computer through a bank of shared memory. DPRAM is advised if more than about 100 data items per second are to be passed between the controller and the host computer in either direction.

- Option 2 provides an on-board 8k x 16 bank of dual-ported RAM. The key component on the board is U23.

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Option 5: CPU & Memory Configurations

If the 40 MHz CPU that comes standard does not have sufficient computational power, faster versions are available as options. These options provide faster CPU ICs in U7 and faster SRAM ICs in U58, U59, and U60.

- Option 5B provides a 60 MHz CPU with zero-wait-state SRAM active memory.
- Option 5C provides an 80 MHz CPU with zero-wait-state SRAM active memory.

Option 6: Extended Servo Algorithm

The standard PID servo algorithm with feedforward and notch filter is suitable for most applications. Systems with difficult dynamics, especially with significant flexibility, may require a more powerful servo algorithm, such as the Extended Servo Algorithm (ESA).

- Option 6 provides firmware in the Mini-PMAC2 that replaces the standard PID servo algorithm with the Extended Servo Algorithm.

Option 7: Plate Mounting

Option 7 provides a mounting plate connected to the Mini-PMAC2 with standoffs. It is used to install the Mini-PMAC2 in standalone applications.

Option 8: High-Accuracy Clock Crystal

The Mini-PMAC2 has a clock crystal (component Y1) of nominal frequency 19.6608 MHz (~20 MHz). The standard crystal's accuracy specification is +/-100 ppm. Long-term velocity accuracy is limited by the accuracy of the crystal, unless an external time base is used.

- Option 8A provides a nominal 19.6608 MHz crystal with a +/-15 ppm accuracy specification.

Option 10: Firmware Version Specification

Normally, the Mini-PMAC2 is provided with the newest released firmware version. A label on the U61 flash memory IC on the CPU board shows the firmware version loaded at the factory.

- Option 10 provides for a user-specified firmware version.

Option 16: Battery-Backed Parameter Memory

The contents of the standard memory are not retained through a power-down or reset unless they have been saved to flash memory first. Option 16 provides supplemental battery-backed RAM for real-time parameter storage that is ideal for holding machine state parameters in case of an unexpected power-down.

- Option 16 provides a 16k x 24 bank of battery-backed parameter RAM in components U84, U85, and U86 with the battery in BT1.

MINI-PMAC2 JUMPER AND SWITCH DESCRIPTIONS

E0: Firmware Reload Enable

E-Point	Physical Layout	Location	Description	Default
E0			Remove jumper for normal operation Jump pin 1 to 2 to lock PMAC2 in reset state (for factory use only) Jump pin 2 to 3 to reload firmware through serial or bus port	No jumper installed

E1: Servo and Phase Clock Direction Control

E-Point	Physical Layout	Location	Description	Default
E1			Remove jumper for Mini-PMAC2 to use its internally generated servo and phase clock signals and to output these signals on the J5 serial port connector	No jumper

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E1: Servo and Phase Clock Direction Control

E-Point	Physical Layout	Location	Description	Default
E1	 		Remove jumper for Mini-PMAC2 to use its internally generated servo and phase clock signals and to output these signals on the J5 serial port connector Jump pins 1 and 2 for Mini-PMAC2 to expect to receive its servo and phase clock signals on the J5 serial port connector	No jumper
If the E1 jumper is ON and the servo and phase clocks are not brought in on the J5 serial port, the watchdog timer will trip immediately.				

E2: CPU Frequency Select

E-Point	Physical Layout	Location	Description	Default
E2			Remove jumper for 40 MHz operation (E4 OFF also) or for 80 MHz operation (E4 ON) Jump pin 1 to 2 for 60 MHz operation (E4 OFF)	No jumper installed (standard or Opt 5C) Jumper installed (Opt 5B)

E3: Normal/Re-Initializing Power-Up/Reset

E-Point	Physical Layout	Location	Description	Default
E3			Jump pin 1 to 2 to re-initialize on power-up/reset, loading factory default settings. Remove jumper for normal power-up/reset, loading user-saved settings.	No jumper installed

E4: CPU Frequency Select

E-Point	Physical Layout	Location	Description	Default
E4			Remove jumper for 40 MHz operation (E2 OFF also) or for 60 MHz operation (E4 ON) Jump pin 1 to 2 for 80 MHz operation (E2 OFF)	No jumper installed (standard or Opt 5B) Jumper installed (Opt 5C)

E5 – E6: (Reserved for future use)

E7 – E10: Host Interrupt Signal Select

E-Point	Physical Layout	Location	Description	Default
E7		A9	Jump pin 1 to 2 to allow "PMAC-INTERRUPT" to host-PC on "IRQ10".	No jumper installed
E8		A9	Jump pin 1 to 2 to allow "PMAC-INTERRUPT" to host-PC on "IRQ11".	No jumper installed
E9		A9	Jump pin 1 to 2 to allow "PMAC-INTERRUPT" to host-PC on "IRQ12".	No jumper installed
E10		A9	Jump pin 1 to 2 to allow "PMAC-INTERRUPT" to host-PC on "IRQ15".	No jumper installed
Only one of the jumpers E7 – E10 should be ON at any time.				

E13: Encoder Sample Clock Direction Control

E-Point	Physical Layout	Location	Description	Default

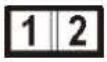
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Only one of the jumpers E7 – E10 should be ON at any time.

E13: Encoder Sample Clock Direction Control

E-Point	Physical Layout	Location	Description	Default
E13			Remove jumper to output SCLK generated in servo ASIC on SCLK_12, or to control direction by software Jump pins 1 to 2 to input SCLK signal for servo ASIC on SCLK_12	No jumper installed

E14: Watchdog Disable Jumper

E-Point	Physical Layout	Location	Description	Default
E14			Jump pin 1 to 2 to disable WATCHDOG timer (for test purposes only!!). Remove jumper to enable WATCHDOG timer.	No jumper installed

E20: Battery-Backed RAM Enable

E-Point	Physical Layout	Location	Description	Default
E20			Jump pins 1 to 2 if Option 16 battery-backed RAM is present as 32-pin ICs in U84, U85 & U86 Jump pins 2 to 3 if Option 16 battery-backed RAM is present as 28-pin ICs in U84, U85, & U86 Remove jumper if no Option 16 battery-backed RAM is present	2-3 jumper installed (no Opt. 16) 1-2 jumper installed (Opt. 16)

E111-112: Command Output Disable State

E-Point	Physical Layout	Location	Description	Default
E111			Jump pin 1 to 2 for digital servo command output signals of Channel 1 to tri-state when amplifier-enable signal for Channel 1 is in disable state. Remove jumper for digital servo command output signals of Channel 1 to remain active (but typically with zero command value) when amplifier-enable signal for Channel 1 is in disable state.	No jumper installed
E112			Jump pin 1 to 2 for digital servo command output signals of Channel 2 to tri-state when amplifier-enable signal for Channel 2 is in disable state. Remove jumper for digital servo command output signals of Channel 2 to remain active (but typically with zero command value) when amplifier-enable signal for Channel 2 is in disable state.	No jumper installed

DIP Switch Block S1: ISA-Bus Address Select

S1B				S1A							
4	3	2	1	8	7	6	5	4	3	2	1
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
⇑	⇑	⇑	⇑	⇑	⇑	⇑	⇑	⇑	⇑	⇑	⇑
⇓	⇓	⇓	⇓	⇓	⇓	⇓	⇓	⇓	⇓	⇓	⇓
ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON

The 12 DIP switches on block S1 set the base address of the PMAC2 on the PC bus. Together they form a binary number. Each switch, if in the "ON" (closed) position, sets its bit to 0; if in the "OFF" (open) position, sets its bit to 1. The possible base addresses are all multiples of 16. Therefore, switch 1 sets a bit value of 16, switch 2 sets a bit value of 32, and so on.

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ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON

The 12 DIP switches on block S1 set the base address of the PMAC2 on the PC bus. Together they form a binary number. Each switch, if in the "ON" (closed) position, sets its bit to 0; if in the "OFF" (open) position, sets its bit to 1. The possible base addresses are all multiples of 16. Therefore, switch 1 sets a bit value of 16; switch 2 sets a bit value of 32, and so on.

Switch #	Bit Value	Default	Default Value	Your Value
1 (S1A-1)	16 (10h)	ON (x1)	16 (10h)	
2 (S1A-2)	32 (20h)	OFF (x0)	0	
3 (S1A-3)	64 (40h)	OFF (x0)	0	
4 (S1A-4)	128 (80h)	OFF (x0)	0	
5 (S1A-5)	256 (100h)	OFF (x0)	0	
6 (S1A-6)	512 (200h)	ON (x1)	512 (200h)	
7 (S1A-7)	1024 (400h)	OFF (x0)	0	
8 (S1A-8)	2048 (800h)	OFF (x0)	0	
9 (S1B-1)	4096 (1000h)	OFF (x0)	0	
10 (S1B-2)	8192 (2000h)	OFF (x0)	0	
11 (S1B-3)	16384 (4000h)	OFF (x0)	0	
12 (S1B-4)	32768 (8000h)	OFF (x0)	0	
Total	--	--	528 (210h)	

If you wish to set the board to a different bus address, it is best to specify the address in hexadecimal form because each hex digit corresponds to 4 switches. The last hex digit of the base address is always zero.

Example: If you wish to set the base address on the PC bus to 992 decimal, or 03E0 hex, the first '0' corresponds to switches 9 through 12. All of these should be ON to set their bits to 0. The '3' corresponds to switches 5 through 8. Switches 8 and 7 should be ON, and switches 6 and 5 should be OFF to define the '3'. The 'E' corresponds to switches 1 through 4. Switches 4, 3, and 2 should be OFF, and switch 1 should be ON to define the 'E'.

Switch #	12	11	10	9	8	7	6	5	4	3	2	1	-	-	-	-
Hex	0				3				E				0			
Binary	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0
Setting	on	on	on	on	on	on	off	off	off	off	off	on	-	-	-	-

HOST PC-AT I/O ADDRESS MAP

Hex. Range	Dec. Range	Usage
000-01F	0-31	DMA Controller 1 8237A-5
020-03F	32-63	Interrupt Controller 1 8259A
040-05F	64-67	Timer 8254-2
060-06F	96-111	8042 (Keyboard)
070-07F	112-127	Real-time clock, NMI mask
080-09F	128-159	DMA Page Registers
0A0-0BF	160-191	Interrupt Controller 2 8259A
0C0-0DF	192-223	DMA Controller 2 8237A-5
0F0-0FF	240-255	Math CO processor
1F0-1F8	496-504	Fixed Disk
200-20F	512-527	Game Control
210-217	528-535	Expansion Unit (usually open)
278-27F	632-639	Parallel Printer: LPT2
2B0-2DF	688-735	Alternate EGA
2F8-2FF	760-767	Asynchronous Common: COM2
300-31F	768-799	Prototype Card (usually open)
360-36F	864-879	PC Network
378-37F	888-895	Parallel Printer: LPT1
380-38F	896-911	SDLC Communications 2

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2B0-2DF	688-733	Alternate EGA
2F8-2FF	760-767	Asynchronous Common: COM2
300-31F	768-799	Prototype Card (usually open)
360-36F	864-879	PC Network
378-37F	888-895	Parallel Printer: LPT1
380-38F	896-911	SDLC Communications 2
390-393	912-915	Cluster
3A0-3A9	928-937	SDLC Communications 1
3B0-3BF	944-959	IBM Monochrome Display/Printer
3C0-3CF	960-975	Enhanced Graphics Adapter
3D0-3DF	976-991	Color/Graphics
3F0-3F7	1000-1015	Diskette Controller
3F8-3FF	1016-1023	Asynchronous Common.: COM1
x2E1		GPIB Adapter
x390-x393		Cluster Adapter

Note: It is highly recommended that the above address space segment not be used for the PMAC host base address unless the "Usage" column indicates "Usually Open."

MINI-PMAC2 MATING CONNECTORS

J2 (JTHW)/Multiplexer Port

1. 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 qty. 2-T&B Ansley P/N 609-2641
2. 171-26 T&B Ansley stan. flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J3 (JIO)/Digital I/O

1. 40-pin female flat cable connector Delta Tau P/N 014-R00F40-0K0 qty. 2 - T&B Ansley P/N 609-4041
2. 171-40 T&B Ansley stan. flat cable stranded 40-wire
3. Phoenix varioface module type FLKM 40 (male pins)

J4 (JMACRO)/MACRO Digital Data

1. 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 qty. 2 - T&B Ansley P/N 609-2641
2. 171-26 T&B Ansley stan. flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

JS1 (JADC)/A/D Converter Interface

1. 16-pin female flat cable connector Delta Tau P/N 014-R00F16-0K0 qty. 2 - T&B Ansley P/N 609-1641
2. 171-16 T&B Ansley stan. flat cable stranded 16-wire
3. Phoenix varioface modules type FLKM16 (male pins) P/N 22 81 03 1

J5 (JRS232)/RS-232 Serial Communications

1. 10-pin female flat cable connector Delta Tau P/N 014-ROOF10-0K0 qty. 2 - T&B Ansley P/N 609-1041
2. 171-10 T&B Ansley stan. flat cable stranded 10-wire
3. Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

J6 (JDISP)/Display

1. 14-pin female flat cable connector Delta Tau P/N 014-R00F14-0K0 qty. 2 - T&B Ansley P/N 609-1441
2. 171-14 T&B Ansley stan. flat cable stranded 14-wire
3. Phoenix varioface modules type FLKM14 (male pins) P/N 22 81 02 1

J7 (JHW)/Auxiliary Channel

1. 20-pin female flat cable connector Delta Tau P/N 014-R00F20-0K0 qty. 2 - T&B Ansley P/N 609-2041
2. 171-20 T&B Ansley stan. flat cable stranded 20-wire
3. Phoenix varioface modules type FLKM20 (male pins)

J9 (JMACH1)/Machine Port 1

1. 100-pin high density board edge with center key, 0.050" pitch,

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qty. 2, AMP P/N 1-04068-7, Delta Tau P/N 014-00010-ERB

2041
2. 171-20 T&B Ansley stan. flat cable stranded 20-wire
3. Phoenix varioface modules type FLKM20 (male pins)

J9 (JMACH1)/Machine Port 1

1. 100-pin high-density box header with center key, 0.050" pitch, qty. 2. AMP P/N 1-04068-7, Delta Tau P/N 014-00010-FPB
2. High-density flat cable stranded 100-wire

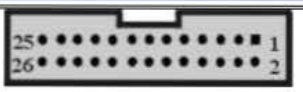
J11 (JEXP)/Expansion

1. 50-pin female flat cable connector Delta Tau P/N 014-R00F50-0K0 qty. 2 - T&B Ansley P/N 609-5041
2. 171-50 T&B Ansley stan. flat cable stranded 50-wire
3. Phoenix varioface module type FLKM 50 (male pins) P/N 22 81 08 9

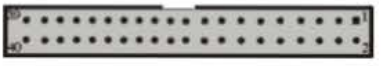
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MINI-PMAC2 CONNECTOR PINOUTS

J2 (JTHW): Multiplexer Port Connector

J2 JTHW (26-Pin Connector)				Front View 
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	GND	Common	PMAC Common	
2	GND	Common	PMAC Common	
3	DAT0	Input	Data-0 Input	Data Input from MUX Port Accessories
4	SEL0	Output	Select-0 Output	Address/Data Output for MUX Port Accessories
5	DAT1	Input	Data-1 Input	Data Input from MUX Port Accessories
6	SEL1	Output	Select-1 Output	Address/Data Output for MUX Port Accessories
7	DAT2	Input	Data-2 Input	Data Input from MUX Port Accessories
8	SEL2	Output	Select-2 Output	Address/Data Output for MUX Port Accessories
9	DAT3	Input	Data-3 Input	Data Input from MUX Port Accessories
10	SEL3	Output	Select-3 Output	Address/Data Output for MUX Port Accessories
11	DAT4	Input	Data-4 Input	Data Input from MUX Port Accessories
12	SEL4	Output	Select-4 Output	Address/Data Output for MUX Port Accessories
13	DAT5	Input	Data-5 Input	Data Input from MUX Port Accessories
14	SEL5	Output	Select-5 Output	Address/Data Output for MUX Port Accessories
15	DAT6	Input	Data-6 Input	Data Input from MUX Port Accessories
16	SEL6	Output	Select-6 Output	Address/Data Output for MUX Port Accessories
17	DAT7	Input	Data-7 Input	Data Input from MUX Port Accessories
18	SEL7	Output	Select-7 Output	Address/Data Output for MUX Port Accessories
19	N.C.	N.C.	No Connection	
20	GND	Common	PMAC Common	
21	BRLD/	Output	Buffer Request	Low is "Buffer Req."
22	GND	Common	PMAC Common	
23	IPLD/	Output	In Position	Low is "In Position"
24	GND	Common	PMAC Common	
25	+5V	Output	+5VDC Supply	Power Supply Out
26	INIT/	Input	PMAC Reset	Low is "Reset"
The JTHW connector provides 8 inputs and 8 outputs at TTL levels; PMAC software supports the use of multiplexed I/O on this port.				

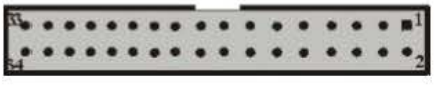
J3 (JI/O): General Input/Output Connector

J3 JIO (40-Pin Connector)			Top View 	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	I/O00	I/O	Digital I/O 0	Software Direction Control
2	I/O01	I/O	Digital I/O 1	Software Direction Control
3	I/O02	I/O	Digital I/O 2	Software Direction Control

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J3 JIO (40-Pin Connector)			Top View 	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	I/O00	I/O	Digital I/O 0	Software Direction Control
2	I/O01	I/O	Digital I/O 1	Software Direction Control
3	I/O02	I/O	Digital I/O 2	Software Direction Control
4	I/O03	I/O	Digital I/O 3	Software Direction Control
5	I/O04	I/O	Digital I/O 4	Software Direction Control
6	I/O05	I/O	Digital I/O 5	Software Direction Control
7	I/O06	I/O	Digital I/O 6	Software Direction Control
8	I/O07	I/O	Digital I/O 7	Software Direction Control
9	I/O08	I/O	Digital I/O 8	Software Direction Control
10	I/O09	I/O	Digital I/O 9	Software Direction Control
11	I/O10	I/O	Digital I/O 10	Software Direction Control
12	I/O11	I/O	Digital I/O 11	Software Direction Control
13	I/O12	I/O	Digital I/O 12	Software Direction Control
14	I/O13	I/O	Digital I/O 13	Software Direction Control
15	I/O14	I/O	Digital I/O 14	Software Direction Control
16	I/O15	I/O	Digital I/O 15	Software Direction Control
17	I/O16	I/O	Digital I/O 16	Software Direction Control
18	I/O17	I/O	Digital I/O 17	Software Direction Control
19	I/O18	I/O	Digital I/O 18	Software Direction Control
20	I/O19	I/O	Digital I/O 19	Software Direction Control
21	I/O20	I/O	Digital I/O 20	Software Direction Control
22	I/O21	I/O	Digital I/O 21	Software Direction Control
23	I/O22	I/O	Digital I/O 22	Software Direction Control
24	I/O23	I/O	Digital I/O 23	Software Direction Control
25	I/O24	I/O	Digital I/O 24	Software Direction Control
26	I/O25	I/O	Digital I/O 25	Software Direction Control
27	I/O26	I/O	Digital I/O 26	Software Direction Control
28	I/O27	I/O	Digital I/O 27	Software Direction Control
29	I/O28	I/O	Digital I/O 28	Software Direction Control
30	I/O29	I/O	Digital I/O 29	Software Direction Control
31	I/O30	I/O	Digital I/O 30	Software Direction Control
32	I/O31	I/O	Digital I/O 31	Software Direction Control
33	GND	Common	Ref. Voltage	
34	GND	Common	Ref. Voltage	
35	PHASE/	Output	Phase Clock	For latching data
36	SERVO/	Output	Servo Clock	For latching data
37	GND	Common	Ref. Voltage	
38	GND	Common	Ref. Voltage	
39	+5V	Output	Supply Voltage	To power ext. circuitry
40	+5V	Output	Supply Voltage	To power ext. circuitry
The JI/O connector provides 32 input/output pins at TTL levels. Direction can be controlled in byte-wide groups.				

J4 (JMACRO): MACRO Network Ring Interface Connector

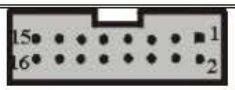
J4 JMACRO (34-Pin Connector)			Top View 	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	DOUT7	Output	Ring out bit 7	Macro ring command
2	DOUT6	Output	Ring out bit 6	Macro ring transmit
3	DOUT5	Output	Ring out bit 5	Macro ring transmit
4	DOUT4	Output	Ring out bit 4	Macro ring transmit
5	DOUT3	Output	Ring out bit 3	Macro ring transmit
6	DOUT2	Output	Ring out bit 2	Macro ring transmit
7	DOUT1	Output	Ring out bit 1	Macro ring transmit
8	DOUT0	Output	Ring out bit 0	Macro ring transmit

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3	DOUT5	Output	Ring out bit 5	Macro ring transmit
4	DOUT4	Output	Ring out bit 4	Macro ring transmit
5	DOUT3	Output	Ring out bit 3	Macro ring transmit
6	DOUT2	Output	Ring out bit 2	Macro ring transmit
7	DOUT1	Output	Ring out bit 1	Macro ring transmit
8	DOUT0	Output	Ring out bit 0	Macro ring transmit
9	CMD_OUT	Output		
10	GND	Common	Ref. Voltage	
11	GND	Common	Ref. Voltage	
12	STB_OUT	Output	Byte Strobe	
13	GND	Common	Ref. Voltage	
14	GND	Common	Ref. Voltage	
15	GND	Common	Ref. Voltage	
16	TCLK	Output	Ring Clock	12.5 MHz
17	GND	Common	Ref. Voltage	
18	GND	Common	Ref. Voltage	
19	DIN7	Input	Ring In Bit 7	Macro ring receive
20	DIN6	Input	Ring In Bit 6	Macro ring receive
21	DIN5	Input	Ring In Bit 5	Macro ring receive
22	DIN4	Input	Ring In Bit 4	Macro ring receive
23	DIN3	Input	Ring In Bit 3	Macro ring receive
24	DIN2	Input	Ring In bit 2	Macro ring receive
25	DIN1	Input	Ring In bit 1	Macro ring receive
26	DIN0	Input	Ring In bit 0	Macro ring receive
27	CMD_IN	Input		
28	GND	Common	Ref. Voltage	
29	GND	Common	Ref. Voltage	
30	DAT_STB	Input	Data Byte Strobe	
31	GND	Common	Ref. Voltage	
32	CMD_STB	Input	Cmd. Byte Strobe	
33	GND	Common	Ref. Voltage	
34	VLTN	Input	Violation Flag	Taxi chip receive error

The JMACRO connector provides the interface to the ACC-42P2 MACRO driver/receiver accessory board, permitting the Mini-PMAC2 to command axes and I/O through the MACRO ring.

JS1 (JADC): A/D Converter Connector

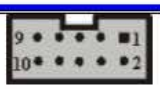
JS1 (16-Pin Header) — **Front View** 

Pin #	Symbol	Function	Description	Notes
1	ADC_CLK-	Output	A/D Converter Clock	Programmable frequency
2	N.C.		No Connect	
3	SCLK12+	Output	Encoder Sample Clock	
4	SCLK12-	Input / output	Encoder Sample Clock	Programmable frequency
5	ADC_STB+	Output	A/D Converter Strobe	Programmable sequence
6	N.C.		No Connect	
7	EQU3+	Output	Position Compare 1	Programmable polarity
8	EQU4+	Output	Position Compare 2	Programmable polarity
9	AENA3+	Output	Amplifier Enable 3	High true
10	AENA4+	Output	Amplifier Enable 4	High true
11	ADC_DAA3+	Input	Chan. 3A Serial data	MSB first
12	ADC_DAB3+	Input	Chan. 3B Serial data	MSB first
13	ADC_DAA4+	Input	Chan. 4A Serial data	MSB first
14	ADC_DAB4+	Input	Chan. 4B Serial data	MSB first

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11	ADC_DAA3+	Input	Chan. 3A Serial data	MSB first
12	ADC_DAB3+	Input	Chan. 3B Serial data	MSB first
13	ADC_DAA4+	Input	Chan. 4A Serial data	MSB first
14	ADC_DAB4+	Input	Chan. 4B Serial data	MSB first
15	+5V	Supply	+5V Power	MSB first
16	GND	Common	Reference Voltage	
The JS1 provides direct connection to an ACC-28B board, interfacing to ADC channels 3A, 3B, 4A, and 4B on the Mini-PMAC2. It does not conflict with serial ADC data brought into channels 1 and 2 through the J9 (JMACH) connector either from another ACC-28B, or from a direct-PWM drive.				

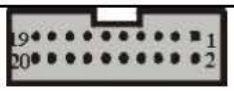
J5 (JRS232): Serial Port Connector

J5 JRS232 (10-Pin Connector)			Top View 	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	PHASE	Output	Phasing Clock	
2	DTR	Bi-directional	Data Terminal Ready	Tied to "DSR"
3	TXD/	Input	Receive Data	Host Transmit Data
4	CTS	Input	Clear to Send	Host Ready Bit
5	RXD/	Output	Send Data	Host Receive Data
6	RTS	Output	Request to Send	PMAC Ready bit
7	DSR	Bi-directional	Data Set Ready	Tied to "DTR"
8	SERVO	Output	Servo Clock	
9	GND	Common	PMAC Common	
10	+5V	Output	+5VDC Supply	Power Supply Out
The JRS232 connector provides the PMAC2-PC with the ability to communicate serially with an RS232 port. This connector cannot be used for daisychain interconnection of multiple PMACs. The Option 9L RS-422 interface is required for daisychaining.				

J6 (JDISP): Display Connector

J6 JDISP (14-Pin Connector)			Front View 	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	Vdd	Output	+5V Power	Power Supply Out
2	Vss	Common	PMAC Common	
3	Rs	Output	Read Strobe	TTL Signal Out
4	Vee	Output	Contrast Adjust. VEE	0 to +5 VDC *
5	E	Output	Display Enable	High is Enable
6	R/W	Output	Read or Write	TTL Signal Out
7	DB1	Output	Display Data 1	
8	DB0	Output	Display Data 0	
9	DB3	Output	Display Data 3	
10	DB2	Output	Display Data 2	
11	DB5	Output	Display Data 5	
12	DB4	Output	Display Data 4	
13	DB7	Output	Display Data 7	
14	DB6	Output	Display Data 6	
The JDISP connector is used to drive the 2 line x 24 character (Acc-12), 2 x 40 (Acc-12A) LCD, or the 2 x 40 vacuum fluorescent (Acc. 12C) display unit. The DISPLAY command may be used to send messages and values to the display.				

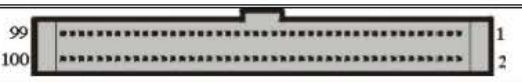
J7 (JHW): Handwheel Encoder Connector

J7 JHW (20-Pin Connector)			Top View 	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	GND	Common	Ref. Voltage	
2	+5V	Output	Supply voltage	To power ext. circuitry
3	HWA1+	Input	HW Pos. A Chan.	Also pulse input

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Pin #	Symbol	Function	Description	Notes
1	GND	Common	Ref. Voltage	
2	+5V	Output	Supply voltage	To power ext. circuitry
3	HWA1+	Input	HW Pos. A Chan.	Also pulse input
4	HWA1-	Input	HW Neg. A Chan.	Also pulse input
5	HWB1+	Input	HW Pos. B Chan.	Also direction input
6	HWB1-	Input	HW Neg. B Chan.	Also direction input
7	HWA2+	Input	HW Pos. A Chan.	Also pulse input
8	HWA2-	Input	HW Neg. A Chan.	Also pulse input
9	HWB2+	Input	HW Pos. B Chan.	Also direction input
10	HWB2-	Input	HW Neg. B Chan.	Also direction input
11	PUL_1+	Output	PFM Pos. Pulse	Also PWM output
12	PUL_1-	Output	PFM Neg. Pulse	Also PWM output
13	DIR_1+	Output	PFM Pos. Dir. Out	Also PWM output
14	DIR_1-	Output	PFM Neg. Dir. Out	Also PWM output
15	PUL_2+/EQU1+	Output	PFM Pos. Pulse	Also PWM output
16	PUL_2-/EQU1-	Output	PFM Neg. Pulse	Also PWM output
17	DIR_2+/EQU2+	Output	PFM Pos. Dir. Out	Also PWM output
18	DIR_2-/EQU2-	Output	PFM Neg. Dir. Out	Also PWM output
19	GND	Common	Ref. Voltage	
20	+5V	Output	Supply Voltage	To power ext. circuitry

J9 (JMACH1): Servo Channel 1 & 2 Connector

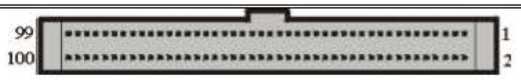
J9 JMACH1 (100-Pin Connector)			Top View 	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	+5V	I/O	+5V Power	For external circuit or from ext. supply
2	+5V	I/O	+5V Power	For external circuit or from ext. supply
3	GND	Common	Reference Voltage	
4	GND	Common	Reference Voltage	
5	CHA1+	Input	Enc. 1 Pos. A Chan.	Also pulse input
6	CHA1-	Input	Enc. 1 Neg. A Chan.	Also pulse input
7	CHB1+	Input	Enc. 1 Pos. B Chan.	Also direction input
8	CHB1-	Input	Enc. 1 Neg. B Chan.	Also direction input
9	CHC1+	Input	Enc. 1 Pos. C Chan.	Index channel
10	CHC1-	Input	Enc. 1 Neg. C Chan.	Index channel
11	CHU1	Input	Chan. 1 U Flag	Hall EFFECT, Fault Code, or SUB-count
12	CHV1	Input	Chan. 1 V Flag	Hall EFFECT, Fault Code, or SUB-count
13	CHW1	Input	Chan. 1 W Flag	Hall EFFECT, Fault Code, or SUB-count
14	CHT1	Input	Chan. 1 T Flag	Fault Code, or SUB-count
15	USER1	Input	Gen. Purpose User Flag	Hardware capture flag, or sub-count
16	PLIM1	Input	Positive Overtravel Limit	Hardware capture flag
17	MLIM1	Input	Negative Overtravel Limit	Hardware capture flag
18	HOME1	Input	Home Switch Input	Hardware capture flag
19	ACCFLT1	Input	Accessory Fault Flag	For loss of acc. supply voltage
20	WD0/	Output	Watchdog Output	Low is PMAC watchdog fault
21	SCLK12+	I/O	Encoder Sample Clock	Direction controlled by PMAC2 jumper
22	SCLK12-	I/O	Encoder Sample Clock	Direction controlled by PMAC2 jumper
23	ADC_CLK1+	Output	A/D Converter Clock	Programmable frequency
24	ADC_CLK1-	Output	A/D Converter Clock	Programmable frequency
25	ADC_STB1+	Output	A/D Converter Strobe	Programmable sequence
26	ADC_STB1-	Output	A/D Converter Strobe	Programmable sequence
27	ADC_DAA1+	Input	Chan A ADC Serial Data	MSB first
28	ADC_DAA1-	Input	Chan A ADC Serial Data	MSB first
29	ADC_DAB1+	Input	Chan B ADC Serial Data	MSB first
30	ADC_DAB1-	Input	Chan B ADC Serial Data	MSB first
31	AENA1+	Output	Amplifier Enable	High is enable
32	AENA1-	Output	Amplifier Enable	Low is enable
33	FAULT1+	Input	Amplifier Fault	Programmable polarity

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28	ADC_DAA1-	Input	Chan A ADC Serial Data	MSB first
29	ADC_DAB1+	Input	Chan B ADC Serial Data	MSB first
30	ADC_DAB1-	Input	Chan B ADC Serial Data	MSB first
31	AENA1+	Output	Amplifier Enable	High is enable
32	AENA1-	Output	Amplifier Enable	Low is enable
33	FAULT1+	Input	Amplifier Fault	Programmable polarity
34	FAULT1-	Input	Amplifier Fault	Programmable polarity
35	PWMATOP1+ DAC_CLK1+	Output	Phase A Top Cmd. or DAC Clock	Programmable function control
36	PWMATOP1- DAC_CLK1-	Output	Phase A Top Cmd. or DAC Clock	Programmable function control
37	PWMABOT1+ DAC1A+	Output	Phase A Bottom Cmd. or DAC A Serial Data	Programmable function control
38	PWMABOT1- DAC1A-	Output	Phase A Bottom Cmd. or DAC A Serial Data	Programmable function control
39	PWMBTOP1+ DAC_STB1+	Output	Phase B Top Cmd. or DAC Strobe	Programmable function control

J9 JMACH1 (100-Pin Connector) (Continued)

Top View

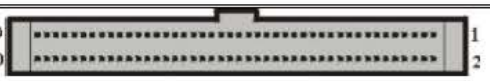


Pin #	Symbol	Function	Description	Notes
40	PWMBTOP1- DAC_STB1-	Output	Phase B Top Cmd. or DAC Strobe	Programmable function control
41	PWMBBOT1+ DAC1B+	Output	Phase B Bottom Cmd. or DAC B Serial Data	Programmable function control
42	PWMBBOT1- DAC1B-	Output	Phase B Bottom Cmd. or DAC B Serial Data	Programmable function control
43	PWMCTOP1+ DIR1+	Output	Phase B Top Cmd. or PFM Direction	Programmable function control
44	PWMCTOP1- DIR1-	Output	Phase B Top Cmd. or PFM Direction	Programmable function control
45	PWMCBOT1+ PULSE1+	Output	Phase B Bottom Cmd. or PFM Pulse	Programmable function control
46	PWMCBOT1- PULSE1-	Output	Phase B Bottom Cmd. or PFM Pulse	Programmable function control
47	GND	Common	Reference Voltage	
48	GND	Common	Reference Voltage	
49	+5V	I/O	+5V Power	For external circuit or from ext. supply
50	+5V	I/O	+5V Power	For external circuit or from ext. supply
51	+5V	I/O	+5V Power	For external circuit or from ext. supply
52	+5V	I/O	+5V Power	For external circuit or from ext. supply
53	GND	Common	Reference Voltage	
54	GND	Common	Reference Voltage	
55	CHA2+	Input	Enc. 2 Pos. A Chan.	Also Pulse input
56	CHA2-	Input	Reference Voltage	Also Pulse input
57	CHB2+	Input	Enc. 2 Pos. B Chan.	Also direction input
58	CHB2-	Input	Enc. 2 Neg. B Chan.	Also direction input
59	CHC2+	Input	Enc. 2 Pos. C Chan.	Index channel
60	CHC2-	Input	Enc. 2 Neg. C Chan.	Index channel
61	CHU2	Input	Chan. 2 U Flag	Hall Effect, Fault Code, or Sub-count
62	CHV2	Input	Chan. 2 V Flag	Hall Effect, Fault Code, or Sub-count
63	CHW2	Input	Chan. 2 W Flag	Hall Effect, Fault Code, or Sub-count
64	CHT2	Input	Chan. 2 T Flag	Fault Code, or Sub-count
65	USER2	Input	Gen. Purpose User flag	Hardware capture flag, or sub-count
66	PLIM2	Input	Pos. Overtravel Limit	Hardware capture flag
67	MLIM2	Input	Neg. Overtravel Limit	Hardware capture flag
68	HOME2	Input	Home Switch Input	Hardware capture flag
69	ACCFLT2	Input	Accessory Fault Flag	For loss of acc. supply voltage
70	WD0/	Output	Watchdog Output	Low is PMAC watchdog fault
71	SCLK12+	I/O	Encoder Sample Clock	Direction controlled by PMAC2 jumper
72	SCLK12-	I/O	Encoder Sample Clock	Direction controlled by PMAC2 jumper
73	ADC_CLK2+	Output	A/D Converter Clock	Programmable frequency
74	ADC_CLK2-	Output	A/D Converter Clock	Programmable frequency
75	ADC_STB2+	Output	A/D Converter Strobe	Programmable sequence

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70	WD0/	Output	Watchdog Output	Low is PMAC watchdog fault
71	SCLK12+	I/O	Encoder Sample Clock	Direction controlled by PMAC2 jumper
72	SCLK12-	I/O	Encoder Sample Clock	Direction controlled by PMAC2 jumper
73	ADC_CLK2+	Output	A/D Converter Clock	Programmable frequency
74	ADC_CLK2-	Output	A/D Converter Clock	Programmable frequency
75	ADC_STB2+	Output	A/D Converter Strobe	Programmable sequence
76	ADC_STB2-	Output	A/D Converter Strobe	Programmable sequence
77	ADC_DAA2+	Input	Chan. A ADC Serial Data	MSB first
78	ADC_DAA2-	Input	Chan. A ADC Serial Data	MSB first
79	ADC_DAB2+	Input	Chan. B ADC Serial Data	MSB first

J9 JMACH1 (100-Pin Connector) (Continued)

Top View 

Pin #	Symbol	Function	Description	Notes
80	ADC_DAB2-	Input	Chan. B ADC Serial Data	MSB first
81	AENA2+	Output	Amplifier Enable	High is enable
82	AENA2-	Output	Amplifier Enable	Low is enable
83	FAULT2+	Input	Amplifier Fault	Programmable polarity
84	FAULT2-	Input	Amplifier Fault	Programmable polarity
85	PWMATOP2+ DAC_CLK2+	Output	Phase A Top Cmd. or DAC Clock	Programmable function control
86	PWMATOP2- DAC_CLK2-	Output	Phase A Top Cmd. or DAC Clock	Programmable function control
87	PWMABOT2+ DAC2A+	Output	Phase A Bottom Cmd. or DAC A Serial Data	Programmable function control
88	PWMABOT2- DAC2A-	Output	Phase A Bottom Cmd. or DAC A Serial Data	Programmable function control
89	PWMBTOP2+ DAC_STB2+	Output	Phase B Top Cmd. or DAC Strobe	Programmable function control
90	PWMBTOP2- DAC_STB2-	Output	Phase B Top Cmd. or DAC Strobe	Programmable function control
91	PWMBBOT2+ DAC2B+	Output	Phase B Bottom Cmd. or DAC B Serial Data	Programmable function control
92	PWMBBOT2- DAC2B-	Output	Phase B Bottom Cmd. or DAC B Serial Data	Programmable function control
93	PWMCTOP2+ DIR2+	Output	Phase B Top Cmd. or PFM Direction	Programmable function control
94	PWMCTOP2- DIR2-	Output	Phase B Top Cmd. or PFM Direction	Programmable function control
95	PWMCBOT2+ PULSE2+	Output	Phase B Bottom Cmd. or PFM Pulse	Programmable function control
96	PWMCBOT2- PULSE2-	Output	Phase B Bottom Cmd. or PFM Pulse	Programmable function control
97	GND	Common	Reference Voltage	
98	GND	Common	Reference Voltage	
99	+5V	I/O	+5V Power	For external circuit or from ext. supply
100	+5V	I/O	+5V Power	For external circuit or from ext. supply

The JMACH1 connector provides the interface pins for channels 1 and 2. It is usually connected to a breakout board, such as one of the ACC-8x family of boards, or an application-specific interface board.

Connector: 100-pin male box header with center key, 0050" pitch. AMP part # 1-04068-7
Delta Tau part # 014-00010-FPB.

TB1: Standalone Power Supply Terminal Block

TB1 (2-Pin Terminal Block)

Top View 

Pin #	Symbol	Function	Description	Notes
1	GND	Common	Reference Voltage	
2	+5V	Input	Positive Supply Voltage	Supplies all PMAC digital circuits

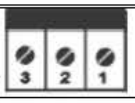
This terminal block can be used to provide the input for the power supply for the circuits on the PMAC2 board when it is not configured to receive its power from the bus connector. Typically, the PMAC2's +5V power is supplied externally come through the bus connector from the bus power supply; in this case, this terminal block should not be used

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1	GND	Common	Reference Voltage	
2	+5V	Input	Positive Supply Voltage	Supplies all PMAC digital circuits

This terminal block can be used to provide the input for the power supply for the circuits on the PMAC2 board when it is not in a bus configuration. When the PMAC2 is in a bus configuration, these supplies automatically come through the bus connector from the bus power supply; in this case, this terminal block should not be used.

TB2: Watchdog Output Terminal Block

TB2 (3-Pin Terminal Block) Top View 

Pin #	Symbol	Function	Description	Notes
1	WD_NC	Output	Watchdog Relay Out	Normally closed
2	COM	Input	Watchdog Return	+V or 0V
3	WD_NO	Output	Watchdog Relay Out	Normally open

This terminal block provides the output for PMAC2's watchdog timer relay, both normally open and normally closed contacts.

Note: The "normally closed" relay contact is open while PMAC2 is operating properly (it has power and the watchdog timer is not tripped) and closed when the PMAC2 is not operating properly (either it has lost power or the watchdog timer has tripped). The "normally open" relay contact is closed while PMAC2 is operating properly, and open when PMAC2 is not operating properly.

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