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# ^1 HARDWARE REFERENCE MANUAL

# PMAC2-Lite

Programmable Multi-Axis Controller

4xx-602406-xHxx

July 17, 2003

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# Table of Contents

**INTRODUCTION** ..... **1**
Overview ..... 1
Board Configuration ..... 1
*Base Version* ..... *1*
*Option 2: Dual Ported RAM* ..... *1*
*Option 5: CPU & Memory Configurations* ..... *2*
*Option 6: Extended Servo Algorithm* ..... *2*
*Option 7: Plate Mounting* ..... *2*
*Option 8: High-Accuracy Clock Crystal* ..... *2*
*Option 9: Serial Port Configuration* ..... *2*
*Option 10: Firmware Version Specification* ..... *2*
*Option 12: Analog-to-Digital Converters* ..... *2*
*Option 16: Battery-Backed Parameter Memory* ..... *3*
Hardware Updates ..... 3
Compatibility Issues ..... 4

**PMAC2-LITE E-POINT DESCRIPTIONS** ..... **5**
E0: Firmware Reload Enable ..... 5
E1: Servo and Phase Clock Direction Control ..... 5
E2: CPU Frequency Select ..... 5
E3: Normal/Re-initializing Power-Up/Reset ..... 5
E4: CPU Frequency Select ..... 6
E5 – E6: (Reserved for Future Use) ..... 6
E7 – E10: Host Interrupt Signal Select ..... 6
E11-12: JEQU Port Configuration ..... 7
E13: Encoder Sample Clock Direction Control ..... 7
E14: Watchdog Disable Jumper ..... 7
E17 – E18: Serial Port Select ..... 8
E20: Battery-Backed RAM Enable ..... 8
E111-114: Command Output Disable State ..... 9
DIP Switch Block S1: ISA-BUS Address Select ..... 10

**HOST PC-AT I/O ADDRESS MAP** ..... **11**

**PMAC2-LITE MATING CONNECTORS** ..... **13**
J1 (JANA)/Analog (Option 12) ..... 13
J2 (JTHW)/Multiplexer Port ..... 13
J3 (JIO)/Digital I/O ..... 13
J4 (JMACRO)/MACRO Digital Data ..... 13
J5 (JRS232)/RS-232 Serial Communications ..... 13
J5A (JRS422)/RS-422 Serial Communications ..... 13
J6 (JDISP)/Display ..... 13
J7 (JHW)/Auxiliary Channel ..... 14
J8 (JEQU)/Position Compare ..... 14
J9 (JMACH1)/Machine Port 1 ..... 14
J10 (JMACH2)/Machine Port 2 ..... 14
J11 (JEXP)/Expansion ..... 14

**PMAC2-LITE CONNECTOR PINOUTS** ..... **15**
J1 (JANA) Analog Input Port Connector ..... 15
J2 (JTHW) Multiplexer Port Connector ..... 16
J3 (JIO) General Input/Output Connector ..... 17
J4 (JMACRO) MACRO Network Ring Interface Connector ..... 18



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J5 (JRS232) Serial Port Connector ..... 19
J5A (JRS422) RS422 Serial Port Connector ..... 20
J6 (JDISP) Display Connector ..... 21
J7 (JHW) Handwheel Encoder Connector ..... 21
J8 (JEQU) Position Compare Output Connector ..... 22
J9 (JMACH1) Servo Channel 1 & 2 Connector ..... 23
J10 (JMACH2) Servo Channel 3 & 4 Connector ..... 27
TB1 (2/4-Pin Terminal Block) ..... 30
TB2 (4-Pin Terminal Block) ..... 31



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# INTRODUCTION

## Overview

The PMAC2-Lite is a member of the PMAC2 family of boards optimized for interface to three or four sinewave or direct PWM servo drives and to pulse-and-direction stepper drives. It has two channels of servo interface circuitry, but its software is capable of eight axes of control. It is completely software compatible with the PMAC2-PC and the Mini-PMAC2.

The PMAC2-Lite is a full-sized ISA-bus expansion card, with a small piggyback board containing the CPU board. While the PMAC2-Lite is capable of ISA bus communications, with or without the optional on-board dual-ported RAM, it does not need to be inserted into an ISA expansion slot. Communications can be done through the standard on-board RS-232 serial port. Standalone operation is possible.

## Board Configuration

### Base Version

The base version of the PMAC2-Lite provides a 2/3-slot board with:

- 40 MHz DSP56002 CPU
- 128k x 24 zero-wait-state SRAM active memory
- 512k x 8 flash memory for user backup and firmware
- Latest released firmware version
- RS-232 serial interface, ISA (PC) bus interface
- One 16-node MACRO interface IC
- Four channels axis interface circuitry, each including:
  - Three output command signal sets, configurable as either:
    - Two serial data streams to external DACs, one pulse-and-direction
    - Three PWM top-and-bottom pairs
  - 3-channel differential/single-ended encoder input
  - Nine input flags, 2 output flags
  - Interface to two external serial ADCs, 8 to 18 bits
- Two channels supplemental interface circuitry, each including:
  - Two-channel differential/single-ended encoder input
  - One output command signal set, configurable as pulse-&-direction or PWM top-and-bottom pair
- Display, MACRO, muxed I/O, direct I/O interface ports
- PID/notch/feedforward servo algorithms
- 1-year warranty from date of shipment
- One manual per set of one to four PMACs shipped
- Cables, mounting plates, mating connectors not included

### Option 2: Dual Ported RAM

Dual-ported RAM provides a high-speed communications path for bus communications with the host computer through a bank of shared memory. DPRAM is advised if more than 100 data items per second are to be passed between the controller and the host computer in either direction.



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Option 2 provides an on-board 8k x 16 bank of dual-ported RAM. The key component on the board is U23.

## Option 5: CPU & Memory Configurations

If the 40MHz CPU that comes standard does not have sufficient computational power, faster versions are available as options. These options provide faster CPU ICs in U7 and faster SRAM ICs in U58, U59, and U60.

- Option 5B provides a 60MHz CPU with zero-wait-state SRAM active memory.
- Option 5C provides an 80MHz CPU with zero-wait-state SRAM active memory.

## Option 6: Extended Servo Algorithm

The standard PID servo algorithm with feedforward and notch filter is suitable for most applications. Systems with difficult dynamics, especially with significant flexibility, may require a more powerful servo algorithm, such as the Extended Servo Algorithm (ESA).

- Option 6 provides firmware in the PMAC2-Lite that replaces the standard PID servo algorithm with the Extended Servo Algorithm.

## Option 7: Plate Mounting

If the PMAC2-Lite is used as an ISA bus expansion board, the standard hardware provides for proper mounting of the board in the bus. However, if it is not installed in an ISA expansion slot, other provisions must be made for mounting.

- Option 7 provides a mounting plate connected to the PMAC2-Lite with standoffs. It is used to install the PMAC2-Lite in standalone applications.

## Option 8: High-Accuracy Clock Crystal

The PMAC2-Lite has a clock crystal (component Y1) of nominal frequency 19.6608MHz (~20MHz). The standard crystal's accuracy specification is +/-100 ppm. Long-term velocity accuracy is limited by the accuracy of the crystal, unless an external time base is used.

- Option 8A provides a nominal 19.6608MHz crystal with a +/-15 ppm accuracy specification.

## Option 9: Serial Port Configuration

The original standard PMAC2-Lite (602406-100) included a single RS-232 serial port. Optionally, this could be converted to RS-422, and a second serial port can be added. On the Universal PMAC2-Lite (602406-101 and newer), both the RS-232 and RS-422 ports come standard. Jumpers E17 and E18 select which port is used.

- On the original PMAC2-Lite, Option 9L replaces main RS-232 port with an RS-422 port on a small piggyback board. This option is not available on the Universal PMAC2-Lite.

## Option 10: Firmware Version Specification

Normally, the newest released firmware version is provided with the PMAC2-Lite. A label on the U61 flash memory IC on the CPU board shows the firmware version loaded at the factory.

- Option 10 provides for a user-specified firmware version.

## Option 12: Analog-to-Digital Converters

Option 12 permits the installation of 8 or 16 channels of on-board multiplexed analog-to-digital converters. One or two of these converters are read every phase interrupt. The analog inputs are not optically isolated, and each can have a 0 – 5V input range, or a +/-2.5V input range, individually selectable.



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- Option 12 provides an 8-channel 12-bit A/D converter. The key components on the board are U28 and connector J1.
- Option 12A provides an additional 8-channel 12-bit A/D converter. The key component on the board is U29.

### Option 16: Battery-Backed Parameter Memory

The contents of the standard memory are not retained through a power-down or reset unless they have been saved to flash memory first. Option 16 provides supplemental battery-backed RAM for real-time parameter storage that is ideal for holding machine state parameters in case of an unexpected power-down.

- Option 16 provides a 16k x 24 bank of battery-backed parameter RAM in components U84, U85, U86, with the battery in BT1.

## Hardware Updates

Significant upgrades were made to the PMAC2-Lite board between the original 602406-100 version and the 602406-101 version. These included replacement of obsolescent circuitry, feature enhancement, and changes for more cost-effective manufacturing. The upgrades include:

- **80 MHz CPU**: The new PMAC2-Lite supports the Option 5C 80 MHz CPU for high-end operations.
- **Supplemental Battery-Backed Parameter Memory**: The new PMAC2-Lite supports the Option 16 supplemental battery-backed parameter memory to complement the flash-backed main memory.
- **Raised Bottom Edge**: The bottom edge of the board has been raised so that it can clear high-profile parts on the PC mother board – up to 25mm (1 inch) high.
- **Standard RS-422 Serial Port**: An RS-422 serial interface, which formerly required the Option 9L piggyback board, now is standard. Jumpers E17 and E18 must be set properly to select between the RS-232 port and the RS-422 port.
- **Improved ADC Protection Circuitry**: The protection circuitry for the Option 12 A/D converters no longer has the potential to distort the input slightly near 5V.
- **Encoder-Loss Detection Circuitry**: Circuitry that detects the loss of differential encoders has been added.
- **Improved Position Compare Drive**: The socket for U74 has been enlarged to 20 pins to support the 74ACT563 and 573 high-speed CMOS drivers for the JEQU port as well as the slower 18-pin 24V driver ICs. In addition, a 2A fuse has been added to the +V input on the JEQU port.
- **Increased Use of Surface Mount Technology**: Several components have been changed from through-hole to surface-mount, for better part availability and lower cost.
- **Expanded JMACRO Connector**: The J4 JMACRO connector has been expanded from 26 pins to 34 pins, separating the input and output lines to reduce crosstalk, and permitting a straight flat-cable connection to the ACC-24P2 MACRO Driver/Receiver board.
- **Tristatable Servo Output Signals**: Jumpers E111 through E114 permit the user to tristate the servo command output signals automatically for channels 1 through 4, respectively, when the amplifier-enable signal for the channel is in the disable state.
- **In-System-Programmable Logic**: Interface logic ICs can now be programmed when installed in the PMAC2-Lite, permitting elimination of sockets for higher reliability, and easier manufacturing and upgradability.



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## Compatibility Issues

The new PMAC2-Lite can be operated in a manner that is 100% compatible with the old PMAC2-Lite. The board is shipped from the factory with settings for 100% compatible operation. To ensure an operation is compatible, double-check the following settings:

- **Raised Bottom Edge**: The higher bottom edge moves the lower left mounting hole for standoffs up 12.7 mm (0.5 in). If using standoff mounting, and the matching mounting hole cannot be moved, contact Delta Tau for free offset standoffs.
- **Serial Port Choice**: Because both RS-232 and RS-422 ports are always provided, jumpers must be set correctly to use the port of choice. Jumpers E17 and E18 must connect pins 1 and 2 to use the RS-232 port on the J4 connector; to use the RS-422 port on the J4A connector, they must connect pins 2 and 3
- **Surface Mount DIP Switch**: Instead of a single 12-point DIP switch S1, there is an 8-point DIP switch S1A and a 4-point DIP switch S1B. New S1A switches 1-8 correspond to old S1 switches 1-8, respectively; new S1B switches 1-4 correspond to old S1 switches 9-12, respectively.
- **TriState Output Jumpers**: Jumpers E111-E114 should be all OFF so that the servo output signals stay enabled (not tristated) when the amplifier-enable signal for the channel is in the disable state.
- **Firmware Reload**: Putting jumper E3 ON is now for re-initialization to factory default values only. Firmware reload is set up by jumping pins 2 and 3 of E0.
- **Position Compare Driver IC**: If an 18-pin ULN2803A or UDN2981A driver IC is installed in the 20-pin U74 DIP socket, it should be mounted in the right-most 18 pins.



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# PMAC2-LITE E-POINT DESCRIPTIONS

## E0: Firmware Reload Enable

| E Point & Physical Layout | Location | Description | Default |
|---|---|---|---|
| **E0**<br>(1)<br>(2)<br>(3) | | Remove jumper for normal operation<br>Jump pin 1 to 2 to reload firmware through serial or bus port.<br>Jump pin 2 to 3 to lock PMAC2 in reset state (for factory use only). | No jumper installed |
| **Note:** On –100 versions of the PMAC2-Lite, the firmware reload function was accomplished by putting jumper E3 ON and giving the board a <CTRL-O> command. | | | |

## E1: Servo and Phase Clock Direction Control

| E Point & Physical Layout | Location | Description | Default |
|---|---|---|---|
| **E1**<br> | | Remove jumper for PMAC2-Lite to use its internally generated servo and phase clock signals and to output these signals on the J5 serial port connector.<br>Jump pins 1 and 2 for PMAC2-Lite to expect to receive its servo and phase clock signals on the J5 serial port connector. | No jumper installed |
| **Note:** If the E1 jumper is ON and the servo and phase clocks are not brought in on the J5 serial port, the watchdog timer will trip immediately. | | | |

## E2: CPU Frequency Select

| E Point & Physical Layout | Location | Description | Default |
|---|---|---|---|
| **E2**<br> | | Remove jumper for 40MHz operation (E4 OFF also) or for 80MHz operation (E4 ON).<br>Jump pin 1 to 2 for 60MHz operation (E4 OFF). | No jumper installed (standard or Opt 5C)<br>Jumper installed (Opt 5B) |

## E3: Normal/Re-initializing Power-Up/Reset

| E Point & Physical Layout | Location | Description | Default |
|---|---|---|---|
| **E3**<br> | | Jump pin 1 to 2 to re-initialize on power-up/reset, loading factory default settings.<br>Remove jumper for normal power-up/reset, loading user-saved settings. | No jumper installed |
| **Note:** On –100 versions of the PMAC2-Lite board, this jumper was used both for re-initialization and for firmware reload. With this jumper ON, after power-up/reset, a <CTRL-R> command would load factory default settings; a <CTRL-O> command would prepare the card for loading of new firmware. Now E0 permits loading of new firmware. | | | |



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## E4: CPU Frequency Select

| E Point & Physical Layout | Location | Description | Default |
|---|---|---|---|
| **E4**  | | Remove jumper for 40MHz operation (E2 OFF also) or for 60MHz operation (E4 ON).<br>Jump pin 1 to 2 for 80MHz operation (E2 OFF). | No jumper installed (standard or Opt 5B)<br>Jumper installed (Opt 5C) |
| **Note:** On –100 versions of the PMAC2-Lite board, the maximum CPU frequency supported was 60 MHz, so this jumper was to be OFF in all cases. | | | |

## E5 – E6: (Reserved for Future Use)

## E7 – E10: Host Interrupt Signal Select

| E Point & Physical Layout | Location | Description | Default |
|---|---|---|---|
| **E7**  | A9 | Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ10. | No jumper installed |
| **E8**  | A9 | Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ11. | No jumper installed |
| **E9**  | A9 | Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ12. | No jumper installed |
| **E10**  | A9 | Jump pin 1 to 2 to allow PMAC Interrupt to host-PC on IRQ15. | No jumper installed |
| **Note:** Only one of the jumpers E7 – E10 should be ON at any one time. | | | |



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## E11-12: JEQU Port Configuration

| E Point & Physical Layout | Description | Default |
|---|---|---|
| **E11**<br> | **JEQU port configuration:**<br>Jump pins 1 to 2 for sinking driver (ULN2803a) on port (default configuration)<br>Jump pins 2 to 3 for sourcing driver (UDN 2981a) on port (alternate configuration) | 1 - 2 JUMPERED |
| **E12**<br> | **JEQU port configuration:**<br>Jump pins 1 to 2 for sinking driver (ULN 2803a) on JEQU port (default configuration) jump pins 2 to 3 for sourcing driver (UDN2981a) on JEQU port (alternate configuration) | 1 - 2 JUMPERED |

## E13: Encoder Sample Clock Direction Control

| E Point & Physical Layout | Location | Description | Default |
|---|---|---|---|
| **E13**<br>(1)<br>(2)<br>(3) | | Remove jumper to output SCLK generated in servo ASIC on SCLK_12 and SCLK_34, or to control direction by software.<br>Jump pins 1 to 2 to input SCLK signal for servo ASIC on SCLK_34 and output this signal on SCLK_12.<br>Jump pins 2 to 3 to input SCLK signal for servo ASIC on SCLK_12 and output this signal on SCLK_34. | No jumper installed |

## E14: Watchdog Disable Jumper

| E Point & Physical Layout | Location | Description | Default |
|---|---|---|---|
| **E14**<br> | | Jump pin 1 to 2 to disable Watchdog timer (for test purposes only).<br>Remove jumper to enable Watchdog timer. | No jumper installed |



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## E17 – E18: Serial Port Select

| E Point & Physical Layout | Location | Description | Default |
|---|---|---|---|
| **E17**   | | Jump E17 pin 1 to 2 to select RS-232 serial data input from J5.<br>Jump E17 pin 2 to 3 to select RS-422 serial data input from J5A | Pins 1 – 2 jumpered |
| **E18**   | | Jump E18 pin 1 to 2 to select RS-232 serial handshake input from J5.<br>Jump E17 pin 2 to 3 to select RS-422 serial handshake input from J5A | Pins 1 – 2 jumpered |

## E20: Battery-Backed RAM Enable

| E Point & Physical Layout | Location | Description | Default |
|---|---|---|---|
| **E20**   | | Jump pins 1 to 2 if Option 16 battery-backed RAM is present in U84, U85 & U86.<br>Jump pins 2 to 3 if Option 16 battery-backed RAM is not present in U84, U85, & U86. | 2-3 jumper installed (no Opt 16)<br>1-2 jumper installed (Opt 16) |
| Note: If no Battery Backed memory option ordered, this jumper does not exist. | | | |



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## E111-114: Command Output Disable State

| E Point & Physical Layout | Location | Description | Default |
|---|---|---|---|
| **E111**  | | Jump pin 1 to 2 for digital servo command output signals of Channel 1 to tri-state when amplifier-enable signal for Channel 1 is in disable state.<br><br>Remove jumper for digital servo command output signals of Channel 1 to remain active (but typically with zero command value) when amplifier-enable signal for Channel 1 is in disable state. | No jumper installed |
| **E112**  | | Jump pin 1 to 2 for digital servo command output signals of Channel 2 to tri-state when amplifier-enable signal for Channel 2 is in disable state.<br><br>Remove jumper for digital servo command output signals of Channel 2 to remain active (but typically with zero command value) when amplifier-enable signal for Channel 2 is in disable state. | No jumper installed |
| **E113**  | | Jump pin 1 to 2 for digital servo command output signals of Channel 3 to tri-state when amplifier-enable signal for Channel 3 is in disable state.<br><br>Remove jumper for digital servo command output signals of Channel 3 to remain active (but typically with zero command value) when amplifier-enable signal for Channel 3 is in disable state. | No jumper installed |
| **E114**  | | Jump pin 1 to 2 for digital servo command output signals of Channel 4 to tri-state when amplifier-enable signal for Channel 4 is in disable state.<br><br>Remove jumper for digital servo command output signals of Channel 4 to remain active (but typically with zero command value) when amplifier-enable signal for Channel 4 is in disable state. | No jumper installed |



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## DIP Switch Block S1: ISA-BUS Address Select

| S1B | | | | S1A | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 | 3 | 2 | 1 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| ⇑ | ⇑ | ⇑ | ⇑ | ⇑ | ⇑ | ⇑ | ⇑ | ⇑ | ⇑ | ⇑ | ⇑ |
| ⇓ | ⇓ | ⇓ | ⇓ | ⇓ | ⇓ | ⇓ | ⇓ | ⇓ | ⇓ | ⇓ | ⇓ |
| ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON |

The 12 DIP switches on block S1 set the base address of the PMAC2 on the PC bus. Together they form a binary number. Each switch, if in the ON (closed) position, sets its bit to 0; if in the OFF (open) position, sets its bit to 1. The possible base addresses are all multiples of 16, so switch 1 sets a bit value of 16, switch 2 sets a bit value of 32, and so on.

| Switch # | Bit Value | Default | Default Value | Your Value |
|---|---|---|---|---|
| 1 (S1A-1) | 16 (10h) | ON (x1) | 16 (10h) | |
| 2 (S1A-2) | 32 (20h) | OFF (x0) | 0 | |
| 3 (S1A-3) | 64 (40h) | OFF (x0) | 0 | |
| 4 (S1A-4) | 128 (80h) | OFF (x0) | 0 | |
| 5 (S1A-5) | 256 (100h) | OFF (x0) | 0 | |
| 6 (S1A-6) | 512 (200h) | ON (x1) | 512 (200h) | |
| 7 (S1A-7) | 1024 (400h) | OFF (x0) | 0 | |
| 8 (S1A-8) | 2048 (800h) | OFF (x0) | 0 | |
| 9 (S1B-1) | 4096 (1000h) | OFF (x0) | 0 | |
| 10 (S1B-2) | 8192 (2000h) | OFF (x0) | 0 | |
| 11 (S1B-3) | 16384 (4000h) | OFF (x0) | 0 | |
| 12 (S1B-4) | 32768 (8000h) | OFF (x0) | 0 | |
| Total | -- | -- | 528 (210h) | |

To set the board to a different bus address, specify that address in hexadecimal form, because each hex digit corresponds to four switches. The last hex digit of the base address is always zero.

For example, to set the base address on the PC bus to 992 decimal, or 03E0 hex. The first '0' corresponds to switches 9 through 12. All of these should be ON to set their bits to zero. The '3' corresponds to switches 5 through 8. Switches 8 and 7 should be ON, and switches 6 and 5 should be OFF to define the '3'. The 'E' corresponds to switches 1 through 4. Switches 4, 3, and 2 should be OFF, and switch 1 should be ON to define the 'E'.

| **Switch #** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **-** | **-** | **-** | **-** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Hex** | | | | 0 | | | | 3 | | | | E | | | | 0 |
| **Binary** | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| **Setting** | on | on | on | on | on | on | off | off | off | off | off | on | - | - | - | - |



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# HOST PC-AT I/O ADDRESS MAP

| Hex Range | Dec Range | Usage |
|---|---|---|
| 000-01F | 0-31 | DMA Controller 1 8237A-5 |
| 020-03F | 32-63 | Interrupt Controller 1 8259A |
| 040-05F | 64-67 | Timer 8254-2 |
| 060-06F | 96-111 | 8042 (Keyboard) |
| 070-07F | 112-127 | Real-time clock, NMI mask |
| 080-09F | 128-159 | DMA Page Registers |
| 0A0-0BF | 160-191 | Interrupt Controller 2 8259A |
| 0C0-0DF | 192-223 | DMA Controller 2 8237A-5 |
| 0F0-0FF | 240-255 | Math CO processor |
| 1F0-1F8 | 496-504 | Fixed Disk |
| 200-20F | 512-527 | Game Control |
| 210-217 | 528-535 | Expansion Unit (usually open) |
| 278-27F | 632-639 | Parallel Printer: LPT2 |
| 2B0-2DF | 688-735 | Alternate EGA |
| 2F8-2FF | 760-767 | Asynchronous Common: COM2 |
| 300-31F | 768-799 | Prototype Card (usually open) |
| 360-36F | 864-879 | PC Network |
| 378-37F | 888-895 | Parallel Printer: LPT1 |
| 380-38F | 896-911 | SDLC Communications 2 |
| 390-393 | 912-915 | Cluster |
| 3A0-3A9 | 928-937 | SDLC Communications 1 |
| 3B0-3BF | 944-959 | IBM Monochrome Display/Printer |
| 3C0-3CF | 960-975 | Enhanced Graphics Adapter |
| 3D0-3DF | 976-991 | Color/Graphics |
| 3F0-3F7 | 1000-1015 | Diskette Controller |
| 3F8-3FF | 1016-1023 | Asynchronous Common.: COM1 |
| x2E1 | | GPIB Adapter |
| x390-x393 | | Cluster Adapter |

The above chart helps prevent possible contention with existing I/O. If a contention occurs, try a new unused address.

Contention is exhibited by:

- Total Malfunction
- Partial Function, Input O.K., Output bad or vice versa
- Intermittent operation



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# PMAC2-LITE MATING CONNECTORS

## J1 (JANA)/Analog (Option 12)

1. Two 14-pin female flat cable connector Delta Tau P/N 014-R00F14-0K0 - T&B Ansley P/N 609-1441
2. 171-14 T&B Ansley standard flat cable stranded 14-wire
3. Phoenix varioface modules type FLKM14 (male pins) P/N 22 81 02 1

## J2 (JTHW)/Multiplexer Port

1. Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 – T&B Ansley P/N 609-2641
2. 171-26 T&B Ansley standard flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

## J3 (JIO)/Digital I/O

1. Two 40-pin female flat cable connector Delta Tau P/N 014-R00F40-0K0 – T&B Ansley P/N 609-4041
2. 171-40 T&B Ansley standard flat cable stranded 40-wire
3. Phoenix varioface module type FLKM 40 (male pins)

## J4 (JMACRO)/MACRO Digital Data

1. Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 – T&B Ansley P/N 609-2641
2. 171-26 T&B Ansley standard flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

## J5 (JRS232)/RS-232 Serial Communications

1. Two 10-pin female flat cable connector Delta Tau P/N 014-ROOF10-0K0 – T&B Ansley P/N 609-1041
2. 171-10 T&B Ansley standard flat cable stranded 10-wire
3. Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

## J5A (JRS422)/RS-422 Serial Communications

1. Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 – T&B Ansley P/N 609-2641
2. 171-26 T&B Ansley standard flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

## J6 (JDISP)/Display

1. Two 14-pin female flat cable connector Delta Tau P/N 014-R00F14-0K0 – T&B Ansley P/N 609-1441
2. 171-14 T&B Ansley standard flat cable stranded 14-wire
3. Phoenix varioface modules type FLKM14 (male pins) P/N 22 81 02 1



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## J7 (JHW)/Auxiliary Channel

1. Two 20-pin female flat cable connector Delta Tau P/N 014-R00F20-0K0 – T&B Ansley P/N 609-2041
2. 171-20 T&B Ansley standard flat cable stranded 20-wire
3. Phoenix varioface modules type FLKM20 (male pins)

## J8 (JEQU)/Position Compare

1. Two 10-pin female flat cable connector Delta Tau P/N 014-ROOF10-0K0 – T&B Ansley P/N 609-1041
2. 171-10 T&B Ansley standard flat cable stranded 10-wire
3. Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

## J9 (JMACH1)/Machine Port 1

1. Two 100-pin high-density box header with center key, 0.050” pitch – AMP P/N 1-04068-7, Delta Tau P/N 014-00010-FPB
2. High-density flat cable stranded 100-wire

## J10 (JMACH2)/Machine Port 2

1. Two 100-pin high-density box header with center key, 0.050” pitch – AMP P/N 1-04068-7, Delta Tau P/N 014-00010-FPB
2. High-density flat cable stranded 100-wire

## J11 (JEXP)/Expansion

1. Two 50-pin female flat cable connector Delta Tau P/N 014-R00F50-0K0 – T&B Ansley P/N 609-5041
2. 171-50 T&B Ansley standard flat cable stranded 50-wire
3. Phoenix varioface module type FLKM 50 (male pins) P/N 22 81 08 9



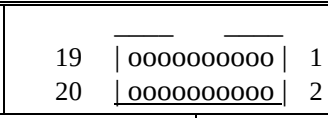
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# PMAC2-LITE CONNECTOR PINOUTS

## J1 (JANA) Analog Input Port Connector

### J1 JANA (20-Pin Connector)

(Present only if Option 12 ordered)




| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 1 | ANAI00 | Input | Analog Input 0 | 0-5V or +/-2.5V range |
| 2 | ANAI01 | Input | Analog Input 1 | 0-5V or +/-2.5V range |
| 3 | ANAI02 | Input | Analog Input 2 | 0-5V or +/-2.5V range |
| 4 | ANAI03 | Input | Analog Input 3 | 0-5V or +/-2.5V range |
| 5 | ANAI04 | Input | Analog Input 4 | 0-5V or +/-2.5V range |
| 6 | ANAI05 | Input | Analog Input 5 | 0-5V or +/-2.5V range |
| 7 | ANAI06 | Input | Analog Input 6 | 0-5V or +/-2.5V range |
| 8 | ANAI07 | Input | Analog Input 7 | 0-5V or +/-2.5V range |
| 9 | ANAI08 | Input | Analog Input 8 | 0-5V or +/-2.5V range |
| 10 | ANAI09 | Input | Analog Input 9 | 0-5V or +/-2.5V range |
| 11 | ANAI10 | Input | Analog Input 10 | 0-5V or +/-2.5V range |
| 12 | ANAI11 | Input | Analog Input 11 | 0-5V or +/-2.5V range |
| 13 | ANAI12 | Input | Analog Input 12 | 0-5V or +/-2.5V range |
| 14 | ANAI13 | Input | Analog Input 13 | 0-5V or +/-2.5V range |
| 15 | ANAI14 | Input | Analog Input 14 | 0-5V or +/-2.5V range |
| 16 | ANAI15 | Input | Analog Input 15 | 0-5V or +/-2.5V range |
| 17 | GND | Common | PMAC common | Not isolated from digital |
| 18 | +12V | Output | Positive supply voltage | To power external circuitry |
| 19 | GND | Common | PMAC common | Not isolated from digital |
| 20 | -12V | Output | Negative supply voltage | To power external circuitry |

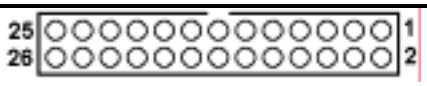
The JANA connector provides the inputs for the 8 or 16 optional analog inputs on the PMAC2.



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## J2 (JTHW) Multiplexer Port Connector

**J2 JTHW (26-Pin Connector)**



Front View

| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 1 | GND | Common | PMAC common | |
| 2 | GND | Common | PMAC common | |
| 3 | DAT0 | Input | Data-0 input | Data input from MUX port accessories |
| 4 | SEL0 | Output | Select-0 output | Address/data output for MUX port accessories |
| 5 | DAT1 | Input | Data -1 input | Data input from MUX port accessories |
| 6 | SEL1 | Output | Select -1 output | Address/data output for MUX port accessories |
| 7 | DAT2 | Input | Data -2 input | Data input from MUX port accessories |
| 8 | SEL2 | Output | Select -2 output | Address/data output for MUX port accessories |
| 9 | DAT3 | Input | Data -3 input | Data input from MUX port accessories |
| 10 | SEL3 | Output | Select -3 output | Address/data output for MUX port accessories |
| 11 | DAT4 | Input | Data -4 input | Data input from MUX port accessories |
| 12 | SEL4 | Output | Select -4 output | Address/data output for MUX port accessories |
| 13 | DAT5 | Input | Data -5 input | Data input from MUX port accessories |
| 14 | SEL5 | Output | Select -5 output | Address/data output for MUX port accessories |
| 15 | DAT6 | Input | Data -6 input | Data input from MUX port accessories |
| 16 | SEL6 | Output | Select -6 output | Address/data output for MUX port accessories |
| 17 | DAT7 | Input | Data -7 input | Data input from MUX port accessories |
| 18 | SEL7 | Output | Select -7 output | Address/data output for MUX port accessories |
| 19 | N.C. | N.C. | No connection | |
| 20 | GND | Common | PMAC common | |
| 21 | BRLD/ | Output | Buffer request | Low is buffer request |
| 22 | GND | Common | PMAC common | |
| 23 | IPLD/ | Output | In position | Low is in position |
| 24 | GND | Common | PMAC common | |
| 25 | +5V | Output | +5Vdc supply | Power supply out |
| 26 | INIT/ | Input | PMAC reset | Low is reset |

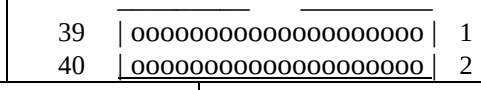
The JTHW connector provides eight inputs and eight outputs at TTL levels; PMAC software supports the use of multiplexed I/O on this port.



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## J3 (JIO) General Input/Output Connector

### J3 JIO (40-Pin Connector)




| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 1 | I/O00 | In/Out | Digital I/O 0 | Software direction control |
| 2 | I/O01 | In/Out | Digital I/O 1 | Software direction control |
| 3 | I/O02 | In/Out | Digital I/O 2 | Software direction control |
| 4 | I/O03 | In/Out | Digital I/O 3 | Software direction control |
| 5 | I/O04 | In/Out | Digital I/O 4 | Software direction control |
| 6 | I/O05 | In/Out | Digital I/O 5 | Software direction control |
| 7 | I/O06 | In/Out | Digital I/O 6 | Software direction control |
| 8 | I/O07 | In/Out | Digital I/O 7 | Software direction control |
| 9 | I/O08 | In/Out | Digital I/O 8 | Software direction control |
| 10 | I/O09 | In/Out | Digital I/O 9 | Software direction control |
| 11 | I/O10 | In/Out | Digital I/O 10 | Software direction control |
| 12 | I/O11 | In/Out | Digital I/O 11 | Software direction control |
| 13 | I/O12 | In/Out | Digital I/O 12 | Software direction control |
| 14 | I/O13 | In/Out | Digital I/O 13 | Software direction control |
| 15 | I/O14 | In/Out | Digital I/O 14 | Software direction control |
| 16 | I/O15 | In/Out | Digital I/O 15 | Software direction control |
| 17 | I/O16 | In/Out | Digital I/O 16 | Software direction control |
| 18 | I/O17 | In/Out | Digital I/O 17 | Software direction control |
| 19 | I/O18 | In/Out | Digital I/O 18 | Software direction control |
| 20 | I/O19 | In/Out | Digital I/O 19 | Software direction control |
| 21 | I/O20 | In/Out | Digital I/O 20 | Software direction control |
| 22 | I/O21 | In/Out | Digital I/O 21 | Software direction control |
| 23 | I/O22 | In/Out | Digital I/O 22 | Software direction control |
| 24 | I/O23 | In/Out | Digital I/O 23 | Software direction control |
| 25 | I/O24 | In/Out | Digital I/O 24 | Software direction control |
| 26 | I/O25 | In/Out | Digital I/O 25 | Software direction control |
| 27 | I/O26 | In/Out | Digital I/O 26 | Software direction control |
| 28 | I/O27 | In/Out | Digital I/O 27 | Software direction control |
| 29 | I/O28 | In/Out | Digital I/O 28 | Software direction control |
| 30 | I/O29 | In/Out | Digital I/O 29 | Software direction control |
| 31 | I/O30 | In/Out | Digital I/O 30 | Software direction control |
| 32 | I/O31 | In/Out | Digital I/O 31 | Software direction control |
| 33 | GND | Common | Reference voltage | |
| 34 | GND | Common | Reference voltage | |
| 35 | PHASE/ | Output | Phase clock | For latching data |
| 36 | SERVO/ | Output | Servo clock | For latching data |
| 37 | GND | Common | Reference voltage | |
| 38 | GND | Common | Reference voltage | |
| 39 | +5V | Output | Supply voltage | To power external circuitry |
| 40 | +5V | Output | Supply voltage | To power external circuitry |

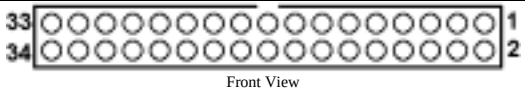
The JI/O connector provides 32 input/output pins at TTL levels. Direction can be controlled in byte-wide groups.



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## J4 (JMACRO) MACRO Network Ring Interface Connector

**J4 JMACRO (34-Pin Connector)**



Front View

| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 1 | DOUT7 | Output | Ring out bit 7 | Macro ring command |
| 2 | DOUT6 | Output | Ring out bit 6 | Macro ring transmit |
| 3 | DOUT5 | Output | Ring out bit 5 | Macro ring transmit |
| 4 | DOUT4 | Output | Ring out bit 4 | Macro ring transmit |
| 5 | DOUT3 | Output | Ring out bit 3 | Macro ring transmit |
| 6 | DOUT2 | Output | Ring out bit 2 | Macro ring transmit |
| 7 | DOUT1 | Output | Ring out bit 1 | Macro ring transmit |
| 8 | DOUT0 | Output | Ring out bit 0 | Macro ring transmit |
| 9 | CMD_OUT | Output | | |
| 10 | GND | Common | Reference voltage | |
| 11 | GND | Common | Reference voltage | |
| 12 | STB_OUT | Output | Byte strobe | |
| 13 | GND | Common | Reference voltage | |
| 14 | GND | Common | Reference voltage | |
| 15 | GND | Common | Reference voltage | |
| 16 | TCLK | Output | Ring clock | 12.5MHz |
| 17 | GND | Common | Reference voltage | |
| 18 | GND | Common | Reference voltage | |
| 19 | DIN7 | Input | Ring in bit 7 | Macro ring receive |
| 20 | DIN6 | Input | Ring in bit 6 | Macro ring receive |
| 21 | DIN5 | Input | Ring in bit 5 | Macro ring receive |
| 22 | DIN4 | Input | Ring in bit 4 | Macro ring receive |
| 23 | DIN3 | Input | Ring in bit 3 | Macro ring receive |
| 24 | DIN2 | Input | Ring in bit 2 | Macro ring receive |
| 25 | DIN1 | Input | Ring in bit 1 | Macro ring receive |
| 26 | DIN0 | Input | Ring in bit 0 | Macro ring receive |
| 27 | CMD_IN | Input | | |
| 28 | GND | Common | Reference voltage | |
| 29 | GND | Common | Reference voltage | |
| 30 | DAT_STB | Input | Data byte strobe | |
| 31 | GND | Common | Reference voltage | |
| 32 | CMD_STB | Input | Command byte strobe | |
| 33 | GND | Common | Reference voltage | |
| 34 | VLTN | Input | Violation flag | Taxi chip receive error |

The JMACRO connector provides the interface to the ACC-42P2 MACRO driver/receiver accessory board, permitting the PMAC2-Lite to command axes and I/O through the MACRO ring.



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## J5 (JRS232) Serial Port Connector

### J5 JRS232 (10-Pin Connector)



Front View

| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 1 | PHASE | Output | Phasing clock | |
| 2 | DTR | Bidirectional | Data terminal ready | Tied to DSR |
| 3 | TXD/ | Input | Receive data | Host transmit data |
| 4 | CTS | Input | Clear to send | Host ready bit |
| 5 | RXD/ | Output | Send data | Host receive data |
| 6 | RTS | Output | Request to send | PMAC ready bit |
| 7 | DSR | Bidirectional | Data set ready | Tied to DTR |
| 8 | SERVO | Output | Servo clock | |
| 9 | GND | Common | PMAC common | |
| 10 | +5V | Output | +5Vdc supply | Power supply output |

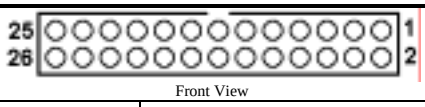
The JRS232 connector provides the PMAC2-PC with the ability to communicate serially with an RS232 port. E17 and E18 must connect pins 1 and 2 to use this connector. This connector cannot be used for daisy-chain interconnection of multiple PMACs – the J5A RS422 connector must be used for daisy-chaining.



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## J5A (JRS422) RS422 Serial Port Connector

### J5A JRS422 (26-Pin Connector)



Front View

| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 1 | CHASSI | Common | PMAC common | |
| 2 | S+5V | Output | +5Vdc supply | Deactivated by E8 |
| 3 | RD- | Input | Receive data | Diff. I/O low true * |
| 4 | RD+ | Input | Receive data | Diff. I/O high true * |
| 5 | SD- | Output | Send data | Diff. I/O low true * |
| 6 | SD+ | Output | Send data | Diff. I/O high true * |
| 7 | CS+ | Input | Clear to send | Diff. I/O high true * |
| 8 | CS- | Input | Clear to send | Diff. I/O low true * |
| 9 | RS+ | Output | Request to send | Diff. I/O high true * |
| 10 | RS- | Output | Request to send | Diff. I/O high true * |
| 11 | DTR | Bidirectional | Data terminal ready | Tied to DSR |
| 12 | INIT/ | Input | PMAC reset | Low is reset |
| 13 | GND | Common | PMAC common | * |
| 14 | DSR | Bidirectional | Data set ready | Tied to DTR |
| 15 | SDIO- | Bidirectional | Special data | Diff. I/O low true * |
| 16 | SDIO+ | Bidirectional | Special data | Diff. I/O high true * |
| 17 | SCIO- | Bidirectional | Special control | Diff. I/O low true * |
| 18 | SCIO+ | Bidirectional | Special control | Diff. I/O high true * |
| 19 | SCK- | Bidirectional | Special clock | Diff. I/O low true * |
| 20 | SCK+ | Bidirectional | Special clock | Diff. I/O high true * |
| 21 | SERVO- | Bidirectional | Servo clock | Diff. I/O low true * |
| 22 | SERVO+ | Bidirectional | Servo clock | Diff. I/O high true * |
| 23 | PHASE- | Bidirectional | Phase clock | Diff. I/O low true * |
| 24 | PHASE+ | Bidirectional | Phase clock | Diff. I/O high true * |
| 25 | GND | Common | PMAC common | |
| 26 | +5V | Output | +5Vdc supply | Power supply output |

* Used to share clocks for precise synchronization in multi-PMAC applications.

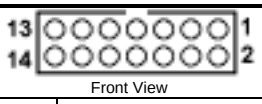
The JRS422 connector provides the PMAC with the ability to communicate in both RS422 and RS232. In addition, this connector is used to daisy-chain interconnect multiple PMACs for synchronized operation. E17 and E18 must connect pins 2 and 3 to use this connector for serial communications.



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## J6 (JDISP) Display Connector

### J6 JDISP (14-Pin Connector)

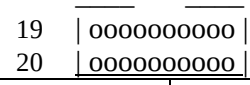



| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 1 | Vdd | Output | +5V Power | Power supply output |
| 2 | Vss | Common | PMAC common | |
| 3 | Rs | Output | Read strobe | TTL signal out |
| 4 | Vee | Output | Contrast adjust VEE | 0 to +5Vdc * |
| 5 | E | Output | Display enable | High is enable |
| 6 | R/W | Output | Read or write | TTL signal out |
| 7 | DB1 | Output | Display data 1 | |
| 8 | DB0 | Output | Display data 0 | |
| 9 | DB3 | Output | Display data 3 | |
| 10 | DB2 | Output | Display data 2 | |
| 11 | DB5 | Output | Display data 5 | |
| 12 | DB4 | Output | Display data 4 | |
| 13 | DB7 | Output | Display data 7 | |
| 14 | DB6 | Output | Display data 6 | |

The JDISP connector is used to drive the 2 line x 24 character (Acc-12), 2 x 40 (Acc-12A) LCD, or the 2 x 40 vacuum fluorescent (Acc 12C) display unit. The **`DISPLAY`** command may be used to send messages and values to the display.

## J7 (JHW) Handwheel Encoder Connector

### J7 JHW (20-Pin Connector)




| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 1 | GND | Common | Reference voltage | |
| 2 | +5V | Output | Supply voltage | To power external circuitry |
| 3 | HWA1+ | Input | HW positive A channel | Also pulse input |
| 4 | HWA1- | Input | HW negative A channel | Also pulse input |
| 5 | HWB1+ | Input | HW positive B channel | Also direction input |
| 6 | HWB1- | Input | HW negative B channel. | Also direction input |
| 7 | HWA2+ | Input | HW positive A channel | Also pulse input |
| 8 | HWA2- | Input | HW negative A channel | Also pulse input |
| 9 | HWB2+ | Input | HW positive B channel | Also direction input |
| 10 | HWB2- | Input | HW negative B channel. | Also direction input |
| 11 | PUL1+ | Output | PFM positive pulse | Also PWM output |
| 12 | PUL1- | Output | PFM negative pulse | Also PWM output |
| 13 | DIR1+ | Output | PFM positive direct out | Also PWM output |
| 14 | DIR1- | Output | PFM negative direct out | Also PWM output |
| 15 | PUL2+ | Output | PFM positive pulse | Also PWM output |
| 16 | PUL2- | Output | PFM negative pulse | Also PWM output |
| 17 | DIR2+ | Output | PFM positive direct out | Also PWM output |
| 18 | DIR2- | Output | PFM negative direct out | Also PWM output |
| 19 | GND | Common | Reference voltage | |
| 20 | +5V | Output | Supply voltage | To power external circuitry |



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# J8 (JEQU) Position Compare Output Connector

## J8 JEQU (10-Pin Connector)



Front View

| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 1 | EQU1/ | Output | Encoder 1 COMP-EQ | Low is true |
| 2 | EQU2/ | Output | Encoder 2 COMP-EQ | Low is true |
| 3 | EQU3/ | Output | Encoder 3 COMP-EQ | Low is true |
| 4 | EQU4/ | Output | Encoder 4 COMP-EQ | Low is true |
| 5 | AENA1/ | Output | Amp Enable 1 | Low is true |
| 6 | AENA2/ | Output | Amp Enable 2 | Low is true |
| 7 | AENA3/ | Output | Amp Enable 3 | Low is true |
| 8 | AENA4/ | Output | Amp Enable 4 | Low is true |
| 9 | +V | Supply | Positive supply | +5V to +24V |
| 10 | GND | Common | Digital ground | |

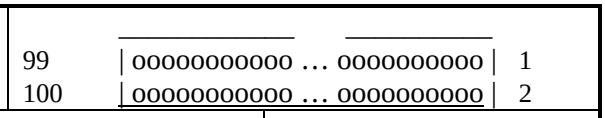
This connector provides the position-compare outputs and the amplifier enable outputs for the four servo interface channels. The board is shipped by default with a ULN2803A or equivalent open-collector driver IC. It may be replaced with UDN2891A or equivalent open-emitter driver (E11 and E12 must be changed), or a 74ACT563 or equivalent 5V CMOS driver.



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## J9 (JMACH1) Servo Channel 1 & 2 Connector

### J9 JMACH1 (100-Pin Connector)

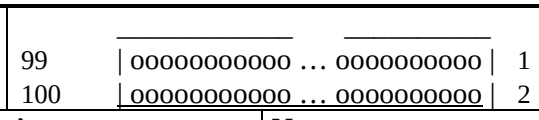



| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 1 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| 2 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| 3 | GND | Common | Reference voltage | |
| 4 | GND | Common | Reference voltage | |
| 5 | CHA1+ | Input | Encoder 1 positive A channel | Also pulse input |
| 6 | CHA1- | Input | Encoder 1 negative A channel | Also pulse input |
| 7 | CHB1+ | Input | Encoder 1 positive B channel | Also direction input |
| 8 | CHB1- | Input | Encoder 1 negative B channel | Also direction input |
| 9 | CHC1+ | Input | Encoder 1 positive C channel | Index channel |
| 10 | CHC1- | Input | Encoder 1 negative C channel | Index channel |
| 11 | CHU1 | Input | Channel 1 U flag | Hall effect, fault code, or sub-count |
| 12 | CHV1 | Input | Channel 1 V flag | Hall effect, fault code, or sub-count |
| 13 | CHW1 | Input | Channel 1 W flag | Hall effect, fault code, or sub-count |
| 14 | CHT1 | Input | Channel 1 T flag | Fault code, or sub-count |
| 15 | USER1 | Input | General purpose user flag | Hardware capture flag, or sub-count |
| 16 | PLIM1 | Input | Positive overtravel limit | Hardware capture flag |
| 17 | MLIM1 | Input | Negative overtravel limit | Hardware capture flag |
| 18 | HOME1 | Input | Home switch input | Hardware capture flag |
| 19 | ACCFLT1 | Input | Accessory fault flag | For loss of ACC supply voltage |
| 20 | WD0/ | Output | Watchdog output | Low is PMAC watchdog fault |
| 21 | SCLK12+ | Input/Output | Encoder sample clock | Direction controlled by PMAC2 jumper |
| 22 | SCLK12- | Input/Output | Encoder sample clock | Direction controlled by PMAC2 jumper |
| 23 | ADC_CLK1+ | Output | A/D converter clock | Programmable frequency |
| 24 | ADC_CLK1- | Output | A/D converter clock | Programmable frequency |
| 25 | ADC_STB1+ | Output | A/D converter strobe | Programmable sequence |
| 26 | ADC_STB1- | Output | A/D converter strobe | Programmable sequence |
| 27 | ADC_DAA1+ | Input | Channel A ADC serial data | MSB first |
| 28 | ADC_DAA1- | Input | Channel A ADC serial data | MSB first |
| 29 | ADC_DAB1+ | Input | Channel B ADC serial data | MSB first |
| 30 | ADC_DAB1- | Input | Channel B ADC serial data | MSB first |
| 31 | AENA1+ | Output | Amplifier enable | High is enable |
| 32 | AENA1- | Output | Amplifier enable | Low is enable |
| 33 | FAULT1+ | Input | Amplifier fault | Programmable polarity |
| 34 | FAULT1- | Input | Amplifier fault | Programmable polarity |
| 35 | PWMATOP1+ DAC_CLK1+ | Output | Phase A top Cmd. or DAC clock | Programmable function control |
| 36 | PWMATOP1- DAC_CLK1- | Output | Phase A top Cmd. or DAC clock | Programmable function control |



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## J9 JMACH1 (100-Pin Connector) (Continued)

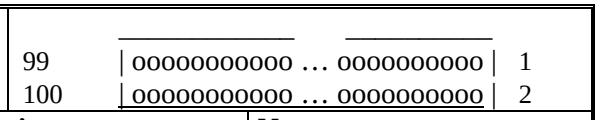



| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 37 | PWMABOT1+ DAC1A+ | Output | Phase A bottom Cmd. or DAC A serial data | Programmable function control |
| 38 | PWMABOT1- DAC1A- | Output | Phase A bottom Cmd. or DAC A serial data | Programmable function control |
| 39 | PWMBTOP1+ DAC_STB1+ | Output | Phase B top Cmd. or DAC strobe | Programmable function control |
| 40 | PWMBTOP1- DAC_STB1- | Output | Phase B top Cmd. or DAC strobe | Programmable function control |
| 41 | PWMBBOT1+ DAC1B+ | Output | Phase B bottom Cmd. or DAC B serial data | Programmable function control |
| 42 | PWMBBOT1- DAC1B- | Output | Phase B bottom Cmd. or DAC B serial data | Programmable function control |
| 43 | PWMCTOP1+ DIR1+ | Output | Phase B top Cmd. or PFM direction | Programmable function control |
| 44 | PWMCTOP1- DIR1- | Output | Phase B top Cmd. or PFM direction | Programmable function control |
| 45 | PWMCBOT1+ PULSE1+ | Output | Phase B bottom Cmd. or PFM pulse | Programmable function control |
| 46 | PWMCBOT1- PULSE1- | Output | Phase B bottom Cmd. or PFM pulse | Programmable function control |
| 47 | GND | Common | Reference voltage | |
| 48 | GND | Common | Reference voltage | |
| 49 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| 50 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| 51 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| 52 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| 53 | GND | Common | Reference voltage | |
| 54 | GND | Common | Reference voltage | |
| 55 | CHA2+ | Input | Encoder 2 positive A channel | Also pulse input |
| 56 | CHA2- | Input | Encoder 2 negative A channel. | Also pulse input |
| 57 | CHB2+ | Input | Encoder 2 positive B channel | Also direction input |
| 58 | CHB2- | Input | Encoder 2 negative B channel | Also direction input |
| 59 | CHC2+ | Input | Encoder 2 positive C channel | Index Channel |
| 60 | CHC2- | Input | Encoder 2 negative C channel | Index Channel |
| 61 | CHU2 | Input | Channel 2 U flag | Hall effect, fault code, or sub-count |
| 62 | CHV2 | Input | Channel 2 V flag | Hall effect, fault code, or sub-count |
| 63 | CHW2 | Input | Channel 2 W flag | Hall effect, fault code, or sub-count |
| 64 | CHT2 | Input | Channel 2 T flag | Fault code, or sub-count |
| 65 | USER2 | Input | General purpose user flag | Hardware capture flag, or sub-count |
| 66 | PLIM2 | Input | Positive overtravel limit | Hardware capture flag |
| 67 | MLIM2 | Input | Negative overtravel limit | Hardware capture flag |
| 68 | HOME2 | Input | Home switch input | Hardware capture flag |



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## J9 JMACH1 (100-Pin Connector) (Continued)

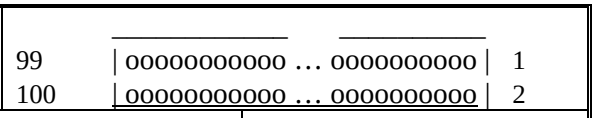



| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 69 | ACCFLT2 | Input | Accessory fault flag | For loss of ACC supply voltage |
| 70 | WD0/ | Output | Watchdog output | Low is PMAC watchdog fault |
| 71 | SCLK12+ | Input/Output | Encoder sample clock | Direction controlled by PMAC2 jumper |
| 72 | SCLK12- | Input/Output | Encoder sample clock | Direction controlled by PMAC2 jumper |
| 73 | ADC_CLK2+ | Output | A/D converter clock | Programmable frequency |
| 74 | ADC_CLK2- | Output | A/D converter clock | Programmable frequency |
| 75 | ADC_STB2+ | Output | A/D converter strobe | Programmable sequence |
| 76 | ADC_STB2- | Output | A/D converter strobe | Programmable sequence |
| 77 | ADC_DAA2+ | Input | Channel A ADC serial data | MSB first |
| 78 | ADC_DAA2- | Input | Channel A ADC serial data | MSB first |
| 79 | ADC_DAB2+ | Input | Channel B ADC serial data | MSB first |
| 80 | ADC_DAB2- | Input | Channel B ADC serial data | MSB first |
| 81 | AENA2+ | Output | Amplifier enable | High is enable |
| 82 | AENA2- | Output | Amplifier enable | Low is enable |
| 83 | FAULT2+ | Input | Amplifier fault | Programmable polarity |
| 84 | FAULT2- | Input | Amplifier fault | Programmable polarity |
| 85 | PWMATOP2+ DAC_CLK2+ | Output | Phase A top Cmd. or DAC clock | Programmable function control |
| 86 | PWMATOP2- DAC_CLK2- | Output | Phase A top Cmd. or DAC clock | Programmable function control |
| 87 | PWMABOT2+ DAC2A+ | Output | Phase A bottom Cmd. or DAC A serial data | Programmable function control |
| 88 | PWMABOT2- DAC2A- | Output | Phase A bottom Cmd. or DAC A serial data | Programmable function control |
| 89 | PWMBTOP2+ DAC_STB2+ | Output | Phase B top Cmd. or DAC strobe | Programmable function control |
| 90 | PWMBTOP2- DAC_STB2- | Output | Phase B top Cmd. or DAC strobe | Programmable function control |
| 91 | PWMBBOT2+ DAC2B+ | Output | Phase B bottom Cmd. or DAC B serial data | Programmable function control |
| 92 | PWMBBOT2- DAC2B- | Output | Phase B bottom Cmd. or DAC B serial data | Programmable function control |
| 93 | PWMCTOP2+ DIR2+ | Output | Phase C bottom Cmd. or DAC C serial data | Programmable function control |
| 94 | PWMCTOP2- DIR2- | Output | Phase C top Cmd. or PFM direction | Programmable function control |
| 95 | PWMCBOT2+ PULSE2+ | Output | Phase C bottom Cmd. or PFM pulse | Programmable function control |
| 96 | PWMCBOT2- PULSE2- | Output | Phase C bottom Cmd. or PFM pulse | Programmable function control |
| 97 | GND | Common | Reference voltage | |



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## J9 JMACH1 (100-Pin Connector) (Continued)




| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 98 | GND | Common | Reference voltage | |
| 99 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| 100 | +5V | Output/Input | +5V power | For external circuit or from external supply |

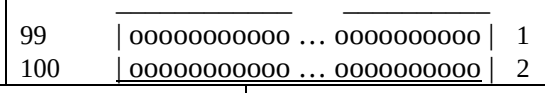
The JMACH1 connector provides the interface pins for channels 1 and 2. Usually, it is connected to a breakout board, such as one of the ACC-8x family of boards, or an application-specific interface board.
Connector: 100-pin male box header with center key, 0.050" pitch. AMP part # 1-04068-7
Delta Tau part # 014-00100-FPB.



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## J10 (JMACH2) Servo Channel 3 & 4 Connector

**J10 JMACH2 (100-Pin Connector)**

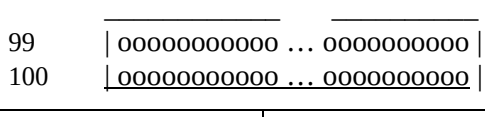



| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 1 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| 2 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| 3 | GND | Common | Reference voltage | |
| 4 | GND | Common | Reference voltage | |
| 5 | CHA3+ | Input | Encoder 3 positive A channel | Also pulse input |
| 6 | CHA3- | Input | Encoder 3 negative A channel | Also pulse input |
| 7 | CHB3+ | Input | Encoder 3 positive B channel | Also direction input |
| 8 | CHB3- | Input | Encoder 3 negative B channel | Also direction input |
| 9 | CHC3+ | Input | Encoder 3 positive C channel | Index channel |
| 10 | CHC3- | Input | Encoder 3 negative C channel | Index channel |
| 11 | CHU3 | Input | Channel 3 U flag | Hall effect, fault code, or sub-count |
| 12 | CHV3 | Input | Channel 3 V flag | Hall effect, fault code, or sub-count |
| 13 | CHW3 | Input | Channel 3 W flag | Hall effect, fault code, or sub-count |
| 14 | CHT3 | Input | Channel 3 T flag | Fault code, or sub-count |
| 15 | USER3 | Input | General purpose user flag | Hardware capture flag, or sub-count |
| 16 | PLIM3 | Input | Positive overtravel limit | Hardware capture flag |
| 17 | MLIM3 | Input | Negative overtravel limit | Hardware capture flag |
| 18 | HOME3 | Input | Home switch input | Hardware capture flag |
| 19 | ACCFLT3 | Input | Accessory fault flag | For loss of ACC supply voltage |
| 20 | WD0/ | Output | Watchdog output | Low is PMAC watchdog fault |
| 21 | SCLK34+ | Input/Output | Encoder sample clock | Direction controlled by PMAC2 jumper |
| 22 | SCLK34- | Input/Output | Encoder sample clock | Direction controlled by PMAC2 jumper |
| 23 | ADC_CLK3+ | Output | A/D converter clock | Programmable frequency |
| 24 | ADC_CLK3- | Output | A/D converter clock | Programmable frequency |
| 25 | ADC_STB3+ | Output | A/D converter strobe | Programmable sequence |
| 26 | ADC_STB3- | Output | A/D converter strobe | Programmable sequence |
| 27 | ADC_DAA3+ | Input | Channel A ADC serial data | MSB first |
| 28 | ADC_DAA3- | Input | Channel A ADC serial data | MSB first |
| 29 | ADC_DAB3+ | Input | Channel B ADC serial data | MSB first |
| 30 | ADC_DAB3- | Input | Channel B ADC serial data | MSB first |
| 31 | AENA3+ | Output | Amplifier enable | High is enable |
| 32 | AENA3- | Output | Amplifier enable | Low is enable |
| 33 | FAULT3+ | Input | Amplifier fault | Programmable polarity |
| 34 | FAULT3- | Input | Amplifier fault | Programmable polarity |
| 35 | PWMATOP3+ DAC_CLK3+ | Output | Phase A top Cmd. or DAC clock | Programmable function control |



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## J10-JMACH2 (100-Pin Connector) (Continued)

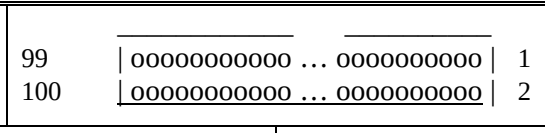



| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 36 | PWMATOP3-<br>DAC_CLK3- | Output | Phase A top Cmd. or DAC clock | Programmable function control |
| 37 | PWMABOT3+<br>DAC3A+ | Output | Phase A bottom Cmd. or DAC A serial data | Programmable function control |
| 38 | PWMABOT3-<br>DAC3A- | Output | Phase A bottom Cmd. or DAC A serial data | Programmable function control |
| 39 | PWMBTOP3+<br>DAC_STB3+ | Output | Phase B top Cmd. or DAC strobe | Programmable function control |
| 40 | PWMBTOP3-<br>DAC_STB3- | Output | Phase B top Cmd. or DAC strobe | Programmable function control |
| 41 | PWMBBOT3+<br>DAC3B+ | Output | Phase B bottom Cmd. or DAC B serial data | Programmable function control |
| 42 | PWMBBOT3-<br>DAC3B- | Output | Phase B bottom Cmd. or DAC B serial data | Programmable function control |
| 43 | PWMCTOP3+<br>DIR3+ | Output | Phase C top Cmd. or PFM direction | Programmable function control |
| 44 | PWMCTOP3-<br>DIR3- | Output | Phase C top Cmd. or PFM direction | Programmable function control |
| 45 | PWMCBOT3+<br>PULSE3+ | Output | Phase C bottom Cmd. or PFM pulse | Programmable function control |
| 46 | PWMCBOT3-<br>PULSE3- | Output | Phase C bottom Cmd. or PFM pulse | Programmable function control |
| 47 | GND | Common | Reference voltage | |
| 48 | GND | Common | Reference voltage | |
| 49 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| 50 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| 51 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| 52 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| 53 | GND | Common | Reference voltage | |
| 54 | GND | Common | Reference voltage | |
| 55 | CHA4+ | Input | Encoder 4 positive A channel | Also pulse input |
| 56 | CHA4- | Input | Encoder 4 negative A channel | Also pulse input |
| 57 | CHB4+ | Input | Encoder 4 positive B channel | Also direction input |
| 58 | CHB4- | Input | Encoder 4 negative B channel | Also direction input |
| 59 | CHC4+ | Input | Encoder 4 positive C channel | Index channel |
| 60 | CHC4- | Input | Encoder 4 negative C channel | Index channel |
| 61 | CHU4 | Input | Channel 4 U flag | Hall effect, fault code, or sub-count |



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## J10 JMACH2 (100-Pin Connector) (Continued)




| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 62 | CHV4 | Input | Channel 4 V flag | Hall effect, fault code, or sub-count |
| 63 | CHW4 | Input | Channel 4 W flag | Hall effect, fault code, or sub-count |
| 64 | CHT4 | Input | Channel 4 T flag | Fault code, or sub-count |
| 65 | USER4 | Input | General purpose user flag | Hardware capture flag, or sub-count |
| 66 | PLIM4 | Input | Positive overtravel limit | Hardware capture flag |
| 67 | MLIM4 | Input | Negative overtravel limit | Hardware capture flag |
| 68 | HOME4 | Input | Home switch input | Hardware capture flag |
| 69 | ACCFLT4 | Input | Accessory fault flag | For loss of ACC supply voltage |
| 70 | WD0/ | Output | Watchdog output | Low is PMAC watchdog fault |
| 71 | SCLK34+ | Input/Output | Encoder sample clock | Direction controlled by PMAC2 jumper |
| 72 | SCLK34- | Input/Output | Encoder sample clock | Direction controlled by PMAC2 jumper |
| 73 | ADC_CLK4+ | Output | A/D converter clock | Programmable frequency |
| 74 | ADC_CLK4- | Output | A/D converter clock | Programmable frequency |
| 75 | ADC_STB4+ | Output | A/D converter strobe | Programmable sequence |
| 76 | ADC_STB4- | Output | A/D converter strobe | Programmable sequence |
| 77 | ADC_DAA4+ | Input | Channel A ADC serial data | MSB first |
| 78 | ADC_DAA4- | Input | Channel A ADC serial data | MSB first |
| 79 | ADC_DAB4+ | Input | Channel B ADC serial data | MSB first |
| 80 | ADC_DAB4- | Input | Channel B ADC serial data | MSB first |
| 81 | AENA4+ | Output | Amplifier enable | High is enable |
| 82 | AENA4- | Output | Amplifier enable | Low is enable |
| 83 | FAULT4+ | Input | Amplifier fault | Programmable polarity |
| 84 | FAULT4- | Input | Amplifier fault | Programmable polarity |
| 85 | PWMATOP4+ DAC_CLK4+ | Output | Phase A top Cmd. or DAC clock | Programmable function control |
| 86 | PWMATOP4- DAC_CLK4- | Output | Phase A top Cmd. or DAC clock | Programmable function control |
| 87 | PWMABOT4+ DAC4A+ | Output | Phase A bottom Cmd. or DAC A serial data | Programmable function control |
| 88 | PWMABOT4- DAC4A- | Output | Phase A bottom Cmd. or DAC A serial data | Programmable function control |
| 89 | PWMBTOP4+ DAC_STB4+ | Output | Phase B top Cmd. or DAC strobe | Programmable function control |
| 90 | PWMBTOP4- DAC_STB4- | Output | Phase B top Cmd. or DAC strobe | Programmable function control |
| 91 | PWMBBOT4+ DAC4B+ | Output | Phase P bottom Cmd. or DAC B serial data | Programmable function control |
| 92 | PWMBBOT4- DAC4B- | Output | Phase P bottom Cmd. or DAC B serial data | Programmable function control |
| 93 | PWMCTOP4+ DIR4+ | Output | Phase C top Cmd. or PFM direction | Programmable function control |



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| **J10 JMACH2 (100-Pin Connector) (Continued)** | | | | |
|---|---|---|---|---|
| | | | 99 \| oooooooooo … oooooooooo \| 1<br>100 \| oooooooooo … oooooooooo \| 2 | |
| **Pin #** | **Symbol** | **Function** | **Description** | **Notes** |
| 94 | PWMCTOP4-<br>DIR4- | Output | Phase C top Cmd. or PFM direction | Programmable function control |
| 95 | PWMCBOT4+<br>PULSE4+ | Output | Phase C bottom Cmd. or PFM pulse | Programmable function control |
| 96 | PWMCBOT4-<br>PULSE4- | Output | Phase C bottom Cmd. or PFM pulse | Programmable function control |
| 97 | GND | Common | Reference voltage | |
| 98 | GND | Common | Reference voltage | |
| 99 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| 100 | +5V | Output/Input | +5V power | For external circuit or from external supply |
| The JMACH2 connector provides the interface pins for channels 3 and 4. Usually, it is connected to a breakout board, such as one of the ACC-8x family of boards, or an application-specific interface board.<br>Connector: 100-pin male box header with center key, 0.050" pitch. AMP part # 1-04068-7<br>Delta Tau part # 014-00100-FPB. | | | | |

## TB1 (2/4-Pin Terminal Block)

This terminal block can be used to provide the input for the power supply for the circuits on the PMAC2 board when it is not in a bus configuration. When the PMAC2 is in a bus configuration, these supplies come through the bus connector from the bus power supply automatically; in this case, this terminal block should not be used.

| **Pin #** | **Symbol** | **Function** | **Description** | **Notes** |
|---|---|---|---|---|
| 1 | GND | Common | Reference voltage | |
| 2 | +5V | Input | Positive supply voltage | Supplies all PMAC digital circuits |
| 3 | +12V | Input | Positive supply voltage | +12V to +15V; not required on-board; used on J1 to supply analog inputs |
| 4 | -12V | Input | Negative supply voltage | -12V to -15V; required for Opt-12 ADCs; used on J1 to supply analog inputs |
| **Note:** Unless Option 12 (Analog-to-Digital Converters) is included on the board, only pins 1 and 2 will be provided on this terminal block. | | | | |



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## TB2 (4-Pin Terminal Block)

This terminal block provides the output for PMAC2's watchdog timer relay, both normally open and normally closed contacts.

| Pin # | Symbol | Function | Description | Notes |
|---|---|---|---|---|
| 1 | WD_NC | Output | Watchdog relay out | Normally closed |
| 2 | COM | Input | Watchdog return | +V or 0V |
| 3 | WD_NO | Output | Watchdog relay out | Normally open |
| 4 | COM | Input | Watchdog return | +V or 0V |
| **Note:** The normally closed relay contact is open while PMAC2 is operating properly — it has power and the watchdog timer is not tripped — and closed when the PMAC2 is not operating properly — either it has lost power or the watchdog timer has tripped. The normally open relay contact is closed while PMAC2 is operating properly and open when PMAC2 is not operating properly. | | | | |



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