HARDWARE REFERENCE MANUAL

PMAC PC

Programmable Multi-Axis Controller

3Ax-602191-xHxx

May 26, 2004

DELTA TAU
Data Systems, Inc.
NEW IDEAS IN MOTION ...

Single Source Machine Control *Power // Flexibility // Ease of Use*
21314 Lassen Street Chatsworth, CA 91311 // Tel. (818) 998-2095 Fax. (818) 998-7807 // www.deltatau.com

Copyright Information

To report errors or inconsistencies, call or email:

Delta Tau Data Systems, Inc. Technical Support
Phone: (818) 717-5656
Fax: (818) 998-7807
Email: support@deltatau.com
Website: http://www.deltatau.com

Operating Conditions

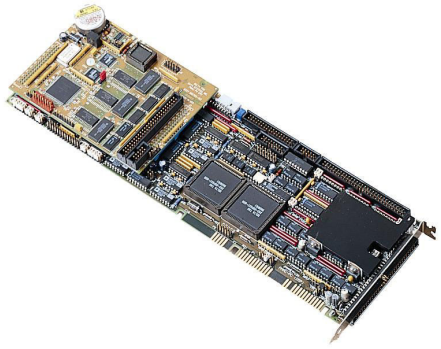
All Delta Tau Data Systems, Inc. motion controller products, accessories, and amplifiers contain static sensitive components that can be damaged by incorrect handling. When installing or handling Delta Tau Data Systems, Inc. products, avoid contact with highly insulated materials. Only qualified personnel should be allowed to handle this equipment.

In the case of industrial applications, we expect our products to be protected from hazardous or conductive materials and/or environments that could cause harm to the controller by damaging components or causing electrical shorts. When our products are used in an industrial environment, install them into an industrial electrical cabinet or industrial PC to protect them from excessive or corrosive moisture, abnormal ambient temperatures, and conductive materials. If Delta Tau Data Systems, Inc. products are exposed to hazardous or conductive materials and/or environments, we cannot guarantee their operation.

Table of Contents

INTRODUCTION

The PMAC PC is a member of the PMAC family of boards optimized for interface to traditional Servo drives with single analog inputs representing velocity or torque commands. Its software is capable of eight axes of control. It can have up to four or eight channels of on-board axis interface circuitry.



The PMAC PC is a full-sized ISA-bus expansion card, with a small piggyback board containing the CPU board. This piggyback board occupies part of the next slot, but ½-sized boards (such as the Option 2 Dual-Ported RAM board) are permitted in this next slot. While the PMAC PC is capable of ISA bus communications, with or without the optional dual-ported RAM, it does not need to be inserted into an ISA expansion slot. Communications can be done through an RS-232 or RS-422 serial port. Standalone operation is also possible.

Board Configuration

Base Version

The base version of the PMAC PC provides a 1-1/2 slot board with:

- 20 MHz DSP56002 CPU
- 128k x 24 Static one wait-state battery-backed RAM
- 128k x 8 PROM memory for firmware storage
- 2k x 8 EEPROM memory for setup variable backup
- Latest released firmware version
- RS-422 serial interface, ISA (PC) bus interface
- Four channels axis interface circuitry, each including:
  - 16-bit +/-10V analog output
  - 3-channel differential/single-ended encoder input
  - Four input flags, two output flags
- Interface to external 16-bit serial ADC
  - Display, control panel, muxed I/O, direct I/O interface ports
  - Buffered expansion port
  - Clock crystal with +/-100 ppm accuracy
- PID/notch/feedforward servo algorithms
- 1-year warranty from date of shipment
- One Manuals CD per set of one to four PMACs in shipment
  (Cables, mounting plates, mating connectors not included)

Option 1: Additional Four Channels Axis Interface Circuitry

Option 1 provides an additional four channels of on-board axis interface circuitry, identical to the standard first four channels.

Option 2: Dual-Ported RAM

Dual-ported RAM provides a very high-speed communications path for bus communications with the host computer through a bank of shared memory. If more than about 100 data items per second are to be passed between the controller and the host computer in either direction, DPRAM should be used.

- Option 2 provides an 8k x 16 bank of dual-ported RAM on a separate half-slot board.

- Option A provides a 20-cm (8") 50-pin 3-connector cable. This cable is necessary when using the Option 2 board combined with any of the Acc-14D, 24P, 29P, or 36P boards.

Option 4A and Option 5x: CPU Type

The base PMAC version without options has a 20 MHz CPU with one wait-state battery-backed RAM. The CPU memory option is flash type with zero-wait state, allowing faster access from the CPU, and therefore, provides a significant increase in speed. However, any change in a flash type memory must be saved in PMAC so that it can be retained on a power-up\reset cycle. Therefore, if machine parameters like parts counters or state variables are required, the Option 16 battery-backed parameter RAM is suggested as a complement to the faster CPU options.

- Option 4A: 20 MHz CPU, zero-wait RAM, flash backup, no battery, (~25% speed increase)
- Option 5A: 40 MHz CPU, zero-wait RAM, flash backup, no battery, (~125% speed increase)
- Option 5B: 60 MHz CPU, zero-wait RAM, flash backup, no battery, (~250% speed increase)
- Option 5C: 80 MHz CPU, zero-wait RAM, flash backup, no battery, (~375% speed increase)

Option 6: Extended Firmware Algorithm

- Option 6 provides an Extended (Pole-Placement) Servo Algorithm firmware. This is required only in difficult-to-control systems (resonances, backlash, friction, disturbances, changing dynamics). This option requires a one-time purchase of the Acc-25 program, which is necessary for tuning the Option 6 firmware.

Option 7: Plate Mounting

- Option 7 provides a mounting plate connected to the PMAC with standoffs. It is used to install the PMAC in standalone applications.

Option 8A: High-Accuracy Clock Crystal

The PMAC PC has a clock crystal of nominal frequency 19.6608 MHz (~20 MHz). The standard crystal's accuracy specification is +/-100 ppm.

- Option 8A provides a nominal 19.6608 MHz crystal with a +/-15 ppm accuracy specification.

Option 10: Firmware Version Specification

Normally, the PMAC PC is provided with the latest firmware version. A label on the memory IC shows the firmware version loaded at the factory.

- Option 10 provides for a user-specified firmware version.

Option 14: Replacement of Flag OPTO-Isolators with Socketed Shunts

Normally, the flag inputs on all servo channels have OPTO-isolator circuits that require 12 to 24V inputs to turn on. When the Acc-8D Option 8 Analog Encoder Interpolator is used on a pair of channels, it uses the flag inputs on the second (even-numbered) channel to provide sub-count information at 5V levels referenced to digital ground.

- Option 14 provides for the replacement of the OPTO-isolators on the even-numbered channels of PMAC PC with socketed shunts that permit the input of 5V non-isolated signals from the Acc-8D Option 8 boards.

Option 15: V-to-F Converter for Analog Input

The JPAN control panel port on the PMAC PC has an optional analog input called Wiper (because it is often tied to a potentiometer's wiper pin). PMAC PC can digitize this signal by passing it through an optional voltage-to-frequency converter, using E-point jumpers to feed this into the Encoder 4 circuitry (no other use is then permitted). It then executes frequency calculations using the time base feature of the encoder conversion table.

- Option 15 provides a voltage-to-frequency converter that permits the use of the Wiper input on the control panel port.

Option 16: Battery-Backed Parameter Memory

The contents of the standard memory are not retained through a power-down or reset unless they have been saved to flash memory first. Option 16 provides supplemental battery-backed RAM for real-time parameter storage that is ideal for holding machine-state parameters in case of an unexpected power-down.

- Option 16A provides a 16k x 24 bank of battery-backed parameter RAM. This Option requires Option 4A, Option 5A, Option 5B or Option 5C.

PMAC Connectors and Indicators

J1 - Display Port Outputs (JDISP Port)

The JDISP connector allows connection of the Acc-12 or Acc-12A liquid crystal displays, or of the Acc-12C vacuum fluorescent display. Both text and variable values may be shown on these displays through the use of the **DISPLAY** command, executing in either motion or PLC programs.

J2 - Control-Panel Port I/O (JPAN Port)

The JPAN connector is a 26-pin connector with dedicated control inputs, dedicated indicator outputs, a quadrature encoder input, and an analog input (requires PMAC Option 15). The control inputs are low true with internal pull-up resistors. They have predefined functions unless the control-panel-disable I-variable (I2) has been set to 1. If this is the case, they may be used as general-purpose inputs by assigning M-variable to their corresponding memory-map locations (bits of Y address $FFC0).

J3 - Thumbwheel Multiplexer Port I/O (JTHW Port)

The Thumbwheel Multiplexer Port, or Multiplexer Port, on the JTHW connector has eight input lines and eight output lines. The output lines can be used to multiplex large numbers of inputs and outputs on the port, and Delta Tau provides accessory boards and software structures (special M-variable definitions) to capitalize on this feature. Up to 32 of the multiplexed I/O boards may be daisy-chained on the port, in any combination.

J4 - Serial Port Connection

For serial communications, use a serial cable to connect the PC's COM port to the PMAC's serial port connector. Delta Tau provides the Acc-3D cable for this purpose, which connects PMAC to a DB-25 connector. Standard DB-9-to-DB-25 or DB-25-to-DB-9 adapters may be needed for a particular setup.

J5 - General-Purpose Digital Inputs and Outputs (JOPTO Port)

PMAC's JOPTO connector provides eight general-purpose digital inputs and eight general-purpose digital outputs. Each input and output has its own corresponding ground pin in the opposite row. The 34-pin connector was designed for easy interface to OPTO-22 or equivalent optically isolated I/O modules. Delta Tau's Acc-21F is a six-foot cable for this purpose.

Machine Connectors

The primary machine interface connector is JMACH1, labeled J8 on the PMAC PC. It contains the pins for four channels of machine I/O: analog outputs, incremental encoder inputs, and associated input and output flags, plus power-supply connections.

The next machine interface connector is JMACH2, labeled J7 on the PMAC PC. It is essentially identical to the JMACH1 connector for one to four more axes. It is present only if the PMAC card has been fully populated to handle eight axes (Option 1) because it interfaces the optional extra components.

LED Indicators

PMACs with the Option CPU have three LED indicators: red, yellow, and green. The red and green LEDs have the same meaning as with the standard CPU: when the green LED is lit, this indicates that power is applied to the +5V input; when the red LED is lit, this indicates that the Watchdog timer has tripped and shut down the PMAC.

The yellow LED (located beside the red and green LEDs), when lit, indicates that the phase-locked loop that multiplies the CPU clock frequency from the crystal frequency on the Option CPU is operational and stable. This indicator is for diagnostic purposes only. It may not be present on all boards.

PMAC System Configuration Incompatibilities

In general, PMAC, its options, and its accessories can be mixed and matched at will. However, there are some combinations that are not permissible. These combinations are listed below.

JEXP Expansion Port Accessories

Acc-24P/V and Acc-29P/V may not be used on the same PMAC due to addressing conflicts. To interface with MLDT feedback devices, the PMAC2 controller is recommended instead of the PMAC and Acc-29P/V combination. The PMAC can interface with 2 off-board DSPGATEs. The Acc-24P/V can have only one DSPGATE or a second DSPGATE when Acc-24P/V Option 1 is ordered. The Acc-51P can only have one DSPGATE.

Due to bus drive limitations, a limit of four with an absolute maximum of six expansion port (JEXP) accessories is recommended on any PMAC. In addition, the address spaces for Acc-14D/V and Acc-36P/V boards on the JEXP expansion port are limited to six. One Acc-14D/V occupies a full address space; four Acc-36P/V boards occupy one address space.

JTHW Thumbwheel Multiplexer Port Accessories

A total of 32 boards can be plugged into the thumbwheel multiplexer port (JTHW) through daisy chaining.

The Acc-27 OPTO-Isolated I/O board cannot be used with any other accessory that connects through the thumbwheel multiplexer port (JTHW); the Acc-8D Opt 7 R/D converter (if absolute power-on position is desired); the Acc-8D Opt 9 Yaskawa Encoder Interface, the Acc-18 thumbwheel board, or any of the Acc-34 family of serial I/O boards. This is because the Acc-27 uses the port in non-multiplexed fashion.

There is a limit of 256 addresses for multiplexed accessories on the JTHW thumbwheel multiplexer port: the Acc-8D Opt 7 R/D converter (if absolute power-on position is desired), the Acc-8D Opt 9 Yaskawa Encoder Interface, the Acc-18 thumbwheel board, or any of the Acc-34 family of serial I/O boards.

- An Acc-8D Opt 7 board occupies one address.
- An Acc-8D Opt 9 board occupies one address.
- An Acc-18 board occupies eight consecutive addresses, starting with an address divisible by eight.
- An Acc-34 type board occupies eight consecutive addresses, starting with an address divisible by eight.

JPAN Control Panel Port Accessories

The Acc-16D control panel and the Acc-39 handwheel encoder converter cannot be used on the same PMAC because both use the entire JPAN control panel port. This port is not present on the Mini-PMAC board.

JDISP Display Port Accessories

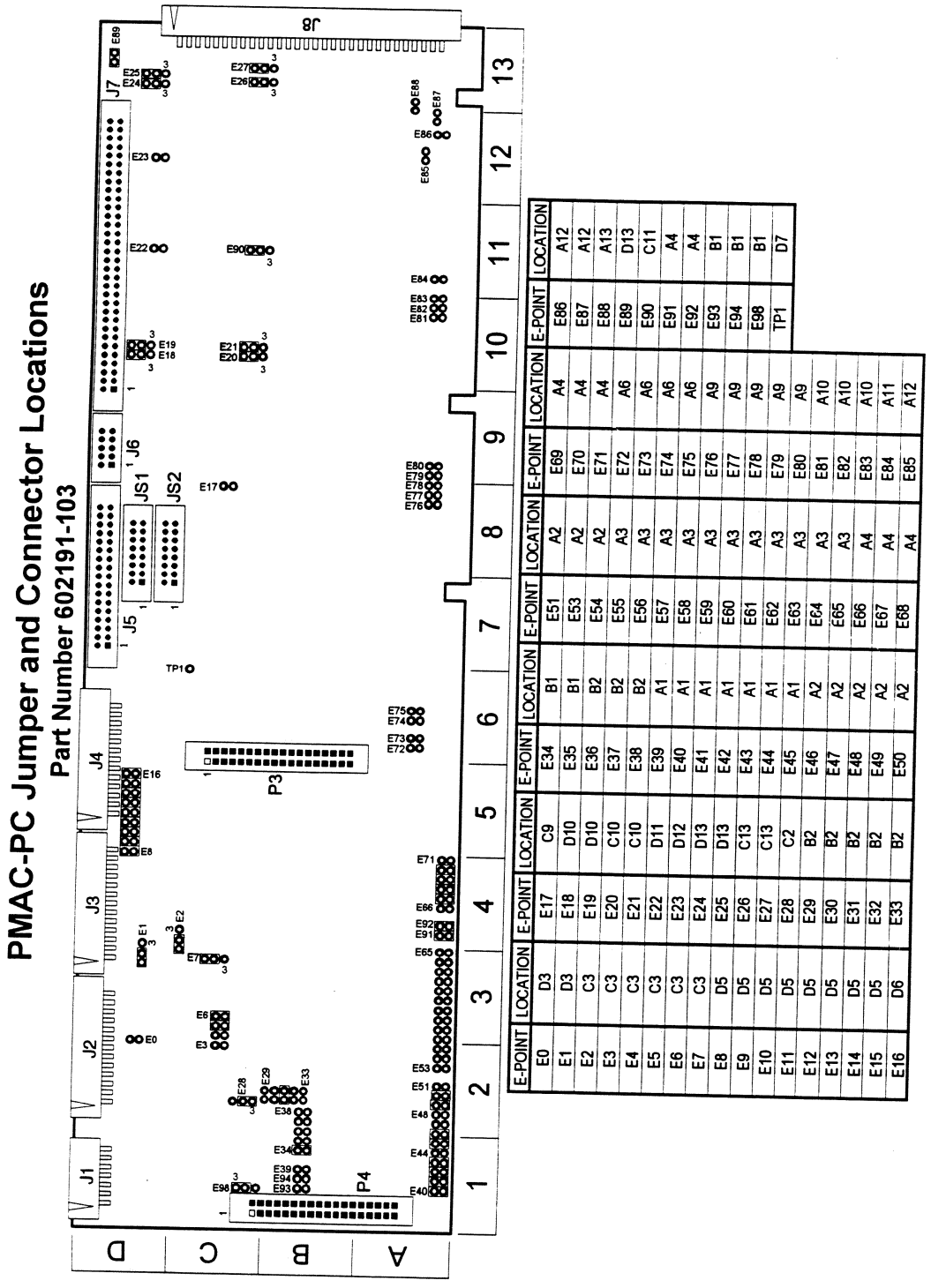
Only one display can be connected to the JDISP display port. This includes any of the Acc-12 family of displays and the built-in display in the Acc-16D control panel.

JSx Port Accessories

Each Acc-28 A/D converter board must interface to a separate DSPGATE gate array IC on PMAC or Acc-24P/V through its JSx connector. Therefore, the limitations on numbers of Acc-28s for a PMAC are as follows:

PMAC, no Opt 1; no Acc-24P/V	1 Acc-28	PMAC with Opt 1; Acc-24P, no Opt 1	3 Acc-28s
PMAC with Opt 1; no Acc-24P/V	2 Acc-28s	PMAC, no Opt 1; Acc-24P with Opt 1	3 Acc-28s
PMAC, no Opt 1; Acc-24P, no Opt 1	2 Acc-28s	PMAC with Opt 1; Acc-24P with Opt 1	4 Acc-28s

PMAC Board Layout Part Number 602191-103



E-POINT	LOCATION
E0	D3
E1	D3
E2	C3
E3	C3
E4	C3
E5	C3
E6	C3
E7	C3
E8	D5
E9	D5
E10	D5
E11	D5
E12	D5
E13	D5
E14	D5
E15	D5
E16	D6

E-POINT	LOCATION
E17	C9
E18	D10
E19	D10
E20	C10
E21	C10
E22	D11
E23	D12
E24	D13
E25	D13
E26	C13
E27	C13
E28	C2
E29	B2
E30	B2
E31	B2
E32	B2
E33	B2

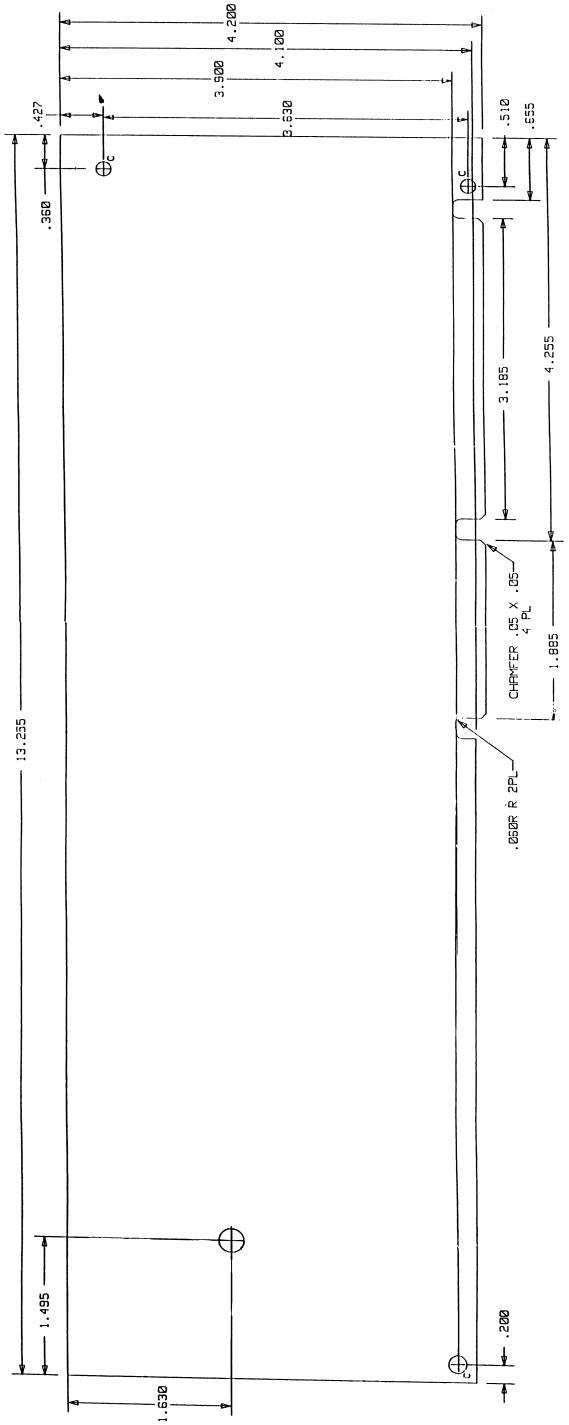
E-POINT	LOCATION
E34	B1
E35	B1
E36	B2
E37	B2
E38	B2
E39	A1
E40	A1
E41	A1
E42	A1
E43	A1
E44	A1
E45	A1
E46	A2
E47	A2
E48	A2
E49	A2
E50	A2

E-POINT	LOCATION
E51	A2
E53	A2
E54	A2
E55	A3
E56	A3
E57	A3
E58	A3
E59	A3
E60	A3
E61	A3
E62	A3
E63	A3
E64	A3
E65	A3
E66	A4
E67	A4
E68	A4

E-POINT	LOCATION
E69	A4
E70	A4
E71	A4
E72	A6
E73	A6
E74	A6
E75	A6
E76	A9
E77	A9
E78	A9
E79	A9
E80	A9
E81	A10
E82	A10
E83	A10
E84	A11
E85	A12

E-POINT	LOCATION
E86	A12
E87	A12
E88	A13
E89	D13
E90	C11
E91	A4
E92	A4
E93	B1
E94	B1
E98	B1
TP1	D7

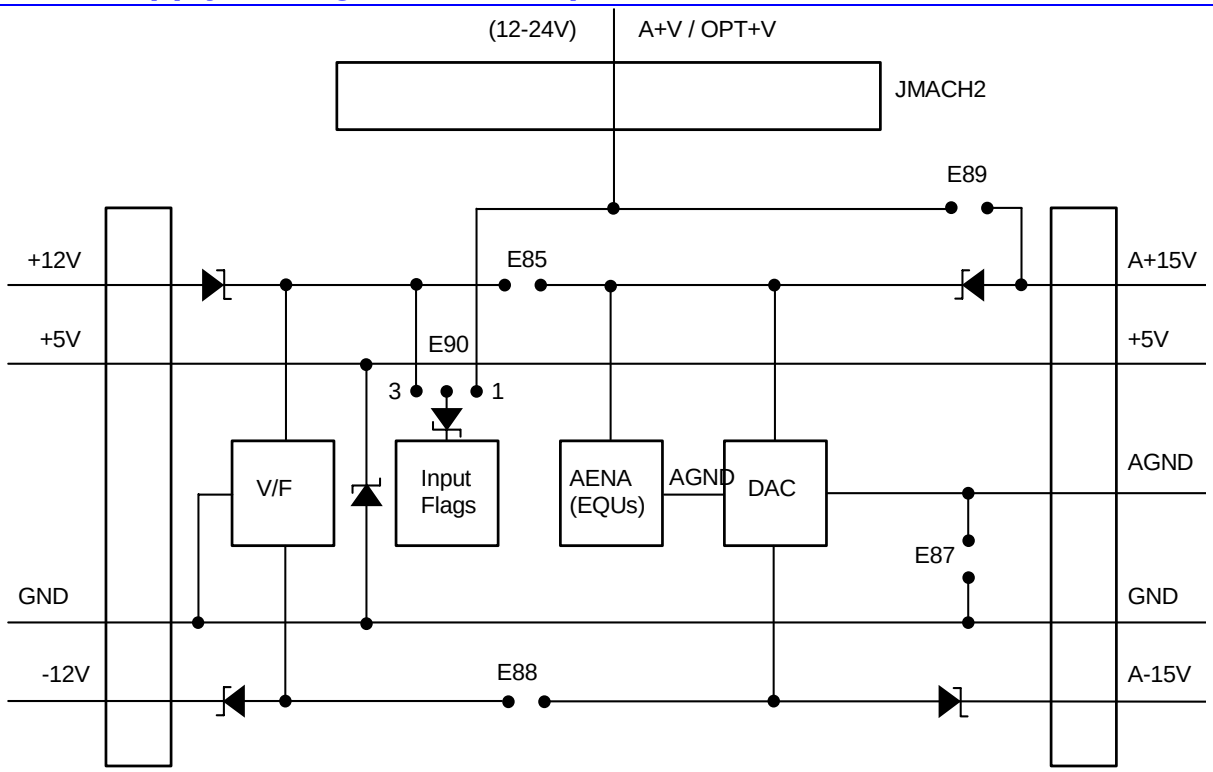
PMAC Board Dimensions Part Number 602191-103



JUMPERS SETUP SUMMARY

On the PMAC, there are many jumpers (pairs of metal prongs), called E-points. Some have been shorted together; others have been left open. These jumpers customize the hardware features of the board for a given application and must be set up appropriately. The following is an overview of the several PMAC jumpers grouped in appropriate categories. For a complete description of the jumper setup configuration, refer to the PMAC PC CPU Board E-Point Descriptions section.

Power-Supply Configuration Jumpers



Control – These jumpers control whether the analog circuitry on the PMAC PC is isolated from the digital circuitry, or electrically tied to it. In the default configuration, these jumpers are off, keeping the circuits isolated from each other (provided separate isolated supplies are used).

When E87 is on, it ties the digital GND reference signal to the analog AGND reference signal, defeating the isolation between the circuits. Putting E85 on ties the digital +12V supply line to the analog A+15V supply line. Putting E88 on ties the digital –12V supply line to the analog A-15V supply line. When these jumpers are on, they permit the bus +/-12V supply to power PMAC's analog circuits.

E89-E90: Input Flag Supply Control – If E90 connects pins 1 and 2, and E89 is on, the input flags (+LIMn, -LIMn, HMFLn, and FAULTn) are supplied from the analog A+15V supply, which can be isolated from the digital circuitry. If E90 connects pins 1 and 2 and E89 is off, the input flags are supplied from a separate A+V supply through pin 59 of the J7 JMACH2 connector (Option 1 is required.). This supply can be in the +12V to +24V range, and can be kept isolated from the digital circuitry. If E90 connects pins 2 and 3, the input flags are supplied from the digital +12V supply and isolation from the digital circuitry is defeated.

Clock Configuration Jumpers

E98: DAC/ADC Clock Frequency Control – Leave E98 in its default setting of 1-2, which creates a 2.45 MHz DCLK signal. If connecting an Acc-28 A/D-converter board, move the jumper to connect pins 2 and 3, which creates a 1.22 MHz DCLK signal.

E29-E33: Phase Clock Frequency Control – Only one of the jumpers E29 – E33, which select the phase-clock frequency, may be on in any configuration. The default setting of E31 ON, which selects a 9-kHz phase-clock frequency, is seldom changed.

E48: Option CPU Clock Frequency Control – When PMAC is ordered with Option 5B, E48 sets up the CPU clock frequency to either 40 MHz or 60 MHz. If PMAC is ordered with Option 5C, additional software setup is necessary for 80 MHz CPU clock frequency operation.

E3-E6: Servo Clock Frequency Control – The jumpers E3 – E6 determine the servo-clock frequency by controlling how many times it is divided down from the phase-frequency. The default setting of E3 and E4 OFF, E5 and E6 ON divides the phase-clock frequency by 4, creating a 2.25 kHz servo-clock frequency. This setting is seldom changed.

E34-E38: Encoder Sample Clock – Only one of the jumpers E34 – E38, which select the encoder sample clock frequency, may be on in any configuration. The frequency must be high enough to accept the maximum true count rate (no more than one count in any clock period), but a lower frequency can filter out longer noise spikes. The anti-noise digital delay filter can eliminate noise spikes up to one sample-clock cycle wide.

E40-43: Servo and Phase Clock Direction Control – Jumpers E40 – E43 control the software address of the card, for serial addressing and for sharing the servo and phase clock over the serial connector. Card @0 sends the clocks and cards @1 – @F receives the clocks. If any of these jumpers is removed, PMAC PC will expect to receive external servo and phase clock signals on the J4 serial port. If these signals are not provided in this configuration, the Watchdog timer will immediately trip.

Encoder Configuration Jumpers

E18-E21, E24-E27: Encoder Complementary Line Control – These jumpers, one per encoder, control the voltage to which the complementary channels A/, B/, and C/ are pulled. The default setting for each jumper, connecting pins 1 and 2, ties the complementary lines to 2.5V. This setting is required for single-ended encoders, and is best if the channel is left unconnected. If encoders with differential line drivers are used, the setting of these jumpers does not matter. Changing the jumpers to connect pins 2 and 3 ties the complementary lines to 5V. This setting is used for complementary open-collector encoders (now obsolete), or if external exclusive-or loss-of-encoder circuitry is used.

The following table shows which jumper affects which encoder channel:

ENC1	E27	**ENC2**	E26	**ENC3**	E25	**ENC4**	E24
ENC5	E21	**ENC6**	E20	**ENC7**	E19	**ENC8**	E18

E22-E23: Control-Panel Handwheel Enable – Putting these jumpers on ties the handwheel-encoder inputs on the JPAN control-panel port to the Channel 2 encoder circuitry. Since these inputs are single-ended, jumper E26 must connect pins 1 and 2. If the handwheel inputs are connected to Channel 2, no encoder should be connected to Channel 2 through the JMACH1 connector.

E72-E73: Control Panel Analog Input Enable – Putting these jumpers on ties the output of the Option 10 voltage-to-frequency converter that can process the Wiper analog input on the JPAN control panel port to the Channel 4 encoder circuitry. If the frequency signal is connected to Channel 4, no encoder should be connected to Channel 4 through the JMACH1 connector.

E74-E75: Encoder Sample Clock Output – Putting these jumpers on ties the encoder sample-clock signal to the CHC4 and CHC4/ lines on the JMACH1 port. This permits the clock signal to be used to synchronize external encoder-processing devices like the Acc-8D Option 8 interpolator board. With these jumpers on, no encoder input signal should be connected to these pins.

Board Reset/Save Jumpers

E39: Reset-From-Bus Enable – Putting this jumper on ties the ISA-bus reset line to the PMAC PC reset line so that a bus reset will automatically reset the PMAC. However, if this jumper is on and the PMAC PC is not installed in an ISA bus, the PMAC will be held permanently in its reset state and will not operate.

E93-E94: Reset from Bus by Software Enable – These jumpers permit hardware resets of the PMAC (which work even if the Watchdog timer has tripped) through software operations from the PC. If E93 is on, the PMAC PC powers up locked in the reset state. It can be put in the operational state by the PC writing a value of 40hex to {base address + 12}; it can be put back in the reset state by the PC writing a value of 40hex to {base address + 10}. If E94 is on, the PMAC PC powers up in operational mode. It can be put in reset mode by the PC writing a value of 40hex to {base address + 12}; it can be put back in operational mode by the PC writing a value of 40hex to {base address + 10}.

E51: Re-Initialization on Reset Control – If E51 is off (default), PMAC executes a normal reset, loading active memory from the last saved configuration in non-volatile flash memory. If E51 is on, PMAC re-initializes on reset, loading active memory with the factory default values.

E50: Flash-Save Enable/Disable Control – If E50 is on (default), the active software configuration of the PMAC can be stored to non-volatile flash memory with the **SAVE** command. If the jumper on E50 is removed, this **SAVE** function is disabled, and the contents of the flash memory cannot be changed.

Communication Jumpers

E9-E16: Serial Interface Configuration Control – With these jumpers in their default configuration (see detailed description), the J4 serial port can connect straight across to a DB-25 serial connector on a PC (or to a DB-9 connector through a standard adapter). In the alternate configuration (rarely used), the send and receive lines for both data and handshake signals are exchanged.

E8: Serial Converter Power-Supply Control – With this jumper on (default), 5V is supplied to the J4 serial connector for use by devices such as the Acc-26A. The jumper can be removed if this supply is not desired.

E44-E47: Serial Baud Rate Selection –The configuration of these jumpers and the particular CPU Option ordered will determine the baud rate at which PMAC will communicate through its J4 serial port. For example, when PMAC is ordered with no CPU Options and only the jumpers E45 and E46 are installed, the baud rate will be set at 9600 baud.

E49: Serial Communications Parity Control – Jump pin 1 to 2 for NO serial parity; remove jumper for ODD serial parity.

E66-E71, E91-E92: ISA Bus Base Address Control – Jumpers E91, E92, E66, E67, E68, E69, E70, and E71 on the PMAC PC determine the base address of the card in the I/O space of the host PC's expansion bus. Together, they form a binary number that specifies the 16 consecutive addresses on the bus where the card can be found. The jumpers form the base address in the following fashion:

Jumper	E91	E92	E66	E67	E68	E69	E70	E71
Bit #	11	10	9	8	7	6	5	4
Dec Value	2048	1024	512	256	128	64	32	16
Hex Value	800	400	200	100	80	40	20	10
If a jumper is on, the value it contributes to the base address is zero. If a jumper is off, the value it contributes to the base address is given in the table above. **Note:** On the PMAC PC, the jumpers are physically arranged in the same order they are presented in the above table.								

From Jumper Configuration To Address

To determine the address specified by a given jumper configuration, use the following formula:

(Decimal)
Address = 2048*E91 + 1024*E92 + 512*E66 + 256*E67 + 128*E68 + 64*E69 + 32*E70 + 16*E71
(Hexadecimal)
Address = $800*E91 + $400*E92 + $200*E66 + $100*E67 + $80*E68 + $40*E69 + $20*E70 + $10*E71

In each case, Exx = 1 if the jumper is off; Exx = 0 if the jumper is on.

Example: On a PMAC card, the jumpers are in the following configuration:

E91	E92	E66	E67	E68	E69	E70	E71
ON	ON	OFF	OFF	ON	ON	ON	ON

The address can be computed as:

Decimal Address = 0 + 0 + 512 + 256 + 0 + 0 + 0 + 0 = 768
Hex Address = 0 + 0 + $200 + $100 + 0 + 0 + 0 + 0 = $300

From Address To Jumper Configuration

Once an I/O address on the PC expansion port has been selected, use the following procedure to set the address jumpers:

1. Convert the address to a 3-digital hexadecimal value ($000 to $FFF, representing 0 to 4095). If the value does not fit in this range, PMAC cannot be set for this address. Make sure the last digit is 0; only addresses divisible by 16 are permitted as PMAC base addresses.

2. Take the first hex digit and convert it to binary. The binary digits represent bits 11 through 8 of the base address. Assign each binary digit to jumpers as follows:

Bit #	11(MSB)	10	9	8(LSB)
Jumper	E91	E92	E66	E67
Digit Value	8	4	2	1
Setting for 1	OFF	OFF	OFF	OFF
Setting for 0	ON	ON	ON	ON

3. Take the second hex digit and convert it to binary. The binary digits represent bits 7 through 4 of the base address. Assign each binary digit to jumpers as follows:

Bit #	7(MSB)	6	5	4(LSB)
Jumper	E68	E69	E70	E71
Digit Value	8	4	2	1
Setting for 1	OFF	OFF	OFF	OFF
Setting for 0	ON	ON	ON	ON

Example 1: Set up the card to be at base address 992 decimal on the PC expansion bus:

1. 992 decimal is equal to 3E0 hexadecimal.
2. The first digit of 3 is binary 0011. This sets E91 ON, E92 ON, E66 OFF, E67 OFF.
3. The second digit of E is binary 1110. This sets E68 OFF, E69 OFF, E70 OFF, E71 ON.

Example 2: Set up the card to be at base address 528 decimal on the PC expansion bus:

1. 528 decimal is equal to 210 hexadecimal.
2. The first digit of 2 is binary 0010. This sets E91 ON, E92 ON, E66 OFF, E67 ON.
3. The second digit of E is binary 0001. This sets E68 ON, E69 ON, E70 ON, E71 OFF.

Example 3: Set up the card to be at base address 544 decimal on the PC expansion bus:

1. 544 decimal is equal to 220 hexadecimal.
2. The first digit of 2 is binary 0010. This sets E91 ON, E92 ON, E66 OFF, E67 ON.
3. The second digit of E is binary 0010. This sets E68 ON, E69 ON, E70 OFF, E71 ON.

E54-E65: Interrupt Source Control – These jumpers control which signals are tied to interrupt lines IR5, IR6 and IR7 on PMAC's programmable interrupt controller (PIC), as shown in the interrupt diagram. Only one signal may be tied into each of these lines.

E76-E84, E86: Host Interrupt Signal Select – This bank of jumpers determines which ISA bus interrupt line can be used by the PMAC PC, as shown in the interrupt diagram. Only one of these sets of jumpers should be on any configuration.

I/O Configuration Jumpers

CAUTION:
A wrong setting of these jumpers will damage the associated output IC.

E1-E2: Machine Output Supply Configure – With the default sinking output driver IC (ULN2803A or equivalent) in U3 for the J5 JOPTO port outputs, these jumpers must connect pins 1 and 2 to supply the IC correctly. If this IC is replaced with a sourcing output driver IC (UDN2981A or equivalent), these jumpers must be changed to connect pins 2 and 3 to supply the new IC correctly.

E7: Machine Input Source/Sink Control – With this jumper connecting pins 1 and 2 (default), the machine input lines on the J5 JOPTO port are pulled up to +5V, or the externally provided supply voltage for the port. This configuration is suitable for sinking drivers. If the jumper is changed to connect pins 2 and 3, these lines are pulled down to GND. This configuration is suitable for sourcing drivers.

E17: Amplifier-Enable Polarity Control – With this jumper on (default), the amplifier-enable lines are low true, so the enable state is low-voltage output and sinking current, and the disable state is not conducting current. With the ULN2803A sinking driver used by the PMAC PC, this is the fail-safe option, allowing the circuit to fail in the disable state. With this jumper off, the amplifier-enable lines are high true so the enable state is not conducting current, and the disable state is low-voltage output and sinking current. This setting is not generally recommended.

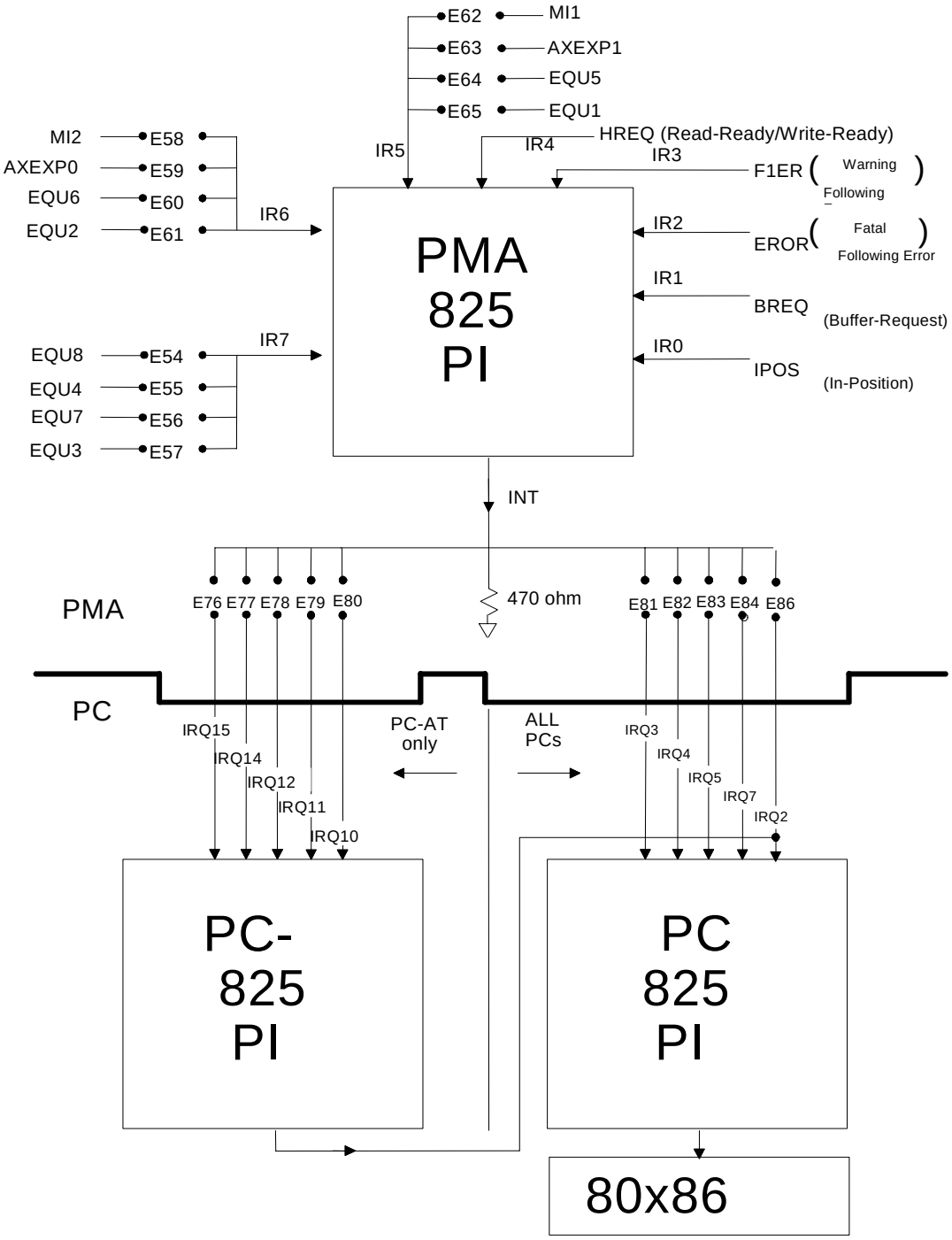
E28: Following-Error/Watchdog-Timer Signal Control – With this jumper connecting pins 2 and 3 (default), the FEFCO/ output on pin 57 of the J8 JMACH1 servo connector outputs the Watchdog timer signal. With this jumper connecting pins 1 and 2, pin 57 outputs the warning following the error status line for the selected coordinate system.

Reserved Configuration Jumpers

E0: Reserved for future use

E53: DSP Interrupt signal select – This function is not currently supported.

PMAC-PC



Piggyback CPU Board Jumper Configuration

E1: Watchdog Timer Jumper - Jumper E1 on the CPU board must be off for the Watchdog timer to operate. This is a very important safety feature, so it is vital that this jumper be OFF during normal operation. E1 should only be put on to debug problems with the Watchdog timer circuit.

E4: Power-Up/Reset Load Source – If jumper E4 on the CPU board is on during power-up/reset, the board comes up in bootstrap mode, which permits the loading of new firmware into the flash-memory IC on the board. When the PMAC Executive program tries to establish communications with a board in this mode, it will detect automatically that the board is in bootstrap mode and ask what file to download as the new firmware.

Jumper E4 must be off during power-up/reset for the board to come up in normal operational mode.

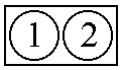
E2-E3 and E8: Expansion Port Configure – Jumpers E2, E3 and E8 permit variations in the configuration of signals on the 50-pin JEXP expansion port. Presently, no expansion-port accessories use the signals placed on the port by putting jumpers E2 and/or E3 on; these jumpers should be left off, unless an accessory manual has specific instructions to put them on.

Jumper E8 must connect pins 1 and 2 (putting address line 4 on the port at pin 31) to communicate to a PMAC2-style Acc-24 board (currently Acc-24P2 in ISA format). Presently, no expansion-port accessories use the signal placed on the port by connecting pins 2 and 3 of jumper E8.

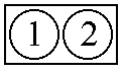
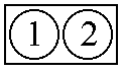
PMAC PC CPU BOARD E-POINT DESCRIPTIONS

The following jumper descriptions are for the PMAC CPU, part number 602705-107.

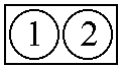
E1: Watchdog Disable Jumper

E Point and Physical Layout	Location	Description	Default
E1 		Jump pin 1 to 2 to disable Watchdog timer (for test purposes only). Remove jumper to enable Watchdog timer.	No jumper

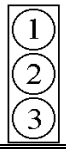
E2-E3: Expansion Port Configure

E Point and Physical Layout	Location	Description	Default
E2 	No longer used	No Jumper	
E3 	No longer used	No Jumper	

E4: Power-Up/Reset Load Source

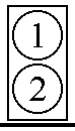
E Point and Physical Layout	Location	Description	Default
E4 		Jump pin 1 to 2 to reload firmware through serial or bus port. Must also install E51 jumper on baseboard. Remove jumper for normal operation.	No jumper

E8: Expansion Port Configure

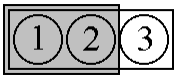
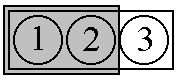
E Point and Physical Layout	Location	Description	Default
E8 		Jump pin 1 to 2 for using the Acc-24P2 expansion board. Remove jumper for normal operation.	No jumper

PMAC PC MAIN BOARD E-POINT JUMPER DESCRIPTIONS

E0: For Future Use

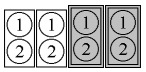
E Point and Physical Layout	Location	Description	Default
E0 	D3	For future use.	No jumper

E1 - E2: Machine Output Supply Voltage Configure

E Point and Physical Layout	Location	Description	Default
E1 	D3	**CAUTION:** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to apply +V (+5V to 24V) to pin 11 of U3 (should be ULN2803A for sink output configuration) JOPTO Machine outputs M01-M08. Jump pin 2 to 3 to apply GND to pin 11 of U3 (should be UDN2981A for source output configuration).	1 and 2 Jumper installed
E2 	C3	**CAUTION** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to apply GND to pin 10 of U3 (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply +V (+5V to 24V) to pin 10 of U3 (should be UDN2981A for source output configuration).	1 and 2 Jumper installed

E3 - E6: Servo Clock Frequency Control

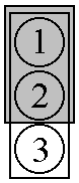
The servo clock (which determines how often the servo loop is closed) is derived from the phase clock (see E98, E29 - E33) through a divide-by-N counter. Jumpers E3 through E6 control this dividing function.

E3	E4	E5	E6	Servo Clock = Phase Clock Divided by N	Default and Physical Layout E3 E4 E5 E6  Location C3 C3 C3 C3
ON	ON	ON	ON	N = divided by 1	
OFF	ON	ON	ON	N = divided by 2	
ON	OFF	ON	ON	N = divided by 3	
OFF	OFF	ON	ON	N = divided by 4	Only E5 and E6 on
ON	OFF	ON	ON	N = divided by 5	
OFF	ON	OFF	ON	N = divided by 6	
ON	OFF	OFF	ON	N = divided by 7	
OFF	OFF	OFF	ON	N = divided by 8	
ON	ON	ON	OFF	N = divided by 9	
OFF	ON	ON	OFF	N = divided by 10	
ON	OFF	ON	OFF	N = divided by 11	
OFF	OFF	ON	OFF	N = divided by 12	
ON	ON	OFF	OFF	N = divided by 13	
OFF	ON	OFF	OFF	N = divided by 14	
ON	OFF	OFF	OFF	N = divided by 15	
OFF	OFF	OFF	OFF	N = divided by 16	

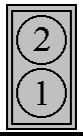
Note: The setting of I-variable I10 should be adjusted to match the servo interrupt cycle time set by E98, E3 through E6, E29 through E33, and the crystal clock frequency. I10 holds the length of a servo interrupt cycle, scaled so that 8,388,608 equals one millisecond. Since I10 has a maximum value of 8,388,607, the servo interrupt cycle time should always be less than a millisecond (unless the basic unit of time on PMAC should be something other than a millisecond). To change the servo sample time to greater than one millisecond, the sampling may be slowed in software with variable Ix60.
Frequency can be checked on J4 pins 21 and 22. It can also be checked using the software by typing RX:0 in the PMAC terminal at 10-second intervals, and dividing the difference of successive responses by 10000. The resulting number is the approximate Servo Clock frequency kHz.

Note: If E40-E43 are not all on, the phase clock is received from an external source through the J4 serial-port connector, and the settings of E3 – E6 are not relevant.

E7: Machine Input Source/Sink Control

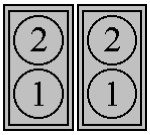
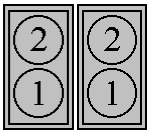
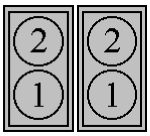
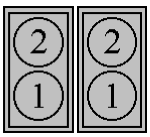
E Point and Physical Layout	Location	Description	Default
E7 	C3	Jump pin 1 to 2 to apply +5V to input reference resistor sip pack; this will bias MI1 to MI8 inputs to +5V for off state; input must then be grounded for on state. Jump pin 2 to 3 to apply GND to input reference resistor sip pack; this will bias MI1 to MI8 inputs to GND for off state; input must then be pulled up for on state (+5V to +24V).	1 and 2 Jumper installed

E8: RS232 Converter Power Supply Control

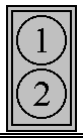
E Point and Physical Layout	Location	Description	Default
E8 	D5	Jump pin 1 to 2 to apply +5V to J4 pin 2 (JRS422). This can be used to power optional RS422 to RS232 converter module which requires +5V for operation.	Jumper installed

E9 - E16: Serial Interface Handshake Control

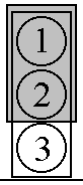
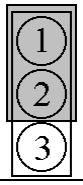
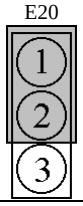
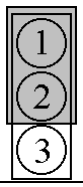
The E9 through E16 jumpers control whether the RS-422 serial port will be in DCE or DTE format. The default configuration permits straight-across connection to a PC DB-25 serial port.

E Point and Physical Layout	Location	Description	Default
E9 E10 	D5	Jump, E9-1 to E9-2 to allow RD- to be input on J4-3. Jump E10-1 to E10-2 to allow SD- to be output on J4-5. Jump E9-1 to E10-1 to allow RD- to be output on J4-3. Jump E9-2 to E10-2 to allow SD- to be input on J4-5.	1 and 2 Jumper installed
E11 E12 	D5	Jump E11-1 to E11-2 to allow RD+ to be input on J4-4. Jump E12-1 to E12-2 to allow SD+ to be output on J4-6. Jump E11-1 to E12-1 to allow RD+ to be output on J4-4. Jump E11-2 to E12-2 to allow SD+ to be input on J4-6.	1 and 2 Jumper installed
E13 E14 	D5	Jump E13-1 to E13-2 to allow CS+ to be input on J4-7. Jump E14-1 to E14-2 to allow RS+ to be output on J4-9. Jump E13-1 to E14-1 to allow CS+ to be output on J4-7. Jump E14-2 to E14-2 to allow RS+ to be input on J4-9.	*1 and 2 Jumper installed*
E15 E16 	D5 D6	Jump E15-1 to E15-2 to allow CS- to be input on J4-8. Jump E16-1 to E16-2 to allow RS- to be output on J4-10. Jump E15-1 to E16-1 to allow CS- to be output on J4-8. Jump E15-2 to E16-2 to allow RS- to be input on J4-10.	1 and 2 Jumper installed

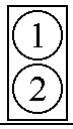
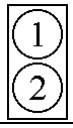
E17: Amplifier Enable/Direction Polarity Control

E Point and Physical Layout	Location	Description	Default
E17 	C9	Jump 1 and 2 for low true AENA (axes 1-8). Remove jumper for high true AENA (axes 1-8).	1 and 2 Jumper installed

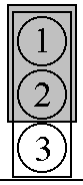
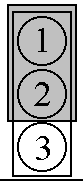
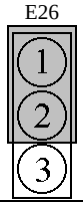
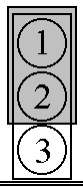
E18 - E21: Encoder Single-Ended/Differential Control

E Point and Physical Layout	Location	Description	Default
E18 	D10	ENC 5 through 8: Jump pin 1 to 2 to tie complementary encoder inputs to 2.5V.	1 and 2 Jumper installed for E18 - E2
E19 	D10	Jump pin 2 to 3 to tie complementary encoder inputs to 5V. For no encoder connection: Jump pin 1 to 2.	E18: ENC 5 E19: ENC 6 E20: ENC 7 E21: ENC 8
E20 	C10	For single-ended encoders: Jump pin 1 to 2. For differential line-driver encoders: Settings do not matter.	
E21 	C10	For complementary open-collector encoders, jump pin 2 to 3.	
Note: Unused encoders should be left non-differential to prevent noise pickup.			

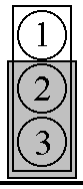
E22 - E23: Control Panel Handwheel Enable

E Point and Physical Layout	Location	Description	Default
E22 	D11	Jump pin 1 to 2 to obtain handwheel encoder signal from front panel at J2-16 for CHB2 (ENC2-B).	No jumper
E23 	D12	Jump pin 1 to 2 to obtain handwheel encoder signal from front panel at J2-22 for CHA2 (ENC2-A).	No jumper
Note: With these jumpers ON, no encoder should be wired into ENC2 on JMACH1. Jumper E26 must connect pins 1 and 2, because these are single-ended inputs. This function is unrelated to the encoder brought in through Acc-39 on J2.			

E24 - E27: Encoder Single-Ended/Differential Control

E Point and Physical Layout	Location	Description	Default
E24 	D13	ENC 4 through 1: Jump pin 1 to 2 to tie complementary encoder inputs to 2.5V.	1 and 2 Jumper installed for E24 - E27.
E25 	D13	Jump pin 2 to 3 to tie complementary encoder inputs to 5V. For no encoder connection: Jump pin 1 to 2.	E24: ENC 4 E25: ENC 3 E26: ENC 2 E27: ENC 1
E26 	C13	For single-ended encoders: Jump pin 1 to 2. For differential line-driver encoders: Settings do not matter.	
E27 	C13	For complementary open-collector encoders: Jump pin 2 to 3.	

E28: Following Error/Watchdog Timer Signal Control

E Point and Physical Layout	Location	Description	Default
E28 	C2	Jump pin 1 to 2 to allow warning following error (Ix12) for the selected coordinate system to control FEFCO/ on J8-57. Jump pin 2 to 3 to cause Watchdog timer output to control FEFCO/. Low true output in either case.	2-3 Jumper installed

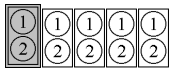
E29 - E33: Phase Clock Frequency Control

Jumpers E29 through E33 control the speed of the phase clock, and, indirectly, the servo clock, which is divided down from the phase clock (see E3 - E6). No more than one of these five jumpers may be on at a time.

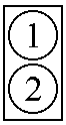
					Phase Clock Frequency		Default and Physical Layout	
E29	**E30**	**E31**	**E32**	**E33**	**E98 Connects Pins 1 and 2**	**E98 Connects Pins 2 And 3**		**Location**
ON	OFF	OFF	OFF	OFF	2.26 kHz	1.13 kHz	 E29	B2
OFF	ON	OFF	OFF	OFF	4.52 kHz	2.26 kHz	 E30	B2
OFF	OFF	ON	OFF	OFF	9.04 kHz	4.52 kHz	 E31	B2
OFF	OFF	OFF	ON	OFF	18.07 kHz	9.04 kHz	 E32	B2
OFF	OFF	OFF	OFF	ON	36.14 kHz	18.07 kHz	 E33	B2
Note: If E40-E43 are not all ON, the phase clock is received from an external source through the J4 serial-port connector, and the settings of E29-E33 are not relevant.								

E34 - E38: Encoder Sampling Clock Frequency Control

Jumpers E34 through E38 control the encoder sampling clock (SCLK) used by the gate array ICs. No more than one of these five jumpers may be on at a time.

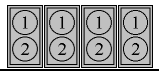
						Default and Physical Layout
						E34 E35 E36 E37 E38  **Location; All At B2**
E34	**E35**	**E36**	**E37**	**E38**	**SCLK Clock Frequency**	
ON	OFF	OFF	OFF	OFF	9.8304 MHz	E34 ON
OFF	ON	OFF	OFF	OFF	4.9152 MHz	
OFF	OFF	ON	OFF	OFF	2.4576 MHz	
OFF	OFF	OFF	ON	OFF	1.2288 MHz	
OFF	OFF	OFF	OFF	ON	External Clock 1 To 30 Mhz maximum input on Chc4 and Chc4/	

E39: Reset-from-Bus Enable

E Point and Physical Layout	Location	Description	Default
E39 	B1	Jump pin 1 to 2 to allow PMAC PC to derive its reset from the PC backplane. Remove jumper to allow PMAC PC to power up in the normal way; PC BUS hardware reset will not reset PMAC PC. This must be removed for standalone operation. Only one of E39, E93, and E94 jumpers should be on at once. See also E93 and E94	No jumper

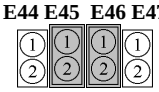
E40 - E43: Software Address Control

Jumpers E40 - E43 control the software address of the card, for serial addressing and for sharing the servo and phase clock over the serial connector. Card @0 sends the clocks and cards @1-@F receive the clocks.

Card Address Control E Points					**Default and Physical Layout** 
E40	E41	E42	E43	**Card Address**	**Location A1 A1 A1 A1**
ON	ON	ON	ON	*@0*	@0
OFF	ON	ON	ON	@1	
ON	OFF	ON	ON	@2	
OFF	OFF	ON	ON	@3	
ON	ON	OFF	ON	@4	
OFF	ON	OFF	ON	@5	
ON	OFF	OFF	ON	@6	
OFF	OFF	OFF	ON	@7	
ON	ON	ON	OFF	@8	
OFF	ON	ON	OFF	@9	
ON	OFF	ON	OFF	@A	
OFF	OFF	ON	OFF	@B	
ON	ON	OFF	OFF	@C	
OFF	ON	OFF	OFF	@D	
ON	OFF	OFF	OFF	@E	
OFF	OFF	OFF	OFF	@F	
Note: The card must either be set up as @0, or receiving clock signals over the serial port from another card that is set up as @0, or the Watchdog timer will trip (red light on) and the card will shut down.					

E44 - E47: Serial Port Baud Rate

Jumpers E44 - E47 control what baud rate to use for serial communications. Any character received over the bus causes PMAC to use the bus for its standard communications. The serial port is disabled if E44-E47 are all on. The baud rate setting of an 80 MHz CPU section ordered with Opt 5C is performed by software; please refer to the dedicated section on the Software Configuration chapter of this manual.

Baud Rate Control E Points				Baud Rate			Default and Physical Layout
E44	**E45**	**E46**	**E47**	**Option 4A**	**Standard, Option 5A**	**Option 5, Option 5B**	**E44 E45 E46 E47**  **Loc. C3 C3 C3 C3**
ON	ON	ON	ON	Disabled	Disabled	Disabled	*Graphic is for a PMAC with a Standard or Option 5A CPU*
OFF	ON	ON	ON	300	600	900	
ON	OFF	ON	ON	400*	800*	1200	
OFF	OFF	ON	ON	600	1200	1800	
ON	ON	OFF	ON	800*	1600*	2400	
OFF	ON	OFF	ON	1200	2400	3600	
ON	OFF	OFF	ON	1600*	3200*	4800	
OFF	OFF	OFF	ON	2400	4800	7200	
ON	ON	ON	OFF	3200*	6400*	9600	Options 5, 5B
OFF	ON	ON	OFF	4800	9600	14400	Std., Opt. 5A
ON	OFF	ON	OFF	6400*	12800*	19200	
OFF	OFF	ON	OFF	9600	19200	28800	Option 4A
ON	ON	OFF	OFF	12800*	25600*	38400	
OFF	ON	OFF	OFF	19200	38400	57600	
ON	OFF	OFF	OFF	25600*	51200*	76800	
OFF	OFF	OFF	OFF	38400	76800	115200	

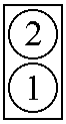
*Non-standard baud rates.
Note: These jumpers are only used to set the baud rate at power-on/reset.

E48: CPU Clock Frequency Control (Option CPU Section)

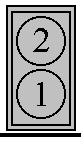
E48 controls the CPU clock frequency only on PMAC, with an option CPU section using flash memory backup (no battery). This CPU section is used on PMACs ordered with Opt 4A, 5A, or 5B. The 80 MHz setting of a CPU section ordered with Opt 5C is performed by software; please refer to the Software Configuration chapter of this manual.

WARNING:

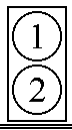
It may be possible to operate a board with 40 MHz components (Option 5A) at 60 MHz under some conditions by changing the setting of jumper E48. However, this operates the components outside of their specified operating range, and proper execution of PMAC under these conditions is not guaranteed. PMAC software failure is possible, even probable, under these conditions, and this can lead to very dangerous machine failure. Operation in this mode is done completely at the user's own risk. Delta Tau can accept no responsibility for the operation of PMAC or the machine under these conditions.

E Point and Physical Layout	Location	Description	Default
E48 	C2	Jump pins 1 and 2 to multiply crystal frequency by 3 inside CPU for 60 MHz operation. Remove jumper to multiply crystal frequency by 2 inside CPU for 40 MHz operation.	Jumper installed (Option 5, 5B) Jumper not installed (Standard, Option 4A, 5A)

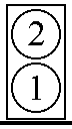
E49: Serial Communications Parity Control

E Point and Physical Layout	Location	Description	Default
E49 	A2	Jump pin 1 to 2 for NO serial parity; remove jumper for ODD serial parity.	Jumper installed

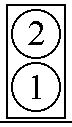
E50: Flash Save Enable/Disable

E Point and Physical Layout	Location	Description	Default
E50 	A2	Jump pin 1 to 2 to enable save to flash memory. Remove jumper to disable save to flash memory.	Jumper Installed

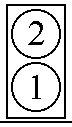
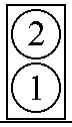
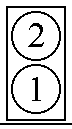
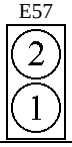
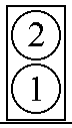
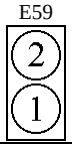
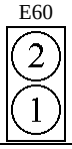
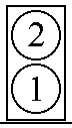
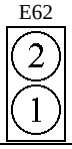
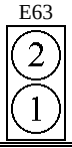
E51: Normal/Re-Initializing Power-Up

E Point and Physical Layout	Location	Description	Default
E51 	A2	Jump pin 1 to 2 to re-initialize on power-up/reset. Remove jumper for normal power-up/ reset.	No jumper installed

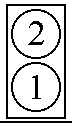
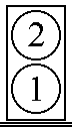
E53: DSP Interrupt Signal Select

E Point and Physical Layout	Location	Description	Default
E53 	A2	Jump pin 1 to 2 to allow MI3 to interrupt local DSP-CPU at IRQB.	No jumper installed
Note: Currently, the software does not support this function.			

E54 - E65: Host Interrupt Signal Select

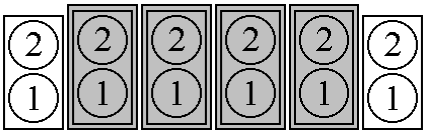
E Point and Physical Layout	Location	Description	Default
E54 	A2	Jump pin 1 to 2 to allow EQU8 to interrupt host-PC at PMAC interrupt level IR7.	No jumper installed
E55 	A3	Jump pin 1 to 2 to allow EQU4 to interrupt host-PC at PMAC interrupt level IR7.	No jumper installed
E56 	A3	Jump pin 1 to 2 to allow EQU7 to interrupt host-PC at PMAC interrupt level IR7.	No jumper installed
E57 	A3	Jump pin 1 to 2 to allow EQU3 to interrupt host-PC at PMAC interrupt level IR7.	No jumper installed
E58 	A3	Jump pin 1 to 2 to allow MI2 to interrupt host-PC at PMAC interrupt level IR6.	No jumper installed
E59 	A3	Jump pin 1 to 2 to allow Axis Expansion INT-0 to interrupt host-PC at PMAC interrupt level IR6.	No jumper installed
E60 	A3	Jump pin 1 to 2 to allow EQU6 to interrupt host-PC at PMAC interrupt level IR6.	No jumper installed
E61 	A3	Jump pin 1 to 2 to allow EQU2 to interrupt host-PC at PMAC interrupt level IR6.	No jumper installed
E62 	A3	Jump pin 1 to 2 to allow MI1 to interrupt host-PC at PMAC interrupt level IR5.	No jumper installed
E63 	A3	Jump pin 1 to 2 to allow AXIS EXPANSION INT-1 to interrupt host-PC at PMAC interrupt level IR5.	No jumper installed

E54 - E65: Host Interrupt Signal Select (Continued)

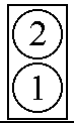
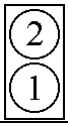
E Point and Physical Layout	Location	Description	Default
E64 	A3	Jump pin 1 to 2 to allow EQU5 to interrupt host-PC at PMAC interrupt level IR5.	No jumper installed
E65 	A3	Jump pin 1 to 2 to allow EQU1 to interrupt host-PC at PMAC interrupt level IR5.	No jumper installed

E66 - E71: Bus Base Hardware Address

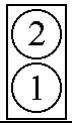
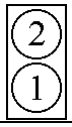
These jumpers work with E91 and E92 to set the base address of PMAC PC on the PC bus. See E91 – E92 — PMAC PC Bus Addressing for details on how to set these jumpers.

E Point and Physical Layout	Location	Description	Default
E66 E67 E68 E69 E70 E71 	A4	E66 - Bit 9 PC bus base address E67 - Bit 8 PC bus base address E68 - Bit 7 PC bus base address E69 - Bit 6 PC bus base address E70 - Bit 5 PC bus base address E71 - Bit 4 PC bus base address	E67-E70 installed
Note: ON = 0 and OFF = 1 for E66 - E71.			

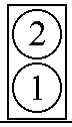
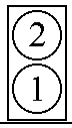
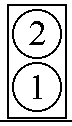
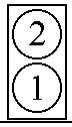
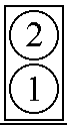
E72 - E73: Panel Analog Time Base Signal Enable

E Point and Physical Layout	Location	Description	Default
E72 	A6	Jump pin 1 to 2 to allow V to F converter FOUT (derived from Wiper input) on J2 to connect to CHA4.	No jumper installed
E73 	A6	Jump pin 1 to 2 to allow V to F converter FOUT/ (derived from Wiper input) on J2 to connect to CHA4/.	No jumper installed
Note: With these jumpers on, no encoder should be wired into ENC4 on JMACH1. E27 must connect pins 1 to 2 because these are single-ended inputs. Variable I915 should be set to 4 to create a positive voltage (frequency) number in PMAC.			

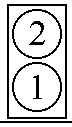
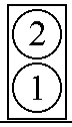
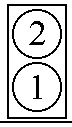
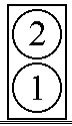
E74 - E75: Clock Output Control For Ext. Interpolation

E Point and Physical Layout	Location	Description	Default
E74 	A6	Jump pin 1 to 2 to allow SCLK/ to output on CHC4/.	No jumper installed
E75 	A6	Jump pin 1 to 2 to allow SCLK to output on CHC4.	No jumper installed
Note: No jumper permits synchronous latching of analog encoder interpolators such as Acc-8D Opt 8.			

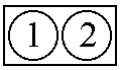
E76 - E84: Host Interrupt Signal Select

E Point and Physical Layout	Location	Description	Default
E76 	A9	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ14.	No jumper installed
E77 	A9	Jump pin 1 to 2 to allow PMAC- Interrupt to host-PC on IRQ15.	No jumper installed
E78 	A9	Jump pin 1 to 2 to allow PMAC- Interrupt to host-PC on IRQ12.	No jumper installed
E79 	A9	Jump pin 1 to 2 to allow PMAC- Interrupt to host-PC on IRQ11.	No jumper installed
E80 	A9	Jump pin 1 to 2 to allow PMAC- Interrupt to host-PC on IRQ10.	No jumper installed

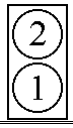
E76 - E84: Host Interrupt Signal Select (Continued)

E Point and Physical Layout	Location	Description	Default
E81 	A10	Jump pin 1 to 2 to allow PMAC- Interrupt to host-PC on IRQ3.	No jumper installed
E82 	A10	Jump pin 1 to 2 to allow PMAC- Interrupt to host-PC on IRQ4.	No jumper installed
E83 	A10	Jump pin 1 to 2 to allow PMAC- Interrupt to host-PC on IRQ5.	No jumper installed
E84 	A11	Jump pin 1 to 2 to allow PMAC- Interrupt to host-PC on IRQ7.	No jumper installed

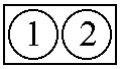
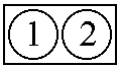
E85: Host-Supplied Analog Power Source Enable

E Point and Physical Layout	Location	Description	Default
E85 	A12	Jump pin 1 to 2 to allow A+14V to come from PC bus. This ties the amplifier and PMAC PC power supply together and defeats OPTO coupling.	No jumper
Note: If E85 is changed, E88 and E87 must also be changed. See E90.			

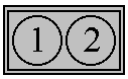
E86: Host Interrupt Signal Select

E Point and Physical Layout	Location	Description	Default
E86 	A12	Jump pin 1 to 2 to allow PMAC- Interrupt to host-PC on IRQ2.	No jumper

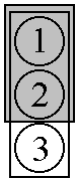
E87 - E88: Host-Supplied Analog Power Source Enable

E Point and Physical Layout	Location	Description	Default
E87 	A12	Jump pin 1 to pin 2 to allow AGND to come from PC bus. This ties the amplifier and PMAC PC GND together and defeats OPTO coupling.	No jumper
Note: If E87 is changed, E85 and E88 must also be changed. See E90.			
E88 	A13	Jump pin 1 to pin 2 to allow A-14V to come from PC bus. This ties the amplifier and PMAC PC power supply together and defeats OPTO coupling.	No jumper
Note: If E88 is changed, E87 and E85 must also be changed. See E90.			

E89: Amplifier-Supplied Switch Pull-Up Enable

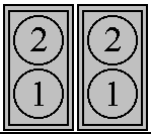
E Point and Physical Layout	Location	Description	Default
E89 	D13	Jump pin 1 to 2 to use A+15V on J8 (JMACH1) pin 59 as supply for input flags. Remove jumper to use A+15V/OPT+V from J7 pin 59 as supply for input flags.	Jumper installed
Note: This jumper setting is relevant only if E90 connects pin 1 to 2.			

E90: Host-Supplied Switch Pull-Up Enable

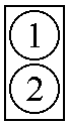
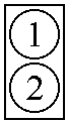
E Point and Physical Layout	Location	Description	Default
E90 	C11	Jump pin 1 to 2 to use A+15V from J8 pin 59 as supply for input flags (E89 on) flags should be tied to AGND or A+15V/OPT+V from J7 pin 59 as supply for input flags (E89 off). Flags should be tied to separate 0V reference. Jump pin 2 to 3 to use +12V from PC bus connector P1-pin B09 as supply for input flags. Flags should be tied to GND. See also E85, E87, E88 and PMAC OPTO-isolation diagram	1 and 2 Jumper installed

E91 - E92: Bus Base Address Select (High Bits)

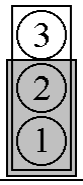
These jumpers work with E66 - E71 to set the base address of PMAC PC on the PC bus. For details on how to set these jumpers, see the Jumpers Setup Summary chapter of this manual.

E Point and Physical Layout	Location	Description	Default
E91 E92 	A4	E91 - Bit 11 PC bus base address E92 - Bit 10 PC bus base address ON = 0 OFF = 1	Jumper installed

E93 - E94: Reset from Bus by Software Enable

E Point and Physical Layout	Location	Description	Default
E93 	B1	Jump 1 to 2 to provide hardware reset of PMAC PC under the software control of the host-PC. PMAC PC will power up and stay in the Reset state until PC software writes 40 HEX to BASE+12. PMAC PC can be put in reset state by PC writing 40 HEX to BASE+10. Remove jumper to disable this function. Only one of E39, E93, E94 E-Points should be on at the same time.	No jumper
E94 	B1	Jump to 2 to provide hardware reset of PMAC PC under the software control of the host-PC. PMAC PC will power up in Normal mode. PMAC PC can be placed in reset state by PC writing 40 HEX to BASE+12. PMAC PC can be released from reset state by PC writing 40 HEX to BASE+10. Remove jumper to disable this function. Only one of E39, E93, E94 E-Points should be on at the same time.	No jumper

E98: DAC/ADC Clock Frequency Control

E Point and Physical Layout	Location	Description	Default
E98 	D4	Jump 1 and 2 to provide a 2.45 MHz DCLK signal to DACs and ADCs. Jump 2 and 3 to provide a 1.22 MHz DCLK signal to DACs and ADCs. This is important for high accuracy A/D conversion on Acc-28.	1 and 2 Jumper installed
Note: This also divides the phase and servo clock frequencies in half. See E29-E33, E3-E6, I10.			

MACHINE CONNECTIONS

Typically, the user connections are made to a terminal block that is attached to the JMACH connector via a flat cable (Accessory 8D or 8P). The pinout numbers on the terminal block are the same as those on the JMACH connector. The following are possible choices for breakout boards:

Board	Mounting	Breakout Style	Breakout Connector	Notes
Acc-8P	DIN – Rail	Monolithic	Terminal Block	Simple Phoenix contact board
Acc-8D	DIN – Rail	Monolithic	Terminal Block	Headers for connection to option boards
Acc-8DCE	DIN – Rail	Modular	D-sub connector	Fully shielded for easy CE mark compliance
Acc-8DP	Panel	Modular	D-sub connector	Used in the PC-pack product

Power Supplies

Digital Power Supply

```
2A @ +5V (+/-5%) (10 W)
(Eight-channel configuration, with a typical load of encoders)
```

The host computer provides the 5V power supply, in case PMAC is installed in its internal bus.

With the board plugged into the bus, it will pull +5V power from the bus automatically and cannot be disconnected. In this case, there must be no external +5V supply, or the two supplies will fight each other, possibly causing damage. This voltage could be measured between pins 1 and 3 of the terminal block.

In a stand-alone configuration, when PMAC is not plugged into a computer bus, it will need an external five-volt supply to power its digital circuits. The +5V line from the supply should be connected to pin 1 or 2 of the JMACH connector (usually through the terminal block) and the digital ground to pin 3 or 4. Acc-1x provides different options for the 5V power supply.

Analog Power Supply

```
0.3A @ +12 to +15V (4.5W)
0.25A @ -12 to -15V (3.8W)
(Eight-channel configuration)
```

The analog output circuitry on PMAC is optically isolated from the digital computation circuitry, and so requires a separate power supply. This is brought in on the JMACH connector. The positive supply (+12 to +15V) should be brought in on the A+15V line on pin 59. The negative supply (-12 to -15V) should be brought in on the A-15V line on pin 60. The analog common should be brought in on the AGND line on pin 58.

Typically this supply can come from the servo amplifier; many commercial amplifiers provide such a supply. If this is not the case, an external supply may be used. Acc-2x provides different options for the ± 15V power supply. Even with an external supply, the AGND line should be tied to the amplifier common. It is possible to get the power for the analog circuits from the bus, but doing so defeats optical isolation. In this case, no new connections need to be made. However, make sure jumpers E85, E87, E88, E89, and E90 are set up for this circumstance. (The card is not shipped from the factory in this configuration.)

Flags Power Supply (Optional)

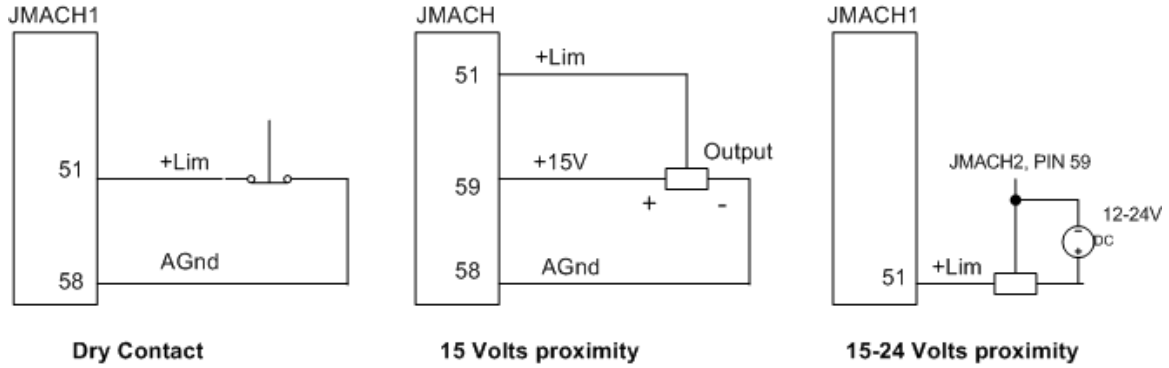
Each channel of PMAC has four dedicated digital inputs on the machine connector: +LIMn, -LIMn (overtravel limits), HMFLn (home flag), and FAULTn (amplifier fault). If the PMAC is ordered with the Option-1 (8-axis PMAC), these inputs can be kept isolated from other circuits. A power supply from 12 to 24V connected on pin 59 of J7 could be used to power the corresponding OPTO-isolators. In this case, jumper E89 must be removed and jumper E90 must connect pins 1 and 2.

Overtravel Limits and Home Switches

When assigned to dedicated uses, these signals provide important safety and accuracy functions. +LIMn and -LIMn are direction-sensitive overtravel limits that must be actively held low (sourcing current from the pins to ground) to permit motion in their direction. The direction sense of +LIMn and -LIMn is as follows: +LIMn should be placed at the negative end of travel, and -LIMn should be placed at the positive end of travel.

Types of Overtravel Limits

PMAC expects a closed-to-ground connection for the limits to be considered valid. This arrangement provides a failsafe condition and therefore cannot be reconfigured. Usually a passive normally closed switch is used. If a proximity switch is needed instead, use a 15 volts normally closed to ground NPN sinking type sensor.



Dry Contact **15 Volts proximity** **15-24 Volts proximity**

Jumper E89 and E90 must be set appropriately for the type of sensor used.

Home Switches

While normally closed-to-ground switches are required for the overtravel limits inputs, the home switches could be either normally closed or normally open types. The polarity is determined by the home sequence setup, through the I-variables I902 and I907 through I977. However, for the following reasons, the same type of switches used for overtravel limits are recommended:

- Normally closed switches are proven to have greater electrical noise rejection than normally open types.
- Using the same type of switches for every input flag simplifies maintenance stock and replacements.

Motor Signals Connections

Incremental Encoder Connection

Each JMACH connector provides two +5V outputs and two logic grounds for powering encoders and other devices. The +5V outputs are on pins 1 and 2; the grounds are on pins 3 and 4. The encoder signal pins are grouped by number. Those numbered 1 (CHA1, CHA1/, CHB1, CHC1, etc.) belong to encoder #1. If the PMAC is not plugged into a bus and drawing +5V and GND from the bus, use these pins to bring in +5V and GND from the power supply. Connect the A and B (quadrature) encoder channels to the appropriate terminal block pins. For encoder 1, the CHA1 is pin 25 and CHB1 is pin 21.

Note:

The encoder number does not have to match the motor number, but usually does.

If it is a single-ended signal, leave the complementary signal pins floating — do not ground them. However, if single-ended encoders are used, check the settings of jumpers E18 to E21 and E24 to E27. For a differential encoder, connect the complementary signal lines — CHA1/ is pin 27, and CHB1/ is pin 23. The third channel (index pulse) is optional; for encoder 1, CHC1 is pin 17, and CHC1/ is pin 19.

Example: differential quadrature encoder connected to channel #1:

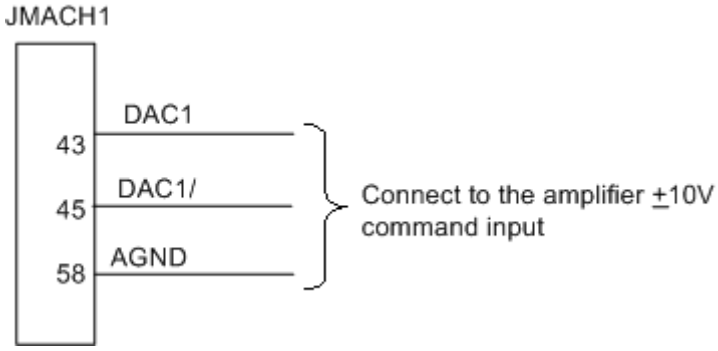
DAC Output Signals

If PMAC is not performing the commutation for the motor, only one analog output channel is required to command the motor. This output channel can be either single-ended or differential, depending on what the amplifier is expecting. For a single-ended command using PMAC channel 1, connect DAC1 (pin 43) to the command input on the amplifier. Connect the amplifier's command signal return line to PMAC's AGND line (pin 58). In this setup, leave the DAC1/ pin floating; do not ground it.

For a differential command using PMAC channel 1, connect DAC1 (pin 43) to the plus command input on the amplifier. Connect DAC1/ (pin 45) to the minus-command input on the amplifier. PMAC's AGND should still be connected to the amplifier common. If the amplifier is expecting separate sign and magnitude signals, connect DAC1 (pin 43) to the magnitude input. Connect AENA1/DIR1 (pin 47) to the sign (direction input). Amplifier signal returns should be connected to AGND (pin 58). This format requires some parameter changes on PMAC. (See Ix25.) Jumper E17 controls the polarity of the direction output; this may have to be changed during the polarity test. This magnitude-and-direction mode is suited for driving servo amplifiers that expect this type of input, and for driving voltage-to-frequency (V/F) converters, such as PMAC's Acc-8D Option 2 board, for running stepper motor drivers.

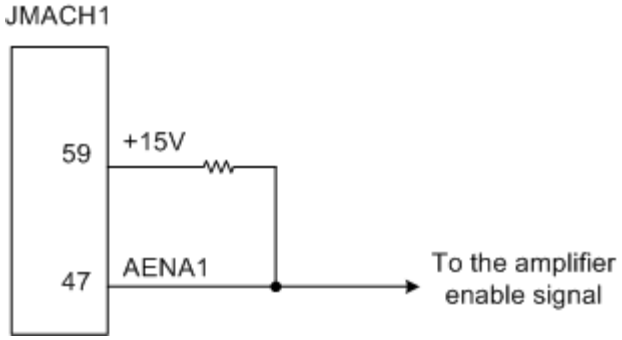
If using PMAC to commutate the motor, use two analog output channels for the motor. Each output may be single-ended or differential, just as for the DC motor. The two channels must be consecutively numbered, with the lower-numbered channel having an odd number (e.g., use DAC1 and DAC2 for a motor, or DAC3 and DAC4, but not DAC2 and DAC3, or DAC2 and DAC4). For the motor #1 example, connect DAC1 (pin 43) and DAC2 (pin 45) to the analog inputs of the amplifier. If using the complements as well, connect DAC1/ (pin 45) and DAC2/ (pin 46) the minus-command inputs; otherwise leave the complementary signal outputs floating. If the range of each signal to +/- 5V needs to be limited, do so with parameter Ix69. Any analog output not used for dedicated servo purposes may be utilized as a general-purpose analog output. Usually, this is done by defining an M-variable to the digital-to-analog-converter register (suggested M-variable definitions M102, M202, etc.) and then writing values to the M-variable. The analog outputs are intended to drive high-impedance inputs with no significant current draw. The 220Ω output resistors will keep the current draw lower than 50 mA in all cases and prevent damage to the output circuitry. But any current draw above 10 mA can result in noticeable signal distortion.

Example:

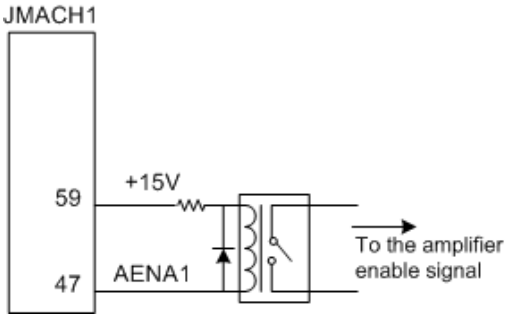


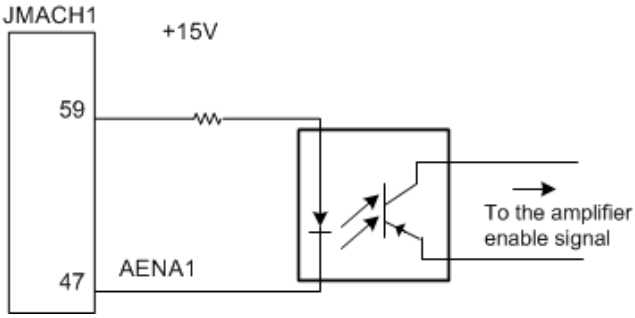
Amplifier Enable Signal (AENAx/DIRn)

Most amplifiers have an enable/disable input that permits complete shutdown of the amplifier, regardless of the voltage of the command signal. PMAC's AENA line is meant for this purpose. If not using a direction and magnitude amplifier or voltage-to-frequency converter, use this pin to enable and disable the amplifier (wired to the enable line). AENA1/DIR1 is pin 47. This signal is an open-collector output and requires a pull up resistor to A+15V. For early tests, it is better to have this amplifier signal under manual control.



The polarity of the signal is controlled by jumper E17. The default is low-true (conducting) enable. For any other kind of amplifier enable signal (i.e., 24V signal), a dry contact of a relay or a solid-state relay could be used:

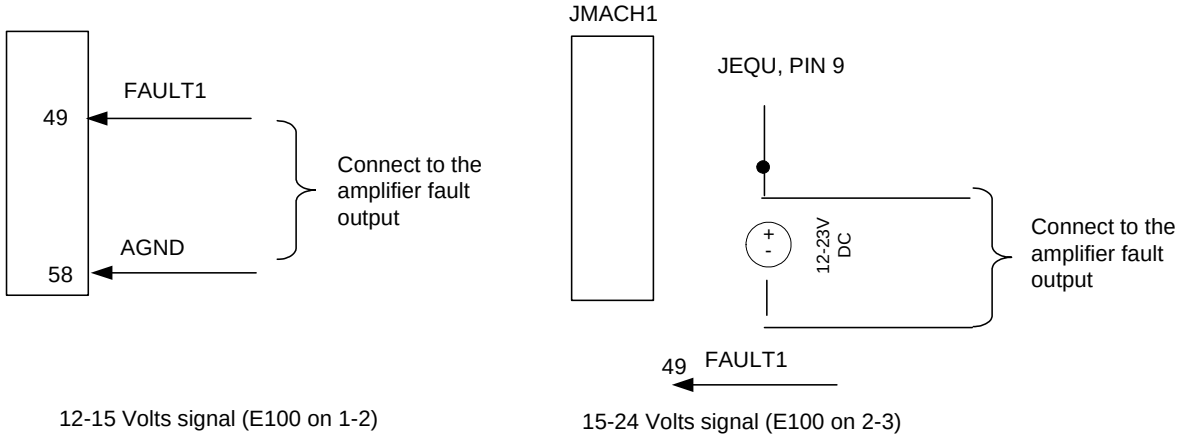




The amplifier enable signal could also be controlled manually by setting Ix00=0 and using the properly defined Mx14 variable.

Amplifier Fault Signal (FAULTn)

This input can take a signal from the amplifier when it is having problems, notify PMAC and shut down action. The polarity is programmable with I-variable Ix25 (I125 for motor #1) and the return signal is analog ground (AGND). FAULT1 is pin 49. With the default setup, this signal must actively be pulled low for a fault condition. In this setup, if nothing is wired into this input, PMAC will consider the motor not to be in a fault condition. The amplifier fault signal could be monitored using the properly defined Mx23 variable.



Jumper E89 and E90

Set these jumpers appropriately for the type of signal used. Some amplifiers share the amplifier fault output with the amplifier enable\disable status output. In this case, a special PLC code must be written with the following sequence: disable the amplifier fault input (see Ix25), enable the motor (J/ command), wait for the amplifier fault input to be false (monitor Mx23), re-enable the amplifier fault input (see Ix25).

General-Purpose Digital Inputs and Outputs (JOPTO Port)

PMAC's J5 or JOPTO connector provides eight general-purpose digital inputs and eight general-purpose digital outputs. Each input and each output has its own corresponding ground pin in the opposite row. The 34-pin connector was designed for easy interface to OPTO-22 or equivalent optically isolated I/O modules. Delta Tau's Acc-21F is a six-foot cable for this purpose. Characteristics of the JOPTO port on the PMAC PC are:

- 16 I/O points. 100 mA per channel, up to 24V.
- Hardware selectable between sinking and sourcing in groups of eight; default is all sinking (inputs can be changed simply by moving a jumper; sourcing outputs must be special-ordered or field-configured.)
- Eight inputs, eight outputs only; no changes. Parallel (fast) communications to PMAC CPU.
- Not OPTO-isolated; easily connected to OPTO-22 (PB16) or similar modules through Acc-21F cable.

Jumper E7 controls the configuration of the eight inputs. If it connects pins 1 and 2 (the default setting), the inputs are biased to +5V for the off state, and they must be pulled low for the on state. If E7 connects pins 2 and 3, the inputs are biased to ground for the off state, and must be pulled high for the on state. In either case, a high voltage is interpreted as a '0' by the PMAC software, and a low voltage is interpreted as a 1.

CAUTION:

Do not connect these outputs directly to the supply voltage, or damage to the PMAC will result from excessive current draw.

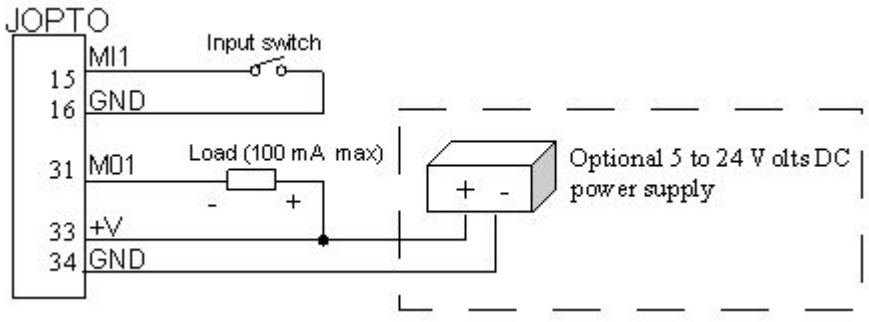
PMAC is shipped standard with a ULN2803A sinking (open-collector) output IC for the eight outputs. These outputs can sink up to 100 mA, but must have a pull-up resistor to go high.

CAUTION:

Having Jumpers E1 and E2 set wrong can damage the IC.

A high-side voltage (+5 to +24V) can be provided into Pin 33 of the JOPTO connector, allowing it to pull up the outputs by connecting pins 1 and 2 of Jumper E1. Jumper E2 must connect also pins 1 and 2 for a ULN2803A sinking output. It is possible for these outputs to be sourcing drivers by substituting a UDN2981A IC for the ULN2803A. This U3 IC is socketed, and so may be replaced easily. For this driver, pull-down resistors should be used. With a UDN2981A driver IC, Jumper E1 must connect pins 2 and 3, and Jumper E2 must connect pins 2 and 3.

Example: Standard configuration using the ULN2803A sinking (open-collector) output IC.



Control-Panel Port I/O (JPAN Port)

The J2 or JPAN connector is a 26-pin connector with dedicated control inputs, dedicated indicator outputs, a quadrature encoder input, and an analog input. The control inputs are low-true with internal pull-up resistors. They have predefined functions unless the control-panel-disable I-variable (I2) has been set to 1. If this is the case, they may be used as general-purpose inputs by assigning M-variables to their corresponding memory-map locations (bits of Y address $FFC0). There are five dedicated low-true outputs on the JPAN connector, usually used to light LEDs. They are BRLD/ (buffer-request LED), IPLD/ (in-position LED), EROR/ (Error condition LED), F1LD/ (1st—warning—following error LED), and F2LD/ (which goes true when the Watchdog timer trips). If I2=0, they refer to the panel-selected coordinate system (by FDPn/). If I2=1, they refer to the host-selected coordinate system (&n). If I2=0, but no coordinate system is selected (all FPDn/ inputs are floating or pulled high), these lines can be used as general purpose outputs, addressed as bits 20-23 of Y:$FFC2.

Thumbwheel Multiplexer Port (JTHW Port)

The Thumbwheel Multiplexer Port, or Multiplexer Port, on the JTHW (J3) connector has eight input lines and eight output lines. The output lines can be used to multiplex large numbers of inputs and outputs on the port, and Delta Tau provides accessory boards and software structures (special M-variable definitions) to capitalize on this feature. Up to 32 of the multiplexed I/O boards may be daisy-chained on the port, in any combination.

The Acc-18 Thumbwheel Multiplexer board provides up to sixteen BCD thumbwheel digits or 64 discrete TTL inputs per board. The TWD and TWB forms of M-variables are used for this board. The Acc-34x family Serial I/O Multiplexer boards provides 64 I/O points per board, optically isolated from PMAC. The TWS form of M-variables is used for these boards. The Acc-8D Option 7 Resolver-to-Digital Converter board provides up to four resolver channels whose absolute positions can be read through the thumbwheel port. The TWR form of M-variables is used for this board. The Acc-8D Option 9 Yaskawa™ Absolute Encoder Interface board can connect to up to four of these encoders. The absolute position is read serially through the multiplexer port on power up.

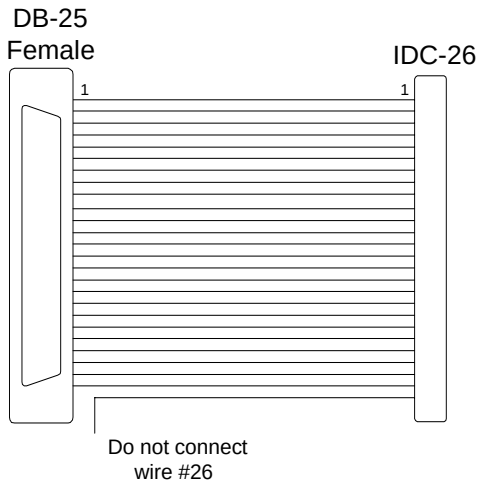
If these accessory boards are not used, the inputs and outputs on this port may be used as discrete, non-multiplexed I/O. They map into PMAC's processor space at Y address $FFC1. The suggested M-variable definitions for this use are M40 to M47 for the eight outputs, and M50 to M57 for the eight inputs. The Acc-27 Optically Isolated I/O board buffers the I/O in this non-multiplexed form, with each point rated to 24V and 100 mA.

Serial Connections

For serial communications, use a serial cable to connect the PC's COM port to the PMAC's J4 serial port connector. Delta Tau provides the Acc-3D cable for this purpose which connects the PMAC PC to a DB-25 connector. Standard DB-9-to-DB-25 or DB-25-to-DB-9 adapters may be needed for a particular setup.

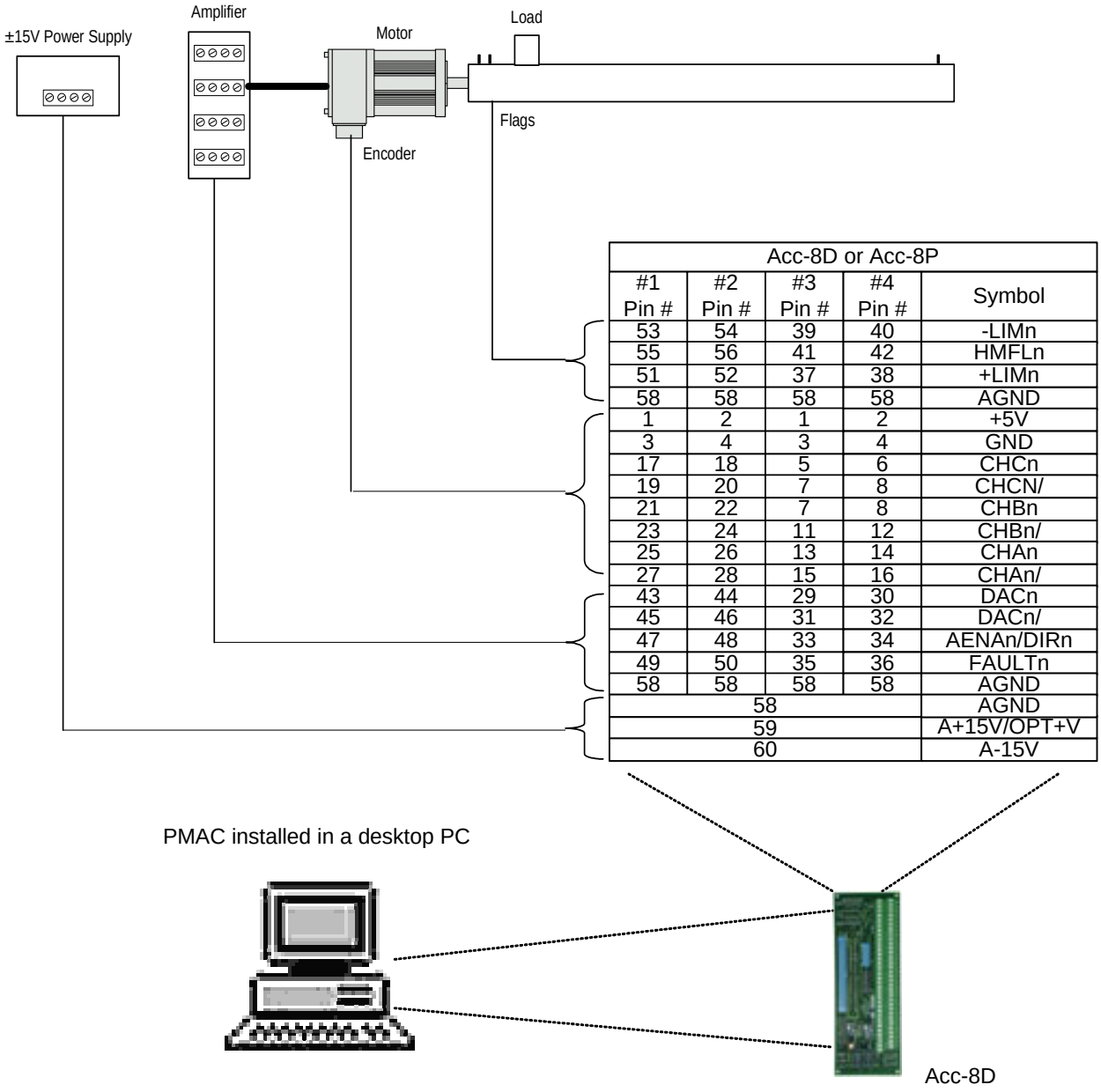
If using the Acc-26 Serial Communications converter, connect from the PC COM port to Acc-26 with a standard DB-9 or DB-25 cable, and from Acc-26 to PMAC using the cable provided with Acc-26. Since the serial ports on PMAC PC are RS-422, this accessory can be useful to provide the level conversion between RS-232 and RS-422. (Communication is possible without this conversion, but at reduced noise margin.) Because the conversion is optically isolated, the accessory also helps prevent noise and ground loop problems.

When a cable must be made, the easiest approach is to use a flat cable prepared with flat-cable type connectors as indicated in the following diagram:



PMAC (IDC-26)	PC (DB-25)
1	1
2	14
3	2 (TXD)
4	15
5	3 (RXD)
6	16
7	4 (RTS)
8	17
9	5 (CTS)
10	18
11	6 (DSR)
12	19
13	7 (Gnd)
14	20 (DTR)
15	8
16	21
17	9
18	22
19	10
20	23
21	11
22	24
23	12
24	25
25	13
26	No connect

Machine Connections Example



Acc-8D or Acc-8P				
#1 Pin #	#2 Pin #	#3 Pin #	#4 Pin #	Symbol
53	54	39	40	-LIMn
55	56	41	42	HMFLn
51	52	37	38	+LIMn
58	58	58	58	AGND
1	2	1	2	+5V
3	4	3	4	GND
17	18	5	6	CHCn
19	20	7	8	CHCN/
21	22	7	8	CHBn
23	24	11	12	CHBn/
25	26	13	14	CHAn
27	28	15	16	CHAn/
43	44	29	30	DACn
45	46	31	32	DACn/
47	48	33	34	AENAn/DIRn
49	50	35	36	FAULTn
58	58	58	58	AGND
58				AGND
59				A+15V/OPT+V
60				A-15V

Note: For this configuration, jumpers E85, E87, E89, E90 and E100 are left at the default settings.

HOST PC-AT I/O ADDRESS MAP

Hex Range	Dec Range	Usage
000-01F	0-31	DMA controller 1 8237A-5
020-03F	32-63	Interrupt controller 1 8259A
040-05F	64-67	Timer 8254-2
060-06F	96-111	8042 (keyboard)
070-07F	112-127	Real-time clock, NMI mask
080-09F	128-159	DMA page registers
0A0-0BF	160-191	Interrupt Controller 2 8259A
0C0-0DF	192-223	DMA Controller 2 8237A-5
0F0-0FF	240-255	Math CO processor
1F0-1F8	496-504	Fixed disk
200-20F	512-527	Game control
210-217	528-535	Expansion unit (usually open)
278-27F	632-639	Parallel printer: LPT2
2B0-2DF	688-735	Alternate EGA
2F8-2FF	760-767	Asynchronous common: COM2
300-31F	768-799	Prototype card (usually open)
360-36F	864-879	PC network
378-37F	888-895	Parallel Printer: LPT1
380-38F	896-911	SDLC Communications 2
390-393	912-915	Cluster
3A0-3A9	928-937	SDLC Communications 1
3B0-3BF	944-959	IBM Monochrome Display/Printer
3C0-3CF	960-975	Enhanced graphics adapter
3D0-3DF	976-991	Color/Graphics
3F0-3F7	1000-1015	Diskette controller
3F8-3FF	1016-1023	Asynchronous common.: COM1
x2E1		GPIB adapter
x390-x393		Cluster adapter

Note:
This chart shows possible contention with existing I/O. If a contention occurs, try a new unused address.
Contention is exhibited by:

- Total malfunction.
- Partial function, input OK, output bad or vice versa.
- Intermittent operation.

PMAC PC MATING CONNECTORS

This section lists several options for each connector. Choose an appropriate one for your application. (See attached PMAC mating connector sketch for typical connection)

Base Board Connectors

J1 (JDISP)/Display

- Two 14-pin female flat cable connector Delta Tau P/N 014-R00F14-0K0 T&B Ansley P/N 609-1441
- 171-14 T&B Ansley standard flat cable-stranded 14-wire
- Phoenix varioface modules type FLKM14 (male pins) P/N 22 81 02 1

J2 (JPAN)/Control Panel

- Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 T&B Ansley P/N 609-2641
- 171.26.T&B Ansley standard flat cable stranded 26-wire
- Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J3 (JTHW)/Multiplexer Port

- Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 T&B Ansley P/N 609-2641
- 171-26 T&B Ansley standard flat cable stranded 26-wire
- Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J4 (JRS422)/RS232 OR 422/Serial Communications

- Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 T&B Ansley P/N 609-2641
- 171-26 T&B Ansley standard flat cable stranded 26-wire
- Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J5 (JOPT)/OPTO I/O

- Two 34-pin female flat cable connector Delta Tau P/N 014-R00F34-0k0 T&B Ansley P/N 609-3441
- 171-34 T&B Ansley standard flat cable stranded 34-wire
- Phoenix varioface module type FLKM 34 (male pins) P/N 22 81 06 3

J6 (JXIO)/Expansion Board

- Two 10-pin female flat cable connector Delta Tau P/N 014-R00F10-0K0 T&B Ansley P/N 609-1041
- 171-10 T&B Ansley standard flat cable stranded 10-wire
- Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

J7 (JMACH2)/2nd Machine Connector (Option 1 Required)

- Two 60-pin female flat cable connector Delta Tau P/N 014-R00F60-0K0 T&B Ansley P/N 609-6041 available as ACC 8P or 8D
- 171-60 T&B Ansley standard flat cable stranded 60-wire
- Phoenix varioface module type FLKM 60 (male pins) P/N 22 81 09 2

> ***Note:***
>
> Normally, J7 and J8 are used with accessory 8P or 8D with Option P, which provides complete terminal strip fan-out of all connections.

J8 (JMACH1)/1st Machine Connector

- Two 60-pin female flat cable connector Delta Tau P/N 014-R00F60-0K0 T&B Ansley P/N 609-6041 available as ACC 8P or 8D
- 171-60 T&B Ansley standard flat cable stranded 60-wire
- Phoenix Varioface module type FLKM 60 (male pins) P/N 22 81 09 2

Note:

Normally, J7 and J8 are used with Acc-8P or 8D with Option P, which provides complete terminal strip fan-out of all connections.

JS1/A-D Inputs 1-4

- Two 16-pin female flat cable connector Delta Tau P/N 014-R00F16-0K0 T&B Ansley P/N 609-1641
- 171-16 T&B Ansley standard flat cable stranded 16-wire
- Phoenix varioface module type FLKM 16 (male pins) P/N 22 81 03 4

JS2/A-D InputS 5-8 (Option 1 Required)

- Two 16-pin female flat cable connector Delta Tau P/N 014-R00F16-0K0 T&B Ansley P/N 609-1641
- 171-16 T&B Ansley standard flat cable stranded 16-wire
- Phoenix varioface module type FLKM 16 (male pins) P/N 22 81 03 4

JEQU (Jumpers E53-E65)/Position Compare

- Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 T&B Ansley P/N 609-2641
- 171-26 T&B Ansley standard flat cable stranded 26-wire
- Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

P1 (PC BUS)

- One 62-pin card edge connector with solder pierced eyelets Delta Tau P/N 014-000F62-SCO Viking P/N 3KH 31/9 JN12 card edge connector pierced solder eyelets.

P2 (AT BUS)

- 36-pin card edge connector with solder pierced eyelets Delta Tau P/N 014-000 F36-SCO qty.1 Viking P/N 3KH 18/9 JN12 card edge connector pierced solder eyelets.

CPU Board Connectors

J2 (JEXP)/Expansion

- Two 50-pin female flat cable connector Delta Tau P/N 014-R00F50-0K0 T&B Ansley P/N 609-5041
- 171-50 T&B Ansley standard flat cable stranded 50-wire
- Phoenix varioface module type FLKM 50 (male pins) P/N 22 81 08 9 used for daisy chaining acc-14 I/0, -23 A and D connectors -24 expansion

J4 (JDPRAM)/Dual Ported Ram

- Two 10-pin female flat cable connector Delta Tau P/N 014-ROOF10-0K0 T&B Ansley P/N 609-1041
- 171-10 T&B Ansley standard flat cable stranded 10-wire
- Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

PMAC PC CPU BOARD CONNECTORS DESCRIPTION

J1: 36-pin header on backside for connection to main PMAC board

J2 (JEXP): 50-pin IDC header for connection to expansion port accessory boards

J3: 36-pin header on backside for connection to main PMAC board

J4 (JEXP): 10-pin IDC header for connection to DPRAM on accessory board

J5 (JTAG/OnCE): 10-pin header for factory use only

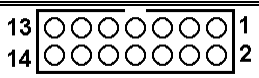
J6: 8-pin SIP header for factory use only

J7: 8-pin SIP header for factory use only

PMAC PC BASE BOARD CONNECTOR PINOUTS

J1: Display Port Connector

J1 JDISP (14-Pin Connector)



Front View

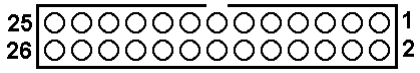
Pin #	Symbol	Function	Description	Notes
1	VDD	Output	+5V Power	Power supply out
2	VSS	Common	PMAC Common	
3	RS	Output	Read Strobe	TTL signal out
4	VEE	Output	Contrast Adjust. VEE	0 to +5 VDC *
5	E	Output	Display Enable	High is enable
6	R/W	Output	Read Or Write	TTL signal out
7	DB1	Output	Display Data1	
8	DB0	Output	Display Data0	
9	DB3	Output	Display Data3	
10	DB2	Output	Display Data2	
11	DB5	Output	Display Data5	
12	DB4	Output	Display Data4	
13	DB7	Output	Display Data7	
14	DB6	Output	Display Data6	

The JDISP connector is used to drive the 2-line x 24-character (Acc-12), 2 x 40 (Acc-12A) LCD, or the 2 x 40 vacuum fluorescent (Acc 12C) display unit. The **DISPLAY** command may be used to send messages and values to the display. Controlled by potentiometer R1.

See Also:
Program Commands: Display
Accessories: Acc-12, 12A, 12C, ACC16D
Memory Map: Y:$0780 - $07D1

J2: Control Panel Port Connector

J2 JPAN (26-Pin Connector)



Front View

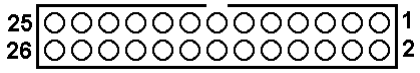
Pin #	Symbol	Function	Description	Notes
1	+5V	Output	+5V Power	For remote panel
2	GND	Common	PMAC Common	
3	FPD0/	Input	Motor/C.S. Select Bit 0	Low is true
4	JOG-/	Input	Jog In - Dir.	Low is jog -
5	FPD1/	Input	Motor/C.S. Select Bit 1	Low is true
6	JOG+/	Input	Jog In + Dir.	Low is jog +
7	PREJ/	Input	Ret. To Prejog Position	Low is return equiv to J= CMD
8	STRT/	*Input*	Start Program Run	Low is start equiv to R CMD
9	STEP/	Input	Step Through Program	Low is step equiv to S or Q
10	STOP/	Input	Stop Program Run	Low is stop equiv to A
11	HOME/	Input	Home Search Command	Low is Go Home equiv to HM
12	HOLD/	Input	Hold Motion	Low is hold equiv to H
13	FPD2/	Input	Motor/C.S. Select Bit 2	Low is true
14	FPD3/	Input	Motor/C.S. Select Bit 3	Low is true
15	INIT/	Input	Reset PMAC	Low is reset equiv to $$$
16	HWCA	Input	Handwheel Enc. A Channel	5v TTL sq. pulse must use E23 (Cha2)
17	IPLD/	Output	In Position Ind. (C.S.)	Low lights LED
18	BRLD/	Output	Buffer Request Ind.	Low lights LED
19	ERLD/	Output	Fatal Follow Err (C.S.)	Low lights LED
20	WIPER	Input	Feed Pot Wiper	0 to +10V input must use E72, E73 (Cha4)
21	(SPARE)	N.C.		
22	HWCB	Input	Handwheel Enc. B Channel	5v TTL sq. pulse must use E22 (Chb2)
23	F1LD/	Output	Warn Follow Err (C.S.)	Low lights LED
24	F2LD/	Output	Watchdog Timer	Low lights LED
25	+5V	Output	+5V Power	For remote panel
26	GND	Common	PMAC Common	

The JPAN connector can be used to connect the Accessory 16 (Control Panel), or customer-provided I/O, to the PMAC, providing manual control of PMAC functions via simple toggle switches. If the automatic control panel input functions are disabled (I2=1), the inputs become general-purpose TTL inputs, and the coordinate system (C.S.) specific outputs pertain to the *host*-addressed coordinate system.

See Also:
Control panel inputs
Accessories: Acc-16, Acc-39
I-variables: I2, Ix06.
I/O and Memory Map Y:$FFC0.
Suggested M-variables M20 - M32

J3: Multiplexer Port Connector

J3 JTHW (26-Pin Connector)



Front View

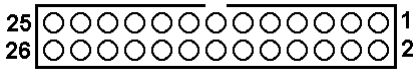
Pin #	Symbol	Function	Description	Notes
1	GND	Common	PMAC Common	
2	*GND*	Common	PMAC Common	
3	DAT0	Input	Data-0 Input	Data input from multiplexed accessory
4	SEL0	Output	Select-0 Output	Multiplexer select output
5	DAT1	Input	Data-1 Input	Data input from multiplexed accessory
6	SEL1	Output	Select-1 Output	Multiplexer select output
7	DAT2	Input	Data-2 Input	Data input from multiplexed accessory
8	SEL2	Output	Select-2 Output	Multiplexer select output
9	DAT3	Input	Data-3 Input	Data Input from multiplexed accessory
10	SEL3	Output	Select-3 Output	Multiplexer select output
11	DAT4	Input	Data-4 Input	Data input from multiplexed accessory
12	SEL4	Output	Select-4 Output	Multiplexer select output
13	DAT5	Input	Data-5 Input	Data input from multiplexed accessory
14	SEL5	Output	Select-5 Output	Multiplexer select output
15	DAT6	Input	Data-6 Input	Data input from multiplexed accessory
16	SEL6	Output	Select-6 Output	Multiplexer select output
17	DAT7	Input	Data-7 Input	Data input from multiplexed accessory
18	SEL7	Output	Select-7 Output	Multiplexer select output
19	N.C.	N.C.	No Connection	
20	GND	Common	PMAC Common	
21	BRLD/	Output	Buffer Request	Low is buffer req.
22	GND	Common	PMAC Common	
23	IPLD/	Output	In Position	Low is in position
24	GND	Common	PMAC Common	
25	+5V	Output	+5VDC Supply	Power supply out
26	INIT/	Input	PMAC Reset	Low is reset

The JTHW multiplexer port provides eight inputs and eight outputs at TTL levels. While these I/O can be used in unmultiplexed form for sixteen discrete I/O points, most users will utilize PMAC software and accessories to use this port in multiplexed form to greatly multiply the number of I/O that can be accessed on this port. In multiplexed form, some of the SELn outputs are used to select which of the multiplexed I/O are to be accessed.

See also:
I/O and Memory Map Y:$FFC1
Suggested M-variables M40 - M58
M-variable formats TWB, TWD, TWR, TWS
Acc-8D Opt 7, Acc-8D Opt 9, Acc-18, Acc-34x, NC Control Panel

J4: Serial Port Connector

J4 JRS422 (26-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	CHASSI	Common	PMAC Common	
2	S+5V	Output	+5VDC Supply	Deactivated by E8
3	RD-	Input	Receive Data	Diff. I/O low true **
4	RD+	Input	Receive Data	Diff. I/O high true *
5	SD-	Output	Send Data	Diff. I/O low true **
6	SD+	Output	Send Data	Diff. I/O high true *
7	CS+	Input	Clear To Send	Diff. I/O high true **
8	CS-	Input	Clear To Send	Diff. I/O low true *
9	RS+	Output	Req. To Send	Diff. I/O high true **
10	RS-	Output	Req. To Send	Diff. I/O low true *
11	DTR	Bidirect	Data Term Read	Tied to DSR
12	INIT/	Input	PMAC Reset	Low is reset
13	GND	Common	PMAC Common	**
14	DSR	Bidirect	Data Set Ready	Tied to DTR
15	SDIO-	Bidirect	Special Data	Diff. I/O low true
16	SDIO+	Bidirect	Special Data	Diff. I/O high true
17	SCIO-	Bidirect	Special Ctrl.	Diff. I/O low true
18	SCIO+	Bidirect	Special Ctrl.	Diff. I/O high true
19	SCK-	Bidirect	Special Clock	Diff. I/O low true
20	SCK+	Bidirect	Special Clock	Diff. I/O high true
21	SERVO-	Bidirect	Servo Clock	Diff. I/O low true ***
22	SERVO+	Bidirect	Servo Clock	Diff. I/O high true ***
23	PHASE-	Bidirect	Phase Clock	Diff. I/O low true ***
24	PHASE+	Bidirect	Phase Clock	Diff. I/O high true ***
25	GND	Common	PMAC Common	
26	+5V	Output	+5VDC Supply	Power supply out

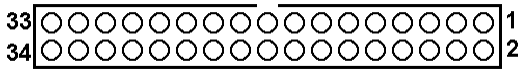
* Note: Required for communications to an RS-422 host port
** Note: Required for communications to an RS-422 or RS-232 host port
*** Note: Output on card @0; input on other cards. These pins are for synchronizing multiple PMACs together by sharing their phasing and servo clocks. The PMAC designated as card 0 (@0) by its jumpers E40-E43 outputs its clock signals. Other PMACs designated as cards 1-15 (@1-@F) by their jumpers E40-E43 take these signals as inputs. If synchronization is desired, these lines should be connected even if serial communications is not used.

The JRS422 connector provides the PMAC with the ability to communicate both in RS422 and RS232. In addition, this connector is used to daisy chain interconnect multiple PMACs for synchronized operation.

See Also:
Serial Communications
Synchronizing PMAC to other PMACs

J5: I/O Port Connector

J5 JOPT (34-Pin Connector)



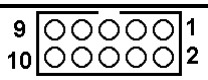
Front View

Pin #	Symbol	Function	Description	Notes
1	*MI8*	Input	Machine Input 8	Low is true
2	GND	Common	PMAC Common	
3	MI7	Input	Machine Input 7	Low is true
4	GND	Common	PMAC Common	
5	MI6	Input	Machine Input 6	Low is true
6	GND	Common	PMAC Common	
7	MI5	Input	Machine Input 5	Low is true
8	GND	Common	PMAC Common	
9	MI4	Input	Machine Input 4	Low is true
10	GND	Common	PMAC Common	
11	MI3	Input	Machine Input 3	Low is true
12	GND	Common	PMAC Common	
13	MI2	Input	Machine Input 2	Low is true
14	GND	Common	PMAC Common	
15	MI1	Input	Machine Input 1	Low is true
16	GND	Common	PMAC Common	
17	MO8	Output	Machine Output 8	Low-true (sinking); High-true (sourcing)
18	GND	Common	PMAC Common	
19	MO7	Output	Machine Output 7	“ ”
20	GND	Common	PMAC Common	
21	MO6	Output	Machine Output 6	“ ”
22	GND	Common	PMAC Common	
23	MO5	Output	Machine Output 5	“ ”
24	GND	Common	PMAC Common	
25	MO4	Output	Machine Output 4	“ ”
26	GND	Common	PMAC Common	
27	MO3	Output	Machine Output 3	“ ”
28	GND	Common	PMAC Common	
29	MO2	Output	Machine Output 2	“ ”
30	GND	Common	PMAC Common	
31	MO1	Output	Machine Output 1	“ ”
32	GND	Common	PMAC Common	
33	+V	Input/ Output	+V Power I/O	+V = +5v to +24v +5v out from PMAC, +5 to +24v in from external source, diode isolation from PMAC
34	GND	Common	PMAC Common	

This connector provides means for eight general-purpose inputs and eight general-purpose outputs. Inputs and outputs may be configured to accept or provide either +5 volt or +24 volt signals. Outputs can be made sourcing with an IC (U11 to UDN2981) and jumper (E1 and E2) change. E7 controls whether the inputs are pulled up or down internally. Outputs are rated at 100mA per channel.

J6: Auxiliary I/O Port Connector

J6 JXIO (10-Pin Connector)



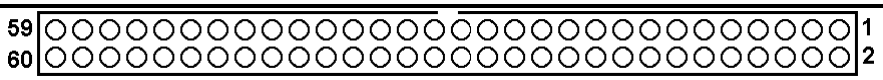
Front View

Pin #	Symbol	Function	Description	Notes
1	CHA1	Input	Encoder A Ch. Pos.	Axis #1 for resolver
2	CHB1	Input	Encoder B Ch. Pos.	Axis #1 for resolver
3	CHC1	Input	Encoder C Ch. Pos.	Axis #1 for resolver
4	CHA3	Input	Encoder A Ch. Pos.	Axis #3 for resolver
5	CHB3	Input	Encoder B Ch. Pos.	Axis #3 for resolver
6	CHC3	Input	Encoder C Ch. Pos.	Axis #3 for resolver
7	E63	Input	Interrupt Ir4	Interrupt from exp brd
8	E59	Input	Interrupt Ir5	Interrupt from exp brd
9	SCLK	Output	Encoder Clock	Encoder sample rate
10	DCLK	Output	D To A, A To D Clock	DAC and ADC clock for all channels

This connector is used for miscellaneous I/O functions related to expansion cards, which are used with PMAC.

J7: Machine Port 2 Connector

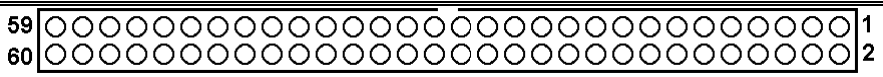
J7 JMACH2 (60-Pin Header)



Front View

Pin #	Symbol	Function	Description	Notes
1	+5V	Output	+5V Power	For encoders, 1
2	+5V	Output	+5V Power	For encoders, 1
3	GND	Common	Digital Common	
4	GND	Common	Digital Common	
5	CHC7	Input	Encoder C CH. Pos.	2
6	CHC8	Input	Encoder C CH. Pos.	2
7	CHC7/	Input	Encoder C CH. Neg.	2,3
8	CHC8/	Input	Encoder C CH. Neg.	2,3
9	CHB7	Input	Encoder B CH. Pos.	2
10	CHB8	Input	Encoder B CH. Pos.	2
11	CHB7/	Input	Encoder B CH. Neg.	2,3
12	CHB8/	Input	Encoder B CH. Neg.	2,3
13	CHA7	Input	Encoder A CH. Pos.	2
14	CHA8	Input	Encoder A CH. Pos.	2
15	CHA7/	Input	Encoder A CH. Neg.	2,3
16	CHA8/	Input	Encoder A CH. Neg.	2,3
17	CHC5	Input	Encoder C CH. Pos.	2
18	CHC6	Input	Encoder C CH. Pos.	2
19	CHC5/	Input	Encoder C CH. Neg.	2,3
20	CHC6/	Input	Encoder C CH. Neg.	2,3
21	CHB5	Input	Encoder B CH. Pos.	2
22	CHB6	Input	Encoder B CH. Pos.	2
23	CHB5/	Input	Encoder B CH. Neg.	2,3
24	CHB6/	Input	Encoder B CH. Neg.	2,3
25	CHA5	Input	Encoder A CH. Pos.	2
26	CHA6	Input	Encoder A CH. Pos.	2
27	CHA5/	Input	Encoder A CH. Neg.	2,3
28	CHA6/	Input	Encoder A CH. Neg.	2,3
29	DAC7	Output	Analog Out Pos. 7	4

J7 JMACH2 (60-Pin Header) Continued



Front View

Pin #	Symbol	Function	Description	Notes
30	DAC8	Output	Analog Out Pos. 8	4
31	DAC7/	Output	Analog Out Neg. 7	4,5
32	DAC8/	Output	Analog Out Neg. 8	4,5
33	AENA7/DIR7	Output	Amp-Ena/Dir. 7	6
34	AENA8/DIR8	Output	Amp-Ena/Dir. 8	6
35	FAULT7	Input	Amp-Fault 7	7
36	FAULT8	Input	Amp-Fault 8	7
37	+LIM7	Input	Neg End Limit 7	8,9
38	+LIM8	Input	Neg End Limit 8	8,9
39	-LIM7	Input	Pos End Limit 7	8,9
49	FAULT5	Input	Amp-Fault 5	7
50	FAULT6	Input	Amp Fault 6	7
51	+LIM5	Input	Neg End Limit 5	8,9
52	+LIM6	Input	Neg End Limit 6	8,9
53	-LIM5	Input	Pos End Limit 5	8,9
54	-LIM6	Input	Pos End Limit 6	8,9
55	HMFL5	Input	Home-Flag 5	10
56	HMFL6	Input	Home-Flag 6	10
57	ORST/	Output	Reset Signal	Indicator/Driver
58	AGND	Input	Analog Common	
59	A+15V/OPT+V	Input	Ana +15V/Flag Supply	
60	A-15V	Input	Analog –15V Supply	

Note 1: In standalone applications, these lines can be used as +5V power supply inputs to power PMAC's digital circuitry. However, if a terminal block is available on your version of PMAC, it is preferable to bring the +5V power in through the terminal block.

Note 2: Reference to digital common (GND). Maximum of ± 12V permitted between this signal and its complement.

Note 3: Leave this input floating if not used (i.e. digital single-ended encoders). In this case, jumper (E18 - 21, E24 - 27) for channel should hold input at 2.5V.

Note 4: ± 10V, 10mA max, reference to analog common (AGND).

Note 5: Leave floating if not used; do not tie to AGND. In this case, AGND is the return line.

Note 6: Functional polarity controlled by jumper(s) E17. The choice between using AENA or DIR is controlled by Ix02 and Ix25.

Note 7: Functional polarity controlled by variable Ix25. Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software. Automatic fault function can be disabled with Ix25.

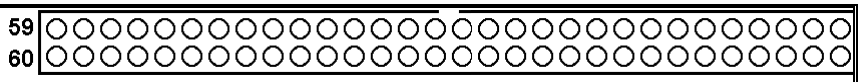
Note 8: Pins marked -LIMn should be connected to switches at the *positive* end of travel. Pins marked +LIMn should be connected to switches at the *negative* end of travel.

Note 9: Must be conducting to 0V (usually AGND) for PMAC to consider itself not into this limit. Automatic limit function can be disabled with Ix25.

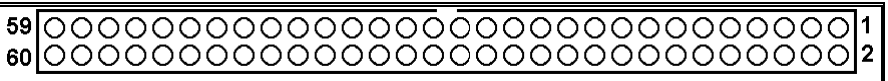
Note 10: Functional polarity for homing or other trigger use of HMFLn controlled by Encoder/Flag Variable 2 (I902, I907, etc.) HMFLn selected for trigger by Encoder/Flag Variable 3 (I903, I908, etc.). Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software.

The J7 connector is used to connect the PMAC to the second four channels (Channels 5, 6, 7, and 8) of servo amps, flags, and encoders.

J8: Machine Port 1 Connector

J8 JMACH1 (60-Pin Header)		 Front View		
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	+5V	Output	+5V Power	For encoders, 1
2	+5V	Output	+5V Power	For encoders, 1
3	GND	Common	Digital Common	
4	GND	Common	Digital Common	
5	CHC3	Input	Encoder C Channel Pos	2
6	CHC4	Input	Encoder C Channel Pos	2
7	CHC3/	Input	Encoder C Channel Neg	2,3
8	CHC4/	Input	Encoder C Channel Neg	2,3
9	CHB3	Input	Encoder B Channel Pos	2
10	CHB4	Input	Encoder B Channel. Pos	2
11	CHB3/	Input	Encoder B Channel Neg	2,3
12	CHB4/	Input	Encoder B Channel Neg	2,3
13	CHA3	Input	Encoder A Channel Pos	2
14	CHA4	Input	Encoder A Channel Pos	2
15	CHA3/	Input	Encoder A Channel Neg	2,3
16	CHA4/	Input	Encoder A Channel Neg	2,3
17	CHC1	Input	Encoder C Channel Pos	2
18	CHC2	Input	Encoder C Channel Pos	2
19	CHC1/	Input	Encoder C Channel Neg	2,3
20	CHC2/	Input	Encoder C Channel Neg	2,3
21	CHB1	Input	Encoder B Channel Pos	2
22	CHB2	Input	Encoder B Channel Pos	2
23	CHB1/	Input	Encoder B Channel Neg	2,3
24	CHB2/	Input	Encoder B Channel Neg	2,3
25	CHA1	Input	Encoder A Channel Pos	2
26	CHA2	Input	Encoder A Channel Pos	2
27	CHA1/	Input	Encoder A Channel Neg	2,3
28	CHA2/	Input	Encoder A Channel Neg	2,3
29	DAC3	Output	Analog Out Pos. 3	4
30	DAC4	Output	Analog Out Pos. 4	4
31	DAC3/	Output	Analog Out Neg. 3	4,5
32	DAC4/	Output	Analog Out Neg. 4	4,5
33	AENA3/DIR3	Output	Amp-Ena/Dir. 3	6
34	AENA4/DIR4	Output	Amp-Ena/Dir. 4	6
35	FAULT3	Input	AMP-Fault 3	7
36	FAULT4	Input	AMP-Fault 4	7
37	+LIM3	Input	Neg End Limit3	8,9
38	+LIM4	Input	Neg End Limit 4	8,9
39	-LIM3	Input	Pos End Limit 3	8,9

J8 JMACH1 (60-Pin Header) Continued



Front View

Pin #	Symbol	Function	Description	Notes
40	-LIM4	Input	Pos End Limit 4	8,9
41	HMFL3	Input	Home-Flag 3	10
42	HMFL4	Input	Home-Flag 4	10
43	DAC1	Output	Analog Out Pos. 1	4
44	DAC2	Output	Analog Out Pos. 2	4
45	DAC1/	Output	Analog Out Neg. 1	4,5
46	DAC2/	Output	Analog Out Neg. 2	4,5
47	AENA1/DIR1	Output	Amp-Ena/Dir. 1	6
48	AENA2/DIR2	Output	Amp-Ena/Dir. 2	6
49	FAULT1	Input	AMP-Fault 1	7
50	FAULT2	Input	AMP- Fault 2	7
51	+LIM1	Input	Neg End Limit 1	8,9
52	+LIM2	Input	Neg End Limit 2	8,9
53	-LIM1	Input	Pos End Limit 1	8,9
54	-LIM2	Input	Pos End Limit 2	8,9
55	HMFL1	Input	Home-Flag 1	10
56	HMFL2	Input	Home-Flag 2	10
57	FEFCO/	Output	Fe/Watchdog Out	Indicator/Driver
58	AGND	Input	Analog Common	
59	A+15V/OPT+V	Input	Analog +15V Supply	
60	A-15V	Input	Analog -15V Supply	

Note 1: In standalone applications, these lines can be used as +5V power supply inputs to power PMAC's digital circuitry. However, if a terminal block is available on your version of PMAC, it is preferable to bring the +5V power in through the terminal block.

Note 2: Reference to digital common (GND). Maximum of ± 12V permitted between this signal and its complement.

Note 3: Leave this input floating if not used (i.e. digital single-ended encoders). In this case, jumper (E18 - 21, E24 - 27) for channel should hold input at 2.5V.

Note 4: ± 10V, 10mA max, reference to analog common (AGND).

Note 5: Leave floating if not used; do not tie to AGND. In this case, AGND is the return line.

Note 6: Functional polarity controlled by jumper(s) E17. The choice between using AENA or DIR is controlled by Ix02 and Ix25.

Note 7: Functional polarity controlled by variable Ix25. Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software. Automatic fault function can be disabled with Ix25.

Note 8: Pins marked -LIMn should be connected to switches at the *positive* end of travel. Pins marked +LIMn should be connected to switches at the *negative* end of travel.

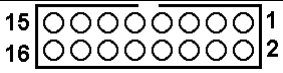
Note 9: Must be conducting to 0V (usually AGND) for PMAC to consider itself not into this limit. Automatic limit function can be disabled with Ix25.

Note 10: Functional polarity for homing or other trigger use of HMFLn controlled by Encoder/Flag Variable 2 (I902, I907, etc.) HMFLn selected for trigger by Encoder/Flag Variable 3 (I903, I908, etc.). Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software.

The J8 connector is used to connect PMAC to the first four channels (Channels 1, 2, 3, and 4) of servo amps, flags, and encoders.

JS1: A/D Port 1 Connector

JS1 (16-Pin Header)

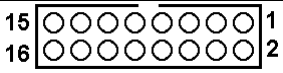


Front View

Pin #	Symbol	Function	Description	Notes
1	DCLK	Output	D To A, A To D Clock	DAC and ADC clock for Channel 1, 2, 3, 4
2	BDATA1	Output	D To A Data	DAC data for Channel 1, 2, 3, 4
3	ASEL0/	Output	CHAN Select Bit 0	Select for Channel 1, 2, 3, 4
4	ASEL1/	Output	CHAN Select Bit 1	Select for Channel 1, 2, 3, 4
5	CNVRT01	Output	A To D Convert	ADC convert SIG. Channel 1, 2, 3, 4
6	ADCIN1	Input	A To D Data	ADC data for Channel 1, 2, 3, 4
7	OUT1/	Output	AMP Enable/DIR	AMP Enable/Dir. for Channel 1
8	OUT2/	Output	AMP Enable/DIR	AMP Enable/Dir. for Channel 2
9	OUT3/	Output	AMP Enable/DIR	AMP Enable/Dir. for Channel 3
10	OUT4/	Output	AMP Enable/DIR	AMP Enable/Dir. for Channel 4
11	HF41	Input	AMP Fault	AMP fault input for Channel 1
12	HF42	Input	AMP Fault	AMP fault input for Channel 2
13	HF43	Input	AMP Fault	AMP fault input for Channel 3
14	HF44	Input	AMP Fault	AMP fault input for Channel 4
15	+5V	Output	+5V Supply	Power supply out
16	GND	Common	PMAC Common	
Acc-28A/B connection; digital amplifier connection.				

JS2: A/D Port 2 Connector

JS2 (16-Pin Header)



Front View

Pin #	Symbol	Function	Description	Notes
1	DCLK	Output	D to A, A to D clock	DAC and ADC clock for Channel 5, 6, 7, 8
2	BDATA2	Output	D to A data	DAC data for Channel 5, 6, 7, 8
3	ASEL2/	Output	CHAN select bit 2	Select for Channel 5, 6, 7, 8
4	ASEL3/	*Output*	CHAN select bit 3	Select for Channel 5, 6, 7, 8
5	CNVRT23	Output	A to D convert	ADC convert SIG. Channel 5, 6, 7, 8
6	ADCIN2	Input	A to D data	ADC data for Channel 5, 6, 7, 8
7	OUT5/	Output	AMP enable/dir	AMP enable/dir. for Channel 5
8	OUT6/	Output	AMP enable/dir	AMP enable/dir. for Channel 6
9	OUT7/	Output	AMP enable/dir	AMP enable/dir. for Channel 7
10	OUT8/	Output	AMP enable/dir	AMP enable/dir. for Channel 8
11	HF45	Input	AMP fault	AMP fault input for Channel 5
12	HF46	Input	AMP fault	AMP fault input for Channel 6
13	HF47	Input	AMP fault	AMP fault input for Channel 7
14	HF48	Input	AMP fault	AMP fault input for Channel 8
15	+5V	Output	+5V supply	Power supply out
16	GND	Common	PMAC common	
Acc-28A/B connection; digital amplifier connection.				

PMAC PC SOFTWARE SETUP

PMAC has a large set of Initialization parameters (I-variables) that determine the personality of the card for a specific application. Many of these are used to configure a motor. Once set up, these variables may be stored in non-volatile EAROM memory (using the **SAVE** command) so the card is always configured properly (PMAC loads the EAROM I-variable values into RAM on power-up).

The easiest way to program, setup and troubleshoot PMAC is by using the PMAC Executive Program, PEWIN, and its related add-on packages P1Setup and PMACPlot. These software packages are available from Delta Tau, ordered through the Acc-9WN accessory.

The programming features and configuration variables for the PMAC PC are fully described in the PMAC User and Software manuals.

Configuring PMAC with Option-5C for 80 MHz Operation

On a PMAC with flash-backed main memory, jumper E48 controls the frequency of operation of the DSP. It can only directly set 40 MHz and 60 MHz DSP operation. On power-up/reset, the DSP, operating at the crystal frequency of 20 MHz, reads the frequency jumper E48 and writes into its own PLL multiplier register at X:$FFFD. Bits 0-3 of this word contain a value one less than the multiplier value (if the frequency is being multiplied by 3, these bits contain a value of 2).

To check the value of the multiplier, use the on-line command RHX:$FFFD and look at the last hexadecimal digit. The actual multiplier is one greater than the value in this last digit. Alternately, define an M-variable such as M99->X:$FFFD,0,4 and then read from or write to these bits with the M-variable.

E48	X:$FFFD; 0-3	True Multiplier	DSP Frequency
OFF	1	X2	40 MHz
ON	2	X3	60 MHz

When PMAC is ordered with the CPU Option 5C, it can run at 80 MHz frequency. To operate the CPU at 80 MHz, set the multiplier value in the user software. In this case, usually E48 will be set to off, so the CPU comes up at 40 MHz. The usual way to set the multiplier value for 80 MHz is to use a reset PLC, one that executes automatically on power-up/reset, then disables itself. Typically, this is PLC 1, the first to execute after power-up/reset (see below).

If using serial communications on an 80 MHz PMAC, the baud rate divider register in the CPU also needs to be changed. On power-up/reset, the firmware reads jumpers E44-E47 and sets the baud rate divider register in the CPU (at X:$FFF2 bits 0 to 11) to set the serial baud rate. Since the baud rate clock is derived from the CPU frequency, a change in the CPU frequency will change the baud rate.

To counteract this change, when changing the CPU frequency, change the baud rate divider register in the CPU. If the CPU frequency is doubled, also double the divider value and add 1. This should also be done in the reset PLC.

This operation can be done with the following code segment. This baud divider algorithm is valid only if the PMAC has been jumpered for 40 MHz operation (E48 OFF).

```
M98->X:$FFF2,0,12
M99->X:$FFFD,0,4
OPEN PLC 1 CLEAR
M99=3                   ; Set x4 frequency multiplication (80 MHz)
M98=2*M98+1             ; Increase baud divider to maintain rate
                        ; (Only needed for serial communications)
...                     ; More of reset PLC
DISABLE PLC 1           ; So PLC 1 will not repeat
CLOSE
```

To make the change in CPU frequency and baud rate over the serial port with on-line commands, make sure that the two commands are on the same command line. If they are on separate command lines, the second command will not be accepted because the baud rate has changed. For example, with the same setup as the above example, use the command line:

```
M99=3 M98=2*M98+1
```

to change the CPU frequency and baud rate divider (to keep the baud rate constant) together.

Option 16 Supplemental Memory

If Option 16 (Supplemental Battery-Backed Parameter Memory) is ordered, an extra bank of memory with battery backup circuitry is provided. This option can be ordered only if the main memory is flash backed (Option 4A, 5A, 5B, or 5C). This memory is for user parameter storage only. From PMAC programs it can be accessed with M-variables only (L-variables also in compiled PLCs). The on-line direct-memory read and write commands can be used from the host computer as well.

With M-variable access, arrays can be created with indirect addressing techniques by pointing a second M-variable to the definition of a first M-variable that points into this memory area. For example, with the M-variable definitions:

```
M0->L:$A000                    ; 1st long word of Opt. 16 RAM floating point
M10->Y:$BC000,0,16             ; Low 16 bits of M0 def., with pointer address
```

The following code segment could load a sine table into the first 360 words of the Option 16 RAM:

```
P1=0
WHILE (P1<360)
     M10=$A000+P1              ; Sets address that M0 points to
     M0=SIN(P1)                ; Puts value in register that M0 points to P1=P1+1
ENDWHILE
```

Note:

This technique is not possible with L-variables in compiled PLCs, but it is possible with M-variables in compiled PLCs.

Physically, the Option 16 memory is a 16k x 24 bank of battery-backed static RAM. It maps into the PMAC and PMAC2 at addresses $A000 to $BFFF, on both the X and Y data buses, an 8k x 48 block of address space. Addresses Y:$BC00 to Y:$BFFF are double-mapped with the main flash-backed RAM for the M-variable definitions, and should not be used for user parameter storage.

Any value written into the Option 16 memory will be retained automatically through a power-down or reset; no Save operation is required. The power draw on the battery is low enough that battery life will be limited only by the quoted 10-year life of the battery.