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USER MANUAL

Accessory 14D

Input/Output Expansion Board

3Ax-602193-xUxx

September 30, 2003

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INTRODUCTION

PMAC's Accessory 14D/V provides expanded and flexible digital I/O capabilities for the controller. It may be configured for a wide variety of different uses to serve many diverse applications. It is commonly used for discrete I/O and for parallel feedback (absolute encoders, and laser inferometers). PMAC Accessory 14 is a single input/output (I/O) expansion board for PMAC-PC (Acc-14D) and for PMAC-VME (Acc-14V). This accessory provides PMAC with 48-bits of digital I/O which may be configured according to the customer's specific needs. A multitude of possibilities for voltage level, sinking/sourcing and latched/non-latched I/O are available for standard and customized ordering.

Up to six Acc-14D/Vs may be connected to a single PMAC at the same time. This extends PMAC's on-board I/O capabilities with a maximum of 288 additional external I/O.

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CONNECTORS

There are 15 connectors on an Acc-14D/V, numbered J1 to J15. Their functions are summarized as follows (pin-by-pin descriptions are located in another part of this manual):

P1	This connector brings in the digital +5V power supply.
J1	Outputs an A/B quadrature signal derived from Acc-14D/V Option 6 in an HP-encoder-compatible format; this signal is intended for input into a PMAC Acc-8D board.
J2	Reserved for future use.
J3	Outputs an A/B quadrature signal derived from Acc-14D/V Option 6 in an HP-encoder-compatible format; this signal is intended for input into a PMAC Acc-8D board.
J4	Reserved for future use.
J5	Outputs A/B quadrature signals derived from Acc-14D/V Option 6 for input to PMAC JXIO connectors; this is the standard method for synthesized quadrature feedback.
J6	Reserved for future use.
J7	Provides the 24 inputs/outputs of Port A, with associated grounds and voltage sources.
J8	Provides the connection from Acc-14D/V directly to PMAC's JEXP connector. It is to be used only on the Acc-14D/V closest to PMAC (or the only Acc-14D/V). (See the Diagrams and Schematics section in this manual.)
J9	Provides the connection for a second or further Acc-14D to the J10 connector of the Acc-14D next closer to the PMAC. (See the Diagrams and Schematics section in this manual.) **Note:** This connector does not exist on Acc-14V; the J10 connector is used instead.
J10	Provides the connection to the J9 connectors of Acc-14s that are further away from PMAC. (See the Diagrams and Schematics section in this manual.)
J15	Provides the 24 inputs/outputs of Port B, with associated grounds and voltage sources.
TB1	Is a 4-pin terminal block providing alternative power supply inputs to Acc-14D/V.

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POWER CONNECTION

The terminal block TB1 provides an alternative connector for the power supply inputs into Acc-14D/V. Normally, the bus connector P1 is used for this purpose. However, in standalone applications, TB1 provides a convenient means for power supply connections.

Note:

The +5V power is required for Acc-14D/V's digital circuits.

The pin-by-pin descriptions of the terminal block's connectors are:

Location	Pin	Description
TB1	Pin #1	GND
TB1	Pin #2	+5V
TB1	Pin #3	+12V (presently not used on Acc-14D/V)
TB1	Pin #4	-12V (presently not used on Acc-14D/V)

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OPTION SELECTION

Each Acc-14D/V must be ordered with one of the following six options:

- OPT-1: 24 inputs and 24 outputs; TTL levels 0 to 5 Volts, low true (3xI4, 3X04)
- OPT-2: 24 inputs and 24 outputs; 0 to 24 volts, low true (3XI1, 3x01)
- OPT-3: 48 inputs, TTL levels; latching; for parallel binary feedback (6x I5)
- OPT-4: Custom configuration of 48 I/O to be specified by customer (see below)
- OPT-6: Parallel Input to A QUAD B Output Converter
- OPT-7: 20cm (8") 50-Pin 3-Connector cable. For use with Acc-14D when PMAC Option 2,
- Acc-24P or Acc-36P is also used.

Acc-14 Option 6 enables the accessory card to generate quadrature feedback. This option also has jumpers to customize the board to the users needs.

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ORDERING CUSTOM CONFIGURATION (OPTION 4)

Acc-14D/V's 48 bits of I/O are grouped into 6 bytes (Bytes 1-6). Each byte may be set up as an input byte or an output byte. These bytes are further grouped into two ports (A and B), each with its own connector (J7 and J15, respectively). Each port has a single supply voltage and a single strobe source (or lack of one), so it is not possible, for instance, to mix 5V and 24V inputs on the same port.

In purchasing an Acc-14D/V, each byte should be specified as to input, output, or empty, and which input or output option. These options are detailed as follows (the IC used for each option is provided for reference):

Custom Input/Output Types

Input Types	Description
I1:	14-25V inverting unlatched inputs (ULN2802A) (external voltage source required)
I2:	6 -15V inverting unlatched inputs (ULN2804A) (external voltage source required)
I3:	5V non-inverting unlatched inputs (74AC573)
I4:	5V inverting unlatched inputs (74AC563) (for input from OPTO-22)
I5:	5V non-inverting edge-triggered inputs (74AC574) (for absolute encoders)

Output Types	Description
O1:	5-24V inverting open-collector (sinking) outputs (ULN2803A) **Note:** External source may be required.
O2:	5-24V non-inverting sourcing outputs (UDN2981A) **Note:** External source may be required.
O3:	5V non-inverting sinking/sourcing outputs (74AC573)
O4:	5V inverting sinking/sourcing outputs (74AC563) (For output to OPTO-22)

Example: To use Port A (Bytes 1-3) for an absolute encoder input, and Port B (Bytes 4-6) for 16 bits of OPTO-22 output and eight bits of OPTO-22 input, specify:

BYTE	I/O Option
1	I5
2	I5
3	I5
4	O4
5	O4
6	I4

Note:

It is possible to specify incompatible configurations. **Example:** I1 and O3 could not work on the same port together because of voltage differences.

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CUSTOM BOARD CONFIGURATION

For a given configuration specification, the board should be configured properly at the factory. This information is provided for reference, troubleshooting, and user configuration changes.

IC Placement:

On each Acc-14D/V, there are six pairs of 20 pin sockets for the I/O buffer ICs (which are chosen from the options above) -- one for each byte of I/O. The left socket is for an input buffer IC, and the right socket is for an output buffer IC. Only one socket of each pair should have an IC in it. The sockets that correspond to each byte are:

Byte	Input Socket	Output Socket	Connector and Pins
1	U9	U10	J7:MI/O0-MI/O7
2	U4	U5	J7:MI/O8-MI/O15
3	U26	U27	J7:MI/O16-MI/O23
4	U28	U29	J15:MI/O24-MI/O31
5	U20	U21	J15:MI/O32-MI/O39
6	U11	U12	J15:MI/O40-MI/O47
Refer to the board layout diagrams of Acc-14D/V in the Diagrams and Schematics section of this manual for locations of these IC sockets.			

Jumpers

Acc-14D/V has many jumpers (E-Points) to provide the required flexibility in configuring the card. While the factory will try to set the jumpers to meet the needs as specified in the ordering configuration, check the jumpers before installing the card in the system. Some jumpers affect the whole card (global), some affect a port, and some affect an individual byte. The E-Point table in the appendix summarizes the jumper settings and can be used to check the configuration. The E-Point jumpers in the table are listed in the order they are presented.

Global Jumpers

Jumper E20 should be OFF (default) for the Acc-14D/V that connects directly to PMAC if it connects with PMAC's J8 connector. For additional Acc-14Ds (up to five more are permitted) that daisy chain through the first Acc-14D, E20 should be ON (See E-Point Jumpers section in this manual.).

Jumper E20 should be OFF if the buffers on the Acc-14D/V are used. This is true only if this Acc-14D/V is connected directly through the J8 connector directly to PMAC, which should only be done for a PMAC with battery-backed RAM.

Jumper E20 should be ON if the buffers on the Acc-14D/V are bypassed. This is true only if this Acc-14D/V is connected through the J9 or J10 (VME) connector to the PMAC or the previous Acc-14D/V or ACC36P/V in the chain. The J9/J10 connector should be used to connect to a PMAC with Flash-backed RAM.

Jumpers E12 through E17 determine the card's address in PMAC's memory and I/O space. Only one of these jumpers should be ON (jumpered) on an Acc-14D/V, and each Acc-14D/V attached to a given PMAC should have a different one of these jumpers ON (See E-Point Jumpers section in this manual.). The list of PMAC word addresses that each jumper selects is as follows:

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PMAC Acc-14D/V Addressing

Jumper	Port A (J7)	Port B (J15)	Control Word
E12	Y:$FFD0	Y:$FFD1	Y:$FFD3
E13	Y:$FFD8	Y:$FFD9	Y:$FFDB
E14	Y:$FFE0	Y:$FFE1	Y:$FFE3
E15	Y:$FFE8	Y:$FFE9	Y:$FFEB
E16	Y:$FFF0	Y:$FFF1	Y:$FFF3
E17	Y:$FFF8	Y:$FFF9	Y:$FFFB

Turbo PMAC Acc-14D/V Addressing

Jumper	Port A (J7)	Port B (J15)	Control Word
E12	Y:$078A00	Y:$078A01	Y:$078A03
E13	Y:$078B00	Y:$078B01	Y:$078B03
E14	Y:$078C00	Y:$078C01	Y:$078C03
E15	Y:$078D00	Y:$078D01	Y:$078D03
E16	Y:$078E00	Y:$078E01	Y:$078E03
E17	Y:$078F00	Y:$078F01	Y:$078F03

Port Jumpers

Jumper E8 (Port A) or **jumper E9 (Port B)** ON, forces the strobe signal high for that port (high) at all times, so that the buffers on the port are transparent latches. This is the setting to be used except for a latched input such as an absolute encoder, which has this jumper off for strobing. If you are strobing the port, the following jumpers are also important:

Jumper E4 ON allows a low ERR1/ input to disable the Port A strobe. Jumper E7 ON does the same for Port B.

Jumper E5 ON allows the rising-edge of the ICLK1 input from J7 to latch Port A inputs when the servo clock is low.

Jumper E5 OFF inverts this input. E6 performs the same function on ICLK2 (J15) for Port B.

If you want the servo clock signal from PMAC to perform the strobing to latch inputs at the beginning of the servo cycle (e.g. for absolute encoder position feedback), then E4 and E5 should be ON, and E8 OFF for Port A; E6 and E7 should be ON, and E9 OFF for Port B. In addition, ICLK1 and ERR1/ should not be externally supplied for Port A. Likewise, ICLK2, and ERR2/ should not be externally supplied for Port B.

Jumper E21 controls whether the servo clock signal is passed to OCLK1 (J7) inverted or non-inverted; E22 does the same for OCLK2 (J15). Jumpering pins 2 and 3 passes the signal on non-inverted; jumpering 1 and 2 inverts it. Since the servo clock falls at the beginning of the cycle, when you want to latch external position latches, jumper 2 to 3 if using a falling-edge-latched encoder, or 1 to 2 if using a rising-edge latched encoder.

Byte Jumpers

Each byte has four associated jumpers that are configured according to the type of input or output that is being used for that byte. The following table shows which jumpers belong to each byte and what they do:

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Byte	For Input or Output Pull-up/Pull-down	For Output only Pin 10: Level Select	For Output only Pin 11: Level or Strobe	For Output Only Pin 11: Level Select
1	E2	E31	E27	E28
2	E1	E30	E25	E26
3	E11	E29	E23	E24
4	E10	E38	E32	E33
5	E41	E39	E34	E35
6	E3	E40	E36	E37
	1-2 is up	1-2 sink	1-2 level	1-2 sink
	2-3 is down	2-3 source	2-3 strobe	2-3 source

Options I1, I2, I3, I4, & I5 should have:
- Pull-up/Pull-down jumper: 1-2 (up)
- Pin 10 Level Select jumper: does not matter
- Pin 11 Level or Strobe jumper: does not matter
- Pin 11 Level Select jumper: does not matter

Option O1 should have:
- Pull-up/Pull-down jumper: 1-2 (up)
- Pin 10 Level Select jumper: 1-2 (GND)
- Pin 11 Level or Strobe jumper: 2-3 (level)
- Pin 11 Level Select jumper: 1-2 (+V)

Option O2 should have:
- Pull-up/Pull-down jumper: 2-3 (down)
- Pin 10 Level Select jumper: 2-3 (+V)
- Pin 11 Level or Strobe jumper: 2-3 (level)
- Pin 11 Level Select jumper: 2-3 (GND)

Options O3 and O4 should have:
- Pull-up/Pull-down jumper: 1-2 (up)
- Pin 10 Level Select jumper: 1-2 (GND)
- Pin 11 Level or Strobe jumper: 1-2 (strobe)
- Pin 11 Level Select jumper: does not matter
- E8 (for Byte 0-2) or E9 (for Byte 3-5) must be ON (strobe always +5V)

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PMAC CONNECTIONS

For a PMAC with battery-backed RAM, the PMAC's JEXP connector should be linked to the first Acc-14D/V's J8 connector via the provided flat cable. For a PMAC with Flash RAM backup, the JEXP connector should be linked to the first Acc-14D/V's J9 connector. If multiple Acc-14D/Vs are to be used, J10 of the first Acc-14D/V should be connected to J9 of the second Acc-14D/V. For the second, third, fourth, fifth, and sixth Acc-14D/Vs, only J9 and J10 should be used (See the Diagrams and Schematics section of this manual.).

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SOFTWARE SETUP

Acc-14D/V must be software-configured each time it is powered up to set, which bytes are inputs and which bytes are outputs. This is done by writing to the control word (base address + 3). Typically, this will be done by a PLC program that writes the proper control words once on power-up automatically, and then disables itself. It could also be done from a motion program or from on-line commands.

The control word is a 24-bit word; each bit must be configured correctly. The bits are as follows:

Bit 0: must be 1
Bit 1: controls Byte 4: 0 for output, 1 for input
Bit 2: must be 0
Bit 3: must be 1
Bit 4: controls Byte 1: 0 for output, 1 for input
Bit 5: must be 0
Bit 6: must be 0
Bit 7: must be 1
Bit 8: must be 0
Bit 9: controls Byte 5: 0 for output, 1 for input
Bit 10: must be 0
Bit 11: must be 0
Bit 12: controls Byte 2: 0 for output, 1 for input
Bit 13: must be 0
Bit 14: must be 0
Bit 15: must be 1
Bit 16: must be 1
Bit 17: controls Byte 6: 0 for output, 1 for input
Bit 18: must be 0
Bit 19: must be 0
Bit 20: controls Byte 3: 0 for output, 1 for input
Bit 21: must be 0
Bit 22: must be 0
Bit 23: must be 1

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The value of the word that must be written to the control word for your particular configuration can be selected from the following table (O stands for output; I stands for input):

Byte:	6	5	4	3	2	1	Hex Control Word
	O	O	O	O	O	O	$818089
	O	O	O	O	O	I	$818099
	O	O	O	O	I	O	$819089
	O	O	O	O	I	I	$819099
	O	O	O	I	O	O	$918089
	O	O	O	I	O	I	$918099
	O	O	O	I	I	O	$919089
	O	O	O	I	I	I	$919099
	O	O	I	O	O	O	$81808B
	O	O	I	O	O	I	$81809B
	O	O	I	O	I	O	$81908B
	O	O	I	O	I	I	$81909B
	O	O	I	I	O	O	$91809B
	O	O	I	I	O	I	$91809B
	O	O	I	I	I	O	$91908B
	O	O	I	I	I	I	$91909B
	O	I	O	O	O	O	$818299
	O	I	O	O	O	I	$818299
	O	I	O	O	I	O	$819289
	O	I	O	O	I	I	$819299
	O	I	O	I	O	O	$918289
	O	I	O	I	O	I	$918299
	O	I	O	I	I	O	$919289
	O	I	O	I	I	I	$919299
	O	I	I	O	O	O	$81828B
	O	I	I	O	O	I	$81829B
	O	I	I	O	I	O	$81928B
	O	I	I	O	I	I	$81929B
	O	I	I	I	O	O	$91828B
	O	I	I	I	O	I	$91829B
	O	I	I	I	I	O	$91928B
	O	I	I	I	I	I	$91929B

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Byte:	6	5	4	3	2	1	Hex Control Word
	I	O	O	O	O	O	$838089
	I	O	O	O	O	I	$838099
	I	O	O	O	I	O	$839089
	I	O	O	O	I	I	$839099
	I	O	O	I	O	O	$938089
	I	O	O	I	O	I	$938099
	I	O	O	I	I	O	$939089
	I	O	O	I	I	I	$939099
	I	O	I	O	O	O	$83808B
	I	O	I	O	O	I	$83809B
	I	O	I	O	I	O	$83908B
	I	O	I	O	I	I	$83909B
	I	O	I	I	O	O	$93808B
	I	O	I	I	O	I	$93809B
	I	O	I	I	I	O	$93908B
	I	O	I	I	I	I	$93909B
	I	I	O	O	O	O	$838289
	I	I	O	O	O	I	$838299
	I	I	O	O	I	O	$839289
	I	I	O	O	I	I	$839299
	I	I	O	I	O	O	$938289
	I	I	O	I	O	I	$938299
	I	I	O	I	I	O	$939289
	I	I	O	I	I	I	$939299
	I	I	I	O	O	O	$83828B
	I	I	I	O	O	I	$83829B
	I	I	I	O	I	O	$83928B
	I	I	I	O	I	I	$83929B
	I	I	I	I	O	O	$93828B
	I	I	I	I	O	I	$93829B
	I	I	I	I	I	O	$93928B
Opt 3 default	I	I	I	I	I	I	$93929B

Example: To use the entire Port B (Bytes 4-6) for output and the entire Port A (Bytes 1-3) for input, the control setup word would be $919099 (See shaded row in the Control Word table). If this Acc-14D was at the first card address, the control word would be at PMAC word address Y:$FFD3 and at address Y:$078A03 for Turbo PMAC. Setting up the Acc-14D/V would simply be a matter of writing $919099 to Y:$FFD3 (for PMAC) or Y:$078A03 (for Turbo PMAC).

From PMAC's host, this could be done with one on-line command: the Write (W) command. Sending the line:

For PMAC `WY:$FFD3,$919099`
For Turbo PMAC `WY:$078A03,$919099`

to PMAC would set up the Acc-14D/V properly. This method is good for trying the board out in development. A similar method is to define an M-variable to the control word (the definition is stored in battery-backed RAM), then assign a value to the M-variable:

PMAC Type	Definition
PMAC	`M948->Y:$FFD3,0,24`
Turbo PMAC	`M948->Y:$078A03,0,24`

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```
M948=$919099                    (sets the value)
```

Typically in actual use, a PLC program will be used to set up the control word. This PLC program will act once, on power-up or reset, to write to the control word; then it will disable itself. The following example shows how to enter a PLC program to set up our one Acc-14D. It presumes M948 has already been defined to the control word as shown above:

```
OPEN PLC 1
CLEAR
M948=$919099
DISABLE PLC 1
CLOSE
```


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USING ACC-14D IN PROGRAMS

Typically, the Acc-14D/V I/O is used in PMAC programs (motion and PLC) through the use of M-variables. M-variables, which point to places in PMAC's memory and I/O address space, are defined ahead of time to the desired location and size. They are then used in programs just as any other variable. Usually, on an Acc-14D/V, the M-variables are defined to individual bits, but this is not required.

The M-variable definition carries no information about whether the location is input or output; it is the user's responsibility to keep the difference straight. A typical set of definitions for a single Acc-14D would be:

Non-Turbo PMAC Sample M-Variable Definitions

M900->Y:$FFD0,0,1	Port A I/O bit 0	M924->Y:$FFD1,0,1	Port B I/O bit 0
M901->Y:$FFD0,1,1	Port A I/O bit 1	M925->Y:$FFD1,1,1	Port B I/O bit 1
M902->Y:$FFD0,2,1	Port A I/O bit 2	M926->Y:$FFD1,2,1	Port B I/O bit 2
M903->Y:$FFD0,3,1	Port A I/O bit 3	M927->Y:$FFD1,3,1	Port B I/O bit 3
M904->Y:$FFD0,4,1	Port A I/O bit 4	M928->Y:$FFD1,4,1	Port B I/O bit 4
M905->Y:$FFD0,5,1	Port A I/O bit 5	M929->Y:$FFD1,5,1	Port B I/O bit 5
M906->Y:$FFD0,6,1	Port A I/O bit 6	M930->Y:$FFD1,6,1	Port B I/O bit 6
M907->Y:$FFD0,7,1	Port A I/O bit 7	M931->Y:$FFD1,7,1	Port B I/O bit 7
M908->Y:$FFD0,8,1	Port A I/O bit 8	M932->Y:$FFD1,8,1	Port B I/O bit 8
M909->Y:$FFD0,9,1	Port A I/O bit 9	M933->Y:$FFD1,9,1	Port B I/O bit 9
M910->Y:$FFD0,10,1	Port A I/O bit 10	M934->Y:$FFD1,10,1	Port B I/O bit 10
M911->Y:$FFD0,11,1	Port A I/O bit 11	M935->Y:$FFD1,11,1	Port B I/O bit 11
M912->Y:$FFD0,12,1	Port A I/O bit 12	M936->Y:$FFD1,12,1	Port B I/O bit 12
M913->Y:$FFD0,13,1	Port A I/O bit 13	M937->Y:$FFD1,13,1	Port B I/O bit 13
M914->Y:$FFD0,14,1	Port A I/O bit 14	M938->Y:$FFD1,14,1	Port B I/O bit 14
M915->Y:$FFD0,15,1	Port A I/O bit 15	M939->Y:$FFD1,15,1	Port B I/O bit 15
M916->Y:$FFD0,16,1	Port A I/O bit 16	M940->Y:$FFD1,16,1	Port B I/O bit 16
M917->Y:$FFD0,17,1	Port A I/O bit 17	M941->Y:$FFD1,17,1	Port B I/O bit 17
M918->Y:$FFD0,18,1	Port A I/O bit 18	M942->Y:$FFD1,18,1	Port B I/O bit 18
M919->Y:$FFD0,19,1	Port A I/O bit 19	M943->Y:$FFD1,19,1	Port B I/O bit 19
M920->Y:$FFD0,20,1	Port A I/O bit 20	M944->Y:$FFD1,20,1	Port B I/O bit 20
M921->Y:$FFD0,21,1	Port A I/O bit 21	M945->Y:$FFD1,21,1	Port B I/O bit 21
M922->Y:$FFD0,22,1	Port A I/O bit 22	M946->Y:$FFD1,22,1	Port B I/O bit 22
M923->Y:$FFD0,23,1	Port A I/O bit 23	M927->Y:$FFD1,23,1	Port B I/O bit 23

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Turbo PMAC Sample M-Variable Definitions

M900->Y:$078A00,0,1	Port A I/O bit 0	M924->Y:$078A01,0,1	Port B I/O bit 0
M901->Y:$078A00,1,1	Port A I/O bit 1	M925->Y:$078A01,1,1	Port B I/O bit 1
M902->Y:$078A00,2,1	Port A I/O bit 2	M926->Y:$078A01,2,1	Port B I/O bit 2
M903->Y:$078A00,3,1	Port A I/O bit 3	M927->Y:$078A01,3,1	Port B I/O bit 3
M904->Y:$078A00,4,1	Port A I/O bit 4	M928->Y:$078A01,4,1	Port B I/O bit 4
M905->Y:$078A00,5,1	Port A I/O bit 5	M929->Y:$078A01,5,1	Port B I/O bit 5
M906->Y:$078A00,6,1	Port A I/O bit 6	M930->Y:$078A01,6,1	Port B I/O bit 6
M907->Y:$078A00,7,1	Port A I/O bit 7	M931->Y:$078A01,7,1	Port B I/O bit 7
M908->Y:$078A00,8,1	Port A I/O bit 8	M932->Y:$078A01,8,1	Port B I/O bit 8
M909->Y:$078A00,9,1	Port A I/O bit 9	M933->Y:$078A01,9,1	Port B I/O bit 9
M910->Y:$078A00,10,1	Port A I/O bit 10	M934->Y:$078A01,10,1	Port B I/O bit 10
M911->Y:$078A00,11,1	Port A I/O bit 11	M935->Y:$078A01,11,1	Port B I/O bit 11
M912->Y:$078A00,12,1	Port A I/O bit 12	M936->Y:$078A01,12,1	Port B I/O bit 12
M913->Y:$078A00,13,1	Port A I/O bit 13	M937->Y:$078A01,13,1	Port B I/O bit 13
M914->Y:$078A00,14,1	Port A I/O bit 14	M938->Y:$078A01,14,1	Port B I/O bit 14
M915->Y:$078A00,15,1	Port A I/O bit 15	M939->Y:$078A01,15,1	Port B I/O bit 15
M916->Y:$078A00,16,1	Port A I/O bit 16	M940->Y:$078A01,16,1	Port B I/O bit 16
M917->Y:$078A00,17,1	Port A I/O bit 17	M941->Y:$078A01,17,1	Port B I/O bit 17
M918->Y:$078A00,18,1	Port A I/O bit 18	M942->Y:$078A01,18,1	Port B I/O bit 18
M919->Y:$078A00,19,1	Port A I/O bit 19	M943->Y:$078A01,19,1	Port B I/O bit 19
M920->Y:$078A00,20,1	Port A I/O bit 20	M944->Y:$078A01,20,1	Port B I/O bit 20
M921->Y:$078A00,21,1	Port A I/O bit 21	M945->Y:$078A01,21,1	Port B I/O bit 21
M922->Y:$078A00,22,1	Port A I/O bit 22	M946->Y:$078A01,22,1	Port B I/O bit 22
M923->Y:$078A00,23,1	Port A I/O bit 23	M927->Y:$078A01,23,1	Port B I/O bit 23

A typical use of an output bit in a program would be:

```
X1000Y1000
DWELL500
M900=1
```

A typical use of an input bit in a program would be:

```
IF (M930=1)
      X1000Y1000
ELSE
      X-1000Y-1000
ENDIF
```


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PARALLEL POSITION FEEDBACK FOR PMAC

If you are providing position information to PMAC (non Turbo) as a parallel data word – as from an absolute encoder or processed from a laser interferometer, the encoder conversion table must be configured properly. For parallel position feedback, use one of the conversion formats **$2x**, **$3x**, **$6x**, or **$7x**. Formats **$2x** and **$3x** get data from the specified source in Y-memory space; **$6x** and **$7x** get it from X-memory space. Usually, this data is brought in on an Acc-14 board, which is in the Y-memory space, so the **$6x** and **$7x** formats are rarely used.

The encoder conversion table can be modified using either PMAC's Executive Program Encoder Conversion Table dialog box or the on-line commands in the Executive terminal mode. The following sections describe in detail PMAC's parallel feedback conversion process and actual setup.

Source Register

Acc-14 uses the following source addresses to bring in the data:

1st Acc-14 Port A (J7):	$FFD0
1st Acc-14 Port B (J15):	$FFD1
2nd Acc-14 Port A (J7):	$FFD8
2nd Acc-14 Port B (J15):	$FFD9
3rd Acc-14 Port A (J7):	$FFE0
3rd Acc-14 Port B (J15):	$FFE1
4th Acc-14 Port A (J7):	$FFE8
4th Acc-14 Port B (J15):	$FFE9
5th Acc-14 Port A (J7):	$FFF0
5th Acc-14 Port B (J15):	$FFF1
6th Acc-14 Port A (J7):	$FFF8
6th Acc-14 Port B (J15):	$FFF9

A typical setup word for this type of feedback is **$20FFD0**, which provides for non-filtered conversion of the parallel data word fed into Port A of the first Acc-14 connected to PMAC.

Unshifted Conversion

If bit 19 of the source and process word for the parallel data conversion is set to 1, the converted data contains no fractional bits. Entries of this form would have the conversion formats (bits 16-23 of this word) $28, $38, $68 or $78, as opposed to the standard entries $20,$30, $60, and $ 70, which provide five fractional bits in the converted data.

The Unshifted format is used for high-speed, very high-resolution applications, typically with parallel laser interferometer feedback. With the normal shifted format, PMAC's internal velocity registers saturate when the counts/sec × Ix08 exceed 256M (268,435,456). With the unshifted format, this limit is 8G (8,589,934,592) or 32 times higher.

Bit-Enable Mask Word

Parallel-feedback conversion requires a double (for non-filtered) or triple (for filtered) entry in the conversion table. The second entry – filtered or non-filtered – specifies the size of the feedback word used. The entry is a 24-bit word in which each bit actually used for the parallel feedback is a one; the unused bits above are zeros (parallel feedback should always be connected starting at bit 0 of the data word).

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For a 12-bit absolute encoder, this entry would be **$000FFF**; for 14 bits, it would be **$003FFF**. The maximum useful entry for the standard shifted conversion is for 19 bits: **$07FFFF** because the high five bits get shifted out of the result register. The maximum useful entry for the unshifted conversion is 24 bits: **$FFFFFF**. In both cases, absolute position over a wider range (up to 43 bits) is supported with Ix10 (See the Absolute Power On Position section of this manual.). The count can also be software-extended by PMAC, permitting rollover.

Filter Word

If the conversion format is **$3x** or **$7x**, the parallel data word is filtered. The filter simply sets a maximum amount that the data word is permitted to change in a single servo cycle. If PMAC sees a change larger than this in the source data word, the converted data only changes by the maximum amount. There is no permanent loss of position information if the filter kicks in.

Purpose of Filtering

This filtering permits protection against spurious changes on high-order data lines, while not delaying legitimate changes at all. This maximum amount is the third setup entry for the encoder in the Y-column of the conversion table. It should be set slightly greater than the maximum actual velocity expected on the sensor, expressed in counts (bits) per servo cycle.

Converted Data

The converted data from the parallel word is put in the X data word matching the last (2nd or 3rd) setup word for the entry. This is the address that should be used by the motor I-variable that picks up position (Ix03, Ix04, or Ix05). **Example:** If the first setup entry (address Y:$0720) in the conversion table were $30FFD0 (filtered parallel data), the size entry would be in Y:$0721, and the maximum change entry would be in Y:$0722. The converted data would be placed in X:$0722. If this were the position feedback for motor #1, Ix03 would be set to $0722 (1826 decimal). For incremental parallel feedback, bit 16 of Ix03 should be set to 1 for proper homing search moves.

For unfiltered parallel feedback, an entry would be:

X-Words	Y-Words
1. Intermediate data: Sign-extended most-significant word	1. Source and process Bits 0-15: Address of source data Y-word if $20 conversion X-word if $60 conversion Bits 16-23: = $20 for Y-word source = $60 for X-word source
2. Converted data: Bits 0-4: Fractional Bits Bits 5-23: Integer Bits	2. Bit-enable mask Bit=1 to use corresponding bit from source word Bit=0 not to use corresponding bit from source word

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For a filtered parallel data conversion, an entry would be:

X-Words	Y-Words
1. Intermediate data: Raw data reading	1. Source and process Bits 0-15: Address of source data Y-word if $30 conversion X-word if $70 conversion Bits 16-23: = $30 for Y-word source = $70 for X-word source
2. Intermediate data: Sign-extended most-significant word	2. Bit-enable mask Bit=1 to use corresponding bit from source word Bit=0 not to use corresponding bit from source word
3. Converted data: Bits 0-4: Fractional Bits Bits 5-23: Integer Bits	3. Filter value: Maximum permitted change in counts/servo cycle

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PARALLEL POSITION FEEDBACK FOR TURBO PMAC

Parallel Feedback Entries ($2, $3, $6, $7)

The parallel feedback entries read a word from the address specified in the low 19 bits (bits 0 to 18) of the first line. The four methods in this class are:

- $2: Y-word parallel, no filtering (2-line entry)
- $3: Y-word parallel, with filtering (3-line entry)
- $6: Y/X-word parallel, no filtering (2-line entry)
- $7: Y/X-word parallel, with filtering (3-line entry)

The Bit-19 mode switch in the first line controls whether the least significant bit (LSB) of the source register is placed in Bit 5 of the result register (normal shift), providing the standard 5 bits of (non-existent) fraction, or the LSB is placed in Bit 0 of the result register (unshifted), creating no fractional bits.

Normally, the Bit-19 mode switch is set to 0 to place the source LSB in Bit 5 of the result register. Bit 19 is set to 1 to place to source LSB in Bit 0 of the result register for one of three reasons:

- The data already comes with five bits of fraction, as from a Compact MACRO Station.
- The normal shift limits the maximum velocity too much ($V_{max}<2^{18}$ LSBs per servo cycle)
- The normal shift limits the position range too much (Range$<\pm 2^{47}$/Ix08/32 LSBs)

Unless this is done because the data already contains fractional information, the unshifted conversion will mean that the motor position loop will consider one LSB of the source to be 1/32 of a count, instead of one count.

Width/Offset Word

The second setup line (I-variable) of a parallel read entry contains the width of the data to be read, and the location of the LSB. This 24-bit value, usually represented as six hexadecimal digits, is split evenly into two halves, each of three hex digits. The first half represents the width of the parallel data in bits and can range from $001 (1 bit wide – not of much practical use) to $018 (24 bits wide).

The second half of the line contains the bit location of the LSB of the data in the source word and can range from $000 (Bit 0 of the Y-word at the source address is the LSB) through $017 (Bit 23 of the Y-word at the source address) and $018 (Bit 24, which is Bit 0 of the next word, is the LSB) to $02F (Bit 47 which is Bit 23 of the next word is the LSB).

If the LSB bit location exceeds 23, or the sum of the LSB bit location and the bit width exceeds 24, the source data extends into the next word. If the method character is $2 or $3, the next word is the Y-word at the source address + 1. If the method character is $6 or $7, the next word is the X-word at the source address.

For example, to use 20 bits starting at bit 0 (bits 0 – 19) of the Y-word of the source address, this word would be set to $014000. To use all 24 bits of the X-word of the source address, this word would be set to $018018. To use 24 bits starting at bit 12 of the specified address (with the highest 12 bits coming from the X-word or the next higher Y-address, this word would be set to $01800C.

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Maximum Change Word

If the method character for a parallel read is $3 or $7, specifying filtered parallel read, there is a third setup line (I-variable) for the entry. This third line contains the maximum change in the source data in a single cycle that will be reflected in the processed result, expressed in LSBs per servo cycle. The filtering that this creates provides an important protection against noise and misreading of data. This number is effectively a velocity value, and should be set slightly greater than the maximum true velocity ever expected.

The Accessory 14 family of boards is often used to bring parallel data feedback to the Turbo PMAC, such as that from parallel absolute encoders, and from interferometers. The following table shows the first line of the entries for Acc-14 boards:

Entries for Acc-14D/V Registers

Register	First Line Value	Register	First Line Value
First Acc-14D/V Port A	$m78A00	Fourth Acc-14D/V Port A	$m78D00
First Acc-14D/V Port B	$m78A01	Fourth Acc-14D/V Port B	$m78D01
Second Acc-14D/V Port A	$m78B00	Fifth Acc-14D/V Port A	$m78E00
Second Acc-14D/V Port B	$m78B01	Fifth Acc-14D/V Port B	$m78E01
Third Acc-14D/V Port A	$m78C00	Sixth Acc-14D/V Port A	$m78F00
Third Acc-14D/V Port B	$m78C01	Sixth Acc-14D/V Port B	$m78F01

Turbo Example: One 24-bit Encoder and One 16-bit Encoder

For this example, encoder 1 is the 24-bit encoder wired to Port A and Encoder 2 is the 16-bit encoder wired to port B. The Acc-14D/V is jumpered for base address $78A00.

```
I8000 = $278A00          ;Process Y:$78A00 as parallel word (ECT location $3501)
I8001 = $018000          ;Start at bit 0 of Y:$78A00 and mask 24-bits
                         ;(ECT location $3502)
I8002 = $278A01          ;Process Y:$78A01 as parallel word (ECT location
$3503)
I8003 = $010000          ;Start at bit 0 of Y:$78A00 and mask 24-bits (ECT
                         ;location $3504)
I103 = $3502             ;Motor 1 uses ECT processed data from $3502 for
                         ;position feedback
I104 = $3502             ;Motor 1 uses ECT processed data from $3502 for
                         ;velocity feedback
I203 = $3504             ;Motor 2 uses ECT processed data from $3504 for
                         ;position feedback
I204 = $3504             ;Motor 2 uses ECT processed data from $3504 for
                         ;velocity feedback
```


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ABSOLUTE ENCODER LATCHING AND HANDSHAKING

When using a parallel-word absolute encoder it is very important to properly latch the encoder data to prevent PMAC from reading the encoder data during an encoder transition. Acc-14D/V allows several latching and handshaking methods to fit most types of latching schemes.

Note:

It is equally important to set up the Encoder Conversion Table Filter Word as a software protection against bad encoder data. (See the Filter Word section of this manual.)

PMAC reads the encoder data when it processes the Encoder Conversion Tables. This happens shortly (approximately 2 μsec) after the falling edge of the servo clock (the phase calculations are performed first). Therefore, most of the following latching methods will be synchronized to the falling edge of the servo clock.

Method 1

This method requires the encoder outputs to be latched on the falling edge of the servo clock and no latching to be done on Acc-14D/V. For latching the encoder outputs, the servo clock is accessed through Acc-14D/V OCLK1 (see J7 pinout) and/or OCLK2 (see J15 pinout). If the encoder requires a rising edge for its latch, then E21/E22 should be jumpered 1 to 2 for OCLK1/OCLK2 respectively. If a falling edge is required, E21/E22 should be jumpered 2 to 3.

For the Acc-14D/V, this is a non-standard (custom) configuration. Acc-14D/V with Option 4 will be needed with I3 type inputs using the 74AC573 chip.

The following table shows the jumper settings and the Acc-14D/V options required for this method:

Required Signal	E5/E6	E8/E9	E21/E22	Acc-14D/V Options
Rising edge of OCLK	ON	Don't care	1 to 2	I3 type inputs (74AC573)
Falling edge of OCLK	ON	Don't care	2 to 3	Requires Option 4

The advantages and disadvantages of this method are as follows:

Advantage	Easy to configure and set up.
Disadvantage	Encoder's output latch must typically happen within 2 μsec. Requires Option 4 (custom configuration)

Method 2

This method requires the encoder outputs to be latched on the rising edge of the servo clock and Acc-14D/V to latch (strobe) the encoder inputs on the falling edge of the servo clock. For latching the encoder outputs, the servo clock is accessed through Acc-14D/V OCLK1 (see J7 pinout) and/or OCLK2 (see J15 pinout). If the encoder requires a rising edge for its latch, then E21/E22 should be jumpered 2 to 3 for OCLK1/OCLK2 respectively. If a falling edge is required, E21/E22 should be jumpered 1 to 2. E8/E9 should *not* be jumpered, to allow latching (strobing) on the Acc-14D/V.

This is a standard configuration for the Acc-14D/V. Acc-14D/V with Option 3 will be needed with I5 type inputs using the 74AC574 chip.

The following table shows the jumper settings and the Acc-14D/V options required for this method:

Required Signal	E5/E6	E8/E9	E21/E22	Acc-14D/V Options
Rising edge of OCLK	ON	OFF	2 to 3	I5 type inputs (74AC574)
Falling edge of OCLK	ON	OFF	1 to 2	Requires Option 3

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The advantages and disadvantages of this method are as follows:

Advantage	Encoder latch-time is not very critical (have almost 1 servo cycle to latch).
Disadvantage	Almost a 1-servo cycle delay between encoder output latch and Acc-14D/V encoder read.

Method 3

This method requires a self-latching encoder that outputs a signal that indicates it is latched and an Acc-14D/V that latches (strobes) the encoder inputs on the falling edge of the ICLK only when the servo clock is low. The "encoder-latched" indicator is brought into Acc-14D/V via the ICLK1/2 inputs (see J7 pinout and/or J15 pinout). If the encoder outputs a rising edge for its latch indicator, then E5/E6 should be jumpered, so that a rising ICLK latches the data when the servo is low. If a falling edge indicator is output, E5/E6 should not be jumpered, so that a falling ICLK latches the data when the servo is low. E8/E9 should not be jumpered, to allow latching (strobing) on the Acc-14D/V.

For the Acc-14D/V, this is a standard configuration. Acc-14D/V with Option 3 will be needed with I5 type inputs using the 74AC574 chip.

The following table shows the jumper settings and the Acc-14D/V options required for this method:

Required Signal	E5/E6	E8/E9	E21/E22	Acc-14D/V Options
High ICLK means latched	ON	OFF	Don't care	I5 type inputs (74AC574)
Low ICLK means latched	OFF	OFF	Don't care	Requires Option 3

The advantages and disadvantages of this method are as follows:

Advantage	Can only read latched encoder data.
Disadvantage	Encoder latch is asynchronous to PMAC's servo cycle.

Method 4

This method is a combination of Method 1 and Method 3 above. It requires that the encoder outputs be latched on the falling edge of the servo clock and the encoder to signal that it is latched. Acc-14D/V must also latch (strobe) the encoder inputs on an edge of the ICLK only when the servo clock is low. For latching the encoder outputs, the servo clock is accessed through Acc-14D/V OCLK1 (see J7 pinout) and/or OCLK2 (see J15 pinout). If the encoder requires a rising edge for its latch, then E21/E22 should be jumpered 1 to 2 for OCLK1/OCLK2 respectively. If a falling edge is required, E21/E22 should be jumpered 2 to 3. The encoder-latched indicator is brought into Acc-14D/V via the ICLK1/2 inputs (see J7 pinout and/or J15 pinout). If the encoder outputs a rising edge for its latch indicator, then E5/E6 should be jumpered so that a rising ICLK latches the data when the servo is low. If a falling edge indicator is output, E5/E6 should not be jumpered so that a falling ICLK latches the data when the servo is low. E8/E9 should not be jumpered to allow latching (strobing) on the Acc-14D/V.

For the Acc-14D/V, this is a standard configuration. Acc-14D/V with Option 3 will be needed with I5 type inputs using the 74AC574 chip.

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The following table shows the jumper settings and the Acc-14D/V options required for this method:

Required Signal	E5/E6	E8/E9	E21/E22	Acc-14D/V Options
High OCLK means latch High ICLK means latched	ON	OFF	1 to 2	I5 type inputs (74AC574) Requires Option 3
Low OCLK means latch High ICLK means latched	ON	OFF	2 to 3	
High OCLK means latch Low ICLK means latched	OFF	OFF	1 to 2	
Low OCLK means latch Low ICLK means latched	OFF	OFF	2 to 3	

The advantages and disadvantages of this method are as follows:

Advantage	Can only read latched encoder data. Have full handshaking between PMAC and encoder
Disadvantage	Typically, encoder's output latch must happen within 2 μsec. More complex wiring and timing.

Method 5

This method requires no latching on the encoder outputs and latching on the Acc-14D/V inputs at the falling edge of the servo clock. For the encoder, no signals are used, so the state of E21/E22 does not matter. E5/E6 must be jumpered and E8/E9 must not be jumpered to allow Acc-14D/V to latch (strobe) its inputs with the falling edge of the servo clock.

This is a standard configuration for the Acc-14D/V. Acc-14D/V with Option 3 will be needed with I5 type inputs using the 74AC574 chip.

The following table shows the jumper settings and the Acc-14D/V options required for this method:

Required Signal	E5/E6	E8/E9	E21/E22	Acc-14D/V Options
None	ON	OFF	Don't care	I5 type inputs (74AC574) requires Option 3
None	ON	OFF	Don't care	

The advantages and disadvantages of this method are as follows:

Advantage	Easy to configure and set up.
Disadvantage	The encoder data may be latched into Acc-14D/V at an encoder transition causing bad encoder data for that servo cycle. Must set up the Encoder Conversion Table Filter (see the Filter Word section of this manual.).

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ABSOLUTE POWER ON POSITION

Both the Non-Turbo PMAC and the Turbo PMAC allow the user to obtain absolute position at power up or upon request (#n$*). The Non-Turbo PMAC must have Ix10 setup and the Turbo PMAC needs both Ixx10 and Ixx95 setup to enable this power on position function.

Ix10 permits an automatic read of an absolute position sensor at power-on/reset. If Ix10 is set to 0, the power-on/reset position for the motor will be considered to be 0, regardless of the type of sensor used.

For the non-Turbo PMAC, Ix10 consists of two parts. The low 16 bits, represented by four hex digits, contain the address of the register containing the power-on position information either a PMAC memory-I/O address or an address on the multiplexer (thumbwheel) port. The high eight bits, represented by two hex digits, specify how to read the information at this address.

Absolute Position for Non-Turbo PMAC

Acc-14D/V Base Address	Port	PMAC Register	Ix10 Value
Y:$FFD0	A (J7)	Y:$FFD0	$xxFFD0
Y:$FFD0	B (J15)	Y:$FFD1	$xxFFD1
Y:$FFD8	A (J7)	Y:$FFD8	$xxFFD8
Y:$FFD8	B (J15)	Y:$FFD9	$xxFFD9
Y:$FFE0	A (J7)	Y:$FFE0	$xxFFE0
Y:$FFE0	B (J15)	Y:$FFE1	$xxFFE1
Y:$FFE8	A (J7)	Y:$FFE8	$xxFFE8
Y:$FFE8	B (J15)	Y:$FFE9	$xxFFE9
Y:$FFF0	A (J7)	Y:$FFF0	$xxFFF0
Y:$FFF0	B (J15)	Y:$FFF1	$xxFFF1
Y:$FFF8	A (J7)	Y:$FFF8	$xxFFF8
Y:$FFF8	B (J15)	Y:$FFF9	$xxFFF9
The xx in the first two hexadecimal digits of Ix10 must specify the number of bits in the absolute sensor as a hexadecimal value. The range is $08 to $30 (8 to 48 decimal). **Example:** If motor 1 used an 18-bit absolute encoder at $FFD0, I110 should be set to $12FFD0. If more than 24 bits are used, the low 24 bits must be on Port A of an Acc-14D/V, and the upper bits must be on Port B, starting at the low end.			

Non-Turbo Power-on Position Example

Motor 6 has a 32-bit absolute encoder with the low 24 bits on Port A of the second Acc-14 (Y:$FFD2), and the high 8 bits on the low 8 bits of Port B (Y:$FFD3; unsigned position value: I610=$20FFD2 ($20=32dec). For a signed position value, I610=$A0FFD2.

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Absolute Position for Turbo PMAC

Acc-14D/V Base Address	Port	PMAC Register	Ix10 Value	Ix95 Value
Y:$078A00	A (J7)	Y:$078A00	Y:$078A00	Y:$xx0000
Y:$078A00	B (J15)	Y:$078A01	Y:$078A01	Y:$xx0000
Y:$078B00	A (J7)	Y:$078B00	Y:$078B00	Y:$xx0000
Y:$078B00	B (J15)	Y:$078B01	Y:$078B01	Y:$xx0000
Y:$078C00	A (J7)	Y:$078C00	Y:$078C00	Y:$xx0000
Y:$078C00	B (J15)	Y:$078C01	Y:$078C01	Y:$xx0000
Y:$078D00	A (J7)	Y:$078D00	Y:$078D00	Y:$xx0000
Y:$078D00	B (J15)	Y:$078D01	Y:$078D01	Y:$xx0000
Y:$078E00	A (J7)	Y:$078E00	Y:$078E00	Y:$xx0000
Y:$078E00	B (J15)	Y:$078E01	Y:$078E01	Y:$xx0000
Y:$078F00	A (J7)	Y:$078F00	Y:$078F00	Y:$xx0000
Y:$078F00	B (J15)	Y:$078F01	Y:$078F01	Y:$xx0000

The 'xx' in the first two hexadecimal digits of Ix95 must specify the number of bits in the absolute sensor as a hexadecimal value. The range is $08 to $30 (8 to 48 decimal) for unsigned data or $80 to $B0 (8 to 48 decimal) for signed data. **Example:** If motor 1 used an 18-bit absolute encoder at $78A00, I110 = $078A00 and Ixx95=$120000. If more than 24 bits are used, the low 24 bits must be on Port A of an Acc-14D/V, and the upper bits must be on Port B, starting at the low end.

Turbo Power-on Position Example

Motor 6 has a 32-bit absolute encoder with the low 24 bits on Port A of the second Acc-14 (Y:$078A00), and the high 8 bits on the low 8 bits of Port B (Y:$078A01); unsigned position value: Ix10=$078A00 and Ix95 = $200000 ($20=32dec). For a signed position value, Ix10=$078A00 and Ix95 = $A00000 ($80 + $20 (32-bit decimal) =$A0).

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BRUSHLESS MOTOR COMMUTATION WITH ACC-14D/V FEEDBACK

Acc-14D/V Option 6 allows an A/B Quadrature signal to be synthesized from a parallel input word. With this option PMAC's phasing routines, which require quadrature encoder signals, can be used with a parallel type encoder for brushless motor commutation.

There are two steps to setting up the synthesized quadrature signal. The first is to determine which bits of the input word to use to generate the signal. E-Points E50-E53 control how the synthesized quadrature is generated for input port A and E-Points E54-E57 control the same for input port B. The quadrature is synthesized using two bits of the parallel input word, a least significant bit (LSB) and a most significant bit (MSB). These bits must be chosen as a sequential (neighboring) pair.

Example: If bit 0 is the LSB (E50 jumpered 1 to 2), then bit 1 must be the MSB (E51 jumpered 1 to 2). The possible choices of LSB and MSB are as follows: (Also see the Option 6 E-Points section of this manual.)

Settings of E50 - E53 for Port A

LSB	MSB	E50	E51	E52	E53
Bit 0	Bit 1	1 to 2	1 to 2	No jumper	No jumper
Bit 2	Bit 3	2 to 3	2 to 3	No jumper	No jumper
Bit 4	Bit 5	No jumper	No jumper	1 to 2	1 to 2
Bit 6	Bit 7	No jumper	No jumper	2 to 3	2 to 3

Settings of E54 - E57 for Port B

LSB	MSB	E54	E55	E56	E57
Bit 0	Bit 1	1 to 2	1 to 2	No jumper	No jumper
Bit 2	Bit 3	2 to 3	2 to 3	No jumper	No jumper
Bit 4	Bit 5	No jumper	No jumper	1 to 2	1 to 2
Bit 6	Bit 7	No jumper	No jumper	2 to 3	2 to 3

Choosing which bits should be used for the quadrature generation is based on a couple of factors. If the encoder is an absolute sensor and Ix81 is used for power-on phasing, bits 0 and 1 must be used. This will match encoder position with phase position for absolute power-on phasing requirements. If the encoder is a laser interferometer, the following three things should also be considered:

1. There must be less than 2^23 (8388608) counts per commutation cycle.
2. There can be only one quadrature count per servo cycle (not phase cycle) or the inputs must come through with transparent latches (E8 ON for port A and E9 ON for port B). This is required because the inputs on the Acc-14D/V are latched at the servo clock rate. If transparent latches are used, set PMAC's Ix67 to the maximum possible position change per servo cycle (use the top speed of the motor to calculate this number).
3. If #2 above is not suitable, contact Delta Tau for instructions on bypassing the latches on the quadrature signals while maintaining it on the position data. This will require some field modification to the Acc-14D/V board.

Setting E-Points E42-E45 ON permits the synthesized quadrature to be brought out to the J1, J3, and J5 connectors. E42 and E43 ON jumper the Port A quadrature; E44 and E45 ON jumper the Port B quadrature (see the Option 6 E-Points section of this manual.).

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Once the quadrature is being generated, the connection to PMAC is done via ribbon cables. The quadrature signal can be brought over to the Acc-8D board by connecting J1 (Port A quadrature) and J3 (Port B quadrature) of Acc-14D/V to J1A, J2A, J3A, or J4A of Acc-8D. The quadrature for both ports can also be brought directly to PMAC's J6 (JXIO) connector using J5 of Acc-14D/V. This ties the Port A quadrature into PMAC's ENC1 and the Port B quadrature into ENC3 automatically.

Because the quadrature signal is single-ended, make sure the encoder jumper for the PMAC encoder channel used connects pins 1 and 2 of the complementary inputs to 2.5V.

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PMAC'S JEXP LIMITATION

JEXP (expansion) is the 50-pin cable connector located on PMAC's CPU board. There are limitations to the amount of unbuffered boards that can be connected to one PMAC. These limitations vary with the type of PMAC ordered. Currently PMAC has several options, which can be ordered to enhance PMAC's processing speed:

Standard	20 MHz CPU, One-Wait State RAM, battery backed
Option 4A	20 MHz CPU, Zero-Wait State RAM, Flash backup
Option 5	30 MHz CPU, Zero-Wait State RAM, battery backed
Option 5A	40 MHz CPU, Zero-Wait State RAM, Flash Backup
Option 5B	60 MHz CPU, Zero-Wait State RAM, Flash Backup

The number of unbuffered accessory boards that can be used with one Standard PMAC, PMAC Option 5, and PMAC Option 4A, 5A, and 5B is listed below:

Note:

All PMAC2 boards have Flash CPU.

PMAC with Flash CPU vs. PMAC with Battery backed CPU

Standard PMAC (20 MHz):	2 unbuffered boards
Option 5 PMAC (30 MHz):	1 unbuffered board
Option 4A, 5A, 5B	No limit (buffers are included on PMAC)

In Addition, the following accessories/options are available:

Unbuffered Accessory Boards

Option 2	Dual Ported RAM (see Note below)
Acc-24	Axis Expansion Board
Acc-29	MLDT Interface Board
First Acc-14 or -36 in chain	

Buffered Accessory Boards

Subsequent Acc-14 in chain	Digital I/O boards
Subsequent Acc-36 in chain	A/D Conversion Boards

If PMAC has flash memory, the on board buffers on the accessory board should be bypassed. However, for PMACs with battery backed CPUs, the accessory board that is connected to PMAC's JEXP connector should use its on board buffers (see the Diagrams and Schematics section of this manual.).

Note:

The maximum length of the cable between boards is 6 in. (150 mm).

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Connecting Instructions for PMACs with Flash CPUs to Accessory 14

When connecting several Acc-14s to a PMAC with Flash Memory, there is an alternate method of connecting (ganging) the boards together. As mentioned before, the on-board buffers will be bypassed.

Example: If there are three Acc-14s, connect them as follows:

From		To	
ACC14 #1	J9	PMAC (JEXP)	
ACC14 #2	J9	ACC 14 #1	J10
ACC14 #3	J9	ACC 14 #2	J10

The reason it is connected to J9 instead of J8 is to bypass buffers on the accessory board, since this PMAC option has its own onboard buffers. Connecting to PMAC in this manner makes the data transfer a much faster process.

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POWER REQUIREMENTS

5V	12V	-12V	Other 24V etc.
1.0A	0	0	

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GETTING STARTED WITH ACC-14

Upon receiving the Acc-14, make a photocopy of the E-Point jumper table from this manual, and go down the list, writing down the jumper settings to familiarize yourself with the board, to check if it matches your order, and to keep as a record just in case somebody accidentally changes the jumper settings.

Example I/O Setup

For this example, there is an Accessory 14 Option 1 (24-bit input on port A and 24-bit output on port B). Power off, and plug the Acc-14 into the motherboard or an external power supply. Connect the input cable (J7) and output cable (J15) to a screw terminal block or compatible OPTO 22 card. Power on, and test the voltage from pins 49 and 50.

Next, construct a simple circuit which will enable access to the input byte and output byte (a single input and output bit would be sufficient). Now download the definitions of the M-Variables, for the input and output bytes, to PMAC. It is important to write the following PLCs to set the control word for Acc-14:

```
 ************************************************
;     PLC to set control word for Acc-14
; ************************************************
;
open plc 11
clear
m95=$919099
disable plc 11
close
```

The following program was written to test the inputs and outputs of Acc-14. The input bits and output bits can be changed as needed:

```
; ************************************************
;      Example Program from Acc-14 Manual
; ************************************************
;
;     Remember, Port A defined as m900..m923
;               Port B defined as m924..m947
;
open prog 4
clear
linear
abs
f5000

x1000
dwell 1000

while (1<2)
  if (m900=0)
    m947=0
    x2000
    dwell 1000
    x0
  else
    x3000
    dwell 500
    x0
  endif
endwhile
close
```

The results from this test will depend on the type of input or output option (Ix or Ox) that was ordered.

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Acc-14 D/V Option Specifications

PMAC Acc-14 Configuration Chart

Byte	**1**	**2**	**3**	**4**	**5**	**6**	←	Enter I/O
I/O Option *								Types as required
	High Voltage --			High Voltage --				
	Port A (J7)			Port B (J15)				

Customer Info:
Name:_____ Date:_____
Engineer's Name:_____ PO #_____
Phone:_____ Fax:_____

Input Options:	
I1:	14-25V inverting unlatched inputs (ULN2802A) (external voltage source required)
I2:	6-15V inverting unlatched inputs (ULN2804A) (external voltage source required)
I3:	5V non-inverting unlatched inputs (74AC573)
I4:	5V inverting unlatched inputs (74AC563) (for input from OPTO-22)
I5:	5V non-inverting edge-triggered inputs (74AC574) (for absolute encoders, data is latched.
Output Options:	
O1:	5-24V inverting open-collector (sinking) outputs (ULN2803A) (external source may be required)
O2:	5-24V non-inverting sourcing outputs (UDN2981A) (external source may be required)
O3:	5V non-inverting sinking/sourcing outputs (74AC573)
O4:	5V inverting sinking/sourcing outputs (74AC563) (for output to OPTO-22)

Default Set Ups:

1. (Option 1) Default Set-Up 1
   Port A (J7) (bytes 1, 2 and 3) 24 inputs, 5V (I4), low true
   Port B (J15) (bytes 4, 5 and 6) 24 outputs, 5V (O4), low true

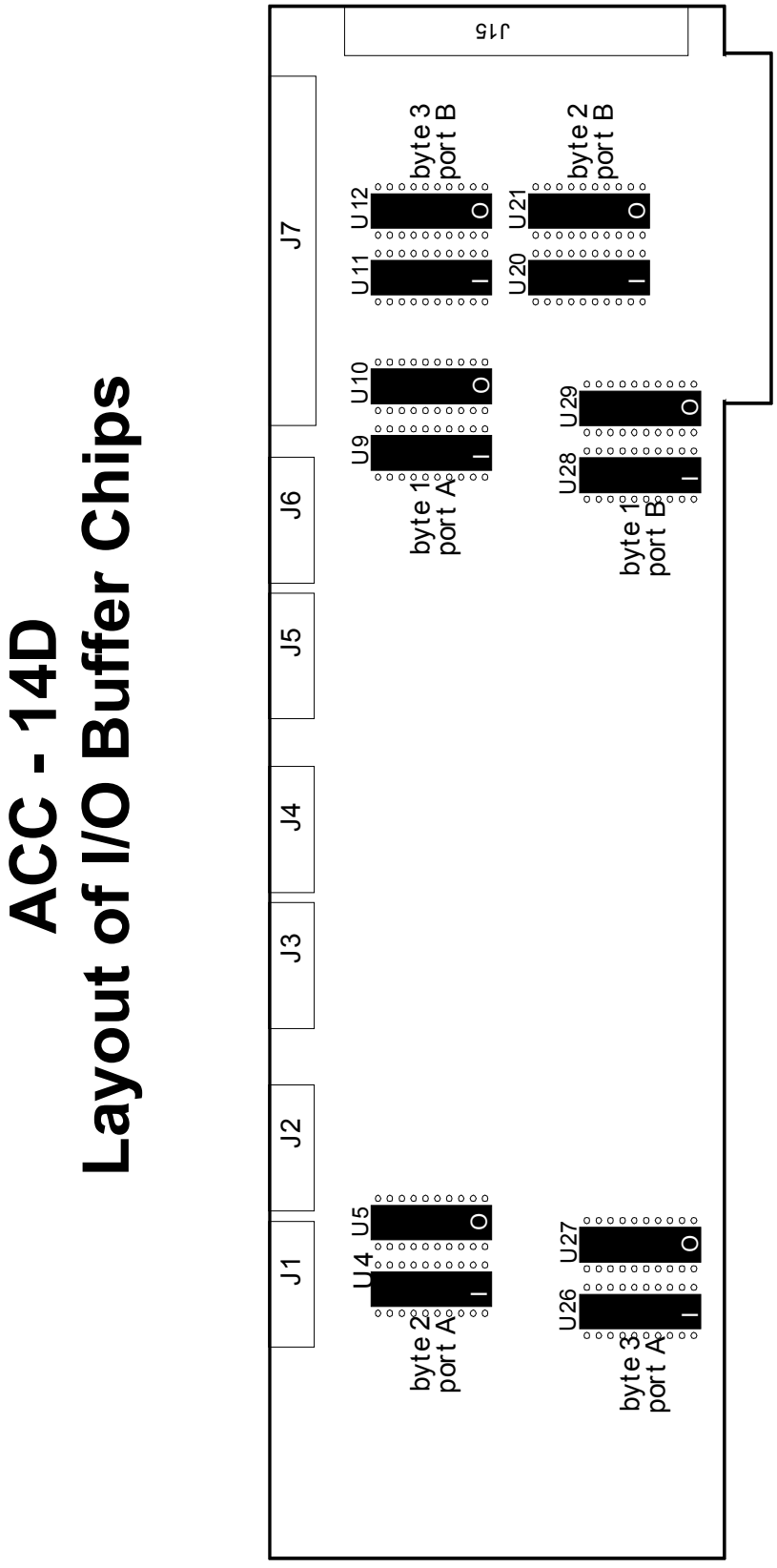
2. (Option 2) Default Set-Up 2
   Port A (J7) (bytes 1, 2 and 3) 24 inputs, 24V. (I1)
   Port B (J15) (bytes 4, 5 and 6) 24 outputs, 24V. (O1)

3. (Option 3) Default Set-Up 3
   For absolute encoder, 48 inputs (2 x 24). (I5) Requires a strobe for latching input data. All data is high true.
   Port A (J7) (bytes 1, 2, and 3) (I5) (parallel binary, 24 bits max.).
   Port B (J15) (bytes 4, 5, and 6) (I5) (parallel binary, 24 bits max.).

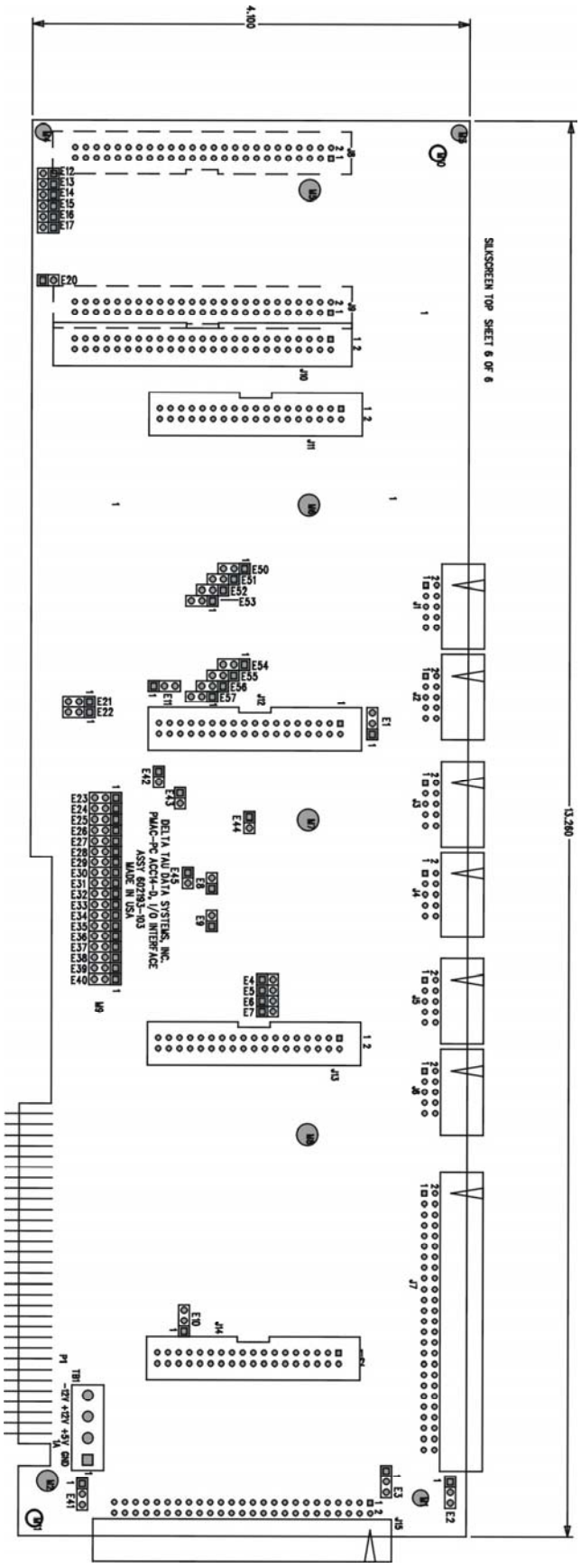
4. (Option 4) Customized Set-Ups.
   Special configuration and combinations (in groups of 8) of I/O may be provided. PMAC's Acc-14 configuration chart shown above must be filled in and faxed to Delta Tau for other processing, and future record keeping.

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DIAGRAMS AND SCHEMATICS

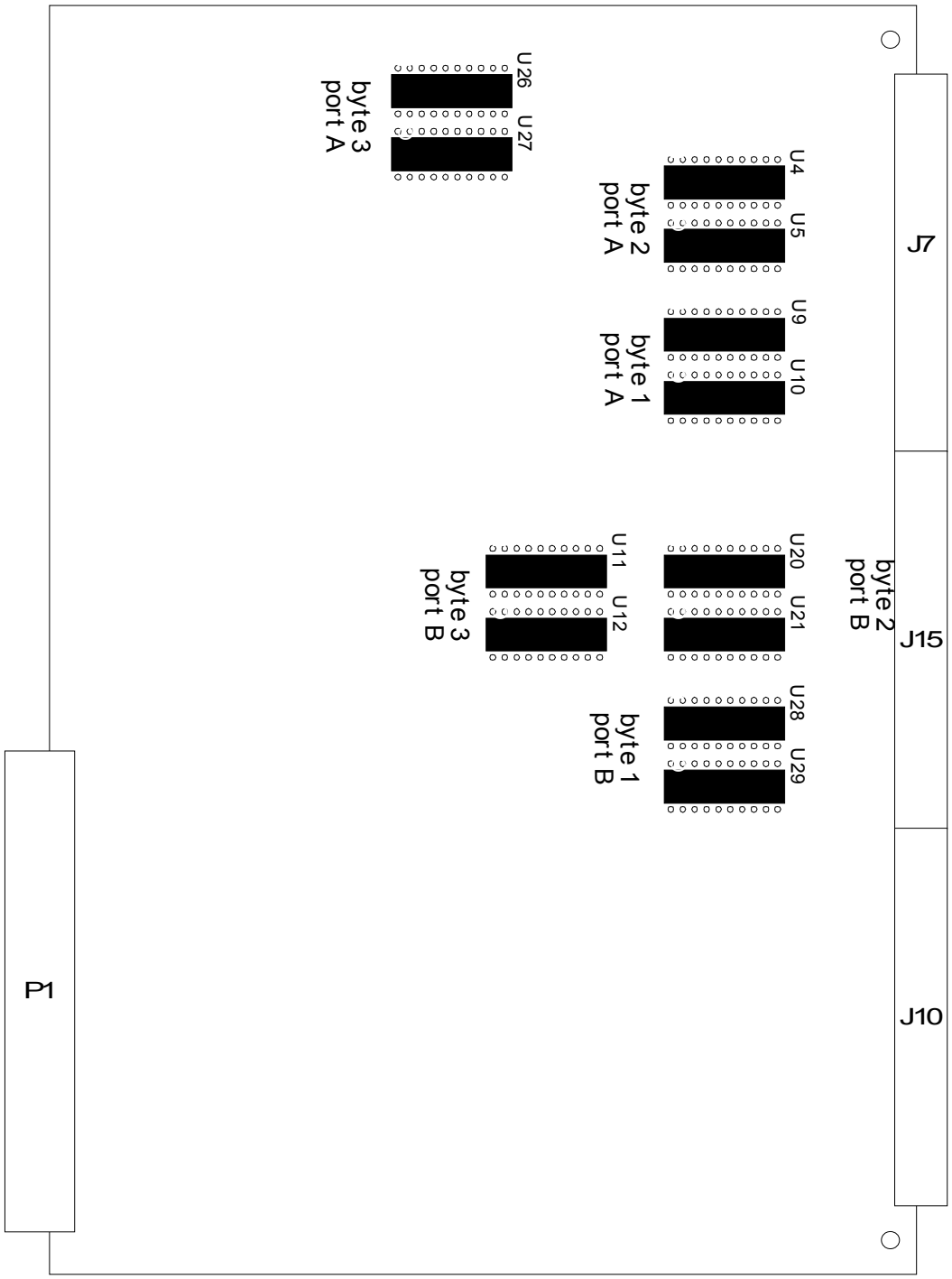


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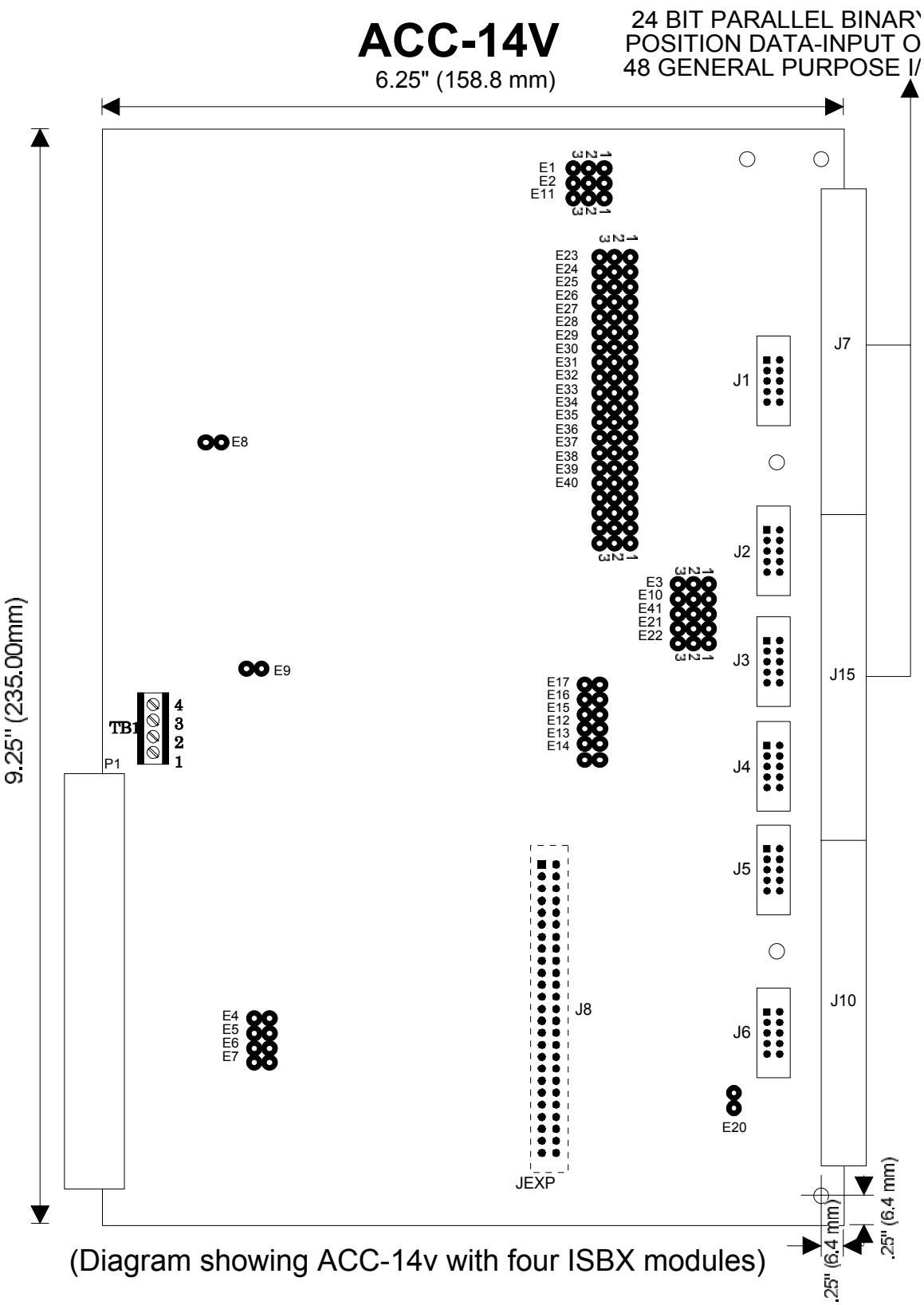


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ACC-14V
Layout of I/O Buffer Chips

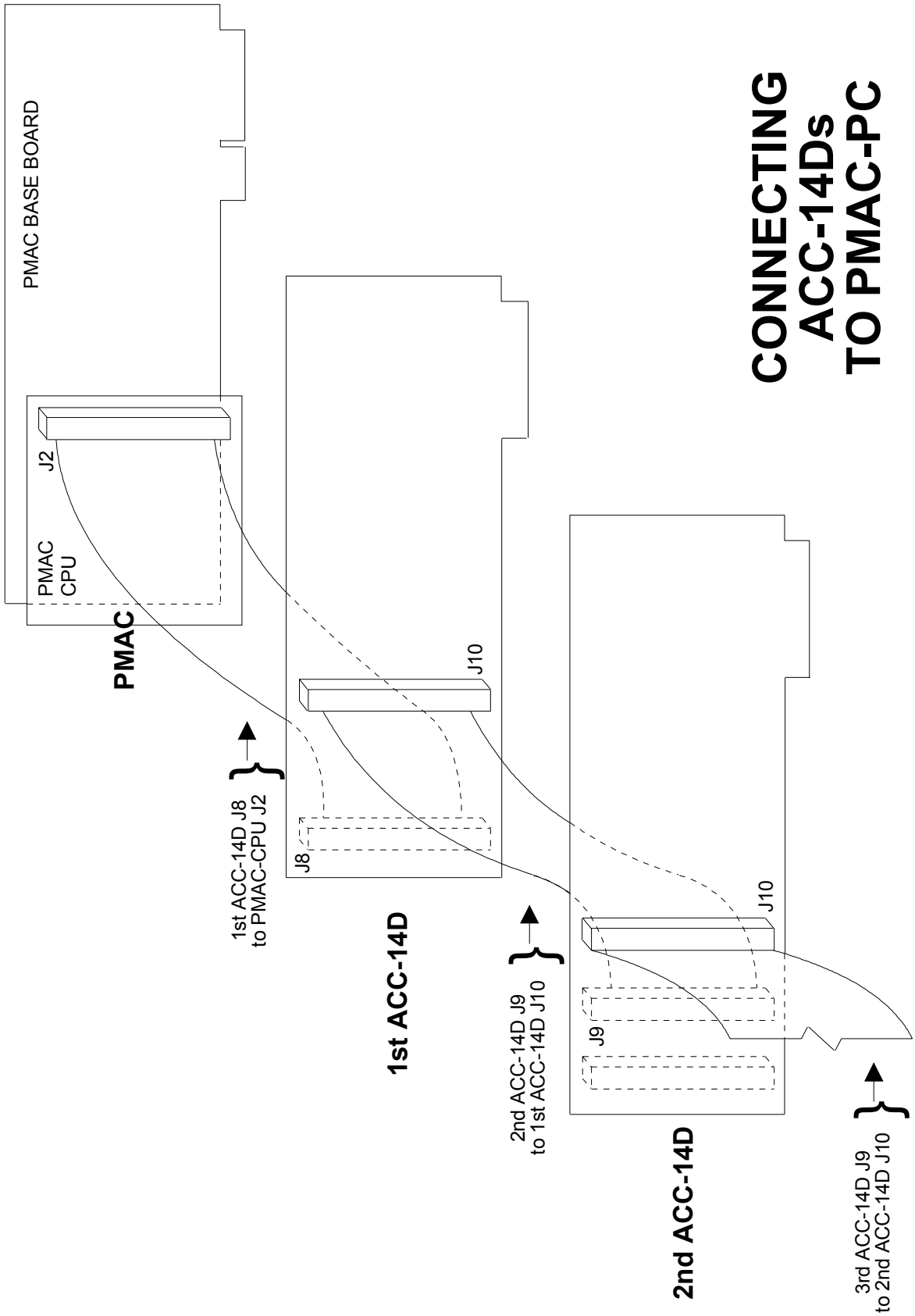


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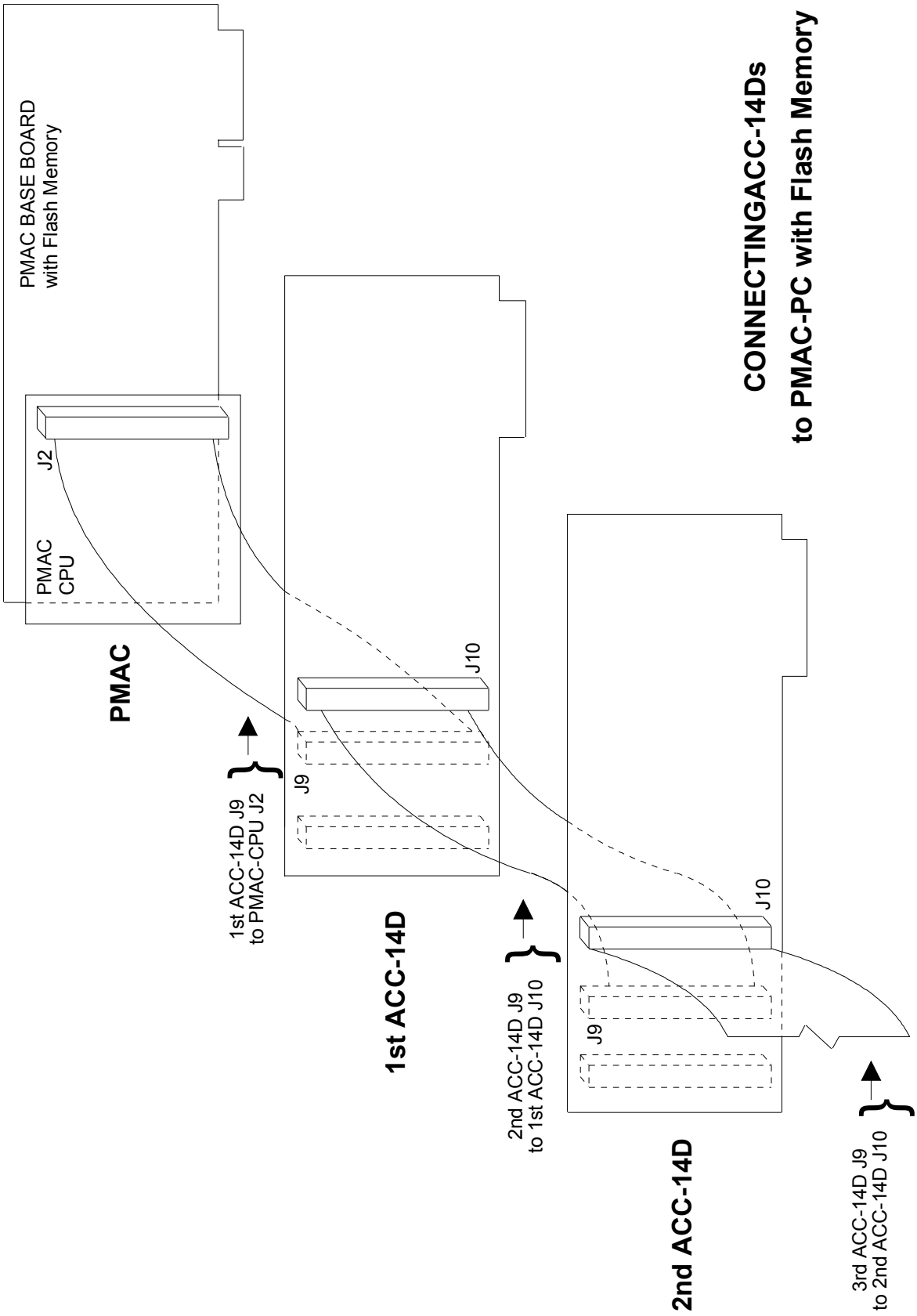


(Diagram showing ACC-14v with four ISBX modules)

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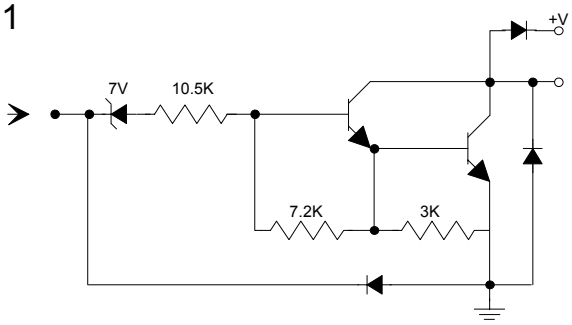
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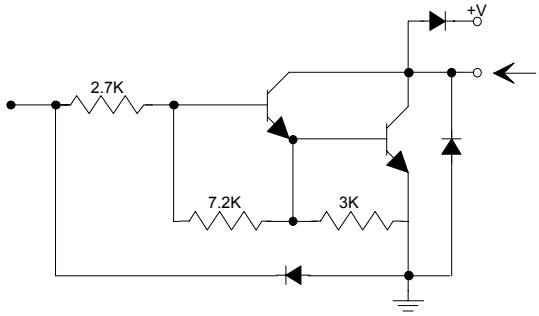
ACC-14D/V I/O OPTION SCHEMATICS

I1



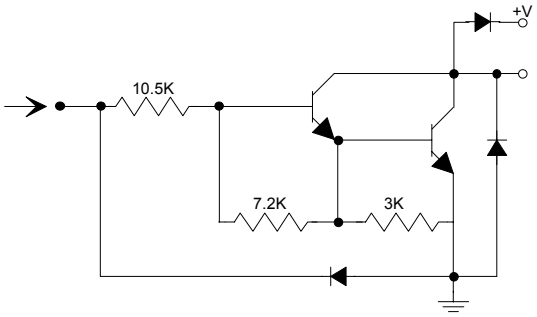
INVERTING, UNLATCHED, 14-25V

O1



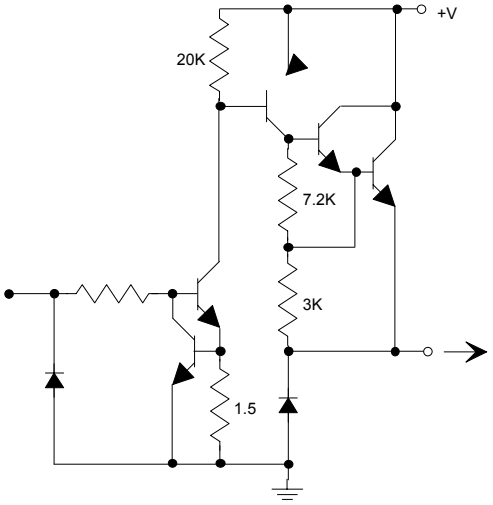
INVERTING, OPEN COLLECTOR, SINKING, 5-24V

I2



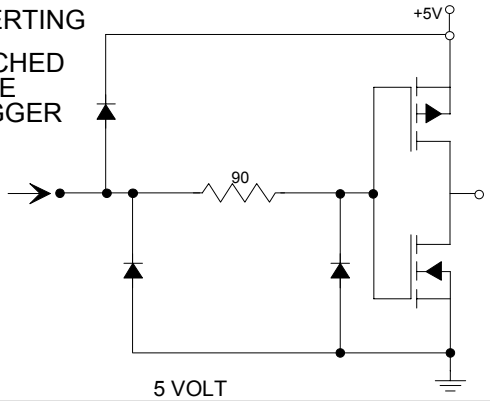
INVERTING, UNLATCHED, 6-15V

O2



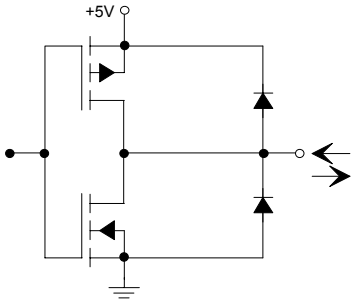
NON-INVERTING, SOURCING, 5-24V

I3. NON-INVERTING
I4. INVERTING
I5. LATCHED EDGE TRIGGER



5 VOLT

O3. NON-INVERTING
O4. INVERTING



SINKING/SOURCING, 5V

(ACC14SCH)

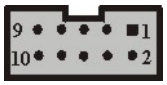
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ACC-14D/V CONNECTORS

Headers

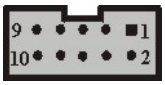
J1 (10- Pin Header)

Top View 

Pin	Symbol	Function	Description	Notes
1	RTDCA2	Output	R/D 2 Quad Channel A	
2	+5V		Positive Voltage Supply	
3	GND	Common	Ground	
4	N.C.	No Connection		
5	N.C.	No Connection		
6	GND	Common	Ground	
7	+5V		Positive Voltage Supply	
8	RTDCB2	Output	R/D 2 Quad. Channel B.	
9	+5V		Positive Voltage Supply	
10	RTDCC2	Output	R/D 2 3rd (Index) Channel	

This connector is an HP. HEDS-5000 compatible pinout of the encoder signal derived from option 6.

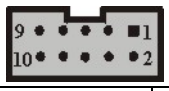
J2 (10- Pin Header)

Top View 

Pin	Symbol	Function	Description	Notes
1	RTDCA4	Output	R/D 4 Quad Channel A	
2	+5V		Positive Voltage Supply	
3	GND	Common	Ground	
4	N.C.	No Connection		
5	N.C.	No Connection		
6	GND	Common	Ground	
7	+5V		Positive Voltage Supply	
8	RTDCB4	Output	R/D 4 Quad. Channel B.	
9	+5V		Positive Voltage Supply	
10	RTDCC4	Output	R/D 4 3rd (Index) Channel	

This connector is reserved for future use.

J3 (10- Pin Header)

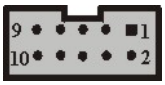
Top View 

Pin	Symbol	Function	Description	Notes
1	RTDCA1	Output	R/D 1 Quad Channel A	
2	+5V		Positive Voltage Supply	
3	GND	Common	Ground	
4	N.C.	No Connection		
5	N.C.	No Connection		
6	GND	Common	Ground	
7	+5V		Positive Voltage Supply	
8	RTDCB1	Output	R/D 1 Quad. Channel B.	
9	+5V		Positive Voltage Supply	
10	RTDCC1	Output	R/D 1 3rd (Index) Channel	

This connector is an HP. HEDS-5000 compatible pinout of the encoder signal derived from option 6.

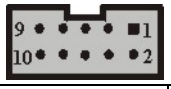
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J4 (10- Pin Header)

Top View 

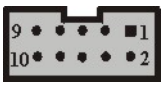
Pin	Symbol	Function	Description	Notes
1	RTDCA3	Output	R/D 3 Quad Channel A	
2	+5V		Positive Voltage Supply	
3	GND	Common	Ground	
4	N.C.	No Connection		
5	N.C.	No Connection		
6	GND	Common	Ground	
7	+5V		Positive Voltage Supply	
8	RTDCB3	Output	R/D 3 Quad. Channel B.	
9	+5V		Positive Voltage Supply	
10	RTDCC3	Output	R/D 3 3rd (Index) Channel	
This connector is reserved for future use.				

J5 (10- Pin Header)

Top View 

Pin	Symbol	Function	Description	Notes
1	RTDCA3	Output	R/D 3 Quad. Channel A	
2	RTDCB3	Output	R/D 3 Quad. Channel B	
3	RTDCC3	Output	R/D 3 3rd (Index) Channel	
4	RTDCA4	Output	R/D 4 Quad. Channel A	
5	RTDCB4	Output	R/D 4 Quad. Channel B	
6	RTDCC4	Output	R/D 4 3rd (Index) Channel	
7	N.C.			
8	N.C.			
9	SCLK	Input	Servo Clock	
10	DCLK	Input	Data Convert Clock	
This connector is a PMAC JXIO (J6) compatible pinout of the encoder signal derived from option 6.				

J6 (10- Pin Header)

Top View 

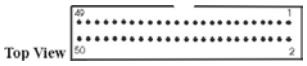
Pin	Symbol	Function	Description	Notes
1	RTDCA1	Output	R/D 1 Quad. Channel A	
2	RTDCB1	Output	R/D 1 Quad. Channel B	
3	RTDCC1	Output	R/D 1 3rd (Index) Channel	
4	RTDCA2	Output	R/D 2 Quad. Channel A	
5	RTDCB2	Output	R/D 2 Quad. Channel B	
6	RTDCC2	Output	R/D 2 3rd (Index) Channel	
7	N.C.			
8	N.C.			
9	SCLK	Input	Servo Clock	
10	DCLK	Input	Data Convert Clock	
This connector is reserved for future use.				

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J7 (50- Pin Header)			Top View 	
Pin	**Symbol**	**Function**	**Description**	**Notes**
1	MI/O23	I/O	I/O at Base Address Bit 23	
2	GND	Common	PMAC Common	
3	MI/O22	I/O	I/O at Base Address Bit 22	
4	GND	Common	PMAC Common	
5	MI/O21	I/O	I/O at Base Address Bit 21	
6	GND	Common	PMAC Common	
7	MI/O20	I/O	I/O at Base Address Bit 20	
8	GND	Common	PMAC Common	
9	MI/O19	I/O	I/O at Base Address Bit 19	
10	GND	Common	PMAC Common	
11	MI/O18	I/O	I/O at Base Address Bit 18	
12	GND	Common	PMAC Common	
13	MI/O17	I/O	I/O at Base Address Bit 17	
14	GND	Common	PMAC Common	
15	MI/O16	I/O	I/O at Base Address Bit 16	
16	GND	Common	PMAC Common	
17	MI/O15	I/O	I/O at Base Address Bit 15	
18	GND	Common	PMAC Common	
19	MI/O14	I/O	I/O at Base Address Bit 14	
20	GND	Common	PMAC Common	
21	MI/O13	I/O	I/O at Base Address Bit 13	
22	GND	Common	PMAC Common	
23	MI/O12	I/O	I/O at Base Address Bit 12	
24	GND	Common	PMAC Common	
25	MI/O11	I/O	I/O at Base Address Bit 11	
26	GND	Common	PMAC Common	
27	MI/O10	I/O	I/O at Base Address Bit 10	
28	GND	Common	PMAC Common	
29	MI/O9	I/O	I/O at Base Address Bit 9	
30	GND	Common	PMAC Common	
31	MI/O8	I/O	I/O at Base Address Bit 8	
32	GND	Common	PMAC Common	
33	MI/O7	I/O	I/O at Base Address Bit 7	
34	GND	Common	PMAC Common	
35	MI/O6	I/O	I/O at Base Address Bit 6	
36	GND	Common	PMAC Common	
37	MI/O5	I/O	I/O at Base Address Bit 5	
38	GND	Common	PMAC Common	
39	MI/O4	I/O	I/O at Base Address Bit 4	
40	GND	Common	PMAC Common	
41	MI/O3	I/O	I/O at Base Address Bit 3	
42	GND	Common	PMAC Common	
43	MI/O2	I/O	I/O at Base Address Bit 2	
44	ERR1	Input	ERROR SIGNAL	
45	MI/O1	I/O	I/O at Base Address Bit 1	
46	ICLK1	Input		
47	MI/O0	I/O	I/O at Base Address Bit 0	
48	OCLK1	Output		
49	+V	Input	12-24V for I/O Pull-Ups	
50	GND	Common		

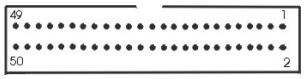
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J8 (50- Pin Header)



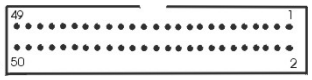
Pin	Symbol	Function	Description	Notes
1	D0	Bidirectional	PMAC Data Bus Bit 0	
2	D1	Bidirectional	PMAC Data Bus Bit 1	
3	D2	Bidirectional	PMAC Data Bus Bit 2	
4	D3	Bidirectional	PMAC Data Bus Bit 3	
5	D4	Bidirectional	PMAC Data Bus Bit 4	
6	D5	Bidirectional	PMAC Data Bus Bit 5	
7	D6	Bidirectional	PMAC Data Bus Bit 6	
8	D7	Bidirectional	PMAC Data Bus Bit 7	
9	D8	Bidirectional	PMAC Data Bus Bit 8	
10	D9	Bidirectional	PMAC Data Bus Bit 9	
11	D10	Bidirectional	PMAC Data Bus Bit 10	
12	D11	Bidirectional	PMAC Data Bus Bit 11	
13	D12	Bidirectional	PMAC Data Bus Bit 12	
14	D13	Bidirectional	PMAC Data Bus Bit 13	
15	D14	Bidirectional	PMAC Data Bus Bit 14	
16	D15	Bidirectional	PMAC Data Bus Bit 15	
17	D16	Bidirectional	PMAC Data Bus Bit 16	
18	D17	Bidirectional	PMAC Data Bus Bit 17	
19	D18	Bidirectional	PMAC Data Bus Bit 18	
20	D19	Bidirectional	PMAC Data Bus Bit 19	
21	D20	Bidirectional	PMAC Data Bus Bit 20	
22	D21	Bidirectional	PMAC Data Bus Bit 21	
23	D22	Bidirectional	PMAC Data Bus Bit 22	
24	D23	Bidirectional	PMAC Data Bus Bit 23	
25	GND	Common	PMAC Common	
26	GND	Common	PMAC Common	
27	A0	Input	PMAC Address Bus Bit 0	
28	A1	Input	PMAC Address Bus Bit 1	
29	A2	Input	PMAC Address Bus Bit 2	
30	A3	Input	PMAC Address Bus Bit 3	
31	CS02/	Input	PMAC Chip Select	
32	X/Y	Input	PMAC X/Y Select	
33	CS2/	Input	PMAC Chip Select	
34	CS3/	Input	PMAC Chip Select	
35	CS04/	Input	PMAC Chip Select	
36	CS06/	Input	PMAC Chip Select	
37	CS10/	Input	PMAC Chip Select	
38	CS11/	Input	PMAC Chip Select	
39	CS12/	Input	PMAC Chip Select	
40	CS13/	Input	PMAC Chip Select	
41	CS14/	Input	PMAC Chip Select	
42	CS16/	Input	PMAC Chip Select	
43	WR/	Input	Write Strobe, Low True	
44	RD/	Read Strobe, Low True		
45	GND	Common	PMAC Common	
46	GND	Common	PMAC Common	
47	RESET	Input	Internal Reset, High True	
48	WT/	Output	CPU Wait	
49	SER	Input	CPU Servo Clock	
50	PHA	Input	CPU Phase Clock	

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J9 (50- Pin Header)			Top View 	
Pin	**Symbol**	**Function**	**Description**	**Notes**
1	BD0	Bidirectional	Buffered Data Bus Bit 0	
2	BD1	Bidirectional	Buffered Data Bus Bit 1	
3	BD2	Bidirectional	Buffered Data Bus Bit 2	
4	BD3	Bidirectional	Buffered Data Bus Bit 3	
5	BD4	Bidirectional	Buffered Data Bus Bit 4	
6	BD5	Bidirectional	Buffered Data Bus Bit 5	
7	BD6	Bidirectional	Buffered Data Bus Bit 6	
8	BD7	Bidirectional	Buffered Data Bus Bit 7	
9	BD8	Bidirectional	Buffered Data Bus Bit 8	
10	BD9	Bidirectional	Buffered Data Bus Bit 9	
11	BD10	Bidirectional	Buffered Data Bus Bit 10	
12	BD11	Bidirectional	Buffered Data Bus Bit 11	
13	BD12	Bidirectional	Buffered Data Bus Bit 12	
14	BD13	Bidirectional	Buffered Data Bus Bit 13	
15	BD14	Bidirectional	Buffered Data Bus Bit 14	
16	BD15	Bidirectional	Buffered Data Bus Bit 15	
17	BD16	Bidirectional	Buffered Data Bus Bit 16	
18	BD17	Bidirectional	Buffered Data Bus Bit 17	
19	BD18	Bidirectional	Buffered Data Bus Bit 18	
20	BD19	Bidirectional	Buffered Data Bus Bit 19	
21	BD20	Bidirectional	Buffered Data Bus Bit 20	
22	BD21	Bidirectional	Buffered Data Bus Bit 21	
23	BD22	Bidirectional	Buffered Data Bus Bit 22	
24	BD23	Bidirectional	Buffered Data Bus Bit 23	
25	GND	Common	PMAC Common	
26	GND	Common	PMAC Common	
27	BA0	Input	Buffered Address Bus Bit 0	
28	BA1	Input	Buffered Address Bus Bit 1	
29	BA2	Input	Buffered Address Bus Bit 2	
30	BA3	Input	Buffered Address Bus Bit 3	
31	CS02	Input	PMAC Chip Select	
32	BX/Y	Input	Buff. X/Y Select	
33	CS2/	Input	PMAC Chip Select	
34	CS3/	Input	PMAC Chip Select	
35	CS04/	Input	PMAC Chip Select	
36	CS05/	Input	PMAC Chip Select	
37	CS10/	Input	PMAC Chip Select	
38	CS11/	Input	PMAC Chip Select	
39	CS12/	Input	PMAC Chip Select	
40	CS13/	Input	PMAC Chip Select	
41	CS14/	Input	PMAC Chip Select	
42	CS15/	Input	PMAC Chip Select	
43	BWR/	Input	Buff. Write Strobe, Low True	
44	BRD/	Input	Buff. Read Strobe, Low True	
45	GND	Common	PMAC Common	
46	GND	Common	PMAC Common	
47	BRST	Input	Buffered Reset, High True	
48	WT/	Output	CPU Wait	
49	SER	Input	CPU Servo Clock	
50	PHA	Input	CPU Phase Clock	

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J10 (50- Pin Header)

Top View 

Pin	Symbol	Function	Description	Notes
1	BD0	Bidirectional	Buffered Data Bus	
2	BD1	Bidirectional	Buffered Data Bus	
3	BD2	Bidirectional	Buffered Data Bus	
4	BD3	Bidirectional	Buffered Data Bus	
5	BD4	Bidirectional	Buffered Data Bus	
6	BD5	Bidirectional	Buffered Data Bus	
7	BD6	Bidirectional	Buffered Data Bus	
8	BD7	Bidirectional	Buffered Data Bus	
9	BD8	Bidirectional	Buffered Data Bus	
10	BD9	Bidirectional	Buffered Data Bus	
11	BD10	Bidirectional	Buffered Data Bus	
12	BD11	Bidirectional	Buffered Data Bus	
13	BD12	Bidirectional	Buffered Data Bus	
14	BD13	Bidirectional	Buffered Data Bus	
15	BD14	Bidirectional	Buffered Data Bus	
16	BD15	Bidirectional	Buffered Data Bus	
17	BD16	Bidirectional	Buffered Data Bus	
18	BD17	Bidirectional	Buffered Data Bus	
19	BD18	Bidirectional	Buffered Data Bus	
20	BD19	Bidirectional	Buffered Data Bus	
21	BD20	Bidirectional	Buffered Data Bus	
22	BD21	Bidirectional	Buffered Data Bus	
23	BD22	Bidirectional	Buffered Data Bus	
24	BD23	Bidirectional	Buffered Data Bus	
25	GND	Common	PMAC Common	
26	GND	Common	PMAC Common	
27	BA0	Output	Buffered Address Bus Bit 0	
28	BA1	Output	Buffered Address Bus Bit 1	
29	BA2	Output	Buffered Address Bus Bit 2	
30	BA3	Output	Buffered Address Bus Bit 3	
31	CS02	Output	PMAC Chip Select	
32	BX/Y	Output	Buff. X/Y Select	
33	CS2/	Output	PMAC Chip Select	
34	CS3/	Output	PMAC Chip Select	
35	CS04/	Output	PMAC Chip Select	
36	CS06/	Output	PMAC Chip Select	
37	CS10/	Output	PMAC Chip Select	
38	CS11/	Output	PMAC Chip Select	
39	CS12/	Output	PMAC Chip Select	
40	CS13/	Output	PMAC Chip Select	
41	CS14/	Output	PMAC Chip Select	
42	CS16/	Output	PMAC Chip Select	
43	BWR/	Buff. Write Strobe		
44	BRD/	Buff. Read Strobe		
45	GND	Common	PMAC Common	
46	GND	Common	PMAC Common	
47	BRST	Output	Buffered Reset	
48	WT/	Input	CPU Wait	
49	SER	Output	CPU Servo Clock	
50	PHA	Output	CPU Phase Clock	

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J15 (50-Pin Header)			Top View 	
Pin	**Symbol**	**Function**	**Description**	**Notes**
1	MI/O47	I/O	I/O Base Address+1, Bit 23	
2	GND	Common	PMAC Common	
3	MI/O46	I/O	I/O Base Address+1, Bit 22	
4	GND	Common	PMAC Common	
5	MI/O45	I/O	I/O Base Address+1, Bit 21	
6	GND	Common	PMAC Common	
7	MI/O44	I/O	I/O Base Address+1, Bit 20	
8	GND	Common	PMAC Common	
9	MI/O43	I/O	I/O Base Address+1, Bit 19	
10	GND	Common	PMAC Common	
11	MI/O42	I/O	I/O Base Address+1, Bit 18	
12	GND	Common	PMAC Common	
13	MI/O41	I/O	I/O Base Address+1, Bit 17	
14	GND	Common	PMAC Common	
15	MI/O40	I/O	I/O Base Address+1, Bit 16	
16	GND	Common	PMAC Common	
17	MI/O39	I/O	I/O Base Address+1, Bit 15	
18	GND	Common	PMAC Common	
19	MI/038	I/O	I/O Base Address+1, Bit 14	
20	GND	Common	PMAC Common	
21	MI/O37	I/O	I/O Base Address+1, Bit 13	
22	GND	Common	PMAC Common	
23	MI/O36	I/O	I/O Base Address+1, Bit 12	
24	GND	Common	PMAC Common	
25	MI/O35	I/O	I/O Base Address+1, Bit 11	
26	GND	Common	PMAC Common	
27	MI/O34	I/O	I/O Base Address+1, Bit 10	
28	GND	Common	PMAC Common	
29	MI/O33	I/O	I/O Base Address+1, Bit 9	
30	GND	Common	PMAC Common	
31	MI/O32	I/O	I/O Base Address+1, Bit 8	
32	GND	Common	PMAC Common	
33	MI/O31	I/O	I/O Base Address+1, Bit 7	
34	GND	Common	PMAC Common	
35	MI/O30	I/O	I/O Base Address+1, Bit 6	
36	GND	Common	PMAC Common	
37	MI/O29	I/O	I/O Base Address+1, Bit 5	
38	GND	Common	PMAC Common	
39	MI/O28	I/O	I/O Base Address+1, Bit 4	
40	GND	Common	PMAC Common	
41	MI/O27	I/O	I/O Base Address+1, Bit 3	
42	GND	Common	PMAC Common	
43	MI/O26	I/O	I/O Base Address+1, Bit 2	
44	ERR2	Input		
45	MI/O25	I/O	I/O Base Address+1, Bit 1	
46	ICLK2	Input		
47	MI/O24	I/O	I/O Base Address+1, Bit 0	
48	OCLK2	Output		
49	+V	Input	12-24V for I/O Pull-Ups	
50	GND	Common		

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E-POINT JUMPERS

The E-Point jumper table is broken into four sections: global, port, byte and Acc-14 Option 6 jumpers

Global E-Points

Jumper	On/off	Description
E20		Should be ON for daisy-chained Acc-14s
		Should be OFF for Acc-14 which plugs into PMAC
E12-E17		Determine the cards address in PMAC's memory and I/O space. Only one of these jumpers should be ON on each Acc-14, and each Acc-14 should have a different jumper ON.

Port E-Points

Jumper	On/off	Description
E4		ON allows a low ERR1/ input to disable the port A strobe
E5		ON passes the ICLK1 input from J7 uninverted to latch port A I/O OFF passes the ICLK1 input from J7 inverted to latch port A I/O
E6		ON passes the ICLK2 input from J15 uninverted to latch port B I/O passes the ICLK2 input OFF from J15 inverted to latch port B I/O
E7		ON allows a low ERR1/ input to disable the port B strobe
E8		ON signal high for port A at all times forces strobe OFF latched input signal for port A, i.e. absolute encoder
E9		ON signal high for port B at all times forces strobe OFF latched input signal for port B, i.e. absolute encoder
E21		Controls whether the servo clock signal is passed to OCLK1 (J7) inverted (1 to 2) or non-inverted (2 to 3)
E22		Controls whether the servo clock signal is passed to OCLK2 (J15) inverted (1 to 2) or non-inverted (2 to 3)

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Byte E-Points

Jumper	On/off	Description
E2		Byte 1 Pull up (1 to 2)/Pull down (2 to 3)
E31		Byte 1 Pin 10 Level Select. (1 to 2) sinking (2 to 3) sourcing
E27		Byte 1 Pin 11 Level or Strobe. (1 to 2) level (2 to 3) strobe
E28		Byte 1 Pin 11 Level Select. (1 to 2) sinking (2 to 3) sourcing
E1		Byte 2 Pull up (1 to 2)/Pull down (2 to 3)
E30		Byte 2 Pin 10 Level Select. (1 to 2) sinking (2 to 3) sourcing
E25		Byte 2 Pin 11 Level or Strobe. (1 to 2) level (2 to 3) strobe
E26		Byte 2 Pin 11 Level Select. (1 to 2) sinking (2 to 3) sourcing
E11		Byte 3 Pull up (1 to 2)/Pull down (2 to 3)
E29		Byte 3 Pin 10 Level Select. (1 to 2) sinking (2 to 3) sourcing
E23		Byte 3 Pin 11 Level or Strobe. (1 to 2) level (2 to 3) strobe
E24		Byte 3 Pin 11 Level Select. (1 to 2) sinking (2 to 3) sourcing
E10		Byte 4 Pull up (1 to 2)/Pull down (2 to 3)
E38		Byte 4 Pin 10 Level Select. (1 to 2) sinking (2 to 3) sourcing
E32		Byte 4 Pin 11 Level or Strobe. (1 to 2) level (2 to 3) strobe
E33		Byte 4 Pin 11 Level Select. (1 to 2) sinking (2 to 3) sourcing
E41		Byte 5 Pull up (1 to 2)/Pull down (2 to 3)
E39		Byte 5 Pin 10 Level Select. (1 to 2) sinking (2 to 3) sourcing
E34		Byte 5 Pin 11 Level or Strobe. (1 to 2) level (2 to 3) strobe
E35		Byte 5 Pin 11 Level Select. (1 to 2) sinking (2 to 3) sourcing
E3		Byte 6 Pull up (1 to 2)/Pull down (2 to 3)
E40		Byte 6 Pin 10 Level Select. (1 to 2) sinking (2 to 3) sourcing
E36		Byte 6 Pin 11 Level or Strobe. (1 to 2) level (2 to 3) strobe
E37		Byte 6 Pin 11 Level Select. (1 to 2) sinking (2 to 3) sourcing

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Option 6 E-Points

Option 6 Jumpers: The following jumpers are only used in conjunction with Acc-14D/V Option 6 (quadrature generation): E42-E45; E50-E57		
Jumper	**On/off**	**Description**
E42		Jump pins 1 to 2 to bring synthesized quadrature A signal from Port A to output connectors Remove jumper to not bring this signal to output connectors
E43		Jump pins 1 to 2 to bring synthesized quadrature B signal from Port A to output connectors Remove jumper to not bring this signal to output connectors
E44		Jump pins 1 to 2 to bring synthesized quadrature A signal from Port B to output connectors Remove jumper to not bring this signal to output connectors
E45		Jump pins 1 to 2 to bring synthesized quadrature B signal from Port B to output connectors Remove jumper to not bring this signal to output connectors
E50		Jump pins 1 to 2 to use MI/O0 as LSB for quadrature synthesis on Port A Jump pins 2 to 3 to use MI/O2 as LSB for quadrature synthesis on Port A Remove jumper to use MI/O4 or MI/O6 for this (see E52)
E51		Jump pins 1 to 2 to use MIO1 as MSB for quadrature synthesis on Port A Jump pins 2 to 3 to use MI/O3 as MSB for quadrature synthesis on Port A Remove jumper to use MI/O5 or MI/O7 for this (see E53)
E52		Jump pins 1 to 2 to use MI/O4 as LSB for quadrature synthesis on Port A Jump pins 2 to 3 to use MI/O6 as LSB for quadrature synthesis on Port A Remove jumper to use MI/O0 or MI/O2 for this (see E50)
E53		Jump pins 1 to 2 to use MIO5 as MSB for quadrature synthesis on Port A Jump pins 2 to 3 to use MI/O7 as MSB for quadrature synthesis on Port A Remove jumper to use MI/O1 or MI/O3 for this (see E51)
E54		Jump pins 1 to 2 to use MI/O24 as LSB for quadrature synthesis on Port B Jump pins 2 to 3 to use MI/O26 as LSB for quadrature synthesis on Port B Remove jumper to use MI/O28 or MI/O30 for this (see E56)
E55		Jump pins 1 to 2 to use MIO25 as MSB for quadrature synthesis on Port B Jump pins 2 to 3 to use MI/O27 as MSB for quadrature synthesis on Port B Remove jumper to use MI/O29 or MI/O31 for this (see E57)
E56		Jump pins 1 to 2 to use MI/O28 as LSB for quadrature synthesis on Port B Jump pins 2 to 3 to use MI/O30 as LSB for quadrature synthesis on Port B Remove jumper to use MI/O24 or MI/O26 for this (see E54)
E57		Jump pins 1 to 2 to use MIO29 as MSB for quadrature synthesis on Port B Jump pins 2 to 3 to use MI/O31 as MSB for quadrature synthesis on Port B Remove jumper to use MI/O25 or MI/O27 for this (see E55)

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