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HARDWARE REFERENCE MANUAL

Flex CPU Piggyback Board

CPU

3xx-603605-xHxx

December 8 2003

DELTA TAU
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Operating Conditions

All Delta Tau Data Systems, Inc. motion controller products, accessories, and amplifiers contain static sensitive components that can be damaged by incorrect handling. When installing or handling Delta Tau Data Systems, Inc. products, avoid contact with highly insulated materials. Only qualified personnel should be allowed to handle this equipment.

In the case of industrial applications, we expect our products to be protected from hazardous or conductive materials and/or environments that could cause harm to the controller by damaging components or causing electrical shorts. When our products are used in an industrial environment, install them into an industrial electrical cabinet or industrial PC to protect them from excessive or corrosive moisture, abnormal ambient temperatures, and conductive materials. If Delta Tau Data Systems, Inc. products are directly exposed to hazardous or conductive materials and/or environments, we cannot guarantee their operation.

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SCHEMATICS

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INTRODUCTION

The Flex CPU piggyback board (Part # 300-603605-10x) for the PMAC/PMAC2 and Turbo PMAC/PMAC2 families of boards provides new high-end capabilities for these controllers and uses newer components with longer product lifetimes. It can be manufactured in a wide variety of configurations, and can be used in the following products:

- PMAC(1)-PC
- PMAC(1)-PCI
- PMAC(1)-VME
- PMAC2-PC
- PMAC2-PCI
- PMAC2-VME
- Turbo PMAC(1)-PC
- Turbo PMAC(1)-PCI
- Turbo PMAC(1)-VME
- Turbo PMAC2-PC
- Turbo PMAC2-PCI
- Turbo PMAC2-VME

On the regular (non-Turbo) PMAC(1) and PMAC2 boards, the Flex CPU is provided automatically when any of the following CPU options are ordered:

- Option 5AF: 40 MHz CPU with 128k x 24 internal SRAM
- Option 5CF: 80 MHz CPU with 128k x 24 internal SRAM
- Option 5EF: 160 MHz CPU with 128k x 24 internal SRAM

The Flex CPU board is not provided if Option 4x or 5x is not ordered, or if Option 4A, 5A, 5B, or 5C is ordered.

On Turbo PMAC(1) and Turbo PMAC2 boards, the Flex CPU may be provided when any of the following CPU options is ordered:

- Option 5C0: 80 MHz DSP56303 CPU with 8k x 24 internal SRAM, 256k x 24 external SRAM
- Option 5C3: 80 MHz DSP56303 CPU with 8k x 24 internal SRAM, 1M x 24 external SRAM
- Option 5D0: 100 MHz DSP56309 CPU with 34k x 24 internal SRAM, 256k x 24 external SRAM
- Option 5D3: 100 MHz DSP56309 CPU with 34k x 24 internal SRAM, 1M x 24 external SRAM

In these cases, however, the older Turbo only CPU piggyback board may also be provided.

On Turbo PMAC(1) and Turbo PMAC2 boards, the Flex CPU will be provided automatically when either of the following CPU options is ordered:

- Option 5E0: 160 MHz DSP56309 CPU with 128k x 24 internal SRAM, 256k x 24 external SRAM
- Option 5E3: 160 MHz DSP56309 CPU with 128k x 24 internal SRAM, 1M x 24 external SRAM

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BOARD CONFIGURATION

Non-Turbo CPU Base Configuration

When assembled for a non-Turbo CPU, the DSP IC in U1 of the Flex CPU board contains all of the memory required for operation. Therefore, there are no ICs installed in the locations for external RAM: U11, U12, U13, U14, U15, and U16.

The CPU is available in several speed options: 40 MHz (Option 5AF), 80 MHz (Option 5CF), and 160 MHz (Option 5EF). The maximum frequency of operation is indicated with a sticker on the CPU in U1.

When the Flex CPU is built for ISA-bus or VME-bus baseboards, the P3 connector consists of a 36-pin header on the solder side for direct connection to the baseboard, and a 10-pin header on the component side for cable connection of the extra signals required for dual-ported RAM interface. When the Flex CPU is built for PCI-bus baseboards the P3 connector consists only of a 56-pin header on the solder side for direct connection of all signals to the baseboard.

Non-Turbo CPU Further Options

The Option 16 battery-backed parameter RAM provides a bank of non-volatile memory for the controller. Its key components are RAM ICs in U17, U18, and U19, and a battery in BT1

Turbo CPU Base Configuration

When assembled for a Turbo CPU section, the Flex CPU board contains external RAM ICs in locations U11, U12, U13, U14, U15, U16. With the standard memory configuration (Option 5x0), these ICs fill the smaller footprint in these locations, leaving an open pin on the board on each end of each side.

When the Flex CPU is built for ISA-bus or VME-bus baseboards, the P3 connector consists of a 36-pin header on the solder side for direct connection to the baseboard, and a 10-pin header on the component side for cable connection of the extra signals required for dual-ported RAM interface. When the Flex CPU is built for PCI-bus baseboards the P3 connector consists only of a 56-pin header on the solder side for direct connection of all signals to the baseboard.

Turbo CPU Further Options

If an expanded memory configuration (Option 5x3) is ordered, larger RAM ICs are installed in locations U11, U12, U13, U14, U15, U16, occupying the full footprints in these locations

If the Option 9T auxiliary serial port is ordered for the Turbo PMAC controller, an RS-232 serial port is provided on the CPU board to supplement the serial port on the baseboard. The key components are ICs in U28 and U29, and the connector J8.

The Option 16A battery-backed parameter RAM provides a bank of non-volatile memory for the controller. Its key components are RAM ICs in U17, U18, and U19, and a battery in BT1

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HARDWARE SETUP

Flex CPU Board Jumper Configuration

Watchdog Timer Jumper

Jumper E1 on the Turbo CPU board must be OFF for the watchdog timer to operate. This is a very important safety feature, so it is vital that this jumper be OFF in normal operation. E1 should be put ON only to debug problems with the watchdog timer circuit.

Dual-Ported RAM Source Jumper

Jumper E2 must connect pins 1 and 2 to access dual-ported RAM (non-Turbo addresses $Dxxx, Turbo addresses $06xxxx) from the baseboard. If it is desired to use the Option 2 DPRAM on the baseboard, jumper E2 must be in this setting. All Delta Tau base boards except the PMAC(1)-PC board have the option for installing DPRAM on the base board.

Jumper E2 must connect pins 2 and 3 to access dual-ported RAM (non-Turbo addresses $Dxxx, Turbo addresses $06xxxx) through the JEXP expansion port. If it is desired to use DPRAM on an external accessory board, jumper E2 must be in this setting. The PMAC(1)-PC base board (part # 602191-10x) does not have the option for installing on-board DPRAM; it requires the external Option 2 DPRAM board (part #602240-10x) for this functionality. Use of this DPRAM board, interfacing through the JEXP port, requires E2 to connect pins 2 and 3.

Power-Up State Jumpers

Jumper E4 on the Turbo CPU board must be OFF, jumper E5 must be ON, and jumper E6 must be ON, in order for the CPU to copy the firmware from flash memory into active RAM on power-up/reset. This is necessary for normal operation of the card. (Other settings are for factory use only.)

Firmware Load Jumper

If jumper E7 on the CPU board is ON during power-up/reset, the board comes up in “bootstrap mode,” which permits loading new firmware into the flash-memory IC on the board. When the PMAC Executive program tries to establish communications with a board in this mode, it will automatically detect that the board is in bootstrap mode and ask you what file you want to download as the new firmware.

Jumper E7 must be OFF during power-up/reset for the board to come up in normal “operational mode.”

Flash Memory Bank Select Jumpers

The flash-memory IC in location U10 on the Flex CPU board has the capacity for eight separate banks of firmware, only one of which can be used at any given time. The eight combinations of settings for jumpers E10A, E10B, and E10C select which bank of the flash memory is used. In the factory production process, firmware is loaded only into Bank 0, which is selected by having all of these jumpers OFF.

Installation

The Flex CPU board installs on the base controller board using the P1 and P3 stack connectors on the solder side of the CPU board. The CPU board can be further secured to the base board with a standoff and screw through the central hole. When a complete PMAC or Turbo PMAC controller is purchased, this assembly is done at the factory. In the case of retrofits or updates to existing controllers, this assembly is easy to do in the field.

ESD Warning: The Flex CPU board and PMAC controller boards contain static-sensitive components. Make sure proper ESD protection is employed.

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OPERATION OF THE FLEX CPU

Operation as Non-Turbo CPU

When used as a non-Turbo CPU, the Flex CPU board operates in a manner that is fundamentally compatible with older CPU designs. However, there are a few issues to note:

- The Flex CPU requires the use of V1.17 or newer firmware. There are few differences between the previous V1.16H firmware and the V1.17 firmware other than the addition of internal support for the Flex CPU design.
- Due to more advanced processor logic and the internal integration of all memory, the Flex CPU will operate significantly faster than older non-Turbo CPU designs, *even for equivalent CPU frequencies*. The Flex CPU in a non-Turbo configuration will generally operate more than twice as fast as older non-Turbo CPUs running at the same frequency.

  This will result in significantly faster cycle times for background tasks such as PLC programs (the frequency of interrupt-driven foreground tasks is not affected, although the increased computational speeds permit higher frequencies for these tasks). Generally, this will not be a problem, but if existing programs controlled timing by computational delay (e.g. number of loops waiting), operational differences may occur.
- The operational frequency of the CPU can now be set in software by new variable I46. If this variable is set to 0, PMAC firmware looks at the jumpers (E48 on a PMAC(1), E2 and E4 on a PMAC2) to set the operational frequency, retaining backward compatibility for 40, 60, and 80 MHz operation.. If I46 is set to a value greater than 0, the operational frequency is set to 10MHz * (I46 + 1), regardless of the jumper setting. If the desired operational frequency is higher than the maximum rated frequency for that CPU, the operational frequency will be reduced to the rated maximum. It is always possible to operate the Flex CPU board at a frequency below its rated maximum.

  On a Flex CPU board configured for Option 5AF with 40 MHz maximum frequency, I46 should be set to 3 to operate the CPU at its maximum rated frequency.

  On a Flex CPU board configured for Option 5CF with 80 MHz maximum frequency, I46 should be set to 7 to operate the CPU at its maximum rated frequency.

  On a Flex CPU board configured for Option 5EF with 160 MHz maximum frequency, I46 should be set to 15 to operate the CPU at its maximum rated frequency.

  I46 is only used at power-up/reset, so to change the operational frequency, set a new value of I46, issue a **SAVE** command to store this value in non-volatile flash memory, then issue a **$$$** command to reset the controller.

  To determine the frequency at which the CPU is actually operating, issue the **TYPE** command to the PMAC. The PMAC will respond with five data items, the last of which is `CLK Xn`, where *n* is the multiplication factor from the 20 MHz crystal frequency (not 10 MHz). *n* should be equivalent to (I46+1)/2 if I46 is not requesting a frequency greater than the maximum rated for that CPU board. *n* will be “2” for 40 MHz operation, 4 for 80 MHz operation, and 8 for 160 MHz operation.
- If the CPU’s operational frequency has been determined by (a non-zero setting of) I46, the serial communications baud rate is determined at power-up/reset by variable I54 alone according to the following table:

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I54	Baud Rate	I54	Baud Rate
0	600	8	9600
1	900	9	14,400
2	1200	10	19,200
3	1800	11	28,800
4	2400	12	38,400
5	3600	13	57,600
6	4800	14	76,800
7	7200	15	115,200

Note that these values can be different from those used on PMAC2 boards with jumper-set CPU frequencies (see below).

- If the saved value of I46 is 0, so the CPU's operational frequency is determined by jumper settings, then the serial baud rate is determined by a combination of the setting of jumpers E44-E47 and the CPU frequency on a PMAC(1) board, as shown in the following table. These settings maintain backward compatibility.

E44	E45	E46	E47	Baud Rate for 20MHz	Baud Rate for 40MHz	Baud Rate for 60MHz
N	ON	ON	ON	Disabled	Disabled	Disabled
OFF	ON	ON	ON	300	600	900
ON	OFF	ON	ON	400*	800*	1200
OFF	OFF	ON	ON	600	1200	1800
ON	ON	OFF	ON	800*	1600*	2400
OFF	ON	OFF	ON	1200	2400	3600
ON	OFF	OFF	ON	1600*	3200*	4800
OFF	OFF	OFF	ON	2400	4800	7200
ON	ON	ON	OFF	3200*	6400*	9600
OFF	ON	ON	OFF	4800	9600	14400
ON	OFF	ON	OFF	6400*	12800*	19200
OFF	OFF	ON	OFF	9600	19200	28800
ON	ON	OFF	OFF	12800*	25600*	38400
OFF	ON	OFF	OFF	19200	38400	57600
ON	OFF	OFF	OFF	25600*	51200*	76800
OFF	OFF	OFF	OFF	38400	76800	115200
* Not an exact baud rate						

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For a PMAC2 board with a saved value of 0 for I46, the serial baud rate is determined by the combination of I54 and the CPU frequency on a PMAC2 board as shown in the following table. These settings maintain backward compatibility.

I54	Baud Rate for 40 MHz CPU	Baud Rate for 60 MHz CPU	Baud Rate for 80 MHz CPU
0	600	Disabled	1200
1	900* (-0.05%)	900	1800* (-0.1%)
2	1200	1200	2400
3	1800* (-0.1%)	1800	3600* (-0.19%)
4	2400	2400	4800
5	3600* (-0.19%)	3600	7200* (-0.38%)
6	4800	4800	9600
7	7200* (-0.38%)	7200	14,400*(-0.75%)
8	9600	9600	19,200
9	14,400*(-0.75%)	14,400	28,800*(-1.5%)
10	19,200	19,200	38,400
11	28,800*(-1.5%)	28,800	57,600*(-3.0%)
12	38,400	38,400	76,800
13	57,600*(-3.0%)	57,600	115,200*(-6.0%)
14	76,800	76,800	153,600
15	Disabled	115,200	DISABLED
* Not an exact baud rate			

- With the Flex CPU, the card number (0 – 15) for serial addressing of multiple cards on a daisy-chain serial cable is determined by variable I0, even on PMAC(1) boards. This has always been the case for PMAC2 boards, but with other CPU boards, the card number on PMAC(1) boards has been determined by the settings of jumpers E40 – E43. Jumpers E40 – E43 on a PMAC(1) board with the Flex CPU still determine the "direction" of the phase and servo clocks: all of these jumpers must be ON for the card to use its internally generated clock signals and to output these on the serial port connector; if any of these jumpers is OFF, the card will expect to input these clock signals from the serial port connector, and its watchdog timer will trip immediately if it does not receive these signals.

Operation as a Turbo CPU

When used as a Turbo CPU, the Flex CPU is fully compatible with older CPU designs. It does permit higher-speed configurations (Option 5Ex at 160 MHz), which offer significantly higher performance both due to increased operation frequency and added internal memory.

Variable I52 determines the actual operating frequency of the Turbo CPU. The operational frequency is set to 10MHz * (I52 + 1). I52 should be set to 7 to operate an Option 5Cx board at its maximum rated frequency of 80 MHz; it should be set to 9 to operate an Option 5Dx board at its maximum rated frequency of 100 MHz; it should be set to 15 to operate an Option 5Ex board at is maximum rated frequency of 160 MHz.

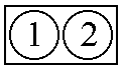
I52 is used only at power-up/reset, so to change the operational frequency, set a new value of I52, issue a **SAVE** command to store this value in non-volatile flash memory, then issue a **$$$** command to reset the controller.

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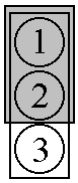
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FLEX CPU BOARD JUMPER DESCRIPTIONS

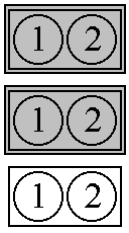
E1: Watchdog Disable Jumper

E Point and Physical Layout	Description	Default
E1 	Jump pin 1 to 2 to disable Watchdog timer (for test purposes only). Remove jumper to enable Watchdog timer.	No jumper installed

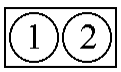
E2: Dual-Ported RAM Port Select

E Point and Physical Layout	Description	Default
E2 	Jump pin 1 to 2 to access DPRAM from baseboard. Jump pin 2 to 3 to access DPRAM through JEXP expansion port (PMAC(1)-PC with Option 2 DPRAM board).	Pins 2 and 3 jumpered (with PMAC(1)-PC base board only) Pins 1 and 2 jumpered (when used on all other base boards)

E4 – E6: Power-Up/Reset Load Source

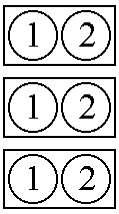
E Point and Physical Layout	Description	Default
E6  **E4**	Remove jumper E4; jump E5 pin 1 to 2; jump E6 pin 2 to 3; to read flash IC on power-up/reset Other combinations are for factory use only; the board will not operate in any other configuration.	No E4 jumper installed; E5 and E6 jump pin 1 to 2

E7: Firmware Reload Enable

E Point and Physical Layout	Description	Default
E7 	Jump pin 1 to 2 to reload firmware through serial or bus port. Remove jumper for normal operation.	No jumper installed

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E10A, B, C: Flash Memory Bank Select

E Point and Physical Layout	Description	Default
E10A  **E10C**	Remove all 3 jumpers to select flash memory bank with factory-installed firmware. Use other configuration to select one of the 7 other flash memory banks	No jumpers installed

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CONNECTOR SUMMARY

J2: JEXP Expansion Port (50-pin IDC header for Delta Tau accessory boards)

J5: JTAG/OnCE Port (for factory use only)

J6: JSIO Port (for factory use only)

J7: JISP Port (for factory use only)

J8: Auxiliary Serial Port (10-pin IDC header)*

P1: Stack Connector (Internal connections to main PMAC board)

P3: Stack Connector (Internal connections to main PMAC board)

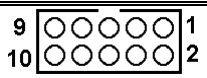
*Pinout shown in next section

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CONNECTOR PINOUTS

J8 JRS232 (10-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	N.C.		No Connect	
2	DTR	Bidirect	Data Terminal Ready	Tied to DSR
3	TXD/	Input	Receive Data	Host transmit data
4	CTS	Input	Clear to Send	Host ready bit
5	RXD/	Output	Send Data	Host receive data
6	RTS	Output	Request to Send	PMAC ready bit
7	DSR	Bidirect	Data Set Ready	Tied to DTR
8	N.C.		No Connect	
9	GND	Common	PMAC Common	
10	+5V	Output	+5VDC Supply	Power supply out

The JRS232 connector provided with Option 9T on a Turbo PMAC is an auxiliary serial port that can be used independently of the standard main serial port and other communications ports. It can be connected with a straight-across flat cable to a DB-9 connector with the standard RS-232 pinout.

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NOTE1: INSTALL 'F2' ONLY FOR DSP56303PW80' DO NOT INSTALL 'VR1,C89,C90,R11,R12' FOR DSP56309PW80'

NOTE2: INSTALL 'VR1,C89,C90,R11,R12' FOR DSP56309PW80' AND 'SP5631GC150' DO NOT INSTALL 'F2'

VR2 LM1117MPX-1.8 MC33269ST-1.8 (SOT-223) C89 10UF 16V (TANT) C90 10UF 16V (TANT)

VR1 LM1117MPX-3.3 MC33269ST-3.3 (SOT-223) C37 10UF 16V (TANT) C38 10UF 16V (TANT)

Y3 C-002RX 32.768Khz Vbat U5 DS2415P (TSOC) C104 .1UF

(Request 6pf load capacitance) (See layout instructions)

NETLIST CHANGE

RESET- PINIT TRST- MODD/IRQD- MODC/IRQC- MODB/IRQB- MODA/IRQA- DE- TA- TMS TCK TDO TDI BSC12 BSC11 BSTD1 BSRD1 SC02 SC01

F2 55FZ103N NOTE1: VCCQL

C7 C8 C9 C10 C11 C12 C13 C14 .1UF

C3 C4 C5 C6 .1UF

+3P3V GND

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A15X/YP WR- RD-

D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23

NOTE: THIS PART MUST BE 'MAX3232ECWE' TO PROVIDE ESD* PROTECTION OF THE 'RS232' INPUT SECTION.

+3P3V C76 .1UF C72 .1UF C73 .1UF U29 MAX3232ECWE (SOL16) C74 1UF C75 1UF +5V

J8 DB9(RS232) 1 N.C. 2 TXD- 3 RXD- 4 RTS- 5 CTS- 6 N.C. 7 +5V 8 9 10 HEADER 10 (BOX)

U28 MAX3100CEE (QSOP) STD0 SRD0 SCK0 CS- SIRQ- N.C. IRQ- GND DIN DOUT SCLK CS- N.C. IRQ- SHDN GND VCC TX RX RTS N.C. CTS X1 X2 TXD RXD RTS CTS

C32 .1UF Y2 ECS-36-20-5P 3.6864Mhz C70 22pf C71 22pf

TP2 SIRQ- R3 1K GND

GUARD BANDING REQ'D

J5 (JTAG/OnCE) HEADER14_NO6 TDI TDO TCK RESET- TMS DE- TRST-

J6 (Jtag) HEA_SIP 8 (.100 PICCH) JUMP 'J6' PIN 6 TO 7 TO LOAD 'init' PART TXD RXD CTS- RTS- INIT-

J7 (Jtag) HSIP8NO5 RD- FLASHCS- BSCAN- PRAMCS- WR-

RP1 9 3.3KSIP10C

U7 74LCX16245 (TSSOP48) U8 74LCX16245 (TSSOP48) RP3 10KSIP10C RP6 10KSIP10C

GUARD BAND GPUCLK HACK- A15X/YP WR- RD- BAX/Y BWR- BRD- BAX/Y BWR- BRD- EXTAL BHACK-

NETLIST CHANGE ******** GUARD BAND

U1 DSP56311GC150

VCCQL 55FZ103N C41 1UF C42 47UF C43 001 (2905) POLY GND **POLY CAP**

TP1 GND E4 E5 E6 E7

P:$000000-$01FFFF STANDARD MEMORY OPTION (64K) P:$000000-$03FFFF EXTENDED MEMORY OPTION (256K)

RP2 3.3KSIP10C MODA/IRQA- MODB/IRQB- MODC/IRQC- BOOTEN- SCI01 SIRQ- RTXD- BSCI11

U6 ISPLSI2064E_DECODE (TSQFP100) E2 1-to-2 is for DPR on base board E2 2-to-3 is for DPR on expansion board

Memory Range

P:$000000-$03FFFF (MAXIMUM OF 16 BANKS)
X/Y:$050000-$05FFFF STANDARD MEMORY OPTION (64K)
X/Y:$050000-$05FFFF EXTENDED MEMORY OPTION (448K)

U25 PI74FCT16245ATA (TSSOP48) C100 .1UF C101 .1UF C102 .1UF C103 .1UF C105 .1UF

CS0- CS1- CS2- CS3- CS4- CS5- CS6- CS10- CS12- CS14- CS16- BRCLK VMECS- DPRCS- WDTC

X/Y:$078000-$0780FF X/Y:$078100-$0781FF X/Y:$078200-$0782FF X/Y:$078300-$0783FF X/Y:$078400-$0784FF X/Y:$078500-$0785FF X/Y:$078600-$0786FF X/Y:$078700-$0787FF X/Y:$078E00-$078EFF X/Y:$078F00-$078FFF X/Y:$078F00-$078FFF X/Y:$060000-$060FFF STANDARD MEMORY OPTION (4K) X/Y:$060000-$063FFF EXTENDED MEMORY OPTION (16K) X/Y:$060000-$06FFFF EXTENDED MEMORY OPTION (64K) X/Y:$070000-$077FFF

DUAL FOOTPRINT Y1A 1UF MHR13FAJ19.6608 (4 PIN SMT) Y1B 19.6608MHz (DIP14WIDE) C33 CPUCLK U4F (SO14) 74ACT14 R1 10 19.6608Mhz

U9 NC7SZ00 (SOT23-5) C40 .1UF WAIT1- WAIT2- TA-

U4A U4B U4C (SO14) 74ACT14 INIT- R2 10K C1 .1UF RESET

Q4 2N7002 (SOT23) WDTC C35 .01UF RP5A 1KSIP8I RP5B 1KSIP8I D3 MMBD301LT1 RP5C 1KSIP8I Q1 MMBT3906LT1 (SOT23) U3 DS1231S (SOL16) R4 100K C34 1UF 35V tant C2 .1UF D4 MMBD301LT1 U4D U4E WDO

D2 LED GRN PWR D2A LED GRN PWR D1 LED RED MD D1A LED RED MD R5 1K R5A 1K R6 1K R6A 1K

BT1 3.6V BAT D5 MMBD301LT1 D6 MMBD301LT1 Q3 MMBT3906LT1 (SOT23) R7 100 .01FARAD FMOH103Z NEC C17 C16 .1UF U2 MAX795CSA (SO8) C15 .1UF Q2 2N7002 (SOT23)

NETLIST CHANGE ********

RESET- BBRCS- BBRAMCS- TRST-

U30 PI74FCT2451L (TSSOP20) RP9A 330SIP8I STD1 SRD1 SCK1 SC12 SC11 TXD RTS HREQ- C88 .1UF

RP7 3.3KSIP10C RP8 3.3KSIP10C P1 U26C 74ACT14 (SO14) RESET- INIT- RESET A HA2 HA1 HA0 HRW HDS- HREQ- H7 H6 H5 H4 H3 H2 H1 H0 WAIT2- 19.6608Mhz WDO HACK- RXD TXD CTS- STD1 SRD1 SCK1 SC12 SC11 IRQB- CS4- WAIT1- VSP01VT18A01 D7 1SMC5.0AT3 U26A U26B BPHA U26F U26E BSER U26D RESET_B

U24A U24B U24C U24D (SO14) 74ACT32 IOCS_A- BWR- IOCS_B- BRD- BWR_A- BRD_A- BWR_B- BRD_B-

RP4 3.3KSIP10C U27 74LCX245 (TSSOP20) BRXD BCTS- SER_A PHA_A BHA2 BHA1 BHA0 MOOD/IRQD- T/R- RESET- RXD CTS- BSER BPHA HA2 HA1 HA0 IRQB- C87 .1UF

PRAM MEMORY P:

$000000-$00FFFF Firmware (64K)
$040000-$0403FF User Written Phase (1K)
$040400-$040BFF User Written Servo (2K)
$050000-$05FFFF Plcc Standard Memory Option (64K)
$050000-$0BFFFF Plcc Extended Memory Option (448K)

Delta Tau Data Systems, Inc.

Title: DSP563XX CPU Piggyback Board

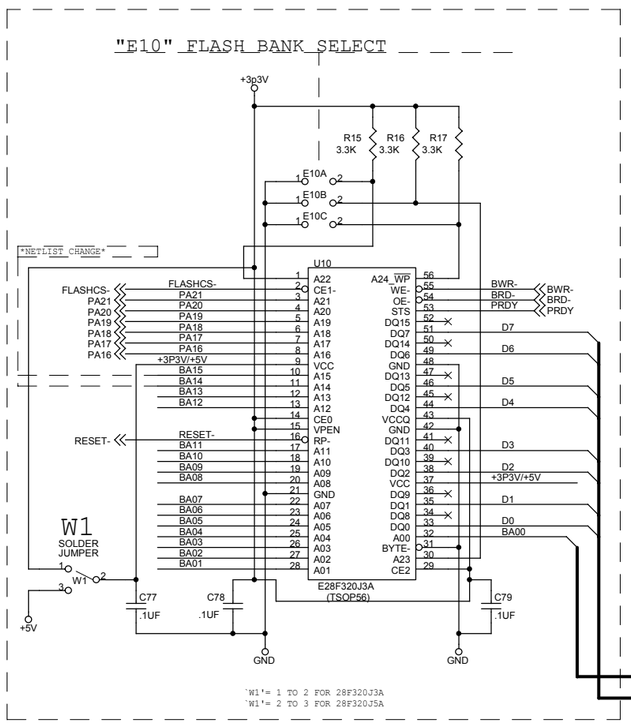
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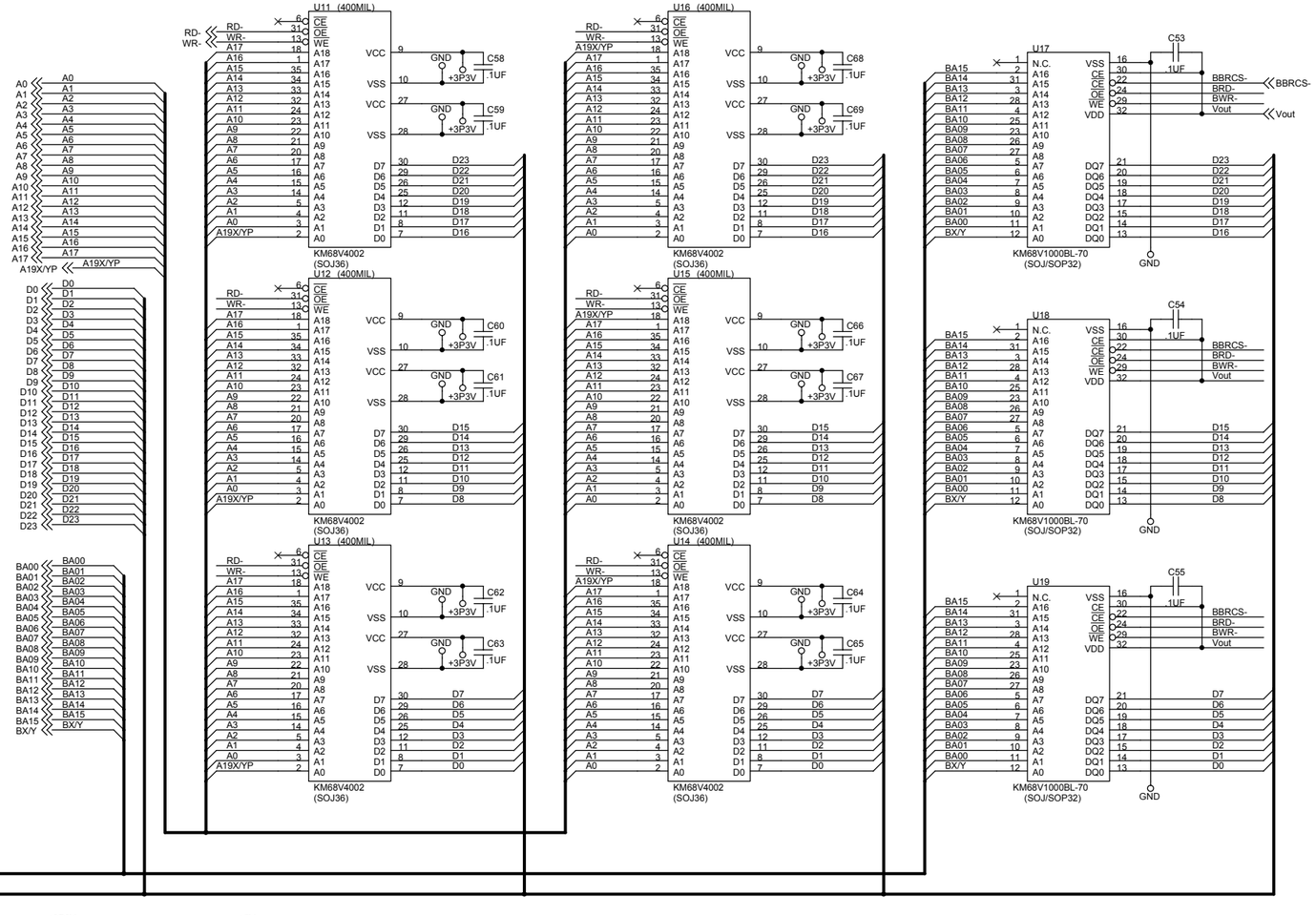
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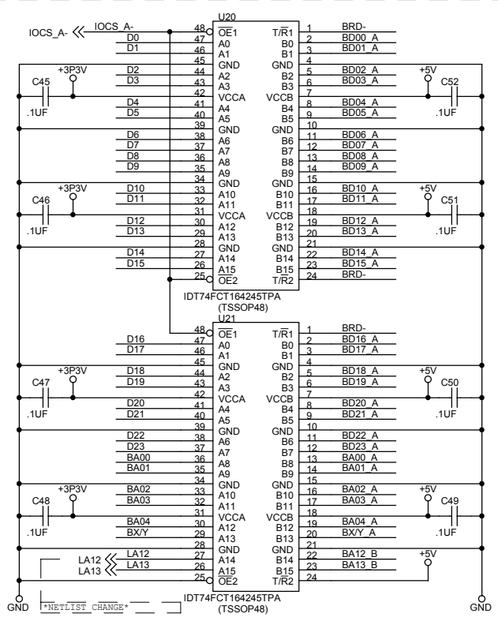
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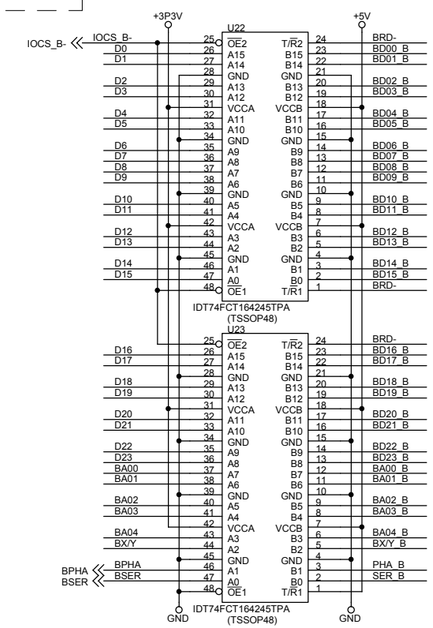
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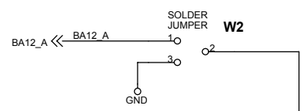


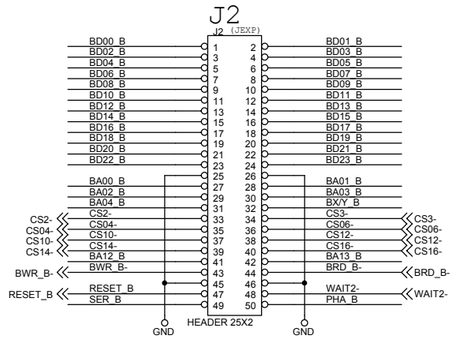


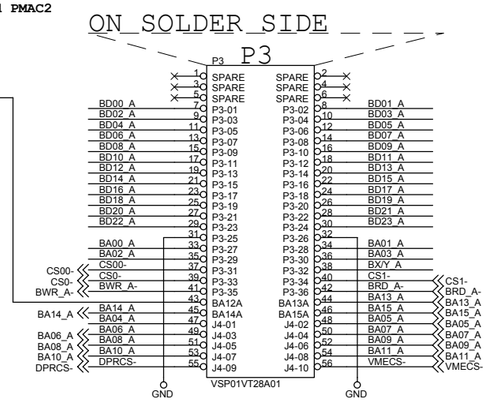
W2 JUMPER SELECTION

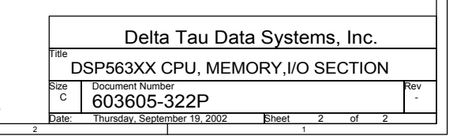
JUMPER 2-3 for Standard PMAC1 and PMAC2

JUMPER 1-2 for TURBO









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