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HARDWARE REFERENCE MANUAL

PMAC2-PC & PMAC2-PC LITE

Programmable Multi-Axis Controllers

3xx-602598-xHxx

January 28, 2003



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INTRODUCTION

Overview

The PMAC2-PC and PMAC2-Lite provide state-of-the-art motion control for a wide variety of applications, including machine tools, robotics, semiconductor manufacturing, packaging equipment, and general-purpose automation. They utilize the latest developments in electronics, software, and modern control theory to bring motion control capabilities to a whole new level.

The PMAC2-PC and PMAC2-Lite are designed as ISAbus expansion cards, but are capable of standalone operation. The configurations are:

- PMAC2-PC: ISAbus-compatible, 1-1/2 slots, 4 or 8 machine interface channels.
- PMAC2-Lite: ISAbus-compatible, 1 slot, 4 machine interface channels.

Features

PMAC2-PC and PMAC2-Lite support a wide variety of servo and stepper interfaces:

- Analog +/-10V velocity command (requires ACC-8E or equivalent)
- Analog +/-10V torque command (requires ACC-8E or equivalent)
- Sinusoidal analog +/-10V phase current commands (requires ACC-8E or equivalent)
- Direct digital pulse-width modulated (PWM) phase voltage commands (requires ACC-8F, -8K or equivalent)
- Pulse-and-direction commands (requires ACC-8S or equivalent)
- MACRO™ ring network commands (requires ACC-42)

PMAC2-PC and PMAC2-Lite also provide unparalleled speeds and resolutions:

- 40 MHz encoder count rate
- 18-bit analog outputs
- 18 microsecond per axis servo update time (60 MHz)
- 120 MHz PWM clock frequency (10-bit resolution at 120 kHz, 12-bit and 30 kHz, 14-bit at 7.5 kHz)
- 120 MHz MLDT (e.g. Temposonics™) timer frequency (0.024mm, 0.9mil resolution)
- 10 MHz maximum pulse-and-direction output frequency
- 10 MHz maximum position-compare output update rate
- 125 Mbit/sec optical ring network data rate

PMAC2 ASICs

Delta Tau has designed its own custom application-specific integrated circuits (ASICs) for the PMAC2-PC and PMAC2-Lite using the latest sub-micron gate-array technology. Each ASIC contains 45,000 active logic gates. These ASICs contain all of the digital interface circuitry to tie the DSP to the machine; the rest of the circuitry on the board is buffer circuitry.

DSPGATE1 Servo ASIC

The "DSPGATE1" ASIC contains the digital servo interface circuitry for 4 channels, usually sufficient for four axes of control. Each channel contains:

Three command output sets:

1. Top-and-bottom PWM or serial DAC data with clock
2. Top-and-bottom PWM or serial DAC data with strobe
3. Top-and-bottom PWM or PFM pulse-and-direction

- Encoder quadrature or pulse-and-direction decode and count

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- Index channel input internally gated to 1 quadrature state wide
- 4 flags with capability to perform hardware latching of encoder position
- HOME, PLIM, MLIM, USER
- Double-sided position-compare output with auto-increment capability
- Amplifier enable output
- Amplifier fault input
- 4 supplementary flag inputs (T, U, V, W)
- 2 inputs from serial analog-to-digital converters (ADCs)
- ADC clock and strobe signal outputs

The DSPGATE1 ASIC also generates several clock frequencies necessary for hardware and software operation, under the user's software control:

- PWM output frequency
- DAC clock frequency

Phase interrupt clock frequency and Servo interrupt clock frequency are generated from the first DSPGATE1 only.

- ADC clock frequency
- Encoder sample clock frequency
- Pulse-frequency modulation (PFM) clock frequency
- Phase interrupt clock frequency
- Servo interrupt clock frequency

DSPGATE2 I/O ASIC

There is also a "DSPGATE2" ASIC on PMAC2-PC and PMAC2-Lite, which is used for interface to other I/O. The DSPGATE2 ASIC has 3 parts:

- General-purpose digital I/O: 56 I/O points for JIO, JTHW, and JDISP ports
- Servo interface circuitry for 2 supplemental channels with clock generation
- MACRO ring interface circuitry

The general-purpose I/O and the servo interface circuitry on the DSPGATE2 generally share pins, except for two 2-channel encoder inputs and 2 PWM/PFM output sub-channels. The shared pins are almost always used for general-purpose I/O instead of extra servo interface circuitry, but this is up to the individual user.

PMAC2-PC Configuration

A PMAC2-PC can have 1 or 2 DSPGATE1 ASICs; the first one is standard, and the second one comes if Option 1 is ordered. Each also has a DSPGATE2 ASIC supporting the non-servo I/O.

PMAC2-Lite Configuration

A PMAC2-Lite board (PC bus only) has a single DSPGATE1 ASIC on-board, supporting up to 4 axes of servo interfaces. It also has a DSPGATE2 ASIC supporting the non-servo I/O. It cannot be expanded on-board to add a second DSPGATE1 ASIC to support a full 8 axes.

PMAC2-PC Board Configuration

Jumpers on the PMAC2-PC determine the frequency at which the DSP on the PV CPU board will operate. The 56002 DSP has a "phased-locked loop" (PLL) that allows it to multiply the crystal frequency by a programmable integer value, permitting very high CPU frequencies with a moderate crystal frequency. The crystal frequency on the PV CPU board is always 19.6608 MHz, commonly called "20 MHz".

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The component rating of the DSP IC specifies the *highest* frequency at which it safely *can* run, but it is the multiplication factor typically set by jumpers that specifies the frequency at which it actually runs. Usually this is a frequency at or near the maximum for the component.

It is safe to run a DSP at a frequency below the maximum. It *may* be possible to run a DSP at a frequency higher than its maximum frequency, particularly at low ambient temperatures, *but safe operation cannot be guaranteed. Unpredictable and possibly dangerous operation may result.*

On power-up/reset, the DSP, operating at the crystal frequency of 20 MHz, reads the frequency jumpers (E2 and E4) and writes into its own PLL multiplier register at X:$FFFD. Bits 0-3 of this word contain a value one less than the multiplier value (if the frequency is being multiplied by 3, these bits contain a value of 2).

If you wish to check the value of your multiplier, you can use the on-line command RHX:$FFFD and look at the last hexadecimal digit. The actual multiplier is one greater than the value in this last digit. Alternately, you can define an M-variable such as M99->X:$FFFD,0,4 and then read from or write to these bits with the M-variable.

PMAC2-PC Setup

On PMAC2-PC, jumpers E2 and E4 control the frequency of operation of the DSP according to Table 1-2.

E2	E4	X:$FFFD; 0-3	True Multiplier	DSP Frequency
OFF	OFF	1	x2	40 MHz
ON	OFF	2	x3	60 MHz
OFF	ON	3	x4	80 MHz

On the PMAC2-PC, I54 is read at power-up to set the baud rate clock. Because this clock is derived from the CPU clock frequency, the proper setting of I54 is dependent on the CPU clock frequency as set by E2 and E4. Table 1-3 shows the settings of I54 for 40, 60, and 80 MHz CPU operation.

I54	Baud Rate for 40 MHz CPU	Baud Rate for 60 MHz CPU	Baud Rate for 80 MHz CPU
0	600	DISABLED	1200
1	900* (-0.05%)	900	1800* (-0.1%)
2	1200	1200	2400
3	1800* (-0.1%)	1800	3600* (-0.19%)
4	2400	2400	4800
5	3600* (-0.19%)	3600	7200* (-0.38%)
6	4800	4800	9600
7	7200* (-0.38%)	7200	14,400*(-0.75%)
8	9600	9600	19,200
9	14,400*(-0.75%)	14,400	28,800*(-1.5%)
10	19,200	19,200	38,400
11	28,800*(-1.5%)	28,800	57,600*(-3.0%)
12	38,400	38,400	76,800
13	57,600*(-3.0%)	57,600	115,200*(-6.0%)
14	76,800	76,800	153,600
15	DISABLED	115,200	DISABLED
* Not an exact baud rate			

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PMAC2 CPUs

The PMAC2-PC CPU communicates with the axes through specially designed custom gate array ICs, referred to as "DSPGATES". Each of these ICs can handle four analog output channels, four encoders as input, and four analog-derived inputs from accessory boards. One PMAC2-PC can utilize from one to four of these gate array ICs, so specifying the hardware configuration amounts to counting the numbers and types of inputs and outputs. Up to 16 PMAC2-PCs may be ganged together with complete synchronization, for a total of 128 axes. A PMAC2-PC may have one of three available CPU configurations. These configurations are described in the following paragraphs.

Note:

The CPUs are only installed on the PMAC2-PC.

P/N 602398

This is the original standard CPU board for the PMAC2-PC. It has a 20MHz clock and a battery backup RAM.

P/N 602405

This is a flash memory CPU board with no battery backup. This board provides either a 40MHz or 60MHz clock.

P/N 602705

The PMAC2-PC PV CPU piggyback board provides 80 MHz CPU operation and supplemental battery-backed RAM for the PMAC2-

The PV CPU board gets its name from the PV package style of the Motorola 56002 DSP IC on the board. The board is also called the Universal CPU because it can support all speeds and configurations of the CPU section.

The PV CPU has operational differences from earlier CPU configurations to support the new features. The following paragraphs explain these differences and are only relevant if you have the 602705 CPU piggyback board on your controller.

Configurations

The PV CPU board is configured at the factory to the customer's specifications. The JEXP expansion port is buffered, providing the capability to connect many boards on the expansion port.

The following table shows the configuration of the key components on the PV CPU board for the PMAC2-PC.

Version	Main Memory Backup	U6, U9, U15 Components	U7, U10, U16 Components	U5 Components	BT1 Component
Standard	Flash	Empty	32-pin RAM	Flash ROM	Empty
Opt 5B	Flash	Empty	32-pin RAM	Flash ROM	Empty
Opt 5C	Flash	Empty	32-pin RAM	Flash ROM	Empty
+Opt 16	Flash	28-pin RAM	32-pin RAM	Flash ROM	Battery

Firmware

The PV CPU board does not support firmware versions before V1.16 of August 1996 without changes in programming of the on-board logic (GALs). If the firmware must be changed between a version previous to V1.16 and a version V1.16 or newer, the on-board logic must be re-programmed.

When loading new firmware into the flash configurations of the PV CPU, E4 on the CPU board must be ON in addition to having the PMAC2-PC reinitialization jumper E3 ON.

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Option 16 Supplemental Memory

If the Option 16 supplemental battery-backed parameter memory is ordered, an extra bank of memory with battery backup circuitry is provided. This option can only be ordered if the main memory is flash backed (Option 4A, 5A, 5B, or 5C). This memory is for user parameter storage only. From PMAC programs it can be accessed with M-variables only (L-variables also in compiled PLCs). The on-line direct-memory read and write commands can be used from the host computer as well.

With M-variable access, arrays can be created with indirect addressing techniques by pointing a second M-variable to the definition of a first M-variable that points into this memory area. For example, with the M-variable definitions:

```
M0->L:$A000; 1st long word of Opt. 16 RAM; floating point
M10->Y:$BC000,0,16    ; Low 16 bits of M0 def., with pointer address
```

The following code segment could load a sine table into the first 360 words of the Option 16 RAM:

```
P1=0
WHILE (P1<360)
  M10=$A000+P1   ; Sets address that M0 points to
  M0=SIN(P1)     ; Puts value in register that M0 points to
  P1=P1+1
ENDWHILE
```

Note:

This technique is not possible with L-variables in compiled PLCs.

Physically, the Option 16 memory is a 16k x 24 bank of battery-backed static RAM. It maps into the PMAC2-PC at addresses $A000 to $BFFF, on both the X and Y data buses, an 8k x 48 block of address space. Addresses Y:$BC00 to Y:$BFFF are “double-mapped” with the main flash-backed RAM for the M-variable definitions, and should not be used for user parameter storage.

Any value written into the Option 16 memory will automatically be retained through a power-down or reset; no **SAVE** operation is required. The power draw on the battery is low enough that battery life will typically be limited only by the quoted 10-year life of the battery.

Related Technical Documentation

Manual Number	Manual Title
3A0-602413-363	PMAC2 User’s Manual
3A0-602XXX-363	PMAC User’s Software Reference

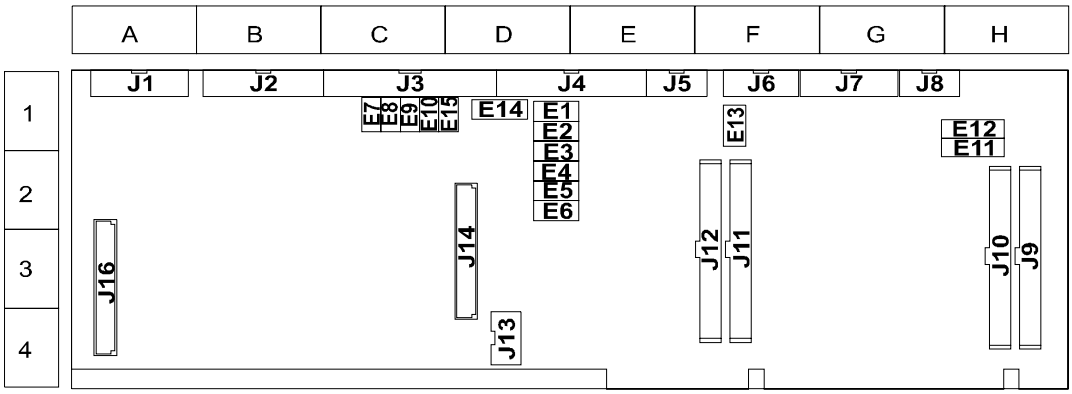
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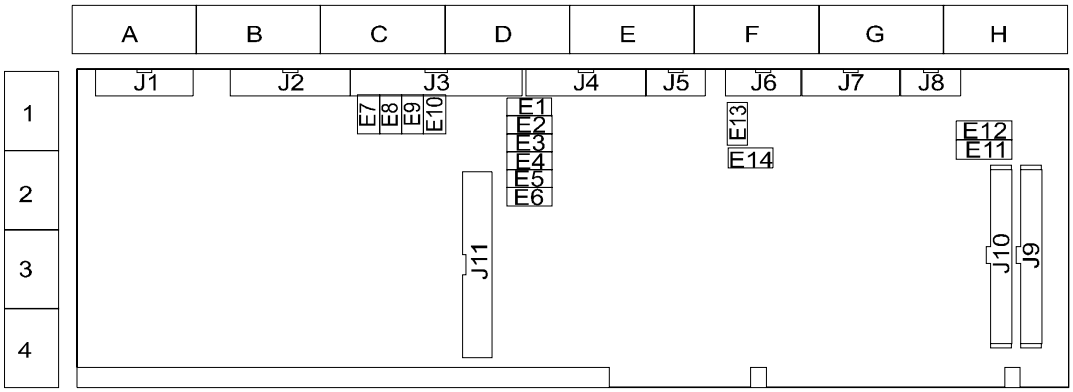
CONNECTORS AND JUMPERS

PMAC2-PC AND PMAC2-Lite Connector Summary

The following paragraphs provide a brief description of each connector on the PMAC2-PC and PMAC2-Lite, its use, and individual pinout information (see Figure 2-1).



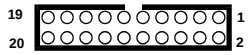
P M A C 2 - P C



PMAC2-LITE

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J1 (JANA) Analog Input Port Connector



Front View

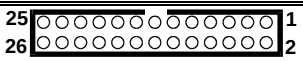
Pin #	Symbol	Function	Description	Notes
1	ANAI00	Input	Analog Input 0	0-5V or +/-2.5V range
2	ANAI01	Input	Analog Input 1	0-5V or +/-2.5V range
3	ANAI02	Input	Analog Input 2	0-5V or +/-2.5V range
4	ANAI03	Input	Analog Input 3	0-5V or +/-2.5V range
5	ANAI04	Input	Analog Input 4	0-5V or +/-2.5V range
6	ANAI05	Input	Analog Input 5	0-5V or +/-2.5V range
7	ANAI06	Input	Analog Input 6	0-5V or +/-2.5V range
8	ANAI07	Input	Analog Input 7	0-5V or +/-2.5V range
9	ANAI08	Input	Analog Input 8	0-5V or +/-2.5V range
10	ANAI09	Input	Analog Input 9	0-5V or +/-2.5V range
11	ANAI10	Input	Analog Input 10	0-5V or +/-2.5V range
12	ANAI11	Input	Analog Input 11	0-5V or +/-2.5V range
13	ANAI12	Input	Analog Input 12	0-5V or +/-2.5V range
14	ANAI13	Input	Analog Input 13	0-5V or +/-2.5V range
15	ANAI14	Input	Analog Input 14	0-5V or +/-2.5V range
16	ANAI15	Input	Analog Input 15	0-5V or +/-2.5V range
17	GND	Common	PMAC Common	Not isolated from digital
18	+12V	Output	Positive Supply Voltage	To power external circuitry
19	GND	Common	PMAC Common	Not isolated from digital
20	-12V	Output	Negative Supply Voltage	To power external circuitry

The JANA connector provides the inputs for the 8 or 16 optional analog inputs on the PMAC2-PC and PMAC2-Lite.

Note: This connector is only present if Option 12 is ordered.

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J2 (JTHW) Multiplexer Port Connector



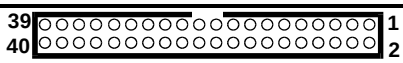
Front View

Pin #	Symbol	Function	Description	Notes
1	GND	COMMON	PMAC Common	
2	GND	COMMON	PMAC Common	
3	DAT0	INPUT	Data-0 Input	Data input from mux port accessories
4	SEL0	OUTPUT	Select-0 Output	Address/data output for mux port accessories
5	DAT1	INPUT	Data -1 Input	Data input from mux port accessories
6	SEL1	OUTPUT	Select-1 Output	Address/data output for mux port accessories
7	DAT2	INPUT	Data -2 Input	Data input from mux port accessories
8	SEL2	OUTPUT	Select-2 Output	Address/data output for mux port accessories
9	DAT3	INPUT	Data-3 Input	Data input from mux port accessories
10	SEL3	OUTPUT	Select-3 Output	Address/data output for mux port accessories
11	DAT4	INPUT	Data-4 Input	Data input from mux port accessories
12	SEL4	OUTPUT	Select-4 Output	Address/data output for mux port accessories
13	DAT5	INPUT	Data-5 Input	Data input from mux port accessories
14	SEL5	OUTPUT	Select-5 Output	Address/data output for mux port accessories
15	DAT6	INPUT	Data-6 Input	Data input from mux port accessories
16	SEL6	OUTPUT	Select-6 Output	Address/data output for mux port accessories
17	DAT7	INPUT	Data-7 Input	Data input from mux port accessories
18	SEL7	OUTPUT	Select-7 Output	Address/data output for mux port accessories
19	N.C.	N.C.	No Connection	
20	GND	COMMON	PMAC Common	
21	BRLD/	OUTPUT	Buffer Request	Low is "buffer req."
22	GND	COMMON	PMAC Common	
23	IPLD/	OUTPUT	In Position	Low is "in position"
24	GND	COMMON	PMAC Common	
25	+5V	OUTPUT	+5Vdc Supply	Power supply out
26	INIT/	INPUT	PMAC Reset	Low is "reset"

The JTHW connector provides eight inputs and eight outputs at TTL levels that are dedicated to reading BCD thumbwheel switches. Two thumbwheels may be read by direct connection to J3. More thumbwheels, up to 512 switches, may be read using Accessory 18 (ACC-18, Thumbwheel Multiplexer). J3 inputs and outputs may be used as general purpose multiplexed TTL I/O if thumbwheels are not used.

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J3 (JI/O) General I/O Connector



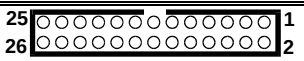
Front View

Pin #	Symbol	Function	Description	Notes
1	I/O00	IN/OUT	Digital I/O 0	Software direction ctrl.
2	I/O01	IN/OUT	Digital I/O 1	Software direction ctrl.
3	I/O02	IN/OUT	Digital I/O 2	Software direction ctrl.
4	I/O03	IN/OUT	Digital I/O 3	Software direction ctrl.
5	I/O04	IN/OUT	Digital I/O 4	Software direction ctrl.
6	I/O05	IN/OUT	Digital I/O 5	Software direction ctrl.
7	I/O06	IN/OUT	Digital I/O 6	Software direction ctrl.
8	I/O07	IN/OUT	Digital I/O 7	Software direction ctrl.
9	I/O08	IN/OUT	Digital I/O 8	Software direction ctrl.
10	I/O09	IN/OUT	Digital I/O 9	Software direction ctrl.
11	I/O10	IN/OUT	Digital I/O 10	Software direction ctrl.
12	I/O11	IN/OUT	Digital I/O 11	Software direction ctrl.
13	I/O12	IN/OUT	Digital I/O 12	Software direction ctrl.
14	I/O13	IN/OUT	Digital I/O 13	Software direction ctrl.
15	I/O14	IN/OUT	Digital I/O 14	Software direction ctrl.
16	I/O15	IN/OUT	Digital I/O 15	Software direction ctrl.
17	I/O16	IN/OUT	Digital I/O 16	Software direction ctrl.
18	I/O17	IN/OUT	Digital I/O 17	Software direction ctrl.
19	I/O18	IN/OUT	Digital I/O 18	Software direction ctrl.
20	I/O19	IN/OUT	Digital I/O 19	Software direction ctrl.
21	I/O20	IN/OUT	Digital I/O 20	Software direction ctrl.
22	I/O21	IN/OUT	Digital I/O 21	Software direction ctrl.
23	I/O22	IN/OUT	Digital I/O 22	Software direction ctrl.
24	I/O23	IN/OUT	Digital I/O 23	Software direction ctrl.
25	I/O24	IN/OUT	Digital I/O 24	Software direction ctrl.
26	I/O25	IN/OUT	Digital I/O 25	Software direction ctrl.
27	I/O26	IN/OUT	Digital I/O 26	Software direction ctrl.
28	I/O27	IN/OUT	Digital I/O 27	Software direction ctrl.
29	I/O28	IN/OUT	Digital I/O 28	Software direction ctrl.
30	I/O29	IN/OUT	Digital I/O 29	Software direction ctrl.
31	I/O30	IN/OUT	Digital I/O 30	Software direction ctrl.
32	I/O31	IN/OUT	Digital I/O 31	Software direction ctrl.
33	GND	COMMON	Reference Voltage	
34	GND	COMMON	Reference Voltage	
35	PHASE/	OUTPUT	Phase Clock	For latching data
36	SERVO/	OUTPUT	Servo Clock	For latching data
37	GND	COMMON	Reference Voltage	
38	GND	COMMON	Reference Voltage	
39	+5V	OUTPUT	Supply Voltage	To power external circuitry
40	+5V	OUTPUT	Supply Voltage	To power external circuitry

The JI/O connector provides 32 input/output pins at TTL levels. Direction can be controlled in byte-wide groups.

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J4 (JMACRO) 26-Pin Connector

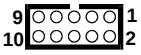


Front View

Pin #	Symbol	Function	Description	Notes
1	DOUT7	OUTPUT	Ring Out Bit 7	Macro ring command
2	DOUT6	OUTPUT	Ring Out Bit 6	Macro ring transmit
3	DOUT5	OUTPUT	Ring Out Bit 5	Macro ring transmit
4	DOUT4	OUTPUT	Ring Out Bit 4	Macro ring transmit
5	DOUT3	OUTPUT	Ring Out Bit 3	Macro ring transmit
6	DOUT2	OUTPUT	Ring Out Bit 2	Macro ring transmit
7	DOUT1	OUTPUT	Ring Out Bit 1	Macro ring transmit
8	DOUT0	OUTPUT	Ring Out Bit 0	Macro ring transmit
9	CMD_IN	INPUT		
10	DIN7	INPUT	Ring In Bit 7	Macro ring receive
11	DIN6	INPUT	Ring In Bit 6	Macro ring receive
12	DIN5	INPUT	Ring In Bit 5	Macro ring receive
13	DIN4	INPUT	Ring In Bit 4	Macro ring receive
14	DIN3	INPUT	Ring In Bit 3	Macro ring receive
15	DIN2	INPUT	Ring In Bit 2	Macro ring receive
16	DIN1	INPUT	Ring In Bit 1	Macro ring receive
17	DIN0	INPUT	Ring In Bit 0	Macro ring receive
18	CMD_OUT	OUTPUT		
19	TCLK	OUTPUT	Ring Clock	10 MHz
20	GND	COMMON	Reference Voltage	
21	STB_OUT	OUTPUT	Byte Strobe	
22	GND	COMMON	Reference Voltage	
23	DAT_STB	INPUT	Data Byte Strobe	
24	GND	COMMON	Reference Voltage	
25	CMD_STB	INPUT	CMD Byte Strobe	
26	VLTN	INPUT	Violation Flag	Taxi chip receive error

The JMACRO Network Ring Interface Connector provides the interface to the MACRO driver/receiver accessory board.

J5 (JRS232) Serial Port Connector



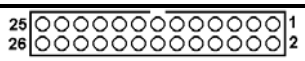
Front View

Pin #	Symbol	Function	Description	Notes
1	PHASE	OUTPUT	Phasing Clock	
2	DTR	BIDIRECT	Data Term Rdy	Tied to DSR
3	TXD/	INPUT	Receive Data	Host transmit data
4	CTS	INPUT	Clear To Send	Host ready bit
5	RXD/	OUTPUT	Send Data	Host receive data
6	RTS	OUTPUT	Req. To Send	PMAC ready bit
7	DSR	BIDIRECT	Data Set Ready	Tied to DTR
8	SERVO	OUTPUT	Servo Clock	
9	GND	COMMON	PMAC Common	
10	+5V	OUTPUT	+5Vdc Supply	Power supply out

This connector is present and operational on the standard PMAC2-PC or PMAC2-Lite. If the Option-9L RS-422 interface has been ordered, this connector is non-functional. The serial interface is made through one of the RS-422 connectors on the Option-9L piggyback board.

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JRS422 (26-Pin Connector)

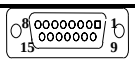


Front View

Pin #	Symbol	Function	Description	Notes
1	CHASSI	COMMON	PMAC Common	
2	S+5V	OUTPUT	+5Vdc Supply	Deactivated by "E8"
3	RD-	INPUT	Receive Data	Diff I/O low true
4	RD+	INPUT	Receive Data	Diff I/O high true
5	SD-	OUTPUT	Send Data	Diff I/O low true
6	SD+	OUTPUT	Send Data	Diff I/O high true
7	CS+	INPUT	Clear To Send	Diff I/O high true
8	CS-	INPUT	Clear To Send	Diff I/O low true
9	RS+	OUTPUT	Req. To Send	Diff I/O high true
10	RS-	OUTPUT	Req. To Send	Diff I/O low true
11	DTR	BIDIRECT	Data Term Read	Tied to "DSR"
12	INIT/	INPUT	PMAC Reset	Low is "reset"
13	GND	COMMON	PMAC Common	
14	DSR	BIDIRECT	Data Set Ready	Tied to "DTR"
15	SDIO-	BIDIRECT	Special Data	Diff I/O low true
16	SDIO+	BIDIRECT	Special Data	Diff I/O high true
17	SCIO-	BIDIRECT	Special Ctrl.	Diff I/O low true
18	SCIO+	BIDIRECT	Special Ctrl.	Diff I/O high true
19	SCK-	BIDIRECT	Special Clock	Diff I/O low true
20	SCK+	BIDIRECT	Special Clock	Diff I/O high true
21	SERVO-	BIDIRECT	Servo Clock	Diff I/O low true
22	SERVO+	BIDIRECT	Servo Clock	Diff I/O high true
23	PHASE-	BIDIRECT	Phase Clock	Diff I/O low true
24	PHASE+	BIDIRECT	Phase Clock	Diff I/O high true
25	GND	COMMON	PMAC Common	
26	+5V	OUTPUT	+5Vdc Supply	Power supply out

The JRS422 connector provides the PMAC with the ability to communicate both in RS422 and RS232. In addition, this connector is used to daisy chain interconnect multiple PMACs for synchronized operation.
Note: This connector is only present if the Option 9L RS-422 interface has been ordered.

JRS422 (DB-15 Connector)



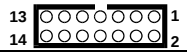
Front View

Pin #	Symbol	Function	Description	Notes
1	CHASSI	COMMON	PMAC Common	
2	N.C.	NONE	No Connect	
3	N.C.	NONE	No Connect	
4	N.C.	NONE	No Connect	
5	S+5V	OUTPUT	+5Vdc Supply	Deactivated By "E8"
6	RS-	OUTPUT	Req. To Send	Diff I/O low true
7	GND	COMMON	PMAC Common	
8	CS+	INPUT	Clear To Send	Diff I/O high true
9	N.C.	NONE	No Connect	
10	RD-	INPUT	Receive Data	Diff I/O low true
11	RD+	INPUT	Receive Data	Diff I/O high true
12	SD-	OUTPUT	Send Data	Diff I/O low true
13	SD+	OUTPUT	Send Data	Diff I/O high true
14	RS+	OUTPUT	Req. To Send	Diff I/O high true
15	CS-	INPUT	Clear To Send	Diff I/O low true

This connector is only present if the Option-9L RS-422 interface has been ordered.

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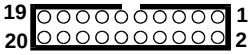
J6 (JDISP) Display Connector



Pin #	Symbol	Function	Description	Notes
1	Vdd	OUTPUT	+5V Power	Power supply out
2	Vss	COMMON	PMAC Common	
3	Rs	OUTPUT	Read Strobe	TTL signal out
4	Vee	OUTPUT	Contrast Adjust. Vee	0 to +5 Vdc
5	E	OUTPUT	Display Enable	High is enable
6	R/W	OUTPUT	Read Or Write	TTL signal out
7	DB1	OUTPUT	Display Data1	
8	DB0	OUTPUT	Display Data0	
9	DB3	OUTPUT	Display Data3	
10	DB2	OUTPUT	Display Data2	
11	DB5	OUTPUT	Display Data5	
12	DB4	OUTPUT	Display Data4	
13	DB7	OUTPUT	Display Data7	
14	DB6	OUTPUT	Display Data6	

The JDISP connector is used to drive the 2 line x 24 character (ACC-12), 2 x 40 (ACC-12A) LCD, or the 2 x 40 vacuum fluorescent (ACC-12C) display unit. The DISPLAY command may be used to send messages and values to the display.

J7 (JHW) Handwheel Encoder Connector

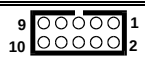


Front View

Pin #	Symbol	Function	Description	Notes
1	GND	COMMON	Reference Voltage	
2	+5V	OUTPUT	Supply Voltage	To power ext. Circuitry
3	HWA1+	INPUT	HW Positive A Channel	Also pulse input
4	HWA1-	INPUT	HW Negative A Channel	Also pulse input
5	HWB1+	INPUT	HW Positive B Channel	Also direction input
6	HWB1-	INPUT	HW Negative B Channel	Also direction input
7	HWA2+	INPUT	HW Positive A Channel	Also pulse input
8	HWA2-	INPUT	HW Negative A Channel	Also pulse input
9	HWB2+	INPUT	HW Positive B Channel	Also direction input
10	HWB2-	INPUT	HW Negative B Channel	Also direction input
11	PUL1+	OUTPUT	PFM Positive Pulse Out	Also PWM output
12	PUL1-	OUTPUT	PFM Negative Pulse Out	Also PWM output
13	DIR1+	OUTPUT	PFM Positive Direction	Also PWM output
14	DIR1-	OUTPUT	PFM Negative Direction	Also PWM output
15	PUL2+	OUTPUT	PFM Positive Pulse Out	Also PWM output
16	PUL2-	OUTPUT	PFM Negative Pulse Out	Also PWM output
17	DIR2+	OUTPUT	PFM Positive Direction	Also PWM output
18	DIR2-	OUTPUT	PFM Negative Direction	Also PWM output
19	GND	COMMON	Reference Voltage	
20	+5V	OUTPUT	Supply Voltage	To power external circuitry

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J8 (JEQU) Position Compare Output Connector

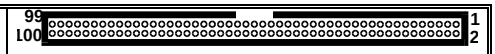


Front View

Pin #	Symbol	Function	Description	Notes
1	EQU1/	OUTPUT	Encoder 1 COMP-EQ	Low is true
2	EQU2/	OUTPUT	Encoder 2 COMP-EQ	Low is true
3	EQU3/	OUTPUT	Encoder 3 COMP-EQ	Low is true
4	EQU4/	OUTPUT	Encoder 4 COMP-EQ	Low is true
5	EQU5/	OUTPUT	Encoder 5 COMP-EQ	Low is true
6	EQU6/	OUTPUT	Encoder 6 COMP-EQ	Low is true
7	EQU7/	OUTPUT	Encoder 7 COMP-EQ	Low is true
8	EQU8/	OUTPUT	Encoder 8 COMP-EQ	Low is true
9	+V	SUPPLY	Positive Supply	+5V to +24V
10	GND	COMMON	Digital Ground	

This connector provides the position-compare outputs for the eight encoder channels.

J9 (JMACH1) Connector Description



Front View

Pin#	Symbol	Function	Description	Notes
1	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
2	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
3	GND	COMMON	Reference Voltage	
4	GND	COMMON	Reference Voltage	
5	CHA1+	INPUT	Encoder 1 Positive A Channel	Also pulse input
6	CHA1-	INPUT	Encoder 1 Negative A Channel	Also pulse input
7	CHB1+	INPUT	Encoder 1 Positive B Channel	Also direction input
8	CHB1-	INPUT	Encoder 1 Negative B Channel	Also direction input
9	CHC1+	INPUT	Encoder 1 Positive C Channel	Index channel
10	CHC1-	INPUT	Encoder 1 Negative C Channel	Index channel
11	CHU1	INPUT	Channel 1 U Flag	Hall effect, fault code, or sub-count
12	CHV1	INPUT	Channel 1 V Flag	Hall effect, fault code, or sub-count
13	CHW1	INPUT	Channel 1 W Flag	Hall effect, fault code, or sub-count
14	CHT1	INPUT	Channel 1 T Flag	Fault code, or sub-count
15	USER1	INPUT	General Purpose User Flag	Hardware capture flag, or sub-count
16	PLIM1	INPUT	Positive Overtravel Limit	Hardware capture flag
17	MLIM1	INPUT	Negative Overtravel Limit	Hardware capture flag
18	HOME1	INPUT	Home Switch Input	Hardware capture flag
19	ACCFLT1	INPUT	Accessory Fault Flag	For loss OF ACC supply voltage
20	WD0/	OUTPUT	Watchdog Output	Low is PMAC watchdog fault
21	SCLK12+	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC2 jumper
22	SCLK12-	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC2 jumper
23	ADC_CLK1+	OUTPUT	A/D Converter Clock	Programmable frequency
24	ADC_CLK1-	OUTPUT	A/D Converter Clock	Programmable frequency
25	ADC_STB1+	OUTPUT	A/D Converter Strobe	Programmable sequence
26	ADC_STB1-	OUTPUT	A/D Converter Strobe	Programmable sequence

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27	ADC_DAA1+	INPUT	Channel A ADC Serial Data	MSB first
28	ADC_DAA1-	INPUT	Channel A ADC Serial Data	MSB first
29	ADC_DAB1+	INPUT	Channel B ADC Serial Data	MSB first
30	ADC_DAB1-	INPUT	Channel B ADC Serial Data	MSB first
31	AENA1+	OUTPUT	Amplifier Enable	High is enable
32	AENA1-	OUTPUT	Amplifier Enable	Low is enable
33	FAULT1+	INPUT	Amplifier Fault	Programmable polarity
34	FAULT1-	INPUT	Amplifier Fault	Programmable polarity
35	PWMATOP1+ DAC_CLK1+	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
36	PWMATOP1- DAC_CLK1-	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
37	PWMABOT1+ DAC1A+	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control
38	PWMABOT1- DAC1A-	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control
39	PWMBTOP1+ DAC_STB1+	OUTPUT	Phase B TOP CMD or DAC Strobe	Programmable function control
40	PWMBTOP1- DAC_STB1-	OUTPUT	Phase B TOP CMD or DAC Strobe	Programmable function control
41	PWMBBOT1+ DAC1B+	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
42	PWMBBOT1- DAC1B-	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
43	PWMCTOP1+ DIR1+	OUTPUT	Phase B TOP CMD or PFM Direction	Programmable function control
44	PWMCTOP1- DIR1-	OUTPUT	Phase B TOP CMD or PFM Direction	Programmable function control
45	PWMCBOT1+ PULSE1+	OUTPUT	Phase B Bottom CMD or PFM Pulse	Programmable function control
46	PWMCBOT1- PULSE1-	OUTPUT	Phase B Bottom CMD or PFM Pulse	Programmable function control
47	GND	COMMON	Reference Voltage	
48	GND	COMMON	Reference Voltage	
49	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
50	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
51	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
52	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
53	GND	COMMON	Reference Voltage	
54	GND	COMMON	Reference Voltage	
55	CHA2+	INPUT	Encoder 2 Positive A Channel	Also pulse input
56	CHA2-	INPUT	Encoder 2 Negative A Channel	Also pulse input
57	CHB2+	INPUT	Encoder 2 Positive B Channel	Also direction input
58	CHB2-	INPUT	Encoder 2 Negative B Channel	Also direction input
59	CHC2+	INPUT	Encoder 2 Positive C Channel	Index channel
60	CHC2-	INPUT	Encoder 2 Negative C Channel	Index channel
61	CHU2	INPUT	Channel 2 U Flag	Hall effect, fault code, or sub-count
62	CHV2	INPUT	Channel 2 V Flag	Hall effect, fault code, or sub-count

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63	CHW2	INPUT	Channel 2 W Flag	Hall effect, fault code, or sub-count
64	CHT2	INPUT	Channel 2 T Flag	Fault code, or sub-count
65	USER2	INPUT	General Purpose User Flag	Hardware capture flag, or sub-count
66	PLIM2	INPUT	Positive Overtravel Limit	Hardware capture flag
67	MLIM2	INPUT	Negative Overtravel Limit	Hardware capture flag
68	HOME2	INPUT	Home Switch Input	Hardware capture flag
69	ACCFLT2	INPUT	Accessory Fault Flag	For loss of ACC supply voltage
70	WD0/	OUTPUT	Watchdog Output	Low is PMAC watchdog fault
71	SCLK12+	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC2 jumper
72	SCLK12-	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC2 jumper
73	ADC_CLK2+	OUTPUT	A/D Converter Clock	Programmable frequency
74	ADC_CLK2-	OUTPUT	A/D Converter Clock	Programmable frequency
75	ADC_STB2+	OUTPUT	A/D Converter Strobe	Programmable sequence
76	ADC_STB2-	OUTPUT	A/D Converter Strobe	Programmable sequence
77	ADC_DAA2+	INPUT	Channel A ADC Serial Data	MSB First
78	ADC_DAA2-	INPUT	Channel A ADC Serial Data	MSB First
79	ADC_DAB2+	INPUT	Channel B ADC Serial Data	MSB First
80	ADC_DAB2-	INPUT	Channel B ADC Serial Data	MSB First
81	AENA2+	OUTPUT	Amplifier Enable	High is enable
82	AENA2-	OUTPUT	Amplifier Enable	Low is enable
83	FAULT2+	INPUT	Amplifier Fault	Programmable polarity
84	FAULT2-	INPUT	Amplifier Fault	Programmable polarity
85	PWMATOP2+ DAC_CLK2+	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
86	PWMATOP2- DAC_CLK2-	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
87	PWMABOT2+ DAC2A+	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control
88	PWMABOT2- DAC2A-	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control
89	PWMBTOP2+ DAC_STB2+	OUTPUT	Phase B Top CMD or DAC Strobe	Programmable function control
90	PWMBTOP2- DAC_STB2-	OUTPUT	Phase B Top CMD or DAC Strobe	Programmable function control
91	PWMBBOT2+ DAC2B+	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
92	PWMBBOT2- DAC2B-	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
93	PWMCTOP2+ DIR2+	OUTPUT	Phase B Top CMD or PFM Direction	Programmable function control
94	PWMCTOP2- DIR2-	OUTPUT	Phase B Top CMD or PFM Direction	Programmable function control
95	PWMCBOT2+ PULSE2+	OUTPUT	Phase B Bottom CMD or PFM Pulse	Programmable function control
96	PWMCBOT2- PULSE2-	OUTPUT	Phase B Bottom CMD or PFM Pulse	Programmable function control
97	GND	COMMON	Reference Voltage	
98	GND	COMMON	Reference Voltage	

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99	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
100	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply

The JMACH1 connector provides the interface pins for channels 1 and 2. It is usually connected to a breakout board, such as one of the ACC-8 (Series) family of boards, or an application-specific interface board.
Note: 100-pin male box header with center key, 0050" pitch. AMP part # 1-04068-7. Delta Tau part # 014-00010-FPB.

J10 (JMACH2) Connector Description



Front View

Pin#	Symbol	Function	Description	Notes
1	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
2	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
3	GND	COMMON	Reference Voltage	
4	GND	COMMON	Reference Voltage	
5	CHA3+	INPUT	Encoder 3 Positive A Channel	Also pulse input
6	CHA3-	INPUT	Encoder 3 Negative A Channel	Also pulse input
7	CHB3+	INPUT	Encoder 3 Positive B Channel	Also direction input
8	CHB3-	INPUT	Encoder 3 Negative B Channel	Also direction input
9	CHC3+	INPUT	Encoder 3 Positive C Channel	Index channel
10	CHC3-	INPUT	Encoder 3 Negative C Channel	Index channel
11	CHU3	INPUT	Channel 3 U Flag	Hall effect, fault code, or sub-count
12	CHV3	INPUT	Channel 3 V Flag	Hall effect, fault code, or sub-count
13	CHW3	INPUT	Channel 3 W Flag	Hall effect, fault code, or sub-count
14	CHT3	INPUT	Channel 3 T Flag	Fault code, or sub-count
15	USER3	INPUT	General Purpose User Flag	Hardware capture flag, or sub-count
16	PLIM3	INPUT	Positive Overtravel Limit	Hardware capture flag
17	MLIM3	INPUT	Negative Overtravel Limit	Hardware capture flag
18	HOME3	INPUT	Home Switch Input	Hardware capture flag
19	ACCFLT3	INPUT	Accessory Fault Flag	For loss of acc supply voltage
20	WD0/	OUTPUT	Watchdog Output	Low is PMAC watchdog fault
21	SCLK34+	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC2 jumper
22	SCLK34-	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC2 jumper
23	ADC_CLK3+	OUTPUT	A/D Converter Clock	Programmable frequency
24	ADC_CLK3-	OUTPUT	A/D Converter Clock	Programmable frequency
25	ADC_STB3+	OUTPUT	A/D Converter Strobe	Programmable frequency
26	ADC_STB3-	OUTPUT	A/D Converter Strobe	Programmable frequency
27	ADC_DAA3+	INPUT	Channel A ADC Serial Data	MSB first
28	ADC_DAA3-	INPUT	Channel A ADC Serial Data	MSB first
29	ADC_DAB3+	INPUT	Channel B ADC Serial Data	MSB first
30	ADC_DAB3-	INPUT	Channel B ADC Serial Data	MSB first
31	AENA3+	OUTPUT	Amplifier Enable	High is enable
32	AENA3-	OUTPUT	Amplifier Enable	Low is enable
33	FAULT3+	INPUT	Amplifier Fault	Programmable polarity

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34	FAULT3-	INPUT	Amplifier Fault	Programmable polarity
35	PWMATOP3+ DAC_CLK3+	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
36	PWMATOP3- DAC_CLK3-	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
37	PWMABOT3+ DAC3A+	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control
38	PWMABOT3- DAC3A-	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control
39	PWMBTOP3+ DAC_STB3+	OUTPUT	Phase B Top CMD or DAC Strobe	Programmable function control
40	PWMBTOP3- DAC_STB3-	OUTPUT	Phase B Top CMD or DAC Strobe	Programmable function control
41	PWMBBOT3+ DAC3B+	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
42	PWMBBOT3- DAC3B-	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
43	PWMCTOP3+ DIR3+	OUTPUT	Phase B Top CMD or PFM Direction	Programmable function control
44	PWMCTOP3- DIR3-	OUTPUT	Phase B Top CMD or PFM Direction	Programmable function control
45	PWMCBOT3+ PULSE3+	OUTPUT	Phase B Bottom CMD or PFM Pulse	Programmable function control
46	PWMCBOT3- PULSE3-	OUTPUT	Phase B Bottom CMD or PFM Pulse	Programmable function control
47	GND	COMMON	Reference Voltage	
48	GND	COMMON	Reference Voltage	
49	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
50	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
51	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
52	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
53	GND	COMMON	Reference Voltage	
54	GND	COMMON	Reference Voltage	
55	CHA4+	INPUT	Encoder 4 Positive A Channel	Also pulse input
56	CHA4-	INPUT	Encoder 4 Negative A Channel	Also pulse input
57	CHB4+	INPUT	Encoder 4 Positive B Channel	Also direction input
58	CHB4-	INPUT	Encoder 4 Negative B Channel	Also direction input
59	CHC4+	INPUT	Encoder 4 Positive C Channel	Index channel
60	CHC4-	INPUT	Encoder 4 Negative C Channel	Index channel
61	CHU4	INPUT	Channel 4 U Flag	Hall effect, fault code, or sub-count
62	CHV4	INPUT	Channel 4 V Flag	Hall effect, fault code, or sub-count
63	CHW4	INPUT	Channel 4 W Flag	Hall effect, fault code, or sub-count
64	CHT4	INPUT	Channel 4 T Flag	Fault code, or sub-count
65	USER4	INPUT	General Purpose User Flag	Hardware capture flag, or sub-count
66	PLIM4	INPUT	Positive Overtravel Limit	Hardware capture flag
67	MLIM4	INPUT	Negative Overtravel Limit	Hardware capture flag

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68	HOME4	INPUT	Home Switch Input	Hardware capture flag
69	ACCFLT4	INPUT	Accessory Fault Flag	For loss of ACC supply voltage
70	WD0/	OUTPUT	Watchdog Output	Low is PMAC watchdog fault
71	SCLK34+	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC2 jumper
72	SCLK34-	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC2 jumper
73	ADC_CLK4+	OUTPUT	A/D Converter Clock	Programmable frequency
74	ADC_CLK4-	OUTPUT	A/D Converter Clock	Programmable frequency
75	ADC_STB4+	OUTPUT	A/D Converter Strobe	Programmable sequence
76	ADC_STB4-	OUTPUT	A/D Converter Strobe	Programmable sequence
77	ADC_DAA4+	INPUT	Channel A ADC Serial Data	MSB First
78	ADC_DAA4-	INPUT	Channel A ADC Serial Data	MSB First
79	ADC_DAB4+	INPUT	Channel B ADC Serial Data	MSB First
80	ADC_DAB4-	INPUT	Channel B ADC Serial Data	MSB First
81	AENA4+	OUTPUT	Amplifier Enable	High is enable
82	AENA4-	OUTPUT	Amplifier Enable	Low is enable
83	FAULT4+	INPUT	Amplifier Fault	Programmable polarity
84	FAULT4-	INPUT	Amplifier Fault	Programmable polarity
85	PWMATOP4+ DAC_CLK4+	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
86	PWMATOP4- DAC_CLK4-	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
87	PWMABOT4+ DAC4A+	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control
88	PWMABOT4- DAC4A-	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control
89	PWMBTOP4+ DAC_STB4+	OUTPUT	Phase B Top CMD or DAC Strobe	Programmable function control
90	PWMBTOP4- DAC_STB4-	OUTPUT	Phase B Top CMD or DAC Strobe	Programmable function control
91	PWMBBOT4+ DAC4B+	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
92	PWMBBOT4- DAC4B-	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
93	PWMCTOP4+ DIR4+	OUTPUT	Phase B Top CMD or PFM Direction	Programmable function control
94	PWMCTOP4- DIR4-	OUTPUT	Phase B Top CMD or PFM Direction	Programmable function control
95	PWMCBOT4+ PULSE4+	OUTPUT	Phase B Bottom CMD or PFM Pulse	Programmable function control
96	PWMCBOT4- PULSE4-	OUTPUT	Phase B Bottom CMD or PFM Pulse	Programmable function control
97	GND	COMMON	Reference Voltage	
98	GND	COMMON	Reference Voltage	
99	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
100	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply

The JMACH2 connector provides the interface pins for channels 3 and 4. It is usually connected to a breakout board, such as one of the ACC-8(Series) family of boards, or an application- specific interface board.
Note: 100-pin male box header with center key, 050" pitch. AMP part # 1-04068-7. Delta Tau part # 014-00010-FPB.

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J11 (JMACH3) Connector Description



Pin#	Symbol	Function	Description	Notes
1	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
2	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
3	GND	COMMON	Reference Voltage	
4	GND	COMMON	Reference Voltage	
5	CHA5+	INPUT	Encoder 5 Positive A Channel	Also pulse input
6	CHA5-	INPUT	Encoder 5 Negative A Channel	Also pulse input
7	CHB5+	INPUT	Encoder 5 Positive B Channel	Also direction input
8	CHB5-	INPUT	Encoder 5 Negative B Channel	Also direction input
9	CHC5+	INPUT	Encoder 5 Positive C Channel	Index channel
10	CHC5-	INPUT	Encoder 5 Negative C Channel	Index channel
11	CHU5	INPUT	Channel 5 U Flag	Hall effect, fault code, or sub-count
12	CHV5	INPUT	Channel 5 V Flag	Hall effect, fault code, or sub-count
13	CHW5	INPUT	Channel 5 W Flag	Hall effect, fault code, or sub-count
14	CHT5	INPUT	Channel 5 T Flag	Fault code, or sub-count
15	USER5	INPUT	General Purpose User Flag	Hardware capture flag, or sub-count
16	PLIM5	INPUT	Positive Overtravel Limit	Hardware capture flag
17	MLIM5	INPUT	Negative Overtravel Limit	Hardware capture flag
18	HOME5	INPUT	Home Switch Input	Hardware capture flag
19	ACCFLT5	INPUT	Accessory Fault Flag	For loss of ACC supply voltage
20	WD0/	OUTPUT	Watchdog Output	Low is PMAC watchdog fault
21	SCLK56+	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC2 jumper
22	SCLK56-	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC2 jumper
23	ADC_CLK5+	OUTPUT	A/D Converter Clock	Programmable frequency
24	ADC_CLK5-	OUTPUT	A/D Converter Clock	Programmable frequency
25	ADC_STB5+	OUTPUT	A/D Converter Strobe	Programmable sequence
26	ADC_STB5-	OUTPUT	A/D Converter Strobe	Programmable sequence
27	ADC_DAA5+	INPUT	Channel A ADC Serial Data	MSB First
28	ADC_DAA5-	INPUT	Channel A ADC Serial Data	MSB First
29	ADC_DAB5+	INPUT	Channel B ADC Serial Data	MSB First
30	ADC_DAB5-	INPUT	Channel B ADC Serial Data	MSB First
31	AENA5+	OUTPUT	Amplifier Enable	High is enable
32	AENA5-	OUTPUT	Amplifier Enable	Low is enable
33	FAULT5+	INPUT	Amplifier Fault	Programmable polarity
34	FAULT5-	INPUT	Amplifier Fault	Programmable polarity
35	PWMATOP5+ DAC_CLK5+	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
36	PWMATOP5- DAC_CLK5-	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
37	PWMABOT5+ DAC5A+	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control
38	PWMABOT5- DAC5A-	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control

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39	PWMBTOP5+ DAC_STB5+	OUTPUT	Phase B Top CMD or DAC Strobe	Programmable function control
40	PWMBTOP5- DAC_STB5-	OUTPUT	Phase B Top CMD or DAC Strobe	Programmable function control
41	PWMBBOT5+ DAC5B+	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
42	PWMBBOT5- DAC5B-	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
43	PWMCTOP5+ DIR5+	OUTPUT	Phase B Top CMD or PFM Direction	Programmable function control
44	PWMCTOP5- DIR5-	OUTPUT	Phase B Top CMD or PFM Direction	Programmable function control
45	PWMCBOT5+ PULSE5+	OUTPUT	Phase B Bottom CMD or PFM Pulse	Programmable function control
46	PWMCBOT5- PULSE5-	OUTPUT	Phase B Bottom CMD or PFM Pulse	Programmable function control
47	GND	COMMON	Reference Voltage	
48	GND	COMMON	Reference Voltage	
49	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
50	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
51	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
52	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
53	GND	COMMON	Reference Voltage	
54	GND	COMMON	Reference Voltage	
55	CHA6+	INPUT	Encoder 6 Positive A Channel	Also pulse input
56	CHA6-	INPUT	Encoder 6 Negative A Channel	Also pulse input
57	CHB6+	INPUT	Encoder 6 Positive B Channel	Also direction input
58	CHB6-	INPUT	Encoder 6 Negative B Channel	Also direction input
59	CHC6+	INPUT	Encoder 6 Positive C Channel	Index channel
60	CHC6-	INPUT	Encoder 6 Negative C Channel	Index channel
61	CHU6	INPUT	Channel 6 U Flag	Hall effect, fault code, or sub-count
62	CHV6	INPUT	Channel 6 V Flag	Hall effect, fault code, or sub-count
63	CHW6	INPUT	Channel 6 W Flag	Hall effect, fault code, or sub-count
64	CHT6	INPUT	Channel 6 T Flag	Fault code, or sub-count
65	USER6	INPUT	General Purpose User Flag	Hardware capture flag, or sub-count
66	PLIM6	INPUT	Positive Overtravel Limit	Hardware capture flag
67	MLIM6	INPUT	Negative Overtravel Limit	Hardware capture flag
68	HOME6	INPUT	Home Switch Input	Hardware capture flag
69	ACCFLT6	INPUT	Accessory Fault Flag	For loss of ACC supply voltage
70	WD0/	OUTPUT	Watchdog Output	Low is PMAC watchdog fault
71	SCLK56+	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC 2 jumper
72	SCLK56-	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC 2 jumper
73	ADC_CLK6+	OUTPUT	A/D Converter Clock	Programmable frequency
74	ADC_CLK6-	OUTPUT	A/D Converter Clock	Programmable frequency

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75	ADC_STB6+	OUTPUT	A/D Converter Strobe	Programmable sequence
76	ADC_STB6-	OUTPUT	A/D Converter Strobe	Programmable sequence
77	ADC_DAA6+	INPUT	Channel A ADC Serial Data	MSB first
78	ADC_DAA6-	INPUT	Channel A ADC Serial Data	MSB first
79	ADC_DAB6+	INPUT	Channel B ADC Serial Data	MSB first
80	ADC_DAB6-	INPUT	Channel B ADC Serial Data	MSB first
81	AENA6+	OUTPUT	Amplifier Enable	High is enable
82	AENA6-	OUTPUT	Amplifier Enable	Low is enable
83	FAULT6+	INPUT	Amplifier Fault	Programmable polarity
84	FAULT6-	INPUT	Amplifier Fault	Programmable polarity
85	PWMATOP6+ DAC_CLK6+	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
86	PWMATOP6- DAC_CLK6-	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
87	PWMABOT6+ DAC6A+	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control
88	PWMABOT6- DAC6A-	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control
89	PWMBTOP6+ DAC_STB6+	OUTPUT	Phase B Top CMD or DAC Strobe	Programmable function control
90	PWMBTOP6- DAC_STB6-	OUTPUT	Phase B Top CMD or DAC Strobe	Programmable function control
91	PWMBBOT6+ DAC6B+	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
92	PWMBBOT6- DAC6B-	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
93	PWMCTOP6+ DIR6+	OUTPUT	Phase B Top CMD or PFM Direction	Programmable function control
94	PWMCTOP6- DIR6-	OUTPUT	Phase B Top CMD or PFM Direction	Programmable function control
95	PWMCBOT6+ PULSE6+	OUTPUT	Phase B Bottom CMD or PFM PULSE	Programmable function control
96	PWMCBOT6- PULSE6-	OUTPUT	Phase B Bottom CMD or PFM PULSE	Programmable function control
97	GND	COMMON	Reference Voltage	
98	GND	COMMON	Reference Voltage	
99	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
100	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply

The JMACH3 connector (not present on PMAC2-Lite) provides the interface pins for channels 5 and 6. It is usually connected to a breakout board, such as one of the ACC-8(Series) family of boards, or an application-specific interface board.

Note: 100-pin male box header with center key, 0050" pitch. AMP part # 1-04068-7. Delta Tau part # 014-00010-FPB.

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J12 (JMACH4) Connector Description



Pin#	Symbol	Function	Description	Notes
1	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
2	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
3	GND	COMMON	Reference Voltage	
4	GND	COMMON	Reference Voltage	
5	CHA7+	INPUT	Encoder 7 Positive A Channel	Also pulse input
6	CHA7-	INPUT	Encoder 7 Negative A Channel	Also pulse input
7	CHB7+	INPUT	Encoder 7 Positive B Channel	Also direction input
8	CHB7-	INPUT	Encoder 7 Negative B Channel	Also direction input
9	CHC7+	INPUT	Encoder 7 Positive C Channel	Index channel
10	CHC7-	INPUT	Encoder 7 Negative C Channel	Index channel
11	CHU7	INPUT	Channel 7 U Flag	Hall effect, fault code, or sub-count
12	CHV7	INPUT	Channel 7 V Flag	Hall effect, fault code, or sub-count
13	CHW7	INPUT	Channel 7 W Flag	Hall effect, fault code, or sub-count
14	CHT7	INPUT	Channel 7 T Flag	Fault code, or sub-count
15	USER7	INPUT	General Purpose User Flag	Hardware capture flag, or sub-count
16	PLIM7	INPUT	Positive Overtravel Limit	Hardware capture flag
17	MLIM7	INPUT	Negative Overtravel Limit	Hardware capture flag
18	HOME7	INPUT	Home Switch Input	Hardware capture flag
19	ACCFLT7	INPUT	Accessory Fault Flag	For loss of ACC supply voltage
20	WD0/	OUTPUT	Watchdog Output	Low is PMAC watchdog fault
21	SCLK78+	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC2 jumper
22	SCLK78-	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC2 jumper
23	ADC_CLK7+	OUTPUT	A/D Converter Clock	Programmable frequency
24	ADC_CLK7-	OUTPUT	A/D Converter Clock	Programmable frequency
25	ADC_STB7+	OUTPUT	A/D Converter Strobe	Programmable sequence
26	ADC_STB7-	OUTPUT	A/D Converter Strobe	Programmable sequence
27	ADC_DAA7+	INPUT	Channel A ADC Serial Data	MSB first
28	ADC_DAA7-	INPUT	Channel A ADC Serial Data	MSB first
29	ADC_DAB7+	INPUT	Channel B ADC Serial Data	MSB first
30	ADC_DAB7-	INPUT	Channel B ADC Serial Data	MSB first
31	AENA7+	OUTPUT	Amplifier Enable	High is enable
32	AENA7-	OUTPUT	Amplifier Enable	Low is enable
33	FAULT7+	INPUT	Amplifier Fault	Programmable polarity
34	FAULT7-	INPUT	Amplifier Fault	Programmable polarity
35	PWMATOP7+ DAC_CLK7+	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
36	PWMATOP7- DAC_CLK7-	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
37	PWMABOT7+ DAC7A+	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control

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38	PWMABOT7- DAC7A-	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control
39	PWMBTOP7+ DAC_STB7+	OUTPUT	Phase B Top CMD or DAC Strobe	Programmable function control
40	PWMBTOP3- DAC_STB7-	OUTPUT	Phase B Top CMD or DAC Strobe	Programmable function control
41	PWMBBOT7+ DAC7B+	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
42	PWMBBOT7- DAC7B-	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
43	PWMCTOP7+ DIR7+	OUTPUT	Phase B Top CMD or PFM Direction	Programmable function control
44	PWMCTOP7- DIR7-	OUTPUT	Phase B Top CMD or PFM Direction	Programmable function control
45	PWMCBOT7+ PULSE7+	OUTPUT	Phase B Bottom CMD or PFM Pulse	Programmable function control
46	PWMCBOT7- PULSE7-	OUTPUT	Phase B Bottom CMD or PFM Pulse	Programmable function control
47	GND	COMMON	Reference Voltage	
48	GND	COMMON	Reference Voltage	
49	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
50	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
51	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
52	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
53	GND	COMMON	Reference Voltage	
54	GND	COMMON	Reference Voltage	
55	CHA8+	INPUT	Encoder 8 Positive A Channel	Also pulse input
56	CHA8-	INPUT	Encoder 8 Negative A Channel	Also pulse input
57	CHB8+	INPUT	Encoder 8 Positive B Channel	Also direction input
58	CHB8-	INPUT	Encoder 8 Negative B Channel	Also direction input
59	CHC8+	INPUT	Encoder 8 Positive C Channel	Index channel
60	CHC8-	INPUT	Encoder 8 Negative C Channel	Index channel
61	CHU8	INPUT	Channel 8 U Flag	Hall effect, fault code, or sub-count
62	CHV8	INPUT	Channel 8 V Flag	Hall effect, fault code, or sub-count
63	CHW8	INPUT	Channel 8 W Flag	Hall effect, fault code, or sub-count
64	CHT8	INPUT	Channel 8 T Flag	Fault code, or sub-count
65	USER8	INPUT	General Purpose User Flag	Hardware capture flag, or sub-count
66	PLIM8	INPUT	Positive Overtravel Limit	Hardware capture flag
67	MLIM8	INPUT	Negative Overtravel Limit	Hardware capture flag
68	HOME8	INPUT	Home Switch Input	Hardware capture flag
69	ACCFLT8	INPUT	Accessory Fault Flag	For loss of ACC supply voltage
70	WD0/	OUTPUT	Watchdog Output	Low is PMAC watchdog fault
71	SCLK78+	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC2 jumper
72	SCLK78-	INPUT / OUTPUT	Encoder Sample Clock	Direction controlled by PMAC2 jumper

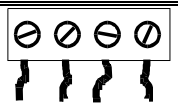
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73	ADC_CLK8+	OUTPUT	A/D Converter Clock	Programmable frequency
74	ADC_CLK8-	OUTPUT	A/D Converter Clock	Programmable frequency
75	ADC_STB8+	OUTPUT	A/D Converter Strobe	Programmable sequence
76	ADC_STB8-	OUTPUT	A/D Converter Strobe	Programmable sequence
77	ADC_DAA8+	INPUT	Channel A ADC Serial Data	MSB first
78	ADC_DAA8-	INPUT	Channel A ADC Serial Data	MSB first
79	ADC_DAB8+	INPUT	Channel B ADC Serial Data	MSB first
80	ADC_DAB8-	INPUT	Channel B ADC Serial Data	MSB first
81	AENA8+	OUTPUT	Amplifier Enable	High is enable
82	AENA8-	OUTPUT	Amplifier Enable	Low is enable
83	FAULT8+	INPUT	Amplifier Fault	Programmable polarity
84	FAULT8-	INPUT	Amplifier Fault	Programmable polarity
85	PWMATOP8+ DAC_CLK8+	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
86	PWMATOP8- DAC_CLK8-	OUTPUT	Phase A Top CMD or DAC Clock	Programmable function control
87	PWMABOT8+ DAC8A+	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control
88	PWMABOT8- DAC8A-	OUTPUT	Phase A Bottom CMD or DAC A Serial Data	Programmable function control
89	PWMBTOP8+ DAC_STB8+	OUTPUT	Phase B Top CMD or DAC Strobe	Programmable function control
90	PWMBTOP8- DAC_STB8-	OUTPUT	Phase B Top CMD or DAC Strobe	Programmable function control
91	PWMBBOT8+ DAC8B+	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
92	PWMBBOT8- DAC8B-	OUTPUT	Phase B Bottom CMD or DAC B Serial Data	Programmable function control
93	PWMCTOP8+ DIR8+	OUTPUT	Phase B Top CMD or PFM Direction	Programmable function control
94	PWMCTOP8- DIR8-	OUTPUT	Phase B Top CMD or PFM Direction	Programmable function control
95	PWMCBOT8+ PULSE8+	OUTPUT	Phase B Bottom CMD or PFM Pulse	Programmable function control
96	PWMCBOT8- PULSE8-	OUTPUT	Phase B Bottom CMD or PFM Pulse	Programmable function control
97	GND	COMMON	Reference Voltage	
98	GND	COMMON	Reference Voltage	
99	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply
100	+5V	OUTPUT / INPUT	+5V Power	For external circuit or from external supply

Note: 100-pin male box header with center key, 0050" pitch. AMP part # 1-04068-7. Delta Tau part # 014-00010-FPB.
The JMACH4 connector (Not present on PMAC2-Lite) provides the interface pins for channels 7 and 8. It is usually connected to a breakout board, such as one of the ACC-8(Series) family of boards, or an application-specific interface board.

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TB1 (2/4-Pin Terminal Block)


Front View

Pin#	Symbol	Function	Description	Notes
1	GND	COMMON	Reference Voltage	
2	+5V	INPUT	Positive Supply Voltage	Supplies all PMAC digital circuits
3	+12V	INPUT	Positive Supply Voltage	+12V to +15V; not required on-board; used on J1 to supply analog inputs
4	-12V	INPUT	Negative Supply Voltage	-12V to -15V; required for OPT-12 ADCS; used on J1 to supply analog inputs

Note: Unless Option 12 (Analog-to-Digital Converters) is included on the board, only pins 1 and 2 will be provided on this terminal block.
This terminal block can be used to provide the input for the power supply for the circuits on the PMAC2 board when it is not in a bus configuration. When the PMAC2 is in a bus configuration, these supplies automatically come through the bus connector from the bus power supply. In this case, this terminal block should not be used.

TB2 (3-Pin Terminal Block)


Front View

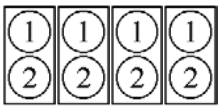
Pin#	Symbol	Function	Description	Notes
1	WD_NC	OUTPUT	Watchdog Relay Out	Normally closed
2	COM	INPUT	Watchdog Return	+V or 0V
3	WD_NO	OUTPUT	Watchdog Relay Out	Normally open

This terminal block provides the output for the PMAC2 watchdog timer relay, both normally open and normally closed contacts. The normally closed relay contact is open while PMAC2 is operating properly -- it has power and the watchdog timer is not tripped -- and closed when the PMAC2 is not operating properly -- either it has lost power or the watchdog timer has tripped.

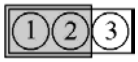
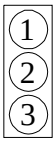
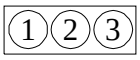
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PMAC2-PC and PMAC2-Lite Jumper Summary

Refer to the PMAC2-PC and PMAC2-Lite layout diagram (see Figure 2-1) for jumper locations.

E Point & Physical Layout	Location	Description	Default
E1 	D1	**Card 0 Jumper:** Remove jumper to specify that this PMAC is Card 0, which generates its own phase and servo clock (default). Jump pins 1 to 2 to specify that this PMAC is not Card 0, but Card 1 to F (15), which requires external phase and servo clock signals from the serial port to operate.	No Jumper
E2 	D1	**40/60 MHz Jumper:** Remove jumper to specify 40 MHz operation of the PMAC CPU (2 x crystal frequency). Default setting for standard (40 MHz) CPU. Jump pins 1 to 2 to specify 60 MHz operation of the PMAC CPU (3 x crystal frequency). Default setting for Option 5B (60 MHz) CPU.	No Jumper
E3 	D1	**Re-initialize Jumper:** Remove jumper for normal reset mode (default) Jump pins 1 to 2 for re-initialization on reset	No Jumper
E4 	D1	**80MHz Jumper:** Remove jumper for 40/60 MHz operation (ref Jumper E2) Install jumper for 80MHz operation.	No Jumper
E5 and E6 	D1	Reserved for future use	No Jumper
E7 thru E10 	C1	**Interrupt Select:** Jump E7 pins 1 to 2 to interrupt PC on IRQ10 Jump E8 pins 1 to 2 to interrupt PC on IRQ11 Jump E9 pins 1 to 2 to interrupt PC on IRQ12 Jump E10 pins 1 to 2 to interrupt PC on IRQ15	No Jumper **Note:** Only 1 jumper of E7 thru E10 should be on at one time.
E11 	H2	**JEQU Port Configuration:** Jump pins 1 to 2 for sinking driver (ULN2803A) on port (default configuration) Jump pins 2 to 3 for sourcing driver (UDN2981A) on port (alternate configuration)	1 - 2 Jumpered

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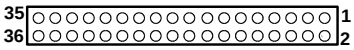
E Point & Physical Layout	Location	Description	Default
E12  	H2	**JEQU Port Configuration:** Jump pins 1 to 2 for sinking driver (ULN2803A) on JEQU port (default configuration) Jump pins 2 to 3 for sourcing driver (UDN2981A) on JEQU port (alternate configuration)	1 - 2 Jumpered
E13  	F1	**Encoder Sample Clock Direction:** Remove jumper to output SCLK generated in first ASIC on SCLK_12 and SCLK_34, or to control direction by software. Jump pins 1 to 2 to input SCLK signal for first ASIC on SCLK_34 and output this signal on SCLK_12. Jump pins 2 to 3 to input SCLK signal for first ASIC on SCLK_12 and output this signal on SCLK_34.	No Jumper
E14  PMAC2-PC	D1	**Encoder Sample Clock Direction:** Remove jumper to output SCLK generated in second ASIC on SCLK_56 and SCLK_78, or to control direction by software. Jump pins 1 to 2 to input SCLK signal for second ASIC on SCLK_78 and output this signal on SCLK_56. Jump pins 2 to 3 to input SCLK signal for second ASIC on SCLK_56 and output this signal on SCLK_78	No Jumper
E14  PMAC2-Lite	F2	**Watchdog Timer Control:** Remove jumper to enable watchdog timer operation. Jump pins 1 to 2 to disable watchdog timer operation (for test purposes only).	No Jumper

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PMAC2-VME CPU Connector Summary

The following paragraphs provide a brief description of each connector on the PMAC2-PC CPUs (see Figure 2-2).

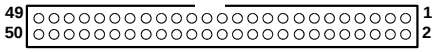
J1



Front View

36-pin header on backside for connection to main PMAC/PMAC2 board.

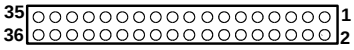
J2 (JEXP)



Front View

50-pin IDC header for connection to expansion port accessory boards.

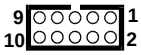
J3



Front View

36-pin header on backside for connection to main PMAC/PMAC2 board.

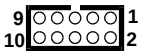
J4 (JEXP)



Front View

10-pin IDC header for connection to DPRAM on accessory board (PMAC-PC) or main PMAC board (PMAC-VME, PMAC2-PC, PMAC2-VME).

J5 (JTAG/OnCE)



Front View

10-pin header for factory use only.

J6



Front View

8-pin SIP header for factory use only.

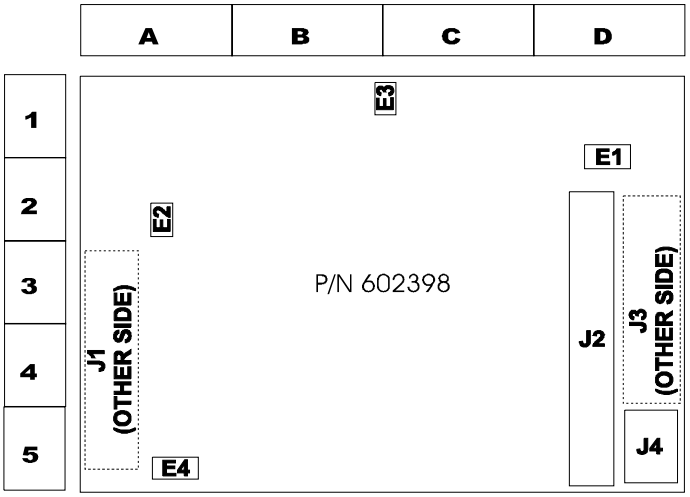
J7

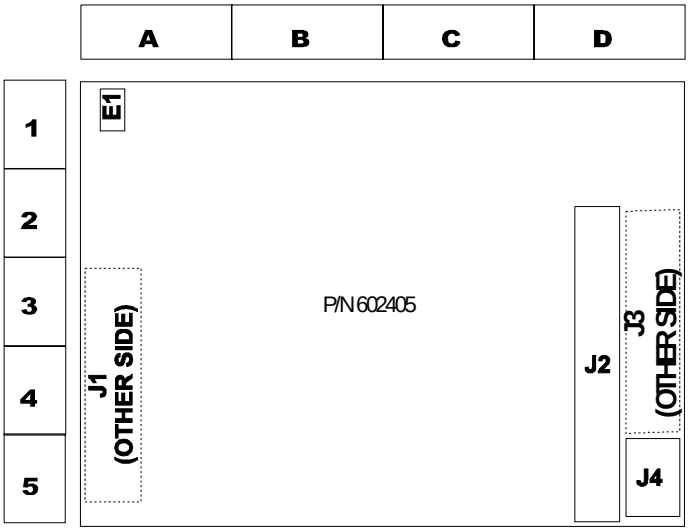


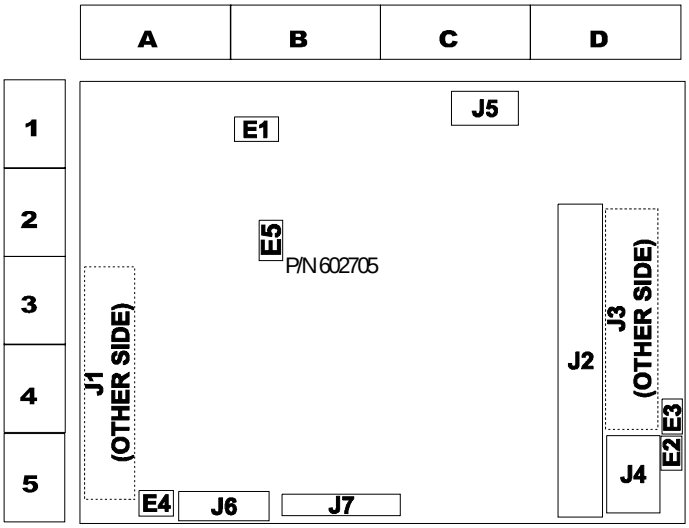
Front View

8-pin SIP header for factory use only.

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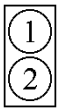
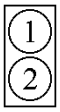
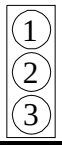






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PMAC2-PC CPU Piggyback Board Jumpers

E Point & Physical Layout	Location	Description	Default
E1 	D1 (602398) A1 (602405) B1 (602705)	Remove jumper to enable watchdog timer operation. Jump pins 1 to 2 to disable watchdog timer operation (for test purposes only).	No Jumper
E2 	A2 (602398) D5 (602705)	Remove jumper to disable extended channel addressing (Channels 9-16). Jump pins 1 to 2 to enable extended channel addressing (Channels 9-16)	No Jumper
E3 	C1 (602398) D4 (602705)	Remove jumper (or no jumper present) to disable extended channel addressing (Channels 9-16). Jump pins 1 to 2 to enable extended channel addressing (Channels 9-16)	No Jumper
E4 	A5 (602398) B1 (602705)	Boot Enable Jumper. Remove jumper for normal use. Jump pins 1 and 2 for external firmware load (with MAIN board E3 on).	No Jumper
E5 	B3 (602705)	Battery-backed RAM Size Select - Jump pins 2 and 3 for supple-mental battery-backed memory (Option 16 only). No Jumper if no battery-backed memory	No Jumper

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