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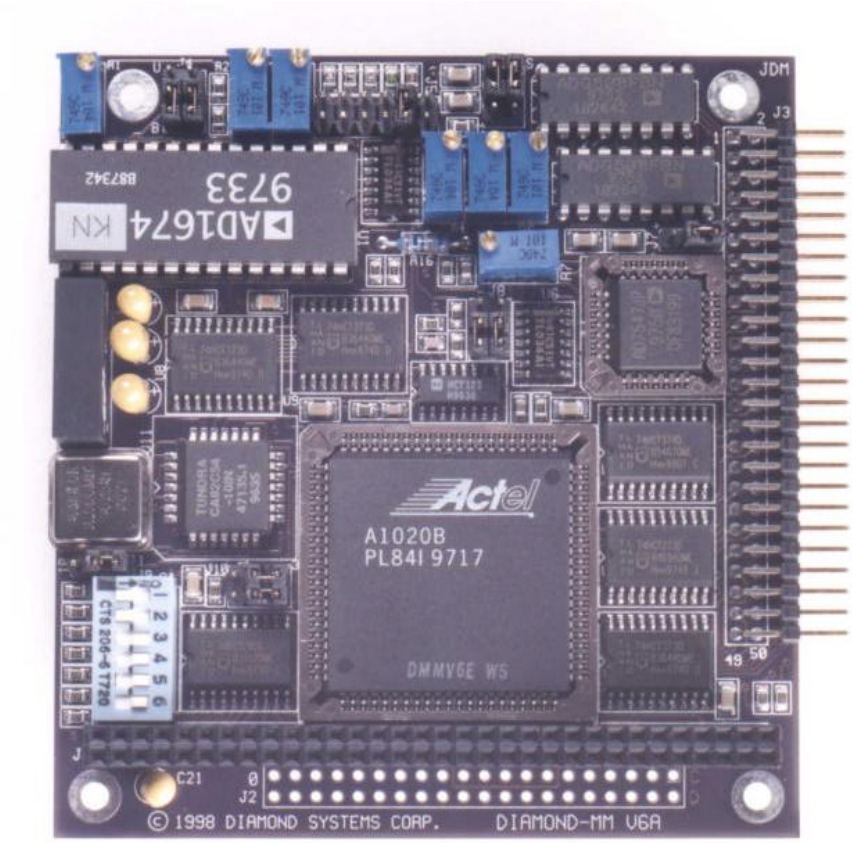
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DIAMOND SYSTEMS CORPORATION

DIAMOND-MM

Multifunction Analog I/O PC/104 Module

User Manual V2.2



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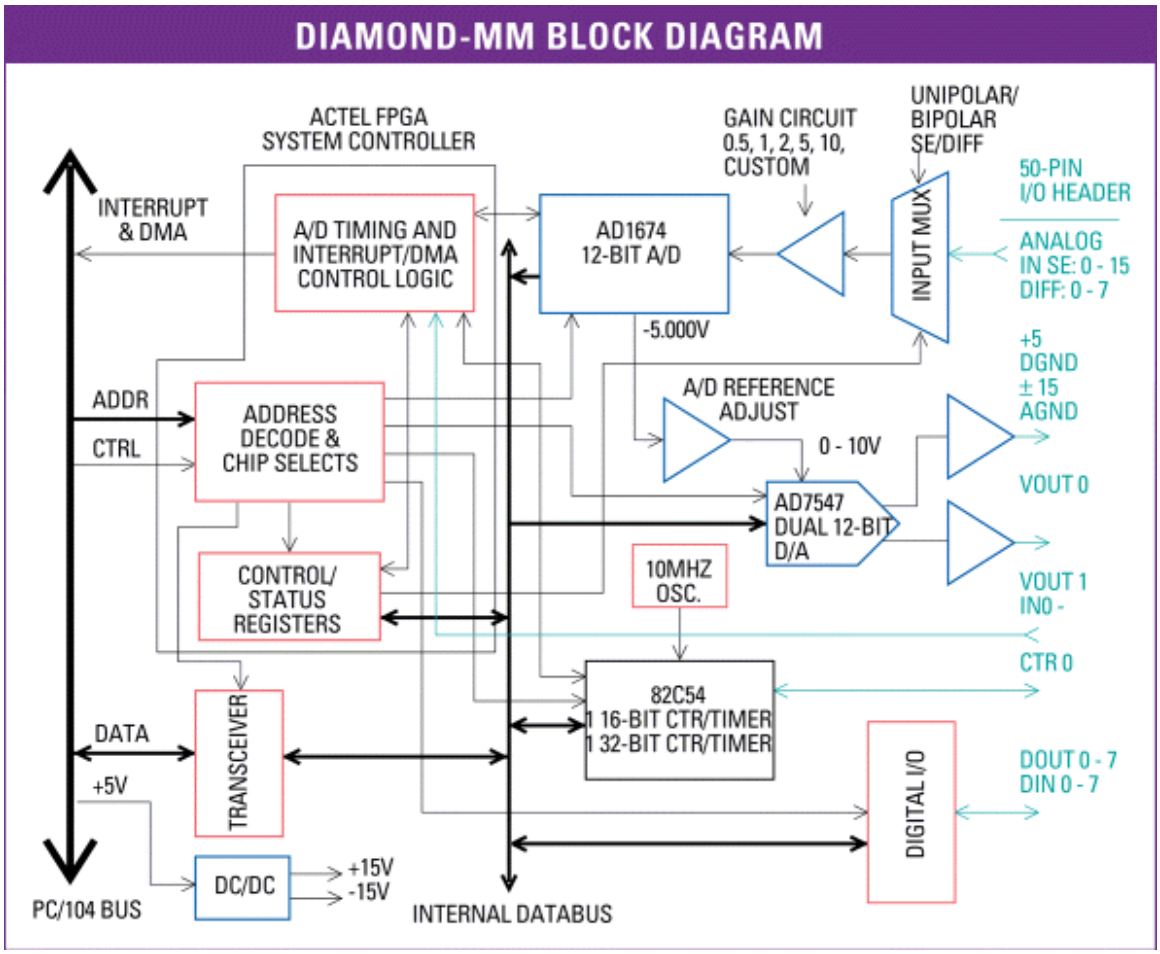
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1. DESCRIPTION

Diamond-MM is a PC/104-format data acquisition board containing a wide range of analog and digital I/O features. It offers 16 single-ended or 8 differential analog inputs with 12-bit resolution; gains of 0.5, 1, 2, 5, 10, and User; 100,000 samples per second with DMA operation; 2 optional analog outputs with 12-bit resolution (-NA versions do not have analog outputs); user-adjustable analog output range; 8 bits of digital input; 8 bits of digital output; one 32-bit counter/timer for A/D conversion timing; and one 16-bit counter/timer for general purpose use. The board is compatible with Keithley/MetraByte's DAS-16F ISA-bus plug-in board.

Diamond-MM is available in four models:

DMM	Analog input and output, 0 to 70°C operating temperature
DMM-NA	Analog input only, 0 to 70°C operating temperature
DMM-XT	Analog input and output, -40 to +85°C operating temperature
DMM-NA-XT	Analog input only, -40 to +85°C operating temperature



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2. I/O HEADER PINOUT AND PIN DESCRIPTION

Diamond-MM provides a 50-pin header labeled J3 for all user I/O.

Vin 15 / 7-	1	2	Vin 7 / 7+
Vin 14 / 6-	3	4	Vin 6 / 6+
Vin 13 / 5-	5	6	Vin 5 / 5+
Vin 12 / 4-	7	8	Vin 4 / 4+
Vin 11 / 3-	9	10	Vin 3 / 3+
Vin 10 / 2-	11	12	Vin 2 / 2+
Vin 9 / 1-	13	14	Vin 1 / 1+
Vin 8 / 0-	15	16	Vin 0 / 0+
Agnd	17	18	Vref Out
Agnd	19	20	Vout 0
Agnd	21	22	Vout 1
Agnd	23	24	+15V
-15V	25	26	Vref In 0
Agnd	27	28	Vref In 1
In 0-	29	30	Dgnd
Out 0	31	32	Out 2
Dout 7	33	34	Dout 6
Dout 5	35	36	Dout 4
Dout 3	37	38	Dout 2
Dout 1	39	40	Dout 0
Din 7	41	42	Din 6
Din 5	43	44	Din 4
Din 3	45	46	Din 2 / Gate 0
Din 1	47	48	Din 0 / Gate 1/2
+5V	49	50	Dgnd

Signal Name	Definition
Vin 7/7+ ~ Vin 0/0+	Analog input channels 7 - 0 in single-ended mode; High side of input channels 7 - 0 in differential mode
Vin 15/7- ~ Vin 8/0-	Analog input channels 15 - 8 in both single-ended mode; Low side of input channels 7 - 0 in differential mode
Vout0, Vout 1	Analog output channels 0 and 1
Vref Out	+5V or -5V precision reference voltage output (user selectable)
Vref In 0, 1	External reference voltage inputs for custom D/A full-scale ranges
Dout7 - Dout0	Digital output port, TTL / CMOS compatible
Din7 - Din0	Digital input port, TTL / CMOS compatible
Din2 / Gate 0	Digital input line 2 doubles as the gate control for counter 0; Counter 0 counts when this line is high and holds when it is low
Din0 / Gate 1/2	Digital input line 0 doubles as a gate signal for counters 1 and 2 as determined by the control register at base + 11
In0-	Counter 0 input, negative polarity (negative edge trigger)
Out0, Out2	Counter 0 and Counter 2 output signals
±15V	Analog power supply; maximum current draw 10mA per line
+5V	Connected to PC/104 bus power supply
Agnd	Analog ground
Dgnd	Digital ground

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3. BOARD CONFIGURATION

Refer to the Drawing of Diamond-MM in chapter 4 for locations of the configuration items mentioned here.

3.1 Base Address

Each board in the system must have a different base address. Diamond-MM's base address is set with Dipswitch S1, located at the lower left corner of the board. Each of the six switches on S1 corresponds to a different address bit. An Off position is equal to a 1, and an On position is equal to a 0. The dipswitch is used to select address bits 9-4, resulting in a 16-byte I/O decode. The leftmost switch selects address bit A9, and the rightmost switch selects address bit A4. Although any 16-byte location is selectable, certain locations are reserved or may cause conflicts. The table below lists recommended base address settings for Diamond-MM. The default setting is 300 Hex.

Base Address		**Switch Position**					
Hex	**Decimal**	**1**	**2**	**3**	**4**	**5**	**6**
220	544	Off	On	On	On	Off	On
240	576	Off	On	On	Off	On	On
250	592	Off	On	On	Off	On	Off
260	608	Off	On	On	Off	Off	On
280	640	Off	On	Off	On	On	On
290	656	Off	On	Off	On	On	Off
2A0	672	Off	On	Off	On	Off	On
2B0	688	Off	On	Off	On	Off	Off
2C0	704	Off	On	Off	Off	On	On
2D0	720	Off	On	Off	Off	On	Off
2E0	736	Off	On	Off	Off	Off	On
300	768 (Default)	Off	Off	On	On	On	On
330	816	Off	Off	On	On	Off	Off
340	832	Off	Off	On	Off	On	On
350	848	Off	Off	On	Off	On	Off
360	864	Off	Off	On	Off	Off	On
380	896	Off	Off	Off	On	On	On
390	912	Off	Off	Off	On	On	Off
3A0	928	Off	Off	Off	On	Off	On
3C0	960	Off	Off	Off	Off	On	On
3E0	992	Off	Off	Off	Off	Off	On

3.2 Custom A/D Gain

Diamond-MM can be set for a custom gain on the A/D by selecting the "User" gain. This gain is factory-set to 20 but can be changed. To select a custom gain setting, set the jumper on J5 to the leftmost position and install a resistor in location R16. The value of this resistor is calculated by the formula **R = Gain x 10K Ohms**. The factory-installed value is 200K Ohms, for a gain of 20. R16 is located just to the right of the A/D chip U1, in the approximate center of the board.

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3.3 J4: Unipolar/Bipolar A/D Mode

Unipolar mode: Both jumpers in upper position (over top and middle pins)
Bipolar mode: Both jumpers in lower position (over middle and bottom pins)

These jumpers are mounted vertically (i.e. parallel to the potentiometers next to them).

The default setting is Bipolar mode.

3.4 J5: A/D Gain

Gain	Position	Notes
User	1 (Left)	Factory-set to 20; can be changed (see section 3.2)
10	2	
5	3	
2	4	
1	5	
0.5	6 (Right)	Default setting

3.5 J6: Single-Ended / Differential A/D Mode

Single-ended mode: Both jumpers in upper position (over top and middle pins)
Differential mode: Both jumpers in lower position (over middle and bottom pins)

In Single-ended mode, Diamond-MM has 16 input channels numbered 0 - 15.
In Differential mode, Diamond-MM has 8 input channels numbered 0 - 7.

The default setting is Single-ended mode.

3.6 J7: Output Reference Voltage

+5.000V: Jumper in left position
-5.000V: Jumper in right position

The default setting is +5.000V.

3.7 J8: D/A Reference Voltage

Internal (-5.000V): Jumper in lower position (over middle and bottom pins)
External: Jumper in upper position (over top and middle pins)

These jumpers are mounted vertically (parallel to IC U6 next to them). The default is Internal. The right jumper is for channel 0, and the left jumper is for channel 1.

For external references, D/A channel 0 takes its full-scale reference from pin 26 on the I/O connector, and D/A channel 1 takes its full-scale reference from pin 28.

3.8 J9: Counter/Timer Input Clock Frequency

10MHz: Jumper in left position
1MHz: Jumper in right position

The default is 1MHz. The selected frequency feeds the inputs of 82C54 counters 1 and 2.

3.9 J10: DMA Level

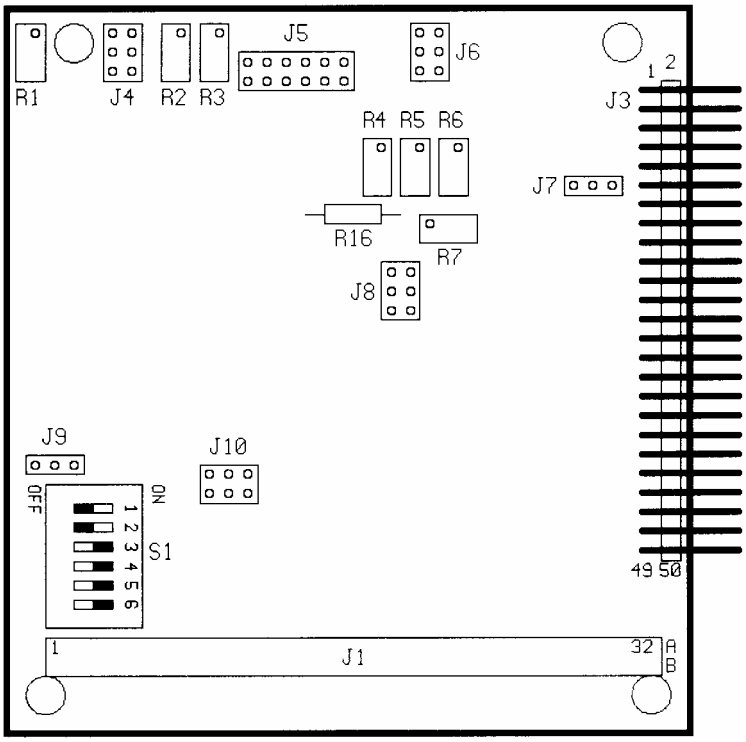
Level 1: Both jumpers in left position
Level 3: Both jumpers in right position

These jumpers are horizontal with respect to the board (parallel to the PC/104 connector). The default setting is Level 3.

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4. DIAMOND-MM BOARD DRAWING

DIAMOND-MM CONFIGURATION DIAGRAM



TOP OF BOARD
FRONT VIEW

J1: PC BUS CONNECTION
J3: I/O HEADER (2X25 PINS)
J4: UNIPOLAR / BIPOLAR SELECT
J5: A/D GAIN SELECT
J6: SINGLE-ENDED / DIFFERENTIAL SELECT
J7: VREFOUT SELECT
J8: D/A REFERENCE SELECT
J9: OSCILLATOR FREQUENCY SELECT
J10: DMA LEVEL SELECT

S1: BASE ADDRESS SELECT
R16: USER GAIN SETTING RESISTOR
R1-R7: CALIBRATION RESISTORS

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5. I/O MAP

Diamond-MM occupies 16 bytes in I/O space. These registers are described in detail in the next chapter.

Base +	Write Function	Read Function
0	Start A/D conversion	A/D LSB + channel tag
1	Not used	A/D MSB
2	A/D channel register	A/D channel register
3	Digital output port	Digital input port
4	D/A 0 LSB	Not used
5	D/A 0 MSB + update	Not used
6	D/A 1 LSB	Not used
7	D/A 1 MSB + update	Not used
8	Clear interrupt flip flop	Status register
9	Control register	Control register readback
10	Counter/timer enable/select	Not used
11	Not used	Special readback register
12	Counter/timer 0 data register	Counter/timer 0 data register
13	Counter/timer 1 data register	Counter/timer 1 data register
14	Counter/timer 2 data register	Counter/timer 2 data register
15	Counter/timer control register	Counter/timer control register

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6. REGISTER DEFINITIONS

Base + 0 Read A/D LSB + Channel Tag

Bit No.	7	6	5	4	3	2	1	0
Name	AD3	AD2	AD1	AD0	CH3	CH2	CH1	CH0

Definitions:

AD3 - 0 A/D data bits 3 - 0; AD0 is the LSB; A/D data is an unsigned 12-bit value.

CH3 - 0 A/D channel data, 0 - 15 (0 - 7 in differential mode)

Base + 0 Write Start A/D Conversion

Writing to Base + 0 starts an A/D conversion. The value written does not matter.

Base + 1 Read A/D MSB

Bit No.	7	6	5	4	3	2	1	0
Name	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

Definitions:

AD11 - 4 A/D data bits 11 - 4; AD11 is the MSB; A/D data is an unsigned 12-bit value.

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Base + 2 Read/Write A/D Channel Register

Bit No.	7	6	5	4	3	2	1	0
Name	HIGH3	HIGH2	HIGH1	HIGH0	LOW3	LOW2	LOW1	LOW0

Definitions:

HIGH3 - 0 High channel of channel scan range; ranges from 0 to 15 in single-ended mode, 0 - 7 in differential mode.

LOW3 - 0 Low channel of channel scan range; ranges from 0 to 15 in single-ended mode, 0 - 7 in differential mode.

Note: the high channel does not need to be higher than the low channel; for example, LOW = 8 and HIGH = 2 are valid settings.

Base + 3 Read Digital Input Port

Bit No.	7	6	5	4	3	2	1	0
Name	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

These pins correspond directly to the correspondingly-named pins on I/O connector J3.

Base + 3 Write Digital Output Port

Bit No.	7	6	5	4	3	2	1	0
Name	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

These pins correspond directly to the correspondingly-named pins on I/O connector J3.

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Base + 4 **Write** **DAC 0 LSB**

Bit No.	7	6	5	4	3	2	1	0
Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

Definitions:

DA7 - 0 D/A data bits 7 - 0 for output channel 0; DA0 is the LSB; D/A data is an unsigned 12-bit value.

Base + 5 **Write** **DAC 0 MSB**

Bit No.	7	6	5	4	3	2	1	0
Name	X	X	X	X	DA11	DA10	DA9	DA8

X Don't Care; these bits are ignored

DA11 - 8 D/A bits 11 - 8 for output channel 0; DA11 is the MSB; D/A data is an unsigned 12-bit value.

Base + 6 **Write** **DAC 1 LSB**

Bit No.	7	6	5	4	3	2	1	0
Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

Definitions:

DA7 - 0 D/A data bits 7 - 0 for output channel 1; DA0 is the LSB; D/A data is an unsigned 12-bit value.

Base + 7 **Write** **DAC 1 MSB**

Bit No.	7	6	5	4	3	2	1	0
Name	X	X	X	X	DA11	DA10	DA9	DA8

X Don't Care; these bits are ignored

DA11 - 8 D/A bits 11 - 8 for output channel 1; DA11 is the MSB; D/A data is an unsigned 12-bit value.

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Base + 8 Write Clear Interrupt Flip Flop

Writing to this register clears the on-board interrupt flip flop. The value written does not matter.

The interrupt flip flop is set whenever an interrupt is generated on Diamond-MM (i.e. during A/D conversions), and it must be cleared by software before another interrupt can be generated. Diamond-MM's software driver includes an interrupt handler that performs this task automatically.

Base + 8 Read Status Register

Bit No.	7	6	5	4	3	2	1	0
Name	STS	U/B	S/D	INT	ADCH3	ADCH2	ADCH1	ADCH0

STS A/D chip status:
- 1 A/D conversion in progress
- 0 A/D idle

U/B Unipolar / Bipolar A/D input mode setting:
- 1 unipolar: A/D can measure only positive input voltages.
- 0 bipolar (default): A/D can measure both negative and positive input voltages.

S/D Single-ended / Differential A/D input mode setting:
- 1 Single-ended (default)
- 0 Differential

INT Interrupt request status:
- 1 Interrupt is pending; A/D has generated a new value
- 0 No interrupt is pending

Note: A/D conversions continue to occur on schedule regardless of whether this bit is cleared. If a new conversion occurs before this bit is cleared, an overrun condition will occur, and the unread A/D value will be lost. There is no way to tell if an overrun condition has occurred. Therefore the programmer must ensure that the interrupt rate is not faster than the capability of the system and program to respond.

ADCH3 - 0 Current A/D channel; this is the channel currently selected on board and is the channel that will be used for the next A/D conversion (unless a new value is written to the channel register).

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Base + 9 Read/Write Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	INTE	INT2	INT1	INT0	X	DMAEN	TRIGE	INTTRIG

INTE — Interrupt enable:
- 1 Enable interrupts
- 0 Disable interrupts

INT2 - 0 — Interrupt level select: 011 = level 3, 100 = level 4, etc. INT2 is the MSB. Only levels 2 - 7 are valid; levels 0 and 1 are not connected on the board.

X — Don't Care; the value of this bit is ignored.

DMAEN — DMA enable (DMA operation is explained later in this manual):
- 1 Enable DMA operation
- 0 Disable DMA operation

TRIGE — Enable hardware A/D trigger:
- 1 Enable hardware trigger (source is selected with INTTRIG bit)
- 0 Disable hardware trigger

INTTRIG — A/D trigger select:
- 1 Internal trigger: **Rising** edges on the output of counter/timer 2 (82C54) generate A/D conversions
- 0 External trigger: **Falling** edges on DI0 / Trigger, pin 48 on I/O connector J3, generate A/D conversions.

Base + 10 Write Counter/Timer Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	C2	C1	C0

C2 — External gate enable:
- 1 IN0- (pin 29 on the I/O header) acts as a gate for A/D sample control when external A/D clock is enabled (INTTRIG = 0 above). When IN0- is high, falling edges on DI0 (pin 48 on the I/O header) will initiate A/D conversions. When IN0- is low, the DI0 signal is inhibited. IN0- is connected to a 10KΩ pull-up resistor.
- 0 IN0- does not act as a gate for external A/D clocking.

C1 — Counter 0 input source:
- 1 Input to Counter 0 is a 100kHz on-board reference frequency derived from the 10MHz oscillator. IN0- (pin 29 on the I/O header) gates this signal. When it is high (default), the 100kHz signal runs. When it is low, the 100kHz signal is stopped.
- 0 Input to Counter 0 is an inverted polarity copy of IN0-. IN0- is connected to a 10KΩ pull-up resistor.

C0 — Counters 1 and 2 gate control:
- 1 Counters 1 and 2 are gated by DI0 (pin 48 on the I/O header). When DI0 is low PRIOR TO THE START OF DMA CONVERSIONS, A/D conversions will not occur until it is brought high. DI0 is connected to a 10KΩ pull-up resistor.
- 0 Counters 1 and 2 run freely with no gating.

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Base + 11 Read Special Readback Register

Bit No.	7	6	5	4	3	2	1	0
Name	X	X	X	WAIT	C2	EQUAL	C1	C0

WAIT 10 microsecond timer. This bit goes high for 10 microseconds whenever register 2 (channel register) is written to. It serves as an indicator that the analog input circuit is settling on the new input channel signal. When WAIT goes low, the board is ready to start the next A/D conversion.

After writing to the channel register, the user program should monitor this bit until it is low before starting an A/D conversion.

This bit is only valid for boards with Actel chip revision V6H or above. See the label on the chip for the revision number.

EQUAL This bit indicates that the current A/D channel is equal to the high channel stored in register 2. Upon the next A/D conversion, the A/D channel will be reset to the low channel stored in register 2.

C2 - C0 Readback of the bits C2 - C0 in Register 10 described above.

Base + 12 ~ Base + 15 Read/Write 82C54 Counter/Timer Registers

These registers map directly to the 82C54. The definitions of these registers can be found in the 82C54 datasheet appended to the back of this manual.

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7. ANALOG INPUT RANGES AND RESOLUTION

7.1 Resolution

Diamond-MM uses a 12-bit A/D converter. This means that the analog input voltage can be measured to the precision of a 12-bit binary number. The maximum value of a 12-bit binary number is 2^{12} - 1, or 4095, so the full range of numerical values that you can get from a Diamond-MM analog input channel is 0 - 4095.

The smallest change in input voltage that can be detected is $1/(2^{12})$, or 1/4096, of the full-scale input range. This smallest change results in an increase or decrease of 1 in the A/D code, and so this change is referred to as 1 LSB, or 1 least significant bit.

7.2 Unipolar and Bipolar Inputs

Diamond-MM can measure both unipolar (positive only) and bipolar (positive and negative) analog voltages, depending on the configuration jumpers (see Chapter 4, J4 setting). The full-scale voltage for Diamond-MM is 0-10V in unipolar configuration and ±5V in bipolar configuration. In front of the A/D converter is a user-configured gain circuit that can multiply or divide the input voltage before reaching the A/D converter (see Chapter 4, J5 setting). This gain circuit has the effect of scaling the input voltage range to match the A/D converter for better resolution. In general you should select the highest gain you can that will allow the A/D converter to read the full range of voltages over which your input signals will vary. However, if you pick too high a gain, then the A/D converter will clip at either the high end or low end, and you will not be able to read the full range of voltages on your input signals.

7.3 Single Ended and Differential Inputs

Diamond-MM can handle both single-ended and differential inputs. A single-ended input is a single-wire input that is referenced to analog ground on the board. This means that the input voltage will be measured with respect to the board's analog ground. A differential input is a two-wire input, and the board will measure the difference between the voltages of the two inputs. Polarity is important for a differential input. Diamond-MM will subtract the voltage on the low (-) input from the voltage of the high (+) input. Differential inputs are frequently used when the grounds of the input device and the measurement device (Diamond-MM) are at different voltages, or when a low-level signal is being measured that has its own ground wire.

7.4 Input Ranges and Resolution

Mode (J4)	Gain (J5)	Full-Scale Input Range	Resolution (1 LSB)
Unipolar	0.5	N/A	N/A
Unipolar	1	0 - 10V	2.44mV
Unipolar	2	0 - 5V	1.22mV
Unipolar	5	0 - 2.5V	0.61mV
Unipolar	10	0 - 1V	0.244mV
Unipolar	Custom	0 - R/10K V*	R/10K / 4096 V
Bipolar	0.5	±10V	4.88mV
Bipolar	1	±5V	2.44mV
Bipolar	2	±2.5V	1.22mV
Bipolar	5	±1V	0.488mV
Bipolar	10	±0.5V	0.244mV
Bipolar	Custom	±R/10K V*	R/10K / 2048 V

* Custom range is set with a resistor in R16 position. See Chapter 3, Custom A/D Gain. The maximum input voltage range is ±10V.

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8. ANALOG INPUT RANGE SETTINGS

The table below lists the jumper settings required to configure all the possible analog input ranges on Diamond-MM. J4 and J5 are used to for the configuration. J4 is located at the top left corner of the board, and J5 is located at the top middle of the board. The factory configuration for Diamond-MM is ±5V.

Full-Scale Input Range	Mode	J4 Setting[1]	Gain	J5 Setting[2]
0 - 10V	Unipolar	Top	1	5
0 - 5V	Unipolar	Top	2	4
0 - 2V	Unipolar	Top	5	3
0 - 1V	Unipolar	Top	10	2
0 - Custom	Unipolar	Top	R/10KΩ[3]	1
±10V	Bipolar	Bottom	0.5	6
±5V (Factory setting)	Bipolar	Bottom	1	5
±2.5V	Bipolar	Bottom	2	4
±1V	Bipolar	Bottom	5	3
±0.5V	Bipolar	Bottom	10	2
±Custom	Bipolar	Bottom	R/10KΩ[3]	1

Notes:

1. "Top" means the two jumpers are mounted vertically (side by side) across the middle and top pins. "Bottom" means the two jumpers are mounted vertically across the middle and bottom pins.
2. Position 1 is the leftmost position; position 6 is the rightmost position.
3. Custom range is set with a resistor in R16 position. The gain is determined by the formula Gain = R/10KΩ, and the full-scale input range (V_{FS}) is determined by the formula V_{FS} = 5V / Gain. See Chapter 3, Custom A/D Gain. The gain is independent of the unipolar/bipolar configuration.

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9. PERFORMING AN A/D CONVERSION

This chapter describes the steps involved in performing an A/D conversion on a selected input channel using direct programming (not with the driver software).

There are five steps involved in performing an A/D conversion:

1. **Select the input channel**
2. **Perform an A/D conversion on the current channel**
3. **Wait for the conversion to finish**
4. **Read the data**
5. **Convert the numerical data to a meaningful value**

9.1 Select the input channel

To select the input channel to read, write a low-channel/high-channel pair to the channel register at base + 2. (See Chapter 7). The low 4 bits select the low channel, and the high 4 bits select the high channel. When you write any value to this register, the current A/D channel is set to the low channel. About 10 microseconds is required as a settling time for the analog front end circuitry after you select the channel. You can implement this as a short software loop.

⇒ **Note:** When you perform an A/D conversion, the current channel is automatically incremented to the next channel in the selected range. Therefore, to perform A/D conversions on a group of consecutively-numbered channels, you do not need to write the input channel prior to each conversion. For example, to read from channels 0 - 2, write Hex 20 to base + 2. The first conversion is on channel 0, the second will be on channel 1, and the third will be on channel 2. Then the channel counter wraps around to the beginning again, so the fourth conversion will be on channel 0 again and so on.

9.2 Perform an A/D conversion on the current channel

After writing to the channel register and waiting for the analog circuitry to settle, you can perform an A/D conversion on the selected channel. To do this, simply write to base + 0 to start the conversion. The value does not matter and is ignored.

9.3 Wait for the conversion to finish

The A/D converter takes up to 10 microseconds to complete a conversion. Most processors and software can operate fast enough so that if you try to read the A/D converter immediately after writing to base + 0, you will beat the A/D converter and get invalid data. Therefore the A/D converter provides a status signal to indicate whether it is busy or idle. This bit can be read back as bit 7 in the status register at base + 8. When the A/D converter is busy (performing an A/D conversion), this bit is 1, and when the A/D converter is idle (conversion is done and data is available), this bit is 0. Here is a pseudocode explanation:

```
Status = read(base+8) AND 128 ;or Status = read(base+8) AND 80 Hex
If Status = 0 then conversion is complete, else A/D converter is busy
```

Keep repeating this procedure until Status = 0.

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9.4 Read the data

Once the conversion is complete, you can read the data back from the A/D converter. The data is 12 bits wide and is read back in two 8-bit bytes. Refer to the register definitions on p. 8 for the format of the A/D data. The following pseudocode illustrates how to construct the 12-bit A/D value from these two bytes:

```
LSB = read(base) / 16   ;shift right 4 bits & delete channel no.
MSB = read(base+1) * 16 ;shift left 4 bits into proper position
Data = MSB + LSB        ;combine the 2 bytes into a 12-bit value
```

The final data ranges from 0 to 4095 (0 to 2^{12} - 1).

9.5 Convert the numerical data to a meaningful value

Once you have the A/D value, you need to convert it to a meaningful value. The first step is to convert it back to the actual measured voltage. Afterwards you may need to convert the voltage to some other engineering units (for example, the voltage may come from a temperature sensor, and then you would need to convert the voltage to the corresponding temperature according to the temperature sensor's characteristics). Since there are a large number of possible input devices, this secondary step is not included here.

To convert the A/D value to the corresponding input voltage, use the following formulas:

Conversion Formula for Unipolar Input Ranges:

Input voltage = (A/D value / 4096) * Full-scale input range

Example: Input range is 0-5V and A/D value is 1776:
Input voltage = 1776 / 4096 * 5V = 2.168V

Here is an illustration of the relationship between A/D code and input voltage for a unipolar input range (V_{FS} = Full scale input voltage):

A/D Code	Input voltage
0	0V
1	1 LSB (V_{FS} / 4096)
2048	V_{FS} / 2
2049	V_{FS} / 2 + 1 LSB
4095	V_{FS} - 1 LSB (e.g. 4.9988V for 0-5V range)

Conversion Formula for Bipolar Input Ranges:

Input voltage = (A/D value/2048) * Full-scale input range
- Full-scale input range

Example: Input range is ±5V and A/D value is 1776:
Input voltage = 1776 / 2048 * 5V - 5V = -0.664V

Here is an illustration of the relationship between A/D code and input voltage for a bipolar input range (V_{FS} = Full scale input voltage):

A/D Code	Input voltage
0	$-V_{FS}$
1	$-V_{FS}$ + 1 LSB
2047	-1 LSB
2048	0V
2049	+1 LSB
4095	V_{FS} - 1 LSB (e.g. 4.9976V for ±5V range)

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10. ANALOG OUTPUT RANGES AND RESOLUTION

10.1 Description

Diamond-MM uses a two-channel 12-bit D/A converter (DAC) to provide two analog outputs. A 12-bit DAC can generate output voltages with the precision of a 12-bit binary number. The maximum value of a 12-bit binary number is 2^{12} - 1, or 4095, so the full range of numerical values that you can write to the analog outputs on Diamond-MM is 0 - 4095.

These outputs operate in unipolar mode only; all output voltages greater than or equal to 0V. The outputs are preset for 0-5V, but the range can be adjusted to any value between 0V and 10V on the board. In addition an external voltage can be applied to either of the two reference inputs to provide custom ranges for each channel.

⇒ **Note:** In this manual, the terms analog output, D/A, and DAC are all used interchangeably to mean the same thing.

10.2 Resolution

The *resolution* is the smallest possible change in output voltage. For a 12-bit DAC the resolution is $1/(2^{12})$, or 1/4096, of the full-scale output range. This smallest change results from an increase or decrease of 1 in the D/A code, and so this change is referred to as 1 LSB, or 1 least significant bit. The value of this LSB is calculated as follows:

1 LSB = Full-scale output voltage / 4096

Example: Full-scale output voltage = 5V
1 LSB = 5V / 4096 = 1.22mV

10.3 Full-Scale Voltage Selection

Header J8, located in the center of the board, is used to select the full-scale voltage, or reference voltage, for each analog output. The right column of 3 pins controls the reference source for output channel 0, and the left column of 3 pins controls the reference source for output channel 1. If a jumper is inserted over the middle and bottom pins, the reference for the corresponding channel is the on-board analog output reference. If the jumper is inserted over the middle and top pins, the reference for the corresponding channel comes from the I/O header. Pin 26 is the reference input for channel 0, and pin 28 is the reference input for channel 1. Note that each channel can have its own reference source. For example, channel 0 could use the on-board reference while channel 1 uses an external reference, or both channels could use a different external reference.

Potentiometer R4 is used to control the on-board analog output reference voltage. It is preset to -5V. However, you can adjust this potentiometer to change the full-scale output range of both D/A channels without using an external reference input. The on-board reference voltage may be adjusted to any voltage between 0V and -10V. To make the adjustment, first move the jumper in J7 (above the D/A converter IC and near the I/O header) so that it is over the middle and right pins. Then connect a voltmeter to pin 18 on the I/O header. Now adjust R4 to get the voltage you want.

⇒ **Note:** The analog output reference voltage must be a *negative* voltage. This is because the D/A converters invert the reference voltage as part of their operation.

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11. GENERATING AN ANALOG OUTPUT

This chapter describes the steps involved in generating an analog output (also called performing a D/A conversion) on a selected output channel using direct programming (not with the driver software).

There are two steps involved in performing a D/A conversion:

1. **Compute the D/A output value for the desired output voltage**
2. **Write the value to the selected output channel**

11.1 Compute the D/A code for the desired output voltage

Use the following formula to compute the D/A code required to generate the desired voltage:

Output value = Desired output voltage / Full-scale voltage * 4096

Example: Desired output voltage = 2.168V, full-scale voltage = 5V
Output code = 2.168 / 5 * 4096 = 1776

⇒ **Note:** The DAC cannot generate the actual full-scale reference voltage; to do so would require an output code of 4096, which is not possible with a 12-bit number. The maximum output value is 4095. Therefore the maximum possible output voltage is 1 LSB less than the full-scale reference voltage.

11.2 Write the value to the selected output channel

The two DACs are located at addresses base + 4 through base + 7 (see Chapter 6, I/O Map). Each DAC uses one pair of addresses. First write the LSB to the lower address, then write the MSB to the upper address. Writing the MSB causes the DAC to be updated, outputting the new voltage.

First use the following formulas to compute the LSB and MSB values:

LSB = D/A Code AND 255 ;keep only the low 8 bits

MSB = int(D/A code / 256) ;strip off low 8 bits, keep 4 high bits

Example: Output code = 1776
LSB = 1776 AND 255 = 240 (F0 Hex); MSB = int(1776 / 256) = int(6.9375) = 6
(In other words, 1776 = 6*240 + 240)

Note that the LSB does not actually need to be computed, since Diamond-MM uses an 8-bit databus and will ignore the high byte if a program attempts to write a 16-bit word to it.

Now write these values to the selected channel:

For Channel 0: Write 240 to base + 4, then write 6 to base + 5, updating Channel 0

For Channel 1: Write 240 to base + 6, then write 6 to base + 7, updating Channel 1

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12. DIGITAL I/O OPERATION

Diamond-MM contains an 8-bit digital output port and an 8-bit digital input port. Both ports are located at base + 3. To access the output lines, simply write an 8-bit value to base + 3. Similarly, to read the input lines, read from base + 3.

The output lines are located at pins 33 through 40 on the I/O header J3 (see Chapter 2, p. 4). They are CMOS TTL and can drive up to ±6mA max per line. They do not have a readback feature, so your program must keep track of the latest output value.

The inputs are located at pins 41 through 48 on the I/O header J3. They are also CMOS/TTL compatible. There is no latch signal provided. However, the values are latched when being read to prevent transitions during the CPU read operation.

Input line 2 doubles as the gate control for counter 0. When it is high, counter 0 can count, and when it is low, counter 0 holds its present value.

Input line 0 doubles as a programmable gate control for counters 1 and 2. These counters are combined together and used as the A/D pacer clock. Bit 0 of the counter/timer control register at base + 10 determines whether these counters run freely or whether Input line 0 is the gate (see Chapter 6, page 13). This line has a 10KΩ pull-up resistor.

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13. CALIBRATION PROCEDURE

All boards are calibrated at the factory prior to shipment. Drift specifications of Diamond-MM are low enough so that recalibration is usually not required except in high-precision applications or applications where temperatures vary widely. In these situations calibration should be performed approximately on a yearly basis.

To calibrate the board, you will need a voltmeter with a precision of at least 4 1/2 digits and a precision voltage source. In place of the voltage source you can use the analog outputs on Diamond-MM after they have been calibrated.

13.1 A/D Bipolar Range and Full-Scale

Both jumpers on J4 are down; jumper on J5 is in position 5 (gain setting = 1)

a. Connect an analog input channel to ground (0.000V) and adjust **R2** so that the A/D reads 0.

b. Connect an analog input channel to +4.9963V and adjust **R3** so that the A/D toggles between 4094 and 4095.

13.2 A/D Unipolar Range

Both jumpers on J4 are up; jumper on J5 is in position 5 (gain setting = 1)

Connect an analog input channel to +1.22mV and adjust **R1** so that the A/D toggles between 0 and 1.

13.3 +5V Reference

Jumper on J7 in left position

Adjust **R5** so that pin 18 on the I/O connector reads +5.000V.

13.4 D/A Full-Scale Reference

Jumper on J7 in right position

Adjust **R4** so that pin 18 on the I/O connector reads -5.000V.

13.5 D/A Full-Scale Voltages

Jumpers on J8 in lower position

Channel 0: Write 4095 to DAC 0 (Base + 4 and Base + 5) and adjust **R7** so that pin 20 on the I/O connector measures +4.9988V.

Channel 1: Write 4095 to DAC 1 (Base + 6 and Base + 7) and adjust **R6** so that pin 22 on the I/O connector measures +4.9988V.

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14. SPECIFICATIONS

Analog Inputs

No. of inputs	8 differential or 16 single-ended (user selectable)
A/D resolution	12 bits (1/4096 of full scale)
Input ranges	Bipolar: ±10V, ±5V, ±2.5V, ±1V, ±0.5V, Custom Unipolar: 0-10V, 0-5V, 0-2.5V, 0-1V, Custom
Input bias current	50nA max
Maximum input voltage	±10V for linear operation
Overvoltage protection	±35V on any analog input without damage
Nonlinearity	±1LSB, no missing codes
Conversion rate	100,000 samples per second max (with DMA operation)
Conversion trigger	software trigger, internal pacer clock, or external TTL signal

Analog Outputs

No. of outputs	2
D/A resolution	12 bits (1/4096 of full scale)
Output ranges	Unipolar: 0-5V, adjustable, or external reference input
Output current	±8mA max per channel
Settling time	4 S max to ±1/2 LSB
Relative accuracy	±1 LSB
Nonlinearity	±1 LSB, monotonic

Digital I/O

No. of inputs	8, HCT/TTL compatible
Input voltage	Logic 0: 0.0V min, 0.8V max; Logic 1: 2.0V min, 5.0V max
Input current	±1µA max
No. of outputs	8, HCT/TTL compatible
Output voltage	Logic 0: 0.0V min, 0.33V max; Logic 1: 3.8V min, 5.0V max
Output current	±4mA max per line

Counter/Timers

A/D Pacer clock	32-bit down counter (2 82C54 counters cascaded)
Clock source	10MHz on-board clock source or external signal
General purpose	16-bit down counter (1 82C54 counter)
Interrupt/DMA trigger	End of A/D conversion

General

Power supply	+5VDC ±10%
Current consumption	165mA typical
±15V output current	±10mA max with DACs unloaded; **not short-circuit protected**
+5V output current	Depends on PC/104 power supply; **not short-circuit protected**
Operating temperature	Model DMM: 0 to 70°C; Model DMM-XT: -40 to +85°C
Operating humidity	5% to 95% noncondensing
PC/104 bus	8 bits

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HARRIS SEMICONDUCTOR

82C54

March 1997

CMOS Programmable Interval Timer

Features

- 8MHz to 12MHz Clock Input Frequency
- Compatible with NMOS 8254
  - Enhanced Version of NMOS 8253
- Three Independent 16-Bit Counters
- Six Programmable Counter Modes
- Status Read Back Command
- Binary or BCD Counting
- Fully TTL Compatible
- Single 5V Power Supply
- Low Power
  - ICCSB 10μA
  - ICCOP . . . . . .10mA at 8MHz
- Operating Temperature Ranges
  - C82C54 . . . . . .0^oC to $+70^oC$
  - I82C54 . . . . . .-40^oC to $+85^oC$
  - M82C54 . . . . . .-55^oC to $+125^oC$

Description

The Harris 82C54 is a high performance CMOS Programmable Interval Timer manufactured using an advanced 2 micron CMOS process.

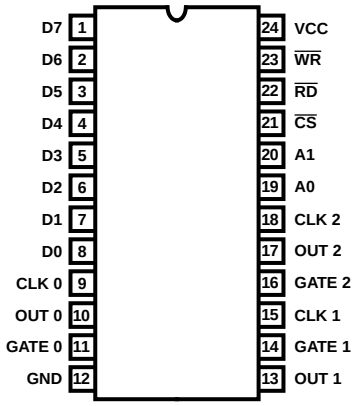
The 82C54 has three independently programmable and functional 16-bit counters, each capable of handling clock input frequencies of up to 8MHz (82C54) or 10MHz (82C54-10) or 12MHz (82C54-12).

The high speed and industry standard configuration of the 82C54 make it compatible with the Harris 80C86, 80C88, and 80C286 CMOS microprocessors along with many other industry standard processors. Six programmable timer modes allow the 82C54 to be used as an event counter, elapsed time indicator, programmable one-shot, and many other applications. Static CMOS circuit design insures low power operation.

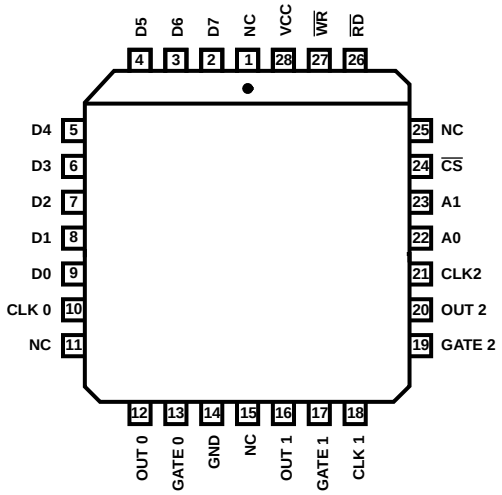
The Harris advanced CMOS process results in a significant reduction in power with performance equal to or greater than existing equivalent products.

Pinouts

82C54 (PDIP, CERDIP, SOIC)
TOP VIEW



82C54 (PLCC/CLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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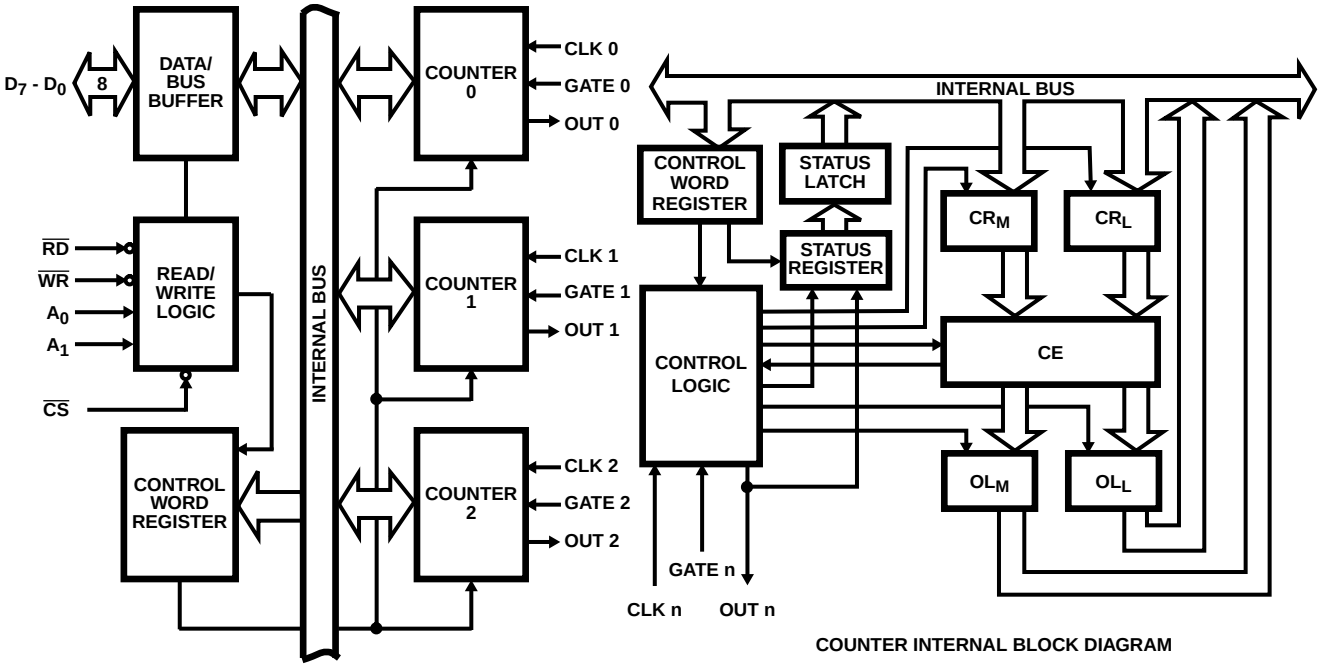
File Number **2970.1**

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Ordering Information

PART NUMBERS			TEMPERATURE RANGE	PACKAGE	PKG. NO.
8MHz	10MHz	12MHz			
CP82C54	CP82C54-10	CP82C54-12	0^oC to $+70^oC$	24 Lead PDIP	E24.6
IP82C54	IP82C54-10	IP82C54-12	-40^oC to $+85^oC$	24 Lead PDIP	E24.6
CS82C54	CS82C54-10	CS82C54-12	0^oC to $+70^oC$	28 Lead PLCC	N28.45
IS82C54	IS82C54-10	IS82C54-12	-40^oC to $+85^oC$	28 Lead PLCC	N28.45
CD82C54	CD82C54-10	CD82C54-12	0^oC to $+70^oC$	24 Lead CERDIP	F24.6
ID82C54	ID82C54-10	ID82C54-12	-40^oC to $+85^oC$	24 Lead CERDIP	F24.6
MD82C54/B	MD82C54-10/B	MD82C54-12/B	-55^oC to $+125^oC$	24 Lead CERDIP	F24.6
MR82C54/B	MR82C54-10/B	MR82C54-12/B	-55^oC to $+125^oC$	28 Lead CLCC	J28.A
SMD # 8406501JA	-	8406502JA	-55^oC to $+125^oC$	24 Lead CERDIP	F24.6
SMD# 84065013A	-	84065023A	-55^oC to $+125^oC$	28 Lead CLCC	J28.A
CM82C54	CM82C54-10	CM82C54-12	0^oC to $+70^oC$	24 Lead SOIC	M24.3

Functional Diagram



COUNTER INTERNAL BLOCK DIAGRAM

Pin Description

SYMBOL	DIP PIN NUMBER	TYPE	DEFINITION
D7 - D0	1 - 8	I/O	DATA: Bi-directional three-state data bus lines, connected to system data bus.
CLK 0	9	I	CLOCK 0: Clock input of Counter 0.
OUT 0	10	O	OUT 0: Output of Counter 0.
GATE 0	11	I	GATE 0: Gate input of Counter 0.
GND	12		GROUND: Power supply connection.
OUT 1	13	O	OUT 1: Output of Counter 1.
GATE 1	14	I	GATE 1: Gate input of Counter 1.
CLK 1	15	I	CLOCK 1: Clock input of Counter 1.
GATE 2	16	I	GATE 2: Gate input of Counter 2.
OUT 2	17	O	OUT 2: Output of Counter 2.

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Pin Description (Continued)

SYMBOL	DIP PIN NUMBER	TYPE	DEFINITION
CLK 2	18	I	CLOCK 2: Clock input of Counter 2.
A0, A1	19 - 20	I	ADDRESS: Select inputs for one of the three counters or Control Word Register for read/write operations. Normally connected to the system address bus.
$\overline{CS}$	21	I	CHIP SELECT: A low on this input enables the 82C54 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
$\overline{RD}$	22	I	READ: This input is low during CPU read operations.
$\overline{WR}$	23	I	WRITE: This input is low during CPU write operations.
V_{CC}	24		V_{CC}: The +5V power supply pin. A 0.1µF capacitor between pins VCC and GND is recommended for decoupling.

A1	A0	SELECTS
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

Functional Description

General

The 82C54 is a programmable interval timer/counter designed for use with microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 82C54 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 82C54 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 82C54 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other computer/timer functions common to microcomputers which can be implemented with the 82C54 are:

- Real time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Data Bus Buffer

This three-state, bi-directional, 8-bit buffer is used to interface the 82C54 to the system bus (see Figure 1).

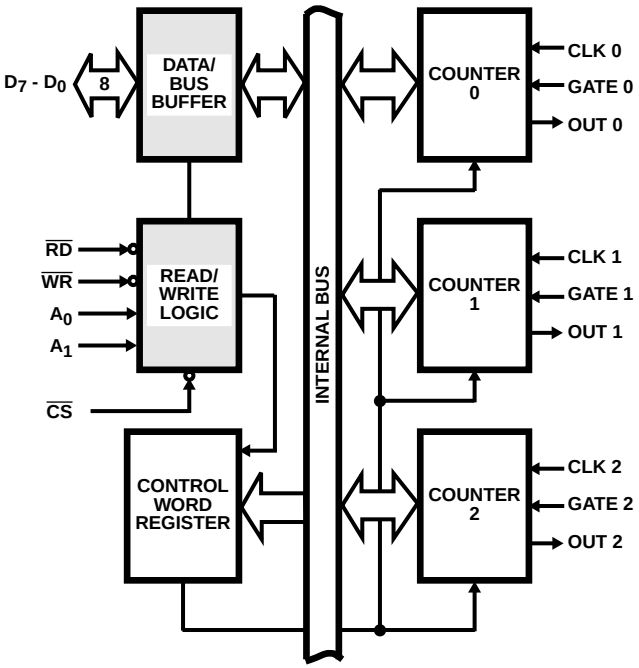


FIGURE 1. DATA BUS BUFFER AND READ/WRITE LOGIC FUNCTIONS

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 82C54. A1 and A0 select one of the three counters or the Control Word Register to be read from/written into. A “low” on the $\overline{RD}$ input tells the 82C54 that the CPU is reading one of the counters. A “low” on the $\overline{WR}$ input tells the 82C54 that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the 82C54 has been selected by holding $\overline{CS}$ low.

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Control Word Register

The Control Word Register (Figure 2) is selected by the Read/Write Logic when A1, A0 = 11. If the CPU then does a write operation to the 82C54, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the Counter operation.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

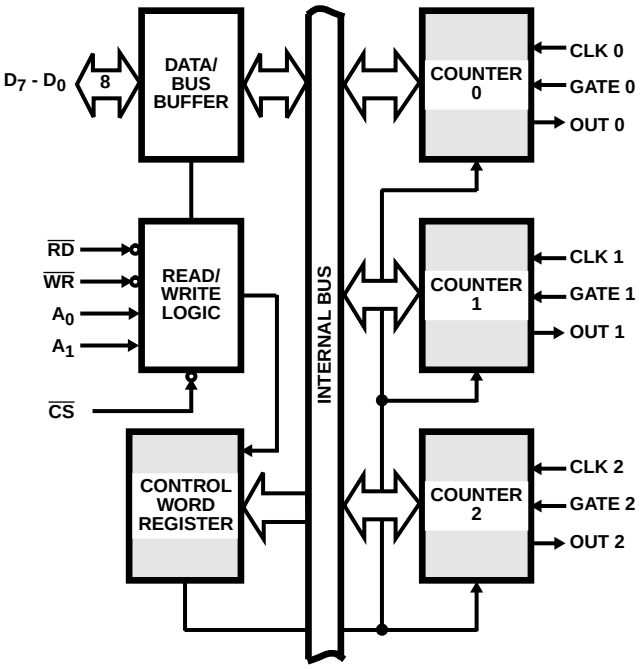


FIGURE 2. CONTROL WORD REGISTER AND COUNTER FUNCTIONS

Counter 0, Counter 1, Counter 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a signal counter is shown in Figure 3. The counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

The status register, shown in the figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labeled CE (for Counting Element). It is a 16-bit presettable synchronous down counter.

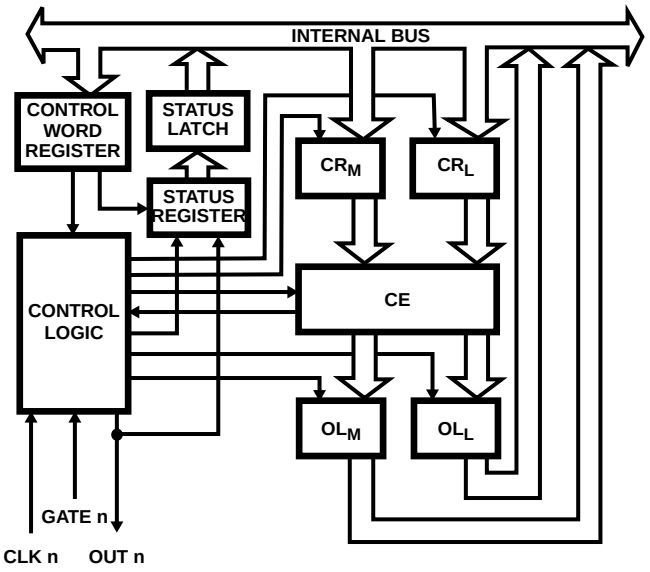


FIGURE 3. COUNTER INTERNAL BLOCK DIAGRAM

OLM and OLL are two 8-bit latches. OL stands for “Output Latch”; the subscripts M and L for “Most significant byte” and “Least significant byte”, respectively. Both are normally referred to as one unit and called just OL. These latches normally “follow” the CE, but if a suitable Counter Latch Command is sent to the 82C54, the latches “latch” the present count until read by the CPU and then return to “following” the CE. One latch at a time is enabled by the counter’s Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CRM and CRL (for “Count Register”). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CRM and CRL are cleared when the Counter is programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

82C54 System Interface

The 82C54 is treated by the system software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method or it can be connected to the output of a decoder.

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Operational Description

General

After power-up, the state of the 82C54 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the 82C54

Counters are programmed by writing a Control Word and then an initial count.

All Control Words are written into the Control Word Register, which is selected when A1, A0 = 11. The Control Word specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A1, A0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

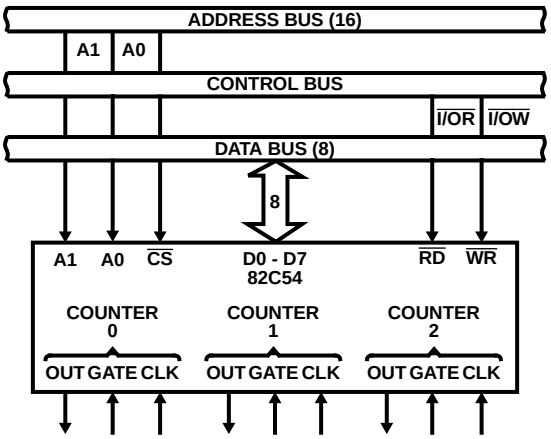


FIGURE 4. 82C54 SYSTEM INTERFACE

Write Operations

The programming procedure for the 82C54 is very flexible. Only two conventions need to be remembered:

1. For Each Counter, the Control Word must be written before the initial count is written.
2. The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A1, A0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

Control Word Format

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC - Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW - Read/Write

RW1	RW0	
0	0	Counter Latch Command (See Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M - Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD - Binary Coded Decimal

0	Binary Counter 16-bit
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

Possible Programming Sequence

	A1	A0
Control Word - Counter 0	1	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 0	0	0
Control Word - Counter 1	1	1
LSB of Count - Counter 1	0	1
MSB of Count - Counter 1	0	1
Control Word - Counter 2	1	1
LSB of Count - Counter 2	1	0
MSB of Count - Counter 2	1	0

Possible Programming Sequence

	A1	A0
Control Word - Counter 0	1	1
Control Word - Counter 1	1	1
Control Word - Counter 2	1	1
LSB of Count - Counter 2	1	0

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Possible Programming Sequence (Continued)

	A1	A0
LSB of Count - Counter 1	0	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 0	0	0
MSB of Count - Counter 1	0	1
MSB of Count - Counter 2	1	0

Possible Programming Sequence

	A1	A0
Control Word - Counter 2	1	1
Control Word - Counter 1	1	1
Control Word - Counter 0	1	1
LSB of Count - Counter 2	1	0
MSB of Count - Counter 2	1	0
LSB of Count - Counter 1	0	1
MSB of Count - Counter 1	0	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 0	0	0

Possible Programming Sequence

	A1	A0
Control Word - Counter 1	1	1
Control Word - Counter 0	1	1
LSB of Count - Counter 1	0	1
Control Word - Counter 2	1	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 1	0	1
LSB of Count - Counter 2	1	0
MSB of Count - Counter 0	0	0
MSB of Count - Counter 2	1	0

NOTE: In all four examples, all counters are programmed to Read/Write two-byte counts. These are only four of many programming sequences.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies. A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 82C54.

There are three possible methods for reading the Counters. The first is through the Read-Back command, which is explained later. The second is a simple read operation of the Counter, which is selected with the A1, A0 inputs. The only requirement is that the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in process of changing when it is read, giving an undefined result.

Counter Latch Command

The other method for reading the Counters involves a special software command called the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when A1, A0 = 11. Also, like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - specify counter to be latched

SC1	SC0	COUNTER
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5, D4 - 00 designates Counter Latch Command, X - Don't Care.
NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

The selected Counter's output latch (OL) latches the count when the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the 82C54 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

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1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a counter is programmed to read or write two-byte counts, the following precaution applies: A program MUST NOT transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

Read-Back Command

The read-back command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 5. The command applies to the counters selected by setting their corresponding bits D3, D2, D1 = 1.

A0, A1 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT 2	CNT 1	CNT 0	0

D5: 0 = Latch count of selected Counter (s)
D4: 0 = Latch status of selected Counter(s)
D3: 1 = Select Counter 2
D2: 1 = Select Counter 1
D1: 1 = Select Counter 0
D0: Reserved for future expansion; Must be 0

FIGURE 5. READ-BACK COMMAND FORMAT

The read-back command may be used to latch multiple counter output latches (OL) by setting the COUNT bit D5 = 0 and selecting the desired counter(s). This signal command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting STATUS bit D4 = 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in Figure 6. Bits D5 through D0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D7: 1 = Out pin is 1
0 = Out pin is 0
D6: 1 = Null count
0 = Count available for reading
D5 - D0 = Counter programmed mode (See Control Word Formats)

FIGURE 6. STATUS BYTE

NULL COUNT bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the counter is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown below.

THIS ACTION: CAUSES:

A. Write to the control word register:(1) . . . . . Null Count = 1
B. Write to the count register (CR):(2) . . . . . Null Count = 1
C. New count is loaded into CE (CR - CE) . . . . . Null Count = 0

(1) Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected.

(2) If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

COMMANDS								DESCRIPTION	RESULT
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	1	0	Read-Back Count and Status of Counter 0	Count and Status Latched for Counter 0
1	1	1	0	0	1	0	0	Read-Back Status of Counter 1	Status Latched for Counter 1
1	1	1	0	1	1	0	0	Read-Back Status of Counters 2, 1	Status Latched for Counter 2, But Not Counter 1
1	1	0	1	1	0	0	0	Read-Back Count of Counter 2	Count Latched for Counter 2
1	1	0	0	0	1	0	0	Read-Back Count and Status of Counter 1	Count Latched for Counter 1, But Not Status
1	1	1	0	0	0	1	0	Read-Back Status of Counter 1	Command Ignored, Status Already Latched for Counter 1

FIGURE 7. READ-BACK COMMAND EXAMPLE

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Both count and status of the selected counter(s) may be latched simultaneously by setting both COUNT and STATUS bits D5, D4 = 0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 7.

If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (Three-State)
1	X	X	X	X	No-Operation (Three-State)
0	1	1	X	X	No-Operation (Three-State)

FIGURE 8. READ/WRITE OPERATIONS SUMMARY

Mode Definitions

The following are defined for use in describing the operation of the 82C54.

CLK PULSE:

A rising edge, then a falling edge, in that order, of a Counter's CLK input.

TRIGGER:

A rising edge of a Counter's Gate input.

COUNTER LOADING:

The transfer of a count from the CR to the CE (See "Functional Description")

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written to the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

(1) Writing the first byte disables counting. Out is set low immediately (no clock pulse required).

(2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the counter as this has already been done.

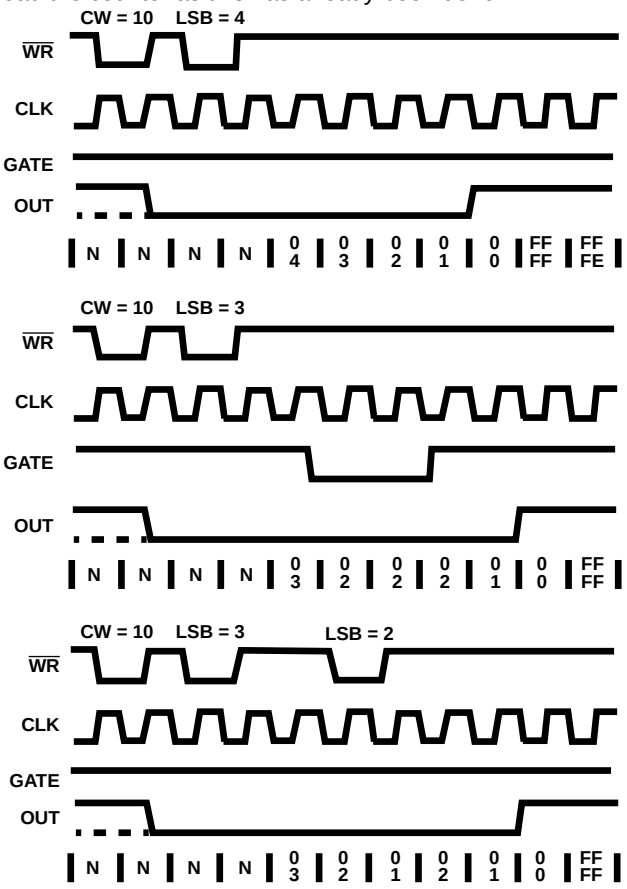


FIGURE 9. MODE 0

NOTES: The following conventions apply to all mode timing diagrams.

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a control word of 10, Hex is written to the counter.
4. LSB stands for Least significant "byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

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Mode 1: Hardware Retriggerable One-Shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggerable. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

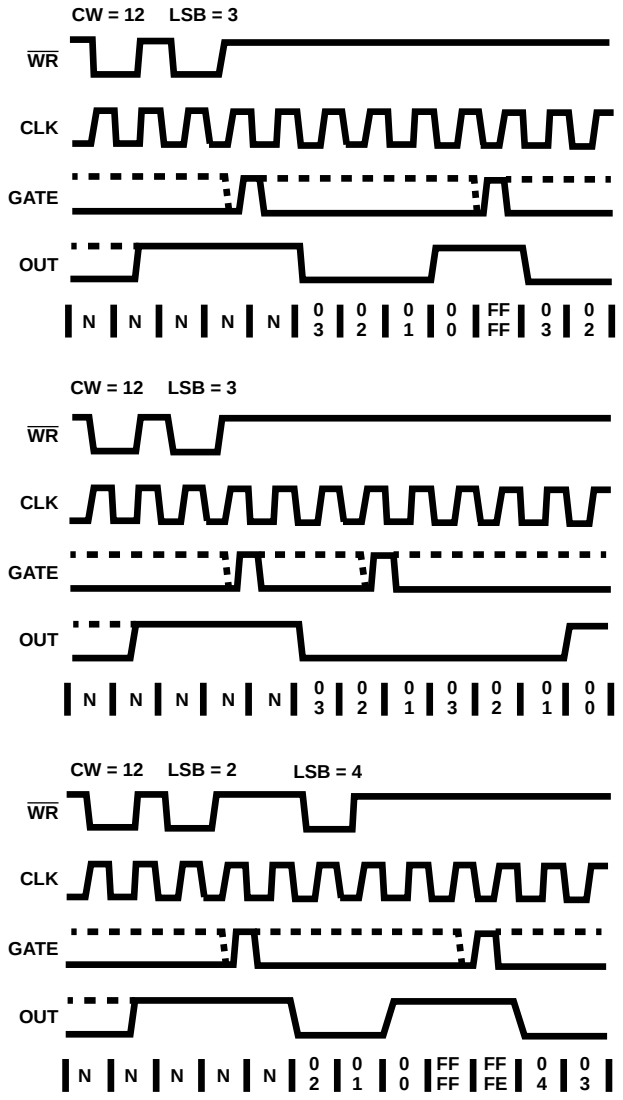


FIGURE 10. MODE 1

Mode 2: Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock Interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the end of the current counting cycle.

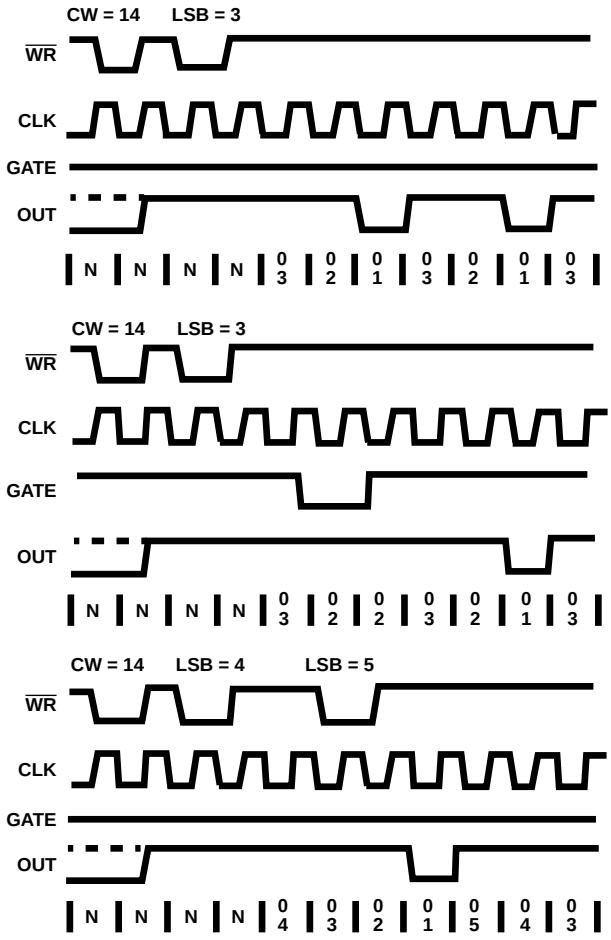


FIGURE 11. MODE 2

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Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

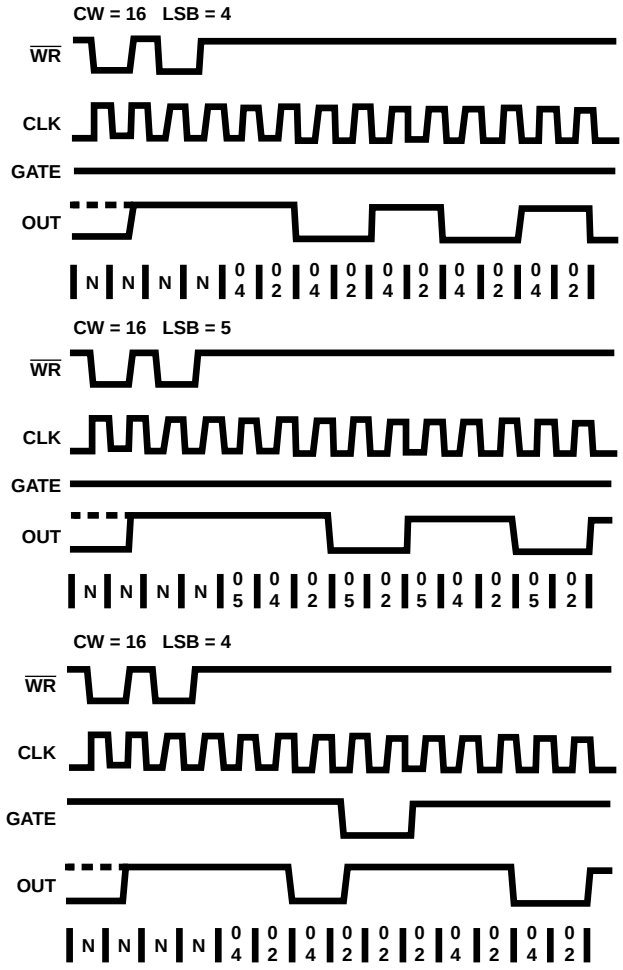


FIGURE 12. MODE 3

Mode 3 is Implemented as Follows:

EVEN COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires, OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

ODD COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse, decremented by one on the next CLK pulse, and then decremented by two on succeeding CLK pulses. When the count expires, OUT goes low and the Counter is reloaded with the initial count. The count is decremented by three on the next CLK pulse, and then by two on succeeding CLK pulses. When the count expires, OUT goes high again and the Counter is reloaded with the initial count. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N + 1)/2 counts and low for (N - 1)/2 counts.

Mode 4: Software Triggered Mode

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse then go high again. The counting sequence is “Triggered” by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

(1) Writing the first byte has no effect on counting.

(2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be “retriggered” by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

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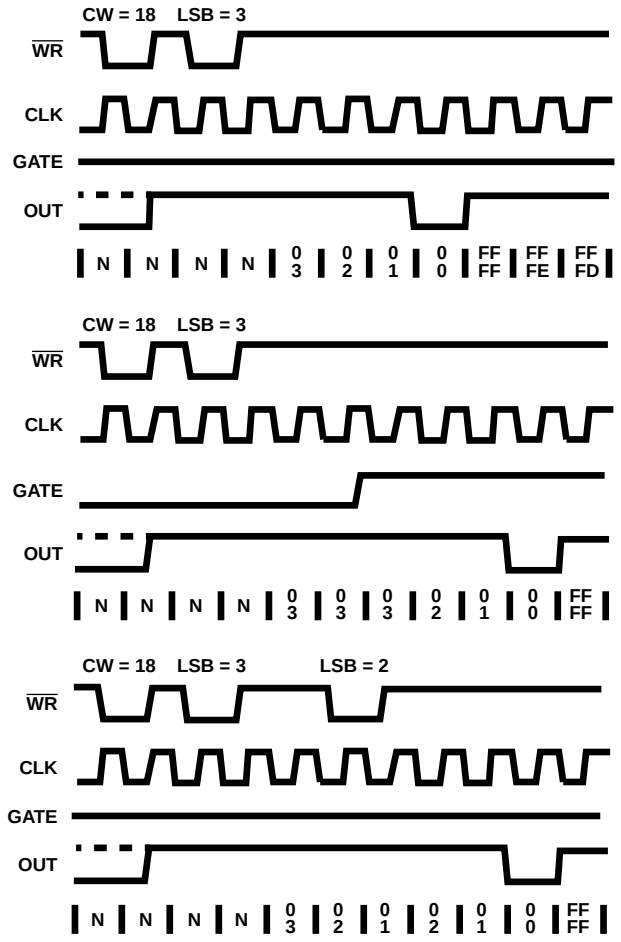


FIGURE 13. MODE 4

Mode 5: Hardware Triggered Strobe (Retriggerable)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is triggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with new count on the next CLK pulse and counting will continue from there.

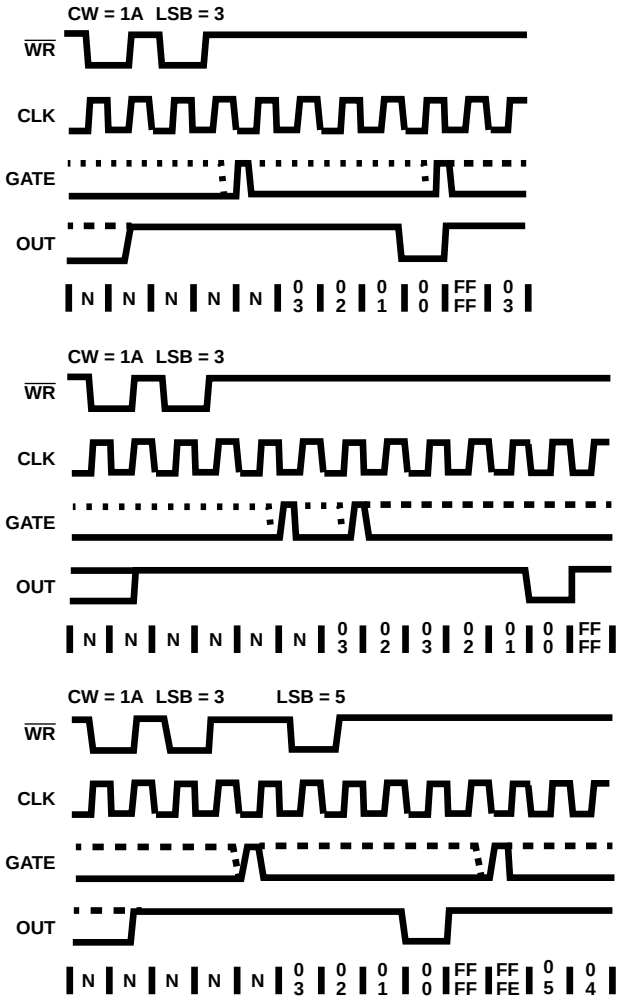


FIGURE 14. MODE 5

Operation Common to All Modes

Programming

When a Control Word is written to a Counter, all Control Logic, is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

Gate

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3 and 4 the GATE input is level sensitive, and logic level is sampled on the rising edge of CLK. In modes 1, 2, 3 and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of Gate (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK. The flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs - a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge- and level-sensitive.

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Counter

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The counter does not stop when it reaches zero. In Modes 0, 1, 4, and 5 the Counter “wraps around” to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

SIGNAL STATUS MODES	LOW OR GOING LOW	RISING	HIGH
0	Disables Counting	-	Enables Counting
1	-	1) Initiates Counting 2) Resets output after next clock	-
2	1) Disables counting 2) Sets output immediately high	Initiates Counting	Enables Counting
3	1) Disables counting 2) Sets output immediately high	Initiates Counting	Enables Counting
4	1) Disables Counting	-	Enables Counting
5	-	Initiates Counting	-

FIGURE 15. GATE PIN OPERATIONS SUMMARY

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

NOTE: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

FIGURE 16. MINIMUM AND MAXIMUM INITIAL COUNTS

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