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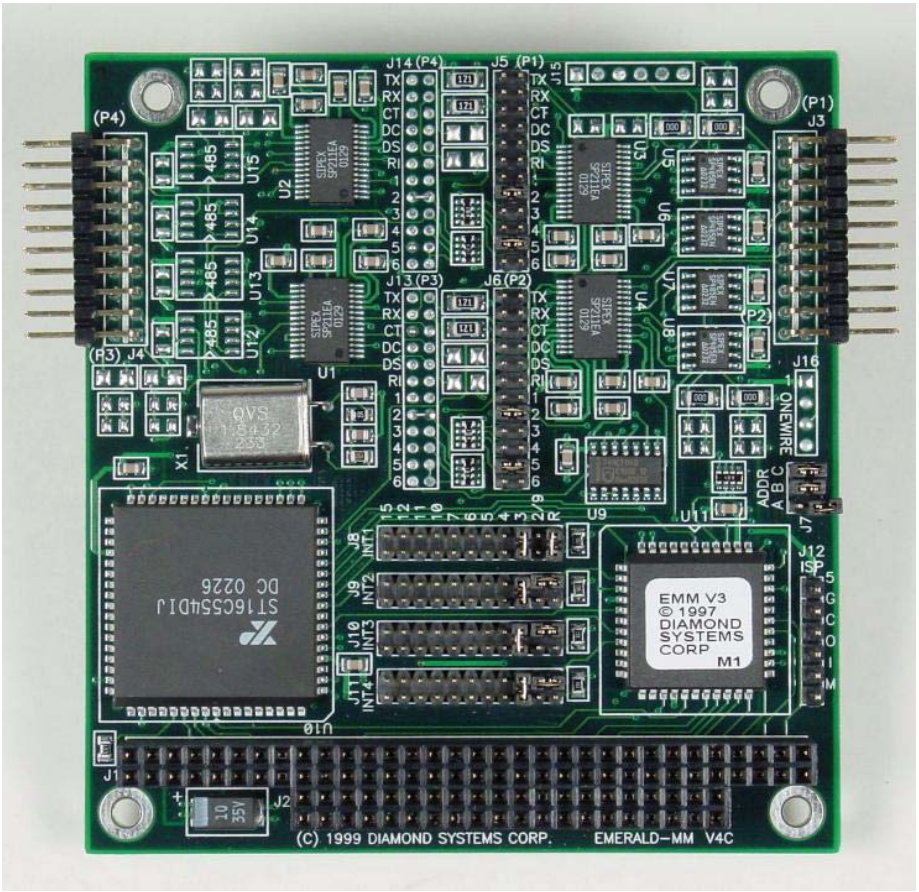
Find the *Diamond Systems EMM-XT* at our website: ***Click HERE***

DIAMOND SYSTEMS CORPORATION

EMERALD-MM

4-Channel Multi-Protocol Serial Port
PC/104 Module

User Manual V4.13



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1. DESCRIPTION

Emerald-MM is a PC/104 format I/O module with 4 serial ports. The board is available in multiple versions with different combinations of protocols:

EMM-XT	2 ports configurable for RS-232, RS-422, or RS-485; 2 ports fixed RS-232 (standard configuration)
EMM-4M-XT	4 ports configurable for RS-232, RS-422, or RS-485
EMM-4232-XT	4 ports fixed in RS-232
EMM-4485-XT	4 ports configurable for RS-422 or RS-485 (special order)
EMM-1W-XT	4 ports fixed RS-232; port 1 has 1-Wire interface (special order)

Eight different I/O address combinations can be selected, and 10 different interrupt levels can be assigned to configure each port, allowing operation as COM1 through COM4 as well as many other settings. Two I/O headers are provided, with two serial ports on each header. The board operates on +5V only, eliminating the need for a +12V supply that is often required for serial port operation.

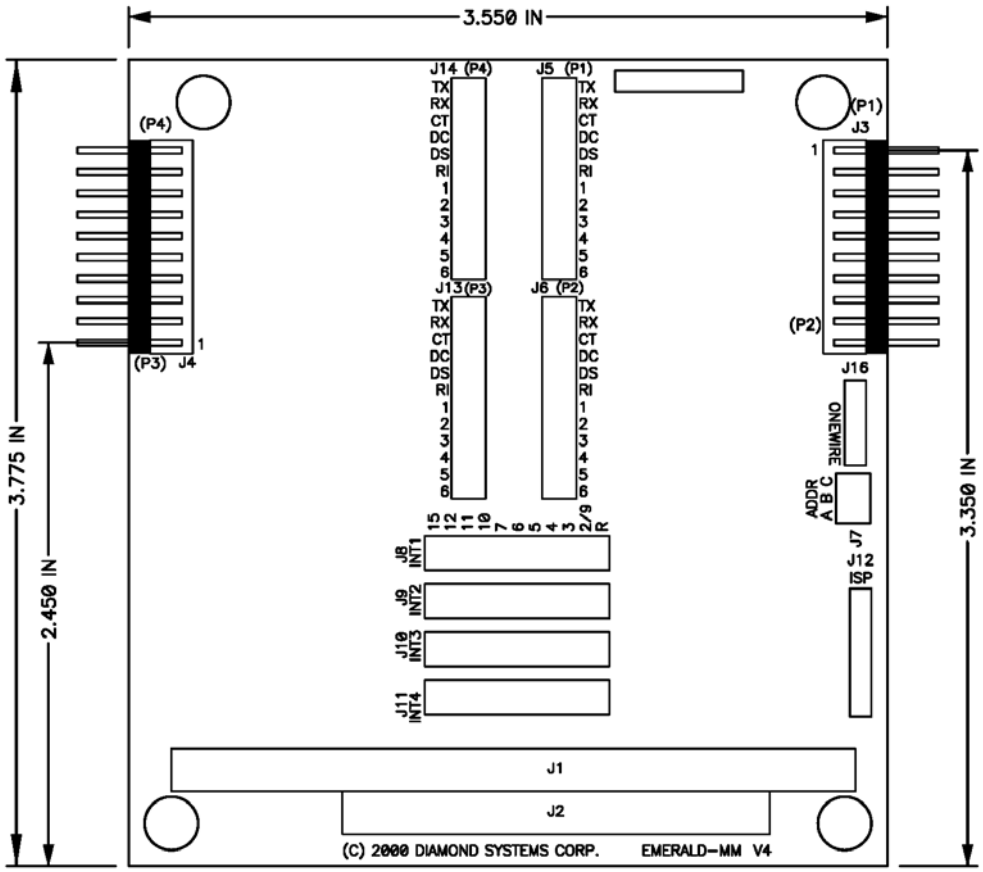
Emerald-MM is based on the 16C554 quad serial port IC. This device contains 4 identical sets of registers, one for each port, and is compatible with the standard PC serial port. Each port contains a 16-byte FIFO. Complete descriptions of these registers may be found in the Appendix. Most users will not need this programming information, as it is normally handled by the operating system's communications software.

2. FEATURES

- 4 16C550-compatible serial ports with 16-byte FIFOs
- RS-232, RS-422, RS-485, and 1-Wire interface capability (depending on the model)
- Up to 115.2kbps in standard configuration (460.8kbps available)
- 8 different I/O address options
- 10 different interrupt level options (using 16-bit PC/104 bus extension)
- I/O lines are short circuit protected
- Dual 20-pin I/O headers, 2 ports per header
- +5V only operation
- Extended temperature (-40 to +85^{o}C) operation

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3. MECHANICAL DRAWING



Description of Key Elements

J1 PC/104 8-bit bus connector
J2 PC/104 16-bit bus connector
J3 User I/O header for serial ports 1 and 2
J4 User I/O header for serial ports 3 and 4
J5 Configuration for serial port 1
J6 Configuration for serial port 2
J7 I/O address configuration
J8 Interrupt level configuration for port 1
J9 Interrupt level configuration for port 2
J10 Interrupt level configuration for port 3
J11 Interrupt level configuration for port 4
J12 Factory use only
J13 Configuration for serial port 3
J14 Configuration for serial port 4
J16 1-Wire interface (Model EMM-1W-XT only)

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4. SERIAL PORT I/O HEADER PINOUT AND PIN DESCRIPTION

Emerald-MM provides two identical 20-pin headers labeled J3 and J4 for the 4 serial ports. Two ports are contained on each header. Pin 1 and numbers are marked on the board for connector polarity identification.

For 1-Wire interface see page 10.

RS-232 Configuration:

J3

DCD 1	1	2	DSR 1
RXD 1	3	4	RTS 1
TXD 1	5	6	CTS 1
DTR 1	7	8	RI 1
GND	9	10	NC
DCD 2	11	12	DSR 2
RXD 2	13	14	RTS 2
TXD 2	15	16	CTS 2
DTR 2	17	18	RI 2
GND	19	20	NC

J4

DCD 3	1	2	DSR 3
RXD 3	3	4	RTS 3
TXD 3	5	6	CTS 3
DTR 3	7	8	RI 3
GND	9	10	NC
DCD 4	11	12	DSR 4
RXD 4	13	14	RTS 4
TXD 4	15	16	CTS 4
DTR 4	17	18	RI 4
GND	19	20	NC

RS-422 Configuration:

J3

NC	1	2	NC
TXD+ 1	3	4	TXD- 1
GND	5	6	RXD- 1
RXD+ 1	7	8	NC
GND	9	10	NC
NC	11	12	NC
TXD+ 2	13	14	TXD- 2
GND	15	16	RXD- 2
RXD+ 2	17	18	NC
GND	19	20	NC

J4

NC	1	2	NC
TXD+ 3	3	4	TXD- 3
GND	5	6	RXD- 3
RXD+ 3	7	8	NC
GND	9	10	NC
NC	11	12	NC
TXD+ 4	13	14	TXD- 4
GND	15	16	RXD- 4
RXD+ 4	17	18	NC
GND	19	20	NC

RS-485 Configuration:

J3

NC	1	2	NC
TXD/RXD+ 1	3	4	TXD/RXD- 1
GND	5	6	NC
NC	7	8	NC
GND	9	10	NC
NC	11	12	NC
TXD/RXD+ 2	13	14	TXD/RXD- 2
GND	15	16	NC
NC	17	18	NC
GND	19	20	NC

J4

NC	1	2	NC
TXD/RXD+ 3	3	4	TXD/RXD- 3
GND	5	6	NC
NC	7	8	NC
NC	9	10	NC
NC	11	12	NC
TXD/RXD+ 4	13	14	TXD/RXD- 4
GND	15	16	NC
NC	17	18	NC
NC	19	20	NC

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Signal Definitions:

Signal Name	Definition	Direction
RS-232:		
DCD	Data Carrier Detect	Input
DSR	Data Set Ready	Input
RXD	Receive Data	Input
RTS	Request To Send	Output
TXD	Transmit Data	Output
CTS	Clear To Send	Input
DTR	Data Terminal Ready	Output
RI	Ring Indicator	Input
RS-422:		
TXD+, TXD-	Differential Transmit Data	Output
RXD+, RXD-	Differential Receive Data	Input
RS-485:		
TXD/RXD+	Differential Transmit/Receive +	Bi-directional
TXD/RXD-	Differential Transmit/Receive -	Bi-directional
Common to all protocols:		
GND	Ground	--
NC	Not Connected	--

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5. BOARD CONFIGURATION

5.1 Port and Interrupt Register Address Selection

Each peripheral board in the computer system must have a unique I/O address or block of addresses. Emerald-MM actually uses five I/O address blocks: one for each of the four serial ports and one for the interrupt status register. Each port's address block consists of 8 consecutive addresses, while the interrupt status register occupies a single address.

The I/O addresses are set with jumper block J7, located at the right edge of the board. Eight different I/O address combinations are selectable. The address shown below for each port is the base address of that port, i.e. the lowest address of the port's I/O address block.

A	B	C	Port 1	Port 2	Port 3	Port 4	Interrupt Status
In	In	In	3F8	2F8	3E8	2E8	220
Out	In	In	3E8	2E8	3A8	2A8	220
In	Out	In	380	388	288	230	224
Out	Out	In	240	248	260	268	224
In	In	Out	100	108	110	118	240
Out	In	Out	120	128	130	138	244
In	Out	Out	140	148	150	158	248
Out	Out	Out	160	168	170	178	24C

5.2 Serial Protocol Selection

J5:	Port 1 protocol configuration
J6:	Port 2 protocol configuration
J13:	Port 3 protocol configuration
J14:	Port 4 protocol configuration

Depending on the model you have, different protocol configurations are possible. For configurable versions, protocol selection is made by installing jumpers in the positions indicated below in the configuration headers J5, J6, J13, and J14. For fixed protocol versions, the configuration is preset with wire jumpers in these same positions.

RS-422 is full-duplex, while RS-485 is half-duplex. In multi-drop mode the transmitter is controlled by the RTS line. This feature requires software control and is not automatic.

Protocol	1	2	3	4	5	6
RS-232 DTE, point to point	Out	In	Out	Out	In	Out
RS-422, point to point	In	Out	In	Out	Out	Out
RS-422, multi-drop	In	Out	In	Out	Out	In
RS-485, multi-drop	In	Out	Out	In	Out	In

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5.3 Configuration for RS-422 and RS-485 Modes

When RS-422 or RS-485 modes are selected, not all signals are used by the line drivers and receivers. Depending on your software configuration, you may need to force some inputs true so that your software will operate correctly. Jumper blocks J5, J6, J13, and J14 provide a means to force the input signals true (connect them to ground, or logic 0) for ports 1 – 4, respectively. The signals that can be controlled in this fashion are CTS, DCD, DSR, and RI. To force an input signal true on a port, install a jumper next to that signal's name on the corresponding header for that port. Jumpers should not be installed in these locations for RS-232 operation.

NOTE: The positions TX and RX are not used for this purpose. Installing jumpers in these locations has an entirely different meaning. See Cable Endpoint Termination below.

5.4 RS-422 / RS-485 Cable Endpoint Termination

In RS-422 or RS-485 networks, termination resistors are normally installed at the endpoints of the cables to minimize reflections on the lines. Emerald-MM provides 120Ω resistors for this purpose. To enable resistor termination, install jumpers in the locations TX and RX of J5, J6, J13, or J14 (for ports 1 – 4, respectively). Termination is only needed, and should only be used, at the cable endpoints. Installing termination resistors at additional points in the network may cause overloading and failure of the line drivers due to the lower impedance caused by multiple resistors in parallel.

5.5 Interrupt Levels

J8:	Port 1 interrupt configuration
J9:	Port 2 interrupt configuration
J10:	Port 3 interrupt configuration
J11:	Port 4 interrupt configuration

Each serial port requires an interrupt level as well as a base I/O address. Four jumper blocks, J8 through J11, are provided to select the interrupt level for each port from among levels 2, 3, 4, 5, 6, 7, 10, 11, 12, and 15. Install a jumper in the position corresponding to the desired interrupt level for each port.

Note: Interrupt levels 2 – 7 are available on the standard 8-bit PC/104 bus header J1. If you are using an 8-bit bus, these are the only levels available to you. Interrupt levels 10, 11, 12, and 15 are available on the 16-bit PC/104 bus extension header J2. If you are using a 16-bit bus, then all 10 levels are available to you. Also, on a system with a 16-bit bus, interrupt level 2 is rerouted to level 9.

5.6 Interrupt Sharing

On the PC/104 bus, interrupt levels may be shared by multiple devices. For this reason, the interrupt is driven to a logic high level by the device requesting service, and when the device is serviced it tri-states the line rather than driving it low. This technique avoids contention by two devices trying to drive the line with opposing logic levels.

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5.7 Interrupt Pulldown Resistor

In order to guarantee valid logic levels on the line when the device is not requesting service, each active interrupt level requires a 1KΩ pulldown resistor. Only one such resistor should be used on each active interrupt line. Each interrupt configuration header on Emerald-MM has a position marked "R" for enabling the pulldown resistor. Install a jumper in this position to connect the resistor, and remove the jumper to disconnect the resistor. If two or more ports are sharing the same interrupt level, install the jumper in the R position for any one of the ports and leave it off the others.

5.8 Interrupt Status Register

The interrupt status register indicates the status of each port's interrupt request line. It operates regardless of whether interrupt sharing is enabled (see below). If two or more ports are sharing the same interrupt level, the status register will still indicate the correct status of each port's interrupt request line.

Bit No.	7	6	5	4	3	2	1	0
Name	X	X	X	X	INT4	INT3	INT2	INT1

Definitions:

X Bit not used; generally reads back as a 1

INT4-1 Status of interrupt request for each port:

0 = no interrupt request active for this port
1 = interrupt request active for this port

5.9 Default Settings

The default settings for Emerald-MM are as follows:

Protocol settings:

All ports set for RS-232

Address/Interrupt settings:

(J7 A B C = In In Out):

Feature	Address	Interrupt level
Port 1	100	3
Port 2	108	3
Port 3	100	3
Port 4	108	3
Interrupt Status	240	

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6. RS-485 TRANSMITTER CONTROL

In an RS-485 network, the same pair of wires is used for both transmit and receive signals. Although any number of nodes can be listening simultaneously, only one can be transmitting or have its transmitter turned on in order for valid data to be transmitted across the network. On Emerald-MM, an RS-485 port's transmitter enable signal is controlled by that port's RTS signal. The RTS signal must be asserted (driven low) to enable the transmitter and deasserted (driven high) to turn off the transmitter.

7. 1-WIRE INTERFACE

In model **EMM-1W-XT**, a 1-Wire interface module (HA7S from Point Six, Inc.) is mounted on the board near the top edge. This port converts the RS-232 signals from port 1 into 1-Wire signals. The user connections for port 1 are made through a separate 4-pin header **J16** on the right side of the board. The port 1 signals on pins 1-10 of J3 may not be used because of conflicts with the RX line being driven by the 1-Wire interface module.

On model EMM-1W-XT, Ports 2, 3, and 4 are fixed in RS-232 mode.

J16 1-Wire Pinout

1	+5
2	Gnd
3	1-Wire
4	Gnd

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8. INSTALLING EMERALD-MM IN WINDOWS NT

1. Run REGEDT32.EXE and go to the following dialog box:

   Key_Local_Machine \ System \ CurrentControlSet \ Service \ Serial \ Parameters

2. Add a new key for each serial port by selecting Edit \ Add Key. The following parameters need to be specified for each serial port:

   SerialN (N = serial port number, 1, 2, 3, 4, etc.):

Parameter	Type	Value, Comments
DosDevices	REG_SZ	Name of port, e.g. COM5, COM6
ForceFifoEnable	REG_DWORD	0x1 for yes
Interrupt	REG_DWORD	IRQ level in Hex format, e.g. 0x5 for 5 or 0xa for 10
InterruptStatus	REG_DWORD	Address of interrupt status register in Hex, e.g. 0x224
PortAddress	REG_DWORD	Address or port in Hex, e.g. 0x120 for Hex 120
PortIndex	REG_DWORD	Bit position in status register: 0x1 for LSB through 0x4
SharedInterrupts	REG_DWORD	0x1 for yes, 0x0 for no

3. Exit REGEDT32.EXE and restart NT.

See the example on the following page.

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Windows NT Example

The following example is for an EMM-XT board installed on a CPU that already contains 2 serial ports called COM1 and COM2. The address setting combination is A out, B in, C out, and all ports are sharing interrupt level 12. Note that all ports share the same interrupt status register, but the bit position changes.

	Port 1	Port 2	Port 3	Port 4	Interrupt Status Register
Address	0x120	0x128	0x130	0x138	0x244
Interrupt Level	12	12	12	12	

Serial3:

DosDevices	REG_SZ	COM3
ForceFifoEnable	REG_DWORD	0x1
Interrupt	REG_DWORD	0xc
InterruptStatus	REG_DWORD	0x244
PortAddress	REG_DWORD	0x120
PortIndex	REG_DWORD	0x1
SharedInterrupts	REG_DWORD	0x1

Serial4:

DosDevices	REG_SZ	COM4
ForceFifoEnable	REG_DWORD	0x1
Interrupt	REG_DWORD	0xc
InterruptStatus	REG_DWORD	0x244
PortAddress	REG_DWORD	0x128
PortIndex	REG_DWORD	0x2
SharedInterrupts	REG_DWORD	0x1

Serial5:

DosDevices	REG_SZ	COM5
ForceFifoEnable	REG_DWORD	0x1
Interrupt	REG_DWORD	0xc
InterruptStatus	REG_DWORD	0x244
PortAddress	REG_DWORD	0x130
PortIndex	REG_DWORD	0x3
SharedInterrupts	REG_DWORD	0x1

Serial6:

DosDevices	REG_SZ	COM6
ForceFifoEnable	REG_DWORD	0x1
Interrupt	REG_DWORD	0xc
InterruptStatus	REG_DWORD	0x244
PortAddress	REG_DWORD	0x138
PortIndex	REG_DWORD	0x4
SharedInterrupts	REG_DWORD	0x1

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9. SPECIFICATIONS

Serial Port Specifications

No. of serial ports:	4
Protocol:	RS-232, RS-422, RS-485 Jumper selected or fixed, depending on the version
Maximum baud rate:	115kbps standard version 460.8kbps available (**-HS** option)
Communications parameters:	5, 6, 7, or 8 data bits; Even, odd, or no parity
Short circuit protection:	All outputs protected against continuous short circuit

RS-232 mode:

Input impedance:	3KΩ min
Input voltage swing:	±30V max
Output voltage swing:	±5V min, ±7V typical

RS-422, RS-485 modes:

Differential input threshold:	-0.2V min, +0.2V max
Input impedance:	12KΩ min
Input current:	+1.0mA max (V_{IN} = 12V) -0.8mA max (V_{IN} = -7V)
Differential output voltage:	2.0V min (R_L = 50Ω)
High/low states differential output voltage symmetry:	0.2V max

General Specifications

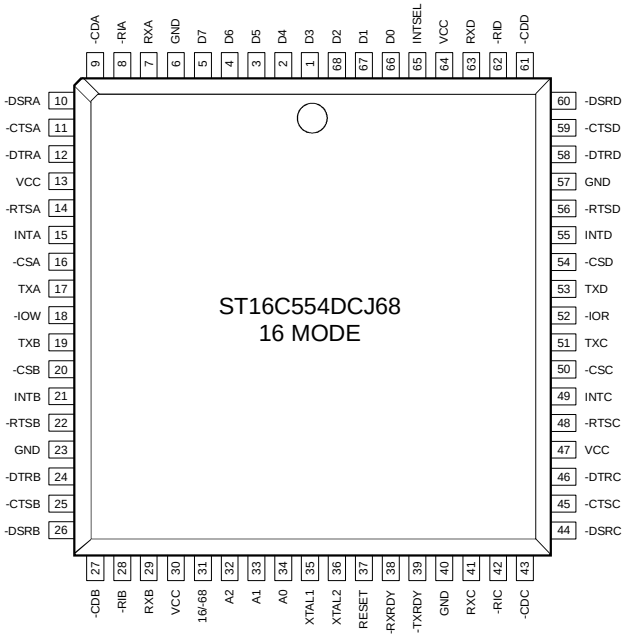
I/O header:	2 20-position (2x10) .025” square pin header on .1” centers; Headers mate with standard ribbon cable (IDC) connectors
Dimensions:	3.55” x 3.775” (PC/104 standard)
Power supply:	+5VDC ±10%
Current consumption:	80mA typical, all outputs unloaded
Operating temperature:	-40 to +85°C standard
Operating humidity:	5% to 95% noncondensing
PC/104 bus:	8 bit and 16-bit bus headers are installed and used (16-bit header is used for interrupt levels only)

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DESCRIPTION

The ST16C554D is a universal asynchronous receiver and transmitter (UART) with a dual foot print interface. The 554D is an enhanced UART with 16 byte FIFOs, receive trigger levels and data rates up to 1.5Mbps. Onboard status registers provide the user with error indications and operational status, modem interface control. System interrupts may be tailored to meet user requirements. An internal loopback capability allows onboard diagnostics. The 554D is available in 64 pin TQFP, and 68 pin PLCC packages. The 68 pin PLCC package offer an additional 68 mode which allows easy integration with Motorola, and other popular microprocessors. The ST16C554CQ64 (64 pin) offers three state interrupt control while the ST16C554DCQ64 provides constant active interrupt outputs. The 64 pin devices do not offer TXRDY/ RXRDY outputs. The 554D combines the package interface modes of the 16C554 and 68C554 series on a single integrated chip.

PLCC Package



FEATURES

- Compatibility with the Industry Standard ST16C454, ST68C454, ST68C554, TL16C554
- 1.5 Mbps transmit/receive operation (24MHz)
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Independent transmit and receive control
- Software selectable Baud Rate Generator
- Four selectable Receive FIFO interrupt trigger levels
- Standard modem interface

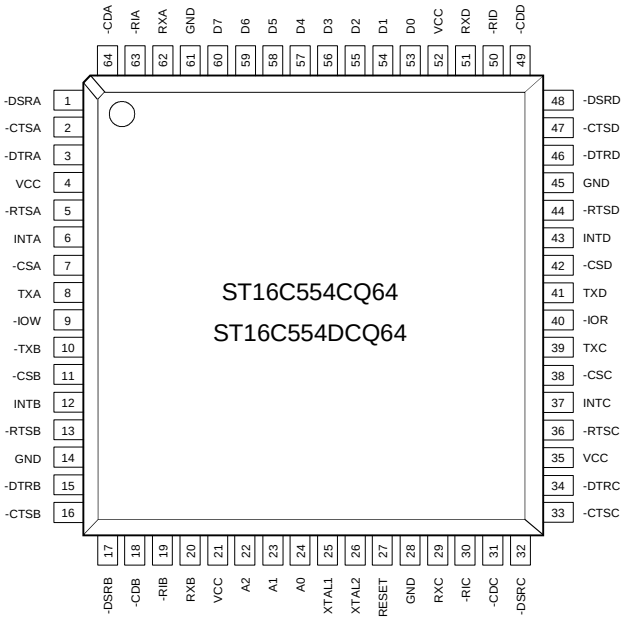
ORDERING INFORMATION

Part number	Pins	Package	Operating temperature
ST16C554DCJ68	68	PLCC	0° C to + 70° C
ST16C554DCQ64	64	TQFP	0° C to + 70° C
ST16C554CQ64	64	TQFP	0° C to + 70° C
ST16C554DIJ68	68	PLCC	-40° C to + 85° C
ST16C554DIQ64	64	TQFP	-40° C to + 85° C

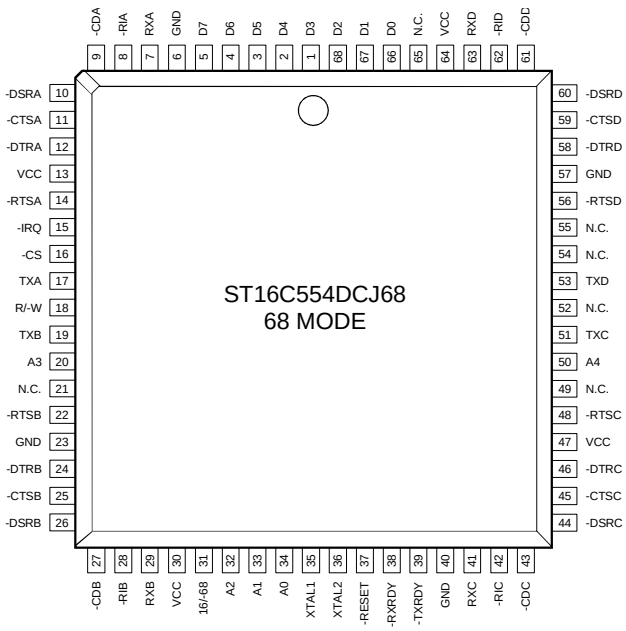
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Figure 1, Package Descriptions

64 Pin TQFP Package

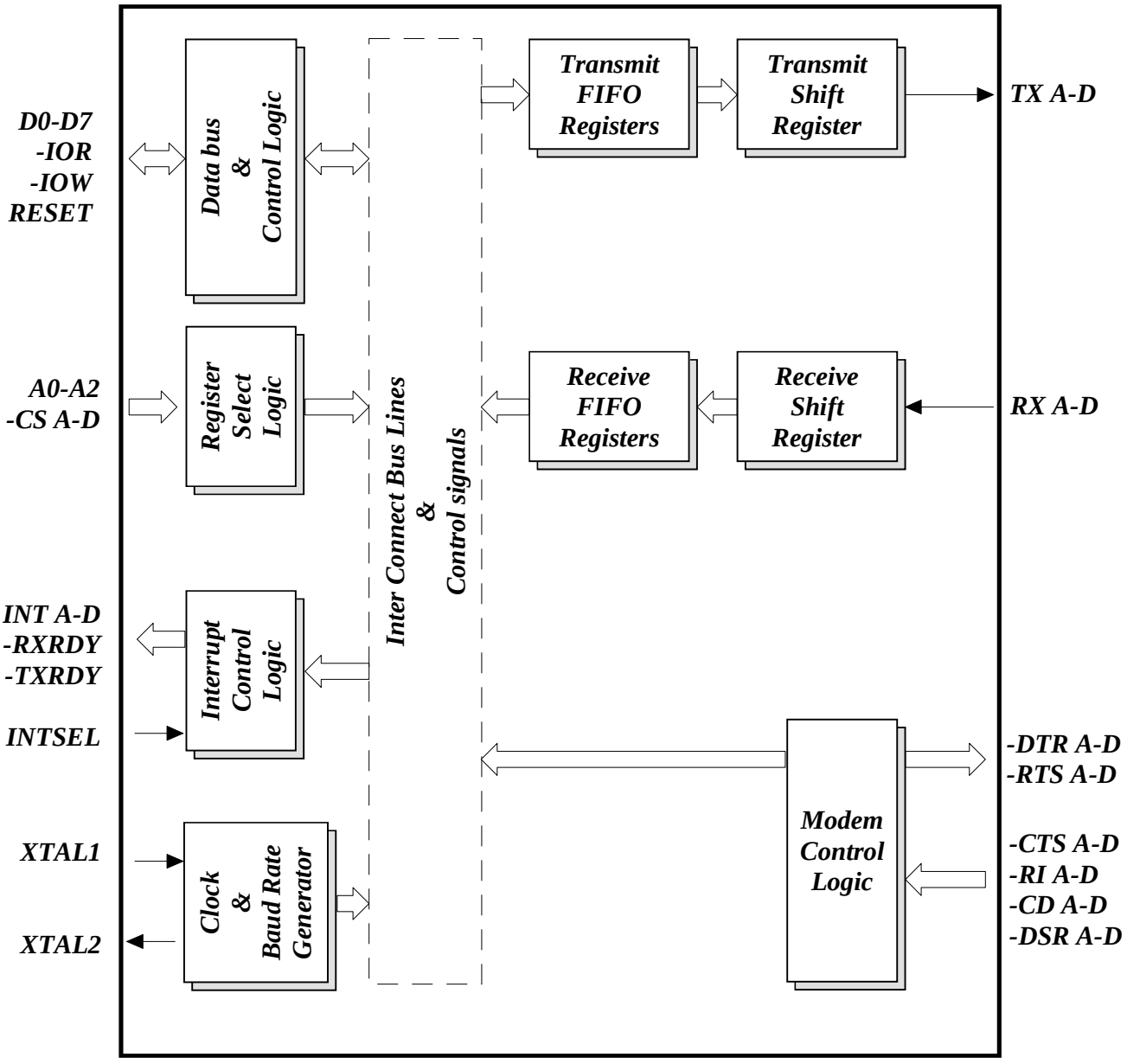


68 Pin PLCC Package



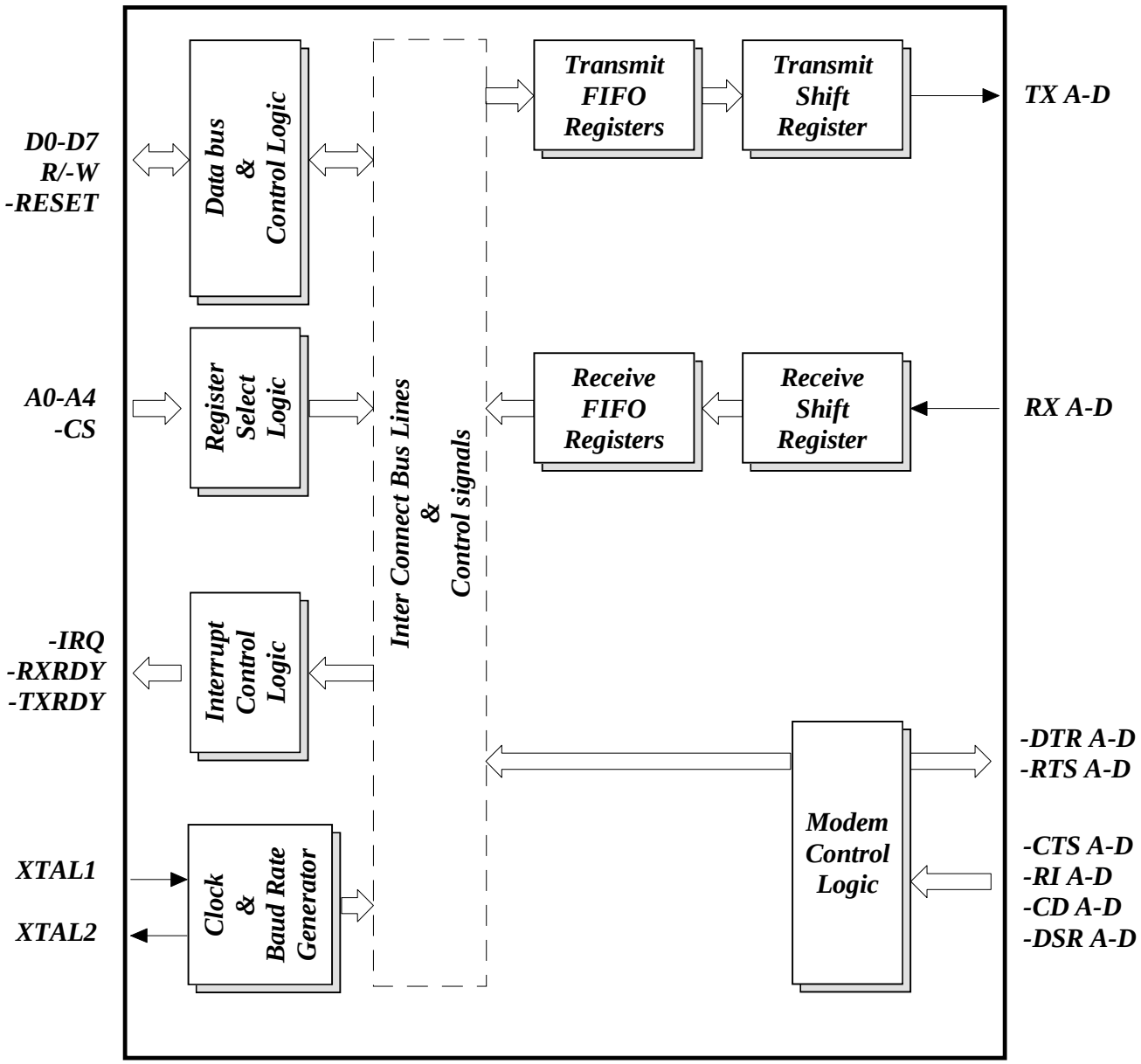
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Figure 2, Block Diagram 16 Mode



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Figure 3, Block Diagram 68 Mode



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SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 64	Signal type	Pin Description
16/-68	31	-	I	16/68 Interface Type Select (input with internal pull-up). - This input provides the 16 (Intel) or 68 (Motorola) bus interface type select. The functions of -IOR, -IOW, INT A-D, and -CS A-D are re-assigned with the logical state of this pin. When this pin is a logic 1, the 16 mode interface 16C554D is selected. When this pin is a logic 0, the 68 mode interface (68C554) is selected. When this pin is a logic 0, -IOW is re-assigned to -R/W, RESET is re-assigned to -RESET, -IOR is not used, and INT A-D(s) are connected in a WIRE-OR" configuration. The WIRE-OR outputs are connected internally to the open source IRQ signal output. This pin is not available on 64 pin packages which operate in the 16 mode only.
A0	34	24	I	Address-0 Select Bit. Internal registers address selection in 16 and 68 modes.
A1	33	23	I	Address-1 Select Bit. Internal registers address selection in 16 and 68 modes.
A2	32	22	I	Address-2 Select Bit. - Internal registers address selection in 16 and 68 modes.
A3-A4	20,50	-	I	Address 3-4 Select Bits. - When the 68 mode is selected, these pins are used to address or select individual UART's (providing -CS is a logic 0). In the 16 mode, these pins are reassigned as chip selects, see -CSB and -CSC. These pins are not available on 64 pin packages which operate in the 16 mode only.
-CS	16	-	I	Chip Select. (active low) - In the 68 mode, this pin functions as a multiple channel chip enable. In this case, all four UARTs (A-D) are enabled when the -CS pin is a logic 0. An individual UART channel is selected by the data contents of address bits A3-A4. When the 16 mode is selected (68 pin device), this pin functions as -CSA, see definition under -CS A-B. This pin is not available on 64 pin packages which operate in the 16 mode only.

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SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 64	Signal type	Pin Description
-CS A-B -CS C-D	16,20 50,54	7,11 38,42	I	Chip Select A, B, C, D (active low) - This function is associated with the 16 mode only, and for individual channels, “A” through “D.” When in 16 Mode, these pins enable data transfers between the user CPU and the ST16C554D for the channel(s) addressed. Individual UART sections (A, B, C, D) are addressed by providing a logic 0 on the respective -CS A-D pin. When the 68 mode is selected, the functions of these pins are reassigned. 68 mode functions are described under the their respective name/pin headings.
D0-D2 D3-D7	66-68 1-5	53-55 56-60	I/O	Data Bus (Bi-directional) - These pins are the eight bit, three state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
GND GND	6,23 40,57	14,28 45,61	Pwr	Signal and power ground.
INT A-B INT C-D	15,21 49,55	6,12 37,43	O	Interrupt A, B, C, D (active high) - This function is associated with the 16 mode only. These pins provide individual channel interrupts, INT A-D. INT A-D are enabled when MCR bit-3 is set to a logic 1, interrupts are enabled in the interrupt enable register (IER), and when an interrupt condition exists. Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected. When the 68 mode is selected, the functions of these pins are reassigned. 68 mode functions are described under the their respective name/pin headings.
INTSEL	65	-	I	Interrupt Select. (active high, with internal pull-down) - This function is associated with the 16 mode only. When the 16 mode is selected, this pin can be used in conjunction with MCR bit-3 to enable or disable the three state interrupts, INT A-D or override MCR bit-3 and force continuous interrupts. Interrupt outputs are enabled continuously by making this

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SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 64	Signal type	Pin Description
				pin a logic 1. Making this pin a logic 0 allows MCR bit-3 to control the three state interrupt output. In this mode, MCR bit-3 is set to a logic "1" to enable the three state outputs. This pin is disabled in the 68 mode. Due to pin limitations on 64 pin packages, this pin is not available. To cover this limitation, two 64 pin QFP package versions are offered. The ST16C554DCQ64 operates in the continuos interrupt enable mode by bonded this pin to VCC internally. The ST16C554CQ64 operates with MCR bit-3 control by bonding this pin to GND.
-IOR	52	40	I	Read strobe. (active low Strobe) - This function is associated with the 16 mode only. A logic 0 transition on this pin will load the contents of an Internal register defined by address bits A0-A2 onto the ST16C554D data bus (D0-D7) for access by an external CPU. This pin is disabled in the 68 mode.
-IOW	18	9	I	Write strobe. (active low strobe) - This function is associated with the 16 mode only. A logic 0 transition on this pin will transfer the contents of the data bus (D0-D7) from the external CPU to an internal register that is defined by address bits A0/A2. When the 16 mode is selected, this pin functions as -R/W, see definition under R/W.
-IRQ	15	-	O	Interrupt Request or Interrupt "A" - This function is associated with the 68 mode only. In the 68 mode, interrupts from UART channels A-D are WIRE-OR'ed" internally to function as a single IRQ interrupt. This pin transitions to a logic 0 (if enabled by the interrupt enable register) whenever a UART channel(s) requires service. Individual channel interrupt status can be determined by addressing each channel through its associated internal register, using -CS and A3-A4. In the 68 mode an external pull-up resistor must be connected between this pin and VCC. The function of this pin changes to INTA when operating in the 16 mode, see definition under INTA.

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SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 64	Signal type	Pin Description
-RESET RESET	37	27	I	Reset. - In the 16 mode a logic 1 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See ST16C554D External Reset Conditions for initialization details.) When 16/-68 is a logic 0 (68 mode), this pin functions similarly but, as an inverted reset interface signal, -RESET.
-R/W	18	-	I	Read/Write Strobe (active low) - This function is associated with the 68 mode only. This pin provides the combined functions for Read or Write strobes. A logic 1 to 0 transition transfers the contents of the CPU data bus (D0-D7) to the register selected by -CS and A0-A4. Similarly a logic 0 to 1 transition places the contents of a 554D register selected by -CS and A0-A4 on the data bus, D0-D7, for transfer to an external CPU.
-RXRDY	38	-	O	Receive Ready (active low) - This function is associated with 68 pin packages only. -RXRDY contains the wire “OR-ed” status of all four receive channel FIFOs, RXRDY A-D. A logic 0 indicates receive data ready status, i.e. the RHR is full or the FIFO has one or more RX characters available for unloading. This pin goes to a logic 1 when the FIFO/RHR is full or when there are no more characters available in either the FIFO or RHR. For 64/68 pin packages, individual channel RX status is read by examining individual internal registers via -CS and A0-A4 pin functions.
-TXRDY	39	-	O	Transmit Ready (active low) - This function is associated with 68 pin package only. -TXRDY contains the wire “OR-ed” status of all four transmit channel FIFOs, TXRDY A-D. A logic 0 indicates a buffer ready status, i.e., at least one location is empty and available in one of the TX channels (A-D). This pin goes to a logic 1 when all four channels have no more empty locations in the TX FIFO or THR.
VCC VCC	13 47,64	4,21 35,52	I	Power supply inputs.

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SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 64	Signal type	Pin Description
XTAL1	35	25	I	Crystal or External Clock Input - Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit (see figure 8). Alternatively, an external clock can be connected to this pin to provide custom data rates (see Baud Rate Generator Programming).
XTAL2	36	26	O	Output of the Crystal Oscillator or Buffered Clock - (See also XTAL1). Crystal oscillator output or buffered clock output.
-CD A-B -CD C-D	9,27 43,61	64,18 31,49	I	Carrier Detect (active low) - These inputs are associated with individual UART channels A through D. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.
-CTS A-B -CTS C-D	11,25 45,59	2,16 33,47	I	Clear to Send (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on the -CTS pin indicates the modem or data set is ready to accept transmit data from the 554D. Status can be tested by reading MSR bit-4.
-DSR A-B -DSR C-D	10,26 44,60	1,17 32,48	I	Data Set Ready (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UART's transmit or receive operation. This pin has no effect on the UART's transmit or receive operation.
-DTR A-B -DTR C-D	12,24 46,58	3,15 34,46	O	Data Terminal Ready (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates that the 554D is powered-on and ready. This pin can be controlled via the modem control register. Writing a logic 1 to MCR bit-0 will set the -DTR output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR bit-0. This pin has no effect on the UART's transmit or receive operation.

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SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 64	Signal type	Pin Description
-RI A-B -RI C-D	8,28 42,62	63,19 30,50	I	Ring Indicator (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt.
-RTS A-B -RTS C-D	14,22 48,56	5,13 36,44	O	Request to Send (active low) - These outputs are associated with individual UART channels, A through D. A logic 0 on the -RTS pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the modem control register (MCR bit-1) will set this pin to a logic 0 indicating data is available. After a reset this pin will be set to a logic 1. This pin has no effect on the UART's transmit or receive operation.
RX A-B RX C-D	7,29 41,63	62,20 29,51	I	Receive Data Input RX A-D. - These inputs are associated with individual serial channel data to the ST16C554D. The RX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loopback mode, the RX input pin is disabled and TX data is internally connected to the UART RX Input, internally.
TX A-B TX C-D	17,19 51,53	8,10 39,41	O	Transmit Data - These outputs are associated with individual serial transmit channel data from the 554D. The TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loopback mode, the TX input pin is disabled and TX data is internally connected to the UART RX Input.

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GENERAL DESCRIPTION

The 554D provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stops bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The ST16C554D represents such an integration with greatly enhanced features. The 554D is fabricated with an advanced CMOS process to achieve low drain power and high speed requirements.

The 554D is an upward solution that provides 16 bytes of transmit and receive FIFO memory, instead of 1 bytes provided in the 16/68C454. The 554D is designed to work with high speed modems and shared network environments, that require fast data processing time. Increased performance is realized in the 554D by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time.

The 554D combines the package interface modes of the 16C554D and 68C554 series on a single integrated chip. The 16 mode interface is designed to operate with the Intel type of microprocessor bus while the 68 mode is intended to operate with Motorola, and other popular microprocessors. Following a reset, the 554D is down-ward compatible with the ST16C454/ ST68C454 dependent on the state of the interface mode selection pin, 16/-68.

The 554D is capable of operation to 1.5Mbps with a 24 MHz crystal or external clock input. With a crystal of 14.7464 MHz, the user can select data rates up to 921.6Kbps.

The rich feature set of the 554D is available through internal registers. Selectable receive FIFO trigger levels, selectable TX and RX baud rates, modem interface controls. In the 16 mode INTSEL and MCR bit-3 can be configured to provide a software controlled or continuous interrupt capability. Due of pin limitations for the 64 pin 554D this feature is offered by two different QFP packages. The ST16C554DCQ64 operates in the continuos interrupt enable mode by bonded INTSEL to VCC internally. The ST16C554CQ64 operates in conjunction with MCR bit-3 by bonding INTSEL to GND internally.

FUNCTIONAL DESCRIPTIONS

Interface Options

Two user interface modes are selectable for the 554D package. These interface modes are designated as the “16 mode” and the “68 mode.” This nomenclature corresponds to the early 16C554D and 68C554 package interfaces respectively.

The 16 Mode Interface

The 16 mode configures the package interface pins for connection as a standard 16 series (Intel) device and operates similar to the standard CPU interface available on the 16C554D. In the 16 mode (pin 16/-68 logic 1) each UART is selected with individual chip select (CSx) pins as shown in Table 2 below.

Table 2, SERIAL PORT CHANNEL SELECTION GUIDE, 16 MODE INTERFACE

-CSA	-CSB	-CSC	-CSD	UART CHANNEL
1	1	1	1	None
0	1	1	1	A
1	0	1	1	B
1	1	0	1	C
1	1	1	0	D

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The 68 Mode Interface

The 68 mode configures the package interface pins for connection with Motorola, and other popular microprocessor bus types. The interface operates similar to the 68C454/554. In this mode the 554D decodes two additional addresses, A3-A4 to select one of the four UART ports. The A3-A4 address decode function is used only when in the 68 mode (16/-68 logic 0), and is shown in Table 3 below.

Table 3, SERIAL PORT CHANNEL SELECTION GUIDE, 68 MODE INTERFACE

-CS	A4	A3	UART CHANNEL
1	N/A	N/A	None
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D

Internal Registers

The 554D provides 13 internal registers for monitoring and control. These resisters are shown in Table 4 below. Twelve registers are similar to those already available in the standard 16C454. These registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user assessable scratchpad register (SPR). Register functions are more fully described in the following paragraphs.

Table 4, INTERNAL REGISTER DECODE

A2	A1	A0	READ MODE	WRITE MODE
General Register Set (THR/RHR, IER/ISR, MCR/MSR, LCR/LSR, SPR):				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
Baud Rate Register Set (DLL/DLM): Note *2				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch

Note *2: These registers are accessible only when LCR bit-7 is set to a logic 1.

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FIFO Operation

The 16 byte transmit and receive data FIFO's are enabled by the FIFO Control Register (FCR) bit-0. With 16C554 devices, the user can only set the receive trigger level. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

Timeout Interrupts

The interrupts are enabled by IER bits 0-3. Care must be taken when handling these interrupts. Following a reset the transmitter interrupt is enabled, the 554D will issue an interrupt to indicate that transmit holding register is empty. This interrupt must be serviced prior to continuing operations. The LSR register provides the current singular highest priority interrupt only. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time Out have the same interrupt priority (when enabled by IER bit-0). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case the 554D FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should recheck LSR bit-0 for additional characters. A Receive Time Out will not occur if the receive FIFO is empty. The time out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read. The actual time out value is T (**T**ime out length in bits) = 4 X P (**P**rogrammed word length) + 12. To convert the time out value to a character value, the user has to consider the complete word length, including data information length, start bit, parity bit, and the size of stop bit, i.e., 1X, 1.5X, or 2X bit times.

Example -A: If the user programs a word length of 7, with no parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) +12 = 40 bit times. The character time will be equal to 40 / 9 = 4.4 characters, or as shown in the fully worked out example: T = [(programmed word length = 7) + (stop bit = 1) + (start bit = 1) = 9]. 40 (bit times divided by 9) = 4.4 characters.

Example -B: If the user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bit times. Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

In the 16 mode for 68 pin packages, the system/board designer can optionally provide software controlled three state interrupt operation. This is accomplished by INTSEL and MCR bit-3. When INTSEL interface pin is left open or made a logic 0, MCR bit-3 controls the three state interrupt outputs, INT A-D. When INTSEL is a logic 1, MCR bit-3 has no effect on the INT A-D outputs and the package operates with interrupt outputs enabled continuously.

Programmable Baud Rate Generator

The 554D supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example a 33.6Kbps modem that employs data compression may require a 115.2Kbps input data rate. A 128.0Kbps ISDN modem that supports data compression may need an input data rate of 460.8Kbps. The 554D can support a standard data rate of 921.6Kbps.

A dual baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of accepting an input clock up to 24 MHz, as required for supporting a 1.5Mbps data rate. The 554D can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant/ 22-33 pF load) is connected externally between the XTAL1 and XTAL2 pins (see figure 8). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. (see Baud Rate Generator Programming).

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The generator divides the input 16X clock by any divisor from 1 to 2^{16} -1. The 554D divides the basic crystal or external clock by 16. Further division of this 16X clock provides two table rates to support low and high data rate applications using the same system design. Customized Baud Rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the Baud Rate Generator Registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 5 below, shows the two selectable baud rate tables available when using a 7.3728 MHz crystal.

Figure 8, Crystal oscillator connection

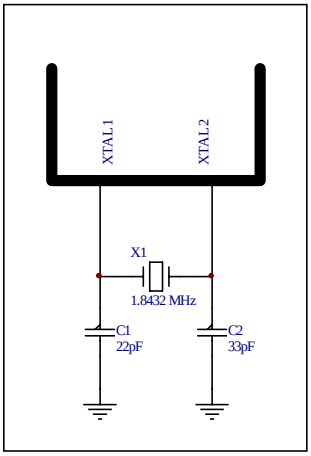


Table 5, BAUD RATE GENERATOR PROGRAMMING TABLE:

Output Baud Rate (1.8432 MHz Clock)	Output Baud Rate (7.3728 MHz Clock)	User 16 x Clock Divisor (Decimal)	User 16 x Clock Divisor (HEX)	DLM Program Value (HEX)	DLL Program Value (HEX)
50	200	2304	900	09	00
300	1200	384	180	01	80
600	2400	192	C0	00	C0
1200	4800	96	60	00	60
2400	9600	48	30	00	30
4800	19.2K	24	18	00	18
9600	38.4k	12	0C	00	0C
19.2k	76.8k	6	06	00	06
38.4k	153.6k	3	03	00	03
57.6k	230.4k	2	02	00	02
115.2k	460.8k	1	01	00	01

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DMA Operation

The 554D FIFO trigger level provides additional flexibility to the user for block mode operation. LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s). The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR bit-3). When the transmit and receive FIFOs are enabled and the DMA mode is deactivated (DMA Mode “0”), the 554D activates the interrupt output pin for each data transmit or receive operation. When DMA mode is activated (DMA Mode “1”), the user takes the advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the preset trigger level. In this mode, the 554D sets the interrupt output pin when characters in the transmit FIFOs are below the transmit trigger level, or the characters in the receive FIFOs are above the receive trigger level.

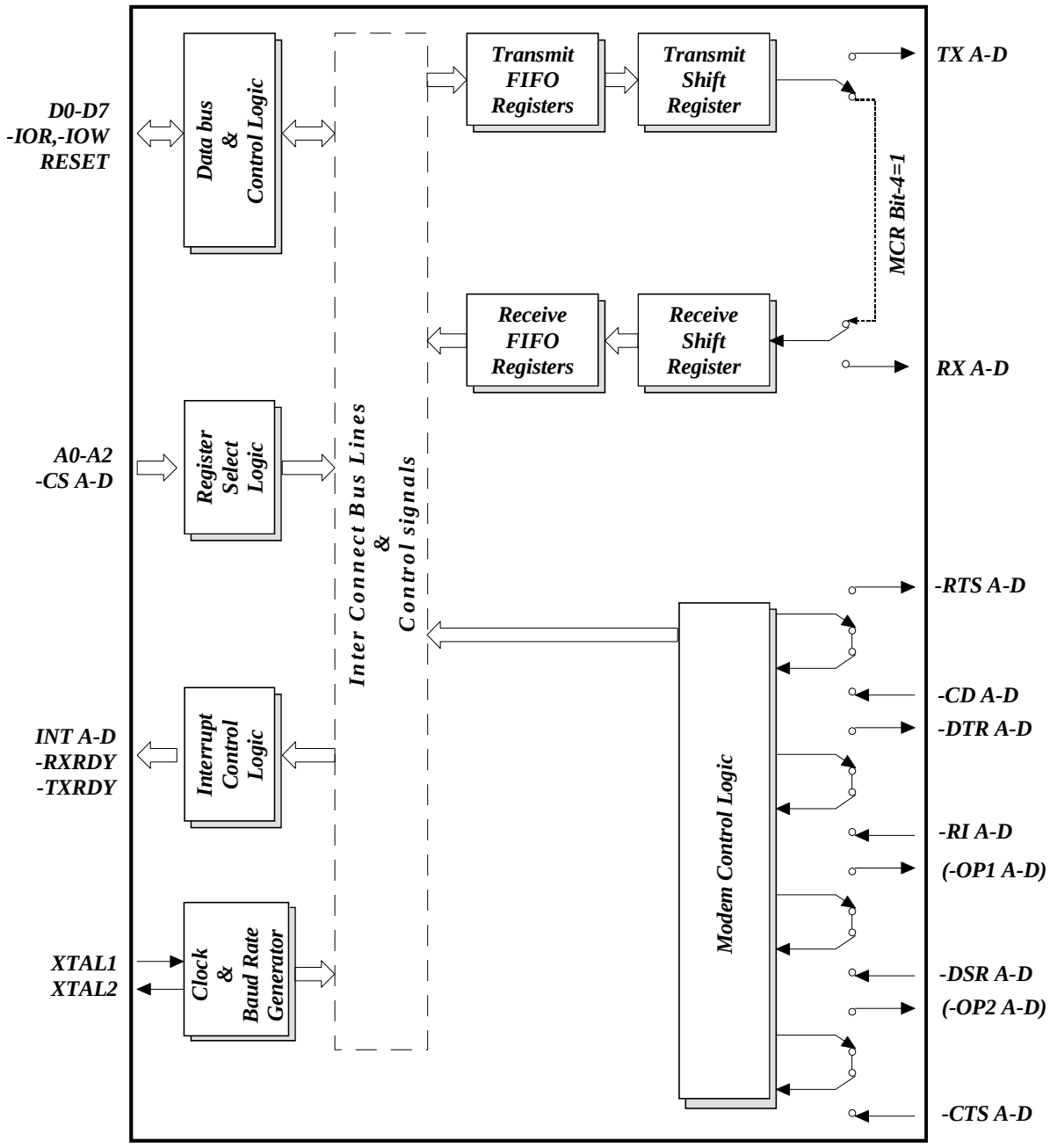
Loopback Mode

The internal loopback capability allows onboard diagnostics. In the loopback mode the normal modem interface pins are disconnected and reconfigured for loopback internally. MCR register bits 0-3 are used for controlling loopback diagnostic testing. In the loopback mode OP1 and OP2 in the MCR register (bits 3/2) control the modem -RI and -CD inputs respectively. MCR signals -DTR and -RTS (bits 0-1) are used to control the modem -CTS and -DSR inputs respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (See Figure 12). The -CTS, -DSR, -CD, and -RI are disconnected from their normal modem control inputs pins, and instead are connected internally to -DTR, -RTS, -OP1 and -OP2. Loopback test data is entered into the transmit holding register via the user data bus interface, D0-D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface, D0-D7. The user optionally compares the received data to the initial transmitted data for verifying error free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. However, the interrupts can only be read using lower four bits of the Modem Control Register (MCR bits 0-3) instead of the four Modem Status Register bits 4-7. The interrupts are still controlled by the IER.

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Figure 12, INTERNAL LOOPBACK MODE DIAGRAM



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REGISTER FUNCTIONAL DESCRIPTIONS

The following table delineates the assigned bit functions for the fifteen 554D internal registers. The assigned bit functions are more fully defined in the following paragraphs.

Table 6, ST16C554D INTERNAL REGISTERS

A2 A1 A0	Register [Note *5]	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
General Register Set									
0 0 0	RHR[XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR[XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER[00]	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR[01]	FIFO's enabled	FIFO's enabled	0	0	INT priority bit-2	INT priority bit-1	INT priority bit-0	INT status
0 1 1	LCR[00]	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR[00]	0	0	0	loop back	-OP2/ INTx enable	-OP1	-RTS	-DTR
1 0 1	LSR[60]	FIFO data error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR[X0]	CD	RI	DSR	CTS	delta -CD	delta -RI	delta -DSR	delta -CTS
1 1 1	SPR[FF]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Special Register set: Note *2									
0 0 0	DLL[XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM[XX]	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

Note *2: The Special register set is accessible only when LCR bit-7 is set to "1".

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Note *5: The value between the square brackets represents the register's initialized HEX value.

Transmit (THR) and Receive (RHR) Holding Registers

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7-D0) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the transmit holding register empty flag is set (logic 0 = FIFO full, logic 1= at least one FIFO location available).

The serial receive section also contains an 8-bit Receive Holding Register, RHR. Receive data is removed from the 554D and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at 16x clock rate. After 7 1/2 clocks the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INT A-D output pins in the 16 mode, or on WIRE-OR IRQ output pin, in the 68 mode.

IER Vs Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = a logic 1) and receive interrupts (IER BIT-0 = logic 1) are enabled, the receive interrupts and register status will reflect the following:

A) The receive data available interrupts are issued to the external CPU when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B) FIFO status will also be reflected in the user accessible ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

IER Vs Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1; resetting IER bits 0-3 enables the 554D in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A) LSR BIT-0 will be a logic 1 as long as there is one byte in the receive FIFO.

B) LSR BIT 1-4 will provide the type of errors encountered, if any.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both the transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate any FIFO data errors.

IER BIT-0:
This interrupt will be issued when the FIFO has reached the programmed trigger level or is cleared when the FIFO drops below the trigger level in the FIFO mode of operation.
Logic 0 = Disable the receiver ready interrupt. (normal

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default condition)
Logic 1 = Enable the receiver ready interrupt.

IER BIT-1:
This interrupt will be issued whenever the THR is empty and is associated with bit-1 in the LSR register.
Logic 0 = Disable the transmitter empty interrupt. (normal default condition)
Logic 1 = Enable the transmitter empty interrupt.
IER BIT-2:
This interrupt will be issued whenever a fully assembled receive character is transferred from the RSR to the RHR/FIFO, i.e., data ready, LSR bit-0.
Logic 0 = Disable the receiver line status interrupt. (normal default condition)
Logic 1 = Enable the receiver line status interrupt.

IER BIT-3:
Logic 0 = Disable the modem status register interrupt. (normal default condition)
Logic 1 = Enable the modem status register interrupt.

IER BIT 4-7:
Not used - Initialized to a logic 0.

FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

DMA MODE
Mode 0 Set and enable the interrupt for each single transmit or receive operation, and is similar to the ST16C454 mode. Transmit Ready (-TXRDY) will go to a logic 0 when ever an empty transmit space is available in the Transmit Holding Register (THR). Receive Ready (-RXRDY) will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character.
Mode 1 Set and enable the interrupt in a block mode operation. The transmit interrupt is set when the transmit FIFO is below the programmed trigger level. -TXRDY remains a logic 0 as long as one empty FIFO location is available. The receive interrupt is set when the receive FIFO fills to the programmed trigger level. However the FIFO continues to fill regardless of the programmed level until the FIFO is full. -RXRDY remains a logic 0 as long as the FIFO fill level is above the programmed trigger level.

FCR BIT-0:
Logic 0 = Disable the transmit and receive FIFO. (normal default condition)
Logic 1 = Enable the transmit and receive FIFO. This bit must be a "1" when other FCR bits are written to or they will not be programmed.

FCR BIT-1:
Logic 0 = No FIFO receive reset. (normal default condition)
Logic 1 = Clears the contents of the receive FIFO and resets the FIFO counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

FCR BIT-2:
Logic 0 = No FIFO transmit reset. (normal default condition)
Logic 1 = Clears the contents of the transmit FIFO and resets the FIFO counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

FCR BIT-3:
Logic 0 = Set DMA mode "0". (normal default condition)
Logic 1 = Set DMA mode "1."

Transmit operation in mode "0":
When the 554D is in the ST16C450 mode (FIFOs disabled, FCR bit-0 = logic 0) or in the FIFO mode (FIFOs enabled, FCR bit-0 = logic 1, FCR bit-3 = logic 0) and when there are no characters in the transmit FIFO or transmit holding register, the -TXRDY pin will be a logic 0. Once active the -TXRDY pin will go to a logic 1 after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When the 554D is in mode "0" (FCR bit-0 = logic 0) or in the FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 0) and there is at least one character in the receive FIFO, the -RXRDY pin will be a logic 0. Once active the -RXRDY pin will go to a logic 1 when there are no more characters in the receiver.

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Transmit operation in mode "1":
When the 554D is in FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 1), the -TXRDY pin will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 if one or more FIFO locations are empty.

Receive operation in mode "1":
When the 554D is in FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 1) and the trigger level has been reached, or a Receive Time Out has occurred, the -RXRDY pin will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO.

FCR BIT 4-5:
Not used - Initialized to a logic 0.

FCR BIT 6-7: (logic 0 or cleared is the default condition, Rx trigger level = 1)
These bits are used to set the trigger level for the receive FIFO interrupt.

An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However the FIFO will continue to be loaded until it is full.

BIT-7	BIT-6	RX FIFO trigger level
0	0	1
0	1	4
1	0	8
1	1	14

Interrupt Status Register (ISR)

The 554D provides four levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after rereading the interrupt status bits. The Interrupt Source Table 7 (below) shows the data values (bit 0-5) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels:

Table 7, INTERRUPT SOURCE TABLE

Priority Level	[ISR BITS] Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	Source of the interrupt
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY (Received Data Ready)
2	0	0	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	0	0	MSR (Modem Status Register)

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ISR BIT-0:
Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
Logic 1 = No interrupt pending. (normal default condition)

ISR BIT 1-3: (logic 0 or cleared is the default condition)
These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (See Interrupt Source Table).

ISR BIT 4-5:
Not used - Initialized to a logic 0.

ISR BIT 6-7: (logic 0 or cleared is the default condition)
These bits are set to a logic 0 when the FIFO is not being used. They are set to a logic 1 when the FIFOs are enabled.

Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR BIT 0-1: (logic 0 or cleared is the default condition)
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2: (logic 0 or cleared is the default condition)
The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	Word length	Stop bit length (Bit time(s))
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
Logic 0 = No parity. (normal default condition)
Logic 1 = A parity bit is generated during the transmission, receiver checks the data and parity for transmission errors.

LCR BIT-4:
If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.
Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted data. The receiver must be programmed to check the same format. (normal default condition)
Logic 1 = EVEN Parity is generated by forcing an even the number of logic 1's in the transmitted. The receiver must be programmed to check the same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = logic 0, parity is not forced. (normal default condition)
LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

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LCR Bit-5	LCR Bit-4	LCR Bit-3	Parity selection
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity “1”
1	1	1	Forced parity “0”

LCR BIT-6:
When enabled the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR bit-6 to a logic 0.
Logic 0 = No TX break condition. (normal default condition)
Logic 1 = Forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition.

LCR BIT-7:
Not used - Initialized to a logic 0.

Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

MCR BIT-0:
Logic 0 = Force -DTR output to a logic 1. (normal default condition)
Logic 1 = Force -DTR output to a logic 0.

MCR BIT-1:
Logic 0 = Force -RTS output to a logic 1. (normal default condition)
Logic 1 = Force -RTS output to a logic 0.

MCR BIT-2:
This bit is used in the Loopback mode only. In the loopback mode this bit is use to write the state of the modem -RI interface signal via -OP1.

*MCR BIT-3: (*Used to control the modem -CD signal in the loopback mode.)
Logic 0 = Forces INT (A-D) outputs to the three state mode during the 16 mode. (normal default condition) In the Loopback mode, sets -OP2 (-CD) internally to a logic 1.
Logic 1 = Forces the INT (A-D) outputs to the active mode during the 16 mode. In the Loopback mode, sets -OP2 (-CD) internally to a logic 0.

MCR BIT-4:
Logic 0 = Disable loopback mode. (normal default condition)
Logic 1 = Enable local loopback mode (diagnostics).

MCR BIT 5-7:
Not used - Initialized to a logic 0.

Line Status Register (LSR)

This register provides the status of data transfers between. the 554D and the CPU.

LSR BIT-0:
Logic 0 = No data in receive holding register or FIFO. (normal default condition)
Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR BIT-1:
Logic 0 = No overrun error. (normal default condition)
Logic 1 = Overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transfered into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR BIT-2:
Logic 0 = No parity error. (normal default condition)
Logic 1 = Parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.

LSR BIT-3:
Logic 0 = No framing error. (normal default condition)
Logic 1 = Framing error. The receive character did not

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have a valid stop bit(s). In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
Logic 0 = No break condition. (normal default condition)
Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.

LSR BIT-5:
This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.

LSR BIT-6:
This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmit FIFO and transmit shift register are both empty.

LSR BIT-7:
Logic 0 = No Error. (normal default condition)
Logic 1 = At least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when LSR register is read.

Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device that the 554D is connected to. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

MSR BIT-0:
Logic 0 = No -CTS Change (normal default condition)
Logic 1 = The -CTS input to the 554D has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-1:
Logic 0 = No -DSR Change. (normal default condition)
Logic 1 = The -DSR input to the 554D has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-2:
Logic 0 = No -RI Change. (normal default condition)
Logic 1 = The -RI input to the 554D has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.

MSR BIT-3:
Logic 0 = No -CD Change. (normal default condition)
Logic 1 = Indicates that the -CD input to the has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-4:
-CTS (active high, logical 1). Normally MSR bit-4 bit is the compliment of the -CTS input. However in the loopback mode, this bit is equivalent to the RTS bit in the MCR register.

MSR BIT-5:
DSR (active high, logical 1). Normally this bit is the compliment of the -DSR input. In the loopback mode, this bit is equivalent to the DTR bit in the MCR register.

MSR BIT-6:
RI (active high, logical 1). Normally this bit is the compliment of the -RI input. In the loopback mode this bit is equivalent to the OP1 bit in the MCR register.

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MSR BIT-7:
CD (active high, logical 1). Normally this bit is the compliment of the -CD input. In the loopback mode this bit is equivalent to the OP2 bit in the MCR register.

Scratchpad Register (SPR)

The ST16C554D provides a temporary data register to store 8 bits of user information.

ST16C554D EXTERNAL RESET CONDITIONS

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7= input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE
TX A-D	High
-RTS A-D	High
-DTR A-D	High
-RXRDY	High
-TXRDY	Low

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