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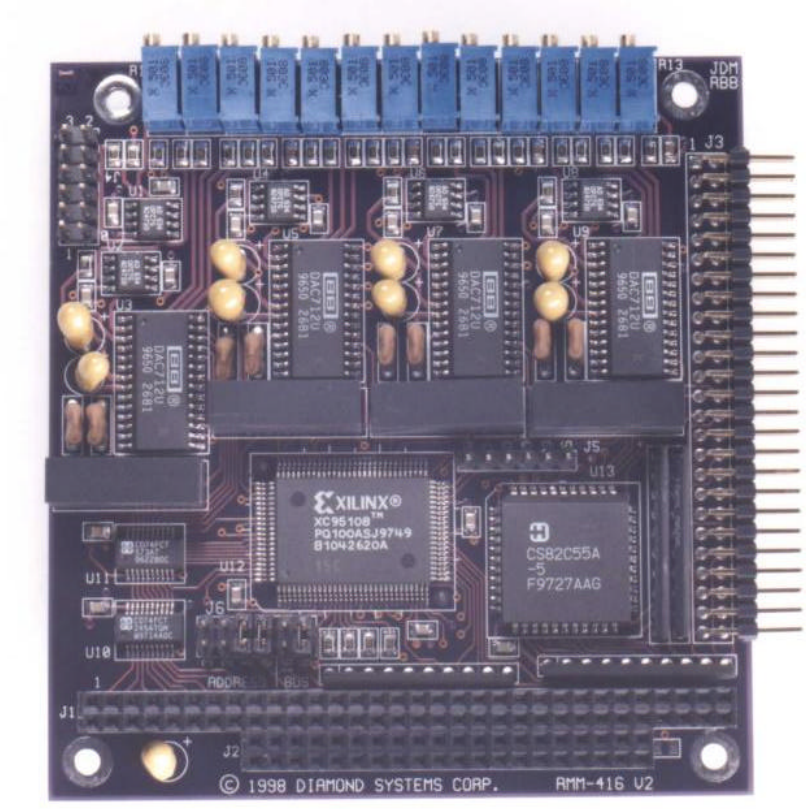
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DIAMOND SYSTEMS CORPORATION

RUBY-MM-416

PC/104 Format
16-Bit Analog Output Module

User Manual V1.1



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1. DESCRIPTION

Ruby-MM-416 is a PC/104-format data acquisition board that provides analog outputs and digital I/O for process control and other applications. Below is a summary of key features:

Analog Outputs

Ruby-MM-416 has 4 analog voltage outputs with 16-bit resolution (1 part in 65536).

⇒ **Note:** Analog output, D/A, and DAC are all used interchangeably in this manual.

Multiple Full-Scale Output Ranges

Three different preset ranges are jumper selectable: 0 - 10V unipolar, ±5V, ±10V bipolar

Simultaneous Update

Analog outputs are updated simultaneously. This prevents time skew errors which can result from updating outputs sequentially on a system which requires two or more control signals to change simultaneously.

External Trigger

An external trigger signal can be connected to the board to update the analog outputs in synchronization to an external event.

Digital I/O

An 82C55 chip is included to provide 24 lines of digital I/O. Each line is CMOS / TTL compatible and can supply up to ±6mA of current.

+5V Operation

Ruby-MM-416 requires only +5VDC from the system power supply for operation. It generates its own ±15V supplies for the analog circuitry on board using miniature DC/DC converters.

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2. I/O HEADER PINOUT

Ruby-MM-416 provides a 50-pin right-angle header labeled J3 for all user I/O. This header is located on the right side of the board. Pins 1, 2, 49, and 50 are marked to aid in proper orientation. A standard 50-pin cable-mount IDC (insulation displacement contact) connector will mate with this header.

J3
(Top of board)

Agnd	1	2	Vout 0
Agnd	3	4	Vout 1
Agnd	5	6	Vout 2
Agnd	7	8	Vout 3
NC	9	10	NC
NC	11	12	NC
NC	13	14	NC
NC	15	16	NC
NC	17	18	NC
Agnd	19	20	+15V
-15V	21	22	Agnd
Dgnd	23	24	External Trigger
A7	25	26	A6
A5	27	28	A4
A3	29	30	A2
A1	31	32	A0
C7	33	34	C6
C5	35	36	C4
C3	37	38	C2
C1	39	40	C0
B7	41	42	B6
B5	43	44	B4
B3	45	46	B2
B1	47	48	B0
+5V	49	50	Dgnd

Signal Name	Definition
Vout0-3	Analog output channels
Agnd	Analog ground reference for analog outputs
Dgnd	Digital ground from PC/104 bus
A7-A0	Digital I/O port A
B7-B0	Digital I/O port B
C7-C0	Digital I/O port C
External Trigger	Input for external control of D/A updating and hardware interrupts
±15V	Analog power supply; maximum current draw 5mA per line
+5V	Connected to PC/104 bus power supply
NC	Not connected

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3. BOARD CONFIGURATION

Refer to the Drawing of Ruby-MM-416 on Page 7.

J6: Base Address

Each board in the system must have a different base address. Ruby-MM-416's base address is set with jumpers in the four leftmost positions of header **J6**, located in the lower section of the board near the PC/104 bus header. These four positions are labeled **3 2 1 0**.

Each of these four locations corresponds to a different address bit in the base address; locations 3 - 0 correspond to address bits 9 - 6, respectively. A location where the jumper is out is equal to a 1 for the corresponding address bit, and a location where the jumper is in is equal to a 0. All address bits not selected (bits 5 - 0) are 0 for the base address. Thus 16 different addresses can be selected. The table below lists the 12 valid base address settings for Ruby-MM-416 (addresses below 100 Hex are reserved for system functions). The default setting is 300 Hex.

Base Address		**Header J6 Position**			
Hex	**Decimal**	**3**	**2**	**1**	**0**
100	256	In	Out	In	In
140	320	In	Out	In	Out
180	384	In	Out	Out	In
1C0	448	In	Out	Out	Out
200	512	Out	In	In	In
240	576	Out	In	In	Out
280	640	Out	In	Out	In
2C0	704	Out	In	Out	Out
300	768 (Default)	Out	Out	In	In
340	832	Out	Out	In	Out
380	896	Out	Out	Out	In
3C0	960	Out	Out	Out	Out

J6: 8-Bit or 16-Bit Bus Interface

Ruby-MM-416 can operate in either 8-bit or 16-bit bus modes. To operate in 16-bit bus modes, the board must be installed in a 16-bit PC/104 bus system (both 64-pin header J1 and 40-pin header J2 are present on the CPU), and a jumper must be installed in the location marked **16** on header J6. 16-bit mode is only active for addresses Base + 0 through Base + 7, which are the addresses used for the DACs. For addresses Base + 8 through Base + 15, the board always operates in 8-bit mode.

The board will operate in 8-bit mode in either 8-bit or 16-bit systems. To force the board into 8-bit mode, remove the jumper from the location marked 16 in J6 (the location marked **8** is just a storage location for the jumper). The board will automatically operate in 8-bit mode whenever it is not installed in a 16-bit system, since it detects the type of bus by detecting the presence or absence of +5V on header J2.

The I/O map is different for 8-bit and 16-bit modes. See page 8 for I/O map information.

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J4: Analog Output Range Configuration

Header **J4** in the upper left corner of the board is used to configure the analog output ranges. Each channel can be independently configured for 0-10V, ±5V, or ±10V range. Each channel uses one of the four quadrants of three pins on this header (the quadrants are marked 3 and 2 at the top of the header and 1 and 0 at the bottom).

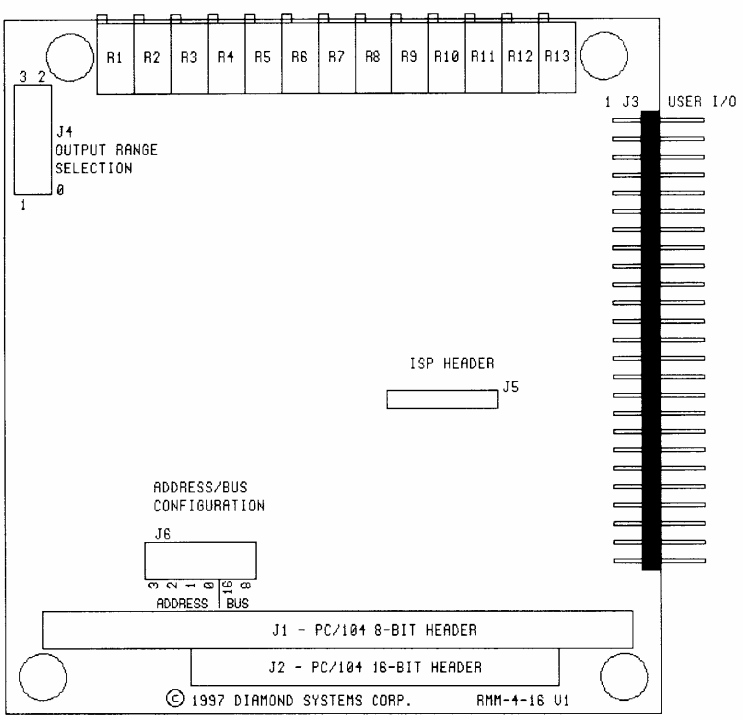
- To set a channel to ±10V output range, do not install a jumper in that channel's quadrant.
- To set a channel for ±5V output range, install a jumper over the two upper pins of that channel's quadrant.
- To set a channel for 0-10V output range, install a jumper over the two lower pins of that channel's quadrant.

J5: ISP Header

Header **J5** is used in manufacturing to program the in-system programmable logic device in location U12. This header serves no function in normal board operation.

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4. RUBY-MM-416 BOARD DRAWING



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5. I/O MAP

Ruby-MM-416 occupies 16 consecutive 8-bit locations in I/O space. For example, the default base address is 300 Hex (768 Decimal); in this case the board occupies addresses 300 - 30F (768 - 783).

The board's I/O map depends on whether it is in 8-bit mode or 16-bit mode.

I/O Map for 8-Bit Mode

Base +	Write Function	Read Function
0	Channel 0 LSB	Update all channels
1	Channel 0 MSB	Update all channels
2	Channel 1 LSB	Update all channels
3	Channel 1 MSB	Update all channels
4	Channel 2 LSB	Update all channels
5	Channel 2 MSB	Update all channels
6	Channel 3 LSB	Update all channels
7	Channel 3 MSB	Update all channels
8	Reset board	N/A
9	Enable external trigger	N/A
10	N/A	N/A
11	N/A	N/A
12	Digital I/O port A data	Digital I/O port A data
13	Digital I/O port B data	Digital I/O port B data
14	Digital I/O port C data	Digital I/O port C data
15	Digital I/O control register	Digital I/O control register

I/O Map for 16-Bit Mode

Base +	Write Function	Read Function
0	Channel 0 data	Update all channels
2	Channel 1 data	Update all channels
4	Channel 2 data	Update all channels
6	Channel 3 data	Update all channels
8	Reset board	N/A
9	Enable external trigger	N/A
10	N/A	N/A
11	N/A	N/A
12	Digital I/O port A data	Digital I/O port A data
13	Digital I/O port B data	Digital I/O port B data
14	Digital I/O port C data	Digital I/O port C data
15	Digital I/O control register	Digital I/O control register

Note that in 16-bit mode, a single write operation to an even address writes all 16-bit data to a DAC, whereas in 8-bit mode two 8-bit writes are required. Note also that regardless of the board's selected mode, it always operates in 8-bit mode during access to addresses Base + 8 through Base + 15.

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Reset information:

A system hardware reset or a write to base + 8 will reset the board. During a reset, the following occurs:

- All analog outputs are set to mid-scale (0V for ±5Vand ±10V ranges, 2.5V for 0-10V range).
- The external trigger is disabled.
- All digital I/O ports are set to input mode.

The next chapter describes all registers on the board. You should familiarize yourself with these registers in order to get a complete understanding of the board's operation.

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6. REGISTER DEFINITIONS

8-Bit Mode

Base + 0, 2, 4, 6 **Write** **DAC LSB**

Bit No.	7	6	5	4	3	2	1	0
Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

DA7 - 0 D/A bits 7 - 0; DA0 is the least significant bit; data is a signed 16-bit value ranging from -32768 (negative full scale) to +32767 (positive full-scale).

⇒ **Note:** The LSB data is held in a separate 8-bit register and is not actually loaded into the DAC until the MSB is written (see below). There is only one LSB register on the board. Therefore, after writing the LSB for a channel, you must write the MSB for that channel prior to writing the LSB for another channel.

⇒ **Note:** The LSB **must** be written to the board **before** the MSB, since writing the MSB causes the contents of the LSB register to be loaded into the DAC along with the MSB.

Base + 1, 3, 5, 7 **Write** **DAC MSB**

Bit No.	7	6	5	4	3	2	1	0
Name	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8

DA15 - 8 D/A bits 15 - 8; DA15 is the most significant bit of the 16-bit value.

16-Bit Mode

Base + 0, 2, 4, 6 **Write** **DAC Data**

Bit No.	15	14	13	...	3	2	1	0
Name	DA15	DA14	DA13	...	DA3	DA2	DA1	DA0

DA15 - 0 D/A bits 15 - 0; DA15 is the most significant bit, and DA0 is the least significant bit. Data is a signed 16-bit value ranging from -32768 (negative full scale) to +32767 (positive full-scale).

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All Modes

Base + 8 **Write** **Board Reset**

This address does not contain a data register. It is simply used to reset the board. Any value written to this address will reset the board, causing the following to occur:

- All analog outputs are set to mid-scale (0V for bipolar ranges and 1/2 full-scale for unipolar ranges).
- The control register is set to 0, disabling all external trigger and interrupt functions.
- All digital I/O ports are set to input mode.

The same reset operation will occur during system reset.

Base + 9 **Write** **External Trigger Enable**

An external trigger can be used to update the board's DACs after data is written to them. Bit 0 of Base + 9 is used for this purpose.

Bit No.	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	EXTTRIG

X	Unused bits
EXTTRIG	External trigger enable: 0 = disable trigger, 1 = enable trigger
	Interrupt operations use the trigger source selected with TRIGSEL.

Base + 10, Base + 11 **N/A** **N/A**

These addresses are not used on Ruby-MM-416.

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Base+12 through Base+15 Read/Write 82C55 Digital I/O Chip Registers

These registers map directly to the 82C55 24-line digital I/O chip.

Base + n, Dir, Function	D7	D6	D5	D4	D3	D2	D1	D0
12, R/W, Port A	A7	A6	A5	A4	A3	A2	A1	A0
13, R/W, Port B	B7	B6	B5	B4	B3	B2	B1	B0
14, R/W, Port C	C7	C6	C5	C4	C3	C2	C1	C0
15, W, Config Register	1	ModeC	ModeA	DirA	DirCH	ModeB	DirB	DirCL

Configuration Register

The configuration register is programmed by writing to Base + 15 using the format below. Once you have set the port directions with this register, you can read and write to the ports as desired.

Bit No.	7	6	5	4	3	2	1	0
Name	1	ModeC	ModeA	DirA	DirCH	ModeB	DirB	DirCL

Definitions:

1	Bit 7 must be set to 1 to indicate port mode set operation.
DirA	Direction control for bits A7 – A0: 0 = output, 1 = input
DirB	Direction control for bits B7 – B0: 0 = output, 1 = input
DirCL	Direction control for bits C3 – C0: 0 = output, 1 = input
DirCH	Direction control for bits C7 – C4: 0 = output, 1 = input
ModeA, ModeB, ModeC	I/O Mode for each port, 0 or 1

Here is a list of common configuration register values (others are possible):

Configuration Byte

Hex	Decimal	Port A	Port B	Port C (both halves)	
9B	155	Input	Input	Input	(all ports input)
92	146	Input	Input	Output	
99	153	Input	Output	Input	
90	144	Input	Output	Output	
8B	139	Output	Input	Input	
82	130	Output	Input	Output	
89	137	Output	Output	Input	
80	128	Output	Output	Output	(all ports output)

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7. ANALOG OUTPUT RANGES AND FORMULAS

The DAC712 D/A chip used in Ruby-MM-416 is designed to operate with a fixed ±10V range and therefore operates in twos complement form. The other ranges are created in circuitry that follows the DAC output. This means that regardless of the selected output range, the data is always written in twos complement form, with -32768 corresponding to the bottom of the output range and +32767 corresponding to the top of the output range.

For any output range, the resolution is equal to the maximum possible range of output voltages divided by the maximum number of possible steps. For a 12-bit D/A converter, the maximum number of steps is 2^{16} = 65536 (the actual output codes range from 0 to 65535, which is the full range of possible 16-bit binary numbers). Thus the resolution is equal to 1/65536 times the full-scale range. This is the smallest possible change in the output and corresponds to a change of 1 in the output code. Because of this fact the resolution is often referred to as the value of **1 LSB**, or 1 least significant bit.

Twos Complement Coding

This method of coding includes the sign of the number in the most significant bit and ranges from $-(2^{n-1})$ to 2^{n-1} -1. A positive number always has a 0 in the MSB, and a negative number always has a 1 in the MSB. For 16-bit data, the most positive number is 32767, which corresponds to 0111 1111 1111 1111 in binary notation, and the most negative number is -32768, which corresponds to 1000 0000 0000 0000.

Decimal number	Binary number
-32768	1000 0000 0000 0000
-32767	1000 0000 0000 0001
-32766	1000 0000 0000 0010
...	...
-2	1111 1111 1111 1110
-1	1111 1111 1111 1111
0	0000 0000 0000 0000
1	0000 0000 0000 0001
2	0000 0000 0000 0010
...	...
32766	0111 1111 1111 1110
32767	0111 1111 1111 1111

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Formulas for ±5V Range

The formula for converting a given 16-bit twos complement value to its equivalent output voltage is:

Output Voltage = (Output Code / 32768) x 5V

Example: Output code = 12625
Output voltage = (12625 / 32768) x 5V = .38528 x 5V = **1.9264V**

Example: Output code = -25250
Output voltage = (-25250 / 32768) x 5V = -.77057 x 5V = **-3.8528V**

Conversely, the output code for a desired output voltage is given by:

Output Code = (Output Voltage / 5V) x 323768

Example: Desired output voltage = 2.3456V
Output Code = (2.3456 / 5V) x 32768 = **15372**

Example: Desired output voltage = -4.6912V
Output Code = (-4.6912 / 5V) x 32768 = **-30744**

Formulas for ±10V Range

The formulas for ±10V range are the same as for ±5V range, except the scale factor is changed to 10V:

Output Voltage = (Output Code / 32768) x 10V

Output Code = (Output Voltage / 10V) x 323768

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Formulas for 0-10V Range

The formulas for the unipolar 0-10V range are slightly more complicated, since an offset must be included to take into account the fact that the DAC is expecting negative numbers for the lower half of its output range. The formula for converting a given 16-bit twos complement value to its equivalent output voltage becomes:

Output Voltage = (Output Code / 32768) x 5V + 5V

Example: Output code = 12625

Output voltage = (12625 / 32768) x 5V + 5V = .38528 x 5V +5V = **6.9264V**

Example: Output code = -32768 (negative full-scale)

Output voltage = (-32768 / 32768) x 5V + 5V = -1 x 5V + 5V = **0V**

Example: Output code = 0 (mid-scale)

Output voltage = (0 / 32768) x 5V + 5V = 0 x 5V + 5V = **5V**

Here is a brief overview of the relationship between output code and output voltage (all voltages shown are theoretical; the actual value will vary slightly within ±1 LSB).

Output Code	±5V Range	±10V Range	0-10V Range
-32768	-5V	-10V	0V
-32767	-4.99985V	-9.9997V	0.00015V
-32766	-4.9997V	-9.9994V	0.0003V
-1	-0.00015V	-0.0003V	4.9998V
0	0V	0V	5V
1	0.00015V	0.0003V	5.00015V
32766	4.9997V	9.9994V	9.9997V
32767	4.99985V	9.9997V	9.99985V

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8. HOW TO GENERATE AN ANALOG OUTPUT

This chapter describes how to generate an analog output on Ruby-MM-416. Refer to the I/O maps on page 8 and the register descriptions starting on page 10 for information on the registers described here.

To generate an analog output on a single channel in 8-bit mode:

1. Write the LSB (least significant byte) to the corresponding address for the channel
2. Write the MSB (most significant byte) to the corresponding address for the channel
3. Perform an update command (read from any address from base + 0 through base + 7)

To generate analog outputs on several channels at once in 8-bit mode:

To write to several channels at once, the update can be performed just once at the end:

1. Write the LSB (least significant byte) for the first channel to the board
2. Write the MSB (most significant byte) for the first channel to the board
3. Write the LSB (least significant byte) for the second channel to the board
4. Write the MSB (most significant byte) for the second channel to the board
5. Perform an update command

To calculate the LSB, use the following formula:

LSB = Data AND 255

This strips off the high 8 bits and keeps only the low 8 bits.

To calculate the MSB, use the following formula:

MSB = (Data AND 65280) / 256

This strips off the low 8 bits, keeps only the high 8 bits, and shifts them into the low 8 bits for output to the board.

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Example:

Assume channel 0 is configured for ±5V. To set channel 0 to 3V, do the following:

D/A code is 3V / 5V x 32768 = 19661 (value is rounded to nearest integer)

LSB = 19661 AND 255 = 205

MSB = (19661 AND 65280) / 256 = 76

Step 1. Write **205** to base + 0 (LSB register for channel 0).

Step 2. Write **76** to base + 1 (MSB register for channel 0). The value 19661 is written to DAC 0.

Step 3. Read from base + 0. DAC 0 now outputs 3.000V.

To generate an analog output on a single channel in 16-bit mode:

1. Write the data to the corresponding address for the channel
2. Perform an update command (read from any address from base + 0 through base + 7)

To generate analog outputs on several channels at once in 16-bit mode:

To write to several channels at once, the update can be performed just once at the end:

1. Write the first channel's data to the first channel's address
2. Write the second channel's data to the second channel's address
3. Perform an update command

Example:

Assume channel 0 is configured for ±5V. To set channel 0 to 3V, do the following:

D/A code is 3V / 5V x 32768 = 19661 (value is rounded to nearest integer)

Step 1. Write **19661** to base + 0. The value 19661 is written to DAC 0.

Step 2. Read from base + 0. DAC 0 now outputs 3.000V.

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9. DAC UPDATE WITH EXTERNAL TRIGGER

The DACs can be updated using an external hardware trigger connected to pin 24 ofthe I/O header as well as in software. This can be useful for applications where the time of the update needs to be synchronized to an external event.

To enable DAC updating via external trigger, use the control register at base + 9. A 1 in bit 0 enables external trigger updating, and a 0 disables it. DAC update occurs on the falling edge of the external trigger. If external triggering is enabled, the line must be driven high and low by the external circuitry. There is no pullup resistor on the board to drive the line inactive if it is left floating.

Note that if a software update command is issued to a channel, then hardware updating will not affect that channel again until new data is written to it. The same is true in reverse. Only one update command is effective for any data value written to the DAC; subsequent update commands have no effect on the DAC until new data is written to it.

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10. DIGITAL I/O OPERATION

Ruby-MM-416 contains an 82C55 chip for digital I/O. This chip provides 3 8-bit ports, called A, B, and C, for a total of 24 I/O lines. The chip contains four registers, 1 each for A, B, and C and 1 for control. These four registers are mapped to Ruby-MM-416's I/O map at base + 12 through base + 15. The 24 I/O lines are brought out to pins 25 - 48 on the user I/O header J3.

The I/O lines are standard CMOS logic with ±2.5mA output current capability. If more output current is required, use a buffer chip such as 74F244 or 74ACT244.

Each port's direction is determined through a control register. In normal "Mode 0" operation (the most common operating mode), ports A and B can be independently configured for input or output, and each half of port C can be independently configured for input or output. Output data is latched in the chip, but input data is not latched. When reading a port that is in input mode, the current logic levels of the port at the time of the read operation will be returned. To latch data into the port, you must use Modes 1 or Mode 2. In "Mode 1" and "Mode 2" operation, A and B are again configurable for input/output, but port C is reconfigured to provide control signals for transfer requests and data latching. A complete 82C55 datasheet is included at the end of this manual; please refer to it for programming details.

At power up, hardware reset, or board reset (write to base + 8), the 82C55 is set to all input and the data registers for ports A, B, and C are set to 0.

When a port is set to output mode, the contents of its output register are cleared to 0.

Here is a quick list of configuration bytes for some common Mode 0 I/O configurations:

Configuration Byte				
Hex	**Decimal**	**Port A**	**Port B**	**Port C (both halves)**
9B	155	Input	Input	Input
92	146	Input	Input	Output
99	153	Input	Output	Input
90	144	Input	Output	Output
8B	139	Output	Input	Input
82	130	Output	Input	Output
89	137	Output	Output	Input
80	128	Output	Output	Output

See page 12 for more detail on the 82C55 registers and operation, and see the datasheet at the back of this manual for a complete description of the chip.

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11. CALIBRATION

The following procedure can be used to calibrate Ruby-MM-416. A voltmeter with a minimum of 5 1/2 digits of precision is needed for accurate calibration. Refer to the board drawing on page 7 for location of the 13 potentiometers used for calibration.

Before beginning calibration, remove all jumpers from J4, the output range configuration header. All analog outputs should be open (no load).

1. Unipolar Offset Calibration

Connect the negative lead of the voltmeter to the upper right pin of J4, and connect the positive lead to the lower left pin. Adjust R1 until the meter reads 10.0000V.

2. Channel 0 Calibration

Connect the voltmeter's negative lead to pin 1 on J3 (the I/O header) and the positive lead to pin 2.

Write -32768 to channel 0 to set it to negative full scale. Adjust R2 until the meter reads -10.0000V.

Write 32767 to channel 0 to set it to positive full scale. Adjust R3 until the meter reads +9.9997V.

Install a jumper in the upper two pins of channel 0's quadrant of J4 (the lower right quadrant) to set the channel to ±5V. Adjust R4 until the meter reads 4.9998V.

3. Channel 1 Calibration

Connect the voltmeter's negative lead to pin 3 on J3, and connect the positive lead to pin 4.

Write -32768 to channel 1 to set it to negative full scale. Adjust R5 until the meter reads -10.0000V.

Write 32767 to channel 1 to set it to positive full scale. Adjust R6 until the meter reads +9.9997V.

Install a jumper in the upper two pins of channel 1's quadrant of J4 (the lower left quadrant) to set the channel to ±5V. Adjust R7 until the meter reads 4.9998V.

4. Channel 2 Calibration

Connect the voltmeter's negative lead to pin 5 on J3, and connect the positive lead to pin 6.

Write -32768 to channel 2 to set it to negative full scale. Adjust R8 until the meter reads -10.0000V.

Write 32767 to channel 2 to set it to positive full scale. Adjust R9 until the meter reads +9.9997V.

Install a jumper in the upper two pins of channel 2's quadrant of J4 (the upper right quadrant) to set the channel to ±5V. Adjust R10 until the meter reads 4.9998V.

5. Channel 3 Calibration

Connect the voltmeter's negative lead to pin 7 on J3, and connect the positive lead to pin 8.

Write -32768 to channel 3 to set it to negative full scale. Adjust R11 until the meter reads -10.0000V.

Write 32767 to channel 3 to set it to positive full scale. Adjust R12 until the meter reads +9.9997V.

Install a jumper in the upper two pins of channel 3's quadrant of J4 (the upper left quadrant) to set the channel to ±5V. Adjust R13 until the meter reads 4.9998V.

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12. SPECIFICATIONS

Analog Outputs

No. of outputs	4, voltage output
Resolution	16 bits (1 part in 65536)
Output ranges	0-10V, ±5V, ±10V, jumper selectable
Settling time	10 s max to ±.003%
Linearity error	±2LSB max
Differential nonlinearity	±2LSB max
Monotonicity	Guaranteed monotonic to 15 bits of resolution
Output current	±5mA max per channel
Minimum output load	2K for ±10V and 0-10V ranges, 1K for ±5V range
Update method	Simultaneous update
Reset	All DACs reset to mid-scale (0V for ±5V and ±10V ranges, 5V for 0-10V range)

Digital I/O

No. of lines	24
Compatibility	CMOS / TTL
Input voltage	Logic 0: -0.5V min, 0.8V max Logic 1: 2.0V min, 5.5V max
Output voltage	Logic 0: 0.0V min, 0.4V max Logic 1: 3.0V min, Vcc - 0.4V max
Output current	±2.5mA max per line
External trigger	TTL / CMOS compatible, active low edge
Reset	All digital I/O lines are set to input and all data registers are set to 0

Miscellaneous

Power supply (Vcc)	+5VDC ±10%
Current Requirement	500mA typical
Operating temperature	0 to 70^{o}C
Operating humidity	5 to 95% non-condensing
Size	3.55” x 3.775”

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82C55A

CMOS Programmable Peripheral Interface

June 1998

Features

- **Pin Compatible with NMOS 8255A**
- **24 Programmable I/O Pins**
- **Fully TTL Compatible**
- **High Speed, No "Wait State" Operation with 5MHz and 8MHz 80C86 and 80C88**
- **Direct Bit Set/Reset Capability**
- **Enhanced Control Word Read Capability**
- **L7 Process**
- **2.5mA Drive Capability on All I/O Ports**
- **Low Standby Power (ICCSB) 10μA**

Ordering Information

PART NUMBERS		PACKAGE	TEMPERATURE RANGE	PKG. NO.
5MHz	8MHz			
CP82C55A-5	CP82C55A	40 Ld PDIP	0^oC to 70^oC	E40.6
IP82C55A-5	IP82C55A		-40^oC to 85^oC	E40.6
CS82C55A-5	CS82C55A	44 Ld PLCC	0^oC to 70^oC	N44.65
IS82C55A-5	IS82C55A		-40^oC to 85^oC	N44.65
CD82C55A-5	CD82C55A	40 Ld CERDIP	0^oC to 70^oC	F40.6
ID82C55A-5	ID82C55A		-40^oC to 85^oC	F40.6
MD82C55A-5/B	MD82C55A/B		-55^oC to 125^oC	F40.6
8406601QA	8406602QA	SMD#		F40.6
MR82C55A-5/B	MR82C55A/B	44 Pad CLCC	-55^oC to 125^oC	J44.A
8406601XA	8406602XA	SMD#		J44.A

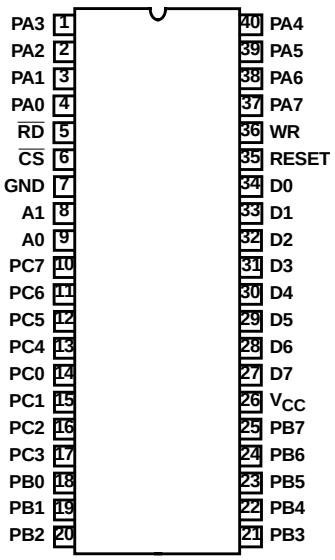
Description

The Intersil 82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance and industry standard configuration of the 82C55A make it compatible with the 80C86, 80C88 and other microprocessors.

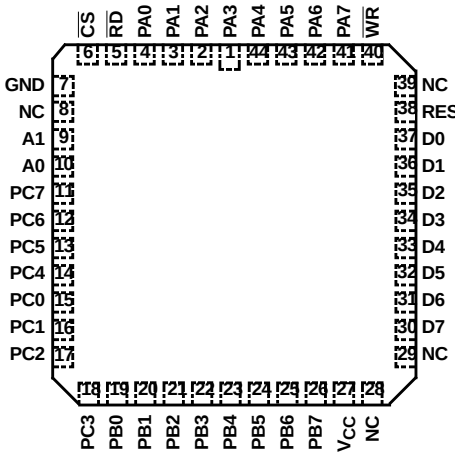
Static CMOS circuit design insures low operating power. TTL compatibility over the full military temperature range and bus hold circuitry eliminate the need for pull-up resistors. The Intersil advanced SAJI process results in performance equal to or greater than existing functionally equivalent products at a fraction of the power.

Pinouts

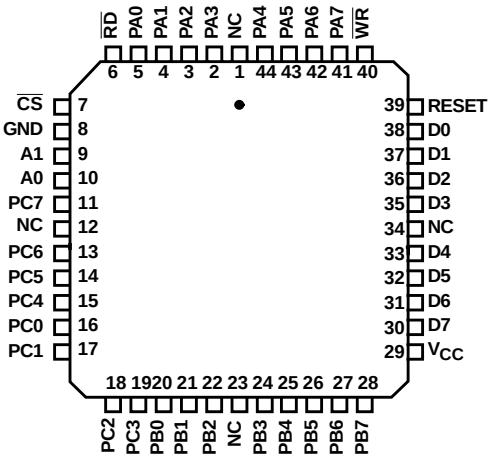
82C55A (DIP)
TOP VIEW



82C55A (CLCC)
TOP VIEW



82C55A (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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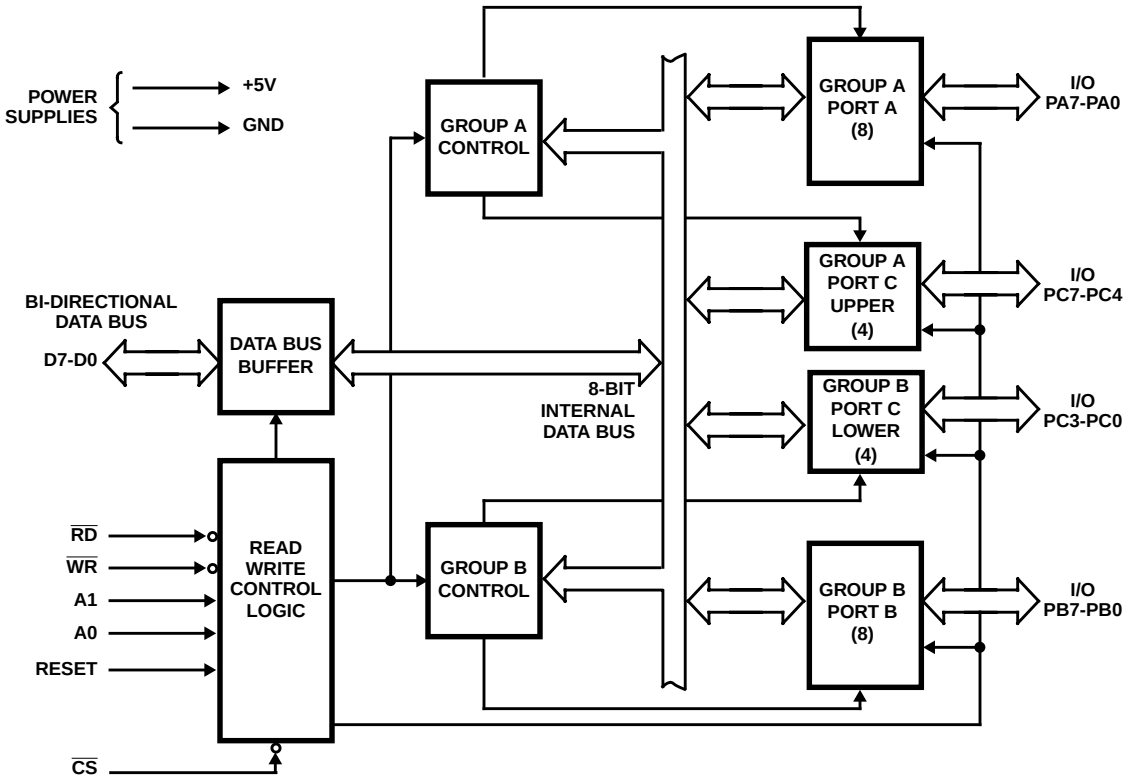
File Number **2969.2**

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Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	26		V_{CC}: The +5V power supply pin. A 0.1µF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7		GROUND
D0-D7	27-34	I/O	DATA BUS: The Data Bus lines are bidirectional three-state pins connected to the system data bus.
RESET	35	I	RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode with the “Bus Hold” circuitry turned on.
$\overline{CS}$	6	I	CHIP SELECT: Chip select is an active low input used to enable the 82C55A onto the Data Bus for CPU communications.
$\overline{RD}$	5	I	READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus.
$\overline{WR}$	36	I	WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A.
A0-A1	8, 9	I	ADDRESS: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word register. A0 and A1 are normally connected to the least significant bits of the Address Bus A0, A1.
PA0-PA7	1-4, 37-40	I/O	PORT A: 8-bit input and output port. Both bus hold high and bus hold low circuitry are present on this port.
PB0-PB7	18-25	I/O	PORT B: 8-bit input and output port. Bus hold high circuitry is present on this port.
PC0-PC7	10-17	I/O	PORT C: 8-bit input and output port. Bus hold circuitry is present on this port.

Functional Diagram



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Functional Description

Data Bus Buffer

This three-state bi-directional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

(CS) Chip Select. A “low” on this input pin enables the communcation between the 82C55A and the CPU.

(RD) Read. A “low” on this input pin enables 82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to “read from” the 82C55A.

(WR) Write. A “low” on this input pin enables the CPU to write data or control words into the 82C55A.

(A0 and A1) Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).

82C55A BASIC OPERATION

A1	A0	RD	WR	CS	INPUT OPERATION (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
1	1	0	1	0	Control Word → Data Bus
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					DISABLE FUNCTION
X	X	X	X	1	Data Bus → Three-State
X	X	1	1	0	Data Bus → Three-State

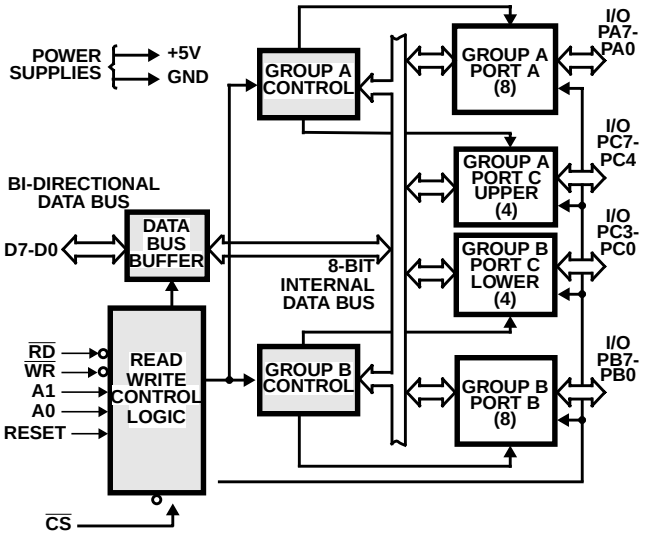


FIGURE 1. 82C55A BLOCK DIAGRAM. DATA BUS BUFFER, READ/WRITE, GROUP A & B CONTROL LOGIC FUNCTIONS

(RESET) Reset. A “high” on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode. “Bus hold” devices internal to the 82C55A will hold the I/O port inputs to a logic “1” state with a maximum hold current of 400µA.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU “outputs” a control word to the 82C55A. The control word contains information such as “mode”, “bit set”, “bit reset”, etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts “commands” from the Read/Write Control logic, receives “control words” from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7 - C4)

Control Group B - Port B and Port C lower (C3 - C0)

The control word register can be both written and read as shown in the “Basic Operation” table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic “1”, as this implies control word mode information.

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Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or “personality” to further enhance the power and flexibility of the 82C55A.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both “pull-up” and “pull-down” bus-hold devices are present on Port A. See Figure 2A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer. See Figure 2B.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with ports A and B. See Figure 2B.

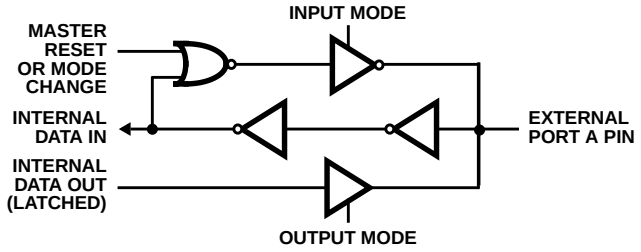


FIGURE 2A. PORT A BUS-HOLD CONFIGURATION

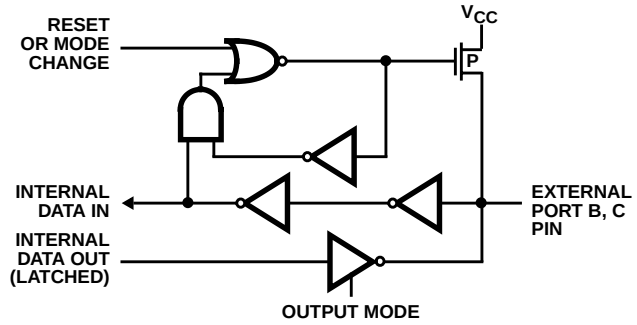


FIGURE 2B. PORT B AND C BUS-HOLD CONFIGURATION

FIGURE 2. BUS-HOLD CONFIGURATION

Operational Description

Mode Selection

There are three basic modes of operation than can be selected by the system software:

Mode 0 - Basic Input/Output
Mode 1 - Strobed Input/Output
Mode 2 - Bi-directional Bus

When the reset input goes “high”, all ports will be set to the input mode with all 24 port lines held at a logic “one” level by internal bus hold devices. After the reset is removed, the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need to pullup or pull-down resistors in all-CMOS designs. The control word register will contain 9Bh. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine. Any port programmed as an output port is initialized to all zeros when the control word is written.

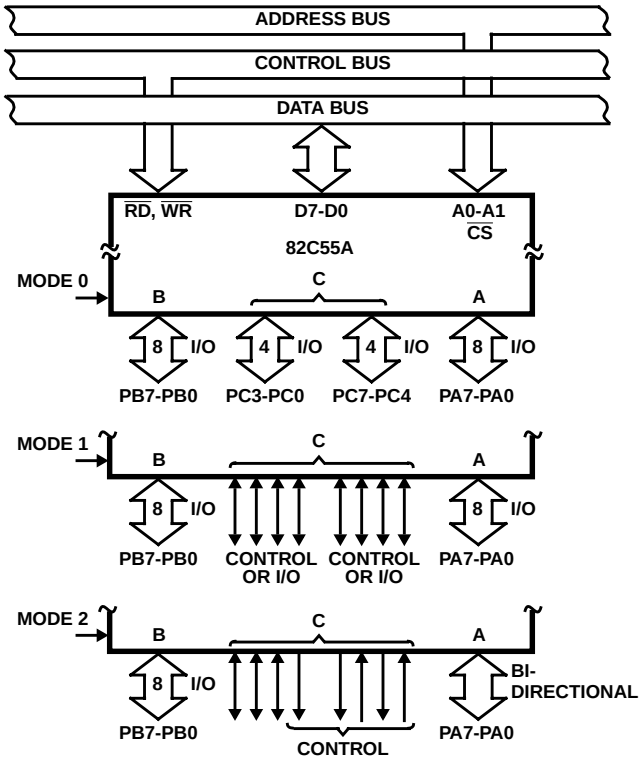


FIGURE 3. BASIC MODE DEFINITIONS AND BUS INTERFACE

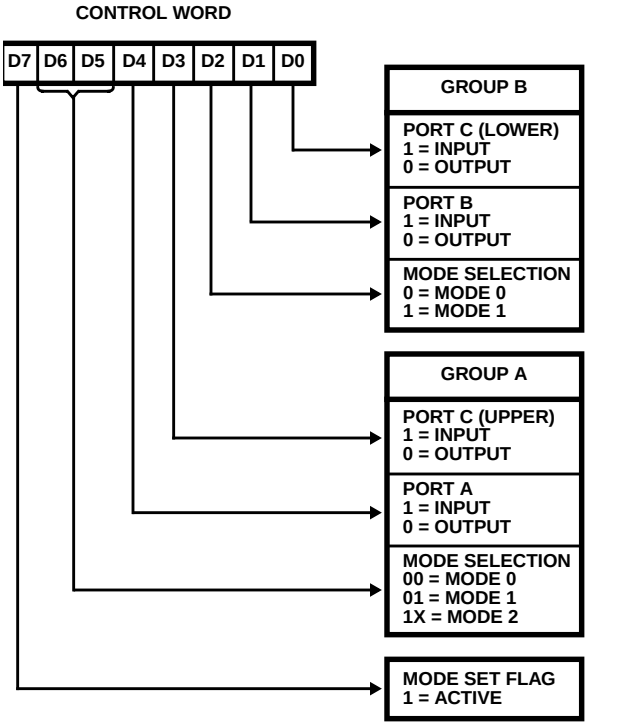


FIGURE 4. MODE DEFINITION FORMAT

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The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be “tailored” to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

The mode definitions and possible mode combinations may seem confusing at first, but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs. PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature (Figure 5)

Any of the eight bits of Port C can be Set or Reset using a single Output instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were output ports.

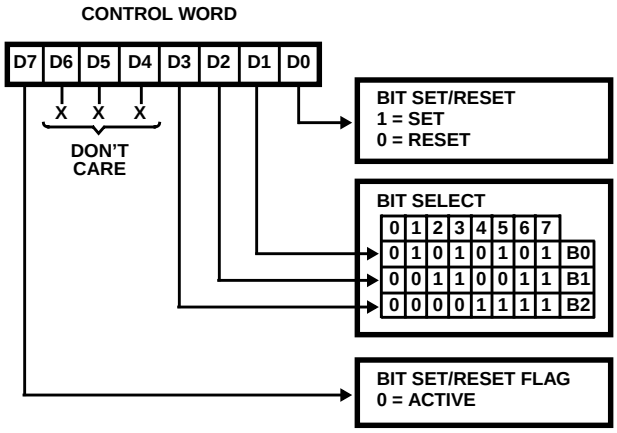


FIGURE 5. BIT SET/RESET FORMAT

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-Flop Definition

(BIT-SET)-INTE is SET - Interrupt Enable

(BIT-RESET)-INTE is Reset - Interrupt Disable

NOTE: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

Mode 0 Basic Functional Definitions:

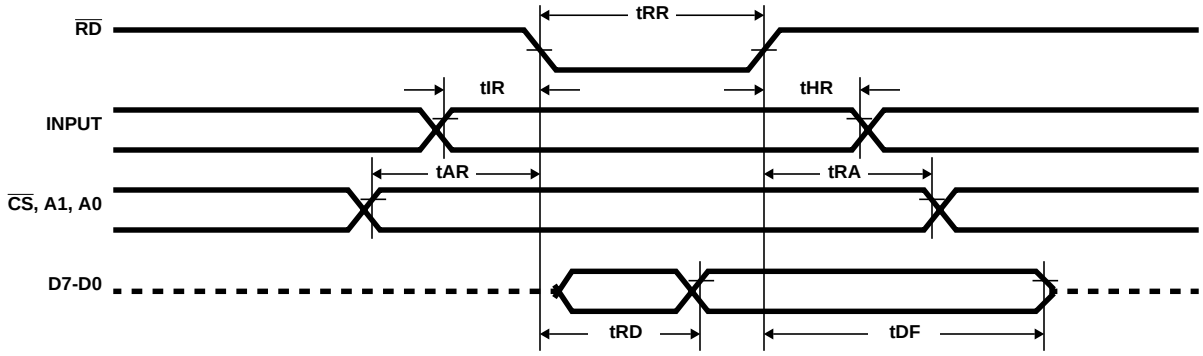
- Two 8-bit ports and two 4-bit ports
- Any Port can be input or output
- Outputs are latched
- Input are not latched
- 16 different Input/Output configurations possible

MODE 0 PORT DEFINITION

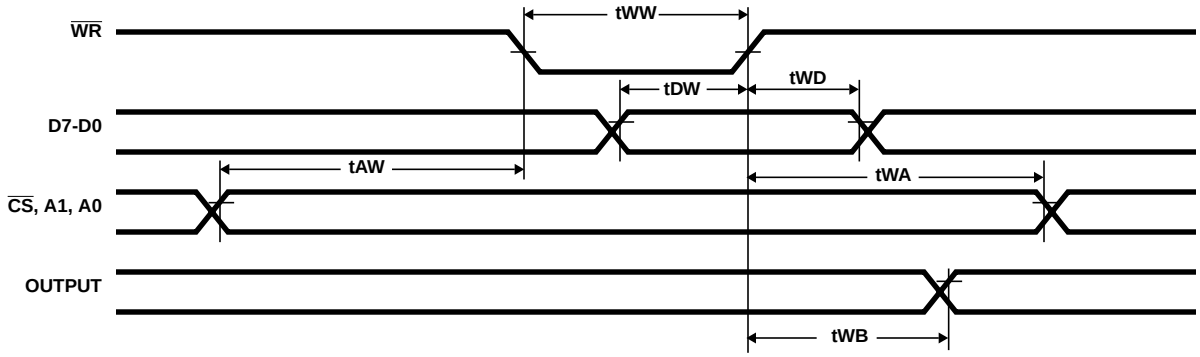
A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (Upper)	#	PORT B	PORT C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

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Mode 0 (Basic Input)



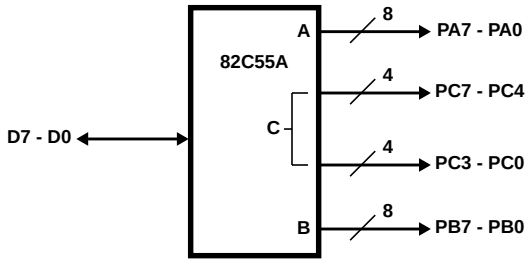
Mode 0 (Basic Output)



Mode 0 Configurations

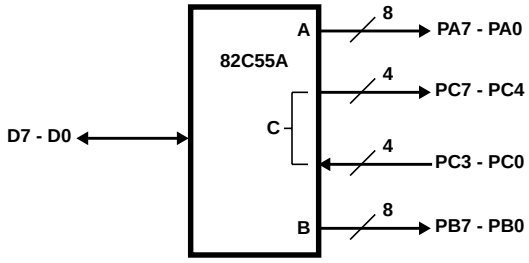
CONTROL WORD #0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0



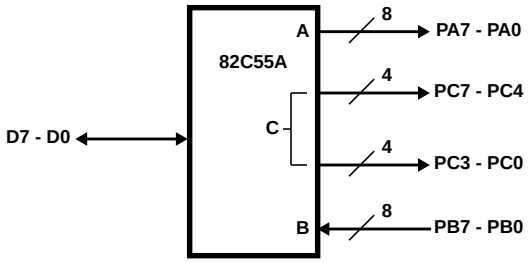
CONTROL WORD #1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	1



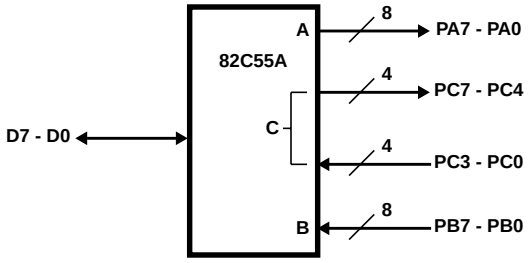
CONTROL WORD #2

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	0



CONTROL WORD #3

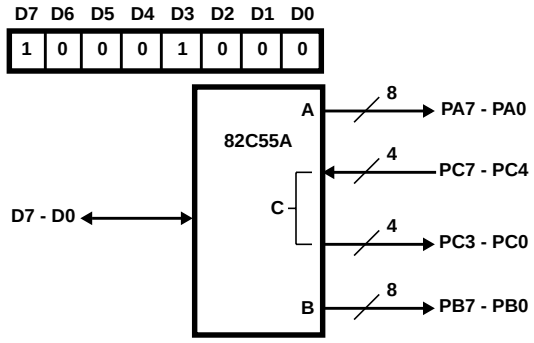
D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	1



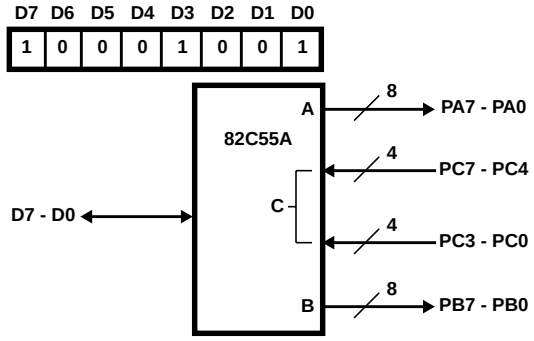
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Mode 0 Configurations (Continued)

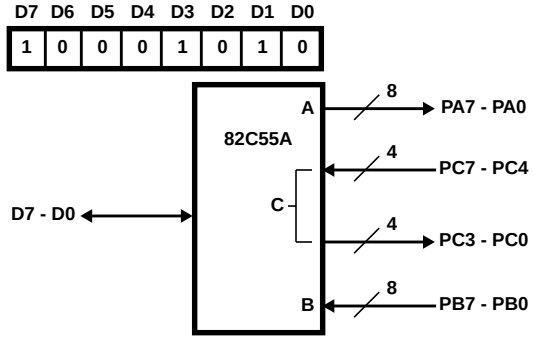
CONTROL WORD #4



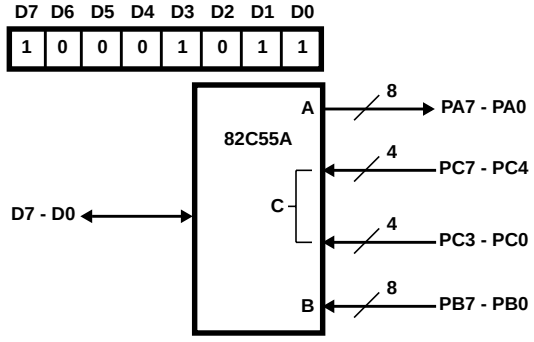
CONTROL WORD #5



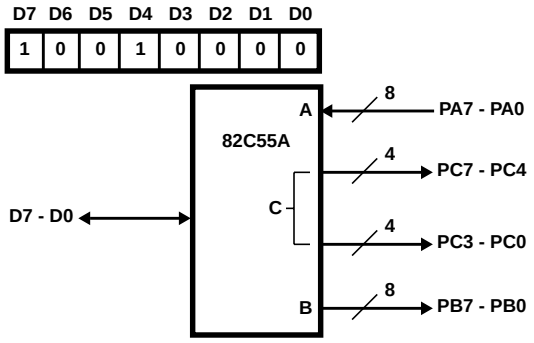
CONTROL WORD #6



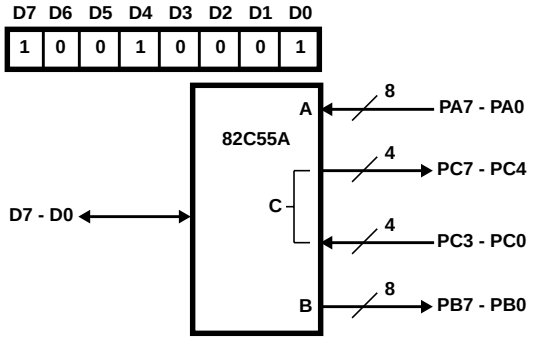
CONTROL WORD #7



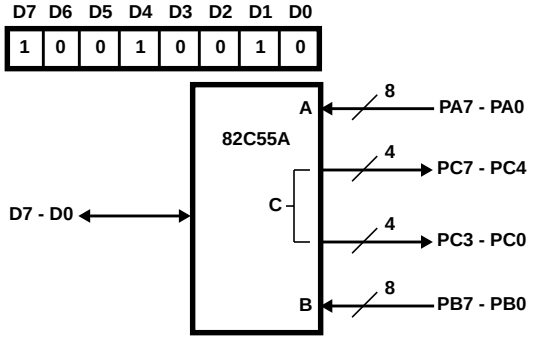
CONTROL WORD #8



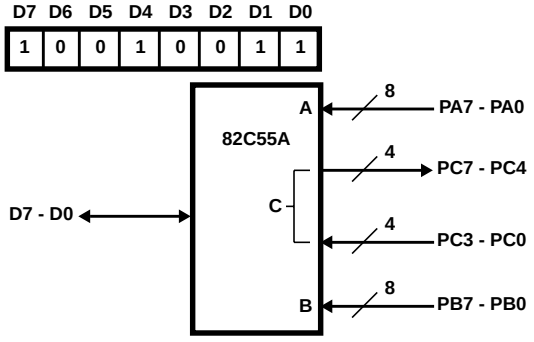
CONTROL WORD #9



CONTROL WORD #10



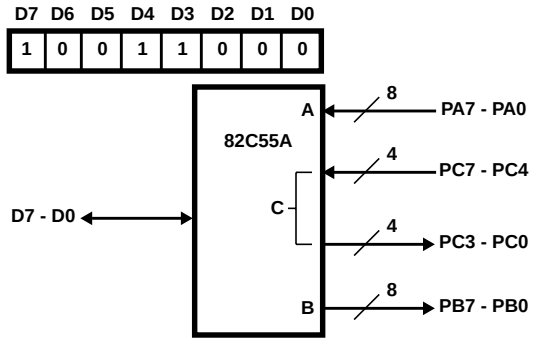
CONTROL WORD #11



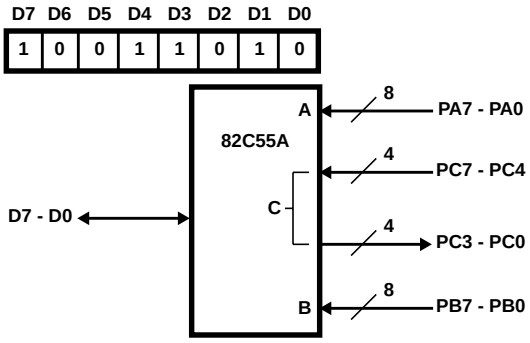
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Mode 0 Configurations (Continued)

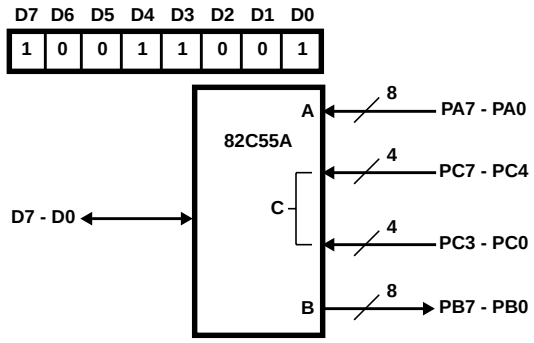
CONTROL WORD #12



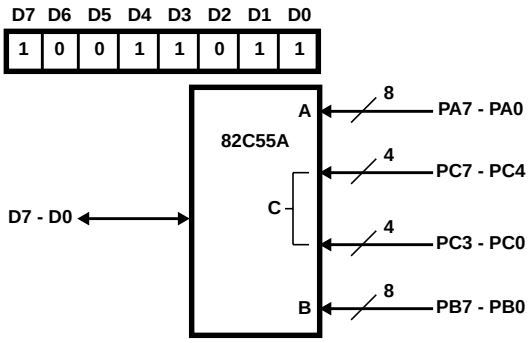
CONTROL WORD #14



CONTROL WORD #13



CONTROL WORD #15



Operating Modes

Mode 1 - (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or “hand shaking” signals. In mode 1, port A and port B use the lines on port C to generate or accept these “hand shaking” signals.

Mode 1 Basic Function Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

(Figures 6 and 7)

STB (Strobe Input)

A “low” on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A “high” on this output indicates that the data has been loaded into the input latch: in essence, and acknowledgment. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

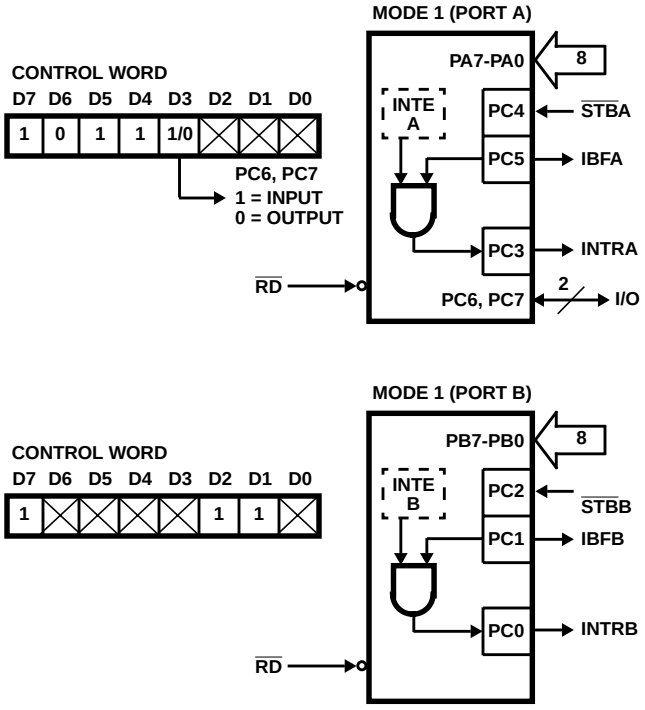


FIGURE 6. MODE 1 INPUT

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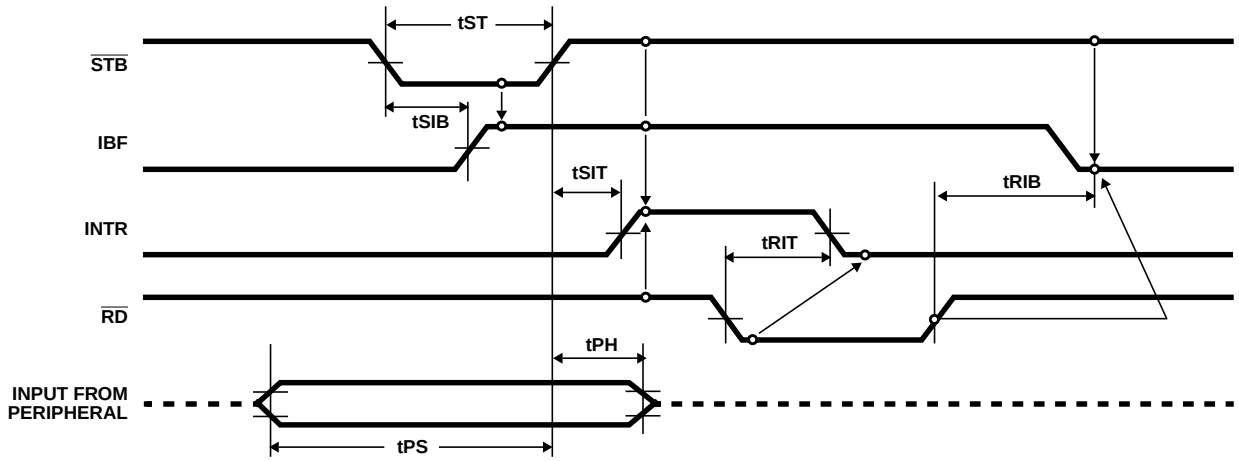


FIGURE 7. MODE 1 (STROBED INPUT)

INTR (Interrupt Request)

A “high” on this output can be used to interrupt the CPU when and input device is requesting service. INTR is set by the condition: $\overline{STB}$ is a “one”, IBF is a “one” and INTE is a “one”. It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC4.

INTE B

Controlled by bit set/reset of PC2.

Output Control Signal Definition

(Figure 8 and 9)

$\overline{OBF}$ - Output Buffer Full F/F). The $\overline{OBF}$ output will go “low” to indicate that the CPU has written data out to be specified port. This does not mean valid data is sent out of the part at this time since $\overline{OBF}$ can go true before data is available. Data is guaranteed valid at the rising edge of $\overline{OBF}$, (See Note 1). The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ - Acknowledge Input). A “low” on this input informs the 82C55A that the data from Port A or Port B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data, (See Note 1).

INTR - (Interrupt Request). A “high” on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a “one”, OBF is a “one” and INTE is a “one”. It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by Bit Set/Reset of PC6.

INTE B

Controlled by Bit Set/Reset of PC2.

NOTE:

1. To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send $\overline{OBF}$ to the peripheral device and then latch data into the peripheral device on the rising edge of $\overline{OBF}$.

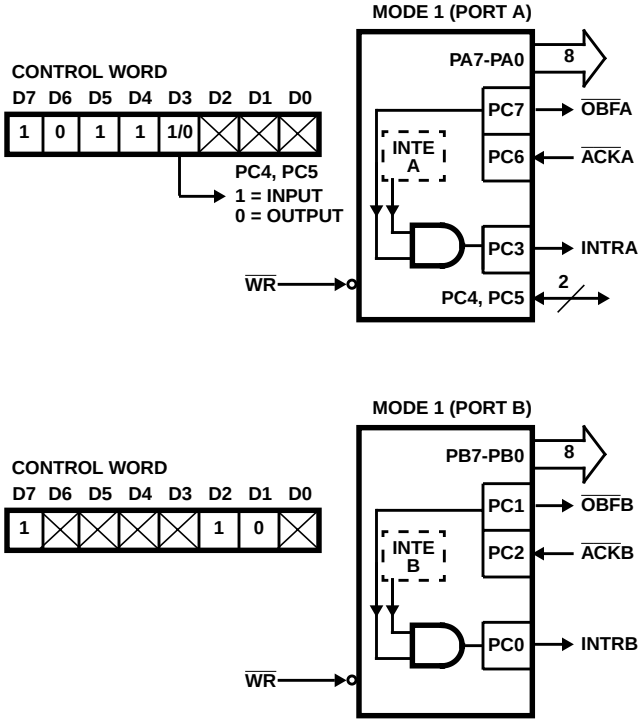


FIGURE 8. MODE 1 OUTPUT

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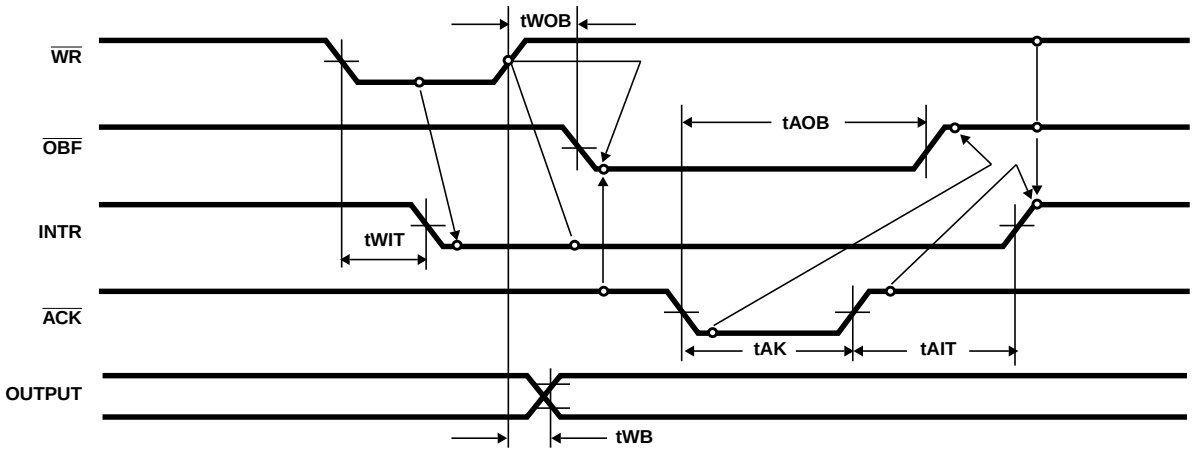
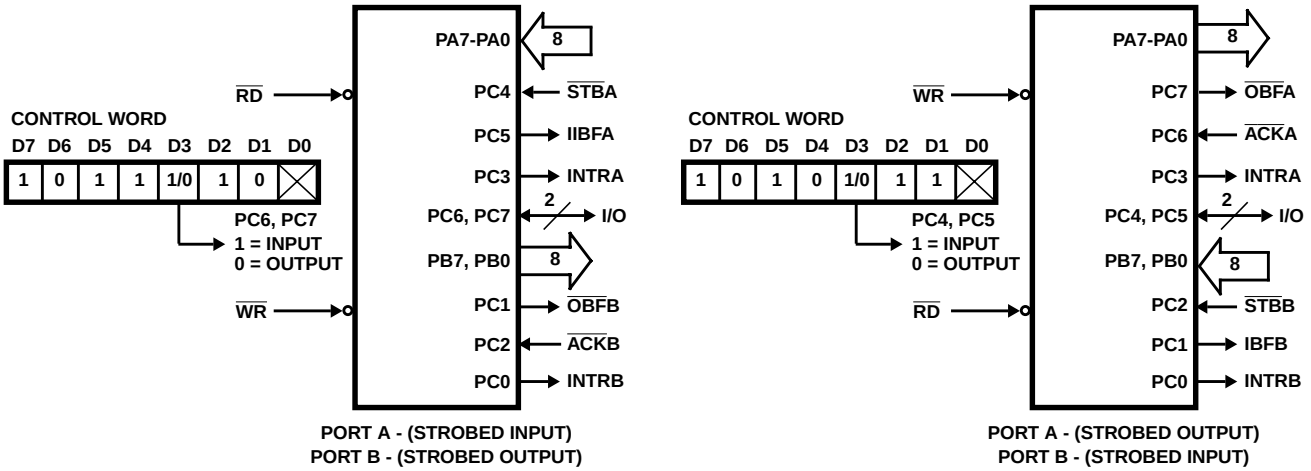


FIGURE 9. MODE 1 (STROBED OUTPUT)



Combinations of Mode 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

FIGURE 10. COMBINATIONS OF MODE 1

Operating Modes

Mode 2 (Strobed Bi-Directional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). “Hand shaking” signals are provided to maintain proper bus flow discipline similar to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C)
- Both inputs and outputs are latched
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A)

Bi-Directional Bus I/O Control Signal Definition

(Figures 11, 12, 13, 14)

INTR - (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{\text{OBF}}$ - (Output Buffer Full). The $\overline{\text{OBF}}$ output will go “low” to indicate that the CPU has written data out to port A.

$\overline{\text{ACK}}$ - (Acknowledge). A “low” on this input enables the three-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 - (The INTE flip-flop associated with $\overline{\text{OBF}}$). Controlled by bit set/reset of PC4.

Input Operations

$\overline{\text{STB}}$ - (Strobe Input). A “low” on this input loads data into the input latch.

IBF - (Input Buffer Full F/F). A “high” on this output indicates that data has been loaded into the input latch.

INTE 2 - (The INTE flip-flop associated with IBF). Controlled by bit set/reset of PC4.

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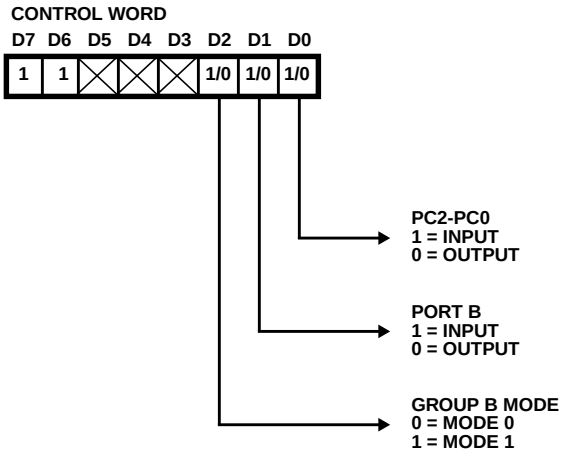


FIGURE 11. MODE CONTROL WORD

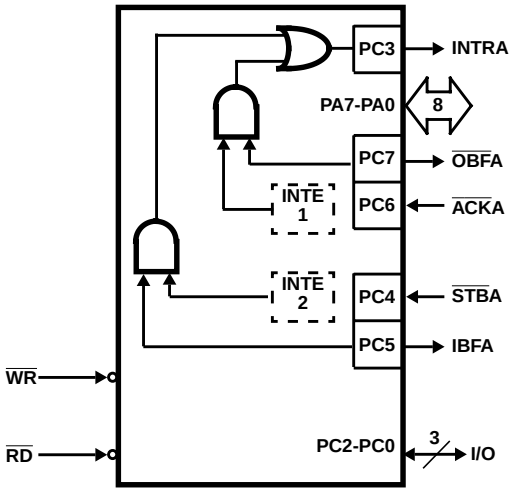
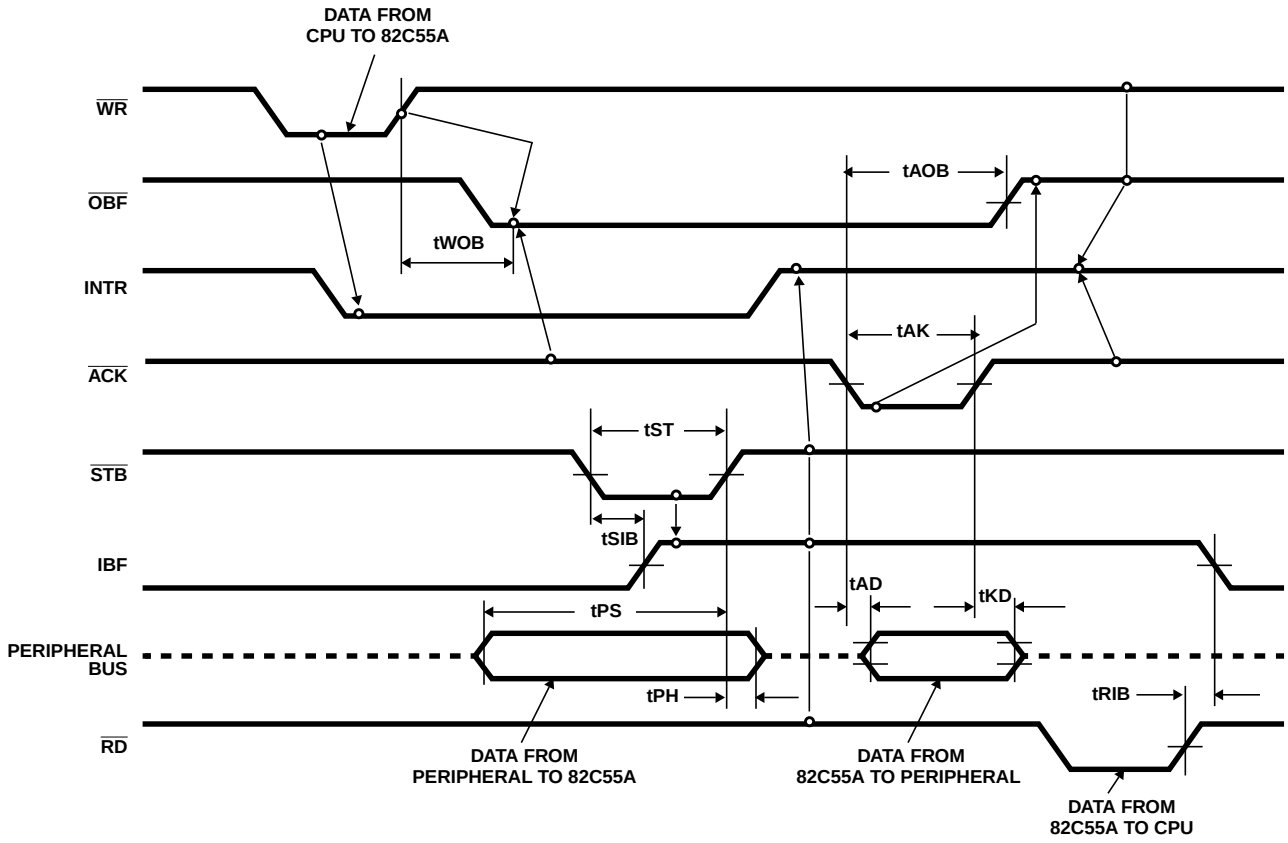


FIGURE 12. MODE 2



NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before RD is permissible. (INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ ÷ $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$)

FIGURE 13. MODE 2 (BI-DIRECTIONAL)

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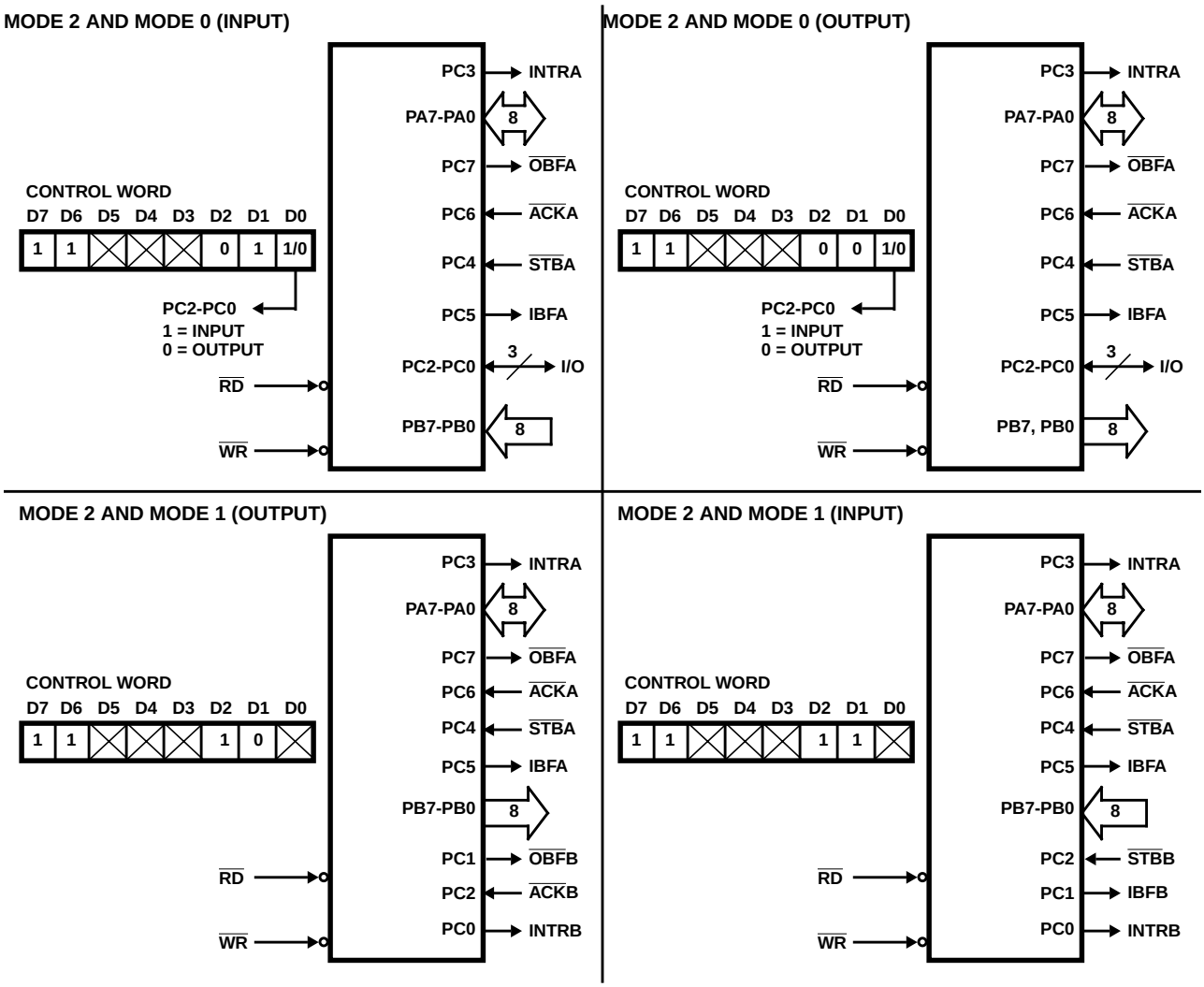


FIGURE 14. MODE 2 COMBINATIONS

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MODE DEFINITION SUMMARY

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA0	In	Out	In	Out	← →	
PA1	In	Out	In	Out	← →	
PA2	In	Out	In	Out	← →	
PA3	In	Out	In	Out	← →	
PA4	In	Out	In	Out	← →	
PA5	In	Out	In	Out	← →	
PA6	In	Out	In	Out	← →	
PA7	In	Out	In	Out	← →	
PB0	In	Out	In	Out		Mode 0 or Mode 1 Only
PB1	In	Out	In	Out		
PB2	In	Out	In	Out		
PB3	In	Out	In	Out		
PB4	In	Out	In	Out		
PB5	In	Out	In	Out		
PB6	In	Out	In	Out		
PB7	In	Out	In	Out		
PC0	In	Out	INTRB	INTRB	I/O	
PC1	In	Out	IBFB	$\overline{OBF}$B	I/O	
PC2	In	Out	$\overline{STB}$B	$\overline{ACK}$B	I/O	
PC3	In	Out	INTRA	INTRA	INTRA	
PC4	In	Out	$\overline{STB}$A	I/O	$\overline{STB}$A	
PC5	In	Out	IBFA	I/O	IBFA	
PC6	In	Out	I/O	$\overline{ACK}$A	$\overline{ACK}$A	
PC7	In	Out	I/O	$\overline{OBF}$A	$\overline{OBF}$A	

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a “Set Mode” command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a “Write Port C” command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a “Write Port C” command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in Mode 1 group or to change an interrupt enable flag, the “Set/Reset Port C Bit” command must be used.

With a “Set/Reset Port Cea Bit” command, any Port C line programmed as an output (including IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C fare not affected by a “Set/Reset Port C Bit” command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the “Set Reset Port C Bit” command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

INPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB
GROUP A					GROUP B		

OUTPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
OBFA	INTEA	I/O	I/O	INTRA	INTEB	OBFB	INTRB
GROUP A					GROUP B		

FIGURE 15. MODE 1 STATUS WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
OBFA	INTE1	IBFA	INTE2	INTRA	X	X	X
GROUP A					GROUP B		

(Defined by Mode 0 or Mode 1 Selection)

FIGURE 16. MODE 2 STATUS WORD FORMAT

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

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Reading Port C Status (Figures 15 and 16)

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts “hand shaking” signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the “status” of each peripheral device and change the program flow accordingly.

There is not special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

INTERRUPT ENABLE FLAG	POSITION	ALTERNATE PORT C PIN SIGNAL (MODE)
INTE B	PC2	$\overline{ACK}$B (Output Mode 1) or $\overline{STB}$B (Input Mode 1)
INTE A2	PC4	$\overline{STB}$A (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}$A (Output Mode 1 or Mode 2)

FIGURE 17. INTERRUPT ENABLE FLAGS IN MODES 1 AND 2

Applications of the 82C55A

The 82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a “service routine” associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 82C55A to exactly “fit” the application. Figures 18 through 24 present a few examples of typical applications of the 82C55A.

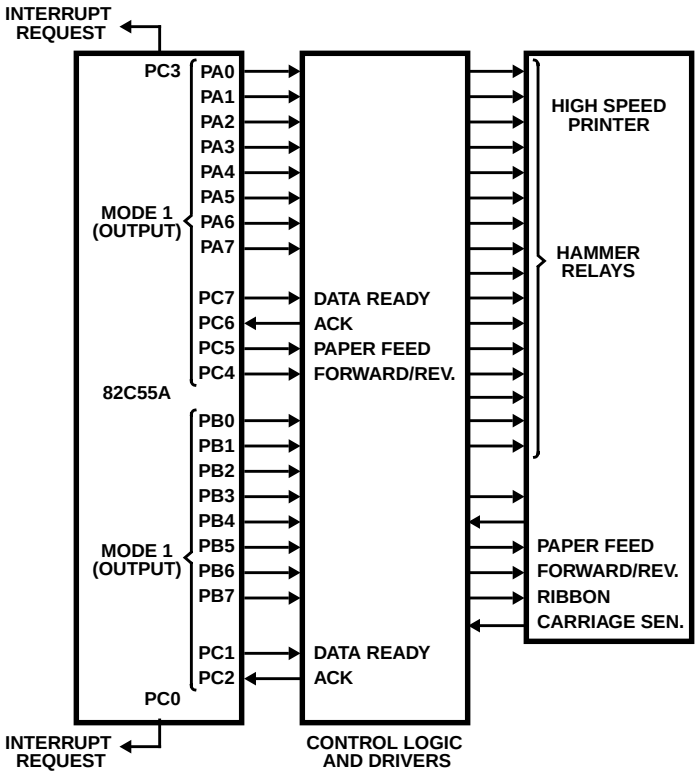


FIGURE 18. PRINTER INTERFACE

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