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April 1998

Digidata 1200B

THEORY AND OPERATION

Part Number 2500-107 Rev E, Printed in U.S.A.

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If you encounter difficulties and need technical support, PLEASE read the **TROUBLESHOOTING** section on page 35 before you call Axon Instruments.

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This instrument is extensively tested and thoroughly calibrated before leaving the factory. Nevertheless, researchers should independently verify the basic accuracy of the instrument using suitable test signals.

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INTRODUCTION

The Digidata 1200B is an advanced, full-featured instrument for data acquisition, stimulation, and environment control. The Digidata 1200B is functionally identical to the 1200A. All functional descriptions of the 1200B also apply to the 1200A. The 1200A and 1200B are also identical at the software level. An important difference between 1200A and 1200B is the I/O connectors. The 1200A uses an 80-pin high-density IDC connector whereas the 1200B uses a 68-pin high-density D-SUB connector. The I/O cable for the 1200A is a flat, ribbon cable. The I/O cable for the 1200B is round and insulated for improved noise performance. The Digidata 1200B is designed to run on IBM AT-compatible computers under both DOS and Microsoft Windows. The Digidata 1200B features a 333-kHz sampling rate, 32 A/D input channels, two D/A output channels, eight digital inputs and eight digital outputs. Large, 8K FIFO memories on both the input and output channels insure reliable data acquisition and control under both DOS and Windows. See the next page for a complete list of features.

The complete system consists of a PC plug-in board, an I/O cable, and a BNC interface box. All active components are located on the plug-in board. The BNC interface box contains both BNC and D-SUB ribbon cable connectors for the signal inputs and outputs.

The Digidata 1200B, as part of the Axon Instruments family of products, has support from a number of Axon hardware and software products. The Digidata 1200B directly couples to the current and voltage outputs of the Axopatch, Axoclamp and GeneClamp amplifiers (and other amplifier types). Primary software support comes from later versions of pCLAMP and AxoScope .

A diskette is included with utility programs for the Digidata 1200B. INITDIGI initializes the Digidata 1200B outputs and real-time clock, and sets the Analog Outputs to any specified value. TESTDIGI exercises the major functions of the Digidata board when troubleshooting, and is used to calibrate the Digital-to-Analog and Analog-to-Digital converters

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FEATURES

- 32-channel analog input channels
- 12-bit 333 kHz A/D converter
- Random channel and gain sequencing list with a maximum 256 entries
- Four programmable input gains: 1, 2, 4, and 8
- Input resolution from 5 mV (gain of 1) to 625 µV (gain of 8) per A/D unit
- Two 12-bit 333 kHz D/A converters
- Maximum range of analog and is ±10.24 V
- 8192 sample FIFO buffer for A/D
- 8192 sample FIFO buffer for D/A
- DMA for A/D (16-bit transfer)
- DMA for D/A (16-bit transfer) and four synchronous digital outputs
- Eight asynchronous or four synchronous digital outputs
- Eight asynchronous digital inputs
- 48-bit 250 ns real-time clock (8254)
- 5-channel counter/timer (9513A)
- A/D timing clock (9513A)
- Separate D/A timing clock (9513A)
- Split-clock acquisition
- Externally triggered A/D sampling
- Three external counter inputs (9513A)
- Dedicated external data tag input
- External sweep trigger input (9513A); for pre-triggered data acquisition
- All gate and source inputs of 9513A are brought to the end connector
- Digital output bit #0 can be optionally programmed to inhibit data acquisition

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INSTALLATION

Installation of the Digidata 1200B system is very simple. For most users, the Digidata board is simply plugged into the computer, and the I/O cable is used to connect the board to the interface. Some users may need to change the base I/O address (see below). Other configuration items such as DMA channels and IRQ levels are set in software, so there are no other jumpers or switches on the board. After going through the Functional Checkout, the Digidata 1200B system is ready to use. Chapters on **UTILITY PROGRAMS**, **TROUBLESHOOTING**, and **CONFIGURATION AND CALIBRATION** contain useful information.

In addition to the Digidata hardware installation, we recommend that you place the utility program INITDIGI in the computer's AUTOEXEC.BAT file to initialize the Digidata board and set the analog outputs to the desired value. See the chapter **UTILITY PROGRAMS** for instructions.

Parts List

The Digidata 1200B hardware includes:

- 1200B-BD plug-in board
- 1200B-C 68-pin HD D-SUB shielded round cable
- 1200B-BNC interface box

Hardware Installation

The Digidata 1200B plug-in board is sensitive to static electricity. Do not remove it from its anti-static bag until installation. Before handling the board, discharge any static buildup by touching a finger on a bare metal surface on the computer case. Hold the board only by its edges; never touch the bus slot connector or the solder points on the back of the board.

Base I/O Address

As shipped from the factory, there is usually no need to change the default base I/O address of the Digidata board. The default base I/O address of the Digidata 1200B is 320 hex and occupies 32 (20 hex) continuous addresses in the I/O address space. If you have other expansion boards installed in your computer such as a network board, check their base I/O addresses. If addresses between 320 hex to 33F hex are being used by another board, you must change the I/O address of one of the boards. See the chapter **CONFIGURATION AND CALIBRATION** to set the Digidata base I/O address. pCLAMP versions 6.0 and up, and AxoScope versions 1.0 and up support alternate Digidata base addresses.

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Installing the 1200B-BD Plug-in Board

The AT-compatible computer must have an available 16-bit ISA expansion slot to accommodate the plug-in board. A 16-bit slot has two in-line connectors; see Figure 1.

1. Turn off the computer, monitor, printer, and all other peripherals attached to the computer. Unplug the power cords.

2. Remove the computer cover. Remove the appropriate slot cover at the back of the computer case.

3. Holding the board by its edges, position it over a 16-bit ISA slot so that the end connector/bracket and bus slot connector are towards the back of the computer, and the front edge aligns properly with the support bracket at the front of the computer.

4. Carefully lower the board so that the front edge properly slides into the support bracket and the end connector slides into the appropriate slot opening. Make sure the bus slot connector lines up properly when it contacts the bus slot. Gently push the board into the slot until fully seated. **Do not force the board into place!** If it does not go in easily, check to see if the board and slots are aligned properly and if there is any obstruction impeding insertion. If the slot just appears to be tight, gently rock the board front to back to ease it into the slot. Do not wiggle the board side to side, as this may damage the board.

5. Make sure that none of the components on the board are in contact with any board in an adjacent slot!

6. Secure the board at the end bracket with the screw that held the slot cover in place.

7. Replace the computer cover and any cables that were previously removed.

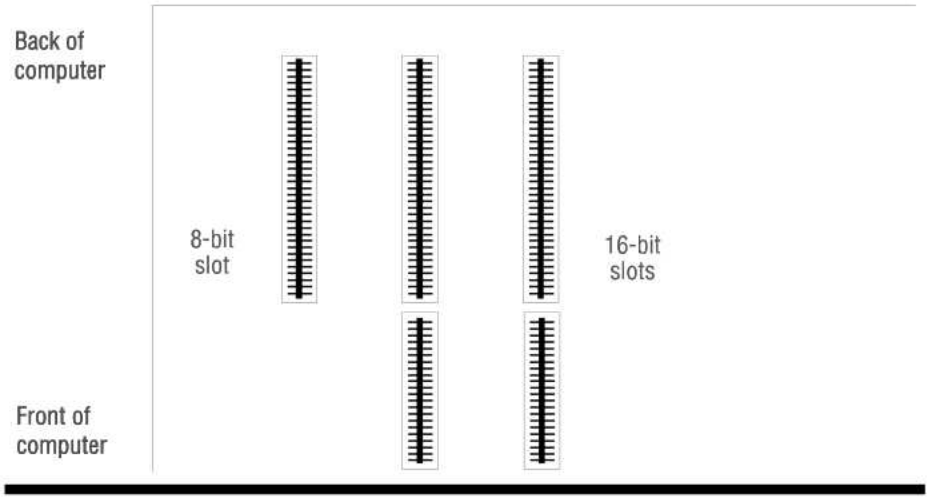


Figure 1. Top view of the computer motherboard.

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Connecting the 1200B-C 68-pin HD D-SUB shielded round cable

Caution: The 68-pin high-density connectors on the Digidata 1200B board and the interfaces have pins that are delicate and closely spaced. Before attaching the cable to the connectors, make sure that the pins are straight and evenly spaced. Use a small screwdriver or needle-nose pliers to gently straighten any bent pins.

Connect either end of the cable to the Digidata board end connector. Press the connectors straight in, applying even pressure on both ends of the connector.

Connecting the Interface

Installing the 1200-BNC Interface Box: Carefully connect the cable to the connector marked "TO DIGIDATA BOARD" on the back panel.

Making Signal Connections

On the **1200-BNC interface box** the center pin of each BNC connector is the active signal. Note that on the sixteen Analog Input BNCs, the BNC shields connect to Analog Return, which is isolated from Analog Ground. The user may connect the BNC shield with the analog ground on peripheral equipment.

WARNING -- Power-Off Loading

When the computer is off, the analog inputs of the Digidata 1200B present a low-impedance load, so the output of instruments connected to the Digidata 1200B will be pulled towards ground.

Grounding and Minimizing Noise

On the Digidata 1200B and on Axon amplifiers, all BNC shields are connected together. Thus, two or more BNC cables between the same two instruments can create a ground loop and produce 60 or 50 cycle hum.

When noise in the set-up occurs, the first step is diagnosis. Take ALL instruments out of their racks, and connect them together with only ONE BNC connection. Observe if the hum is eliminated. Also observe if the hum is produced by pickup from the headstage by shielding the headstage and watching the magnitude of the hum.

If the hum is eliminated at this step, then connect the second BNC cable. If hum is now observed, this is probably a gound loop that is picking up an alternating magnetic field. Next try to eliminate the source of the alternating magnetic field: a cheap tranformer, an electric motor, such as found in a nearby fan or refrigerator. Try to rearrange the two BNC cables to determine if their positioning tells you anything about the source of the alternating field.

If removing the source of the alternating field is not possible, eliminate the ground loop by making one of the connections between the two instruments without a shield. Make this either with a naked unshielded wire, or with a BNC cable that has its shielding cut at one end.

For users of Axon amplifiers, more information regarding noise reduction procedures can be found in

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the Axopatch 200B, Axopatch 1D, and AxoClamp 2B manuals.

Software Installation

The Digidata 1200B comes with utility programs for testing the interfaces and drivers as well as the acquisition programs AxoScope 1.1 and AxoScope 7. The Digidata 1200B is supported by current versions of pCLAMP 6 and pCLAMP 7. To install the utility programs, change to the desired directory on your hard disk and type:

```
copy a:\*.*
```
(Use "b:" if copying from the b: drive)

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FUNCTIONAL CHECKOUT

The Digidata 1200B support diskette includes the TESTDIGI program, which tests the major functions of the Digidata 1200B board. Once the Digidata 1200B and the interface are properly installed, use TESTDIGI to verify the proper functioning of the board. Read the description of TESTDIGI in the next chapter, then follow this procedure:

1. Run the test program by typing **`TESTDIGI`** at the DOS prompt. The program will say if it detected the Digidata board. If you changed the base I/O address of the Digidata from the default of 320h, you need to give the new address on the command line. For example, if you changed the address to 340h, type **`TESTDIGI /A340`**.

2. Use the **DAC** function to set the Analog Outputs to various values, and check the output of Analog Out #0 and #1 with a voltmeter or oscilloscope.

3. Connect an Analog Out channel to an Analog In channel, set the DAC, then use the **ADC** function to read the voltage being sent from the Analog Out channel. Try using different gain values. Remember that the analog input voltage range is reduced proportionally with increasing gain.

4. Connect Digital Out #0 and #1 to Digital In #0 and #1. Use **WriteDigital** to set the digital outputs high and low; use **ReadDigital** to read and check them. Similarly check other digital inputs and outputs if required.

5. The 9513A timer OUT 5 signal is available to the user. Use **Setfreq** to set the OUT 5 signal toggling between logic low and high at the chosen clock period. Use an oscilloscope to verify that the period is correct.

6. The **ShowClock** function displays the real-time counter. The counter is started either by running the INITDIGI program (see next chapter) or when you first execute the ShowClock function in TESTDIGI.

7. Choose **Function** to output a waveform on an Analog Out channel. Use an oscilloscope to verify the shape of the waveform.

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UTILITY PROGRAMS

Two utility programs are provided with the Digidata 1200B board. The **TESTDIGI** test program provides functions to test the various features of the Digidata 1200B board. **INITDIGI** initializes the DAC outputs to a specified voltage and is intended for use in the AUTOEXEC.BAT file.

TESTDIGI

Use TESTDIGI to test the Digidata 1200B input/output functions. Send voltage waveforms or a constant level out of two analog outputs, read voltages from 32 analog inputs, write digital levels to eight digital outputs, read digital levels on eight digital inputs, set a counter output to a specified frequency, and test the real-time clock.

Usage: **`TESTDIGI`** [*options*]

options: **`/A`***Base I/O address in hex*

TESTDIGI assumes the Digidata 1200B will be found at the default I/O address of 320 hex. If the I/O address was changed during installation, specify the new I/O address on the command line. For example, if the I/O address has been changed to 180 hex, type:

```
TESTDIGI /A180
```

To run the various tests, type the name of a listed function and follow the prompts. To accept a default value that appears at a prompt, just hit the <Enter> key. For input functions, the result will be displayed on the screen. For output functions, use a voltmeter or oscilloscope to check the output signal. Note: when typing the name of a function, only the minimum number of characters to select a function unambiguously is needed. Only the first letter is needed for most of the functions.

Functions Available in TESTDIGI:

ADC Read the voltage on the specified Analog In channel. **Amplifier gain:** Specify the desired signal gain. The result is reported in A/D units (from -2048 to 2047 A/D units) and volts. With a gain of one, the input range is -10.240 to 10.235 volts, for a resolution of 5 mV per A/D unit.

DAC Output a voltage on the specified Analog Out channel. **Output voltage:** The voltage is entered as a real number in the range -10.240 to 10.235 volts. The corresponding number of D/A units is displayed.

ReadDigital Read the digital levels on the eight Digital Inputs. The eight values are read as a byte and displayed in decimal, hexadecimal, and as the individual digital levels.

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WriteDigital Set the eight Digital Outputs. Enter a string of zeroes and ones, up to eight digits, to set the Digital Output channels low (zero) or high (one). The right-hand digit in the string corresponds to Digital Output #0. Examples: 1011 sets Digital Outputs #3, #1 and #0 high, the rest are set low; 10001100 sets Digital Outputs #7, #3, and #2 high, the rest are set low.

Setfreq Set counter OUT 5 to toggle continuously at the chosen clock period. Enter the period in microseconds. The clock period will be rounded to the closest even number of microseconds. The rate will also be reported as frequency.

TrimMode This function is used to trim the A/D converter. It assumes that DAC0 is connected to ADC0. Choose an output voltage in the specified range; the TrimMode function continuously reads the voltage on ADC0 until the <Esc> key is pressed. See the chapter **CONFIGURATION AND CALIBRATION** for instructions on A/D and D/A calibration.

ShowClock Display the real-time counter. The display will show elapsed time down to a hundredth of a second, although the Digidata's 8254 timer counts time with 250 nanosecond resolution.

Function Output a waveform on an Analog Out channel. The waveforms available are Sine, Square, Ramp, and Triangle. Specify the amplitude, the number of D/A points in the waveform (points per period) and the time per D/A point. Press <Esc> to stop.

Quit Quit the program and return to the DOS prompt. The D/A level, OUT 5 counter toggling, and the Digital Outputs are left as they have been set.

Error Messages

Most of the error messages are self-explanatory. Here are explanations for the less-obvious error messages:

```
** Error **: Unrecognized option on command line:
```
or
```
** Error **: Invalid I/O port base address specified
```

When invoking the TESTDIGI program, the only command-line option available is to specify an I/O address different from the default of 320 hex. See the proper format above and the chapter **CONFIGURATION AND CALIBRATION** for valid base I/O addresses.

```
The Digidata 1200A ID register value is not correct.
The I/O Port Base address of XXX (Hex) may not be correct.
```


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When TESTDIGI is invoked, it checks the ID register for the proper value (see *Register Descriptions*). If the value is not correct, it is probably because either the Digidata board is not installed in the computer, or the board is not at the I/O address that TESTDIGI expects. Compare the setting of switch block SW1 on the Digidata board with the table in the **CONFIGURATION AND CALIBRATION** chapter.

```
** A/D converter is not responding! **
```

This indicates a hardware problem. Call Axon Instruments for technical support (650-571-9400).

INITDIGI

INITDIGI initializes the Digidata 1200B acquisition board by setting the Analog Outputs, Digital Outputs, 9513A timer outputs, and the real-time clock all to zero; just type INITDIGI. INITDIGI may also set the Analog Outputs to specified values. The state of the Analog Outputs are undefined when the computer is turned on, so we recommend placing INITDIGI in the AUTOEXEC.BAT file to set the Analog Outputs to the desired values upon boot-up of the computer.

Usage: **INITDIGI** [*options*] [*Voltage or Units*]

options: **/A***Base I/O address in hex*
/D*DAC channel number*
/N
/S*DAC scale factor (Units/Volt)*

/A Provide an alternative base I/O address. The default Digidata base I/O address is 320 hex.

/D Set DAC channel #0 or #1.

/N Do not reset the Digital Outputs, the 9513A timer outputs or the real-time clock.

/S If the instrument attached to the Analog Output scales the signal (*e.g.*, the instrument sends out 20 mV per volt at the Analog Output), you may specify the actual units (in mV in this case) by providing the scaling factor.

Example:

```
INITDIGI /A220 /D1 /S20 -70
```

The above command will send -3.5 Volts to Analog Out #1 (-70 mV with a scale factor of 20 mV/Volt) of a Digidata board that has its base I/O address set to 220 hex.

Error Messages

Most of the error messages are self-explanatory, the rest are explained above in the list of error messages for TESTDIGI.

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PRINCIPLES OF OPERATION

A/D Conversion

Analog to digital conversions may be initiated by either a software strobe or pulses from the 9513A timer output channel OUT2. A software strobe is performed by writing a 1 to Clear register bit 7. If a precision sampling rate is required, channel 2 of the 9513A is dedicated to generating the timing pulses for A/D conversion. The 9513A output must be programmed for Output Active High pulse mode. The timer clock source is from its 4 MHz oscillator or from either the external GATE or SOURCE input.

As soon as the A/D data conversion is done, the converted data is temporarily saved in the first-in-first-out (FIFO) buffer. The FIFO buffer has a flag called the Empty Flag (-EF). It is active when the FIFO is empty. The -EF becomes inactive when an A/D conversion is done (the FIFO is not empty). The -EF can be checked from Status register bit 6. The -EF flag will be automatically set active (logic low) by a subsequent read of the A/D data. Alternatively, it can be cleared by writing a 1 to Clear register bit 4, which is the Clear ADC bit.

The FIFO buffer size is 8192 samples. The advantage of having a FIFO memory is that the transfer of data to main memory does not have to be performed immediately after completion of the A/D conversion. The processor and the I/O bus can be freed to perform other tasks. In addition, the speed of DMA transfer can be greatly improved by performing block transfers.

The transfer of A/D data can be done simply by an I/O read of the ADC Data register, which is the FIFO buffer output port. I/O data transfer can be managed by polling the -EF flag through the Status register or from -EF flag-initiated interrupts. The -EF flag can be set up to generate an interrupt request. If a higher data transfer speed is desired, the DMA controller can be set up to perform high-speed transfer. DMA operation will be discussed further in a later section.

When the A/D FIFO buffer is full, it sets a flag called the Full Flag. When full, additional data written to the buffer will be lost. The Full Flag can be monitored through Status register bit 7, and also can be used to generate an interrupt request. The flag is cleared by either writing a 1 to Clear register bit 4 or by reading the ADC Data register.

The ADC Data register width is 16 bits. The 12-bit ADC data is located at the upper twelve bits of the ADC register. Two of the four least significant bits are used as data TAG and SWEEP TRIGGER indicators. TAG and SWEEP TRIGGER will be discussed in the following sections.

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Random Channel and Gain Sequencing

There are 32 analog input channels, 4 programmable input gains, and 256 programmable random channel sequencing registers called the scan list. The scan list determines the channel order and programmable gain settings for a series of A/D conversions. To save I/O space, all 256 registers in the scan list are programmed through one I/O register which is called the Scan List Programming register.

The Scan List Programming register is a 16-bit register. Within this register, the eight least significant bits address the 256 scan list registers, the next five bits select one of the 32 channels, the next two bits select the gain, and the most significant bit (MSB) indicates the entry at the end of the list. The MSB is called the End of List bit. When this bit is set, it indicates the last register in a scan sequence. During A/D operation, the scan list pointer addresses each of the 256 registers in increasing numeric order. The End of List signal brings the scan list pointer back to the first register. The scan list pointer automatically wraps around. The minimum sequencing length is one, in which case the End of List bit should be set. The scan list pointer can be forced to the first location by writing a 1 to Clear register bit 4.

D/A Conversion

The source of D/A data can be either an I/O write or the D/A FIFO buffer. An I/O write to the DAC Data register bypasses the D/A FIFO buffer. The I/O write causes an immediate D/A conversion. If the D/A data source is the D/A FIFO buffer, the FIFO buffer can only be filled through a DMA transfer. During DMA D/A operation, the data are transferred from the processor's main memory to the FIFO buffer through the DMA controller, and from the FIFO buffer to the D/A converter by 9513A output pulses (OUT1 or OUT2). The details of DMA operation will be discussed in a later section.

During I/O operation, the timing can be generated by 9513A channel 1. The Channel 1 output (OUT1) sets a flag called DONE1. A D/A I/O write can be initiated by polling the DONE1 flag through Status register bit 0, or by a DONE1-initiated interrupt. During DMA operation, the D/A timing is controlled by the 9513A. In simultaneous A/D and D/A mode, D/A timing will be synchronous with A/D timing when using the 9513A channel 2 output (OUT2). When D/A timing is asynchronous with the A/D timing, the D/A timing comes from the 9513A channel 1 output (OUT1). To choose OUT1 as the D/A timing source, set bit 2 of the ADC/DAC/TRIG Control register.

The DAC Data register width is 16 bits. The 12-bit D/A data is located at the upper 12 bits of the register. The four least significant bits are used as synchronous digital outputs. In the synchronous digital output mode, the digital outputs are synchronous with the D/A waveform. There is more discussion on digital output in later sections.

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Timer/Counter

There are two timers on the Digidata 1200B, a 9513A and an 8254 timer. The 9513A serves as the timing source for A/D and D/A data conversion, and as a general purpose timer and counter for setting time intervals and counting discrete events. The 8254 is used only as a real-time clock with a 48-bit counter and 250 ns clock period.

The 9513A contains five 16-bit timer/counters. Each timer has five pre-scaled clock rates to select from. The source clock is 4 MHz. Adjacent channels can be cascaded internally so that a wider counter (32 bits vs. 16 bits) or two different rates can be implemented easily.

9513A channel 1 is either a general-purpose counter or a timing source for D/A. Channel 2 is generally dedicated to A/D conversion timing. Channel 3 is either a general-purpose counter or for use with split-clock acquisition. Channel 4 and 5 are general purpose counters. All GATE and SOURCE inputs of the 9513A are brought to the end connector. The GATE inputs of channels 1, 3, and 5 are available on the BNC interface box and the screw terminal panel.

> Split-clock acquisition is a unique feature of the Digidata 1200B. It allows for a faster acquisition rate during the transient state, and a slower rate at the steady state of the input signal. This feature not only saves data memory space but also data processing time. To implement the split-clock acquisition, channel 2 of the 9513A is set up as the clock for A/D conversion. The clock rate can be altered by loading registers with the two values, and changing the input level on the channel 2 gate (GATE2). Channel 3 is set up as a counter which counts the output pulses of channel 2 (OUT2) through an internal link, and its output (OUT3) is set to toggle at terminal count. Channel 3 (OUT3) is fed back to the gate input of GATE2 through external circuitry. During the operation, when OUT3 toggles it changes the channel 2 clock rate. Channel 3 can also alternate between two counter values upon terminal count. As a result, channel 2 alternates between two clock rates and channel 3 controls the number of samples at each clock rate. The split-clock acquisition is enabled by setting bit 5 of the ADC/DAC/TRIG Control register to HIGH and resetting Counter4's output to LOW.
>
> In the Digidata 1200 mode (bit 6 of ADC/DAC/TRIG Control register set to zero), split-clock acquisition is enabled by setting bit 5 of the ADC/DAC/TRIG Control register to 1. The state of Counter4 has no effect in this mode..

Three of the 9513A outputs, OUT1, OUT3, and OUT4, are connected to three Done flip-flops, which set the Done1, Done3, and Done4 flags, respectively. The rising edge of the OUT signals set the Done flags. Each Done flag can be monitored through Status register and cleared through the Clear register. The Done flags can generate interrupt requests.

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Digital Input and Output

There are eight asynchronous digital inputs.

There are eight asynchronous digital outputs. The four least significant bits are shared with synchronous digital outputs. During synchronous mode, the four most significant bits remain unchanged from their previous settings. The asynchronous digital output mode can be enabled by setting bit 3 of ADC/DAC/TRIG Control register.

There are four synchronous digital outputs which share the four least significant bits of asynchronous digital outputs. In the synchronous mode, the digital outputs are specified in the four least significant bits of the D/A data, and therefore are synchronized with the D/A waveform.

Bit 0 of the digital output in either asynchronous and synchronous mode can be used to inhibit the A/D conversion. This is another unique feature to save data memory and data processing time. When this feature is enabled by setting bit 7 in the ADC/DAC/TRIG Control register, setting bit 0 of the digital output will inhibit A/D data conversion, consequently preventing data transfer.

Tagging and External Triggering

There are situations where specific data points need to be tagged to indicate the occurrence of events. The digital event signal can be taken from the Axon AI 2020A Event Detector, or the digital output of any event-counting or window discrimination device. The Event Detector output can be connected to the TAG input of Digidata 1200B. The positive level of the event pulse sets a Tag flag. The Tag flag can be read with the A/D data. The Tag is located at bit 0 of the ADC Data register. The Tag flag reflects the state or logic level of the Tag input.

Since the interrupt latency or loop execution time is a complex function of the total system activity under the MS Windows environment, the Digidata 1200B provides true hardware-gated triggered episodic acquisition. In event-triggered data acquisition, the application program collects data in a circular buffer until a trigger occurs. As triggered data acquisition begins, the application program saves the circular buffer data collected before the trigger event. This is called pre-triggered data acquisition. The external trigger signal sets the XTRG flag. This flag is located at bit 1 of the ADC Data register and is read with the A/D data. The XTRG flag reflects the logic level of the external trigger signal, *i.e.,* it will always follow the state of the external trigger signal. The external trigger input is also connected to GATE4 of the 9513A. The 9513A OUT4 sets a Done4 flag, which in turn generates an interrupt request to the host processor to acknowledge the arrival of the external trigger. At the same time, the HIGH state of OUT4 turns on the gate to let FOUT of the 9513A to be used as the clock source at Counter2, and OUT4 will be connected to GATE1 such that Counter1 can be used as a level-gated generator started by a positive level sensed by Counter4. Counter3 is used as the split-clock counter. The XTRG and Done4 flag can be cleared through the Clear register.

In the Digidata 1200 mode (bit 6 of the ADC/DAC/TRIG Control register set to 0) there is no support for true hardware-gated episode triggering. However, external triggering is still available. When an external trigger arrives, the Done4 flag will generate an interrupt request to the host processor. The application program then needs to start acquisition upon fielding the interrupt. In a single task operating system like DOS, the application program can control the hardware so that the application is

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waiting only for a single interrupt. To obtain even smaller latencies between an external trigger and the start of data acquisition, a DOS application can enter a tight polling loop to check the status of the external start status flag rather than waiting for an interrupt. In this situation, the timing jitter from interrupt latencies or polling loops is relatively small and predictable.

DMA Controller

Since all DMA transfers are 16 bits wide, channels 5, 6, or 7 are used. If simultaneous A/D and D/A is required, two DMA channels can operate at the same time.

The FIFO buffer controller generates three status signals, the Empty Flag (-EF), Half Full Flag (HF), and Full Flag (FF). These three flag signals are used in the DMA request control circuitry. The A/D FIFO HF flag initiates a DMA request and the -EF flag stops the request. In the case of D/A operation, the D/A FIFO HF flag initiates the DMA request and the FF stops the request. Because the process of D/A operation empties the buffer, the D/A FIFO buffer has to be filled before D/A operation.

To operate with the FIFO buffer controller, the computer's DMA controller is programmed in the "demand transfer" mode. The actual transfer is done in small blocks, in short high speed bursts. This allows the host processor to execute instructions in between transfers. In an environment where DMA auto-initialization mode is prohibited, the processor can re-initialize the DMA controller.

Since A/D DMA transfers are generated at the FIFO half-full condition, when A/D acquisition stops there might be data left in the FIFO buffer. The user must flush out the residual data in the FIFO.

Another way to initiate DMA transfer is to enable bit 4 in the DMA/INTERRUPT CONTROL register. Set up the DMA transfer in the "demand transfer" mode. The A/D transfer will be initiated when the A/D FIFO buffer is not empty and the transfer will stop when the FIFO buffer is empty. The advantage to this type to DMA transfer is that the user does not need to flush the FIFO buffer. The disadvantage is that whenever there is data in the FIFO buffer there will be a DMA transfer initiated. When the A/D is set up for a 330 kHz sampling rate, the A/D DMA will occupy the bus all the time. If the system is set up for simultaneous A/D and D/A DMA transfer, the D/A transfer may be suppressed. To avoid the A/D dominating the I/O bus completely, set the DMA controller in the "fixed priority" mode and give higher priority to D/A DMA transfer. By doing so, the D/A DMA block transfers will be guaranteed and the A/D DMA transfers will fill in between the D/A DMA transfers.

At the end of the DMA transfer, the DMA controller generates a Terminal Count pulse (TC). The TC pulse is logically ANDed with the AD DMA ACK and DA DMA ACK signals to set the AD DMA TC and DA DMA TC flags, respectively. The flag can be read from the ADC/DAC/TRIG STATUS register and is used to initiate an interrupt request.

In the Digidata 1200 mode, both the AD and DA DMA will share the same TC flag (bit 5 of ADC/DAC/TRIG STATUS register).

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Interrupt Controller

The interrupt channels available to Digidata 1200B are 10, 11, 12, and 15. Only one of the four interrupt channels can be selected at one time. The selected interrupt line will drive the PC-AT bus IRQ signal. The unselected lines are in tri-state so that other I/O device can use these lines.

Possible interrupt sources are the A/D FIFO Full Flag (FF), A/D FIFO Empty Flag (-ADEF), DA FIFO Underrun Flag (DAEF), AD DMA Transfer Done (AD DMA TC), DA DMA Transfer Done (DA DMA TC), and the Done1, Done3, and Done4 flags. These signals can be individually enabled. The enabled signals are OR'ed to initiate the interrupt request. The origin of the interrupt request can be traced through the ADC/DAC/TRIG STATUS register.

In the Digidata 1200 mode, there is only one TC flag for both AD and DA DMA Terminal Count flags.

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REGISTER DESCRIPTIONS

Register I/O Locations

The Digidata 1200B has fourteen 16-bit registers which are located at even I/O addresses. All commands and data, as well as configuration and status information are sent or accessed through these registers.

The base I/O address is set at the factory to 320H. See the chapter **CONFIGURATION AND CALIBRATION** to change the base address.

The table below lists the description and I/O location of each register.

REGISTER DESCRIPTION	BASE+
DAC data, Synchronous digital output, & ADC inhibit	00H
ADC data, TAG, & XTRG	00H
ID register	02H
9513 Timer data	04H
9513 Timer control/Status	06H
ADC/DAC/TRIG Control	08H
DMA/Interrupt configuration	0AH
Asynchronous digital input/output	0CH
ADC scan list programming	0EH
8254 channel 0 data	10H
8254 channel 1 data	12H
8254 channel 2 data	14H
8254 channel control word	16H
ADC/DAC status	18H
Clear register	1AH
None	1CH
None	1EH

Register Descriptions

DAC DATA & SYNCHRONOUS DIGITAL OUTPUT (Output)	00H
Bit 15	DAC data D11
|	|
Bit 4	DAC data D0
Bit 3	Synchronous digital output D3
Bit 2	Synchronous digital output D2
Bit 1	Synchronous digital output D1
Bit 0	Synchronous digital output D0; or ADC inhibit, active=1

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Bits 0-3 of this register specify Digital Outputs 0-3 when bit 3 of the ADC/DAC/TRIG Control register is set for Synchronous Digital Output mode. Digital Outputs 4-7 remain unchanged from their previous states. The Asynchronous Digital Output register is ignored.

Digital output D0 can be used to inhibit ADC data acquisition. This is enabled by setting bit 7 in the ADC/DAC/TRIG Control register. When this function is disabled, D0 is used as a regular digital output.

ADC DATA (Input)	**00H**
Bit 15	ADC data D11
|	|
Bit 4	ADC data D0
Bit 3	N/C
Bit 2	N/C
Bit 1	XTRIG, active=1
Bit 0	TAG, active=1

ID REGISTER (Input)	**02H**	
	1200A Mode	**1200 Mode**
Bit 7	0	0
Bit 6	0	0
Bit 5	0	0
Bit 4	0	0
Bit 3	0	0
Bit 2	0	0
Bit 1	1	1
Bit 0	1	0

The ID register is a read-only register which helps the user to identify the Digidata boards.

9513 TIMER DATA (Input/Output)	**04H**
Bit 15	Data D15
|	|
Bit 0	Data D0
Read: Current contents Write: New contents	

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9513 TIMER CONTROL (16-bit) (Input/Output)	**06H**
Bit 15	Prefix, always=1
|	|
Bit 8	Prefix, always=1
Bit 7	Control data, D7
|	|
Bit 0	Control data, D0
Read: Status	
Write: Command and data pointer	

For information on programming the 9513A registers, see the Advanced Micro Devices data book.

ADC/DAC/TRIG CONTROL (Output)	**08H**
Bit 7	Digital out inhibit ADC enable, active=1
Bit 6	Digidata 1200 Compatible mode enable, active = 0
Bit 5	ADC split-clock enable, active=1
Bit 4	ADC scan list programming enable, active=1
Bit 3	Asynch. digital output enable, active=1
Bit 2	DAC asynchronous with ADC enable, active=1
Bit 1	DAC channel 1 enable
Bit 0	DAC channel 0 enable

Since the DMA controller cannot address I/O devices, the two D/A channels are located at the same address. If both D/A channels are selected and enabled in the ADC/DAC/TRIG Control register, continuous I/O writes will alternate between DAC0 and DAC1. To select which D/A channel starts first, enable one channel, which will start first, and then enable both channels.

Bit 1	Bit 0	Action
0	0	None
0	1	DAC0 only
1	0	DAC1 only
1	1	DAC0 and DAC1

Bit 2 determines whether D/A operation is synchronous with the A/D conversions. If bit 2 is 0, D/A will be clocked by 9513A channel 2, which is the same clock for the A/D. If bit 2 is 1, the D/A will be clocked by 9513A channel 1.

Bit 3 determines whether the digital output is synchronous to the D/A operation. In synchronous mode, the lower 4 bits of the digital output will be synchronous to the D/A converter(s). The upper 4 bits remain unchanged. In the asynchronous mode, all 8 bits of digital output are controlled through I/O write operations and are asynchronous to the D/A output.

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Bit 4 of the ADC/DAC/TRIG Control register is used to enable programming of the ADC Scan List registers. Bit 4 should be enabled before, and disabled immediately after programming the scan list memory. *Warning:* Leaving this bit active while running acquisition may cause the scan list data to be lost.

Bit 5 enables "split-clock acquisition." In this mode, the output of 9513A channel 3 (OUT3) is fed back to the gate input of channel 2 (GATE2). The detailed operational description can be found in the previous section.

Digital output D0 can be used to inhibit ADC data acquisition. This is done by setting bit 7 in the ADC/DAC/TRIG Control register. When this function is disabled, D0 is used as a regular digital output.

DMA/INTERRUPT CONFIGURATION (Output)	**0AH**
Bit 15	Interrupt request output enable, EN/TRI, 1/0
Bit 14	Interrupt level select
Bit 13	Interrupt level select
Bit 12	DA FIFO underrun interrupt enable, active = 1
Bit 11	Interrupt on "-ADEF inactive" enable, active=1
Bit 10	Interrupt on ADC FIFO full enable, active=1
Bit 9	Interrupt on DMA (TC) transfer done enable, active=1
Bit 8	Interrupt on 9513 DONE4 enable, active=1
Bit 7	Interrupt on 9513 DONE3 enable, active=1
Bit 6	Interrupt on 9513 DONE1 enable, active=1
Bit 5	DA FIFO underrun reset, active = 0
Bit 4	ADC DMA single transfer mode enable, active=1
Bit 3	DAC DMA channel select/enable
Bit 2	DAC DMA channel select/enable
Bit 1	ADC DMA channel select/enable
Bit 0	ADC DMA channel select/enable

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Bit 0, 1, 2, and 3 enable A/D and D/A DMA channels. The unused DMA request lines (DRQ) are in high-impedance state (tri-state). This allows other I/O devices to use the DMA channels.

Bit 3	Bit 2	Bit 1	Bit 0	Action
0	0	0	0	None
0	0	0	1	ADC DMA #5
0	0	1	0	ADC DMA #6
0	0	1	1	ADC DMA #7
0	1	0	0	DAC DMA #5
0	1	0	1	*Illegal*
0	1	1	0	DAC DMA #5 & ADC DMA #6
0	1	1	1	DAC DMA #5 & ADC DMA #7
1	0	0	0	DAC DMA #6
1	0	0	1	DAC DMA #6 & ADC DMA #5
1	0	1	0	*Illegal*
1	0	1	1	DAC DMA #6 & ADC DMA #7
1	1	0	0	DAC DMA #7
1	1	0	1	DAC DMA #7 & ADC DMA #5
1	1	1	0	DAC DMA #7 & ADC DMA #6
1	1	1	1	*Illegal*

When bit 4 is 0, the ADC DMA transfer is in block (demand) mode. When bit 4 is 1, the DMA is initiated at the A/D FIFO not-empty condition and the transfer stops when the FIFO is empty.

Bits 6, 7, 8, 9, 10, and 11 enable the interrupt sources. The selected interrupt source signals are OR'ed together.

Bits 13, 14, and 15 select the interrupt level. Only one of the four channels can be selected at one time. If bit 15 is 0, no interrupt channel is selected. The output to the interrupt request lines (IRQ) is in tri-state. This allows other I/O devices to use the interrupt line.

Bit 15	Bit 14	Bit 13	Action
0	X	X	Tri-state
1	0	0	IRQ10
1	0	1	IRQ11
1	1	0	IRQ12
1	1	1	IRQ15

ASYNCHRONOUS DIGITAL OUTPUT (Output)	**0CH**
Bit 7	Digital output D7
Bit 6	Digital output D6
Bit 5	Digital output D5
Bit 4	Digital output D4
Bit 3	Digital output D3
Bit 2	Digital output D2
Bit 1	Digital output D1
Bit 0	Digital output D0; or ADC inhibit, active=1

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When bit 3 of the ADC/DAC/TRIG Control register is set for Synchronous Digital Output mode, this register is ignored. Use DAC Data register bits 0-3 to set Digital Outputs 0-3. Digital Output bits 4 through 7 remain unchanged from their previous state.

Bit 0 can control A/D conversion (with bit 7 enabled in the ADC/DAC/TRIG Control register). When bit 0 is programmed to inhibit A/D conversion, the bit 0 setting is still available on Digital Output 0.

ASYNCHRONOUS DIGITAL INPUT (Input)	**0CH**
Bit 7	Digital input D7
Bit 6	Digital input D6
Bit 5	Digital input D5
Bit 4	Digital input D4
Bit 3	Digital input D3
Bit 2	Digital input D2
Bit 1	Digital input D1
Bit 0	Digital input D0

SCAN LIST PROGRAMMING (Output)	**0EH**
Bit 15	Last channel indicator bit, active=1
Bit 14	Channel gain select bit 1
Bit 13	Channel gain select bit 0
Bit 12	Analog channel number bit 4
Bit 11	Analog channel number bit 3
Bit 10	Analog channel number bit 2
Bit 9	Analog channel number bit 1
Bit 8	Analog channel number bit 0
Bit 7	Scan list address bit 7
Bit 6	Scan list address bit 6
Bit 5	Scan list address bit 5
Bit 4	Scan list address bit 4
Bit 3	Scan list address bit 3
Bit 2	Scan list address bit 2
Bit 1	Scan list address bit 1
Bit 0	Scan list address bit 0

Bit 15 indicates the last register in the scan list. If this bit is high, the scan-list register pointer will go back to the first scan-list register. If only one A/D channel is used, this bit should be set high.

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Channel gain select:

Bit 14	Bit 13	Gain
0	0	1
0	1	2
1	0	4
1	1	8

Analog channel number selects the next channel to be acquired in a scan sequence.

Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		Channel #
0	0	0	0	0	=	0
0	0	0	0	1	=	1
0	0	0	1	0	=	2
0	0	0	1	1	=	3
0	1	1	1	1	=	15
1	1	1	1	1	=	31

The channel scan list address points to each register in the channel sequence register bank. There are 256 sequence registers. The lower eight bits of the Scan List Programming register are assigned as the register pointer so that each register in the bank can be randomly accessed.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		Register #
0	0	0	0	0	0	0	0	=	0
0	0	0	0	0	0	0	1	=	1
0	0	0	0	0	0	1	0	=	2
0	0	0	0	1	1	1	1	=	15
1	1	1	1	1	1	1	1	=	255

8254 CHANNEL 0 DATA	**10H**
Bit 0 - 7	Timer 0 data

8254 CHANNEL 1 DATA	**12H**
Bit 0 - 7	Timer 1 data

8254 CHANNEL 2 DATA	**14H**
Bit 0 - 7	Timer 2 data

8254 CHANNEL CONTROL WORD	**16H**
Bit 0 - 7	Channel control word

For information on programming the 8254, consult the Intel data book.

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ADC/DAC/TRIG STATUS (Input)	18H
Bit 7	ADC FIFO Full Flag (FF), latched, active=1
Bit 6	ADC FIFO Empty Flag (-EF), latched, active=0
Bit 5	AD DMA transfer done (TC), active = 1
Bit 4	DA DMA transfer done (TC), active = 1
Bit 3	DA FIFO Underrun Flag, active = 1
Bit 2	9513 DONE4, latched, active=1
Bit 1	9513 DONE3, latched, active=1
Bit 0	9513 DONE1, latched, active=1

The ADC FIFO Full Flag is extracted directly from the ADC FIFO memory. This flag is set when the last FIFO memory location is written. The flag is cleared when a FIFO read is performed.

The ADC FIFO Empty Flag (-EF) becomes inactive (logic high) when the ADC conversion has completed (the FIFO is not empty). The flag can be set active (logic low, the FIFO is empty) in two ways: by a subsequent read of the ADC Data register or by writing to bit 4 of the Clear register.

DONE1, DONE3, and DONE4 are flags generated by 9513 terminal count OUT1, OUT3, and OUT4 outputs, respectively. The DONE flag is activated at the rising edge of the OUT signal and can be cleared individually through the Clear register.

CLEAR REGISTER (Output)	1AH
Bit 15 - 10	NC
Bit 9	Clear DAC DMA Transfer Done (TC), active = 1
Bit 8	Clear ADC DMA Transfer Done (TC), active = 1
Bit 7	ADC software start conversion, active=1
Bit 6	NC
Bit 5	Clear DMA transfer done, active=1
Bit 4	Reset A/D FIFO, scan list pointer, -EF, , active=1
Bit 3	Reset D/A FIFO, active=1
Bit 2	Clear 9513 DONE4, active=1
Bit 1	Clear 9513 DONE3, active=1
Bit 0	Clear 9513 DONE1, active=1

Writing a 1 to bit 3 resets the D/A FIFO internal pointers.

By writing a 1 to bit 4, the A/D FIFO is reset, -EF and are cleared, and the channel scan list pointer is reset to the first channel

Writing a 1 to bit 7 starts an A/D conversion.

NONE	**1CH**
NONE	**1EH**

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REGISTER INITIALIZATION

It is good practice to initialize each configuration register upon power up, although the default setting in each register is 0. Make sure that the correct bits in a register are enabled. The registers involved in each specific operation are listed in the following chart. The chart does not include the data registers, scan list programming register, and DMA and interrupt controller registers on the host computer motherboard.

MODE DESCRIPTION	CONFIGURATION REGISTERS AFFECTED				
	9513A (6H)	Control (8H)	DMA/Int (AH)	Status (18H)	Clear (1AH)
A/D operation:					
Scan list initialization		X			
DMA transfer	X		X	X	X
Split-clock acquisition	X	X			
Interrupt driven	X		X	X	X
Software strobe				X	X
D/A operation (I/O):		X			
D/A operation (DMA):					
Asynchronous with A/D	X	X	X	X	X
Synchronous with A/D	X	X	X	X	X
Digital input:	(none required)				
Digital output:					
Asynchronous		X			
D. output inhibit A/D		X			
Synchronous w/ D/A, I/O		X			
Synchronous w/ D/A, DMA		X			

Do not forget to initialize the DMA controller registers and the interrupt controller registers on the host computer motherboard if DMA and/or interrupts are used. The initialization information for these registers is in the *IBM AT Technical Reference Manual* and the *Intel* data book.

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TECHNICAL NOTES

A/D Conversion

Analog Input Impedance

Each of the 32 analog inputs will have an input impedance of 1 megohm when computer power is ON. The input impedance will appear to be *low* when the computer power is OFF. Connected instruments may not work properly. Remember that *OFF is not the same as disconnected*.

Split-Clock Acquisition

Do not forget to initialize the Split Clock Enable bit in the ADC/DAC/TRIG Control register, to initialize both channel 2 and 3 of the 9513A, and to set OUT4 to LOW.

True Hardware-Gated Episodic Acquisition

Make sure the board is not in the Digidata 1200 mode and split-clock acquisition is enabled (both bits 6 and 5 of ADC/DAC/TRIG Control register set HIGH).

D/A Conversion

Channel Alignment

When two channels of D/A are selected, be sure that the memory data is aligned correctly with the D/A channel, *i.e.,* channel 0 data is sent to DAC 0 and channel 1 data is sent to DAC 1. The alignment can be done in *two steps*: first enable the channel that starts first; then enable both channels, through the ADC/DAC/TRIG Control register.

D/A in I/O Mode

In I/O mode, the D/A data bypasses the D/A FIFO buffer and is directly written into the D/A register.

D/A Using DMA

In DMA mode, the D/A data is buffered through FIFO memory. Before D/A operation, the D/A FIFO buffer should first be filled. The filling can be done by using DMA block transfer mode. Note that the D/A FIFO buffer *cannot* be filled through I/O operation.

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9513A Timer

Load/Hold Register

Writing to the Load or Hold register of a timer in the 9513A during its operation will not terminate the current counting process. However, using the Load command **will** terminate the current counting process and force the counter to terminal count (TC).

Load/Hold Register

If output active pulse is programmed, the count can not be 1 when counting down and can not be FFFF when counting up. The pulse width is one clock period and one count will make the output stay at one level. The number of counts should be at least 2.

Master Reset

When resetting the 9513A timer, do not forget to configure for 16-bit bus width.

DONE FF

There is a "DONE Flip-Flop" connected to each of channel 1, 3, and 4 output. The output of DONE FF is the DONE flag. The DONE flag is set at the rising edge of the timer output. If a DONE FF is used, be sure to program its associated timer output with *active high* output at terminal count.

DONE FF

After the DONE flag is set, it will not be cleared until a Clear DONE bit is set through the Clear register. The DONE flag can be read through the Status register.

Output TC Pulse

When the 9513A output is set up for output TC pulse, the output could be left at TC active level. This condition is contrary to its data specification. It occurs while the 9513A is running and "Load & Arm" then "Disarm" is performed. When output TC is left at active high level, the software start conversion strobe will be blocked. It also causes D/A error. To avoid this problem, use TC toggle mode and initiate a "Toggle output low" immediately after the "Disarm" command.

Reference

Advanced Micro Devices 9513A data sheet.

8254 Timer

Count Reading

Although the counters are 16-bit, the count is read 8 bits at a time. While reading the counters, the software overhead time may cause erroneous readings. The best way to read the count is to use the counter latch command which causes all three counters to be latched at the same time. Each counter can then be read at any time.

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Hardware Connection

The output of channel 0 is connected to the clock input of channel 1, and the output of channel 1 is connected to the clock input of channel 2. All three channels are cascaded for one 48-bit counter.

References

The programming reference is the Intel 8254 data book. There are also many other microprocessor "cookbooks" which give programming tips.

Digital Outputs

Digital Output 0 (D0)

Normally a digital output. When "Digital Out Inhibit ADC" bit is enabled in the ADC/DAC/TRIG Control register, D0 high inhibits ADC conversion. The inhibiting signal (D0 high) is also available at Digital Output 0.

DMA Controller

Remember to *clear* First/Last Flip-Flop prior to loading current address and count.

Programming Order

Be sure to initialize the DRQ channel in the DMA/INT Configuration register *before* you unmask the DMA channel. Otherwise the computer may hang.

DMA Controller #2

Controller #2 is for 16-bit transfers so that the address lines are *shifted* over one position to perform transfers on the even boundaries. The first address bit is connected to A1 of the PC/AT bus (instead of A0). Please keep this in mind when programming the Current Address register.

DMA Controller #2 Mask

Do not mask DMA channel 4 (first channel of controller #2). It is used for memory-to-memory transfers and it is programmed by DOS and other application programs.

DMA Controller Command Register, Priority

In the fixed-priority mode, channel 5 has the highest priority and 7 has the lowest priority. To prevent any channel from monopolizing the system, the DMA controller can be programmed in rotating-priority mode. In the rotating-priority mode, the last-serviced channel has the lowest priority. Unfortunately, testing by Axon Instruments has revealed that the rotating-priority mode on a 386 computer with an OPTi chipset seems to be prohibited because the computer locks up; apparently only the fixed-priority mode can be used. This is not be a problem for Digidata running at 330 kHz with simultaneous dual DMA channels. The DMA transfers are done in bursts to and from the FIFOs; there is enough time between transfers to allow the other channel to perform and complete a transfer.

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DMA Controller Command Register

When simultaneous A/D and D/A DMA is enabled and when A/D is set up in ADC DMA FIFO not-empty mode transfer, set the DMA command register in the "fixed priority" mode and set D/A DMA with high priority.

DMA Controller Command Register, Timing

In the compressed-timing mode, the DMA transfer time can be shortened from 3 clock cycles to 2. On some computers, the programming of compressed timing is ignored, but on others it locks the system up. The safest action is to leave the timing on "normal."

Interrupt Controller

Interrupt Software Overhead Time

With the least amount of the software code necessary (in maskable-interrupt mode), the IRQ line can be driven at about 1 kHz on a 6 MHz IBM AT if the source code is in C language. The software overhead time can be greatly reduced when the code is written in assembly language.

Register Settings

DMA/Interrupt Configuration

It is illegal to program both ADC and DAC to the same DMA channel. The illegal codes for the four lowest bits are: 5H, AH, and FH.

DMA/Interrupt Configuration

Upon power up, you should initialize by setting this register to 0H. This will disable the DMA and interrupt lines so that false DMA or INT triggering will not occur.

Clear Register

When clearing all the flags and counter registers, be sure to send FF7FH to the Clear register. Bit 7 is used to start ADC conversion and activating this bit will consequently set the ADC FIFO -EF flag high (FIFO buffer not empty).

General

Initialization Recommendation

Writing a software initialization procedure for each feature implementation is a good idea. This should simplify the software design.

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TROUBLESHOOTING

If you have any problem with the operation of the Digidata 1200B, follow this section to check out some possible problems and solutions. If your problem is still not solved, **please go through the "Before You Call" checklist on the next page before you call**.

1. If you suspect that the Digidata is not working properly, isolate the problem! Disconnect any external instruments and test the Digidata by itself. If you suspect problems with the analog or digital outputs, use a voltmeter or oscilloscope to monitor the signal. If you suspect a problem with the analog or digital inputs, hook up a known signal source such as a signal generator, or even the analog output if you know it is working properly.

2. **The Digidata appears to be working, but no analog input signals are being drawn on the computer screen.**

   Check the following: 1) Set your Axon Instruments software for a **display gain of 1**, which allows the whole analog input range to be seen on screen; 2) Make sure that the signal amplitude and offset keeps the signal within the analog input range, which is ±10 volts (divided by the programmable gain setting).

3. **The screen shows a straight line instead of the input signal.**

   Are all external connections properly made? Check cables for continuity problems. Make sure the Digidata cable is securely attached to both the board and the interface.

4. **Noise is introduced when the data is digitized.**

   If noise is added to the signal on the analog input, make sure that all cables are routed away from switching power supplies, power cords, monitors, or any other major sources of noise. Check for proper ground connections. See the **INSTALLATION** chapter for proper ground connections.

5. **There is increased noise on an analog input channel when a square wave is connected to an adjacent input channel.**

   Like all digitizing systems, the Digidata is only intended to sample data that has been lowpass filtered at half the sampling rate or lower. Irrespective of the fundamental frequency of a square wave, there are higher frequencies associated with the transitions. For example, a square wave that has a rise and fall time of several tens of nanoseconds contains frequency components of many megahertz. When the square-wave output of a function generator is directly connected to an analog input, the high-frequency components of the transitions will couple into the other analog input channels. This is normal. The solution is to first pass the square-wave signal through a lowpass filter.

6. **If rapidly repeating pulses are connected to a digital input or trigger input, random noise spikes occasionally occur on the analog input.**

   In normal operation, it is expected that a single trigger pulse will be applied to the Sweep Start input in order to initiate a sweep acquisition. If a square wave is connected to the Sweep Start input and maintained during the sweep acquisition, the edges of the trigger signal may couple into the analog inputs. Similarly, the digital inputs are designed to be polled before a sweep

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acquisition, not during it. The solution to these potential cross-talk problems is to avoid applying inappropriate repetitive waveforms to these inputs. For example do not apply rapidly repeating trigger pulses to the Sweep Start input during sweep acquisition, even if the software is not looking for a Sweep Start trigger.

7. **The Digidata does not work at all or it locks up the computer when doing certain operations.**

   Make sure the software is configured properly for the board's I/O address. Check for other software conflicts (see item 8 below). Refer to the **INSTALLATION** chapter to verify that the board is installed properly. There may be a conflict with other plug-in boards installed in the computer. Pull out all non-essential boards and test the Digidata. Check the other boards to determine the I/O addresses, DMA channels, and IRQs being used.

8. When troubleshooting the Digidata or your software, it is best to simplify your software configuration by disabling all device drivers and memory-resident programs in the CONFIG.SYS and AUTOEXEC.BAT files. Just use the REM statement to turn these lines into "remarks," then re-boot the computer and see if the problem still exists.

9. Run the TESTDIGI software and go through the Functional Checkout on page 7.

Before you call. . .

Please write down the following information before you call for technical support. This information can help us identify possible problems and will quickly expose known conflicts.

1. What is the serial number of the Digidata board? (To check for known revision-specific problems).

2. Gather the following computer information: The brand and model of computer you use; the type (i.e., 486 or Pentium) and speed of the microprocessor (i.e., 266 MHz); how much RAM is installed; what version of MS-DOS is loaded; whether you are using a memory manager such as 386MAX, QEMM386, or the memory managers that come with MS-DOS 5.0 or Windows 3.X.

3. What other boards are installed in the computer? (i.e., network board, tape drive controller, mouse bus board, etc). If possible, find out what I/O addresses, DMA channels and IRQs are being used.

4. Write down or print out the contents of the CONFIG.SYS and AUTOEXEC.BAT files in the root directory.

5. Run through all the functions in the TESTDIGI Digidata test program and record the results.

6. If you can reproduce a problem by following a series of steps using software, record these steps so that we may attempt to reproduce the problem.

After following these steps, call Axon Instruments at the number printed at the front of this manual.

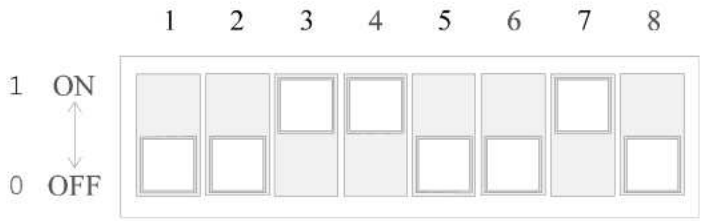
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CONFIGURATION AND CALIBRATION

Setting the Base I/O Address

The base I/O address of the Digidata board is set with switch block SW1. The default address is 320 hex. The following table gives the valid I/O addresses.

Switch Block SW1



Hex addr	Switch Position							
	1	2	3	4	5	6	7	8
100	0	0	0	1	0	0	0	0
120	0	0	0	1	0	0	1	0
140	0	0	0	1	0	1	0	0
160	0	0	0	1	0	1	1	0
180	0	0	0	1	1	0	0	0
1A0	0	0	0	1	1	0	1	0
1C0	0	0	0	1	1	1	0	0
1E0	0	0	0	1	1	1	1	0
200	0	0	1	0	0	0	0	0
220	0	0	1	0	0	0	1	0
240	0	0	1	0	0	1	0	0
300	0	0	1	1	0	0	0	0
320	0	0	1	1	0	0	1	0
340	0	0	1	1	0	1	0	0

Calibration

The Digidata 1200B comes from the factory fully calibrated. Over time, the D/A and A/D circuitry will experience some drift and will need to be recalibrated. The only equipment required is a precision digital voltmeter and a small flat-head screwdriver. The Digidata 1200B board has trim pots for adjusting the offset and gain settings. Remove the computer cover to gain access to the pots. Turn on the computer and let the system warm up for an hour before beginning the calibration procedure.

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Top view of Digidata board



RT1 = DAC1 gain
RT2 = DAC1 offset
RT3 = DAC0 gain
RT4 = DAC0 offset
RT5 = ADC gain
RT6 = ADC offset

The D/A converters will first be calibrated using the voltmeter, then a DAC will be used as the voltage source to recalibrate the A/D converter.

Calibrate the D/A Converters

Run the TESTDIGI program. Hook up the voltmeter to the DAC1 output and set the voltmeter to measure down to the millivolt range. The D/A converters have a resolution of 5 mV per DAC unit.

1. Using the TESTDIGI program, set the DAC1 output to 0 volts. While observing the voltmeter, adjust DAC1 offset trim pot RT2 until a reading of 0.000 V appears.

2. Set the DAC1 output to 10.000 volts (2000 or 7D0H D/A units). While observing the voltmeter, adjust DAC1 gain trim pot RT1 until a reading of 10.000 V appears.

3. Repeat steps 1 and 2 until the pots no longer need to be adjusted.

4. Hook up the voltmeter to the DAC0 output and repeat steps 1, 2, and 3 for DAC0 using DAC0 offset trim pot RT4 and DAC0 gain trim pot RT3.

Calibrate the A/D Converter

Connect DAC0 directly to ADC0.

1. Choose the TrimMode function in TESTDIGI and set the Output voltage to 0 volts. Adjust ADC offset trim pot RT6 until the screen reads 0.000 volts.

2. Hit the <Esc> key to exit TrimMode and choose TrimMode once again, setting the Output voltage to 10.000 volts (2000 or 7D0H D/A units). Adjust ADC gain trim pot RT5 until the screen reads 10.000 volts (2000 or 7D0H A/D units).

3. Repeat steps 1 and 2 until the pots no longer need to be adjusted.

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SPECIFICATIONS

Analog Input

Number of input channels	32 single-ended
Resolution	12-bit, 1 in 4096
Integral linearity error	< ±1/2 LSB
Differential nonlinearity	< ±1 LSB
Acquisition rate (aggregate)	333 kHz
Input range	-10.24 V to +10.23 V
Input bias current	<50 pA @ 25°C
Initial input offset current	<25 pA @ 25°C
Drift vs. temperature	<10 ppm/°C
Input impedance	10 GΩ || 3 pF
Input CMRR	>80 dB
Gain values	1, 2, 4, & 8
Gain error	0.05% typical
Signal-to-noise ratio	65 dB

Analog Output

Number of channels	2
Resolution	12-bit
Integral linearity error	< ±1/2 LSB
Differential nonlinearity	< ±3/4 LSB
Output settling time	3 μsec for 10 V step
Output slew rate	10 V/μsec
Gain drift	±5 ppm/°C
Bipolar zero drift	±3 ppm of FSR/°C
Internal voltage reference	10 V
Output voltage ranges	-10.24 V to +10.23 V
Output current drive capability	±5 mA
Output impedance	0.2 Ohm at DC
Output short circuit to signal ground	Indefinite

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Timing Input/Output

9513A timer:

Number of channels	5 channels
Counter resolution	16-bit
Base clock rates available	4 MHz, 400 kHz, 40 kHz, 4 kHz, & 400 Hz
Gate inputs	3, TTL edge/level programmable
External trigger input	1

8254 timer:

48-bit real-time clock	250 ns resolution

Digital Inputs

Number of bits	8
Input type	TTL compatible

Digital Outputs

Number of bits	8 asynchronous, 7 when A/D inhibit feature is used or 4 synchronous; 3 when A/D inhibit feature is used
Output driver	HC compatible
Output current	25 mA

DMA

Number of channels	2, one each for A/D & D/A
Data transfer width	16-bit

FIFO Memory

A/D FIFO data buffer	8192-sample capacity
D/A FIFO data buffer	8192-sample capacity

TRIGGER IN

TAG, START	2 channels (input duration must be greater than one sample)

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INTERFACE DESCRIPTION

The standard Digidata 1200B BNC interface box is described here. For descriptions of the other interface options, see the instruction sheets included with those items.

1200-BNC Interface Box

All Digidata 1200B input and output signals are brought to an end connector on the plug-in board. The 1200-BNC interface box allows the user to send analog and digital signals to and from the Digidata 1200B. The interface box is linked to the Digidata 1200B board by a 10-foot shielded cable.

The **front panel** connectors are all BNCs. The signal types are listed in the next section. There is an LED which indicates that the acquisition board is powered up and the connection is made with the interface box. The BNC shields for the Analog Inputs are connected to the Analog Return line. The shields for the rest of the BNC connectors are connected to analog ground (Analog GND).

There are three types of connectors on the **rear panel** of the interface box: eight BNCs, two 37-D-SUB connectors, and one 68-pin high-density connector. See the next section for pin assignments. All BNC shields are connected to Analog GND.

CONNECTOR PIN ASSIGNMENTS

1200-BNC Interface Front Panel BNC

Analog Output 0 - 1	2
Analog Input 0 - 15	16
Digital Output 0 - 5	6
Tag, SweepStart	2
Total	26

1200-BNC Interface Rear Panel BNC

Digital Input 0 - 1	2
Digital Output 6 - 7	2
9513A Gate 1, 3, 5	3
9513A Out 5	1
Total	8

Note: All BNC shields connect to Analog GND except the Analog Inputs, which connect to Analog Return.

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High-Density D-Subminature 68-Pin Conductor Connector 1200B-BD, 1200-BNC

DESCRIPTION	PIN#	PIN#	DESCRIPTION
Analog Return	1	2	Analog In 0
Analog In 1	3	4	Analog In 2
Analog In 3	5	6	Analog In 4
Analog In 5	7	8	Analog In 6
Analog In 7	9	10	Analog In 8
Analog In 9	11	12	Analog In 10
Analog In 11	13	14	Analog In 12
Analog In 13	15	16	Analog In 14
Analog In 15	17	18	Analog GND
Analog GND	19	20	Digital GND
Digital Out 1	21	22	Digital Out 3
Digital Out 5	23	24	Digital Out 7
Digital In 6	25	26	Digital In 4
Digital In 2	27	28	Digital In 0
Sweep Start In/9513 Gate 4	29	30	9513 Gate 1
9513 Source 4	31	32	9513 Source 2
ADC Clock In	33	34	9513 Out 5
Analog Return	35	36	Analog In 16
Analog In 17	37	38	Analog In 18
Analog In 19	39	40	Analog In 20
Analog In 21	41	42	Analog In 22
Analog In 23	43	44	Analog In 24
Analog In 25	45	46	Analog In 26
Analog In 27	47	48	Analog In 28
Analog In 29	49	50	Analog In 30
Analog In 31	51	52	Analog Out 0
Analog Out 1	53	54	Tag In
Digital Out 0	55	56	Digital Out 2
Digital Out 4	57	58	Digital Out 6
Digital In 7	59	60	Digital In 5
Digital In 3	61	62	Digital In 1
9513 Gate 5	63	64	9513 Gate 3
9513 Source 5	65	66	9513 Source 3
9513 Source 1	67	68	Non-isolated +5V

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1200-BNC Interface Rear Panel D-SUB-37, "Analog Inputs (32)" (Female)

DESCRIPTION	PIN#		DESCRIPTION
Analog In 0	1	20	Analog In 19
Analog In 1	2	21	Analog In 20
Analog In 2	3	22	Analog In 21
Analog In 3	4	23	Analog In 22
Analog In 4	5	24	Analog In 23
Analog In 5	6	25	Analog In 24
Analog In 6	7	26	Analog In 25
Analog In 7	8	27	Analog In 26
Analog In 8	9	28	Analog In 27
Analog In 9	10	29	Analog In 28
Analog In 10	11	30	Analog In 29
Analog In 11	12	31	Analog In 30
Analog In 12	13	32	Analog In 31
Analog In 13	14	33	Analog Return
Analog In 14	15	34	N/C
Analog In 15	16	35	N/C
Analog In 16	17	36	N/C
Analog In 17	18	37	N/C
Analog In 18	19		

1200-BNC Interface Rear Panel D-SUB-37, "Digital I/O" (Male)

DESCRIPTION	PIN#		DESCRIPTION
Digital Out 0	1	20	Digital Out 1
Digital Out 2	2	21	Digital Out 3
Digital Out 4	3	22	Digital Out 5
Digital Out 6	4	23	Digital Out 7
Analog GND	5	24	Analog GND
Digital In 0	6	25	Digital In 1
Digital In 2	7	26	Digital In 3
Digital In 4	8	27	Digital In 5
Digital In 6	9	28	Digital In 7
Analog GND	10	29	Analog GND
9513 Gate 1	11	30	ADC Clock
9513 Gate 3	12	31	9513 Sweep Start In
9513 Gate 5	13	32	Tag In
Analog GND	14	33	Analog GND
9513 Source 1	15	34	9513 Source 2
9513 Source 3	16	35	9513 Source 4
9513 Source 5	17	36	9513 Out 5
N/C	18	37	N/C
N/C	19		

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WARRANTY

We warrant every Digidata 1200B to be free from defects in material and workmanship under normal use and service. For 12 months from the date of receipt we will repair or replace without cost to the customer any of these products that are defective and which are returned to our factory properly packaged with transportation charges prepaid. We will pay for the return shipping of the product to the customer. If the shipment is to a location outside the United States, the customer will be responsible for paying all duties, taxes and freight clearance charges if applicable.

Before returning products to our factory the customer must contact us to obtain a Return Merchandise Authorization (RMA) and shipping instructions. Failure to do so will cause long delays and additional expense to the customer.

This warranty shall not apply to damage resulting from improper use, improper care, improper modification, connection to incompatible equipment, or to products which have been modified or integrated with other equipment in such a way as to increase the time or difficulty of servicing the product.

This warranty is in lieu of all other warranties, expressed or implied.

Axon Instruments, Inc.

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PROBLEMS AND SUGGESTIONS REPORT

Copy this form. Fill out and mail or fax to:

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Axon Instruments, Inc.
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Foster City, CA 94404, USA

Neatly print your name and address in the box below.

Product: _____

Version: _____ **Serial No.** _____

Computer Make _____ Model: _____

Monitor: _____

Memory size: _____ MB Operating System Vers: __

Speed: _____ MHz

Disk size: _____ MB

Phone: _____

Fax: _____

Acquisition hardware: _____

Other Axon hardware: _____

Description:

Please describe the problem or suggestion and how it can be reproduced. Enclose printouts, figures or data files if helpful. List any error messages and symptoms.

Date: _____

Use continuation pages if necessary.

Axon use only.

Date received: _____ answered: _____ closed: _____ ☐ Product Manager

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