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EK-RL012-UG-005

RL01/RL02 User Guide

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EK-RL012-UG-005

RL01/RL02 User Guide

Prepared by Educational Services
Digital Equipment Corporation

1st Edition, December 1978
2nd Printing (Rev), September 1979
3rd Printing (Rev), June 1980
4th Printing (Rev), October 1980
5th Printing (Rev), September 1981

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CHAPTER 1
INTRODUCTION

1.1 PURPOSE AND SCOPE

This manual provides information on the capabilities, installation, operation, and programming of the RL01/RL02 disk subsystem. A basic subsystem is comprised of one RL11, RLV11, RLV12, or RL8A controller and up to four RL01 or RL02 disk drives.

This manual is intended primarily for operating and programming personnel. Service should be performed only by qualified Digital field engineering and maintenance personnel. A prerequisite for understanding this manual is a basic knowledge of PDP-8 and/or PDP-11 processors and peripherals.

1.2 REFERENCE DOCUMENTS

Table 1-1 lists the documents that provide the information necessary for a complete understanding of the function, theory, and maintenance of the RL01/RL02 disk drives and the controllers. The UNIBUS and LSI-11 Bus are described in the *PDP-11 Bus Handbook* (EB-17525). The OMNIBUS is described in the *PDP-8A Miniprocessor User's Manual* (EK-8A002-MM).

Table 1-1 Reference Documents

Title	Document No.
RL01/RL02 Disk Drive T[illegible]cal Manual	EK-RL012-TM
RL01 Disk Drive Illu[illegible] Parts Breakdown	EP-00016-IP
RL02 Disk Drive [illegible]ted Parts Breakdown	EP-00016-IP
RL01/RL02 [illegible]osystem Preventive Maint[illegible]Manual*	EP-00008-PM
RL01/R[illegible]02 Disk Drive Pocket Service Guide	EK-RL012-PG
RL11 Controller Technical Description Manual	EK-0RL11-TD
RLV11 Controller Technical Description Manual	EK-RLV11-TD
RL8A OMNIBUS Controller Technical Manual	EK-0RL8A-TD
RLV12 Disk Controller User's Guide	EK-RLV12-UG
RLV12 Controller Technical Description Manual	EK-RLV12-TD

* This document is only available to Digital Equipment Corporation Service personnel.

1.3 SUBSYSTEM DESCRIPTION

The RL01/RL02 mass storage subsystem is based on the RL01K/RL02K disk cartridges, the RL01/RL02 drive unit(s), and an appropriate controller such as the RL11 (PDP-11), RLV11 or RLV12 (LSI-11), or RL8A (PDP-8). The basic subsystem is illustrated in Figure 1-1.

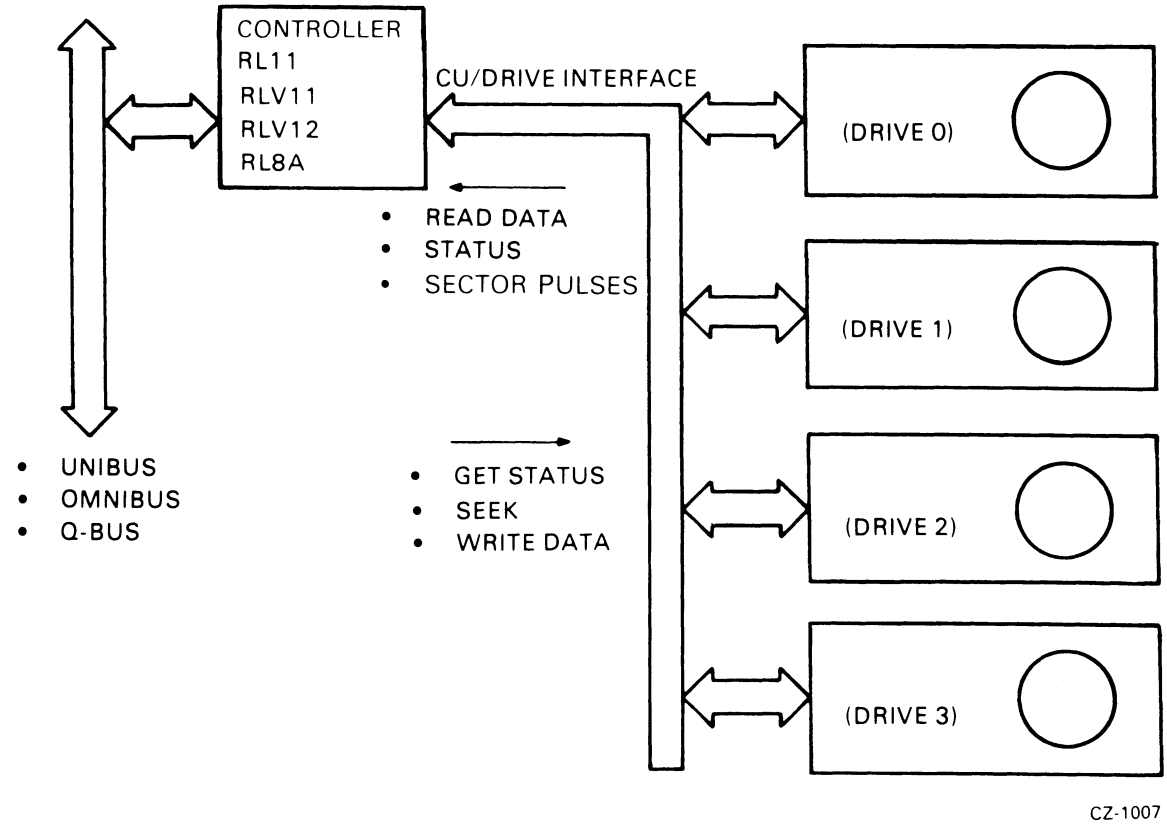


Figure 1-1 Typical RL01/RL02 Mass Storage Subsystem Configuration

1.3.1 RL01/RL02 Disk Drive

The RL01/RL02 drive unit is built into a chassis that slides out of the cabinet to allow operator access to the top cover for loading and unloading of the disk cartridge. If the stops on the slide are manually released, the chassis can be pulled farther out so that the rear top cover can be removed for servicing. The front panel contains operator controls and indicators.

The chassis contains a spindle, two read/write heads mounted on a positioner, logic modules, a power supply with an ac power cord and circuit breaker, a closed-loop clean air system, a cooling air system, appropriate safety interlocks, and connectors for the I/O cable(s).

The drive unit is shown in Figure 1-2.

The RL02 drive unit has a label reading "RL02" on the front panel. The RL01 drive currently does not have a label identifying it as an RL01.

1.3.2 RL Controllers

There are four controllers available for the RL01/RL02 subsystem. All can handle up to four drives and all feature Direct Memory Access (DMA) operation.

1.3.2.1 RL11 Controller Description – The RL11 controller consists of a single, hex-height Small Peripheral Controller (SPC) module designated M7762. It is used to interface the drive with the PDP-11 UNIBUS. The data is formatted in 16-bit words.

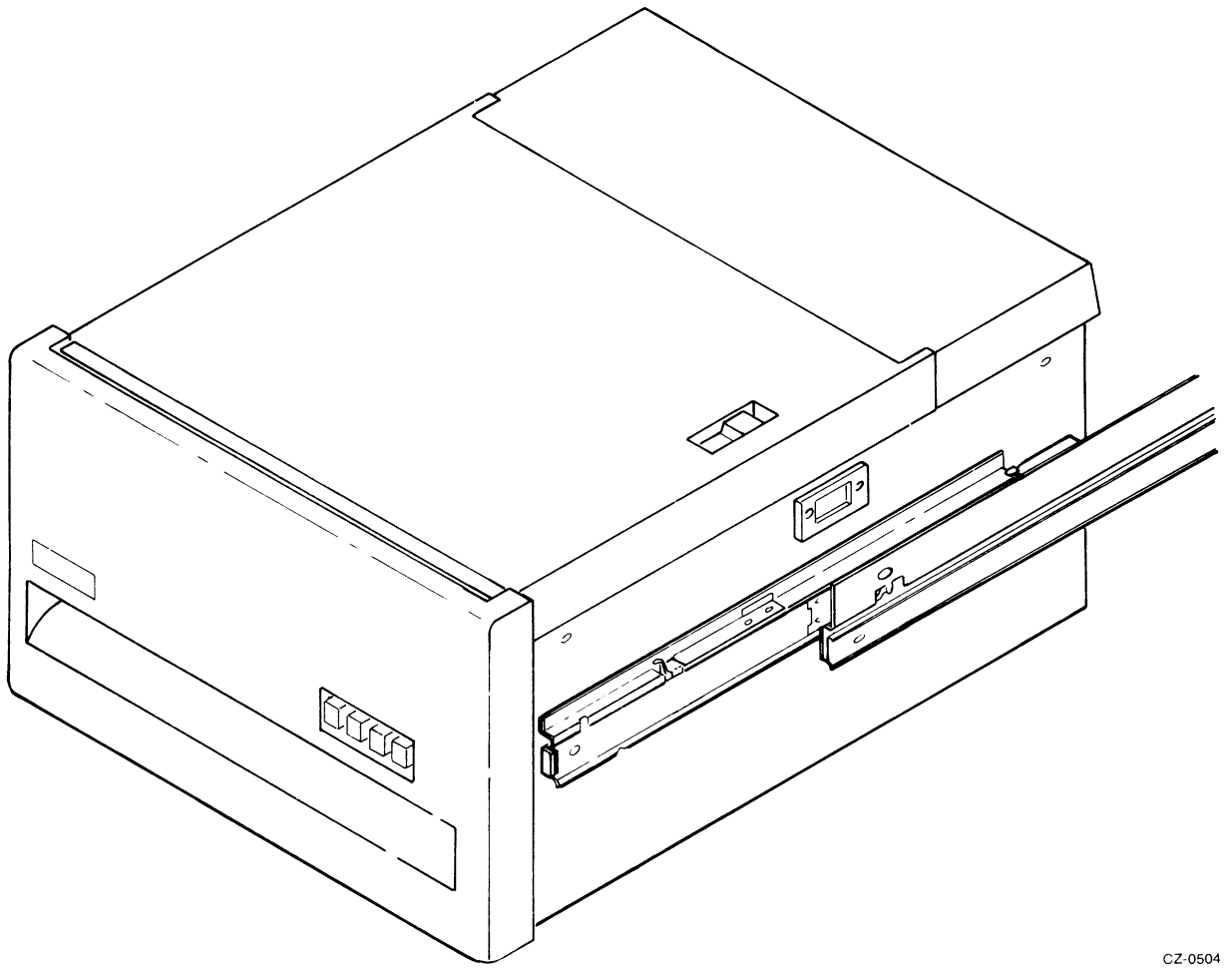


Figure 1-2 RL01/RL02 Disk Drive

1.3.2.2 RLV11 Controller Description – The RLV11 controller consists of two quad-height modules designated M8013 and M8014. This controller interfaces the drive with the LSI-11 Bus. The data is formatted in 16-bit words. The controller can handle any combination of up to four RL01/RL02 drives.

1.3.2.3 RL8A Controller Description – The RL8A controller consists of a single, hex-height module designated M8433. It is used to interface the drive with the PDP-8 OMNIBUS. The data can be formatted in either 8-bit bytes or 12-bit words. This controller has a jumper-determined choice of handling RL01 or RL02 drives. However, in the RL02-jumpered configuration, it can handle any combination of up to four RL01/RL02 drives.

1.3.2.4 RLV12 Controller Description – The RLV12 controller consists of a single, quad-height module designated M8061. It is used to interface the drive with either the extended LSI-11 Bus or the standard LSI-11 Bus. A jumper designates the 22-bit or 18-bit addressing scheme. The data is formatted in 16-bit words. This controller can handle any combination of up to four RL01/RL02 drives.

1.3.3 RL01K/RL02K Disk Cartridge

The RL01K or RL02K is a removable, top-loading 5440-type disk cartridge that is formatted in a manner unique to the RL01/RL02 subsystem. Both cartridges contain a single platter. The RL01K cartridge has a capacity of 5.2 megabytes of user data, and the RL02K cartridge holds 10.4 megabytes of data. Both sides of the platter are used for data. There are 256 tracks on each RL01K platter surface and 512 tracks on each RL02K platter surface. Each track is divided into 40 sectors. Each sector contains 256 bytes of data. The last track of the last surface is reserved for the cartridge serial number and bad sector information. Head positioning servo information and header information are prerecorded at the factory and cannot be reformatted in the field. This information, along with the data, is read by the read/write heads but the internal logic of the drive unit protects the servo and header information from being overwritten.

1.3.3.1 Interchangability – The RL01K and RL02K disk cartridges are not functionally interchangable although they are physically interchangable. It is possible to mount an RL01K cartridge on an RL02 drive, for example, but proper operation will not occur. An RL01K cartridge written on an RL01 unit can be read on any other RL01 unit even if that unit is controlled by a different type of controller. The limitation to this interchangeability is that if an RL8A controller is used to write data and the cartridge is to be used by an 11-Family controller, the RL8A must use the 8-bit byte mode of operation.

An RL02K cartridge written on an RL02 unit can be read on any other RL02 unit (assuming the same conditions mentioned above).

1.3.3.2 Sector Format – As shown in Figure 1-3, each sector contains:

- Servo information for head positioning,
- Header (address) information,
- Data (128 words of 16 bits or 256 bytes of 8 bits or 170 words of 12 bits).

Only the data portion of a sector can be written by the user. The servo and header information is protected by the drive logic and controller to ensure disk integrity and cannot be written in the field.

Each sector starts with a sector pulse that is produced by a sector transducer mounted on the drive unit. It senses the sector notches that are machined into the hub of the disk cartridge.

During the time that the sector notch passes by the sector transducer, the heads detect two servo pulse bursts (S1 and S2) that are prerecorded on the platter. These servo bursts are used by the drive logic for head positioning.

The header follows the servo pulse bursts. It consists of:

- A preamble of three words – 47 "0" bits and one "1" bit,
- A word that contains the address – sector, head, and cylinder,
- A word of all zeros,
- A word containing information created by the Cyclic Redundancy Check (CRC) logic,
- A one-word postamble of all zeros.

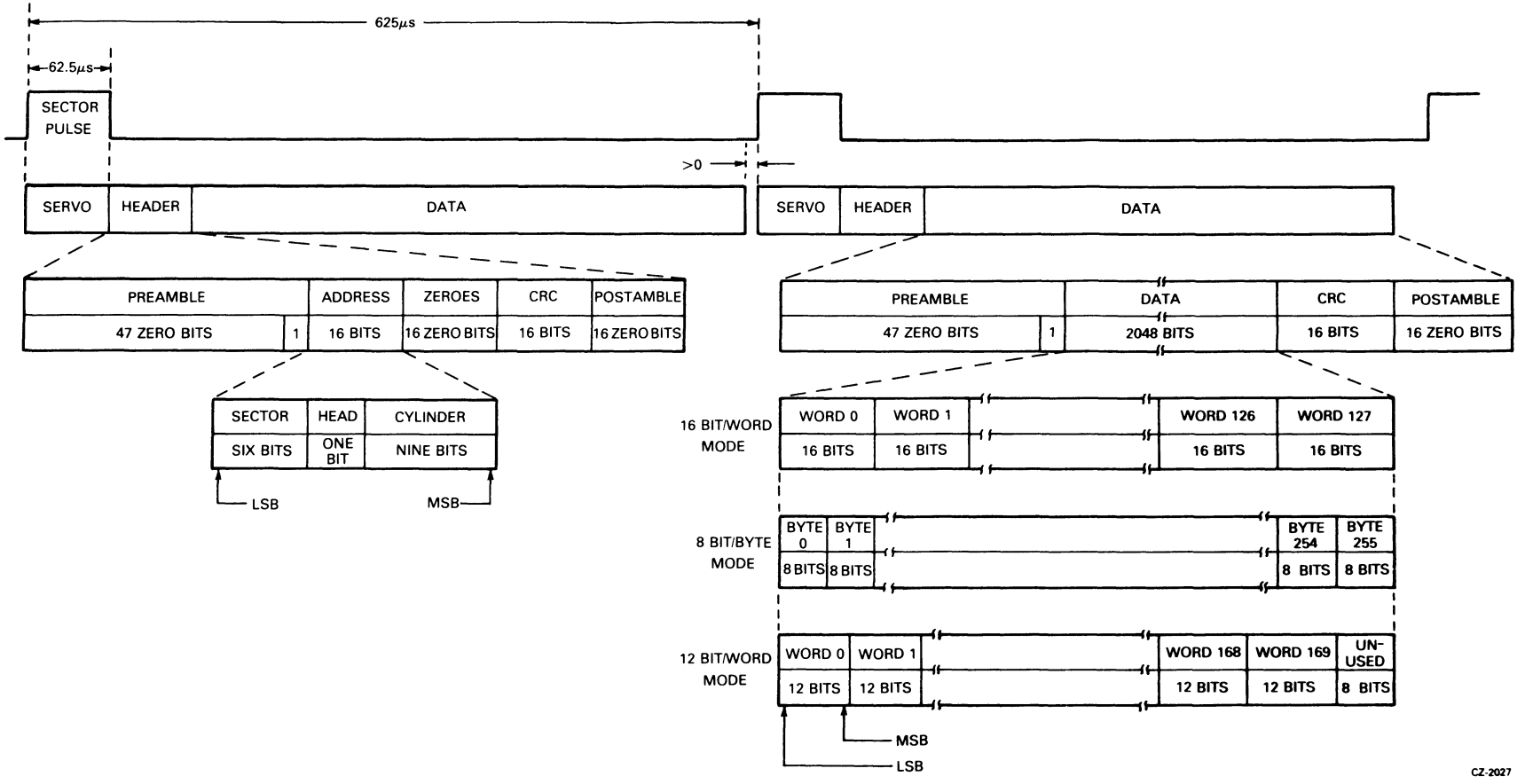


Figure 1-3 RL01K/RL02K Disk Cartridge Format

The user writeable data area follows the header. It consists of:

- A preamble of three words – 47 "0" bits and one "1" bit,
- Data (128 words of 16 bits or 256 bytes of 8 bits or 170 words of 12 bits),
- A word containing CRC-generated information,
- A one-word postamble of all zero bits.

Following each sector is a period of idle time that is simply a wait for the next sector pulse.

In addition to the data tracks, there are tracks both inside and outside of the data area that contain unique servo signals that define those areas as guard bands. If the read/write heads attempt to enter a guard band, the drive logic causes the positioner to retreat from the guard band and return to the data area.

The disk has a nominal rotational speed of 2400 rev/min. Therefore, the time for one revolution is 25 milliseconds. Since the revolution is divided into 40 sectors, the duration of each sector is 625 microseconds. This 625 microsecond period is divided into non-data (sector pulse, header, idle time) time and data time. The data time period is 500 microseconds. Thus, the data is transferred in 500 microsecond bursts that occur every 625 microseconds.

For 16-bit word mode there are 128 words of data in a sector so the peak transfer rate is 3.9 microseconds per word and the average transfer rate is 4.9 microseconds per word.

For 8-bit bytes (256 bytes per sector), the peak transfer rate is 1.9 microseconds per byte and the average transfer rate is 2.4 microseconds per byte.

For 12-bit word mode (170 words per sector), the peak transfer rate is 2.9 microseconds per word and the average transfer rate is 3.7 microseconds per word.

1.4 SECTOR LOCATION

The RL01K/RL02K disk cartridges do not have a physical index notch (occurring once per revolution) machined into the hub as some cartridges do. The controller determines the rotational position of the disk cartridge by reading, from the header, the sector address as well as the head (surface) and cylinder (track) addresses. Thus, the cartridge does not need a physical index. The sectors are relocated to optimize the data transfer rate when it becomes necessary to perform a seek during a data transfer.

A head switch to the other surface is considered a seek because the RL01/RL02 subsystem uses servo information that is recorded on each track. The newly selected head will position itself over the center of the track. There is no hardware-controlled implicit seek on the RL01/RL02 subsystem. All seeks, including spiral (mid-transfer) seeks, must be programmed into the software. The correct head must be selected and positioned over the correct track by a seek operation before the software can initiate a data transfer.

When the end of a track is reached and the data transfer has not been completed, the software must do one of two things. It must switch to the head that is over the corresponding track on the other surface (6.5 milliseconds average, 8 milliseconds maximum) or the software must issue a seek to the next cylinder (15 milliseconds). If the head is to be switched also, the seek and the head switching are normally combined. Once the unit has completed the seek operation, the software can continue the data transfer.

To reduce the rotational latency following a head switch seek, surface one is offset by 17 sectors from surface zero. The eight milliseconds head switch corresponds to 13 sectors of this offset and the additional four sectors allow for software overhead.

To reduce the rotational latency following a one cylinder seek (with head switch), surface 0 of a cylinder is offset by 29 sectors from surface 1 of the previous cylinder. The 15 millisecond seek time takes 24 sectors of this offset and five more sector times are allowed for software overhead.

These two offset patterns are illustrated in Figures 1-4 and 1-5.

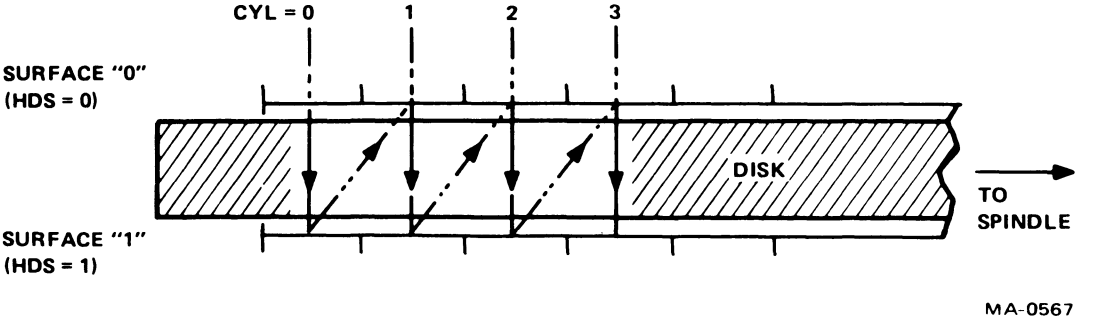


Figure 1-4 Access Method for Sequential Transfers

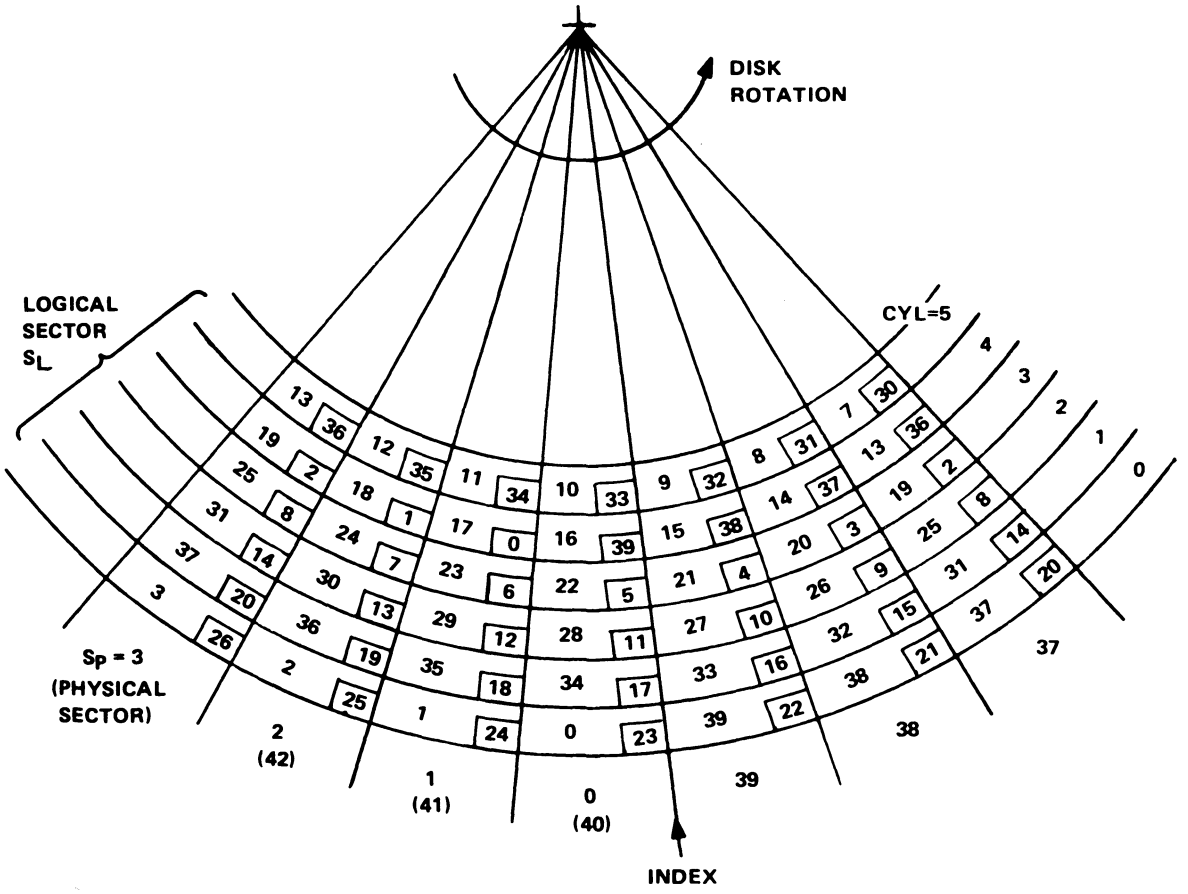


Figure 1-5 Sector Relocation

1.5 BAD SECTOR FILE

The Bad Sector File is a list of all bad sectors found on an RL01K/RL02K disk cartridge. It also contains the cartridge serial number. The operating system uses this information to avoid allocating bad sectors to a user's files.

If there is an error in a header, or if there are 16 consecutive read/write errors within one sector, that sector is defined as a bad sector.

This file is recorded on surface 1, track 255 (decimal) of an RL01K cartridge, and surface 1, track 511 (decimal) of an RL02K cartridge. The file consists of 40 sectors of 128 words each. Figure 1-6 shows the format of the Bad Sector File.

There is room in the file for 128 entries written by the factory and for 128 entries that can be written in the field if bad sectors develop during field use.

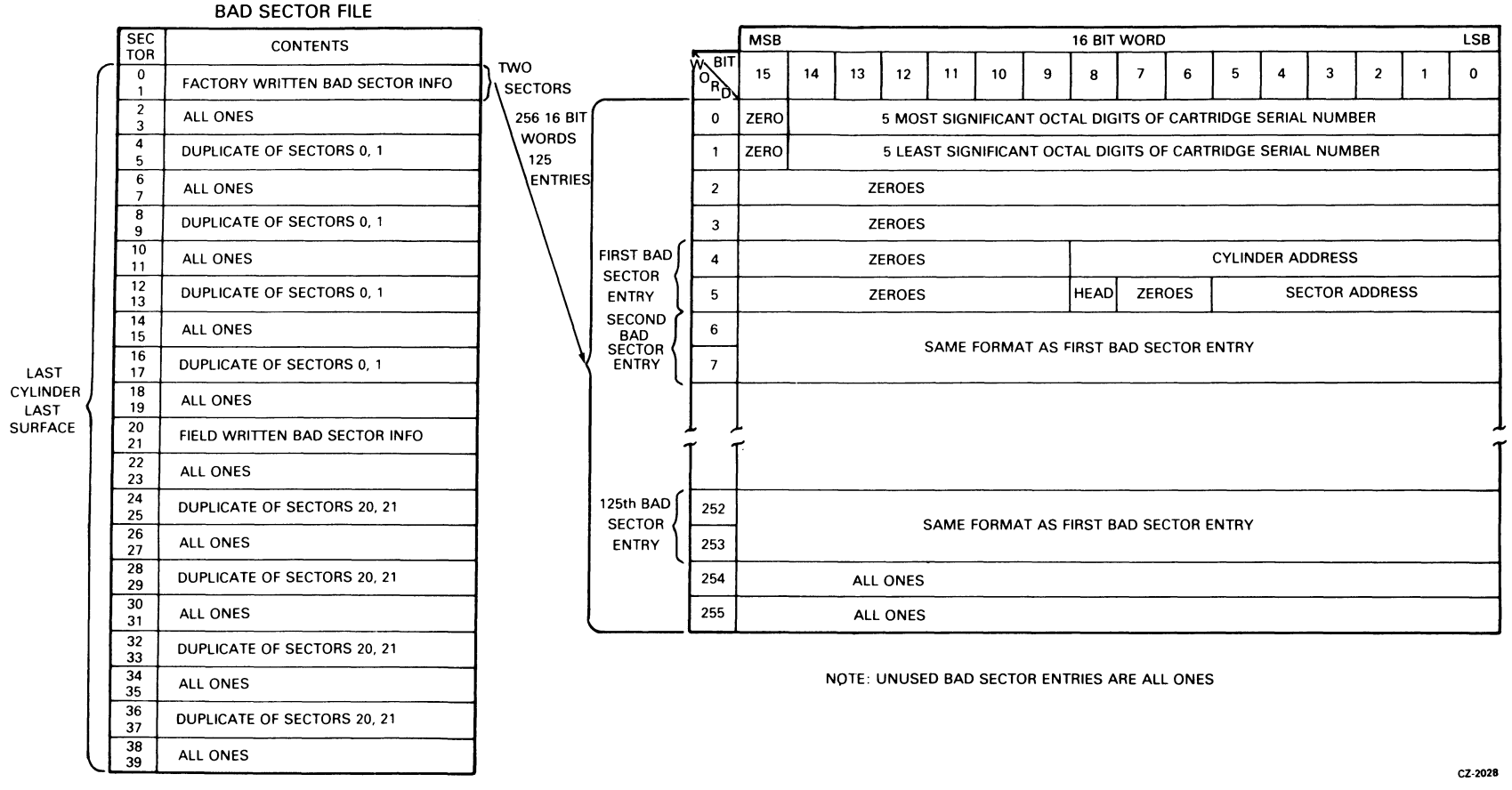


Figure 1-6 Bad Sector File Format

1.6 RL01/RL02 SPECIFICATIONS

The following tables list the specifications of the RL01/RL02 drives and the RL01K/RL02K cartridges.

1. Table 1-2 RL01/RL02 Disk Drive Physical and Environmental Specifications
2. Table 1-3 RL01K/RL02K Disk Drive Operational Specifications
3. Table 1-4 RL01K/RL02K Disk Cartridge Specifications

Table 1-2 RL01/RL02 Disk Drive Physical and Environmental Specifications

Characteristics	Specifications
Width	Compatible with 19 inch RETMA rack
Depth	63.5 cm (25 in) behind bezel
Height	26.52 cm (10.44 in)
Weight	34 kg (75 lb)
Mounting	The drive mounts on chassis slides
Power Source	90-127 Vac (47.5-63 Hz) 180-256 Vac (47.5-63 Hz) (Manually selectable)
Input Power	160 W max at 115 Vac, 60 Hz
Power Factor	Greater than 0.85
Starting Current	3.5A (rms) max @ 90 Vac/47.5-63 Hz 5.0A (rms) max @ 127 Vac/47.5-63 Hz 1.75A (rms) max @ 180 Vac/47.5-63 Hz 2.5A (rms) max @ 254 Vac/47.5-63 Hz
Heat Dissipation	546 Btu/hr max
Power Cord and Connector	A molded line cord compatible with the drive operating voltage and the 861 power control for 120 Vac is attached to the drive. The power cord is 2.74 m (9 ft) long and the plug is NEMA 5-15P. The 230 Vac plug to be attached to high voltage drives is NEMA 6-15P.

Table 1-2 RL01/RL02 Disk Drive Physical and Environmental Specifications (Cont)

Characteristics	Specifications
Safety	The RL01/RL02 disk drive is UL listed and CSA certified.
Interlocks	Interlocks are used where potential exists for damage to drive, media, operators, or service personnel.
Temperature/ Humidity	**Operating:** Temperature: 10° C (50° F) to 40° C (104° F) Note: Maximum allowable operating temperatures are reduced by a factor of 1.8° C/1000 meters (1° F/1000 feet) for operation above sea level. Relative Humidity: 10 to 90 percent with maximum wet bulb temperature 28° C (82° F) and minimum dew point 2° C (36° F) **Nonoperating:** Temperature: −40° C (−40° F) to 66° C (151° F) Relative Humidity: 10 to 95 percent, noncondensing
Altitude	**Operating:** 2440 m (8,000 ft) max **Nonoperating:** 9144 m (30,000 ft) max
Shock	**Operating:** Half sine shock pulse of gravity peak and 10 ± 3 ms duration applied once in either direction of three orthogonal axes (3 pulses total) **Nonoperating:** Half sine shock pulses of 40 gravity peak and 30 ± 10 ms duration perpendicular to each of six package surfaces.
Vibration	**Operating:** Sinusoidal vibration (sweep rate 1 octave/min) 5-50 Hz, 0.002 in displacement amplitude 50-500 Hz, 0.25 gravity peak 500-50 Hz, 0.25 gravity peak 50-5 Hz, 0.002 in displacement amplitude

Table 1-2 RL01/RL02 Disk Drive Physical and Environmental Specifications (Cont)

Characteristics	Specifications
Vibration	**Nonoperating:** Vertical Axis Excitation – 1.40 gravity (rms) overall from 10 to 300 Hz; power spectral density of 0.029 g^2/Hz from 10 to 50 Hz, with 8 dB/octave rolloff from 50 to 300 Hz Longitudinal and Lateral Axis Excitation – 0.68 gravity (rms) overall from 10 to 200 Hz; power spectral density of 0.007 g^2/Hz from 10 to 50 Hz, with 8 dB/octave rolloff from 50 to 200 Hz
EMI	Meets DEC Standard 102, Section 7.
Dust	The drive will operate in an ambient atmosphere of less than 5 million particles 0.5 microns or larger per cubic foot of air. The drive is intended to run in a light industry or cleaner environment.
Attitude	Maximum pitch: ± 15 degrees Maximum roll: ± 15 degrees

Table 1-3 RL01/RL02 Disk Drive Operational Specifications

Characteristics	Specifications
General	Linear bit density: 147 bits/mm (3725 bits/in) at innermost track 16-bit words per sector: 128 Number of sectors per track: 40 Track density: 4.9/mm (125/in) for RL01K, 9.8/mm (250/in) for RL02K Number of tracks per surface: 256 for RL01K, 512 for RL02K Number of surfaces: 2 Formatted capacity (megabytes): 5.2 for RL01K, 10.4 for RL02K Encoding method: Modified Frequency Modulation (MFM)
Transfer Rate (Unbuffered Values)	Bit rate: 4.1 megabits/second ± 1 percent Bit cell width: 244 ns ± 1 percent Word transfer rate (16-bit words): 256 kilowords/second ± 1 percent
Latency	Rotational frequency: 2400 rev/min ± 0.25% Average latency: 12.5 ms ± 0.25% Maximum latency: 25.0 ms ± 0.25%
Seek Time	Average seek time: 55 ms max (85 tracks for RL01, 170 tracks for RL02) One cylinder/track seek time: 15 ms max Maximum seek time: 100 ms max (256 tracks for RL01, 512 tracks for RL02)
Start/Stop Time	Start time: 45 seconds Stop time: 30 seconds
Data Format	Refer to Figure 1-3

Table 1-4 RL01K/RL02K Disk Cartridge Specifications

Characteristics	Specifications
Operating Environment	The cartridge will operate over a temperature range of 4° C to 48° C (40° F to 120° F), at a relative humidity of 8 to 80 percent. The wet bulb reading must be less than 25° C (78° F). Before a cartridge is placed in operation, it should be conditioned within its cover for a minimum of 2 hours in the same environment as that in which the disk drive is operating. (The above specified ranges do not necessarily apply to the disk drive.)
Storage Environment	The cartridge should be stored at a temperature between −40° C to 65° C (−40° F to 150° F), with a wet bulb reading not exceeding 29° C (85° F). For wet bulb temperatures between 0.56° C and 29° C (33° F and 85° F) the disk cartridge will withstand a relative humidity of 8 to 80 percent. The stray magnetic field intensity shall not exceed 50 Oersteds.
Dimensions (Cartridge)	The external diameter of the top cover is 38.35 cm (15.1 in). The external diameter of the protection cover is 37.03 cm (14.58 in). The external height of the cartridge is 6.19 cm (2.44 in).
Maximum Speed	The rotating parts of the disk cartridge are capable of withstanding the effect of stress created while rotating at 2,500 rev/min.
Track Geometry	There are 256 discrete concentric tracks per data surface for the RL01K, 512 tracks per data surface for the RL02K.
Identification of Data Location	Data Track Identification – Data tracks are numbered by consecutive decimal numbers (000 – 255, RL01K; 000 – 511, RL02K) starting at the outermost data track of each data surface. Data Surface Identification – The upper data surface is numbered 0 and the lower surface is numbered 1, to correspond with the head numbers.

Table 1-4 RL01K/RL02K Disk Cartridge Specifications (Cont)

Characteristics	Specifications
	Cylinder Address – A cylinder is defined as both data tracks (on either surface) with a common data track identification. Data Track Address – A 16-bit word defines the data track address. Bits 0 – 5 define the sector, bit 6 defines the surface, and bits 7 – 15 define the cylinder address. This information is in word 1 of each sector's header.

CHAPTER 2
INSTALLATION

2.1 SITE PREPARATION AND PLANNING

This chapter describes power, space, environmental, cabling, and safety requirements that must be considered before installation of the RL01/RL02 disk subsystem.

2.1.1 Environmental Considerations

The RL01/RL02 disk subsystem is designed to operate in a business or light industry environment. Although cleanliness is an important consideration in the installation of any computer system, it is particularly crucial for proper operation of a disk drive. The RL01K/RL02K disk cartridge is not sealed while being loaded and is therefore vulnerable to dust or smoke particles suspended in the air, as well as to fingerprints, hair, lint, etc. These minute obstructions can cause head crashes, resulting in severe damage to the read/write heads and disk surfaces.

2.1.1.1 Cleanliness – The RL01/RL02 disk drives can operate in an ambient with less than five million particles per cubic foot of air which are 0.5 micron or larger in diameter. The drive contains a filter system which, under these conditions, maintains the particle count within the cartridge below 100 particles per cubic foot.

2.1.1.2 Space Requirements – Provision should be made for service clearances of 1 m (39 in) at the front and rear of the rack or cabinet in which the drive is mounted and 1 m (39 in) at either side.

Storage space for the RL01K/RL02K cartridges should also be made available. Each cartridge has a diameter of approximately 38 cm (15 in) and a height of approximately 6 cm (2.5 in).

CAUTION

RL01K/RL02K disk cartridges must never be stacked on top of each other. A designated shelf area or specially designed disk cartridge storage unit is recommended (see the DIGITAL Supplies and Accessories Catalog).

2.1.1.3 Floor Loading – The weight of the RL01/RL02 disk drive alone is 34 kg (75 lb), which will not place undue stress on most floors. However, the added weight of the rack or cabinet as well as the number of drives to be installed should be considered in relation to the weight of existing computer systems. Possible future expansion should also be a consideration.

2.1.1.4 Heat Dissipation – The heat dissipation of each RL01/RL02 disk drive is 546 Btu/hour maximum. The approximate cooling requirements for the entire system can be calculated by multiplying this figure by the number of drives, adding the result to the total heat dissipation of the other system components, and then adjusting the total figure to compensate for personnel, cooling system efficiency, etc. It is advisable to allow a safety margin of at least 25 percent above the maximum estimated requirements.

2.1.1.5 Acoustics – Most computer sites require at least some degree of acoustical treatment. However, the RL01/RL02 disk subsystem should not contribute unduly to the overall system noise level. Ensure that acoustical materials used do not produce or harbor dust.

2.1.1.6 Temperature – The RL01/RL02 disk subsystem operates over a temperature range of 10° C (50° F) to 40° C (104° F). The maximum temperature gradient is 16.6° C (30° F) per hour. The nonoperating temperature range is from −40° C (−40° F) to 66° C (151° F).

2.1.1.7 Relative Humidity – Humidity control is important for proper operation of any computer system since static electricity may cause memory errors or even permanent damage to logic components. The RL01/RL02 disk subsystem is designed to operate within a relative humidity range of 10 to 90 percent with a maximum wet bulb temperature of 28° C (82° F) and a minimum dew point of 2° C (36° F). The nonoperating relative humidity range is from 10 to 95 percent, with a maximum wet bulb temperature of 46° C (115° F).

2.1.1.8 Altitude – Computer systems operating at high altitudes may have heat dissipation problems. Altitude also affects the flying height of read/write heads in disk drives. The maximum altitude specified for operating the RL01/RL02 disk subsystem is 2440 m (8000 ft). Also, the maximum allowable operating temperature is reduced by a factor of 1.8° C per 1000m (1° F per 1000 ft) above sea level. Thus, the maximum allowable operating temperature at 2440 m (8000 ft) would be reduced to 36° C (96° F).

2.1.1.9 Power and Safety Precautions – The RL01/RL02 disk subsystem presents no unusual fire or safety hazards to an existing computer system. AC power wiring should be checked carefully, however, to ensure that its capacity is adequate for the added load as well as for any possible expansion. The RL01/RL02 disk drive is UL listed and CSA certified.

2.1.1.10 Radiated Emissions – Any source of electromagnetic interference (EMI) that is near the computer system may affect the operation of the processor and its related peripheral equipment. Common EMI sources that are known causes of failures include:

- Thunderstorms,
- Broadcast stations,
- Radar,
- Mobile communications,
- High-voltage power lines,
- Power tools,
- Arc welders,
- Vehicle ignition systems,
- Static electricity.

The effect of radiated EMI emissions on a computer system is unpredictable. Thus, grounding plays an important role in protecting the circuits used in disk drive subsystems.

To help reduce the effects of known high-intensity EMI emissions, perform the following actions:

- Ground window screens and other large metal surfaces,
- Ensure that the overall computer system is grounded properly (refer to Paragraph 2.1.5, Grounding Requirements),
- Provide proper storage (metal cabinets with doors) for disk cartridges.

2.1.1.11 Attitude/Mechanical Shock – Performance of the RL01/RL02 disk subsystem will not be affected by an attitude where maximum pitch and roll do not exceed 15 degrees.

The subsystem is designed to operate while a half-sine shock pulse of 10 gravity peak and 10 ± 3 ms duration is applied once in either direction of three orthogonal axes (three pulses total).

2.1.2 Options

The RL01/RL02 disk drive can be shipped with various controllers (for UNIBUS, OMMIBUS and LSI-11 Bus computer systems), and can be configured for 115 Vac or 230 Vac operation.

Table 2-1 shows saleable RL01/RL02 subsystem options. Table 2-2 shows RL01/RL02 cabinet components.

Table 2-1 Saleable RL01/RL02 Subsystem Options

Option Number	Description
RL01A	RL01 unit, BC20J I/O cable, chassis slide and mounting hardware
RL02A	RL02 unit, BC20J I/O cable, chassis slide and mounting hardware
RL01-AK	RL01-A (drive), RL01K-DC (cartridge)
RL02-AK	RL02-A (drive), RL02K-DC (cartridge)
RL01K-DC	RL01 data cartridge
RL02-DC	RL02 data cartridge
RL11-AK	RL01-AK, RL11 controller, BC06R, terminator
RL211-AK	RL02-AK, RL11 controller, BC06R, terminator
RLV11-AK	RL01-AK, RLV11 controller, BC06R, terminator
RLV12-AK	RL02-AK, RLV11 controller, BC06R, terminator
RL8A-AK	RL01-AK, RL8A controller, BC80J, terminator
RL28A-AK	RL02-AK, RL8A controller, BC80J, terminator
RLV21-AK	RL01-AK, RLV12 controller, BC80M, terminator
RLV22-AK	RL02-AK, RLV12 controller, BC80M, terminator

NOTE

BC20J cables come in lengths of 20, 40 or 60 feet. If 10 foot cables are desired, then the cable designation becomes 70-12122-10. Total length of cables from this controller to the last drive must not exceed 30 M (100 ft.).

Table 2-2 Saleable Cabinet Options: (Includes Skins, Doors, Covers, Trim, and Power Controllers)

Type	Volts	Dwg.	Remarks
H950	110 220	H960-BC H960-BD	Includes five 26.67 cm (10.5 in) high panels
H967	110 220	H967-BA H967-BB	26.67 cm (10.5 in) cover panels (H950-QA) must be ordered if required
H9500	110	H9603-ED	SWLB with H9514-B top covers
	220 110	H9603-EE H9601-ED	DWLB with H9514-A top covers
	220 110	H9601-EE H9602-EA	SWHB complete hiboy cabinet
	220 110	H9602-EB H9600-EA	DWHB complete hiboy cabinet
H9500	220	H9600-EB H9602-B-O	SWHB option arrangement dwg. Order as required
		H9600-A-O	DWHB option arrangement dwg. Order as required
		H9603-B-O	SWLB option arrangement dwg. Order as required
H9500		H9601-A-O	DWHB option arrangement dwg. Order as required

2.1.3 AC Power Requirements

The RL01 or RL02 drive can operate within one of four voltage ranges that are manually selected by means of two terminal blocks located at the rear of the device (Figure 2-1). These voltage ranges are:

	110	220
NOM	105–128	210–256
LO	90–110	180–220

The drive will operate when the line frequency is between 47.5 and 63 Hz.

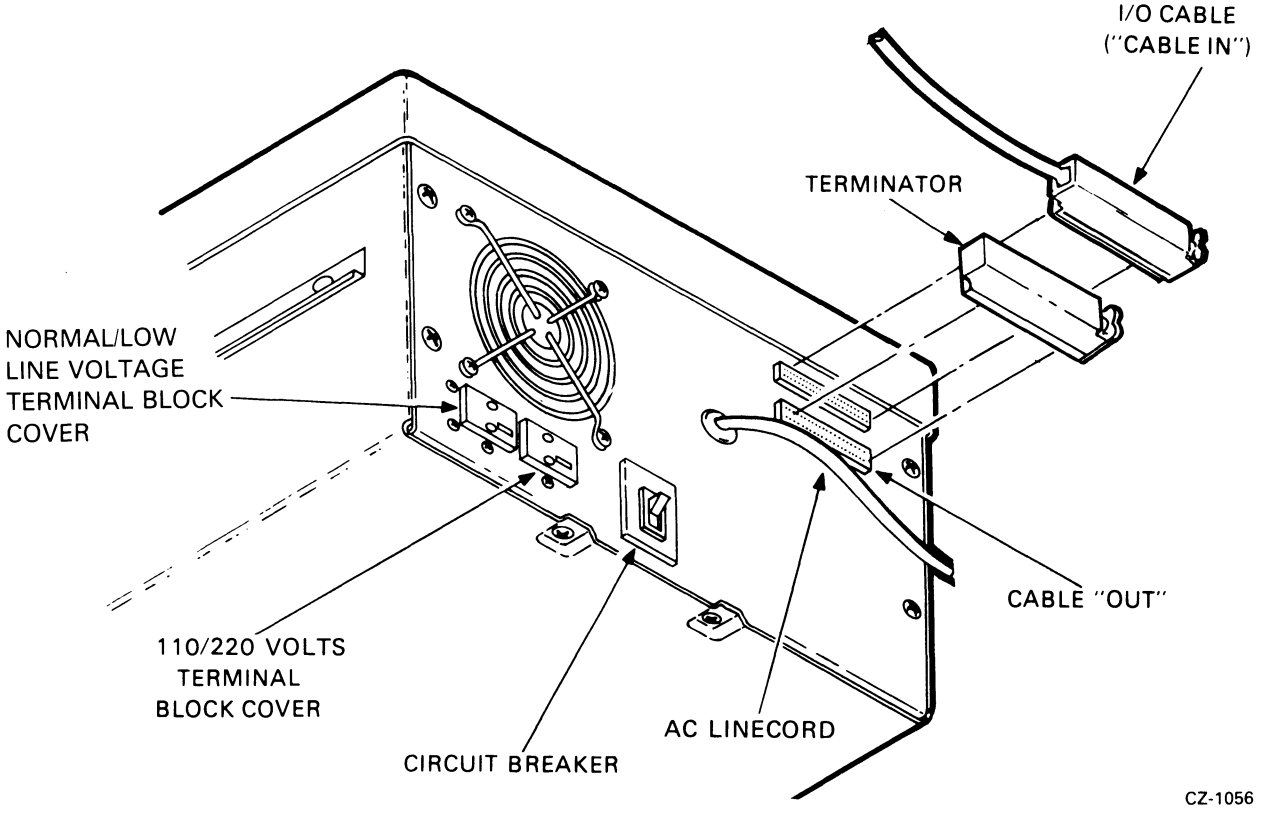


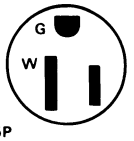
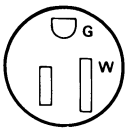
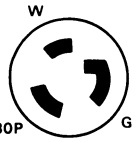
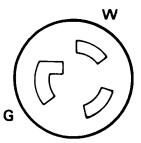
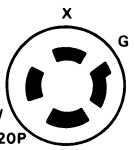
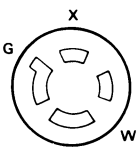
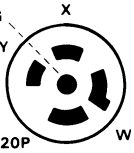
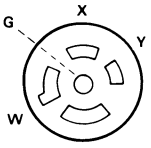
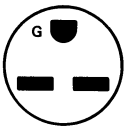
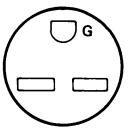
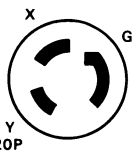
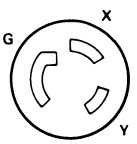
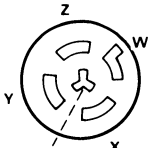
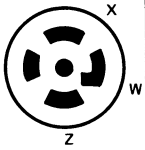
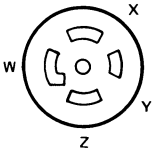
Figure 2-1 RL01/RL02 Disk Drive – Rear View

2.1.3.1 Standard Applications – The drive can be shipped from the factory as a free-standing unit or mounted in various racks and cabinets (refer to Paragraph 2.1.2, Options).

If shipped as a free-standing unit, the 2.74 m (9 ft) ac power cord is terminated with a NEMA type 5-15P plug (DIGITAL Part No. 90-08938). This plug requires a NEMA type 5-15P receptacle (Figure 2-2).

2.1.3.2 Optional Applications – Operation in the high voltage range (180–256 Vac) will require reconfiguring the terminal block at the rear of the drive and changing the line cord plug (Figure 2-1).

In 50 Hz applications, the line cord plug must be changed (Figure 2-2).

SOURCE	PLUG	RECEPTACLE	USED ON	
120V 15A 1-PHASE	 HUBBEL #5266-C NEMA # 5-15P DEC # 90-08938	 #5262 5-15R 12-05351	ALL 120 V TABLE-TOP COMPUTERS. STANDARD 120V LOW-CURRENT DISTRIBUTION. 120V TU10 UNITS. MOST 120V TERMINAL DEVICES.	POWER CONTROLLER 861-F
120/208V 30A 3-PHASE Y	 HUBBEL #2611 NEMA # L5-30P DEC # 12-11193	 #2610 L5-30R 12-11194	ALL 120V STANDARD CABINET MOUNTED EOPT	POWER CONTROLLER 861-C
120/208-240V 20A 2-PHASE or 120/208V 20A 3-PHASE Y	 HUBBEL #2411 NEMA # L14-20P DEC # 12-11045	 #2410 L14-20R 12-11046	120V PDP-11/45 PROCESSOR CABINET ONLY.	POWER CONTROLLER 861-A
120/208V 20A 3-PHASE Y	 HUBBEL #2511 NEMA # L21-20P DEC # 12-11209	 #2510 L21-20R 12-11210	60 Hz RM 10 DRUM 60 Hz RP02/RP03/ RP04, RP05, RP06	
240V 15A 1-PHASE	 NEMA # 6-15P DEC # 90-08863	 6-15R 12-11204	ALL 240V TABLE-TOP COMPUTERS. STANDARD LOW-CURRENT 240V DISTRIBUTION. MOST 240V TERMINAL DEVICES. 240V TU10.	
240V 20A 1-PHASE	 HUBBEL #2321 NEMA # L6-20P DEC # 12-11192	 #2320 L6-20R 12-11191	ALL 240V STANDARD CABINET MOUNTED EQUIPMENT.	POWER CONTROLLER 861-B
240/416V 20A 3-PHASE Y	 NEMA # -- NOT NEMA DEC # 12-09010	 NOT NEMA 12-11259	50 Hz RM10 DRUM 50 Hz RP02/RP03/ RP04	
120V 30A 1-PHASE	 HUBBEL #2811 NEMA L21-30P DEC 12-12314	 #2810 L21-30R 12-12315	PDP11/70 PROCESSOR PDP 11/70 MEM. VAX-11/780 PROCESSOR	POWER CONTROLLER 861-D

CP-1968

Figure 2-2 Approved Electrical Plugs and Receptacles

2.1.4 Installation Constraints

The route from the receiving area to the installation site that the equipment will travel should be studied in advance to ensure problem-free delivery. Among the considerations are:

- Height and location of loading doors,
- Size, capacity, and availability of elevators,
- Number and size of aisles and doors en route,
- Bends or obstructions in hallways.

2.1.5 Grounding Requirements

Each cabinet of a DIGITAL computer system is equipped with ground lug terminals that should be connected to a low-impedance earth ground by No. 4 AWG (5 mm/0.20 in) copper wire or stranded No. 4 AWG welding cable. A Burndy QA4C-B solderless lug (or equivalent) is recommended for terminating the cable. DIGITAL supplies a standard grounding conductor with each I/O and memory cabinet.

A steel building beam is an adequate ground in many instances. However, some disk-oriented systems may require additional connections to earth ground, in addition to the ground leads carried through various signal buses and ground connectors contained within the power cables. The green grounding wire in the power cable must also be returned to ground, usually through the conduit of the electrical distribution system. Note that the green wire is a not a current-carrying conductor, nor a neutral conductor.

Whenever possible, the system power panel must be either mounted in contact with bare building steel by bonded joints (Figure 2-3) or connected to the steel by a short length of cable.

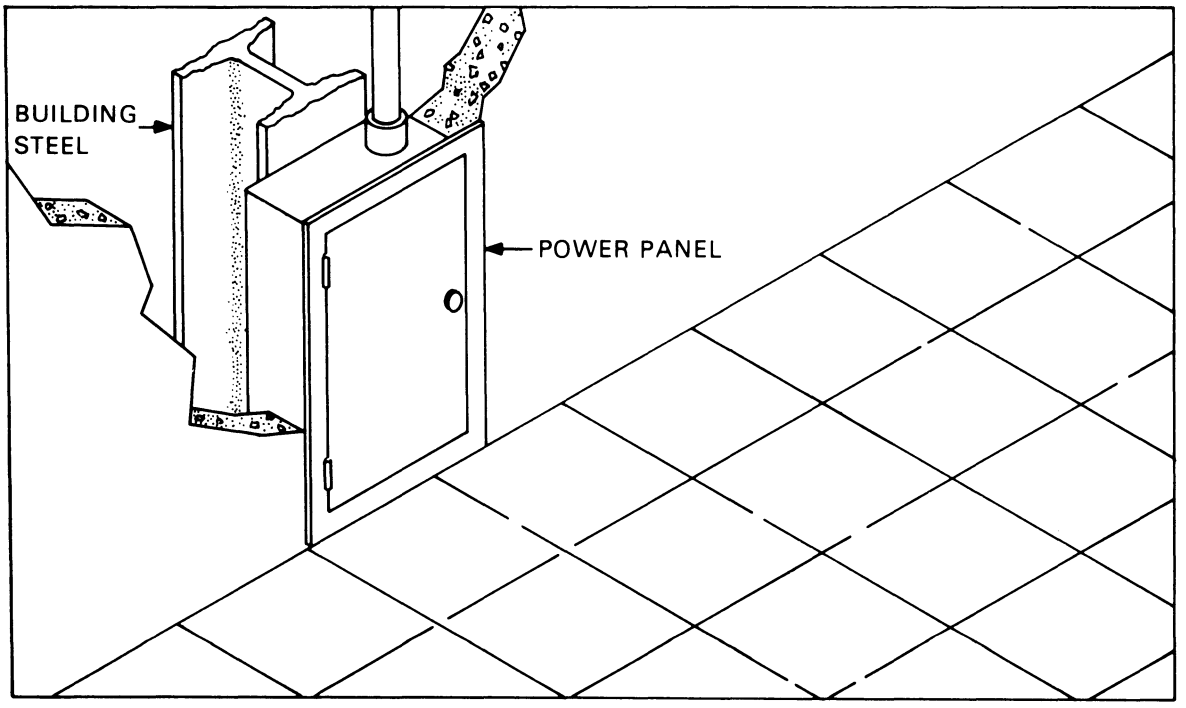


Figure 2-3 Power Panel Grounded Building Frame

Where neither scheme is possible, a metal area (comprising the power panel, the conduit, and a metal plate) of at least 1 m^2 (10 ft^2) that is in contact with masonry must be connected to the green ground wire (Figure 2-4). The connecting wire must not exceed 1.5 m (5 ft) in length and should be at least a No. 12 AWG (2mm).

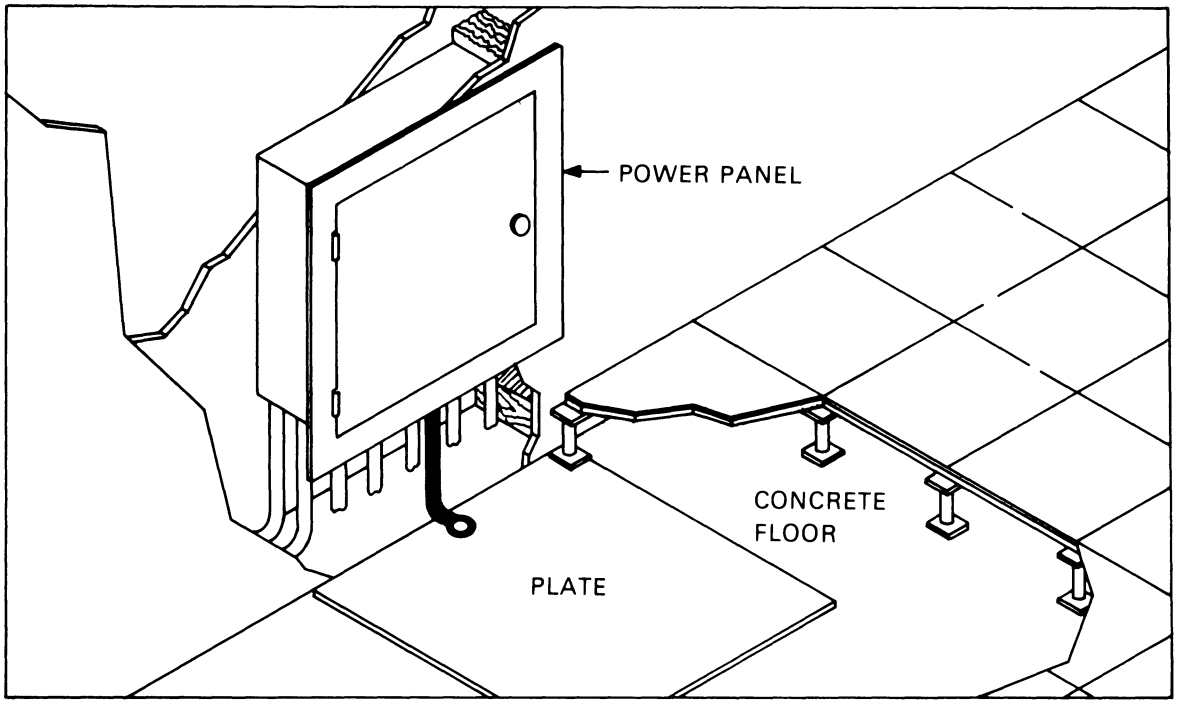


Figure 2-4 Power Panel Grounded To Metal Plate

When two cabinets are bolted together, DIGITAL bonds them electrically with a No. 4 AWG conductor (5 mm/0.20 in) or by several copper mesh straps connected between the cabinet frames.

After the grounding system is installed, it is advisable to take a voltage reading between the cabinet frame and the nearest grounded object. NBFU No. 70 (published by the National Bureau of Underwriters) provides further details regarding preferred grounding procedures.

2.2 AC CABLING

Computer equipment requires a power source with a minimum number of voltage and frequency disturbances. Line voltage disturbances greater than 1/4 cycle (measured at the receptacle during system operation) are undesirable.

DIGITAL power wiring conforms to Underwriters Laboratories, Inc., Handbook UL No. 478, National Electrical Code standards, and the type II requirements of the National Fire Protection Association (NFPA 70). This means that in the United States the wire used as equipment ground is green, or green with a yellow stripe; it carries no load current (except in emergency), but does carry leakage current. No equipment is permitted to leave DIGITAL that does not have a grounding connection to its frame.

The grounded conductor is light grey or white. It must not be used to ground equipment. Its purpose is to conduct current.

Lines 1, 2, and 3 in a typical 60 Hz power system (Figure 2-5) are represented by black, red, and blue wires, respectively, and phase rotation is in that order.

CAUTION

Where no grounded wire can be guaranteed, it must not be assumed. There are some 115 V/60 Hz systems within the United States where neither side of the line is grounded (115 V 3-phase delta).

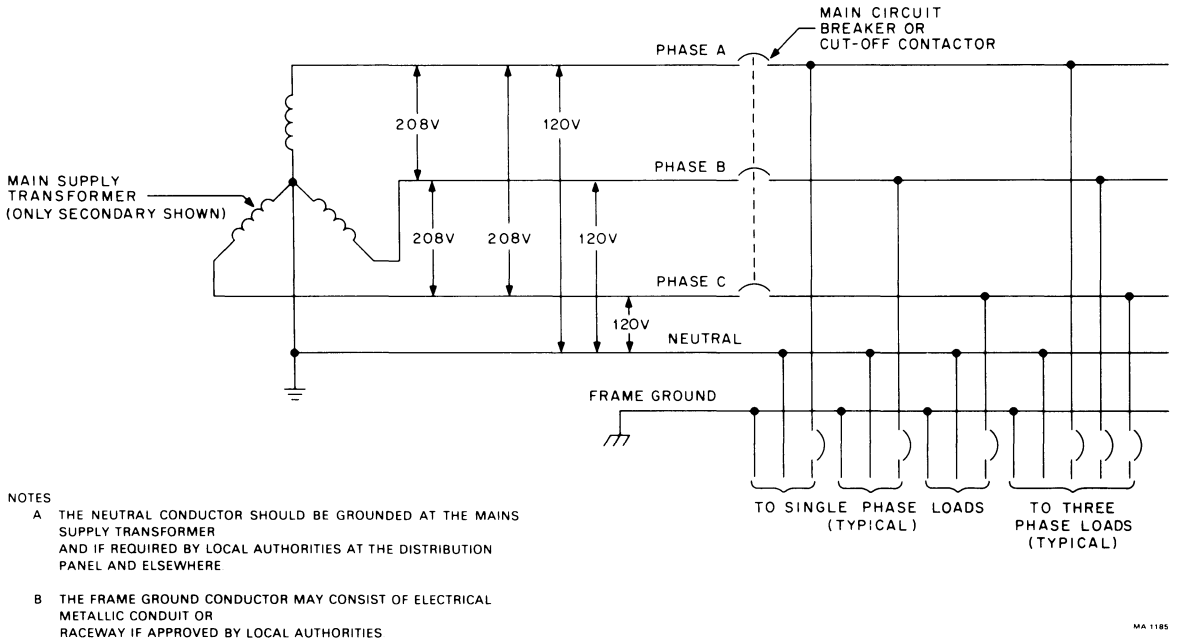


Figure 2-5 Typical 60 Hz Power System

Figure 2-6 shows a typical 50 Hz power system.

Two types of power systems can be used to provide power to the NEMA type L14-20R receptacle. The type shown in Figure 2-7 is referred to as split-phase (or 2-phase 180° displaced) 120/240 Vac. It comprises a center-tapped transformer with 120 Vac between the center tap and either of the two legs. 240 Vac exists between the two outside legs.

The second type (Figure 2-8) is referred to as 3-phase Y (120° displaced) 120/280 Vac. The 120 Vac exists between neutral and any of the three other legs (X, Y, or Z), and 208 Vac exists between any two of the outer legs (i.e., between X and Y, X and Z, or Y and Z). Although Figure 2-8 shows the X and Y connections as the two phases used for the receptacle, any two of the three phases shown can be used.

The ground terminal on the L14-ZOR receptacle will normally have a green screw, the neutral terminal will be white or silver, and the "hot" terminal will be brass covered.

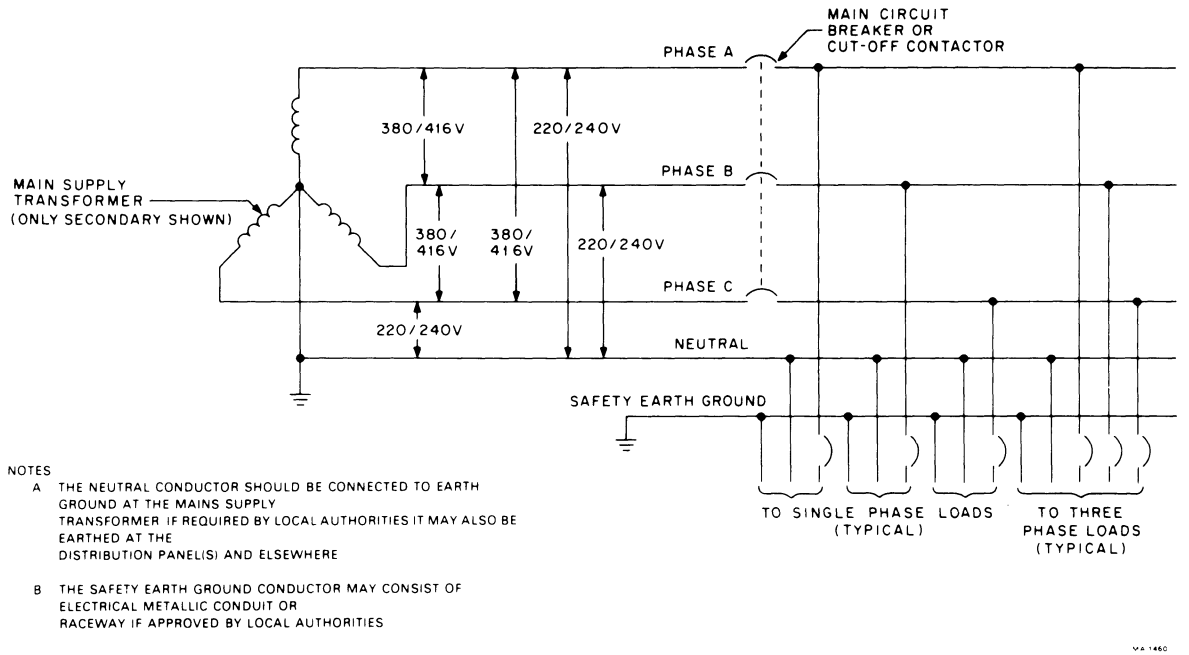


Figure 2-6 Typical 50 Hz Power System

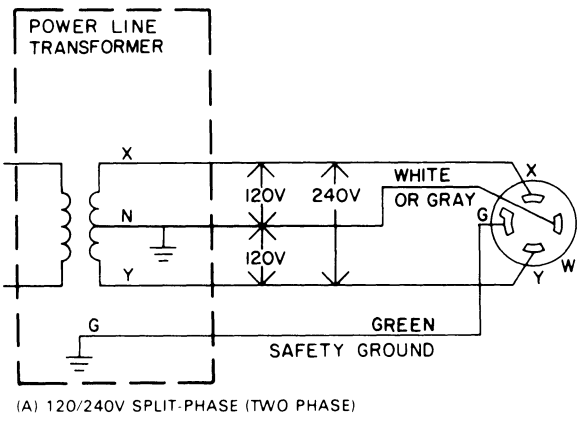


Figure 2-7 Split Phase (2-phase) Power System

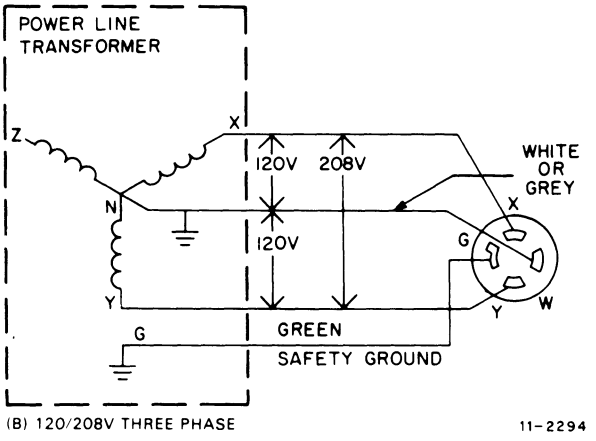


Figure 2-8 Three Phase Y Power System

2.3 INSTALLATION - GENERAL

The controller should be installed first, followed by the drive(s). Next, the diagnostics should be run to demonstrate that the subsystem is functioning properly or to diagnose any problems. Paragraph 2.4 explains the installation of the RL11 controller, Paragraph 2.5 deals with the RLV11, Paragraph 2.6 describes RLV12 installation and Paragraph 2.7 describes RL8A installation.

Paragraph 2.8 contains instructions to install the unit and Paragraph 2.9 explains acceptance testing and contains separate paragraphs for each of the three controllers. Paragraph 2.10 describes the use of the M9312 bootstrap module that may be used on RL11-based systems.

2.4 RL11 CONTROLLER INSTALLATION

The RL11 controller (M7762) is a single hex-height module that is installed in a hex-height Small Peripheral Controller (SPC) slot. Connector J1 connects the controller to the drive bus (Figure 2-9).

Of the 21 jumpers on the RL11 controller, five are used for factory test purposes. The remaining 16 are for address selection:

W1-W6	VECTOR ADDRESS (160)
W7-W16	BASE ADDRESS (774400)

NOTE

A logical one is represented by the presence of a jumper wire.

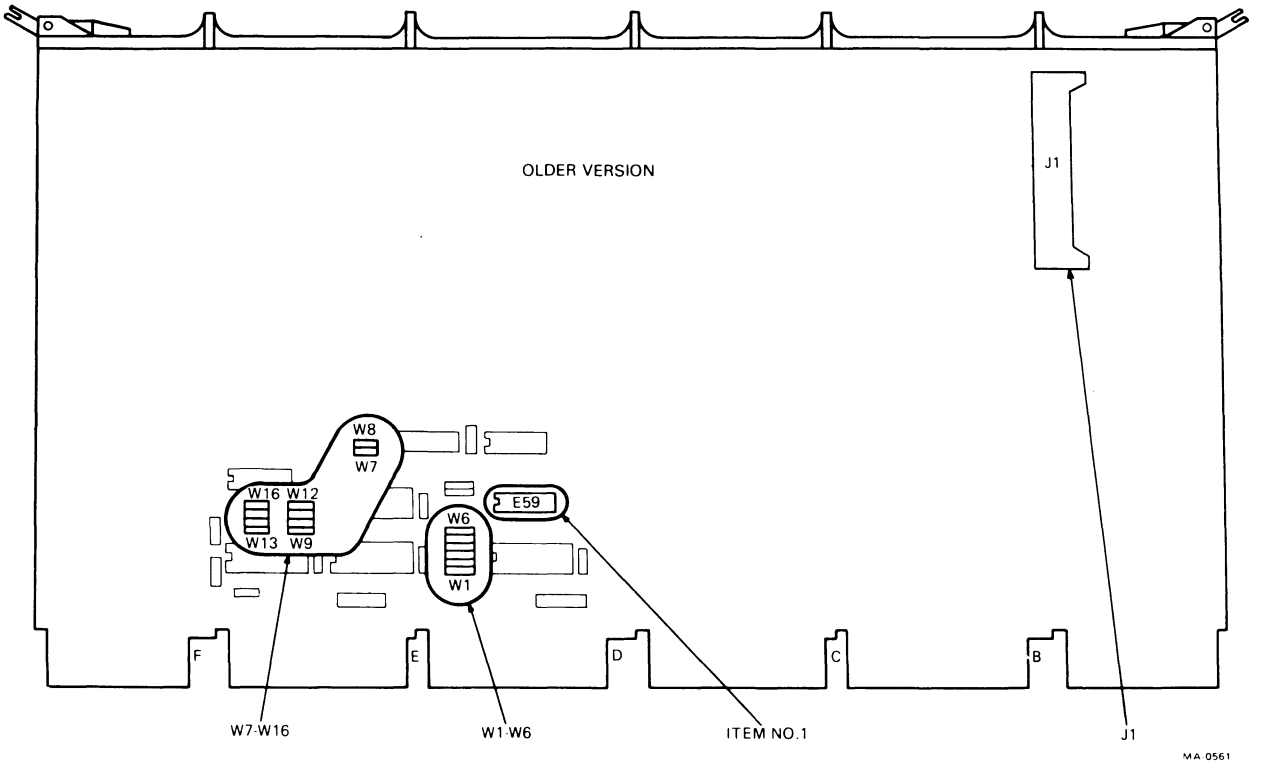


Figure 2-9 RL11 Component Layout (Sheet 1 of 2)

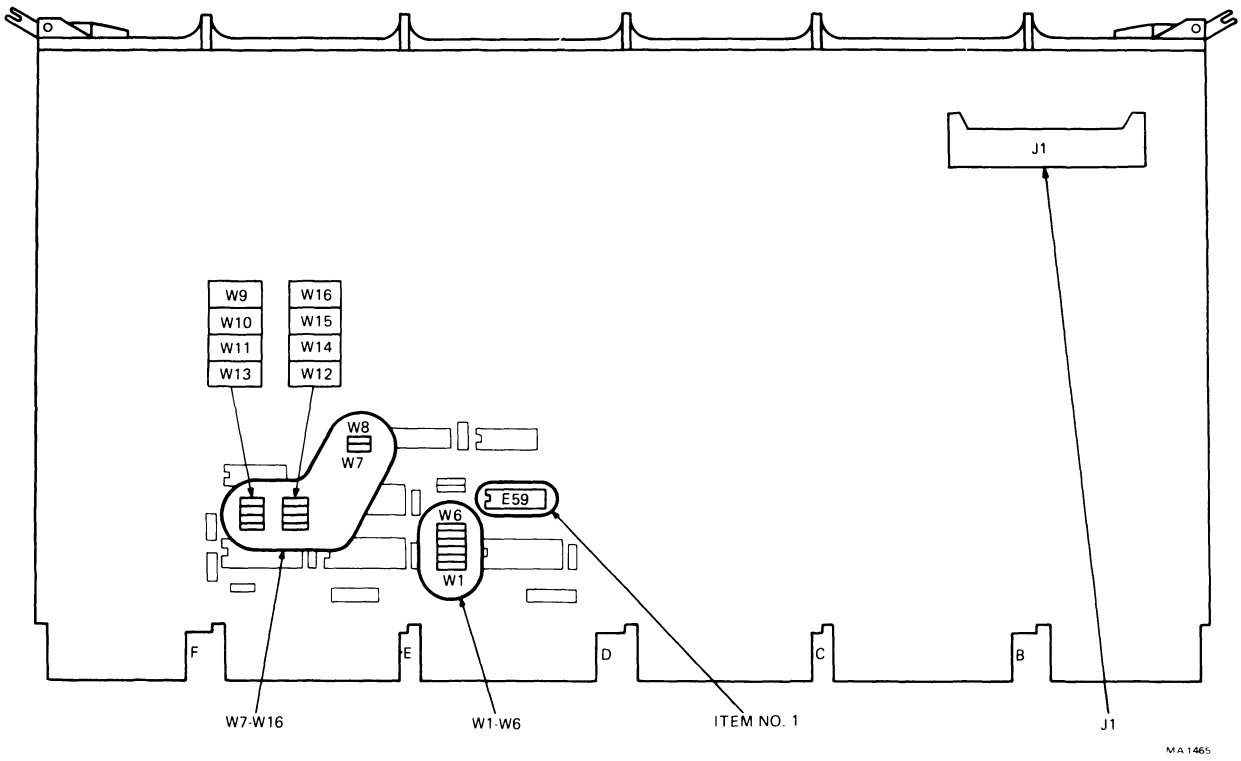


Figure 2-9 RL11 Component Layout (Sheet 2 of 2)

The UNIBUS priority plug sets the priority for bus requests. For the RL11 subsystem, bus requests are at priority level 5 (BR5/BG5). (See Figures 2-10 and 2-11.)

To install the controller:

1. Remove the M7762 module from its shipping container and examine it for any physical damage.

2. If a priority level other than 5 is required, obtain an appropriate priority jumper assembly or set up the priority jumper assembly (Item 1, Figure 2-9) using Figure 2-11 as a guide. The vector and base address jumpers W1-W16 are for 160 and 774400, respectively. If the subsystem configuration requires other than standard addresses, set the jumpers up as shown in Figure 2-10. Physical location of these jumpers is shown on Figure 2-9.

3. Install the ribbon cable (BC06R-XX) with the red indicator stripe to the right and the smooth side facing the viewer when viewing the component side of the controller as shown in Figure 2-12. Dress the cable as necessary.

4. Insert the controller into its appropriate slot in the SPC backplane as shown in Figure 2-12 after ensuring that the slot does not contain a grant continuity module in row D. Do not chafe the ribbon cable. Route the cable up and out to the rear of the cabinet, allowing for cable strain relief.

NOTE
Adjustments on the RL11 are preset at the factory and are not to be changed in the field.

VECTOR ADDRESS SCHEME

	0			0			0			1			6				0	
2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
X	X	X	X	X	X	X	X	X	X	W_1	W_3	W_4	W_5	W_6	W_2	X	X

FOR VECTOR ADDRESS 160 - W_3, W_4, W_5 JUMPERS IN
W_1, W_2, W_6 JUMPERS OUT

BASE ADDRESS SCHEME

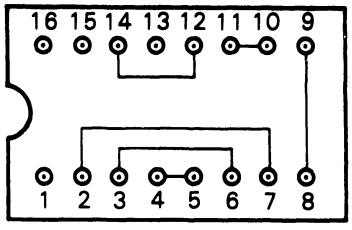
	7			7			4			4			0				0	
2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0
X	X	X	X	X	X	W_{12}	W_{16}	W_{15}	W_{14}	W_7	W_8	W_9	W_{11}	W_{10}	W_{13}	X	X	X

FOR BASE ADDRESS 774400 – W_{12}, W_{16}, W_7 JUMPERS IN
W_1, W_9, W_{10}, W_{11}, W_{13}, W_{14}, W_{15}, JUMPERS OUT

NOTE:
X'S DENOTE DON'T CARE (NOT SELECTABLE)
1'S DENOTE JUMPER IN
0'S DENOTE JUMPER OUT

CZ-2004

Figure 2-10 RL11 Base and Vector Address Jumper Configuration

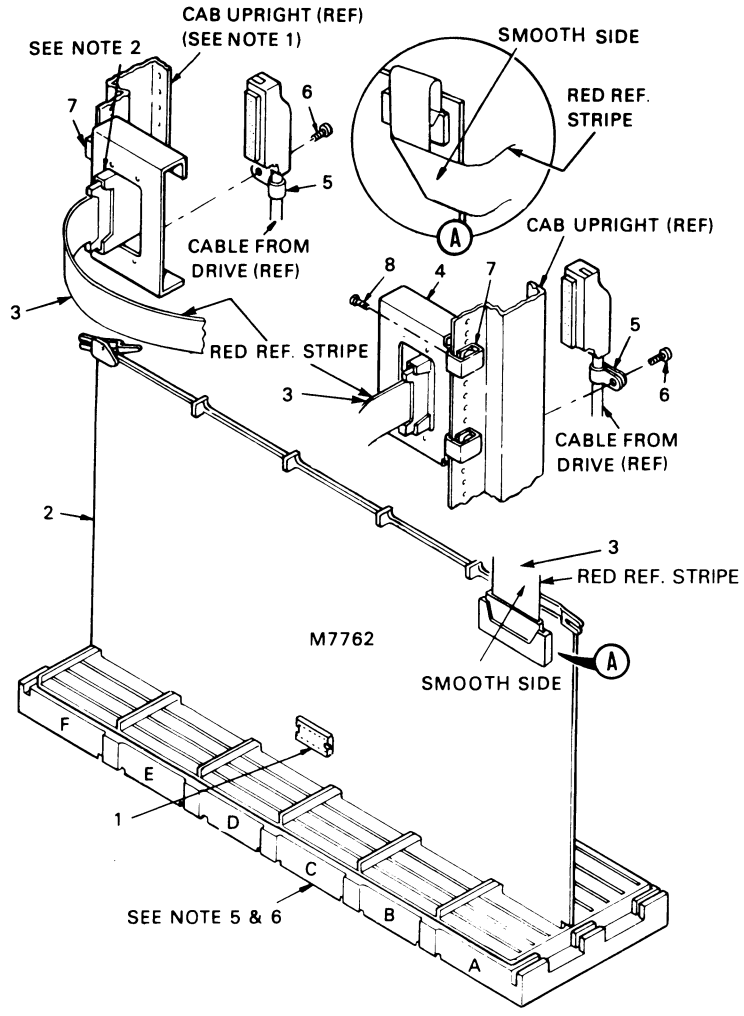


PRIORITY JUMPER PLUG FOR
BUS REQUEST LEVEL FIVE (5)

PLUG PIN NUMBER	SIGNAL NAME	UNIBUS PIN
1		
2	BG IN	
3	BG OUT	
4	UB BG 4	DT2
5	UB BG 4 IN	DS2
6	UB BG 5	DR2
7	UB BG 5 IN	DP2
8	UB BG 6	DN2
9	UB BG 6 IN	DM2
10	UB BG 7	DL2
11	UB BG 7 IN	DK2
12	BR	
13	UB BR 4	DD2
14	UB BR 5	DE2
15	UB BR 6	DF2
16	UB BR 7	DH2

MA-0560

Figure 2-11 RL11 Priority Jumper Assembly Connections



NOTES:

1. WHEN INSTALLED IN BA11K OR BA11L EXPANSION BOX, BC06R CABLE (ITEM #3) SHOULD BE FOLDED 90° AND ROUTED UP OUT OF THE BOX AS SHOWN.

2. WHEN ALTERNATE MOUNTING POSITION IS USED CONNECTOR IN TRANSITION BRACKET MUST BE INVERTED SO THAT I/O CABLE FROM DRIVE WILL HANG IN A DOWNWARD POSITION AS SHOWN.

3. ITEM #3 THRU ITEM #8 ARE NOT ASSEMBLED AT THIS POINT BUT ARE SHIPPED WITH UNIT FOR ASSEMBLY AT INSTALLATION TIME.

4. PRIORITY JUMPER ASSY (ITEM #1) TO BE PLUGGED INTO M7762 AT FINAL ASSY.

5. THE RL11 MODULE (M7762) WILL OCCUPY ONE HEX SPC SLOT.

6. JUMPER WIRE FROM CA1 TO CB1 ON THE SPC BACKPLANE MUST BE REMOVED AT INSTALLATION.

DESCRIPTION	DWG PART NO.	ITEM NO.
2 SCREW, PHL TRS HD. #10-32 X .50 LG	9006073-03	8
2 NUT, SPRING #10-32	9007786-00	7
1 SCREW, TAP-TLTE, #8 X .38 LG	9006418-01	6
1 CLAMP, CABLE	9007083-00	5
1 TRANSITION BRACKET ASSY	C-AD-7012415-0-0	4
1 CABLE ASSY	D-UA-BC06R-06	3
1 RL11 CONTROLLER	D-UA-M7762-0-0	2
1 PRIORITY JUMPER ASSY	5408778	1

CZ-2005

Figure 2-12 RL11 Controller Installation

NOTE
See Appendix A for configuration rules and SPC slot selection considerations.

5. Remove the jumper between CA1 and CB1 (NPR Grant) on the backplane if the jumper exists.

6. Install the transition bracket at the rear of the cabinet shown in Figure 2-12. Assemble and install transition connector.

7. Connect the other end of the ribbon cable (BC06R-XX) with the red indicator stripe on the top. Use Figure 2-12 as a guide.

8. Apply system power and, using a suitable measuring device (i.e., digital voltmeter or equivalent), verify that the voltages are within the ranges specified below.

Voltage	Range	Test Point	
Ground		AC2	
+5 Vdc	+4.75 to +5.25 Vdc	AA2	Backplane
+15 Vdc	+14.25 to +15.75 Vdc	CU1	Location
−15 Vdc	−15.75 to −14.25 Vdc	CB2	

Measure all voltages between the ground test point and the appropriate voltage test point. If any adjustments to the power supply are necessary, refer to the appropriate power supply manual.

2.5 RLV11 CONTROLLER INSTALLATION

An RLV11 controller is comprised of a bus interface module (M8014) and the drive bus module (M8013). Each module has switches, jumpers, trimpots, and connectors that are explained in the following paragraphs.

2.5.1 Bus Interface Module

The bus interface module (M8014) contains the logic circuits that perform the following major functions:

- LSI-11 bus interface functions,
- Programmable registers,
- Silo data storage and control circuits.

An illustration of the component side of M8014 is shown in Figure 2-13. The location of the bus address switches, the vector address switches, and the connector finger assignments are shown in this figure.

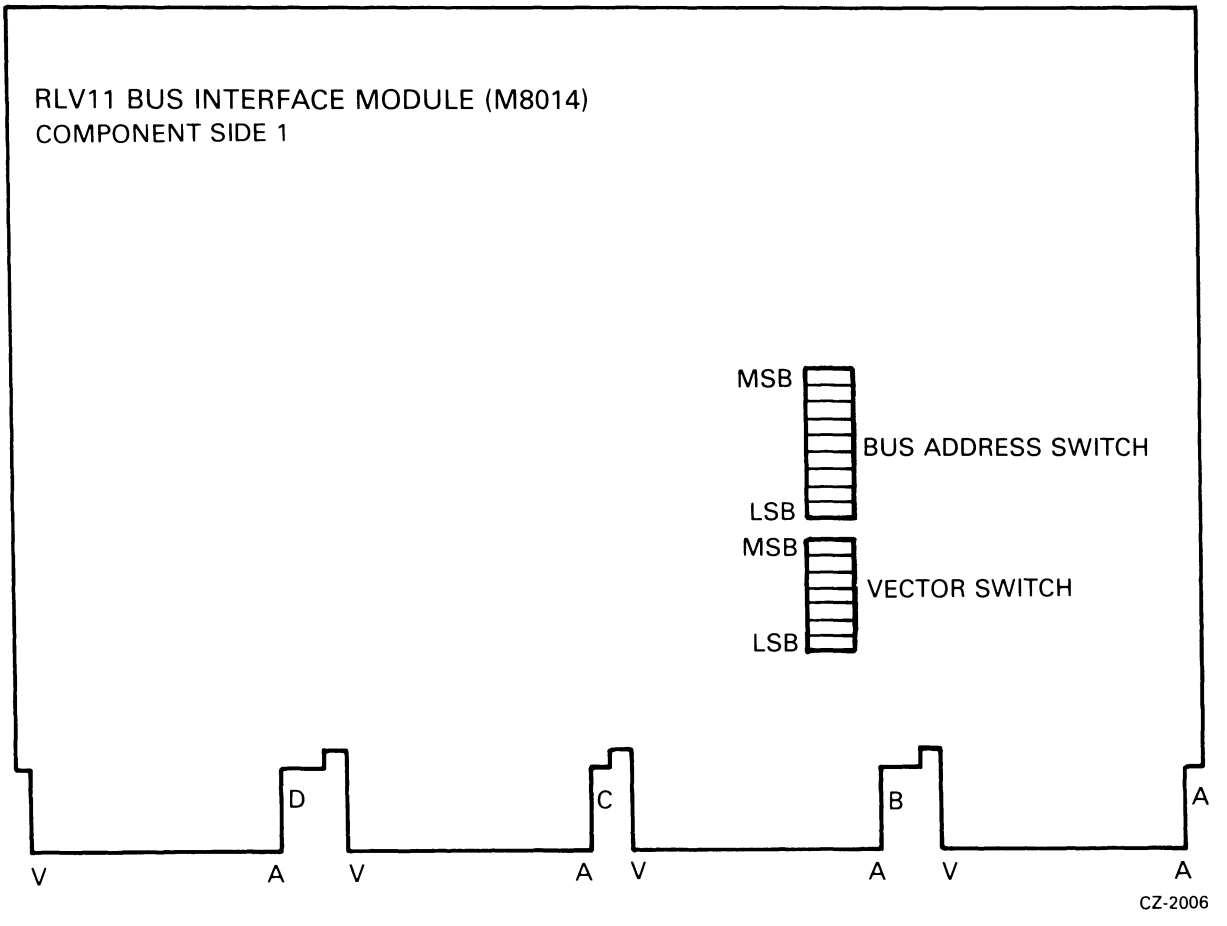


Figure 2-13 RLV11 Bus Interface Module (M8014) (Component Side)

The bus address switch is used to set up the device base address. It is normally factory preset to 7440. This means the device CS register has an address of 174400 and the MP register has an address of 174406. The switches have the ON and OFF positions labeled. The ON position is the logical 1 or true state (Figure 2-14).

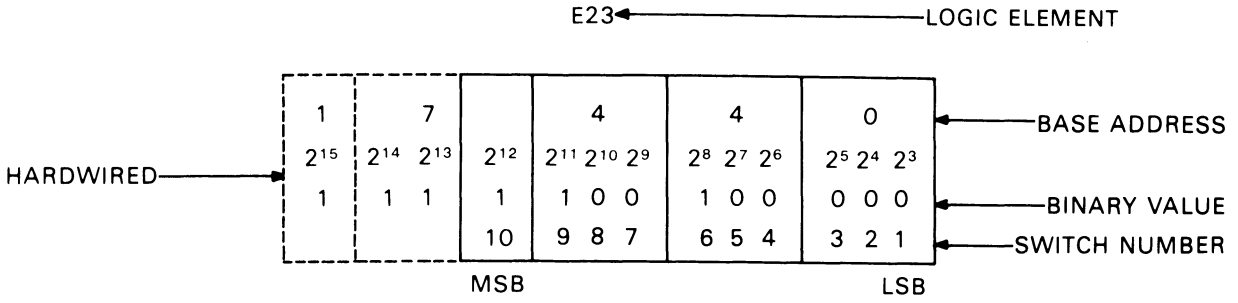


Figure 2-14 RLV11 Base Address Switch Settings

The vector address switch is used to select the address of the vector for this device when it interrupts. It is factory preset for an address of 160 (Figure 2-15).

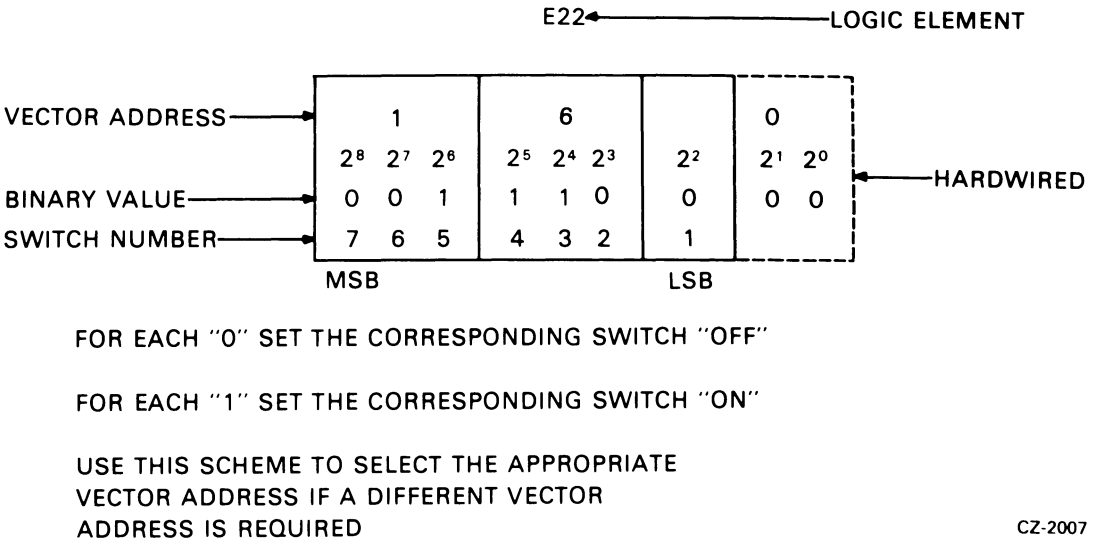


Figure 2-15 RLV11 Vector Address Switch Settings

2.5.2 Drive Module

The drive module (M8013) contains the circuitry that performs the following major functions:

- Data formatting and error-detecting circuits,
- Control microsequencer and timing circuits,
- Drive bus interface.

An illustration of the component side of M8013 is shown in Figure 2-16.

NOTE
Adjustments to the RLV11 are preset at the factory and are not to be adjusted in the field.

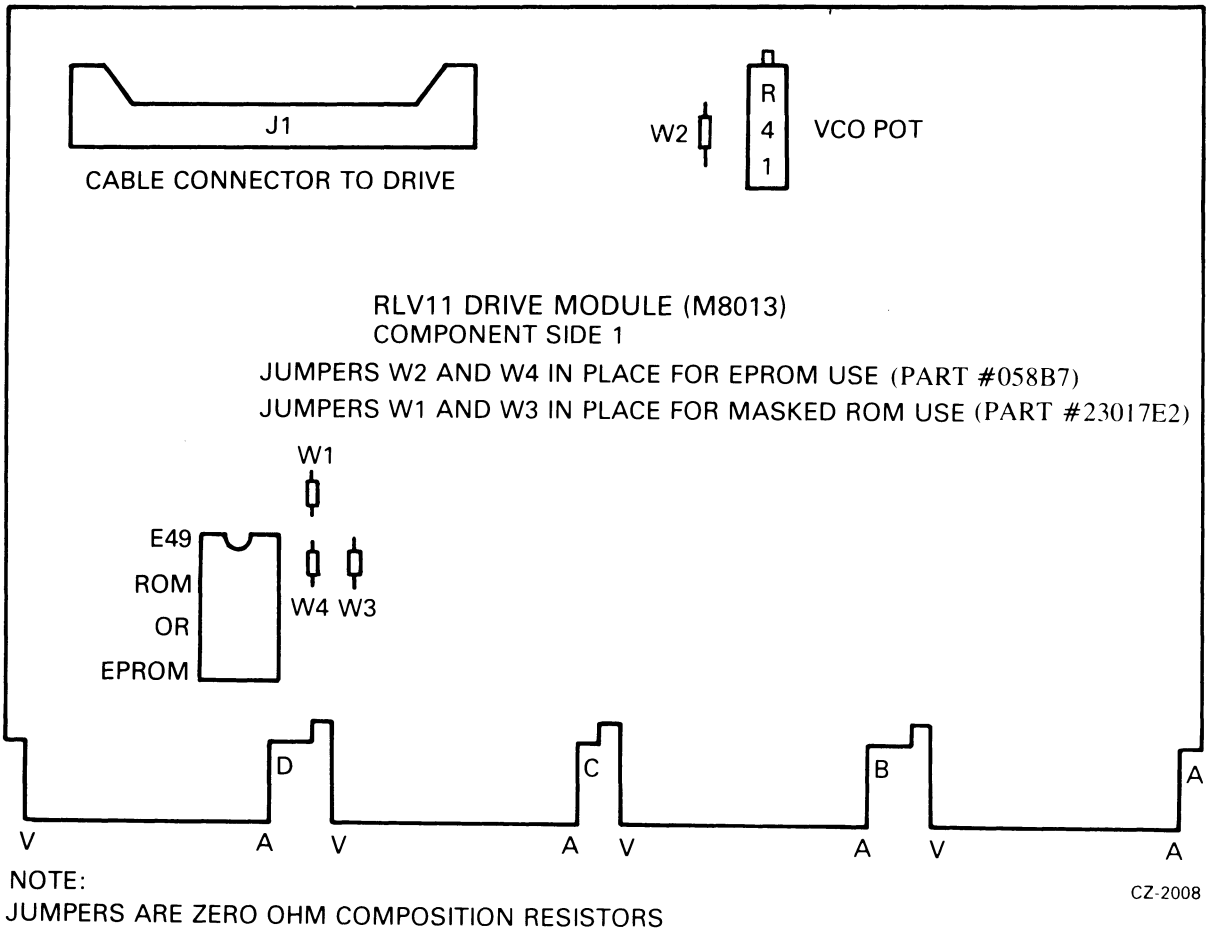


Figure 2-16 RLV11 Drive Module (M8013)

2.5.3 Module Slot Location

Modules M8013 and M8014 must be inserted into the H9273 backplane (Figure 2-17) such that the M8013 module is in the slot closest to the processor. Outside of this one restriction, the two modules can be inserted in any two unused slots. The controller priority level is based solely on its electrical distance from the microprocessor module in slot 1.

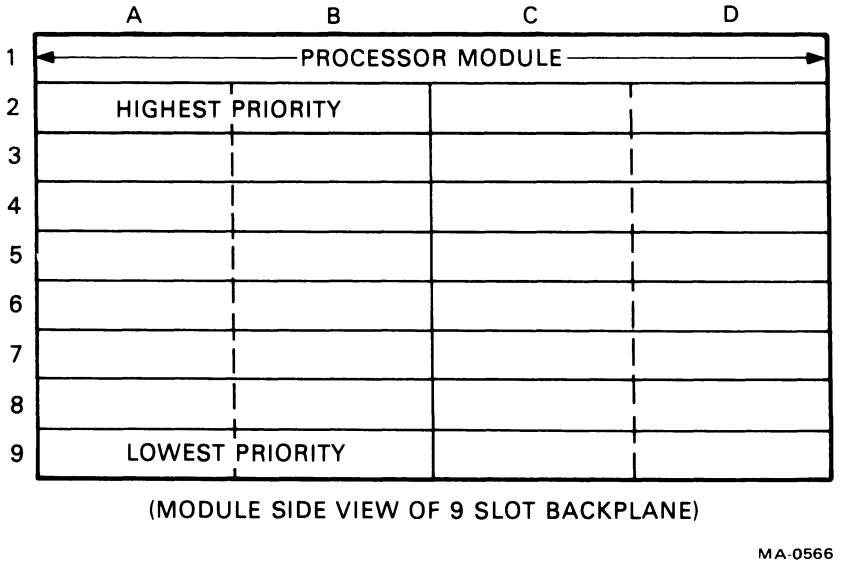


Figure 2-17 H9273 Backplane Grant Priority Structure

2.5.4 Module Installation

1. Using the normal configuration rules, select two adjacent slots in the backplane for the two controller modules.

2. Insert the ribbon cable (BC06R-XX) into J1 on the M8013 with the red stripe edge toward the top (Row A) of the module.

3. Insert the M8013 module into the selected slot that is closest to the processor.

4. Examine the M8014 to insure that the base address switches and the vector address switches are set correctly. Check jumpers W1 thru W4 for correctness. See Figures 2-14, 2-15, and 2-16.

5. Insert the M8014 module next to the M8013.

6. Install the transition bracket at the rear of the cabinet as shown in Figure 2-12. Assemble and install the transition connector.

7. Connect the other end of the ribbon cable with the red stripe up.

8. Apply system power and, using a suitable measuring device (i.e., digital voltmeter or equivalent), verify that the voltages are within the ranges specified below.

Voltage	Range	Test Point
Ground	AC2	
+5 Vdc	+4.75 Vdc to +5.25 Vdc	AA2
+12 Vdc	+11.5 Vdc to +12.5 Vdc	AD2
−5 Vdc	−5.25 Vdc to −4.75 Vdc	AL1 (M8013 only)

NOTE

The -5 Vdc is generated on the M8013 module. It is not adjustable but must be within specifications for proper operation. Module replacement is the only corrective procedure.

Measure all voltages between the ground test point and the appropriate voltage test point. If any adjustments to the power supply are necessary, refer to the appropriate power supply manual.

2.6 RLV12 CONTROLLER INSTALLATION

2.6.1 Introduction

The following paragraphs provide the user or installer with information to correctly configure and install the RLV12 in a 16-, 18-, or 22-bit LSI-11 bus. The user can change the device address, interrupt vector, and memory parity error abort feature.

2.6.2 Device Address Selection

Software control of the RLV12 is by means of four or five device registers – CSR, BAR, DAR, MPR, and BAE. Four registers are used for 16- or 18-bit addressing; five registers are used for 22-bit addressing. The bus address extension (BAE) register is added for upper address bit selection for 22-bit addressing. The usual device starting address is as follows.

Addressing Mode	Starting Address
16-bit	174400
18-bit	774400
22-bit	17774400

The first register, the CSR, is assigned the starting address and the other registers are assigned the next sequential addresses as shown in Table 2-3.

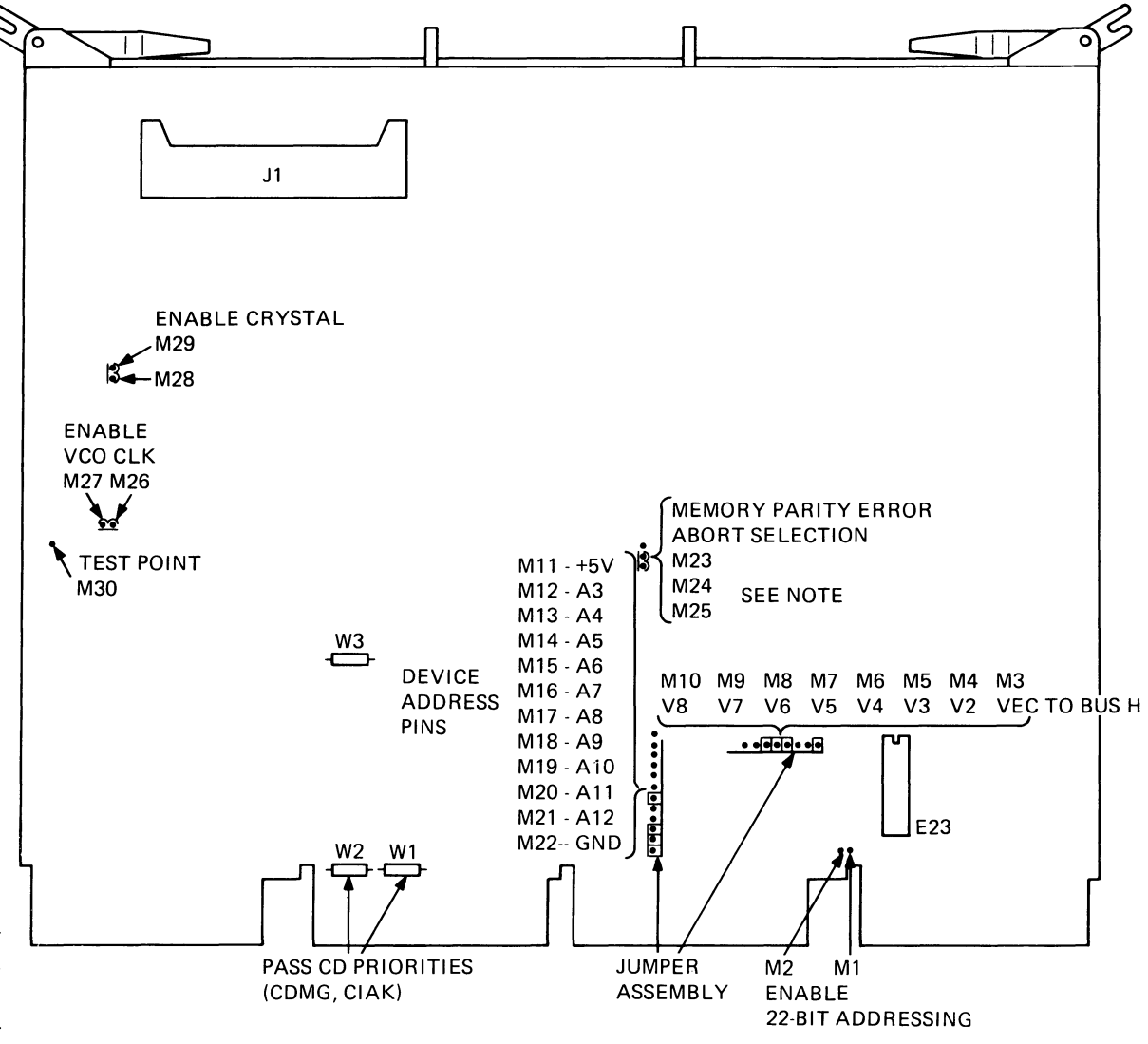
Table 2-3 Address Selection

	16-bit Addressing	18-bit Addressing	22-bit Addressing
Device Address			
Starting Address Range:	160000–177770	760000–777770	17760000–17777760
Starting Address:	174400	774400	17774400
No. of Registers:	4	4	8 (5 are used; 3 are not)
Registers Used:	CSR (174400) BAR (174402) DAR (174404) MPR (174406)	CSR (774400) BAR (774402) DAR (774404) MPR (774406)	CSR (17774400) BAR (17774402) DAR (17774404) MPR (17774406) BAE (17774410)
Jumpers Used:	Tie M22 ("**1**") to: M17, M20, and M21	Tie M22 ("**1**") to: M17, M20, and M21	Tie M22 ("**1**") to: M17, M20, and M21; Tie M11 ("**X**") to: M12
Interrupt Vector			
Vector Range:	0–774	0–774	0–774
Standard Vector:	160	160	160
Jumpers Used:	Tie M3 ("**1**") to: M6, M7, and M8	Tie M3 ("**1**") to: M6, M7, and M8	Tie M3 ("**1**") to: M6, M7, and M8

The device starting address is selected by jumpers for bits 3 through 12. These jumpers are shown in Figure 2-18. A jumper from the selected bit to ground (M22) decodes a **1**; no jumper decodes a **0**; and a jumper to +5 V (M11) decodes an **X (don't care)** condition. Figure 2-19 shows the RLV12 device starting address format.

NOTE

For 22-bit addressing, bit A3 is not decoded in the starting address.



NOTE:
THE MEMORY PARITY ERROR ABORT FEATURE IS AVAILABLE FOR USE WITH MEMORIES THAT HAVE PARITY ERROR CHECKING.
THIS FEATURE DOES NOT HAVE TO BE DISABLED FOR MEMORIES THAT DO NOT HAVE PARITY ERROR CHECKING. THE PINS ARE CONNECTED AS FOLLOWS:

CONNECTION	FUNCTION
M23 - M24	NO PARITY
M24 - M25	PARITY ERROR ABORT

Figure 2-18 RLV12 Jumper Locations

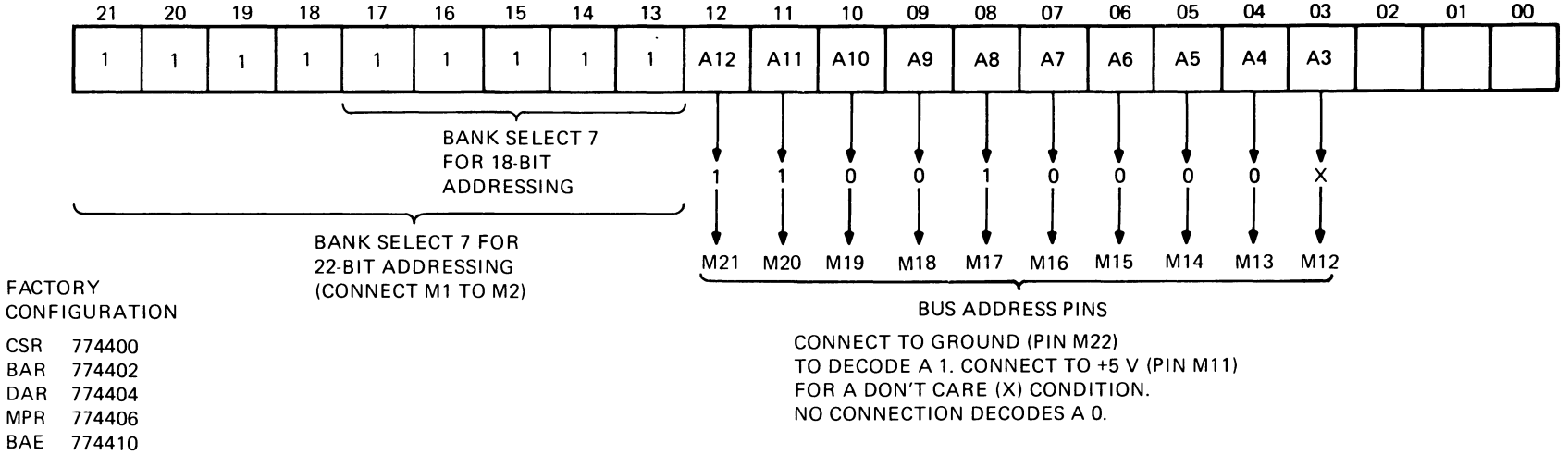


Figure 2-19 RLV12 Device Address Format

2.6.3 Bus Selection

The RLV12 module can be used on 16-, 18-, or 22-bit LSI-11 buses. When sent from the factory, the module operates on 16- or 18-bit buses. To enable the module to operate on a 22-bit extended LSI-11 bus, install jumper M1 to M2, shown in Figure 2-18. When installed, the jumper enables bank select 7 (BBS7) to be determined by the upper address bits (13–21). When the jumper is removed, the RLV12 has an 18-bit mode bank select 7 and can replace an existing RLV11 or RLV21 as the disk controller for RL01 and RL02 disk drives.

2.6.4 Interrupt Vector

The interrupt vector has a range of 0 to 774. The interrupt vector is preset at the factory to 160. The user may select another vector by changing the jumpers for bits V2–V8, as shown in Figure 2-20. A connection to VEC TO BUS H (M3, shown in Figure 2-18) generates a **1** for that bit; no connection generates a **0**.

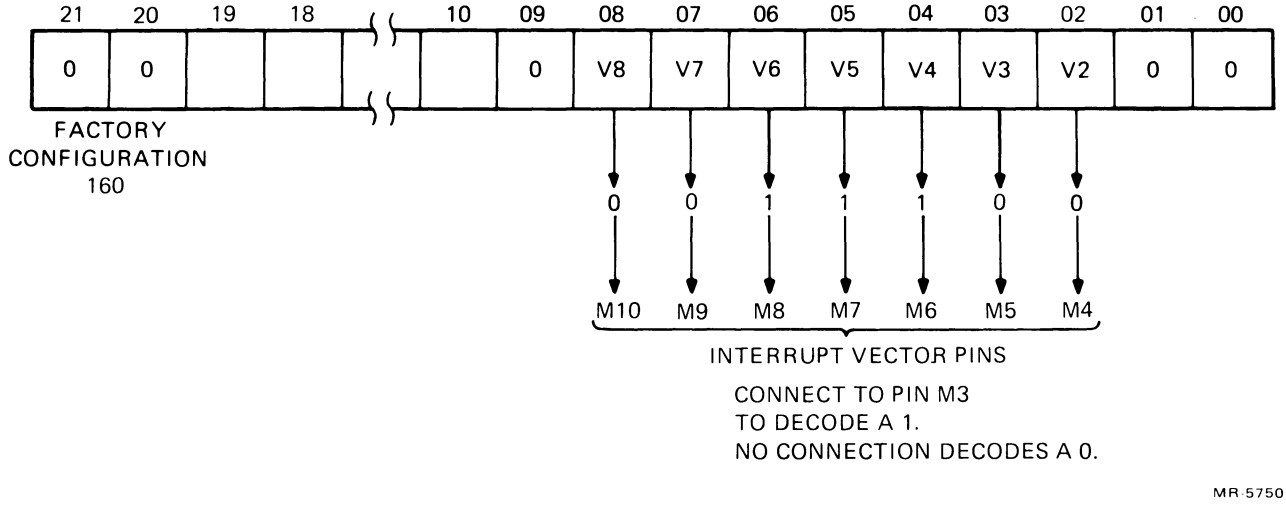


Figure 2-20 RLV12 Format Interrupt Vector

2.6.5 Interrupt Request Level

The RLV12 interrupts at priority level 4 determined by the interrupt chip E23, a DC003.

2.6.6 Memory Parity Error Abort Feature

When reading the system's optional memory with parity error detection, a parity error will set OPI and NXM of the CSR. This is a unique error condition that aborts the current command to the RLV12. This error abort feature is possible only with memories that have parity data bits.

The RLV12 is sent from the factory with the memory parity error abort feature enabled. To disable parity error abort, remove the jumper between pins M24 and M25 and install a jumper between pins M23 and M24 (see Figure 2-18). This feature does not have to be disabled for non-parity memories, as parity errors are not generated. Parity error abort uses data bits 16 and 17.

2.6.7 Other Jumpers

The module has two jumpers, W1 and W2, that enable priority signals to pass on the CD side of the module. The module has these jumpers installed and they should be left in when this controller is installed on the normal LSI-11 bus. If the RLV12 is installed in a C-D interconnect backplane with another module already in place, then these jumpers are removed. If the other module does not use the C-D interconnect scheme, then the status of jumpers W1 and W2 is not important.

Jumper	Signal
W1	CIAKI to CIAKO
W2	CDMGI to CDMGO

One jumper, W3, enables the word count register to automatically increment during a DMA operation. This jumper is used for factory testing and should be left in.

Two jumpers on the module disable the crystal oscillator and the voltage-controlled oscillator during factory testing. These jumpers should be left in.

Jumper	Oscillator
M26-M27	VCO
M28-M29	Crystal

2.6.8 Installation

The RLV12 can be installed in any quad LSI-11 bus slot. The controller's priority level is based on its electrical distance from the processor module. Use the following procedure to install the module.

1. Examine the module to make sure that the base address jumpers and vector address jumpers are set correctly. (See Paragraphs 2.6.2 and 2.6.4.)

2. Check jumpers M1 and M2 for enabling the correct bank select 7 (BBS7) for the 18- or 22-bit LSI-11 bus.

3. If desired, disable the memory parity error abort feature. This feature can only be used with system memories that have parity options, but this feature does not have to be disabled for non-parity memories. (See Paragraph 2.6.6.)

4. Insert the BC80M controller cable into J1 on the M8061.

5. Insert the M8061 in the selected slot in the LSI-11 bus.

6. Connect the other end of the BC80M cable to the drive.

7. Continue with the disk installation. (Refer to Paragraph 2.8.)

2.6.9 Acceptance Testing

The RLV12 controller is tested by running the RLV12 diskless diagnostic test and, if a drive is attached, by running the diagnostics that exercise the RL01 and RL02 disk drive. The diskless diagnostic should be run first. The RLV12 diagnostics are available on different media. Contact your local DIGITAL sales office for the types of media available and their part numbers.

Run the XXDP+ diagnostics in the following order.

1. CVRLB RLV12 Diskless Diagnostic (16-, 18-, or 22-bit mode)

NOTE

When the RLV12 is configured for 16- or 18-bit addressing, the RLV11 diskless diagnostic (CVRLA) is compatible with the RLV12 diskless diagnostic and checks the same logic.

2. CZRLG Controller Test Part 1
3. CZRLH Controller Test Part 2
4. CXRLI Drive Test Part 1
5. CZRLJ Drive Test Part 2
6. CZRLN Drive Test Part 3
7. CZRLK Performance Exerciser
8. CZRLL Compatibility Test
9. CZRLM Bad Sector File Utility

NOTE

The Bad Sector File Utility is not a diagnostic test. It is used by Field Service personnel to examine the bad sector file on the disk and to write entries into that file.

2.7 RL8A CONTROLLER INSTALLATION

2.7.1 Introduction

The RL8A OMNIBUS controller module (M8433) contains the following logic functions:

- Interface logic,
- Programmable registers,
- Silo data storage and control,
- Data formatting and error detection,
- Control microsequencer and timing logic,
- Drive bus interface logic.

NOTE

Adjustments on the RL8A are preset at the factory and are not to be changed in the field.

2.7.2 Module Slot Location

The module can be inserted into any unused OMNIBUS hex-height slot between the CPU and the first memory element. The controller is connected to the first drive via a BC80J-20 interface cable. Connections between drives are made using a BC20J-XX (70-12122-10) cable.

2.7.3 Module Installation

1. Remove the M8433 module (see Figure 2-21) and interface cable (BC80J-20) from the shipping container and inspect them for physical damage.

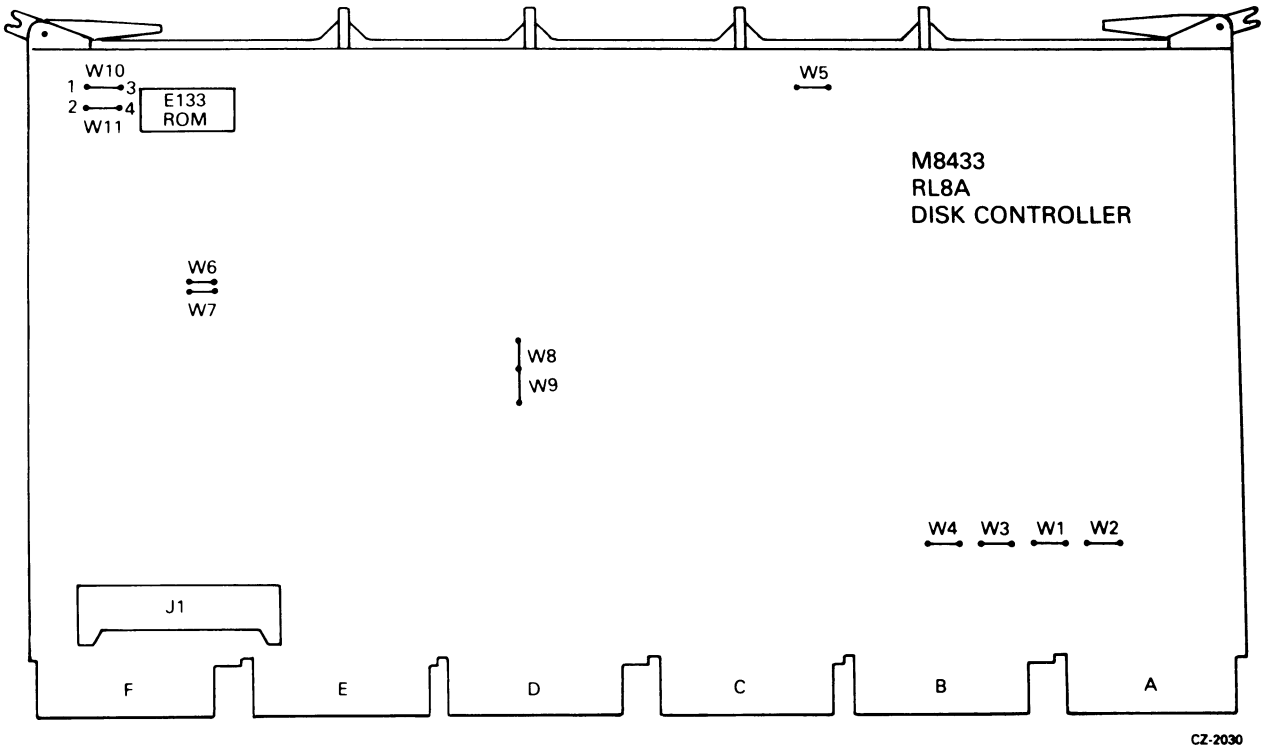


Figure 2-21 RL8A Jumpers

2. Verify the proper jumper configuration for device codes and priority (Figure 2-21).

Device Code	**W1**	**W2**
60,61	IN	OUT
62,63	IN	IN

Break Priority	**W3**	**W4**	**W5**
0	IN	OUT	IN
1	OUT	IN	OUT

NOTE

The RL8A is shipped from the factory with a priority of 0.

Device Type	**W8**	**W9**
RL01	OUT	IN
RL02	IN	OUT

ROM Type (E133)	W10	W11	W6	W7
012E2	OUT	IN	IN	OUT
8708 or 2708	IN	OUT	OUT	IN

3. Position the BC80J-20 interface-to-drive cable in the PDP-8 chassis and connect the Berg connector to the M8344 module.

4. Install the M8344 module into selected slot in the OMNIBUS backplane.

5. Route the cable out to where the first drive will be installed.

2.8 RL01/RL02 DISK DRIVE INSTALLATION

2.8.1 Unpacking and Inspection

1. When delivered, each drive and its associated cabinetry is enclosed by a heavy cardboard carton. If the drive is shipped with a system and mounted in a cabinet, then the carton is attached to a shipping skid (Figure 2-22). Remove the plastic straps that secure the shipping carton to the skid.

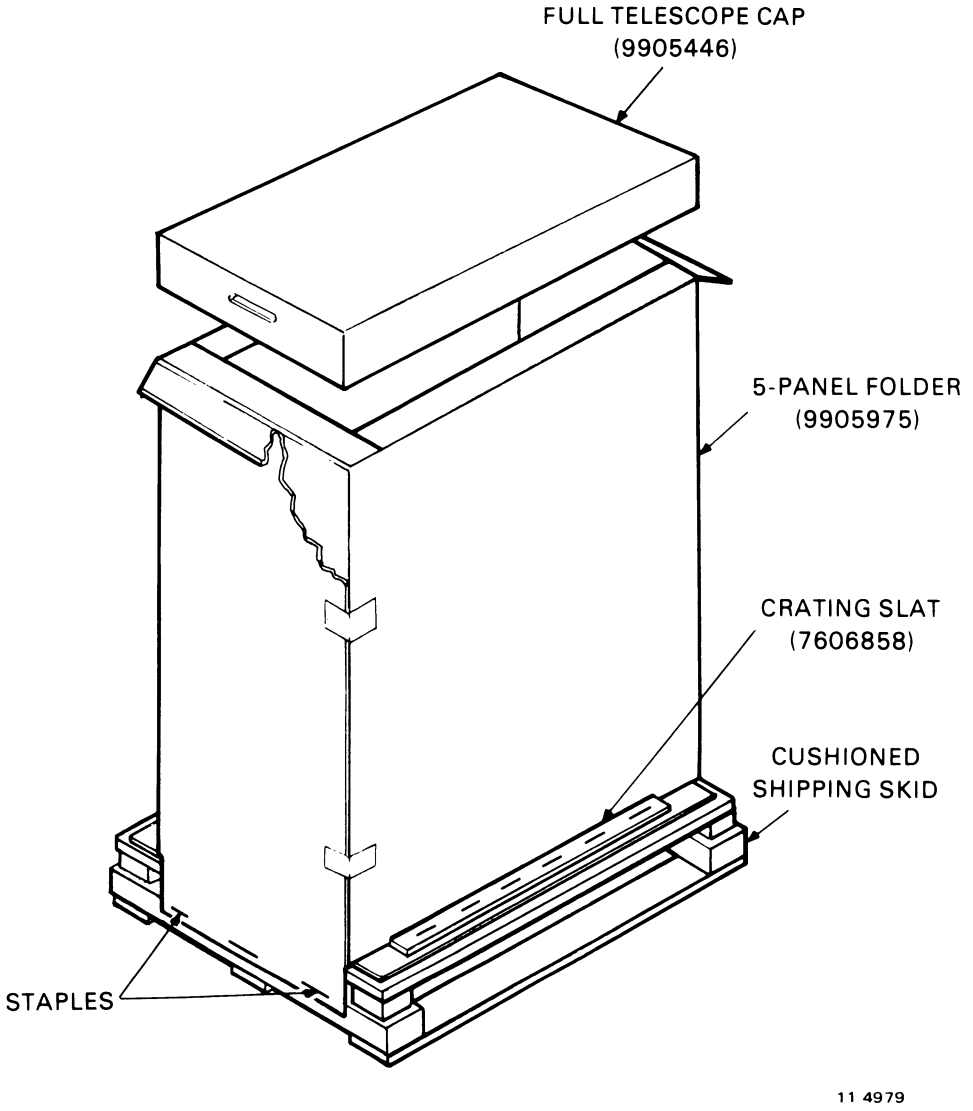


Figure 2-22 H950 Shipping Package

2. Remove the lid from the top of the carton.

3. Remove the staples that fasten the wooden crating slats and carton flanges to the skid.

4. Remove the shipping carton.

5. Inspect the cabinet and drive for signs of damage. Retain all packing material and receipts in the event that any claims for shipping damage must be filed. All claims should be filed promptly with the transportation company.

2.8.2 RL01/RL02 Disk Drive Unit Mounting

NOTE

If the RL01/RL02 is to be mounted in an H950 cabinet, the shipping brackets must be retained and refitted after installation. This is the only way to prevent the drive from sliding while repositioning or moving the H950 cabinet.

The drive may be shipped in a rack or cabinet as an integral part of a system or may be shipped in a separate container for addition to an existing system.

If the drive is to be installed in an existing rack or cabinet, install the chassis slides first as described in Steps 1 through 6 below (Figure 2-23). The procedure for installing the drive itself begins with Step 7.

1. Install cabinet stabilizers before mounting the drive.

2. Remove the slides from the carton. (Retain the hardware for reassembly.)

3. Install slides into the rack or cabinet using enclosed hardware. Be sure the slides are at the correct height to permit installation of pop panels (dress panels) upon completion of installation. Also verify that the slides do not bind on any hardware used to mount the slide.

4. Extend slides to lock position.

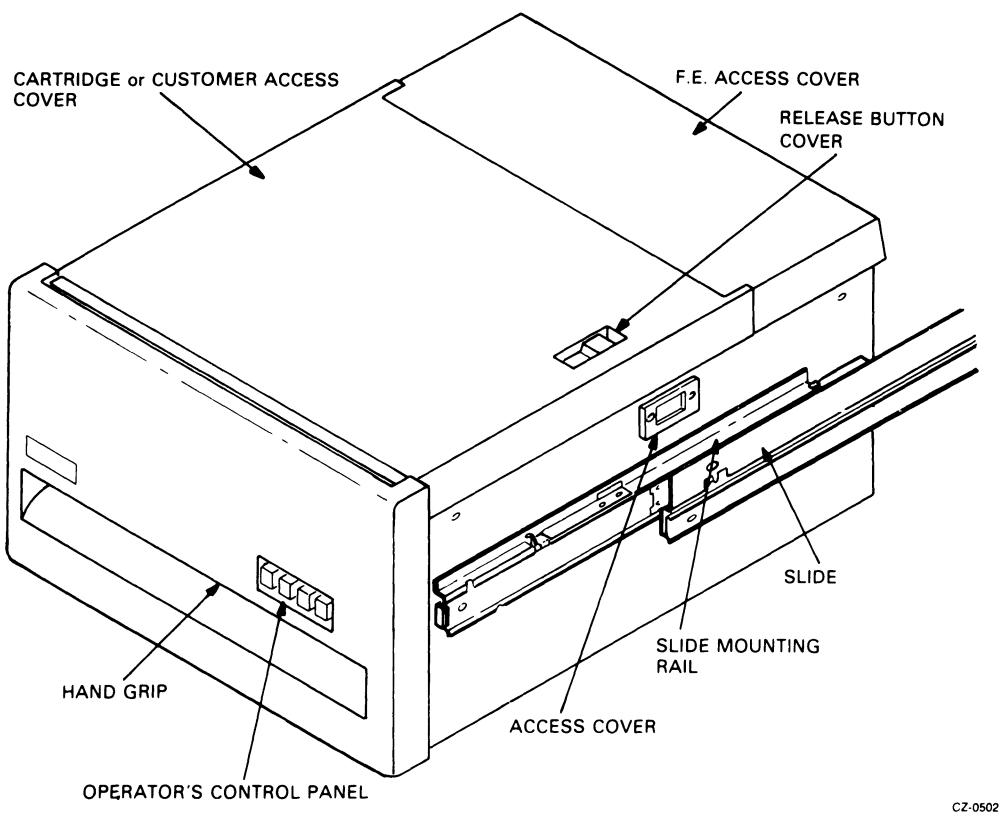


Figure 2-23a RL01/RL02 Cabinet Installation

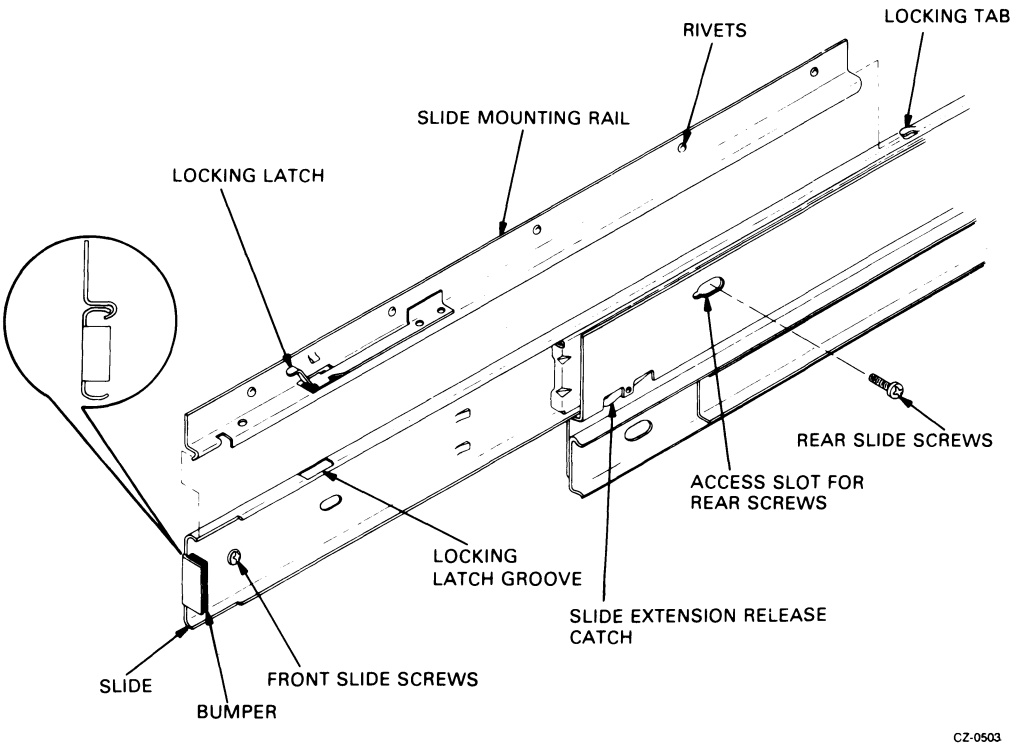


Figure 2-23b RL01/RL02 Cabinet Installation

5. Place drive onto chassis slides and reinstall mounting hardware.

   a. Figure 2-23 shows the relationship between the drive, slide mounting rails, and slides. Note first the position of the slide mounting rails. These rails are currently riveted to the sides of the drive.

   b. The cabinet slides fit under the edge of the mounting rails. The forward edge of the mounting rails are curved to grip the curled edge of the slides (see Figure 2-23a, 2-23b, and detailed view A).

   c. At the rear of each slide is a locking tab that grips the top rear edge of the rail (Figure 2-23b).

   d. The drive should be carefully placed on top of the slides hooking the front and rear of each slide as previously described.

   e. When properly placed, the locking latch (Figure 2-23b) on each mounting rail drops into a groove on each slide. This holds the drive securely so that the screws may be inserted to bolt the front of each slide to the drive (Figure 2-23b).

   f. After bolting the front of each slide, adjust the length of the slide (using the slide extension release catch) so that the rear slide screw may be inserted (Figure 2-23b).

6. Ensure that the disk drive moves easily on the slides, that there is no binding in the cabinet, and that the proper height has been maintained for dress panels.

7. Open the drive access cover by loosening the four captive fasteners holding the module access cover. When the screws are sufficiently loosened to raise the cover, the drive access cover may then be lifted off the drive. The module access cover may be rested on the rear lip of the drive (Figure 2-24).

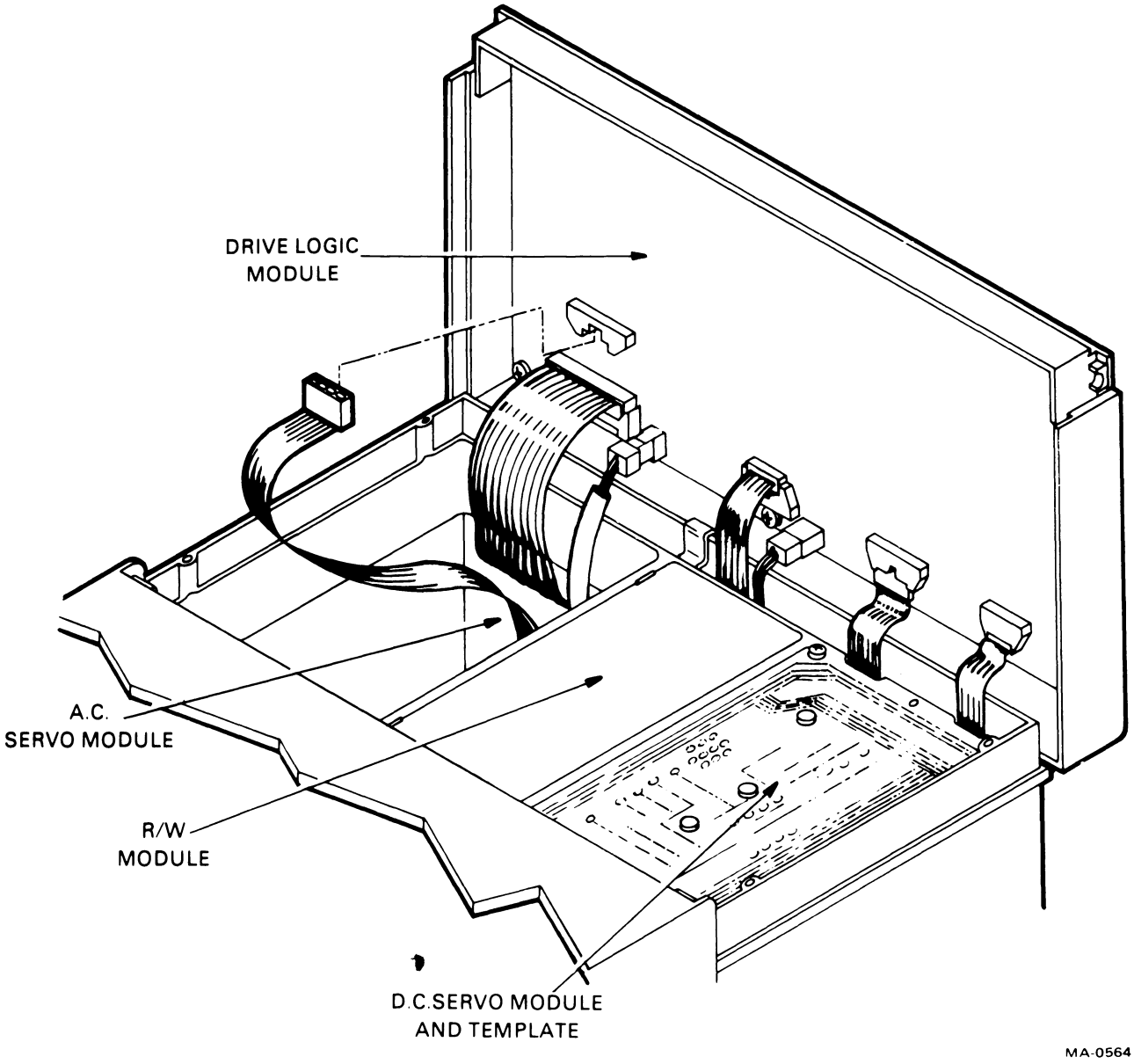


Figure 2-24 RL01/RL02 Disk Drive – Exposed Drive Logic Module

8. Loosen the head restraining bracket screw located on the positioner. Turn the bracket 90 degrees and retighten the screw (Figure 2-25).

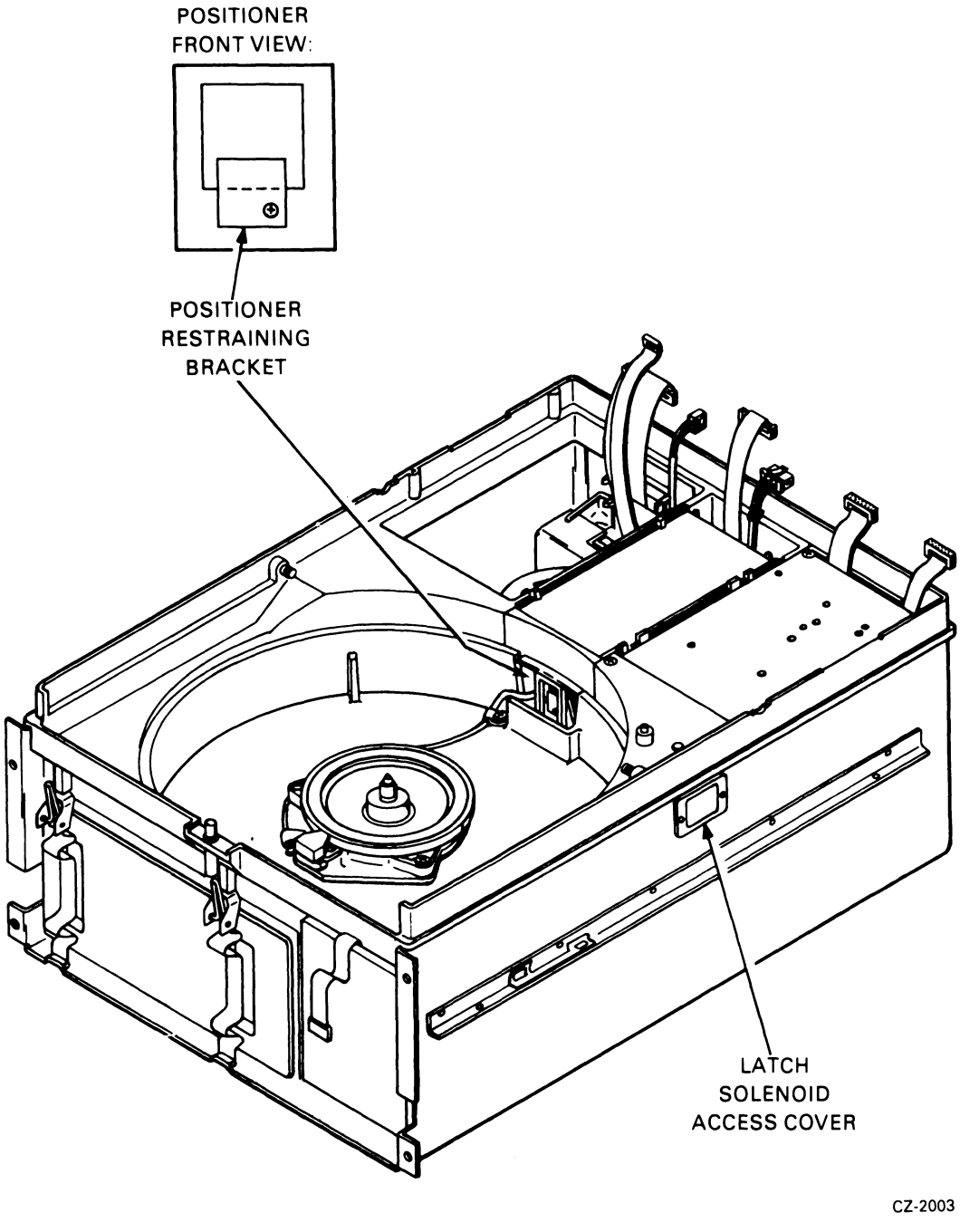


Figure 2-25 RL01/RL02 – Covers Removed

9. On newer drives there are two shipping screws on the bottom of the unit that secure the spindle/blower motor. Remove the screws.

10. If the drive is being installed in a dual-drive cabinet that has an interlock system to prevent more than one drive being extended at a time, ensure that the interlock is connected.

11. Inspect the terminal block covers at the rear of the drive. Ensure that they are configured properly for the input power available (Figure 2-26).

CAUTION
Connection to the wrong power source will result in serious damage to the disk drive.

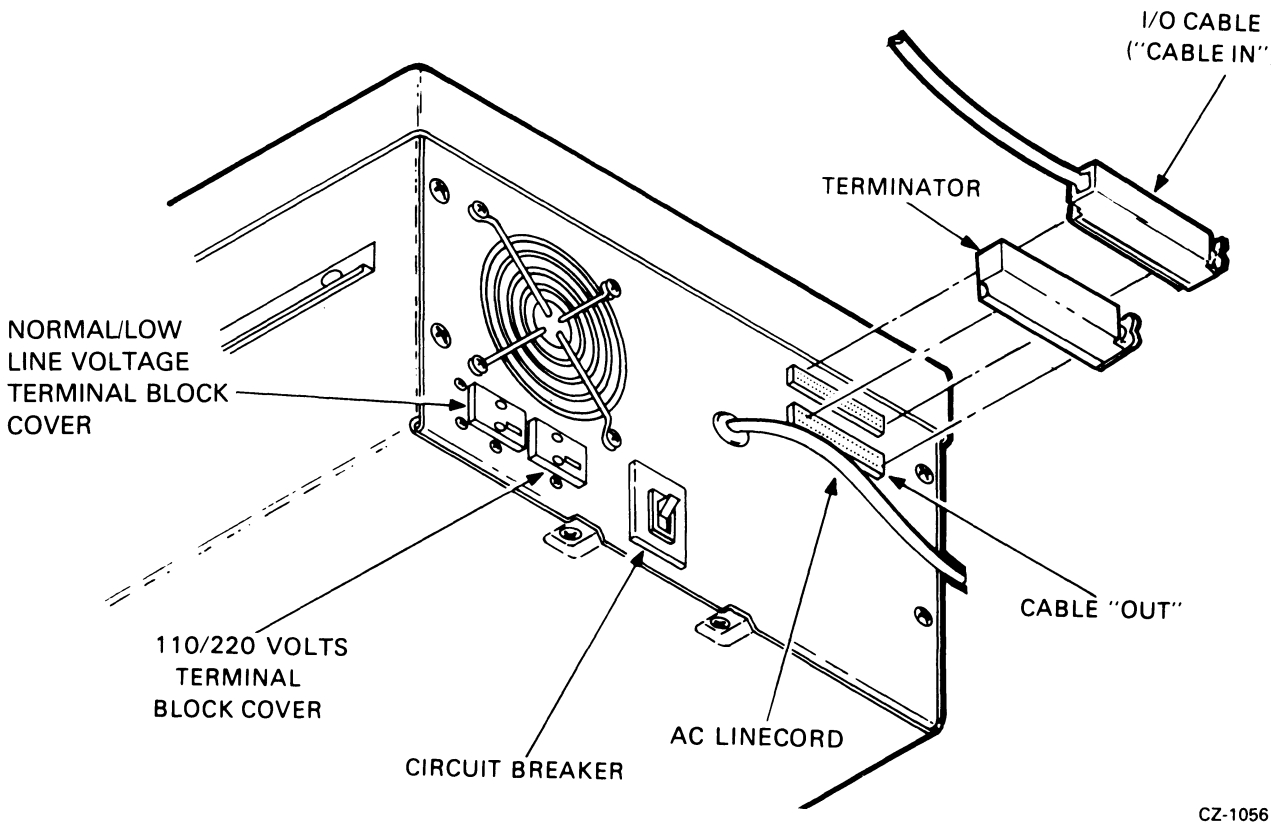


Figure 2-26 RL01/RL02 Disk Drive – Rear View

NOTE
On newer-drives, a shielded cable is used. Its part number is BC21Z-XX.

12. If there is only one disk drive in the system, or if this is the last drive of the daisy chain, install a terminator assembly (DIGITAL part no. 70-12293) in the "cable out" location at the rear of the drive (Figure 2-26).

13. If this is an RL11- or an RLV11-based system, route the I/O cable BC20J-XX (DIGITAL part no. 70-12122-10) between the first drive and the transition connector. If this is an RL8A-based system, route the BC80J-20 cable from the RL8A to the first drive. If this is an RLV12-based system, route the BC80M-6 between the RLV12 and the first drive.

14. If this is a multidrive installation, connect an I/O cable from "cable in" of this drive to the "cable out" connector of the previous drive. Repeat for each drive.

NOTE
The total length of cable from controller to the last drive must not exceed 30 m (100 ft).

15. Install the proper unit-select plug at the front of the drive (Figure 2-27).

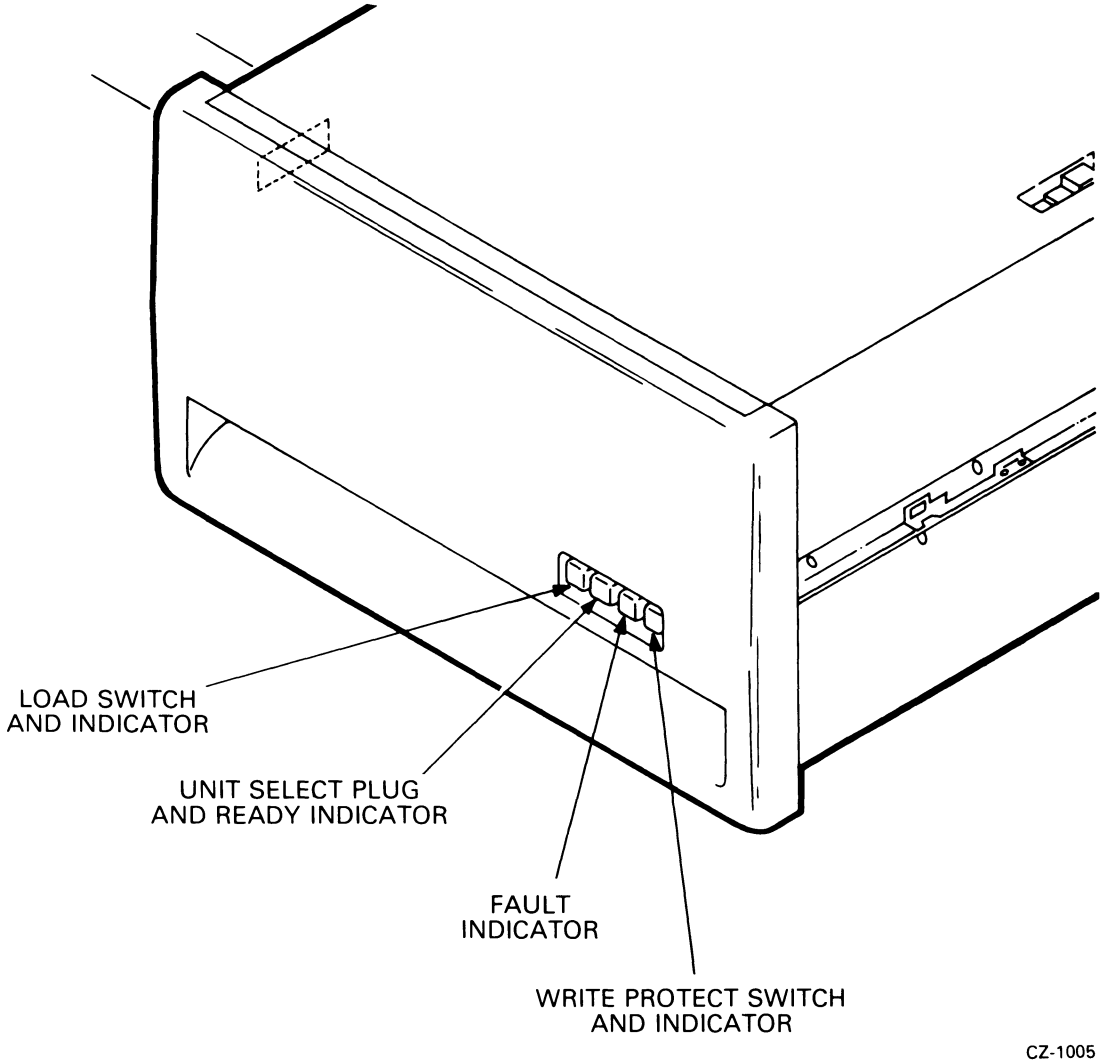


Figure 2-27 RL01/RL02 Disk Drive – Front View

2.8.3 Drive Prestartup Inspection

With the drive power off, follow these steps.

NOTE
If a problem occurs, consult the RL01/RL02 Technical Manual.

1. Ensure that the positioner restraining bracket is secured out of position to prevent interference with the positioner (Figure 2-25).

2. Ensure that the positioner is home.

3. Ensure that the read/write head gimbals are not bent or dirty. (If they are dirty, clean with a solution of 91 percent alcohol and 9 percent water and a lint-free wiper.

4. Ensure that the spindle rotates freely and its top surfaces are not dirty. (Clean as described above.)

5. Ensure that the brush assembly is home (not exposed).

NOTE

An engineering change has eliminated the need for brushes on the drive. On newer RL01 and RL02 drives, the brush assembly has been replaced with a unit containing only the cartridge-in-place and top cover interlock. The Drive Logic Module also contains some logic changes to accommodate the brush cycle removal.

6. Ensure that the logic modules and connectors are seated firmly.

7. Turn CB1 ON.

8. Ensure that the spindle rotates slowly counterclockwise for approximately 15 seconds and stops. At this time, the LOAD light will come on.

NOTE

On the newer drives (without brushes), the spindle will NOT rotate until both the top cover and the cartridge-in-place interlocks are depressed.

9. Ensure that the FAULT light is not on.

10. Ensure that the cooling fan at the rear of the drive is operating.

11. On the newer drives, release the top cover and cartridge-in-place interlocks, noting that the spindle stops rotating.

12. Using a suitable measuring device (i.e., digital voltmeter or equivalent), ensure the following drive voltages are within the specified tolerances.

Voltage	Range	Test Point
+15 UNREG	(+15.0 to +18.0 Vdc)	+V UNREG
−15 UNREG	(−15.0 to −18.0 Vdc)	−V UNREG
+5 REG	(+4.48 to +5.1 Vdc)	TP8
+8 REG	(+7.7 to +8.3 Vdc)	TP4
−8 REG	(−7.7 to −8.3 Vdc)	TP5

See Figure 2-24 for dc servo module location. Test points are located on the mask covering the dc servo module.

13. Verify that the WRITE PROTect switch cycles in and out and the indicator lights up when the switch is pressed.

14. Verify that the LOAD switch cycles in and out and the indicator light goes out when the switch is pressed. Return switch to the "out" position.

15. Turn off CB1.

16. Reinstall the top cover and secure with the captive screws.

17. Ensure that the drive access cover cannot be opened.

18. Turn CB1 on and ensure the drive access cover will open.

2.8.4 Drive Startup Operation Check

1. With the drive power ON, install a scratch cartridge as described in Paragraph 3.3.

2. Close the cover, press the LOAD switch and note the following.

   - The LOAD light will go out.

   - When the cartridge reaches nominal speed (after approximately 30 seconds), a brush cycle commences on those drives that have brushes. When the brushes have returned home, the read/write heads will load and approach cylinder 0. When the heads have locked onto cylinder 0, the READY light will illuminate. The total time for this process is approximately 45 seconds.

3. Press the LOAD switch again. The READY light should go off and the read/write heads should retract to their home position. The spindle should slow down and then come to a complete stop after about 30 seconds. The LOAD light should illuminate when the spindle has stopped.

4. If the drive startup operation check detailed above is successfully completed (i.e., the READY indicator illuminates), run the subsystem confidence tests described in Paragraph 2.9. If there is a problem, consult the *RL01/RL02 Technical Manual.*

2.9 CONFIDENCE TESTING

Confidence testing consists of running the diagnostic programs. Each diagnostic has a listing that contains operating instructions. Each listing explains system hardware requirements, software environment, which features are tested and how they are tested, program options and how to select them, how to interpret printouts, error handling, device information tables, dialogue with the Diagnostic Supervisor, and complete operating instructions. The listings are available as hard copy printouts or on microfiche.

The binary form of the diagnostic programs are available on various media. It is always advisable to keep a copy of the RL01/RL02 diagnostics on a media other than the RL01K or RL02K cartridge so that the diagnostics can be loaded through another device if the RL subsystem is down.

The old MAINDEC naming system is replaced with a new naming system. Manual and microfiche designations are also converted. In addition, part numbers are assigned that conform to DIGITAL's standard twelve character part numbering system.

When ordering diagnostic media, listings, manuals, or microfiche, check the current catalog or index for the latest revision level. The applicable catalogs and indexes are listed in Table 2-4. Unless otherwise specified when ordering, the latest revision will be shipped.

Table 2-4 Diagnostic Catalogs and Indexes

Name	Part Number
PDP-11 Diagnostic Software Components Catalogue*	AV-B021E-TC
PDP-8 Software Components Catalogue*	AV-0872B-TA
PDP-11 Maindec Index (microfiche)	AH-9026P-MC
PDP-8 Maindec Index (microfiche)	AH-6572G-MA

* Both of these catalogs are available on microfiche (EP-08/11)

2.9.1 RL11-Based Diagnostics

The diagnostic package used for an RL11/RL01 subsystem before the release of the RL02 consisted of the six free-standing programs listed in Table 2-5. There were two revisions, Revision A and Revision B. These programs handled only RL01 drives (not RL02 units).

Table 2-5 RL11-Based Diagnostics

Part Number	Description
CZRLAA0	Controller Test Part 1
CZRLBA0	Controller Test Part 2
CZRLCA0	Drive Test Part 1
CZRLDA0	Drive Test Part 2
CZRLEA0	Performance Exerciser
CZRLFA0	Drive Compatibility Test

These diagnostics can be run free-standing under the Diagnostic Supervisor, manually under XXDP, chainable under XXDP (except CZRLFA0 which requires manual intervention), or under manufacturing checkout environments such as SLIDE or ACT-11.

A new diagnostic package is available to test either an RL01 or an RL02 unit. The kit numbers are listed in Table 2-6 and the contents of the tests are shown in Table 2-7.

Table 2-6 RL11 Diagnostic Kit Numbers

Part Number	Description
ZJ283-RB	Documentation and paper tape
ZJ283-RZ	Documentation only
ZJ283-PB	Paper tape only
ZJ283-FR	Microfiche only

Table 2-7 RL11 Diagnostic Components

Part Number	Name	Item
AC-F111A-MC	CZRLGA0 Controller Test #1	Documentation
AH-F110A-MC		Fiche
AK-F108A-MC		Paper tape #1
AK-F109A-MC		Paper tape #2
AF-F111A-M0		DECO
AC-F115A-MC	CZRLHA0 Controller Test #2	Documentation
AH-F114A-MC		Fiche
AK-F112A-MC		Paper tape #1
AK-F113A-MC		Paper tape #2
AF-F115A-M0		DECO
AC-F119A-MC	CZRLIA0 Drive Test #1	Documentation
AH-F118A-MC		Fiche
AK-F116A-MC		Paper tape #1
AK-F117A-MC		Paper tape #2
AF-F119A-M0		DECO
AC-F123A-MC	CZRLJA0 Drive Test #2	Documentation
AH-F122A-MC		Fiche
AK-F120A-MC		Paper tape #1
AK-F121A-MC		Paper tape #2
AF-F123A-M0		DECO
AC-F127A-MC	CZRLKA0 Performance Exerciser	Documentation
AH-F126A-MC		Fiche
AK-F124A-MC		Paper tape #1
AK-F125A-MC		Paper tape #2
AF-F127A-M0		DECO

Table 2-7 RL11 Diagnostic Components (Cont)

Part Number	Name	Item
AC-F131A-MC	CZRLLA0 Drive Compatibility Test	Documentation
AH-F130A-MC		Fiche
AK-F128A-MC		Paper tape #1
AK-F129A-MC		Paper tape #2
AF-F131A-M0		DECO
AC-F135A-MC	CZRLMA0 Bad Sector File Utility	Documentation
AH-F134A-MC		Fiche
AK-F132A-MC		Paper tape #1
AK-F133A-MC		Paper tape #2
AF-F135A-M0		DECO

There is a new program added to the package named CZRLMA0. It is used to read the Bad Sector File and can be used to write entries into the field writable portion of the Bad Sector File. This program is not a diagnostic and should not be used as one. It assumes that the system is functioning properly.

In addition to the free-standing diagnostics, there is a DECX11 module for use with the DECX11 System Exerciser. Revision A (RLAA) will operate an RL01 drive only. Revision B or later (RLAB) will operate either an RL01 or an RL02.

There is also an RL subsystem driver for the Maintenance Program Generator (MPG).

The binary form of the diagnostics are included as part of XXDP. This makes them available on media for the RK05, RK06, RK07, RL01, RX01, DECtape, magnetic tape, and DECassette.

The use of XXDP, DECX11, and MPG is explained in the manuals listed in Table 2-8.

Table 2-8 User Documents

Part Number Hard Copy	Part Number Microfiche	Name
AC-9093I-MC	EP-DZQXA-J-D	CZQXAI0 XXDP User Guide
AC-8240Z-MC	AH-8242Z-MC	CXQBAZ0 DECX11 User Document
AC-816JC-MC	EP-DTUMA-C-D	CTUMAC0 M.P.G. User Manual

2.9.2 RLV11-/RLV12-Based Diagnostics

With one exception, the RLV11/RLV12 controller-based subsystem is tested with the same set of diagnostics as the RL11 controller subsystem. The RLV11 and RLV12 each has an internal maintenance feature that is not tested by the RL11 diagnostics. Therefore, for the RLV11 subsystem, there is an additional diagnostic program called the CVRLAA0 Diskless Test. RLV12 subsystems use the CVRLBA Diskless Test. {At some point in time, this test (CVRLBA) will replace CVRLAA.}

The diagnostic kit includes the same items as the RL11 diagnostic kit plus the CVRLAA0 test. The RLV11/RLV12 kit designations are shown in Table 2-9.

Table 2-9 RLV11/RLV12 Diagnostic Kit Designations

Designation	Contents
ZJ285-RB	Documentation and paper tape
ZJ285-RZ	Documentation only
ZJ285-PB	Paper tape only
ZJ285-FR	Microfiche only

The DECX11 module is the same one used for the RL11.

2.9.3 RL8A-Based Diagnostics

There are six free-standing diagnostic programs for the RL8/RL01 system. There is also a DECX8 module for use with the DECX8 System Exerciser. These diagnostics are available in a kit (see Table 2-10) or as individual components (see Table 2-11) and are for use with the RL01 only.

Table 2-10 RL8/RL01 Diagnostic Kits

Part Number	Contents
ZB233-RB	Documentation and paper tape
ZB233-RZ	Documentation only
ZB233-PB	Paper tape only
ZB233-FR	Microfiche only

Table 2-11 RL8/RL01 Diagnostic Components

Part Number	Designation
AC-C656A-MA	AJRLAA0, RL8A Diskless Control Test (Document)
AH-C657A-MA	AJRLAA0, RL8A Diskless Control Test (Fiche)
AK-C658A-MA	AJRLAA0, RL8A Diskless Control Test (Paper tape)
AL-C659A-NA	AJRLAA0, RL8A Diskless Control Test (DECtape)
AC-C660A-MA	AJRLBA0, RL8A/RL01 Drive Test 1 (Document)
AH-C661A-MA	AJRLBA0, RL8A/RL01 Drive Test 1 (Fiche)
AK-C662A-MA	AJRLBA0, RL8A/RL01 Drive Test 1 (Paper tape)
AL-C663A-NA	AJRLBA0, RL8A/RL01 Drive Test 1 (DECtape)
AC-C664A-MA	AJRLCA0, RL8A/RL01 Drive Test 2 (Document)
AH-C665A-MA	AJRLCA0, RL8A/RL01 Drive Test 2 (Fiche)
AK-C666A-MA	AJRLCA0, RL8A/RL01 Drive Test 2 (Paper tape)
AL-C667A-NA	AJRLCA0, RL8A/RL01 Drive Test 2 (DECtape)
AC-C668A-MA	AJRLDA0, RL8A/RL01 Compat. Verify (Document)
AH-C669A-MA	AJRLDA0, RL8A/RL01 Compat. Verify (Fiche)
AK-C670A-MA	AJRLDA0, RL8A/RL01 Compat. Verify (Paper tape)
AL-C671A-NA	AJRLDA0, RL8A/RL01 Compat. Verify (DECtape)
AC-C672A-MA	AJRLEA0, RL8A/RL01 Perf. Exer. (Document)
AH-C673A-MA	AJRLEA0, RL8A/RL01 Perf. Exer. (Fiche)
AK-C674A-MA	AJRLEA0, RL8A/RL01 Perf. Exer. (Paper tape)
AL-C675A-NA	AJRLEA0, RL8A/RL01 Perf. Exer. (DECtape)
AC-C676A-MA	AXRLAA0, RL8A DECX8 Module (Document)
AH-C677A-MA	AXRLAA0, RL8A DECX8 Module (Fiche)
AK-C678A-MA	AXRLAA0, RL8A DECX8 Module (Paper tape)
AC-C682A-MA	AJRLGA0, RL8A/RL01 Pack Verify (Document)
AH-C683A-MA	AJRLGA0, RL8A/RL01 Pack Verify (Fiche)
AK-C684A-MA	AJRLGA0, RL8A/RL01 Pack Verify (Paper tape)
AL-C685A-NA	AJRLGA0, RL8A/RL01 Pack Verify (DECtape)

There are six free-standing diagnostic programs for the RL8/RL02 subsystem, plus a module for use with the DECX8 System Exerciser. They are available in kit form (Table 2-12) or as individual components (Table 2-13). The Diskless Controller Test (AJRLACO) is simply Revision C of the RL01 test and can test a subsystem with either RL01 or RL02 units. The other diagnostics test RL02-based systems only.

Table 2-12 RL8A Diagnostic Kits

Part Number	Contents
ZF241-RB	Documentation and paper tape
ZF241-RZ	Documentation only
ZF241-PB	Paper tape only
ZF241-FR	Microfiche
ZF241-PH	RL02
ZF241-RH	RL02 and documentation

Table 2-13 RL8/RL02 Diagnostic Components

Part Number	Name	Item
AC-C656C-MA	AJRLAC0 RL8A Diskless Control Test	Documentation
AH-C657C-MA		Fiche
AK-C658C-MA		Paper tape
AL-C659C-NA		DECtape
AK-F362A-MA	AJRLHA0 RL8/RL02 Seek/Function	Documentation
AH-F363A-MA		Paper tape
AH-F364A-MA		Fiche
AL-F365A-MA		DECtape
AF-F362A-M0		DECO/DEPO
AC-F366A-MA	AJRIA0 RL8/RL02 Read/Write	Documentation
AK-F367A-MA		Paper tape
AH-F368A-MA		Fiche
AL-F369A-MA		DECtape
AF-F366A-M0		DECO/DEPO
AC-F370A-MA	AJRLJAO RL8/RL02 Drive Compat.	Documentation
AK-F371A-MA		Paper tape
AH-F372A-MA		Fiche
AL-F373A-MA		DECtape
AF-F370A-M0		DECO/DEPO
AC-F374A-MA	AJRLKA0 RL8/RL02 Perf. Exer.	Documentation
AK-F375A-MA		Paper tape
AH-F376A-MA		Fiche
AL-F377A-MA		DECtape
AF-F374A-M0		DEPO/DECO

Table 2-13 RL8/RL02 Diagnostic Components (Cont)

Part Number	Name	Item
AC-F378A-MA	AJRLLA0 RL8/RL02 Pack Verify	Documentation
AK-F379A-MA		Paper tape
AH-F380A-MA		Fiche
AL-F381A-MA		DECtape
AF-F378A-M0		DECO/DEPO
AC-F382A-MA	AXRLBA0 DEC/X8 MOD RL8/RL02	Documentation
AK-F383A-MA		Paper tape
AH-F384A-MA		Fiche
AF-F38SA-M0		DECO/DEPO

2.10 USE OF THE M9312 BOOTSTRAP WITH AN RL11 SUBSYSTEM

The M9312 module is used on many PDP-11 UNIBUS systems to provide bootstrap capability as well as other functions. The module has five IC sockets for ROM chips, four of which are reserved for peripheral bootstrap programs. There are several ROM chips available for the different peripheral devices, and an M9312 is configured by selecting the appropriate chips for the particular system on which it is used.

The RL subsystem bootstrap program is contained in ROM chip number 23-751A9. This chip can be ordered individually and is also available in kit MR11-EA, which consists of an M9312 module plus all the available ROM chips.

An RL system disk can be booted by a command to the console emulator (a program that is a feature of the M9312). The device mnemonic for the RL11 is DL or DLn, where n is the unit number (0 through 3).

More information on the M9312 is available in the *M9312 Technical Manual.* It is available in printed form (EK-M9312-TM) or on microfiche (EP-M9312-TM).

CHAPTER 3
OPERATOR'S GUIDE

3.1 INTRODUCTION

This chapter describes the function of all external controls on the RL01/RL02 disk drive and explains how to operate the subsystem.

3.2 CONTROLS AND INDICATORS

Figures 3-1 and 3-2 show all the drive controls and indicators.

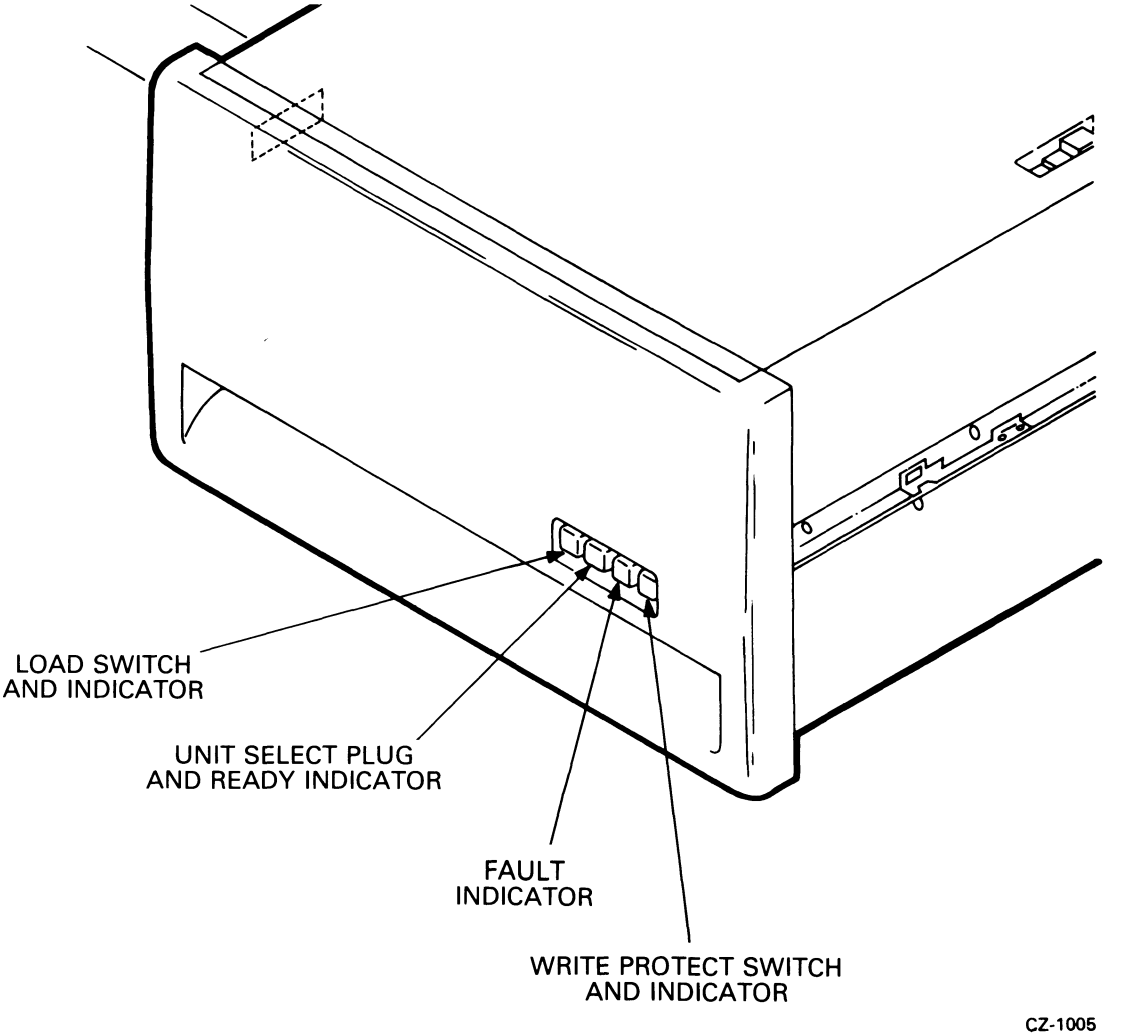


Figure 3-1 RL01/02 Disk Drive – Front View

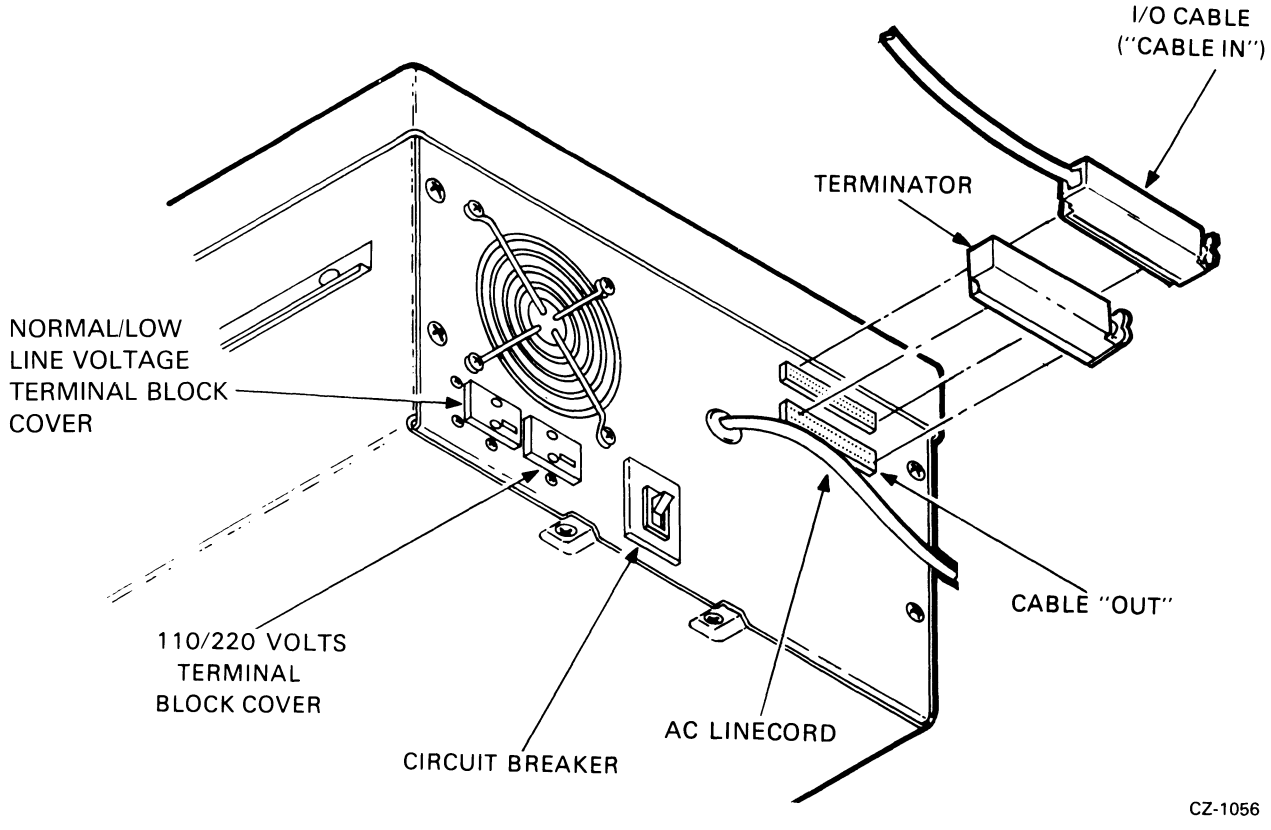


Figure 3-2 RL01/02 Disk Drive – Rear View

3.2.1 Power ON/OFF Circuit Breaker

When the power plug is inserted into the proper ac outlet, ac power is applied to the rear panel circuit breaker on the drive. When the circuit breaker is switched ON, ac power is applied to the drive and the blower motor is energized.

3.2.2 Run/Stop Switch with LOAD Indicator

This push on/push off switch, when pressed in, energizes the spindle motor providing the following conditions have been met.

- The RL01K/RL02K cartridge has been installed.
- The cartridge protective cover is in place and the cartridge access door is closed.
- All ac and dc voltages are within specifications.
- The read/write heads are home (retracted).
- The brushes are home (newer drives have no brush assembly).

When this switch is released, the spindle drive motor is deenergized if the read/write heads are not loaded. If the heads are loaded, they are immediately retracted and the spindle drive motor is then deenergized. In the event of a main power interrupt and subsequent power restoration, the drive will cycle up if the switch is ON since it contains mechanical memory.

The LOAD indicator is illuminated whenever:

- The spindle is stopped,
- The read/write heads are home,
- The brushes are home (on drives so equipped),
- The spindle drive motor is not energized.

3.2.3 UNIT SELECT Switch with READY Indicator

The UNIT SELECT switch is a cam-operated switch that is actuated by inserting a numbered, cammed button. The switch contacts are binary encoded so the drive interface logic recognizes the UNIT SELECT number (0, 1, 2 or 3).

The UNIT SELECT indicator, when lit, indicates a drive READY condition. This condition exists when:

- The read/write heads are loaded,
- The heads are detented on a specific track.

3.2.4 FAULT Indicator

The FAULT indicator is lit whenever the following fault or error conditions develop in the disk drive:

- Drive-select error,
- Seek time-out error,
- Write current in heads (during sector time) error,
- Loss of system clock (this condition is not latched and not represented in status word),
- Write-protect error,
- Write data error,
- Spin error.

NOTE
Volume Check does not light the FAULT indicator but does cause DRIVE ERROR.

3.2.5 WRITE PROTECT Switch and Indicator

This push on/push off switch is used either to set the WRITE PROTECT condition if it has been reset or to reset the WRITE PROTECT condition if it has been set. The switch unit contains a light that is on when the WRITE PROTECT condition is set.

3.3 OPERATING PROCEDURES

This paragraph explains how to load a cartridge into a disk drive and how to cycle up the drive to put the subsystem on-line. The cycle-up procedure assumes that ac power is available, the drive ac circuit breaker is on (cooling fan is energized), system power is on, and the LOAD indicator on the drive control panel is on.

3.3.1 Cartridge Loading and Drive Startup Procedure

1. Raise the drive access cover.

2. Prepare a cartridge (Figure 3-3) for loading as follows.

   a. Lift the cartridge by grasping the top cover handle with the right hand.

   b. Support the cartridge with the left hand holding the protection cover.

   c. Lower the top cover handle and push the handle slide to the left with the thumb of the right hand. Again, raise the handle to its full upright position to release the protection cover.

   d. Lift the cartridge from the protection cover and carefully seat the cartridge on the spindle with the top cover handle recess facing the rear of the machine.

   e. Carefully rotate the top cover handle back and forth to ensure that the spindle locating arms are seated properly within the cartridge housing detent slots.

CAUTION

Use care when seating the cartridge on the drive spindle. Rough handling of the cartridge may cause damage to the spindle/cartridge interface which, in turn, can cause excessive cartridge runout and positioning errors.

   f. Gently lower the top cover handle to a horizontal position to engage the cartridge on the drive spindle.

   g. Place the protection cover on top of the cartridge.

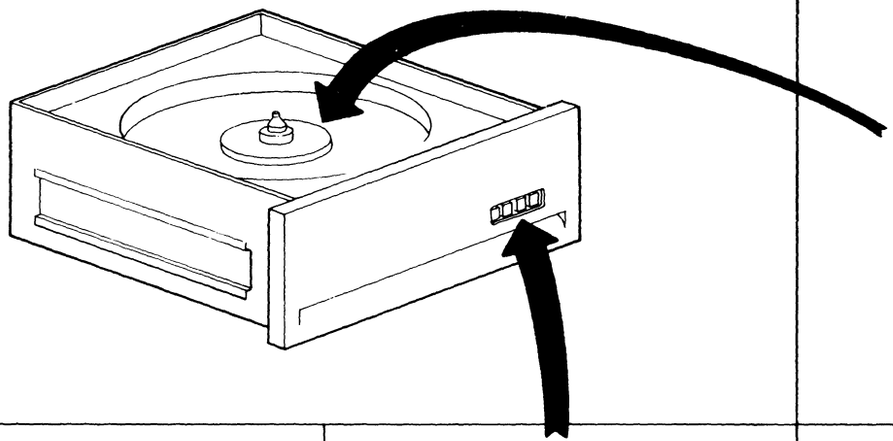
   h. Close the drive access cover.

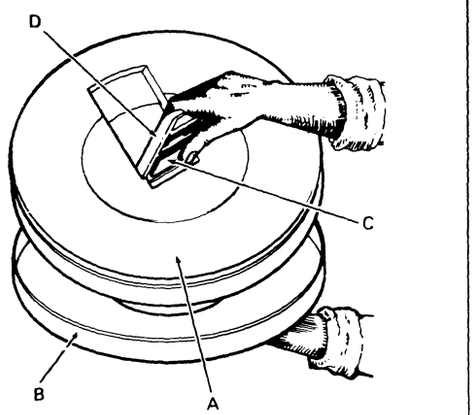
3. Start the drive as follows.

   a. Press the run/stop switch (LOAD indicator).

   b. When the drive has completed the drive startup sequence and the read/write heads are detented on cylinder 0, the READY indicator on the numbered UNIT SELECT switch will be illuminated.

   c. If write protection is desired, press the WRITE PROTect switch.





TO READY DRIVE:

- RAISE CARTRIDGE ACCESS DOOR
- LOAD CARTRIDGE
- DEPRESS RUN/STOP SWITCH (LOAD INDICATOR)
- NOTE THAT SPINDLE MOTOR STARTS TURNING
- AFTER 30 SECONDS, UNIT SELECT INDICATOR SHOULD LIGHT INDICATING DRIVE IS READY TO READ OR WRITE
- IF WRITE PROTECTION IS DESIRED, DEPRESS WRITE PROTECT SWITCH (PROTECT INDICATOR)

DRIVE INDICATORS:

LOAD:
LIGHTS TO INDICATE THAT CARTRIDGE MAY BE LOADED OR THAT SPINDLE IS STOPPED.

UNIT SELECT:
INDICATES LOGICAL DRIVE ADDRESS. WHEN LIT, INDICATES DRIVE IS READY TO READ, WRITE OR RECEIVE CONTROLLER COMMANDS.

FAULT:
WHEN LIT, INDICATES A DRIVE ERROR CONDITION. IF THIS CONDITION PERSISTS, SEEK ASSISTANCE.

WRITE PROTECT:
WHEN LIT, INDICATES THAT CARTRIDGE CURRENTLY MOUNTED IS WRITE PROTECTED.

TO LOAD CARTRIDGE:

- SUPPORT CARTRIDGE "A" WITH LEFT HAND HOLDING PROTECTION COVER "B".
- PUSH HANDLE SLIDE "C" TO LEFT WITH THUMB OF RIGHT HAND.
- RAISE COVER HANDLE "D" TO FULL UPRIGHT POSITION, RELEASING PROTECTION COVER "B".
- LIFT CARTRIDGE "A" FROM PROTECTION COVER "B" AND CAREFULLY SEAT IT ON DRIVE SPINDLE WITH HANDLE RECESS FACING REAR OF DRIVE.
- CAREFULLY ROTATE TOP COVER HANDLE "D" A FEW DEGREES CLOCKWISE AND COUNTER-CLOCKWISE TO ENSURE FIRM SEATING.
- GENTLY LOWER TOP COVER HANDLE "D" TO HORIZONTAL POSITION TO ENGAGE CARTRIDGE ON DRIVE SPINDLE.
- PLACE PROTECTION COVER "B" ON TOP OF CARTRIDGE.

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Figure 3-3 Cartridge Loading Procedure

3.3.2 Cartridge Unloading Procedure

1. Power down the drive as follows.

   a. Press the run/stop switch and wait approximately 30 seconds for the LOAD indicator to illuminate.

   b. Raise the drive access cover.

2. Remove the cartridge as follows.

   a. Remove the cartridge protection cover and hold the cover in the left hand.

   b. Push the top cover handle slide to the left with the thumb before raising the handle.

   c. Raise the top cover handle to a full upright position to release the cartridge from the drive spindle.

   d. Carefully lift the cartridge up and out of the drive and place it in the protection cover.

   e. Lower the top cover handle to the horizontal position to lock the protection cover in place.

3.4 OPERATOR MAINTENANCE

3.4.1 Introduction

User maintenance procedures are limited to the care and cleaning (external) of the disk cartridge and the cleaning of the drive spindle assemblies.

3.4.2 Professional Cartridge Cleaning

Cartridges should be professionally cleaned every six months or whenever practical. Complete cartridge cleaning procedures must be performed by a professional cleaning service. Application of cleaning procedures to the recording surfaces by unqualified personnel may void not only the warranty on the serviced cartridge, but the warranty for any drive on which the cartridge is operated.

3.4.3 User Cartridge Cleaning

The user should clean the outer sides of a completely assembled cartridge by using a lint-free wiper dampened with a solution of 9 percent water and 91 percent isopropyl alcohol. However, the cartridge must not be saturated and all excess solvent must be removed with a dry wiper. This procedure is necessary to prevent solvent from entering the seams of the assembly and contaminating the platter.

CAUTION

For cleaning purposes, use only a solution of 9 percent water with 91 percent isopropyl alcohol. Water, trichloroethylene, or other solvents are not permitted.

3.4.4 Spindle Assembly Cleaning

Using a lint-free wiper dampened with the isopropyl alcohol solution, clean the spindle cone prior to loading the cartridge. However, do not saturate the assembly; remove all excess solvent with a dry wiper. This procedure is necessary to prevent solvent from entering a loaded cartridge and contaminating the platter. In addition, ensure that the shroud is as free of lint and dust as possible before loading a cartridge. Dry lint and dust may be blown from the spindle area using filtered dry air. However, do not use manufacturing environment air that may contain water or oil; canned air is an acceptable substitute.

3.5 CARTRIDGE CARE SUMMARY

The following list summarizes care and cleaning considerations for an RL01K/RL02K disk cartridge.

- Keep cartridges clean.
- Use cartridges at computer room temperature only.
- Manipulate cartridges by the top cover handle only.
- When the protection cover is removed (for loading), do not touch disk surfaces, hub center cone, or surfaces.
- When the protection cover is removed (for loading), interior metal hub surfaces must be clean.
- When the protection cover is removed (for loading), ensure that the disks are not moved or rotated, since improper disk motion may generate plastic particles which can result in disk damage.
- When loading or unloading a drive, insert and remove cartridges gently. In addition, do not use excessive force when manipulating the top cover handle.
- If, during operation, a cartridge makes rumbling or continuous tinging sounds, discontinue use of the cartridge. Use of a damaged cartridge on other drives may damage the drives, resulting in additional damage to all other cartridges used in those drives.
- Each cartridge should be cleaned professionally every six months and/or whenever a specific cartridge is not operating properly.
- Cartridges are factory-repairable only. Disassembly in the field is not permitted, and such action may void the warranty on a cartridge, as well as any drive on which the cartridge may be operated.

CHAPTER 4
11-FAMILY PROGRAMMING INFORMATION

4.1 GENERAL DESCRIPTION

This chapter describes the RL11, RLV11, and RLV12 controllers and points out the differences among them.

4.1.1 RL11 Controller Description

The RL11 controller consists of a single hex-height M7762 module. It can be installed in any hex-height small peripheral controller (SPC) slot. This controller provides a programmable interface between the PDP-11 UNIBUS and the RL01/RL02 disk drive(s). The controller has four addressable registers that are detailed in Paragraph 4.2. The controller can respond to one of seven commands from the software. These controller commands are explained in detail in Paragraph 4.3.

The RL11 buffers the data flow between drive and memory with a 16- x 16-bit IC buffer. This buffer has the designation of SILO as it is a first-in, first-out device.

4.1.2 RLV11 Controller Description

The RLV11 controller consists of 2 quad-height modules designated M8013 and M8014. This controller provides a programmable interface between the LSI-11 Q-Bus and the drive(s). Like the RL11, the RLV11 has four addressable registers that are explained in detail in Paragraph 4.2. The RLV11 can respond to one of eight commands from the software. These commands are explained in Paragraph 4.3.

The RLV11 buffers the data flow between drive and memory with a 256- x 16-bit RAM. This RAM has the designation of FIFO (first-in, first-out).

4.1.3 RLV12 Controller Description

The RLV12 controller consists of one quad-height module designated M8061. This is a fine-line etch, multi-layered module with an extremely high IC chip density. The controller may be used on the standard LSI-11 Q-Bus or the Q-22 Bus. The use of 22-bit addressing (Q-22 Bus) is selected via a jumper. This controller functionally replaces the RLV11 as the programmable interface between the drive(s) and the LSI-11 Q-Bus. The program accessible registers are explained in detail in Paragraph 4.2. Like the RLV11, the RLV12 has a maintenance command that the RL11 does not have. All eight commands are described in Paragraph 4.3. The RLV12 also has a 256- x 16-bit RAM used as a FIFO buffer.

4.2 ADDRESSABLE REGISTERS

There are four addressable registers in the RL11 and RLV11 controllers that are used to control and monitor the operation within the controller itself and within the disk drive unit(s). These are described briefly in Table 4-1 and described in detail in the following text. The RLV12 controller contains these four plus an additional register to hold the balance of the 22-bit memory address.

Table 4-1 Controller Addressable Registers

Address (Octal)	Description
774400	**Control Status (CS)** – Indicates drive ready condition; decodes drive commands and provides overall control functions and error indications.
774402	**Bus Address (BA)** – Contains the memory location involved in a data transfer during a normal read or write operation.
774404	**Disk Address (DA)** – Stores information for: (1) seeking to desired track; or (2) selecting sectors to be transferred during read/write operations; or (3) used when requesting a drive status message.
774406	**Multipurpose (MP)** – (1) Functions as word counter when transferring read/write data between UNIBUS and drives; or (2) acts as storage buffer when reading drive status; or (3) stores header information from controller silo when executing a read header command.
17774410	**Bus Address Extension (BAE)** – Contains the upper six bits of 22-bit memory addressing. This register is used only with the RLV12 controller and then only when 22-bit addressing mode is enabled.

4.2.1 Control Status Register

The Control Status (CS) register (Figure 4-1) is a 16-bit register with a base address of 774400. Bits 1 through 9 can be read or written; the other bits can only be read. Table 4-2 describes the bit format of the Control Status register.

When the controller is initialized, bits 1-6 and 8-13 are cleared and bit 7 is set. Bit 0 is set whenever the selected drive is in the ready condition; otherwise, the bit is cleared. Bit 14 is set whenever there is a drive error; it is cleared when the drive error is corrected or the drive error is cleared by a Get Status command. Bit 15 is set when there is a drive or controller error (indicated in bits 10-14).

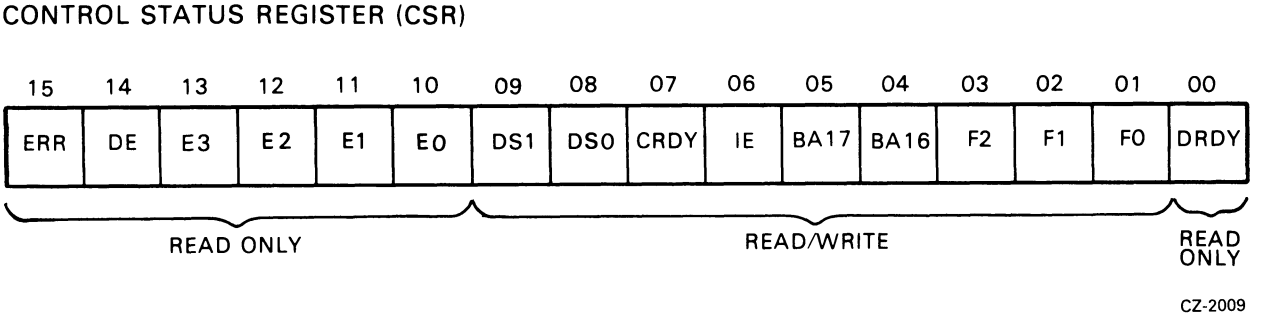


Figure 4-1 CS Register

Table 4-2 Control Status Register Bit Description

Bit(s)	Description
0	**Drive Ready (DRDY)** – When set, this bit indicates that the selected drive is ready to receive a command. The bit is cleared when a seek or head select operation is initiated and set when the operation is completed.
1-3	**Function Code** – These bits are set by software to indicate the command to be executed.

Command	F2-F0
No Op (RL11) or Maintenance Mode (RLV11/RLV12)	000
Write Check	001
Get Status	010
Seek	011
Read Header	100
Write Data	101
Read Data	110
Read Data without Header Check	111

4-5	**Bus Address Extension Bits (BA16, BA17)** – These are the two most significant bus address bits when operating in 18-bit addressing modes. They are read and written as data bits 4 and 5 of the cs register but considered as address bits 16 and 17 of the bus address register (see Paragraph 4.2.2).
6	**Interrupt Enable (IE)** – When this bit is set by software, the controller is allowed to interrupt the processor at the normal command or error termination.
7	**Controller Ready (CRDY)** – When cleared by software, this bit indicates that the command code in bits 1-3 is to be executed (negative G0 bit). The hardware sets this bit to indicate the controller is ready to accept another command.

Table 4-2 Control Status Register Bit Description (Cont)

Bit(s)	Description
8-9	**Drive Select (DS0, DS1)** – These bits determine which drive will communicate with the controller via the drive bus.
10-13	**Error Code**

Error Name	E3-E0
Operation Incomplete (OPI)	0001
Read Data CRC (DCRC or Write Check Error (WCE)	0010
Header CRC (HCRC)	0011
Data Late (DLT)	0100
Header Not Found (HNF)	0101
Non-Existant Memory (NXM)	1000
Memory Parity Error (MPE) RLV12 only	1001

14	**Drive Error (DE)** – This bit is tied directly to the DE interface line. When set, it indicates that the selected drive has flagged an error. (The source of the error can be determined by executing a Get Status command and then executing an MPR read.) DE can be cleared by executing a Get Status command with bit 3 of the DA register set.
15	**Composite Error (ERR)** – When set, this bit indicates that one or more of the error bits (bits 10-14) is set. If the IE bit (bit 6 of CS) is set and an error occurs (which sets bit 7), an interrupt will be initiated.

4.2.2 Bus Address Register

The Bus Address (BA) register (Figure 4-2) is a 16-bit register with an address of 774402. Bits 1 through 15 can be read or written; bit 0 is always zero. Bus address bits 16 and 17 are contained in bits 4 and 5 of the CS register.

The BA register indicates the memory location involved in the data transfer during a normal read or write operation. The contents of the BA register are automatically incremented by two as each word is transferred between the bus and the I/O buffer. This register overflows bits BA16 and BA71 into CS register bits 4 and 5. If the controller is an RLV12 and if 22-bit addressing mode is enabled, then bits BA16 through BA21 are found in the BAE register.

The BA register is cleared by initializing the drive or by loading the register with zeros.

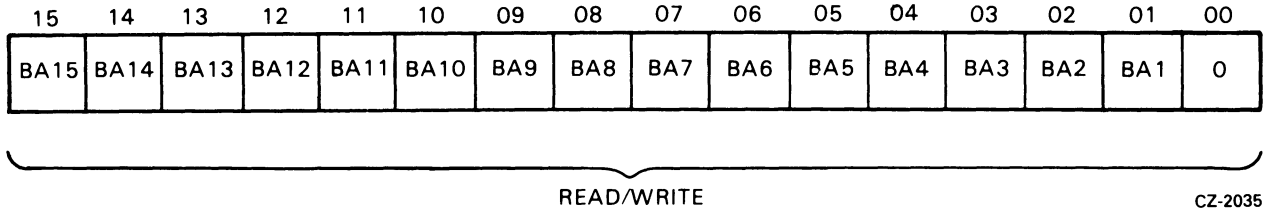


Figure 4-2 BA Register

4.2.3 Disk Address Register

The Disk Address (DA) register is a 16-bit register with an address of 774404. Its contents can have one of three meanings depending on the function being performed. This register is cleared by initializing the device or loading the register with zeros. All 16 bits can be read or written by the processor. The following three paragraphs describe the uses of the Disk Address register.

4.2.3.1 DA Register During a Seek Command – To perform a Seek function, it is necessary to provide cylinder address difference, head-select, and head-directional information to the selected drive. Figure 4-3 shows the bit layout of the Disk Address register during seek commands, while Table 4-3 describes the bit format.

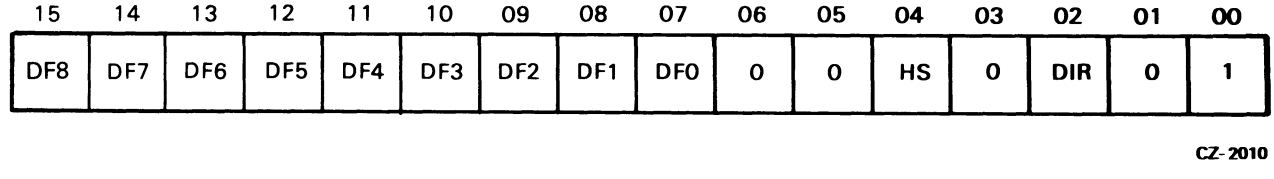


Figure 4-3 DAR Contents to Execute a Seek Command

Table 4-3 Disk Address Register Bit Description for Seek Commands

Bit(s)	Description
0	**Marker Bit** – Must be a one.
1	**Seek** – Must be a zero, indicating to the drive that a seek is being requested. With this bit cleared, the drive uses the remaining contents of the register as seek parameters.
2	**Direction (DIR)** – This bit indicates the direction in which a seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 7-15).
3	Must be a zero.
4	**Head Select (HS)** – Indicates which head (disk surface) is to be selected. A one selects the lower head; a zero, the upper head.
5-6	Reserved.
7-15	**Cylinder Address Difference DF 08:00** – Indicates the number of cylinders the heads are to move on a seek.

4.2.3.2 DA Register During Read or Write Data Command – For a read or write operation, the DA register is loaded with the address of the first sector to be transferred. As each successive sector is transferred, the DA register is automatically incremented. The contents of this register are used by the header comparison logic to locate the desired sector. The header read from the disk is compared against the contents of this register. Figure 4-4 shows the bit format of the Disk Address register during data transfer commands, while Table 4-4 describes the bit format.

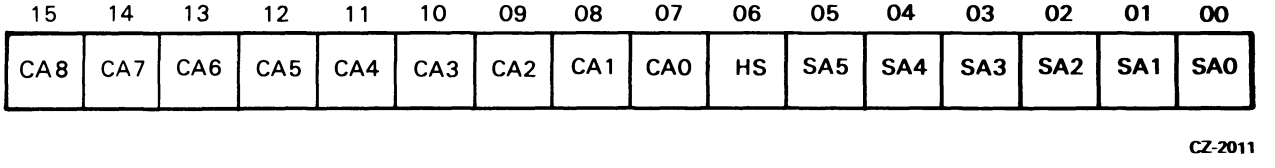


Figure 4-4 DAR Contents During a Read/Write Data Command

Table 4-4 Disk Address Register Bit Description for Data Transfer Commands

Bit(s)	Description
0-5	**Sector Address SA 05:00** – Desired address of one of the 40 sectors on a track as supplied by the software (range is 0 through 47, octal).
6	**Head Select (HS)** – Desired head address of one of the two drive heads. A one indicates the lower head; a zero, the upper head.
7-15	**Cylinder Address CA 08:00** – Desired address of one of the cylinders on the disk (range is 0 through 777, octal). The RL01 has 256 cylinders and the RLV12 has 512 cylinders.

4.2.3.3 DA Register During a Get Status Command – For a Get Status command, the DA register bits must be programmed as shown by Figure 4-5 and described in Table 4-5.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	0	0	0	0	RST	0	1	1

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Figure 4-5 DAR Contents to Execute a Get Status Command

Table 4-5 Disk Address Register Bit Description for Get Status Commands

Bit(s)	Description
0	**Marker Bit** – Must be a one.
1	**Get Status (GS)** – Must be a one, indicating to the drive that the status word is being requested. At the completion of the Get Status command, the drive status word is read into the controller Multipurpose (MP) register. With this bit set, the drive ignores bits 8-15.
2	Must be a zero.
3	**Reset (RST)** – When this bit is set, the drive clears its error register (resets all drive faults) before sending the status word to the controller.

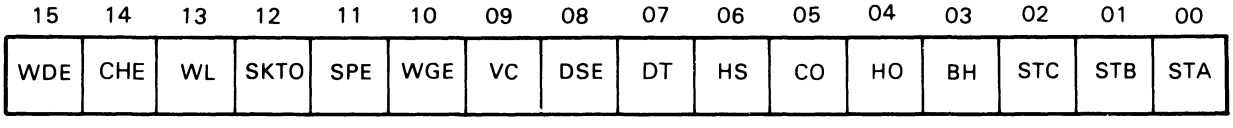
Table 4-5 Disk Address Register Bit Description for Get Status Commands (Cont)

Bit(s)	Description
4-7	Must be a zero.
8-15	Not used during a Get Status.

4.2.4 Multipurpose Register

The Multipurpose (MP) register is a 16-bit register with an address of 774406. This register can have one of three meanings, depending on the function being performed. The following three paragraphs describe the uses of the Multipurpose register.

4.2.4.1 MP Register After a Get Status Command – When a Get Status command is executed, the status word is returned to the controller and transferred to the MP register. Figure 4-6 shows the bit layout, while Table 4-6 describes the bit format.



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Figure 4-6 MPR – Following a Get Status Command

Table 4-6 MP Register Bit Description for Get Status Commands

Bit(s)	Description
0-2	**Major State Code (ST C:A)** – These bits define the state of the drive.

STC	STB	STA	
0	0	0	Load cartridge
0	0	1	Spin-up
0	1	0	Brush cycle
0	1	1	Load heads
1	0	0	Seek
1	0	1	Lock on
1	1	0	Unload heads
1	1	1	Spin-down

Table 4-6 MP Register Bit Description for Get Status Commands (Cont)

Bit(s)	Description
3	**Brush Home (BH)** – Set when the brushes are home.
4	**Heads Out (HO)** – Set when the heads are over the disk.
5	**Cover Open (CO)** – Set when the drive access cover is open or the dust cover is not in place.
6	**Head Select (HS)** – Indicates the currently selected head. A zero indicates the upper head; a one, the lower head.
7	**Drive Type (DT)** – A zero indicates an RL01; a one, an RL02.
8	**Drive-Select Error (DSE)** – Set when a multiple drive selection is detected.
9	**Volume Check (VC)** – Set during transition from a head load state to a head-on-track state. Cleared by execution of a Get Status command with Bit 3 asserted.
10	**Write Gate Error (WGE)** – Sets when Write Gate is asserted and one or more of the following conditions exist. • Drive is not "ready to read/write" • Drive is write-protected • Sector pulse is occurring • Drive has another error
11	**Spin Error (SPE)** – Set when spindle has not reached speed in the required time during spin-up or when spindle speed is too high.
12	**Seek Time Out (SKTO)** – Set when the heads do not come on-track in the required time during a Seek command or when "ready to read/write" is lost while the drive is in position (lock-on) mode.
13	**Write Lock (WL)** – Set when the drive is write protected.
14	**Current Head Error (CHE)** – Set if write current is detected in the heads when Write Gate is not asserted (reading).
15	**Write Data Error (WDE)** – Set if Write Gate is asserted but no transitions are being detected on the Write Data line.

4.2.4.2 MP Register After a Read Header Command – When a Read Header command is executed, the next header is read and its three words are transferred to the MP register. The first word contains sector address, head-select, and cylinder address information. The second word contains zeros. The third word contains header CRC information. All three words can be read sequentially by the program by reading the contents of the MPR. Figure 4-7 shows the bit layout of the MP register for Read Header commands, while Table 4-7 describes the bit format.

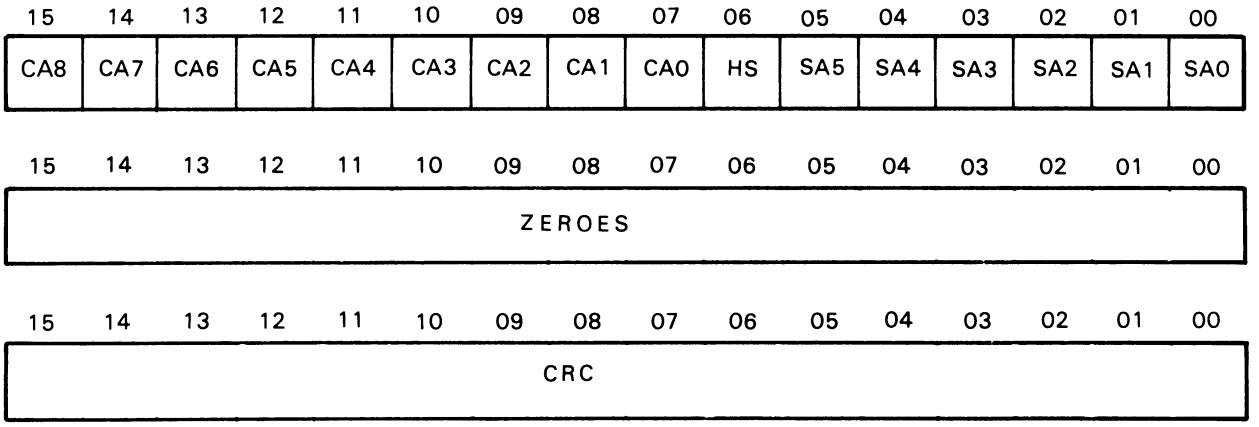


Figure 4-7 MPR – Following a Read Header Command

Table 4-7 MP Register Bit Description for Read Header Commands

Bit(s)	Description
0-5	**SA 0:5** – Sector Address
6	**HS** – Head Select
7-15	**CA 0:8** – Cylinder Address

4.2.4.3 MP Register During Read/Write Data Commands – Before the reading or writing data, the program loads the word count into the MP register in two's complement form. The counter is incremented as each word is transferred. Usually, the reading or writing operation is terminated when the word counter reaches zero (overflows). The word counter can keep track of from one to the full 40-sector count of 5120 data words (decimal). Figure 4-8 shows the bit format of the MP register for data transfer commands, while Table 4-8 describes the bit format.

NOTE

The RL01/RL02 disk drive will not do spiral read/writes. If data is to be transferred past the end of the last sector of a track, it is necessary to break up the operation into the following steps.

1. **Program the data transfer to terminate at the end of the last sector of the track.**
2. **Program a seek to the next track. This can be either a head switch to the other surface but same cylinder or a head switch and move to the next cylinder.**
3. **Program the data transfer to continue at the start of the first sector at the next track.**

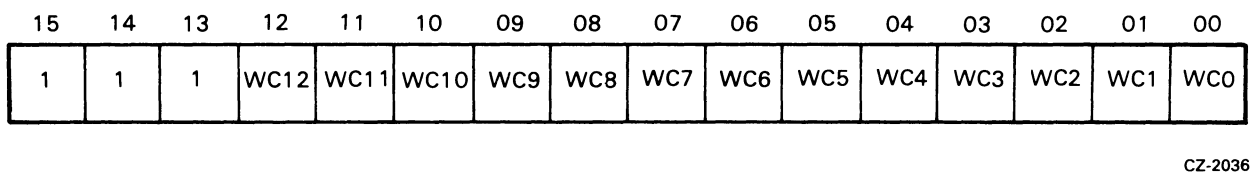


Figure 4-8 MPR – Used as a Word Counter

Table 4-8 MP Register Bit Description for Data Transfer Commands

Bit(s)	Description
0-12	**Word Count WC 12:00** – Contains the two's complement of total number of words to be transferred.
13-15	Must be ones.

4.2.4.4 Bus Address Extension Register – The Bus Address Extension (BAE) register (Figure 4-9) is a six-bit register with an address of 17774410. It is used only with the RLV12 controller, and then only when the 22-bit addressing mode is enabled. Bits 0 through 5 can be read or written. Bits 0 and 1 contain the same information found in the CSR bits 4 and 5.

NOTE

If 22-bit addressing is to be used, the software must correctly load the CSR bits 4 and 5 with the contents of BA17 and 16. Upon command initiation, these two bits are loaded into BAE bits 0 and 1. Figure 4-9 shows the bit format of the Bus Address Extension register.

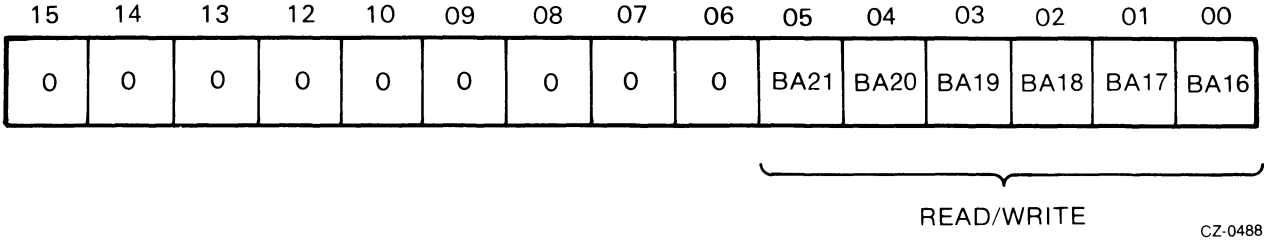


Figure 4-9 BAE Register

4.2.5 Register Summary

Figure 4-10 is a bit and function summary of the CS, BA, BAE, DA, and MP registers.

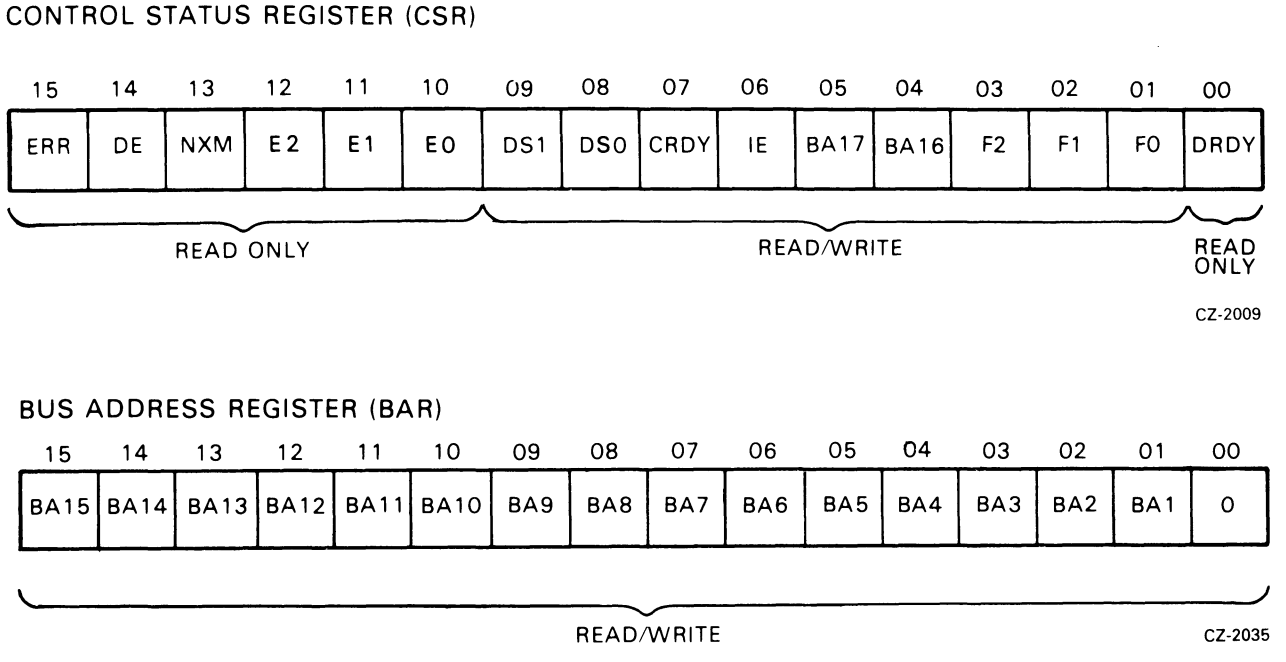
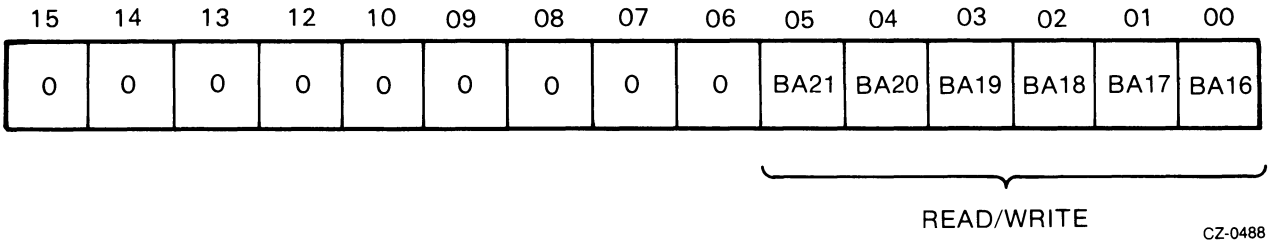
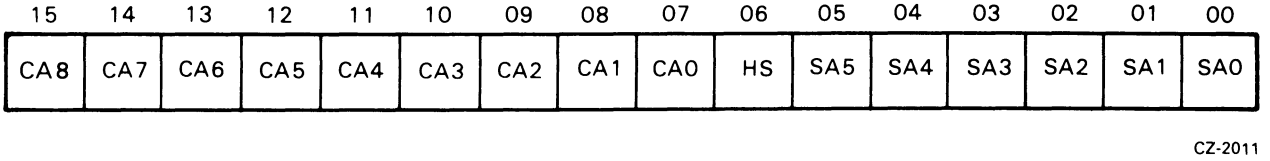


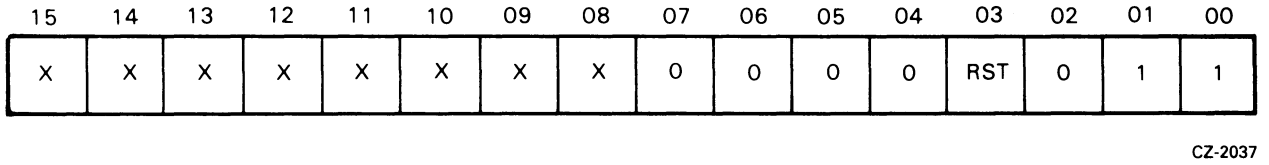
Figure 4-10 Register Summary (Sheet 1 of 3)



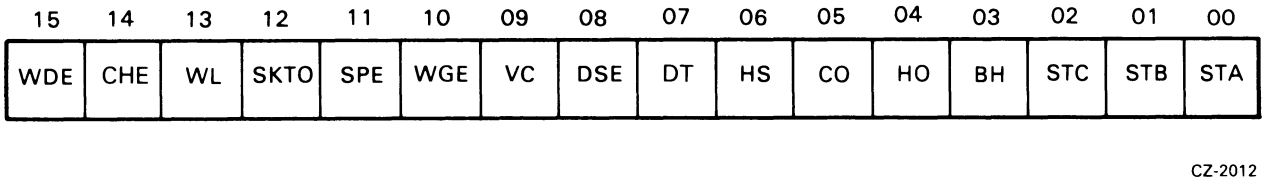
DAR DURING READING OR WRITING DATA COMMANDS



DAR DURING GET STATUS COMMAND



MPR AFTER GET STATUS COMMAND



MPR AFTER READ HEADER COMMAND

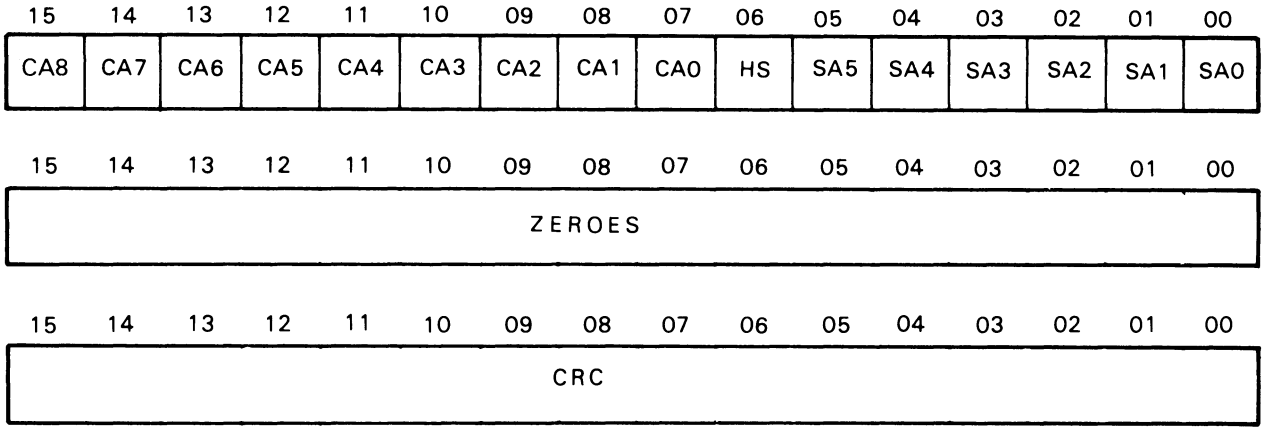


Figure 4-10 Register Summary (Sheet 2 of 3)

MPR DURING READ/WRITE COMMANDS FOR WORD COUNT

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	WC12	WC11	WC10	WC9	WC8	WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0

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Figure 4-10 Register Summary (Sheet 3 of 3)

4.3 CONTROLLER COMMANDS

The RL11 controller responds to one of seven commands from the software, while the RLV11/RLV12 can respond to one of eight commands. Table 4-9 lists the commands. Each command is explained in the following paragraphs.

Table 4-9 RL11/RLV11/RLV12 Controller Commands

Function Code	Command
0	No Op (RL11) or Maint. (RLV11/RLV12)
1	Write Check
2	Get Status
3	Seek
4	Read Header
5	Write Data
6	Read Data
7	Read Data Without Header Check

4.3.1 No-Op (RL11) or Maintenance (RLV11) – Function Code 0

The RL11 performs no operation aside from clearing errors (all except DE), setting CRDY and interrupting if IE is set.

The RLV11/RLV12 maintenance command is used during a diskless diagnostic routine to detect controller malfunctions or to establish a level of confidence in controller operation. Prior to issuing the maintenance command, a buffer area in memory must be set aside for writing and reading of test patterns. The controller registers must be loaded by program with the following information.

- BAR with address of first memory buffer location
- WC register with a count of 511 (177001 octal)
- DAR with test word
- CSR with a function code 0, reset bit 7

When the maintenance command is issued (MAINT) and the CRDY bit is cleared, the OPI timer starts. The microsequencer decodes the command and starts a maintenance routine. Two internal tests are performed and the DAR is incremented after each. DMA transfers take place between memory and the controller FIFO, transferring 256 words from the memory write test buffer into the FIFO. Once the FIFO is full, 255 words are transferred into the memory read test buffer previously prepared. The DAR is now incremented a third time. Throughout MAINT, error checks are made; if an error occurs, the function sets ERR. The DAR is incremented as the test proceeds. This incrementing serves as a trace to determine the failing internal test.

Next, the test word +3 that was initially loaded into the DAR is channeled through the data multiplexer and into the CRC circuit. A CRC word is generated from this test word and sent through the data multiplexer again. This CRC of the test word then passes through the write precompensation circuit and the data separator circuit to eventually end up in the FIFO.

The contents of the DAR are then incremented and become test word +4. This new test word follows the same path as the preceding test word and ends up as the second word in the FIFO. At this point, the FIFO holds:

WORD	FIFO
1st	CRC of test word +3
2nd	CRC of test word +4

The contents of the DAR are now incremented once again and become test word +5.

Next, the second word in the FIFO (CRC of test word +4) is removed from the FIFO and serialized. It is sent through the data multiplexer the CRC, and data multiplexer again, and so on. It follows the same data path as the two previous words and ends up back in the FIFO as the new second FIFO word. At this point, the FIFO holds the following.

WORD	FIFO
1st	CRC of test word +3
2nd	CRC of CRC of test word +4

The contents of the DAR is then incremented for the sixth time to become test word +6. The controller ready bit is then set and the CPU receives an interrupt request. This completes the maintenance command operation.

As a result of this maintenance test, the following circuits are tested: the FIFO, the registers, the data multiplexer, the CRC circuit, the match circuit, the write precompensation circuit, the data separator circuit and the FIFO input and output serializer. Also, many of the microsequencer functions are exercised.

4.3.2 Write Check – Function Code 1

The write check command is used to verify that data was written on the disk correctly. It is used after writing a block of data onto the disk by the write command function. The write check command reads this same block of data from the disk and compares it with the contents of its source data buffer area in main memory. Because this comparison is performed in the controller, this source data must be transferred out of memory and into the controller buffer.

Prior to issuing this command, the BA register must be loaded with the address of the first location of the data block in the main memory. The word counter register must be loaded with the data block length. The DA register is then loaded with the starting disk address location. At this point, the write check command can be loaded into the CS register.

Once the header is found, and the header CRC validates the match, 128 words of data are read from the disk. The disk data is then compared serially with the serial data coming out of the silo (SER DATA OUT). Either a compare error or a data CRC error will set bit 11 in the CS register.

4.3.3 Get Status – Function Code 2

The Get Status command causes the status word from a drive to be transferred to the controller where the software can access it through the MPR. The software should first verify that the controller is ready to perform an operation (the drive does not have to be ready). Then, the software should load the DAR with ones in bits 01 and 00, and zeros in the other locations. Next, the software should load the CSR with drive-select bits, a negative GO bit, IE bit (if desired) and a code of 2 in the function bits. The controller will then command the selected drive to transfer its status word to the MPR in the controller. If the "reset" bit (03) in the DAR is also set, the drive resets its status register before transferring it to the controller. This is the manner in which Volume Check is cleared or to check for hard errors.

4.3.4 Seek – Function Code 3

The Seek operation causes the positioner to move (either forward or reverse) some number of cylinders. The software should first verify that the drive is ready to accept a command, then load the DAR with the difference word (difference between the present position and desired position). This word contains the number of cylinders to move (bits 15 through 07), the head-select bit (04) and the direction bit (bit 02, 1=forward, 0=reverse). Bits 06, 05 and 01 must be reset and bit 00 must be set. After the DAR is loaded, the software should load the CSR with the command word. This word should contain the drive-select bits, the negative GO bit, the IE bit (if desired), and a code of 3 in the function bits. The controller sends the Seek command to the selected drive, causing the drive to start its Seek operation. At this time, the controller becomes ready and interrupts if IE is set. The controller is now ready to accept another command to perform another operation on another drive while the Seek is occurring.

If the difference word is large enough that the heads attempt to move past the innermost or outermost limits, the head will stop at the guard band and retreat to the first even-numbered data track.

4.3.5 Read Header – Function Code 4

When a Read Header function is decoded, the controller will read the first header encountered on the selected drive and place the three header words in the buffer. They pass through the buffer and stop with the first word in the MP register. The software can then access the first word to determine the current sector, head, and cylinder address. When the software extracts the first word from the MP register, the second word automatically moves into the MP register. If the software extracts the second word, the third word automatically moves into the MP. This is the CRC word. The software can now access it for checking purposes.

4.3.6 Write Data – Function Code 5

When this function is decoded with CRDY cleared, the controller reads successive header words and compares them to the DA register. When a match is found, the header CRC is checked and, if correct, that sector is written with the words from memory designated by the BA and/or BAE register(s). The BA and MP registers are incremented for each word that is transferred. For partial sector writes, the remaining sector area is filled with zeros. At the end of the sector, the sector portion of the DA register is incremented. The next sector is written if all the words have not been written. At the end of the transfer, CRDY is set and an interrupt made if IE is set.

4.3.7 Read Data – Function Code 6

When this function is decoded, the controller reads successive header words and compares them to the contents of the DA register. When a match is found, the header CRC is checked and, if correct, that sector is read and the words are placed in the memory location designated by the BA and/or BAE register(s). Both the BA and MP registers are incremented for each word that is transferred. This operation continues until the contents of the MP register are all zeros. Data CRC is checked and the DA register is incremented at the end of each sector. If the word count has not overflowed, the next sector is read. Otherwise, CRDY is set and an interrupt is made if IE is set.

4.3.8 Read Data Without Header Check – Function Code 7

When this function is decoded, the data portion of the sector following the next sector pulse is read and the words requested are placed in the memory locations designated by the BA register. The BA and MP registers (word count in two's complement form) are incremented for each word transferred. The header is neither compared nor checked for CRC errors. Data CRC is checked at the end of a sector. If the word count has not overflowed, the next sector is read. Otherwise, CRDY is set and an interrupt is made if IE is set.

NOTE

The DA register is not incremented during multi-sector transfer.

4.4 CSR ERROR CODE DEFINITIONS

4.4.1 Operation Incomplete (OPI)

This error is flagged by the setting of bit 10 of the CSR. When bit 10 is set and 11 through 13 are clear, the indication is that the current command being executed did not complete within the OPI timer period. For an RL11, this timer period is 200 ms. For the RLV11 controller, the period is 490 ms. The RLV12 controller timer is set for 550 ms.

4.4.2 Data CRC (DCRC) or Write Check (WCE)

This error is flagged by the setting of bit 11 of the CSR. When bit 11 is set and bit 10 is clear, the indication is either that a CRC error has occurred when reading data or that a write check error has occurred. If the function currently being executed is a write check command, then the probabilities are that the error is a WCE. If the function being executed is a read data command, then the error is a DCRC. A write data command cannot flag either of these errors.

4.4.3 Header CRC (HCRC)

This error is flagged by the setting of bit 11 of the CSR. When bit 11 is set and bit 10 is also set, the indication is that a CRC error has occurred when reading a header. This error can set during write data or read data commands.

4.4.4 Data Late (DLT)

This error is flagged by the setting of bit 12 of the CSR. When bit 12 is set and bit 10 is clear, the indication depends upon the command being executed.

- Write Data Command – The silo or FIFO buffer in the controller emptied before the word counter overflowed. This means that the command is not finished but the buffer contains no more words to write. When this happens the DMA cycles are too slow.

- Read Data Command – The silo or FIFO buffer in the controller is full and there are more words to read from the disk. When this happens, the DMA cycles are too slow causing data being read to be lost.

4.4.5 Header Not Found (HNF)
This error is flagged by the setting of bit 12 of the CSR. When bit 12 is set and bit 10 is also set, the indication is that the desired header address could not be found before the OPI timer expired.

4.4.6 Non-Existant Memory (NXM)
This error is flagged by the setting of bit 13 of the CSR. When bit 13 is set and bit 10 is clear, the indication is that the addressed memory did not respond to the DMA cycle request within 10 to 20 microseconds.

4.4.7 Memory Parity Error (MPE)
This error is flagged by the setting of bit 13 of the CSR. When bit 13 is set and bit 10 is also set, the indication is that a data parity error was detected on a DMA cycle to the controller. This error applies to RLV12 controllers only.

4.5 OPERATIONAL CONSIDERATIONS

4.5.1 Interrupt
The controller will request an interrupt if the IE bit and the CRDY bit are both set in the CS register. The IE bit is set or reset by the software and reset with the initialize condition. The CRDY bit is set by the hardware upon completion of a function or upon the setting of an error flag. It is also set by the initialize condition. It is reset by the software to cause the controller to start a function (negative GO bit). The interrupt vector address is 160. The normal priority level for the RL11 is BUS REQUEST 5. The RLV11 and RLV12 controllers use the one priority level provided by the LSI-11 processor.

4.5.2 Seek Operation
The following sequence is an example of performing a seek function.

1. Issue read header function to drive and wait for interrupt or wait for CRDY.
2. Check error flag.
3. Read the header word from the MP register.
4. Calculate difference and direction for the seek.
5. Move difference word to the DA register.
6. Issue seek function to drive and wait for seek to be completed as indicated by drive ready bit.
7. Check error flag.

A software system that optimizes positional latency (see Paragraph 1.4) would keep current cylinder and head-select information in core so that Steps 1, 2, and 3 would be unnecessary. Also, note that reading the header gives rotational position as well so that some rotational optimization is possible.

4.5.3 Overlapped Seeks
Since the controller comes ready and interrupts as soon as a seek is issued, it is possible to issue seeks to additional drives while the first is seeking. However, no interrupt occurs when the seeks are completed, so the transfer command should be issued to the drive requiring the shortest seek as soon as all seeks are issued. In this way, the drive completing its seek first will immediately perform its transfer and interrupt when finished.

4.5.4 Data Transfer

Data transfer is via DMA facility. Sixteen words of silo buffering are provided for data by the RL11. The RLV11 and RLV12 controllers provide 256 words of FIFO (RAM) buffering and will not start transferring a sector unless the FIFO has enough space to hold the entire sector.

To do a data transfer, steps of the seek operation would be followed by:

- Load BA and BAE registers with address of first memory location to be transferred,
- Load DA register with address of first disk location to be transferred,
- Load WC register with two's complement of number of words to be transferred,
- Issue read data or write data and wait for interrupt or test for ready,
- Check error flag.

Other drives could do seeks or data transfers between the issuing of seek and the issuing of the data transfers.

4.5.5 Recovery of Data with Bad Headers

Function 7, read data without header check, is provided to allow the recovery of data should headers become unreadable. If constant HNF of HCRC errors are encountered on a particular sector so that the data is not recoverable by the standard read command, proceed as follows. Perform successive read header commands until the sector preceding the bad sector is found. Then, within 300 microseconds, issue the read data without header check command. The data portion of the next sector will be read without either a header compare or a check of the header CRC. Data CRC errors will be reported.

4.5.6 Non-Interchangability of RL01K/RL02K Disk Cartridges

These two types of cartridges are not functionally interchangeable but a cartridge will physically fit into the "wrong" type of drive. If a cartridge is loaded into the wrong drive, no damage will occur to the drive, media, or data, but the software will not run normally. If such symptoms are exhibited, the operator should check for the proper cartridge type.

4.6 ERROR RECOVERY

There are several errors that can be detected and flagged in the RL01/RL02 subsystem. Some of them can be considered recoverable in the sense that if the operation is retried it is possible that the error will not recur and successful use of the subsystem can continue. Some of the errors are considered fatal because retries could damage the data, media, or equipment. The errors are listed with the recommended reaction in Table 4-10.

The nature of these errors should be considered when determining how many times to retry the operation before declaring that retrying has reached a practical limit. For instance, a DLT error could be caused by a hardware system failure but it could also be the result of bus activity due to other I/O devices exceeding the throughput capability for a short duration. In this latter case, it is likely that the operation would be successful on the first retry. The rate of occurences is a good indicator of overall system performance and an error logging routine should count that. A general increase in the rate of DLT errors could indicate hardware system failures or it could indicate that the usage of the system is approaching its throughput capacity in its present configuration.

Table 4-10 Errors

Controller Error	Bit in C.S.	Recommended Reaction
OPI	10	Retry some practical number of times.
DCRC/HCRC/WCE	11	Retry some practical number of times. Be sure to record contents of the DA register.
DLT/HNF	12	Retry. If HNF, perform a read header, and verify cylinder.
NXM	13	Retry once. Be sure to record the contents of the BA register.
DRIVE ERROR	14	Perform a Get Status and check bits listed below.
Drive Error	**Bit in Status Word**	**Recommended Reaction**
DSE	8	Retry once before notifying operator to verify UNIT SELECT plug.
WGE	10	Retry.
SPE	11	Retry.
SKTO	12	Retry. Wait for 1.5 sec after Reset.
CHE	14	Fatal. Do not retry.
WDE	15	Fatal. Do not retry.

Another example of applying practical reaction to an error is the handling of an HNF error. It should be retried once; if it recurs, then possibly the head is not positioned over the correct track. If a read header operation is performed and the address from the media is examined, the current cylinder and head can be determined to see if it is a position problem. If it is not, then possibly there is a bad spot on the media and another area should be tried. If there is a bad header, that sector address should be entered into the Bad Sector File and the software should avoid using the the original sector.

As an additional example, consider an NXM error. It indicates that a memory unit is not responding to a DMA request for data transfer to/from that memory unit. It is unlikely that the media or disk unit is failing and only slightly more likely that the controller is failing (hardware problem). It is possible that the program is trying to access a non-existant memory unit (software problem). A retry may be worthwhile for one time but more than likely it will recur. The most important piece of information needed for diagnosis is the contents of the BA register.

Each of the errors should be given the same type of practical thought when programming error recovery routines. Whenever an error occurs, the program should log it (along with the symptoms such as the contents of the registers), the status of the unit, and whether or not a retry was successful. The more complete the error log, the more quickly and accurately the cause can be diagnosed.

4.7 DIFFERENCE SUMMARY (RK05 AND RL01/RL02)

This section may be helpful to users who have formerly used DIGITAL's RK05 disk cartridge subsystem. It points out the differences between programming an RK05 subsystem and programming an RL01/RL02 subsystem.

In general, the RK05 subsystem has a lot of its functionality built into the hardware while the RL01/RL02 subsystem requires the software to provide some of the functionality. The major differences are explained below.

4.7.1 Spiral Read/Write or Mid-Transfer Seeks

A spiral read/write is a transfer of data that continues past the end of a track. The RK05 subsystem provides hardware support for this by using the hardware to detect the end-of-track condition. The hardware will then cause a mid-transfer seek to the next track and restart the read/write operation at sector 0 of the next track. Note that this seek is either a head switch from the upper surface to the lower surface of the same cylinder with no head positioner movement, or a switch from lower surface to upper surface with a positioner movement to the next cylinder. The RL01/RL02 subsystem hardware cannot handle this. If a read/write operation continues past the 40th sector, the sector counter in the DAR advances to 50 (octal), which is illegal, and the OPI error flag is set. It is necessary for the software to: 1) prevent this from occurring by calculating the remaining area left versus the amount of data left before the operation, or, 2) detect that it has occurred. The software must initiate a separate seek function as well as a continuance of the read/write function. Note that a head switch from upper to lower surface without a positioner movement to the next cylinder is considered a seek in the RL01/RL02 subsystem. After a head switch, the positioner will seek the center of the new track.

4.7.2 Implicit Seeks Versus Explicit Seeks

The RK05 subsystem can perform either implicit or explicit seeks. An explicit seek is a software-directed seek operation. An implicit seek is a seek initiated by the hardware at the beginning of a read/write operation if the desired cylinder address or head address does not coincide with the present position. The RL01/RL02 subsystem hardware does not have this capability. The software must ensure that the positioner is over the desired cylinder and that the desired head is selected before starting a read/write operation.

4.7.3 Recalibrate

The RK05 subsystem has a return-to-zero or recalibrate function which causes the positioner to move to cylinder 0. There is no similar function in the RL01/RL02 subsystem. An explicit seek to cylinder 0 must be performed. If the current cylinder address is not known then the drive is commanded to seek into the outer guard band. The guard band will be detected and the head will retreat to cylinder 0.

4.7.4 Bad Sector File

There is a bad sector file feature on each RL01/RL02 disk cartridge. Its use is explained in Paragraph 1.6. There is no standard Bad Sector File used with the RK05.

4.7.5 Reformatting

The RK05 cartridge can be reformatted in the field while the RL01K/RL02K cartridges cannot. The embedded servo information and Bad Sector File greatly reduce the need to reformat the cartridge in the field.

4.7.6 Seek Interrupt

The RK05 will provide two interrupts as the result of a seek operation. The first interrupt occurs as soon as the controller has caused the drive to start its movement, indicating that the controller is free to handle another function. The second interrupt occurs when the drive finishes the seek movement. The RL01/RL02 subsystem does not provide the second interrupt. Thus, the software must perform the proper monitoring of the drive to determine when the seek has been completed.

CHAPTER 5
RL8A PROGRAMMING INFORMATION

5.1 GENERAL DESCRIPTION

The RL8A controller consists of a single hex-height M8433 module. It interfaces the PDP-8 OMNIBUS with the RL01/RL02 disk drive bus and contains the control, monitor, and data handling logic for disk operation. The RL8A can handle up to four drives via a daisy-chained I/O cable. A PDP-8 can handle two RL8A controllers, providing control for up to eight drives.

The RL8A has six addressable registers that are detailed in Section 5.2. The PDP-8 computer communicates with the controller by accessing these registers using Input Output Transfer (IOT) instructions which have a format of 6XXX. The device codes X60X and X61X are assigned to the first controller. If there is a second controller, it uses device codes X62X and X63X. The specific instructions that cause a response in a controller are shown in Table 5-1. The instructions are used to monitor and control the controller and are not used to transfer data. Data is transferred using Direct Memory Access (DMA) operation via data break cycles on the OMNIBUS. The result is an exchange of data between the controller and memory directly, one 12-bit word at a time. The controller has a silo which can buffer up to 16 words. The controller can transfer 12-bit words to the disk as 12-bit words or can transform them into 8-bit bytes by dropping the high order four bits in each word. The controller can transfer data coming from the disk onto the OMNIBUS as 12-bit words or it can group the data as 8-bit bytes and fill in the remaining four bits as zeros. The advantages and disadvantages of both the 8-bit and 12-bit mode are covered in Paragraph 5.4.

Table 5-1 RL8A Instruction Set

OCTAL CODE *	MNEMONIC	FUNCTION
6600	RLDC	Clear controller, all registers, AC and flags. (Do not use to terminate a disk function.)
6601	RLSD	Skip on function done. Then clear if set to a one.
6602	RLMA	Load break MA register from AC 0:11
6603	RLCA	Load command register A from AC 0:11
6604	RLCB	Load command register B from AC 0:11, execute command
6605	RLSA	Load sector address register from AC 0:5
6607	RLWC	Load word count register from AC 0:11
6610	RRER	Read error register into AC 0, 1, 2, 10, 11

Table 5-1 RL8A Instruction Set (Cont)

OCTAL CODE *	MNEMONIC	FUNCTION
6611	RRWC	Read word count register into AC 0:11
6612	RRCA	Read command register A into AC 0:11
6613	RRCB	Read command register B into AC 0:11
6614	RRSA	Read sector address register into AC 0:5
6615	RRSI	Read silo word into AC 0:11
6617	RLSE	Skip on composite error, then clear if set to a one.

The RL8A controller is capable of performing eight operations. These are listed briefly in Table 5-2 and detailed in Paragraph 5.3.

Errors and error recovery are covered in Paragraph 5.5.

Table 5-2 RL8A Controller Commands

Function Code	Operation
0	Maintenance
1	Reset
2	Get Status
3	Seek
4	Read Header
5	Write Data
6	Read Data
7	Read Data Without Header Check

5.2 ADDRESSABLE REGISTERS

5.2.1 Command Register A

Command Register A is a 12-bit register used during the Seek, Read Data, and Write Data commands. The register is loaded by an RLCA (6603) command and may be read by an RRCA command (6612). Initialize from the bus will clear this register and the other addressable registers.

5.2.1.1 Command Register A During a Seek Command – To perform a Seek function, it is necessary to provide cylinder address difference, head select, and head direction information to the selected drive as indicated. Figure 5-1 shows the bit layout and Table 5-3 describes the bit format.

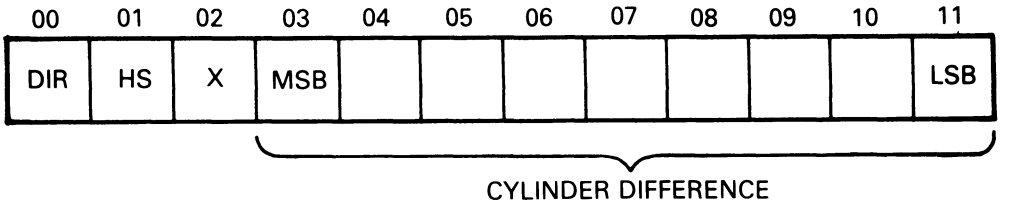


Figure 5-1 Command Register A During a Seek Command

Table 5-3 Command Register A Bit Description for Seek Commands

Bit	Name	Function
AC0	Direction (DIR)	This bit indicates the direction in which a seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 3-11).
AC1	Head Select (HS)	Indicates which head (disk surface) is to be selected. A one indicates the lower head; a zero, the upper head.
AC2	–	Spare
AC3:11	Cylinder Address Difference	Indicates the number of cylinders the heads are to move on a seek.

5.2.1.2 Command Register A During Read or Write Data Command – For a Read or Write operation, the Command Register A is loaded with part of the address of the first sector to be transferred (cylinder address and head select). This information is transferred to the disk address register along with the contents of the Sector Address register to make the complete address of the sector. Figure 5-2 shows the bit layout and Table 5-4 describes the bit format.

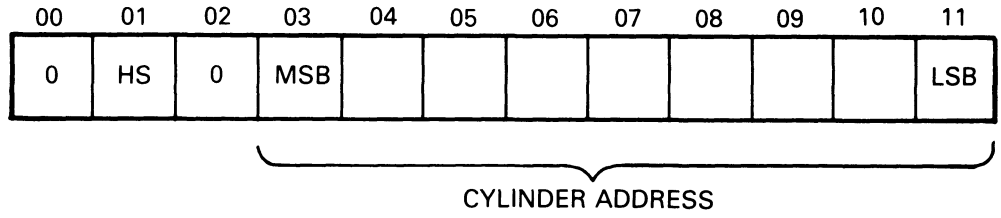


Figure 5-2 Command Register A During a Read/Write Data Command

Table 5-4 Command Register A Bit Description For Data Transfer Commands

Bit	Name	Function
AC0	–	Must be zero
AC1	Head Select (HS)	Head-select bit – a one indicates the lower head; a zero, the upper head
AC2	–	Must be zero
AC3:11	Cylinder Address	Cylinder address

5.2.2 Command Register B

Command Register B is a 12-bit register that contains the mode, drive number, extended memory address bits, interrupt enable, and the function code. The RLCB command (6604) is used to load the register and the RRCB command (6613) reads the register. The RLCB command also executes the function. Figure 5-3 shows the bit layout and Table 5-5 describes the bit format.

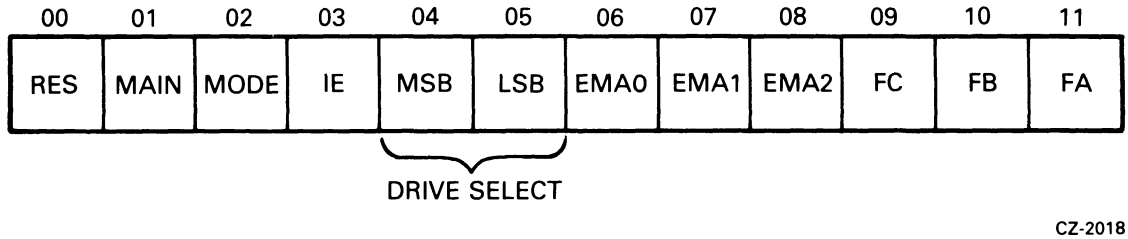


Figure 5-3 Command Register B

Table 5-5 Command Register B Bit Description

Bit	Name	Function
AC0	–	Reserved.
AC1	Maintenance	The contents of the Disk Address (DA) register are looped back to the silo for maintenance purposes. Bit 2 of command register B must also be set for this function to work correctly. See Paragraph 5.3.9.
AC2	Mode	When set, this bit indicates that the data field will be 256 8-bit bytes per sector. When zero, the data field is truncated to 170 12-bit words per sector. This bit must be set when a Maintenance, a Get Status or a Read Header command is to be executed.
AC3	Interrupt Enable (IE)	When this bit is set, the controller is allowed to interrupt the processor at the conclusion of a normal command or error termination.
AC4:5	Drive Select (DS0, DS1)	These bits determine which drive will communicate with the controller via the drive bus.
AC6:8	Extended Memory Addressed (EMA)	These three bits define the memory field location. This allows up to 32K memory locations to be addressed on processors having more than 4K of memory.
AC9:11	Function Code	These bits indicate the command to be executed by the controller/disk subsystem.

Bit 9	Bit 10	Bit 11	Command
0	0	0	Maintenance
0	0	1	Reset
0	1	0	Get Status
0	1	1	Seek
1	0	0	Read Header
1	0	1	Write Data
1	1	0	Read Data
1	1	1	Read Data Without Header Check

5.2.3 Break Memory Address Register

The Break Memory Address (BRK MA) register is a 12-bit register that points to the memory location of the data to be transferred. It is loaded by the RLMA command (6602). The contents of the BRK MA register are automatically incremented as each word is transferred between memory and controller.

The register is cleared by initializing the controller or by loading the register with zeros (Figure 5-4).

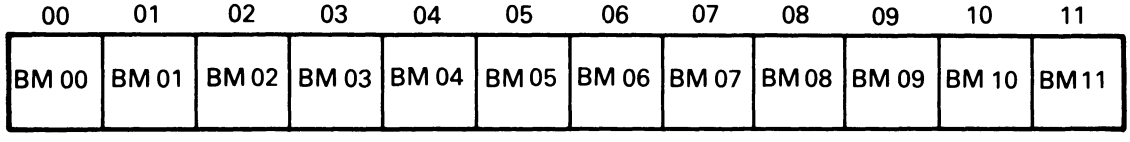


Figure 5-4 Break Memory Address Register

5.2.4 Word Count Register

The Word Count (WC) register is a 12-bit register loaded by the RLWC command (6607) and read by the RRWC command (6611). Before reading or writing data, the word counter is loaded with the two's complement of the number of words to be transferred. As each Direct Memory Address (DMA) transfer takes place, the word counter is incremented and terminates the command on overflow. It can count from 1 to 4096 data words. This corresponds to 24 sectors while operating in 12-bit word mode. In the 8-bit byte mode the transfer is limited to one sector (170 bytes) (Figure 5-5).

NOTE

The disk drive will not do spiral Read/Writes. The program must break up a data transfer if track-to-track Read/Writes are to be done. Between two such data transfers, a seek to the next track or surface must be made.

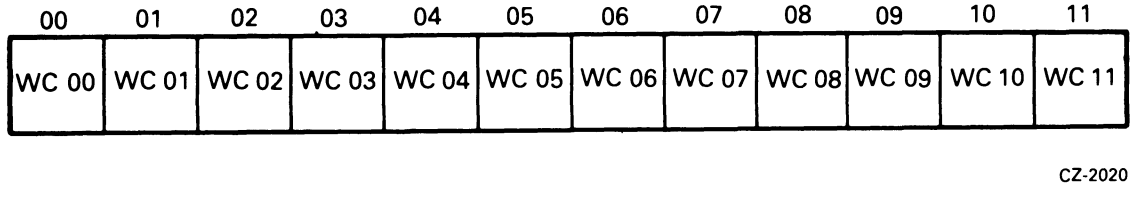


Figure 5-5 Word Count Register

5.2.5 Sector Address Register

The Sector Address (SA) register is a 6-bit register loaded by an RLSA command (6605) and read by an RRSA command (6614). Before executing a Read or Write operation, the sector address is loaded into the SA register (Figure 5-6).

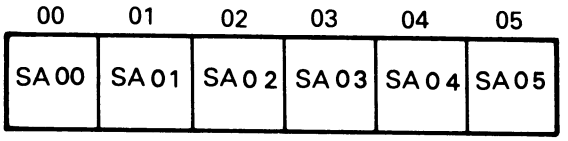


Figure 5-6 Sector Address Register

5.2.6 Error Register

The Error register is a 5-bit register that is read by the RRER command (6610). Bits 0:2 are cleared by initialize or when Command Register B is loaded. Figure 5-7 shows the bit layout and Table 5-6 describes the bit format.

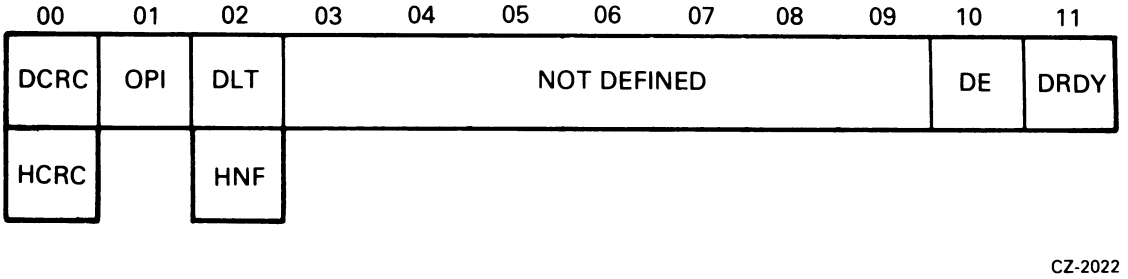


Figure 5-7 Error Register

Table 5-6 Error Register Bit Description

Bit	Name	Function
AC0	Data CRC (DRCR) or Header CRC (HCRC)	If OPI is cleared and this bit is set, the CRC error occurred in the data (DCRC). If OPI is set and this bit is also set, the CRC error occurred on the header (HCRC).
AC1	Operation Incomplete (OPI)	When set, this bit indicates that the current command was not completed within 200 ms. It is also used in conjunction with bits 0 and 2 of this register.
AC2	Data Late (DLT) or Header Not Found (HNF)	This bit is set during a write if the silo is empty and the word count is not yet zero (meaning that no word was available for writing). OPI will not be set.

Table 5-6 Error Register Bit Description (Cont)

Bit	Name	Function
AC2	Data Late (DLT) or Header Not Found (HNF)	This bit is set during a write if the silo is empty and the word count is not yet zero (meaning that no word was available for writing). OPI will not be set. This bit is set during a read if the silo is full and the word count is not yet zero (meaning that the word being read could not enter the silo). OPI will not be set. When this bit and OPI are both set, then a 200 ms timeout occurred while the controller was searching for the correct sector to read or write (no header compare - HNF).
AC0:2	Error Code	Summary **Error** / **Bits** 00 01 02 DLT 0 0 1 OPI 0 1 0 HNF 0 1 1 DCRC 1 0 0 HCRC 1 1 0
AC10	Drive Error (DE)	This bit is tied directly to the Drive Error interface line. When set, it indicates that the selected drive has flagged an error. The source of the error can be determined by writing a Get Status command. The DE bit is cleared with a Reset command to the drive.
AC11	Drive Ready (DRDY)	When set, this bit indicates that the selected drive is ready to receive a command. The bit is cleared when a Seek operation is initiated and set again when the Seek operation is completed.

5.2.7 Silo Data Buffer

The RRSI command (6615) is used to transfer the contents of the silo data buffer to the AC. The silo data buffer contains four different types of information.

5.2.7.1 Data Buffer Contents Following a Get Status Command – When a Get Status command is executed and a status word is returned to the controller, the contents of the silo data buffer appear as shown in Figures 5-8 and 5-9. Figure 5-8 shows the bit layout of the error/status bits for the first RRSI command. Figure 5-9 shows the bit layout of the remaining error/status bits when a second RRSI command is executed. Table 5-7 describes the error/status bits for the first data buffer read, and Table 5-8 describes the error/status bits for the second data buffer read.

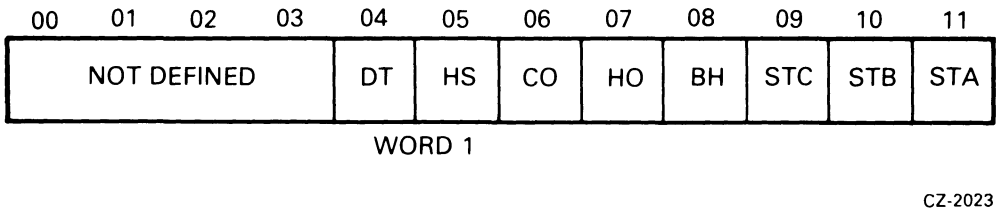


Figure 5-8 Silo Buffer for Status Word 1

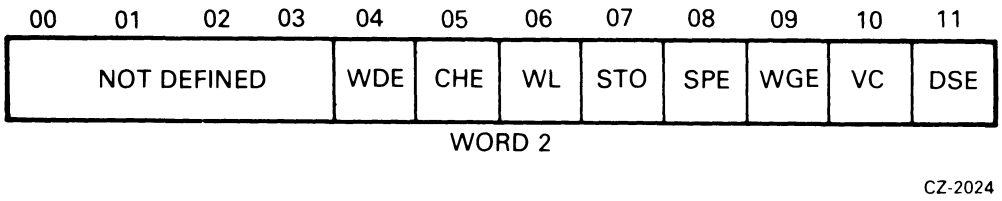


Figure 5-9 Silo Buffer for Status Word 2

5.2.7.2 Silo Data Buffer Contents Following a Read Header Command – When a Read Header command is executed, six 8-bit bytes are stored in the silo as six 12-bit words. The first two are header words and contain the sector address, head select, and cylinder address information. The second two words are zeros. The last two words contain the header CRC information. All six words are read by the RRSI command (6615) (Figure 5-10).

5.2.8 Register Summary

Figure 5-11 is a bit and function summary of the addressable registers.

5.3 CONTROLLER COMMANDS

The RL8A controller is capable of performing eight operations by responding to the function code in the low order three bits of Command Register B. In many cases it is necessary to load other registers prior to loading the function code into Command Register B. No registers should be loaded unless the controller is ready. This condition can be checked by using the appropriate IOT instruction that checks the function done status or by using the interrupt mode.

Table 5-7 Silo Data Buffer Word 1 of Get Status Command

Bit(s)	Name	Function
AC0:3	–	Undefined
AC4	Drive Type	A zero indicates an RL01; a one, an RL02.
AC5	Head Select (HS)	Indicates currently selected head. A zero indicates the upper head; a one, the lower head.
AC6	Cover Open (CO)	Set when the drive access cover is open or the dust cover is not in place.
AC7	Heads Out (HO)	A one indicates that the heads are over the disk; a zero indicates that the heads are home.
AC8	Brush Home (BH)	Set when the brushes are home.
AC9:11	State Bits	These bits define the state of the disk drive.

State Bit Definitions

Bit C	Bit B	Bit A	Definition
0	0	0	Load State
0	0	1	Spin-up
0	1	0	Load Heads
0	1	1	Brush Cycle
1	0	0	Seek (Track Counting)
1	0	1	Lock-on (keeping on track)
1	1	0	Unload Heads
1	1	1	Spin-down

Table 5-8 Silo Data Buffer Word 2 of Get Status Command

Bit(s)	Name	Function
AC0:3	–	Undefined
AC4	Write Data Error (WDE)	This bit is set when the write gate is on but no transitions were detected on the write data line.
AC5	Current Head Error (CHE)	This bit is set when write current is detected in the heads but the write gate has not been asserted.
AC6	Write Lock (WL)	Set when the drive is write-protected.
AC7	Seek Time Out Error (SKTO)	Set when the heads do not come on track in the required time during a seek operation, or when the heads drift off track and do not return within 1.5 seconds.
AC8	Spin Error (SPE)	Set when the spindle does not come up to speed within 40 seconds or when the spindle speed is too high.
AC9	Write Gate Error (WGE)	Set if write gate is asserted and one or more of the following conditions are true. 1. Drive is not "Ready to Read/Write" 2. Drive is write-protected 3. Drive is sensing a sector pulse 4. Drive has another error asserted
AC10	Volume Check (VC)	Set when a new cartridge has been loaded or when the power has been cycled down, then up. This bit is reset by a Reset command.
AC11	Drive Select Error (DSE)	Set when one or more drives has/have the same number (unit select plug) or have responded to the same number.

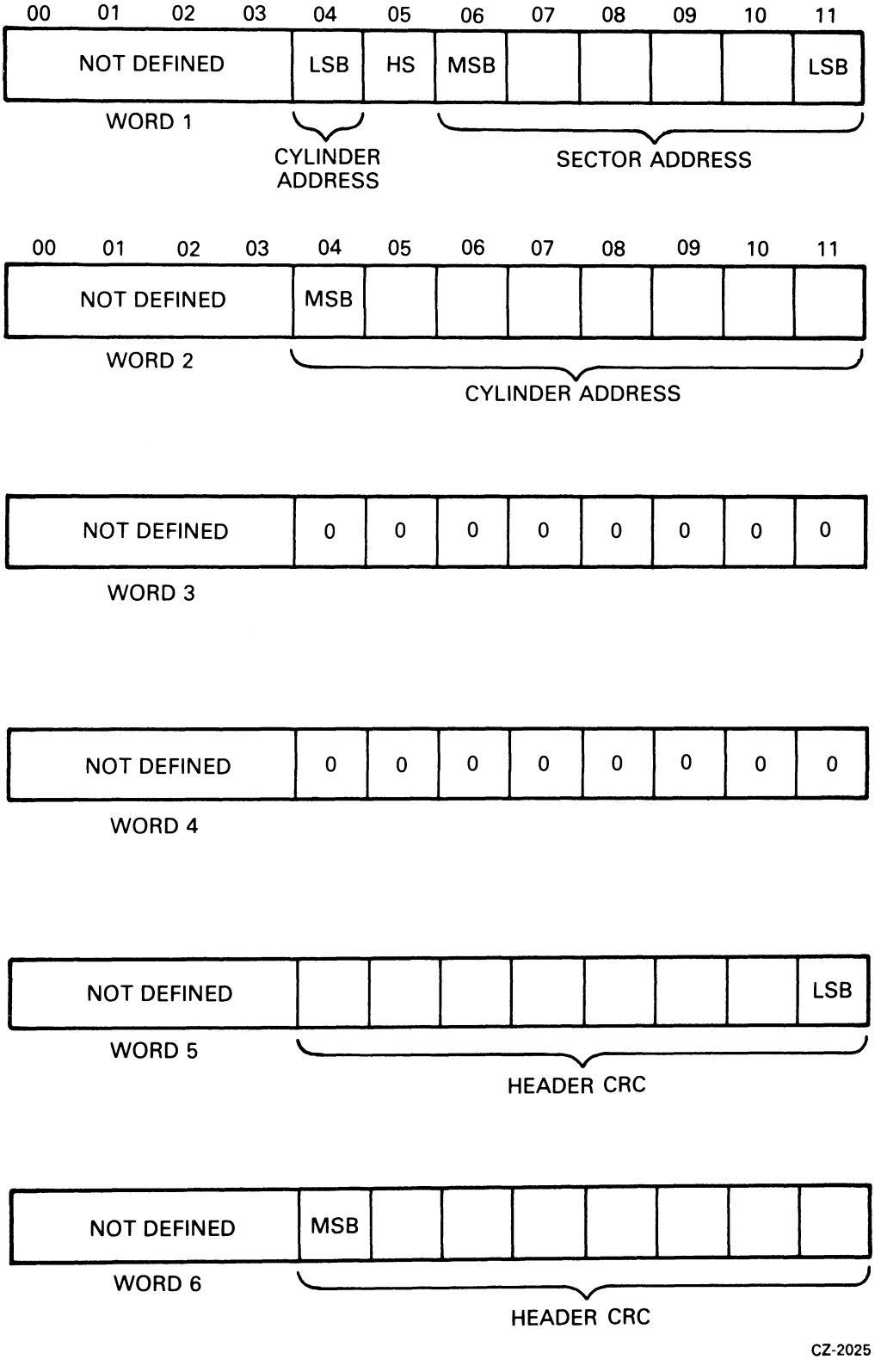
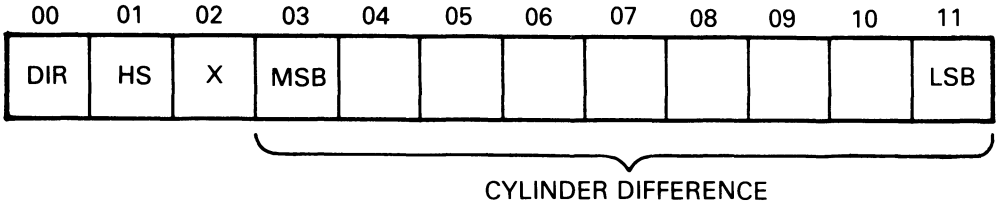
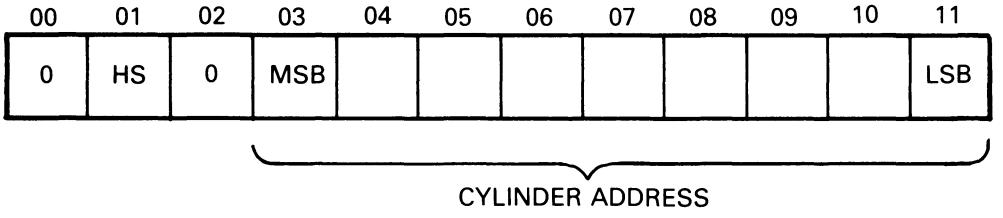


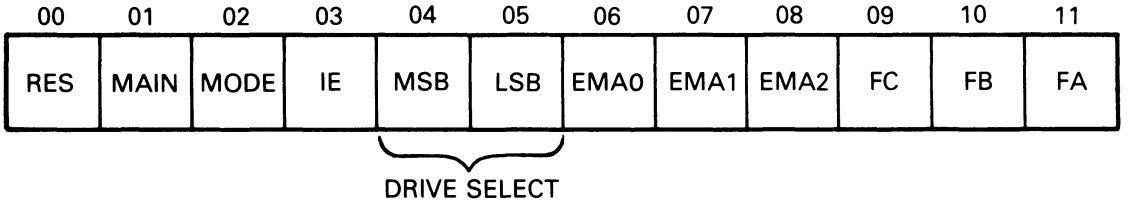
Figure 5-10 Silo Buffer for Header Words



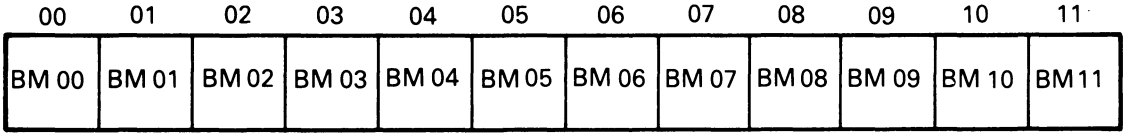
CZ-2016



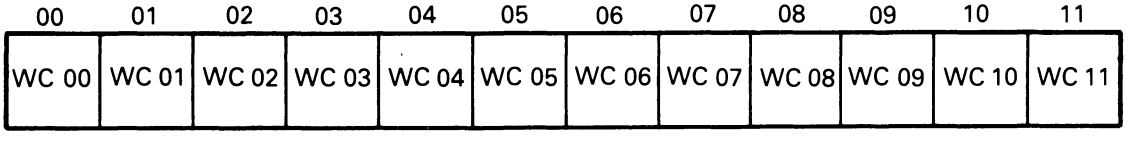
CZ-2017



CZ-2018

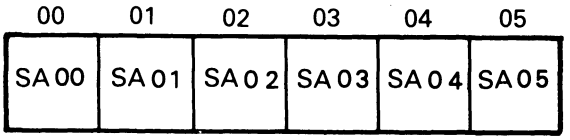


CZ-2019

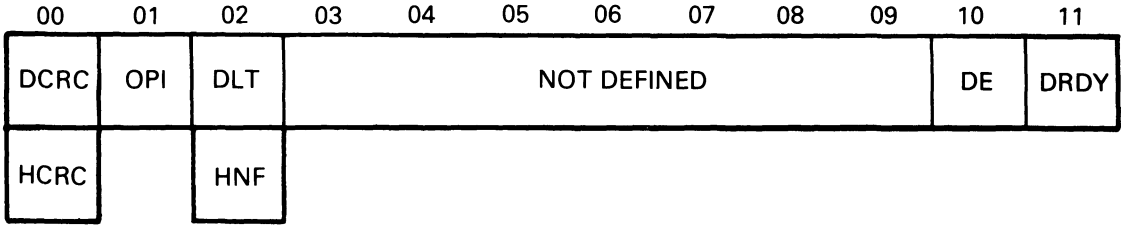


CZ-2020

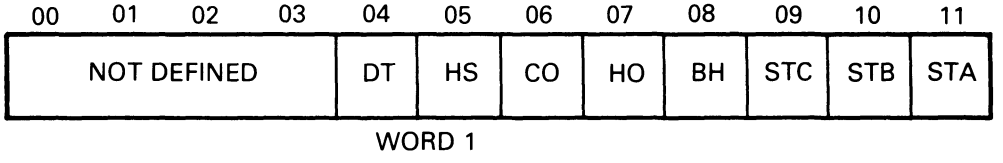
Figure 5-11 Register Summary (Sheet 1 of 3)



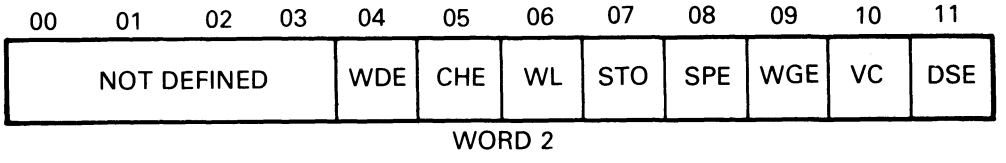
CZ-2021



CZ-2022



CZ-2023



CZ-2024

Figure 5-11 Register Summary (Sheet 2 of 3)

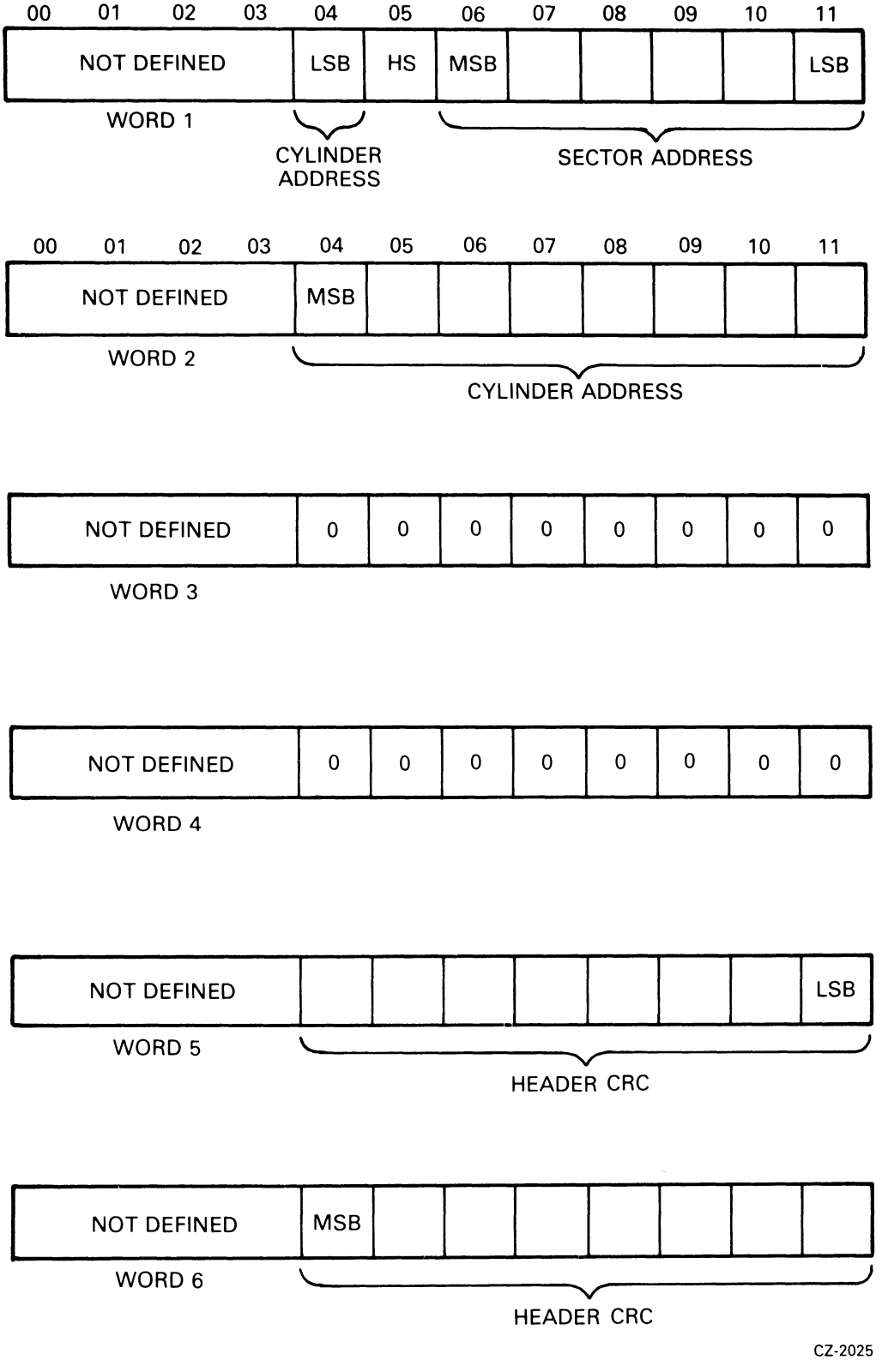


Figure 5-11 Register Summary (Sheet 3 of 3)

5.3.1 Maintenance Command

This command tests the controller by causing it to perform the following tasks.

- The controller requests a data word from memory via the OMNIBUS using the Break Memory Address (BRK MA) register as an address. When the controller receives this word, the BRK MA and the Word Count (WC) register are both incremented.

- The data word is bubbled through the silo, serialized and transferred (in 8-bit mode) through the CRC-generating logic where two more 8-bit bytes are appended. This 24-bit data stream goes through the write data precompensation logic and then is looped back and brought in as if it were read data from the drive. The data passes through the phase-locked loop and data separator logic and into the silo where it is converted back to parallel (eight bits per word), and bubbles through the silo to be available to the OMNIBUS.

- The controller requests three memory accesses and transfers the three words back to memory using the BRK MA register as a pointer. The BRK MA register and WC register are incremented for each transfer. The words are now available for the program to check for diagnostic purposes.

- The above processes repeat and the cycle continues until the WC register equals zero.

Prior to starting this command it is necessary to load the following registers.

- The BRK MA register should be loaded with the address of the first word of data to be transferred to the controller. The next three words of memory will receive three words of data from the controller.

- The WC register should be loaded with the desired count (in two's complement form). A complete cycle takes four counts.

- The Command Register B should be loaded with 10X0 or 14X0. This sets the mode bit to indicate 8-bit mode. The maintenance bit is a zero. The function code is 000. The remaining bits are irrelevant.

5.3.2 Reset Command

This command is used to reset all of the error bits in the selected drive unit. It does not reset any conditions in the controller nor does it cause any head movement in the drive. Prior to executing this command, the Sector Address Register and Command Register A must be cleared by using appropriate IOT instructions.

5.3.3 Get Status Command

The Get Status command reads the 16-bit status word from the selected drive and transfers it into two 8-bit bytes in two consecutive words in the silo. The computer can then extract them with two IOT RRSI instructions. The format of the bits are shown in Paragraph 5.2.7.1. Prior to performing a Get Status command it is necessary to clear both the Sector Address Register and Command Register A. When Command Register B is loaded with the function code, the appropriate drive-select bits should be set, the interrupt enable bit should be set if desired, and the mode bit must be set for 8-bit mode. The controller should be ready before performing any of these load register operations but the drive does not have to be ready.

5.3.4 Seek Command

The Seek command is used to move the heads or to select the other head on the selected drive. Prior to executing the seek command, the Sector Address Register should be cleared and Command Register A should be loaded with a direction bit, a head-select bit, and cylinder difference word. Command Register B is then loaded with the drive-select bits and the seek function code. The controller will send a command to the selected drive to cause it to start a seek operation. The controller will become ready and can then perform another command even though the drive is still seeking.

If the drive attempts to move the head past the innermost or outermost tracks, the head will retreat from the guard band and stop at the first even-numbered track it encounters.

5.3.5 Read Header Command

The Read Header command will read the first header encountered on the selected drive and load the header into six consecutive word locations in the silo, one 8-bit byte per word. The computer can then extract this information with IOT RRSI instructions. The format of the information is shown in Paragraph 5.2.7.2. A check is performed on the header that is read.

5.3.6 Write Data Command

The Write Data command requests data from memory, one word at a time, via the OMNIBUS using the DMA mode. It then transfers the data through the controller silo buffer to the selected drive. The data is written at the specified sector data area. This operation continues, incrementing both the Break Memory Address register and the Word Count register once for each OMNIBUS transfer until the Word Count register reaches zero.

Prior to starting this command it is necessary to position the head over the desired track using a Seek command. Then the registers should be loaded as follows:

- The Break Memory Address register with the address of the first memory word to be transferred,
- The Sector Address register with the address of the first sector to be written,
- The Word Counter register with the two's complement of the number of words to be transferred,
- The Command Register A with the head-select bit and the cylinder address word,
- The Command Register B with a mode bit (8-bit or 12-bit mode), interrupt-enable bit (optional), drive-select bits, extended memory address bits, and the Write Data function code.

The Write Data command will then read headers and perform header checks until the desired header is located. After the header is checked, the data is transferred. The header check includes a header CRC check. There is no implicit seek performed, so if the selected head is not positioned over the desired track, the desired header will not be found and an OPI error will occur. If only a partial sector is written, the remainder of the sector is written with all zeros. A CRC word (16 bits) is generated and written for each sector automatically. Since the word count is limited to 4096, this means that the maximum amount of data that can be written with one Write Data command is 16 sectors in 8-bit mode. If 12 bit mode is used, a maximum of 170 words (one sector) can be transferred. The hardware will not perform a spiral (mid-transfer) seek. Therefore, if data must be written that would overflow to the next track, it is necessary to write the data to the end of the track, seek to the next track, and then continue to write the remainder of the data.

5.3.7 Read Data Command

The Read Data Command will cause the controller to read data from the selected drive. It will read from the track that is currently under the selected head, starting at the specified sector. The data is transferred through the controller silo buffer. The controller requests DMA transfers to memory via the OMNIBUS. The Break Memory Address and the Word Count registers are incremented once for each 12-bit word transferred over the OMNIBUS. When the Word Count register reaches zero, the Read Data command is terminated. Prior to starting the Read Data command, the head should be positioned over the desired track with a Seek command. Load the registers as follows:

- The Break Memory Address register with the address of the first location in memory to which the data is to be transferred,
- The Sector Address register with the address of the first sector from which the data is to be read,
- The Word Counter register with the two's complement of the number of words of data to be read,
- The Command Register A with a head-select bit and a cylinder address word,
- The Command Register B with a mode bit and interrupt-enable bit (optional) drive-select bits, extended memory address bits, and the function code for Read Data.

The Read Data command then reads headers, comparing them to the desired disk address. The data transfer begins when the desired header is found. The header checks include header CRC checks. There is no implicit seek, so if the selected head is not over the desired track, the desired header will not be found and an OPI error will occur.

The RL8A cannot perform a spiral (mid-transfer) seek. If a block of data to be read passes the end of a track and continues on the other surface or on the next cylinder, it is necessary to program a Read Data just to the end of the track. The drive must then Seek to the next track and then continue reading data.

A CRC check is performed on each sector during a Read Data operation.

5.3.8 Read Data without Header Check Command

This command is the same as a Read Data command except that no header check is performed. The next header read is considered a match so that sector is the first sector read. Since no header check takes place, the header CRC is performed.

5.3.9 Maintenance Bit

The maintenance bit in Command Register B enables a path for the serial information leaving the DA register. When this bit is set, the data that is going out to the drive is looped back and shifted into the silo. The data bubbles through the silo and becomes accessible (as two 8-bit bytes) to IOT RRSI instructions. The program can then monitor the operation of the DA register which is not a directly addressable register. This feature must be used only with Reset, Get Status, and Seek commands. Because the DA register is a 16-bit register, the 8-bit mode bit should be set. This insures that the contents of the DA register fit into two 8-bit bytes. The contents of the DA register and the two silo words are illustrated in Figure 5-12. During the loading of the DA register (which occurs on every command), there is more than one input to some of the bit positions. These inputs are ORed together. Normally, Status Register A is cleared before any Reset, Get Status, or Seek command and Control Register A is cleared before any Reset or Get Status command. It is possible to test all the bits in the DA register by using selected patterns in Control Register A and Status Register A.

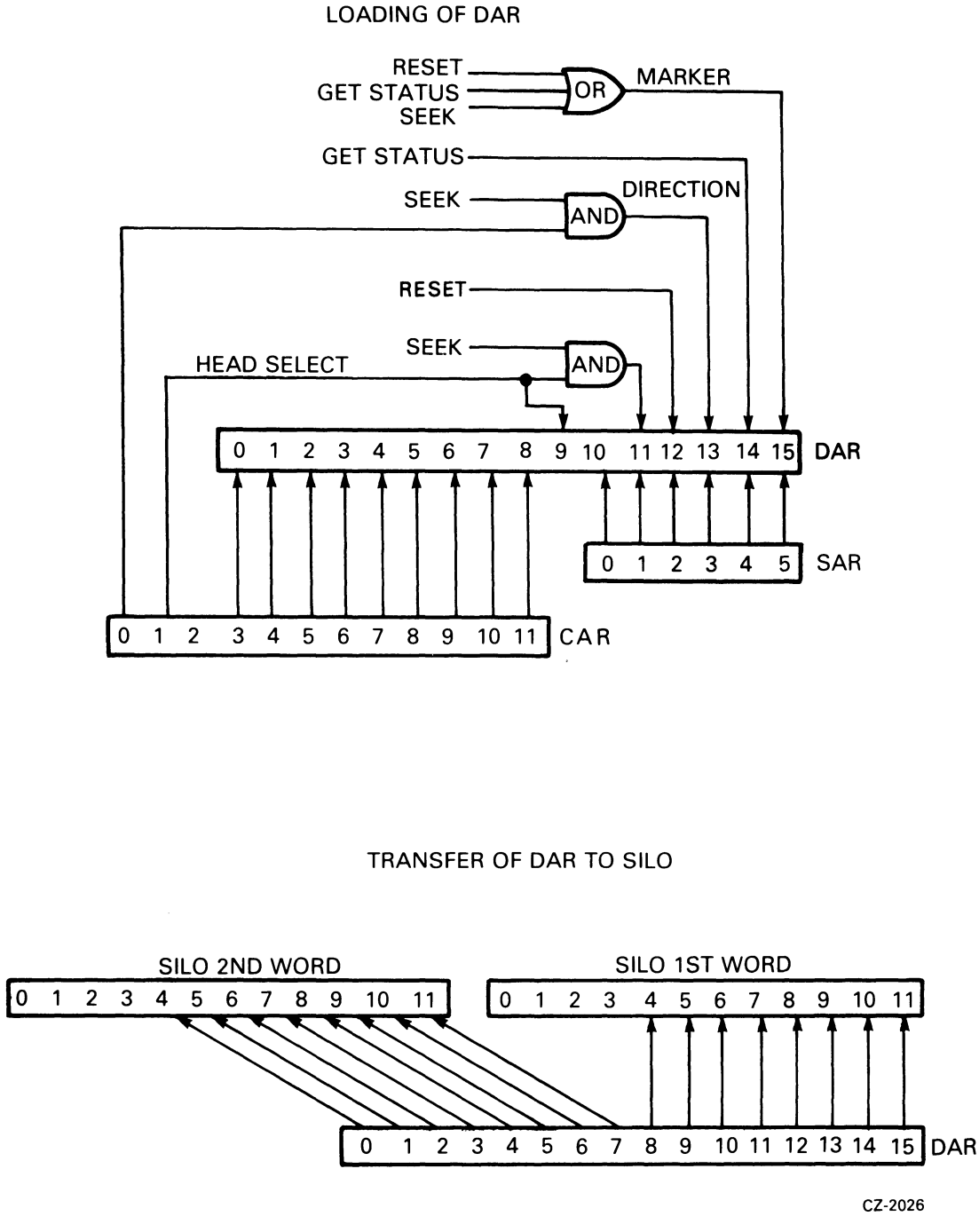


Figure 5-12 Maintenance Mode Bit

5.4 OPERATIONAL CONSIDERATIONS

5.4.1 8-Bit Mode Versus 12-Bit Mode

The disk cartridge is formatted in 8-bit bytes. For instance, the header contains a 16-bit word address, another 16-bit word, then a 16-bit header. The data area is 256 8-bit bytes and the data area CRC is 16 bits. None of these areas are evenly divisible by 12, which is the PDP-8 word length. Therefore, the RL8A controller has the capability of operating in either 8-bit mode or 12-bit mode.

When reading in 8-bit mode, the serial data from the disk is broken into 8-bit bytes and put into the silo with eight bits per word. Since the silo is 12 bits wide, the data goes into the eight low order bit positions and zeros are put into the remaining four high order bit positions. That is the format used when the computer transfers a 12-bit word from the silo to the CPU accumulator or to memory. The 8-bit mode is necessary when performing a Read Header, Get Status, or Maintenance command where 16 bits of data are read. Otherwise, information would be lost.

The 8-bit mode can be used for data on the disk. In such a case, 256 8-bit bytes are read from each sector and transferred to memory as 8-bit words. In some cases, this may be an advantage. For example, if 8-bit ASCII data is being handled, the 8-bit mode is preferable to the 12-bit mode. In most cases, however, the 8-bit mode wastes 33% of the memory space. Because the 12-bit mode uses 12-bit words it uses less memory. In the 12-bit mode, each sector contains 170 words with only 8 wasted bits at the end of each sector.

In the 12-bit mode, the RL8A controller hardware blocks data into 170 words per sector. The operating system for the PDP-8 uses only 128 words per sector, so that while memory is used more efficiently, some disk space is wasted.

5.4.2 Interrupt

The RL8A will interrupt the processor if the Interrupt Enable bit is set and the controller is done. If an error occurs during an operation, the done condition is set.

5.4.3 Seek Operation

If the program does not keep track of the current position of the head (cylinder and surface), and it is desired to read or write from a particular area from the disk, it is necessary to:

- Read Header to obtain the current position of the head,
- Calculate the difference (if any) from the desired position,
- Issue a Seek with the proper difference, direction and head-select information.

5.4.4 Overlapped Seeks

Since a Seek operation does not involve data transfer, it is possible to have one drive seeking while another is transferring data. Only one drive at a time can transfer data, but up to four drives can be seeking simultaneously.

5.4.5 Recovery of Data with Bad Headers

Function 7, Read Data Without Header Check, allows the recovery of data with unreadable headers. If HNF or HCRC errors are repeatedly encountered on a particular sector, and the data is not recoverable by the standard Read command, proceed as follows. Read successive headers until the sector preceding the bad sector is found. Then, within 300 microseconds, issue a Read Data Without Header Check. The data portion of the next sector will be read without either header compare or header CRC check. Data CRC errors will be reported.

5.4.6 Non-Interchangability of Disk Cartridges

5.4.6.1 RL01K/RL02K – These two types of cartridges are physically interchangable but not functionally interchangeable. If a cartridge is installed on the incorrect type of drive, no physical damage will take place and data will not be destroyed. However, the unit will not operate in a normal manner. The symptoms exhibited depend upon the program running at the time. If the system is exhibiting abnormal characteristics, the operator should ensure each drive contains the correct type of cartridge.

5.4.6.2 RL8A/RL11/RLV11/RLV12 – RL01K cartridges are interchangeable with other RL01K cartridges assuming that the RL8A has written the cartridges in 8-bit mode. RL02K cartridges are interchangeable with other RL02K cartridges under the same condition.

5.4.7 Use of Two RL8A Controllers

A PDP-8 system can be configured with two RL8A controllers to increase the capacity of the system up to eight drives. However, if both controllers are trying to perform data transfers at the same time, the throughput capacity of the OMNIBUS may be exceeded. In this case, conflicts (DLTs) will occur.

5.5 ERROR RECOVERY

There are several errors that can be detected and flagged in the RL01/RL02 subsystem. Some of them are considered recoverable. In this case, if the operation is retried, it is possible that the error will not recur and use of the subsystem can continue. Some of the errors are considered fatal, however, because retries may cause damage to the data, media, or equipment. The errors are listed with the recommended reaction in Table 5-9.

The nature of these errors should be considered when determining how many times to retry the operation. For instance, a DLT error could be a hardware system failure but it could also be the result of bus activity due to other I/O devices exceeding the throughput capability. In the latter case, it is likely that the operation will be successful on the first retry. The rate of occurences is a good indicator of overall system performance and an error logging routine should count the rate at which errors occur. A general increase in the rate of DLT errors could indicate that system usage is approaching its throughput capacity in its present configuration.

Another example of applying practical reaction to an error is the handling of an HNF error. It should be retried once. If it recurs, then the head may not be positioned over the correct track. If a Read Header operation is performed and the address from the media is examined, the current cylinder and head can be determined to see if it is a position problem. If not, then possibly there is a bad spot on the media. If there is a bad header, that sector address should be entered into the Bad Sector File and the software should avoid using the original sector.

Whenever an error occurs, the program should log it, along with the contents of the registers, the status of the unit, and whether or not a retry was successful. The more complete the error log, the easier it is to diagnose the cause of errors.

Table 5-9 Errors

Controller Errors	Recommended Reaction
OPI	Retry some practical number of times.
DCRC/HCRC	Retry. Be sure to record the contents of the DA register.
DLT/HNF	Retry. If an HNF error, perform a Read Header and verify cylinder.
Drive Error	Perform a Get Status and check the bits listed below.
Drive Errors	**Recommended Reaction**
DSE	Retry once before notifying operator to verify UNIT SELECT plug.
WGE	Retry.
SPE	Retry.
SKTO	Retry. Wait for 1.5 sec after Reset.
CHE	Fatal. Do not retry.
WDE	Fatal. Do not retry.

5.6 DIFFERENCE SUMMARY (RK05 AND RL01/RL02)

This section may be helpful to users who have used DIGITAL's RK05 disk cartridge subsystem. It points out the differences between programming the RK05 subsystem and programming the RL01/RL02 subsystem.

In general, the RK05 subsystem provides more hardware support of functions while the RL01/RL02 subsystem requires that the software provide some of the functionality. The major differences are explained below.

5.6.1 Spiral Read/Write or Mid-Transfer Seeks

A spiral read/write is a transfer of data that continues past the end of a track. The RK05 subsystem provides hardware support for this by using the hardware to detect the end-of-track condition. The hardware will cause a mid-transfer seek to the next track and then restart the read/write operation at sector 0 of the next track. Note that this seek is either a head switch from the upper surface to the lower surface on the same cylinder with no head positioner movement, or a switch from lower surface to upper surface with a positioner movement to the next cylinder. The RL01/RL02 subsystem hardware cannot handle this. If a read/write operation continues past the 40th sector, the sector counter in the DA register advances to 50 (octal), which is illegal and therefore sets the OPI error flag. It is necessary for the software to 1) prevent this from occurring by calculating the remaining area left versus the amount of data left before the operation or 2) to detect that it has occurred. The software must initiate a separate seek function and initiate a continuance of the read/write function. A head switch from the upper to the lower surface without a positioner movement is considered a Seek in the RL01/RL02 subsystem. After a head switch, the positioner will seek the center of the new track.

5.6.2 Implicit Seeks Versus Explicit Seeks

The RK05 subsystem can perform either implicit or explicit seeks. An explicit Seek is a software-directed seek operation. An implicit Seek is a seek initiated by the hardware at the beginning of a read/write operation if the desired position is different from the present position. The RL01/RL02 subsystem cannot do an implicit seek. The software must ensure that the positioner is over the desired cylinder and that the desired head is selected before starting a read/write operation.

5.6.3 Recalibrate

The RK05 subsystem has a return-to-zero or recalibrate function which causes the positioner to move to cylinder 0. There is no similar function in the RL01/RL02 subsystem. An explicit seek to cylinder zero must be performed. If the current cylinder address is not known and the drive is commanded to seek beyond the outer guard band, this guard band will be detected and the head will retreat to cylinder zero.

5.6.4 Bad Sector File

There is a bad sector file feature on each RL01/RL02 disk cartridge. Its use is explained in Paragraph 1.6. There is no standard Bad Sector File used with the RK05.

5.6.5 Reformatting

The RK05 cartridge can be reformatted in the field while the RL01K/RL02K cartridges cannot. The embedded servo information and Bad Sector File features greatly reduce the need to reformat in the field.

5.6.6 Seek Interrupt

The RK05 will provide two interrupts as the result of a seek operation. The first interrupt occurs as soon as the controller has caused the drive to start its movement, indicating that the controller is free to handle another function. The second interrupt occurs when the drive finishes the seek movement. The RL01/RL02 subsystem does not provide the second interrupt. Thus, the software must perform the proper monitoring of the drive to determine when the seek has been completed.

APPENDIX A
RL11 CONFIGURATION AND INSTALLATION CONSIDERATIONS

A.1 SPC CONSIDERATIONS

The RL11 is a Small Peripheral Controller (SPC) but does not unconditionally fit into any SPC slot. Early SPCs were always quad-height modules or combinations of smaller (single or dual) modules that involved only four rows. Thus, the standard pin assignments applied only to rows C, D, E, and F on a hex-height modules and therefore required that rows A and B be vacant since some SPC slots use rows A and B for UNIBUS cables or power connectors. Some hex-height options require standard UNIBUS pinning on rows A and B and some require Modified UNIBUS Device (MUD) pinning. In the case of the RL11, the only connections used on rows A and B are the +5v and ground. Thus, these rows can be either standard UNIBUS or MUD pinning.

The early SPCs did not utilize Direct Memory Access (DMA) data transfers to/from memory and therefore those signals were not part of the origianl SPC pin assignments. Some of the newer options, such as the RL11, do utilize DMA transfers. There is a new pin assignment called SPC PRIME that includes these signals. If the RL11 is to be used in an older (non SPC-PRIME) slot, then it is necessary to ensure that the following signals are wired on the backplane.

- Pin CA1 – NPG In
- Pin CB1 – NPG Out
- Pin FJ1 – NPR
- Pin CV1 – AC LO
- Pin CU1 – +15v

If the slot has SPC PRIME pinning, then another precaution must be taken. NPG continuity is maintained across an empty SPC PRIME slot by a backplane jumper from pin CA1 to pin CB1. This jumper must be removed whenever a DMA-type option is installed, such as an RL11, and the jumper must be added if the module is removed. This consideration is in addition to the normal Bus Grant Continuity card used in row D of all empty SPC slots.

A.2 CONFIGURATION CONSIDERATIONS

When configuring a UNIBUS system for the best priority assignments, two characteristics of a peripheral option must be taken into consideration. These are the peak word transfer rate and the T1 time (T1 time is a function of the peak transfer rate and the silo size). The RL11 has a peak transfer rate of 256 kHz (3.9 microseconds/word) and a T1 time of 62.4 microseconds. This dictates its position in the priority scheme. The recommended priority scheme is listed below.

CPU
- Memory
- RK11/RK05
- TM11/TU10
- TC11/TU56
- RL11/RL01-RL02
- RJS04
- RM02
- RJP04
- RK611/RK06-RK07
- RP11C/RP03
- RJS03
- TJU16
- RF11/RS11

DB11

Other general configuration rules are:

- On a PDP-11 UNIBUS, a combination of two disk subsystems and a tape or floppy disk subsystem is considered maximum.
- On a PDP-11/70 system, on UNIBUS disk subsystem is considered maximum if there are MASSBUS disks.
- A disk subsystem should not be installed beyond a bus expander.

RL01/RL02 DISK SUBSYSTEM
USER GUIDE
EK-RL012-UG-005

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